Data Sheet

ADM6100

Half-Duplex Power-over-Data (PoD) Transceiver with RS-485 Backwards Compatibility

FEATURES

- PD-Link® Encoding Method Featuring Physical Layer PoD Encoding
  - DC Balance Maintained at Physical Layer
  - Up to 2.5Mbps Data Rate in PoD Mode
  - Resistor Controlled Channel Bandwidth
  - Receiver Gain Control
- RS-485 Backwards Compatibility Mode
  - Up to 20Mbps Data Rate in RS-485 Mode
- Polarity Agnostic Operation
- High ESD Protection
  - ±25kV HBM ESD per JEDEC JS-001
  - ±15kV Air-Gap ESD per IEC 61000-4-2
  - ±10kV Contact ESD per IEC 61000-4-2
- ±25V Fault Protection on Transceiver Pins
- True Fail-Safe Receiver Prevents False Transition on Receiver Input Short or Open Events
- Hot-Swap Capability Eliminates False Transitions During Power-Up or Hot Insertion
- −40°C to +125°C Operating Temperature
- 28-Pin 4mm × 4mm TQFN

FUNCTIONAL BLOCK DIAGRAM

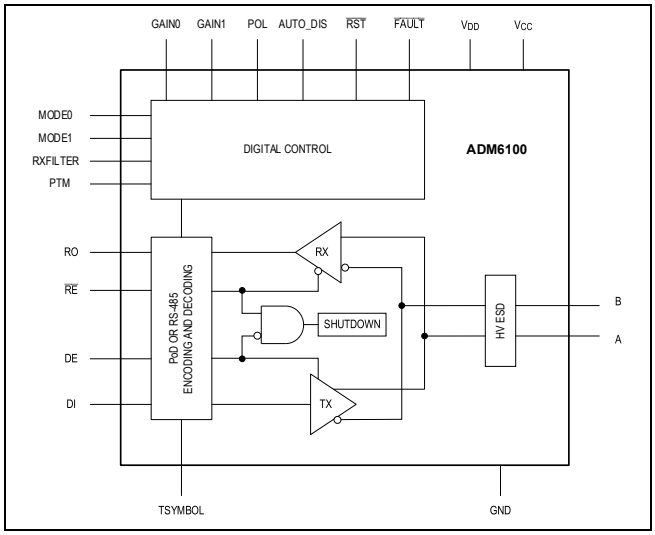


Figure 1. ADM6100 Functional Block Diagram

GENERAL DESCRIPTION

The ADM6100 half-duplex PoD transceiver features the PD-Link encoding, a physical layer (PHY) specific robust channel encoding method that allows for software-agnostic PoD communications, which utilizes only a single pair of wires while minimizing the size and cost of external components. The PD-Link channel bandwidth is configurable, which allows system designers to optimize trade-offs among data rate, cable length, and size of external magnetic components required for PoD implementation. The configurable channel bandwidth allows the use of smaller magnetics even with very low system data rate. The PD-Link encoding used by the ADM6100 enables PoD implementation without requiring any protocol changes or constraints in software layers beyond the physical layer.

The ADM6100 is used to replace standard RS-485 transceivers to provide PoD capability to point-to-point or multinode systems. In the case that RS-485 backwards compatibility is required, the PD-Link encoding feature can be bypassed to enable the device to communicate with standard RS-485 transceivers on the network.

The ADM6100 features PoD receiver gain control to support longer cable lengths across varying cable quality. High ESD protection and up to ±25V fault protection on the transceiver pins ensure robust communication in harsh industrial environments.

The ADM6100 is available in 4mm × 4mm 28-pin TQFN package and is rated to operate over −40°C to +125°C industrial temperature range.

APPLICATIONS

- Building Automation
- HVAC Systems
- Building Access Systems
- Building Intercom Systems
- Industrial Automation Applications

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SIMPLIFIED APPLICATION DIAGRAM

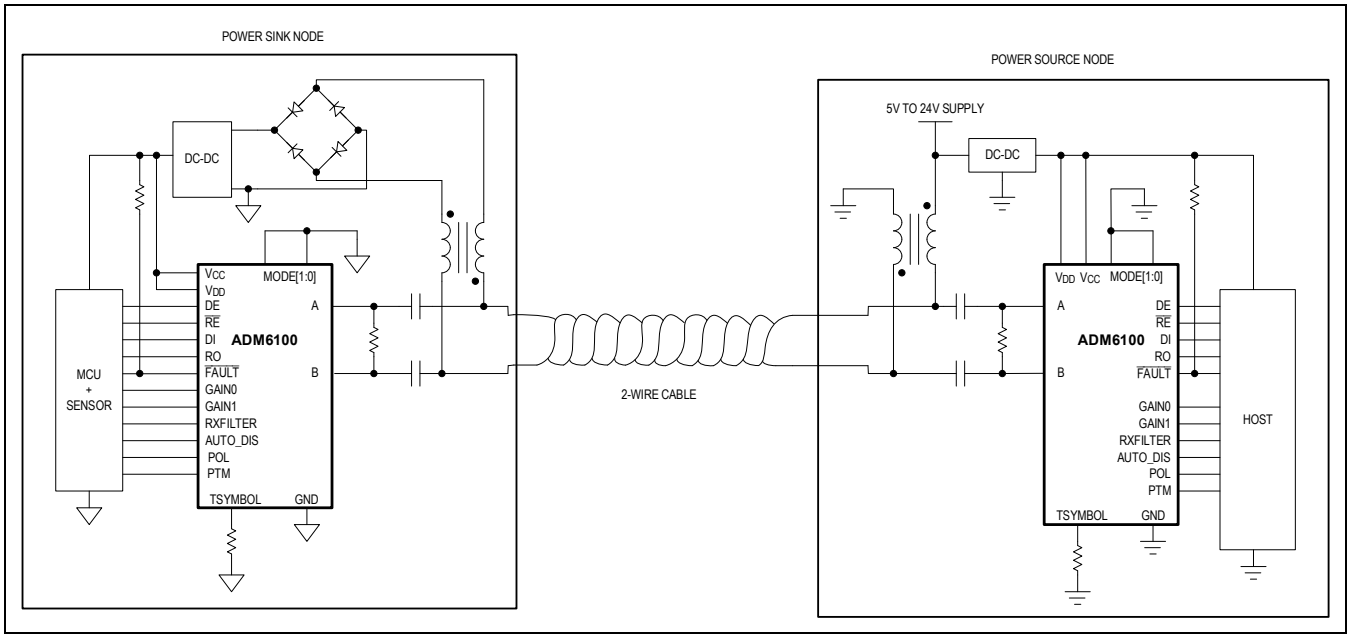


Figure 2. ADM6100 Simplified Application Diagram for PoD Modes

TABLE OF CONTENTS

Features 1
Functional Block Diagram 1
General Description 1
Applications 1
Simplified Application Diagram 2
Revision History 4
Specifications 5
Test and Timing Diagrams 12
Test and Timing Diagrams for RS-485 Mode 12
Test and Timing Diagrams for PoD Modes 15
Absolute Maximum Ratings 18
Thermal Resistance 18
Electrostatic Discharge (ESD) Ratings 19
ESD Ratings for ADM6100 19
ESD Caution 19
Pin Configurations and Function Descriptions 20
Typical Performance Characteristics 23
Theory of Operation 28
Power-over-Data (PoD) Operation 28
RS-485 Mode 28
Power Supply 29
Transceiver Operation 29
Driver and Receiver Enable Pins 29
Operation Modes 29
Function Tables 31
TSYMBOL Configuration 32
Receiver Gain Control in PoD Modes 34
Receiver Filter Operation in PoD Modes 34
Initialization and Polarity Configuration 34
FAULT Pin Operation 38
Fault Protection 38
True Fail-Safe 38
Hot-Swap Inputs 38
Low-Power Shutdown 39

Thermal Shutdown Protection 39
ESD Protection 39
Human Body Model (HBM) 39
IEC 61000-4-2 40
Applications Information 42
Power Supply Decoupling 42
PCB Layout Recommendations 42
Multidrop Network 42
Termination 43
AC-Blocking Inductors and AC Coupling Capacitors 44
Outline Dimensions 45
Ordering Guide 48

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
Sp0	6/26	Initial release	—
A	10/26	Removed the word *Patented* in the *Features* section. Updated the *TSYMBOL* pin description in *Table 6* in the *Pin Configurations and Function Descriptions* section. Updated *Table 7* and the *Operation Modes* section. Updated *Table 10* and *Table 11* in the *Function Tables* section. Removed the *Receiver Second Pulse Decoding* setion. Updated *Figure 39* and the *TSYMBOL Configuration* section. Updated *Figure 42*, *Figure 43*, and the *Initialization and Polarity Configuration* section.	1, 22, 30, 32 to 38

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{DD} = +3.0V to +5.5V, V_{CC} = +4.5V to +5.5V, GND = 0V, T_A = −40°C to +125°C, unless otherwise specified. Typical values are at V_{DD} = +3.3V, V_{CC} = +5V, and T_A = +25°C.) ([1])

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Power Supply						
Supply Voltage	V_{CC}		4.5		5.5	V
Digital Interface Supply Voltage	V_{DD}		3.0		5.5	V
Digital Interface Supply Current	I_{DD_RS485}	DI and RO switching at 20Mbps, DE = V_{DD}, $\overline{RE}$ = 0V, no load, MODE[1:0] = 0x3		2		mA
	I_{DD_PoD}	DI and RO switching at 2.5Mbps, DE = V_{DD}, $\overline{RE}$ = 0V, no load, MODE[1:0] ≠ 0x3		100		µA
	I_{DD_IDLE}	All digital input pins at GND or V_{DD}, no switching on A or B			10	µA
RS-485 Mode Supply Current	I_{CC_RS485}	DI switching at 20Mbps, DE = V_{DD}, $\overline{RE}$ = 0V, no load, MODE[1:0] = 0x3		40	54	mA
		DI idle (no switching), DE = V_{DD}, $\overline{RE}$ = 0V, no load, MODE[1:0] = 0x3		4.6	7	mA
PoD Mode Supply Current	I_{CC_PoD}	DI switching at 2.5Mbps, DE = V_{DD}, $\overline{RE}$ = 0V, no load, MODE[1:0] ≠ 0x3, T_{SYMBOL} = 33kΩ		13.5	18	mA
		DI idle (no switching), DE = V_{DD}, $\overline{RE}$ = 0V, no load, MODE[1:0] ≠ 0x3, T_{SYMBOL} = 33kΩ		9	12	mA
Analog Shutdown Supply Current	I_{CC_SHDN}	DI idle (no switching), DE = 0V, $\overline{RE}$ = V_{DD}, no load			10	µA
RS-485 Mode Driver (MODE[1:0] = 0x3)						
Differential Driver Output	$\lvert V_{OD} \rvert$	R_L = 54Ω (*Figure 3A*)	1.5			V
		R_L = 60Ω (*Figure 3A*)	1.5			V
		R_L = 100Ω (*Figure 3A*)	2			V
	$\lvert V_{OD_3B} \rvert$	R_L = 60Ω || (375Ω + 375Ω) with V_{CM} set from −7V to +12V (*Figure 3B*)	1.5			V
Change in Magnitude of Differential Driver Output Voltage	ΔV_{OD}	R_L = 54Ω or 60Ω or 100Ω (*Figure 3A*) ([2])	−200		+200	mV
	ΔV_{OD_3B}	R_L = 60Ω || (375Ω + 375Ω) with V_{CM} set from −7V to +12V (*Figure 3B*) ([2])	−200		+200	mV

(V_{DD} = +3.0V to +5.5V, V_{CC} = +4.5V to +5.5V, GND = 0V, T_A = −40°C to +125°C, unless otherwise specified. Typical values are at V_{DD} = +3.3V, V_{CC} = +5V, and T_A = +25°C.) ([1])

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω or 60Ω or 100Ω (*Figure 3A*)	1	V_{CC}/2	V_{CC}	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 54Ω or 60Ω or 100Ω (*Figure 3B*) ([2])	−200		+200	mV
Single-Ended Driver Output Voltage High	V_{OH}	A or B output, output is high, I_{SOURCE} = 3mA	2.4	V_{CC} − 0.2		V
Single-Ended Driver Output Voltage Low	V_{OL}	A or B output, output is low, I_{SINK} = 3mA			200	mV
Average Driver Short-Circuit Output Current	I_{AVG_SCDR}	0V ≤ (V_A or V_B) ≤ V_{CC}	−250		+250	mA
PoD Mode Driver (MODE[1:0] ≠ 0x3)						
Differential Driver Output	$\lvert V_{OD} \rvert$	R_L = 54Ω (*Figure 11*)	1.5			V
		R_L = 60Ω (*Figure 11*)	1.5			
		R_L = 100Ω (*Figure 11*)	2			
Change in Magnitude of Differential Driver Output Voltage	ΔV_{OD}	R_L = 54Ω or 60Ω or 100Ω (*Figure 11*)	−200		+200	mV
Driver Idle Output Voltage	V_{IDLE}	No switching, DI = 0V or V_{DD}	0.45 × V_{CC}	0.5 × V_{CC}	0.55 × V_{CC}	V
Single-Ended Driver Output Voltage High	V_{OH}	A or B output, output is high, I_{SOURCE} = 45mA	V_{CC} − 1.5			V
Single-Ended Driver Output Voltage Low	V_{OL}	A or B output, output is low, I_{SINK} = 45mA			1.2	V
RS-485 Mode Receiver (MODE[1:0] = 0x3)						
Input Current (A, B)	I_A, I_B	DE = 0, 0V ≤ V_{CC} ≤ 5.5V, V_{CM} = −7V to +12V	−73		+125	µA
Receiver Input Resistance	R_{IN}	DE = 0, −7V ≤ V_{CM} ≤ +12V	96			kΩ
Common-Mode Voltage Range	V_{CM}	*Figure 3B*	−7		+12	V
Receiver Differential Threshold Voltage Rising	V_{TLH}	−7V ≤ V_{CM} ≤ +12V			−50	mV

(V_{DD} = +3.0V to +5.5V, V_{CC} = +4.5V to +5.5V, GND = 0V, T_A = −40°C to +125°C, unless otherwise specified. Typical values are at V_{DD} = +3.3V, V_{CC} = +5V, and T_A = +25°C.) ([1])

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Receiver Differential Threshold Voltage Falling	V_{THL}	−7V ≤ V_{CM} ≤ +12V	−200			mV
Receiver Input Hysteresis	ΔV_{TH}	−7V ≤ V_{CM} ≤ +12V		20		mV
Differential Input Capacitance	C_{A_B}	Measured between A and B, f = 1MHz		10		pF
PoD Mode Receiver (MODE[1:0] ≠ 0x3)						
Input Current (A, B)	I_A, I_B	DE = 0, 0V ≤ V_{CC} ≤ 5.5V, 0V ≤ V_A ≤ 5.5V, V_A = V_B	−28		+28	µA
Receiver Input Resistance	R_{IN}		96			kΩ
Absolute Value of Receiver Differential Threshold to Start Detection	$\lvert V_{TH_DET} \rvert$	GAIN[1:0] = 0x0 ([3]), $R_{TSYMBOL}$ = 33kΩ	540	805	1100	mV
		GAIN[1:0] = 0x1 ([3]), $R_{TSYMBOL}$ = 33kΩ	460	635	790	
		GAIN[1:0] = 0x2 ([3]), $R_{TSYMBOL}$ = 33kΩ	240	320	400	
		GAIN[1:0] = 0x3 ([3]), $R_{TSYMBOL}$ = 33kΩ	100	155	210	
Differential Input Capacitance	C_{A_B}	Measured between A and B, f = 1MHz		10		pF
Logic Output (RO, $\overline{\text{FAULT}}$)						
RO Output Logic High Voltage	V_{OH}	I_{SOURCE} = 3mA	V_{DD} − 0.4			V
RO Output Logic Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
Leakage Current	I_{OZR}	0V ≤ V_{RO} ≤ V_{DD}	−1		+1	µA
Short-Circuit Current	$\lvert I_{OSR} \rvert$	0V ≤ V_{RO} ≤ V_{DD}		200	360	mA
$\overline{\text{FAULT}}$ Open-Drain Logic Low	V_{ODL}	I_{SINK} = 2mA			0.3	V
$\overline{\text{FAULT}}$ Open-Drain Leakage	I_{ODL}	0V ≤ $V_{\overline{FAULT}}$ ≤ 5.5V, output not asserted			1	µA
Logic Input (DE, $\overline{\text{RE}}$, DI, POL, MODE1, MODE0, PTM, GAIN1, GAIN0, $\overline{\text{RST}}$, RXFILTER, AUTO_DIS)						
Input Logic High Voltage	V_{IH}		0.7 × V_{DD}			V
Input Logic Low Voltage	V_{IL}				0.3 × V_{DD}	V
Input Hysteresis	V_{HYS}			100		mV
Input Leakage Current	I_{IN}		−1		+1	µA

(V_{DD} = +3.0V to +5.5V, V_{CC} = +4.5V to +5.5V, GND = 0V, T_A = −40°C to +125°C, unless otherwise specified. Typical values are at V_{DD} = +3.3V, V_{CC} = +5V, and T_A = +25°C.) (1)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Protection						
Thermal Shutdown Threshold	T_{SHDN}	Temperature rising		160		°C
Thermal Shutdown Hysteresis	T_{HYST}			12		°C
Fault Protection (Pin A and Pin B to GND)			−25		+25	V

1 All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

2 ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when DI changes state.

3 For the receiver to recognize the leading edge of the first pulse of a symbol, the absolute value of the differential signal must exceed $|V_{TH_DET}|$ threshold. Pulses below the minimum threshold voltage do not trigger the symbol detection and pulses exceeding the maximum threshold voltage guarantee to start the symbol detection. Pulses with an amplitude between the minimum voltage and maximum voltage are in an indeterminate region. Recommend to use the lowest gain setting for which the threshold requirement is met.

Table 2. Timing Characteristics

(V_{DD} = +3.0V to +5.5V, V_{CC} = +4.5V to +5.5V, GND = 0V, T_A = −40°C to +125°C, unless otherwise specified. Typical values are at V_{DD} = +3.3V, V_{CC} = +5V, and T_A = +25°C) (1)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Timing Parameters That Apply to All Modes (MODE[1:0] = 0x0, 0x1, 0x2, or 0x3)						
Initialization Delay	t_{INIT}	Delay from power-up or deassertion of $\overline{RST}$ before the device can transmit or receive	450		1000	ms
Reset Pulse Duration	t_{RESET}	Time the $\overline{RST}$ pin must be asserted for the device to properly reset		1		µs
Time to Avoid Entering Shutdown Mode	t_{NO_SHDN}	(2)			50	ns
Time to Enter Shutdown Mode	t_{SHDN}	(3)	1500			ns
RS-485 Mode (MODE[1:0] = 0x3)						
Maximum Data Rate	DR_{MAX_RS485}		20			Mbps
RS-485 Mode Transmitter (Driver) Timing (4)						

(V_{DD} = +3.0V to +5.5V, V_{CC} = +4.5V to +5.5V, GND = 0V, T_A = −40°C to +125°C, unless otherwise specified. Typical values are at V_{DD} = +3.3V, V_{CC} = +5V, and T_A = +25°C) (1)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Differential Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF (*Figure 4* and *Figure 5*)			26	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF (*Figure 4* and *Figure 5*)			10	ns
Driver Enable Time from Not Shutdown to Output High/Low	t_{DZH}, t_{DZL}	R_L = 110Ω, C_L = 50pF (*Figure 6* and *Figure 7*) (2)			60	ns
Driver Disable Time from Output High/Low	t_{DHZ}, t_{DLZ}	R_L = 110Ω, C_L = 50pF (*Figure 6* and *Figure 7*)			50	ns
Driver Enable Time from Shutdown to Output High/Low	$t_{DZH(SHDN)}$, $t_{DZL(SHDN)}$	R_L = 110Ω, C_L = 50pF (*Figure 6* and *Figure 7*) (3)			170	µs
RS-485 Mode Receiver Timing (4)						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF (*Figure 8* and *Figure 9*)			80	ns
Receiver Output Skew $\lvert t_{RPLH} - t_{RPHL} \rvert$	t_{RSKEW}	C_L = 15pF (*Figure 8* and *Figure 9*)			12	ns
Receiver Enable Time from Not Shutdown to Output High/Low	t_{RZH}, t_{RZL}	R_L = 1kΩ, C_L = 15pF (*Figure 10*) (2)			30	ns
Receiver Disable Time from High/Low	t_{RHZ}, t_{RLZ}	R_L = 1kΩ, C_L = 15pF (*Figure 10*)			50	ns
Receiver Enable Time from Shutdown to Output High/Low	$t_{RZH(SHDN)}$, $t_{RZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF (*Figure 10*) (3)			170	µs
Delay to Fail-Safe Operation	t_{D_FS}			10		µs
PoD Mode (MODE[1:0] ≠ 0x3)						
Maximum Data Rate	DR_{MAX_POD}	PD-Link encoding enabled	2.5			Mbps

(V_{DD} = +3.0V to +5.5V, V_{CC} = +4.5V to +5.5V, GND = 0V, T_A = −40°C to +125°C, unless otherwise specified. Typical values are at V_{DD} = +3.3V, V_{CC} = +5V, and T_A = +25°C) (1)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
PoD Mode Transmitter (Driver) Timing (4)						
Differential Driver Propagation Delay	t_{DPLH_PoD}, t_{DPHL_PoD}	R_L = 54Ω, C_L = 50pF, 0.2Mbps (*Figure 12*, *Figure 13*, and *Figure 14*)			450	ns
		R_L = 54Ω, C_L = 50pF, 2.5Mbps (*Figure 12*, *Figure 13*, and *Figure 14*)			55	
Differential Driver Output Skew $\lvert t_{DPLH_PoD} - t_{DPHL_PoD} \rvert$	t_{DSKEW_PoD}	R_L = 54Ω, C_L = 50pF, 0.2Mbps (*Figure 12*, *Figure 13*, and *Figure 14*)			45	ns
		R_L = 54Ω, C_L = 50pF, 2.5Mbps (*Figure 12*, *Figure 13*, and *Figure 14*)			8	
DE Rise Setup Time from Not Shutdown	t_{DES1}	DE rising edge to DI rising edge setup time (*Figure 15*) (2)	0			ns
	t_{DES0}	DE rising edge to DI falling edge setup time (*Figure 15*) (2)	0			
DE Rise Setup Time from Shutdown	$t_{DES1(SHDN)}$	DE rising edge to DI rising edge setup time (*Figure 15*) (3)	90			ns
	$t_{DES0(SHDN)}$	DE rising edge to DI falling edge setup time (*Figure 15*) (3)	90			
PoD Mode Receiver Timing (4)						
Receiver Propagation Delay	t_{RPLH_PoD}, t_{RPHL_PoD}	R_L = 54Ω, C_L = 50pF, 0.2Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x0 (*Figure 12*)			5100	ns
		R_L = 54Ω, C_L = 50pF, 0.2Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x1 (*Figure 13*)			150	
		R_L = 54Ω, C_L = 50pF, 0.2Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x2 (*Figure 14*)			150	
Receiver Output Skew $\lvert t_{RPLH_PoD} - t_{RPHL_PoD} \rvert$	t_{RSKEW_PoD}	R_L = 54Ω, C_L = 50pF, 0.2Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x0 (*Figure 12*)			150	ns

(V_{DD} = +3.0V to +5.5V, V_{CC} = +4.5V to +5.5V, GND = 0V, T_A = −40°C to +125°C, unless otherwise specified. Typical values are at V_{DD} = +3.3V, V_{CC} = +5V, and T_A = +25°C) (1)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
		R_L = 54Ω, C_L = 50pF, 0.2Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x1 (*Figure 13*)			20	
		R_L = 54Ω, C_L = 50pF, 0.2Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x2 (*Figure 14*)			20	
Receiver Propagation Delay	t_{RPLH_PoD}, t_{RPHL_PoD}	R_L = 54Ω, C_L = 50pF, 2.5Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x0 (*Figure 12*)			500	ns
		R_L = 54Ω, C_L = 50pF, 2.5Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x1 (*Figure 13*)			150	
		R_L = 54Ω, C_L = 50pF, 2.5Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x2 (*Figure 14*)			150	
Receiver Output Skew $\lvert t_{RPLH_PoD} - t_{RPHL_PoD} \rvert$	t_{RSKEW_PoD}	R_L = 54Ω, C_L = 50pF, 2.5Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x0 (*Figure 12*)			20	ns
		R_L = 54Ω, C_L = 50pF, 2.5Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x1 (*Figure 13*)			20	
		R_L = 54Ω, C_L = 50pF, 2.5Mbps, $\overline{RE}$ = 0V, RXFILTER = 0, MODE[1:0] = 0x2 (*Figure 14*)			20	
Receiver Enable Time from Not Shutdown to Output High/Low	t_{RZH_PoD}, t_{RZL_PoD}	R_L = 1kΩ, C_L = 15pF, (*Figure 16*) (2)			130	ns
Receiver Disable Time from High/Low	t_{RHZ_PoD}, t_{RZL_PoD}	R_L = 1kΩ, C_L = 15pF, (*Figure 16*)			100	ns
Receiver Enable Time from Shutdown to Output High/Low	$t_{RZH_PoD(SHDN)}$, $t_{RZL_PoD(SHDN)}$	R_L = 1kΩ, C_L = 15pF, (*Figure 16*) (3)			170	µs

[1] All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

[2] When the device is active, that is, either the transmitter or the receiver is powered up, if both DE and $\overline{RE}$ are deasserted for less than 50ns, the device is guaranteed not to enter shutdown.

[3] If both DE and $\overline{RE}$ are deasserted for at least 1500ns, the device is guaranteed to have entered shutdown.

[4] Capacitive load includes test probe and fixture capacitance.

Test and Timing Diagrams

Test and Timing Diagrams for RS-485 Mode

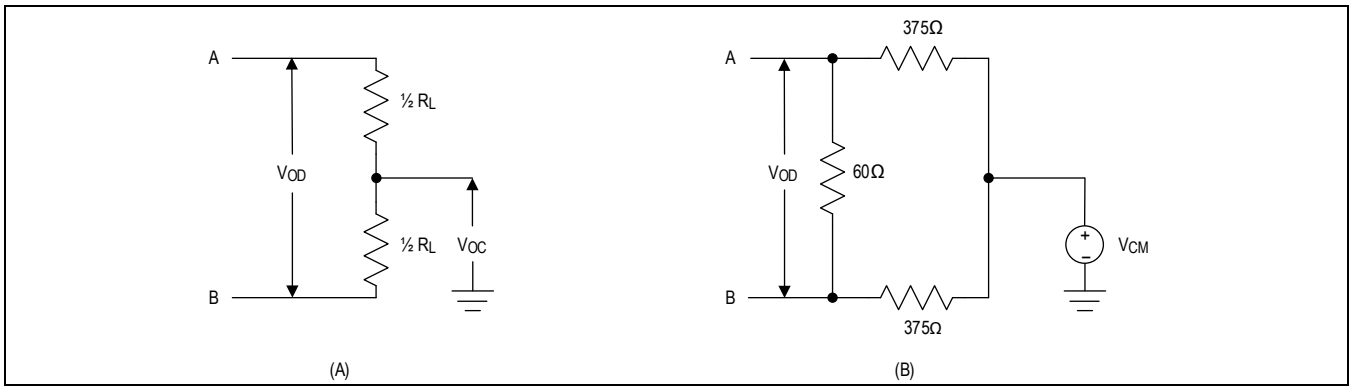


Figure 3. RS-485 Mode Driver DC Test Load

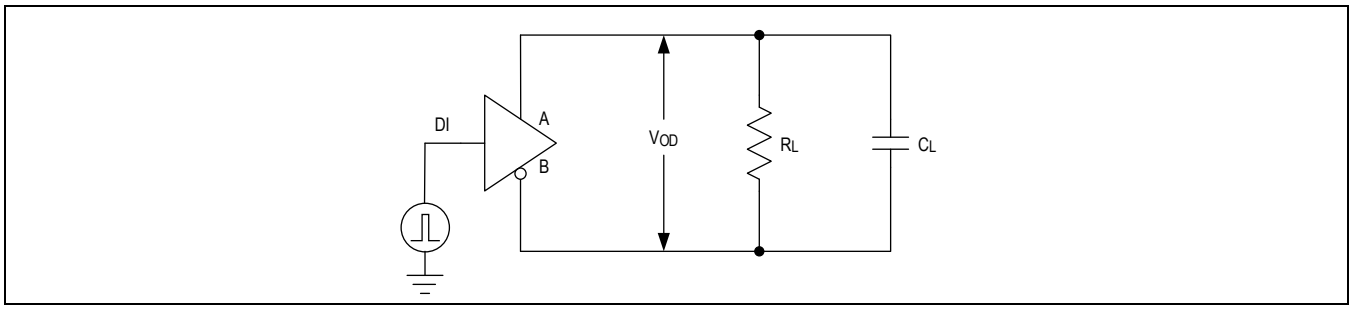


Figure 4. RS-485 Mode Driver Timing Test Circuit

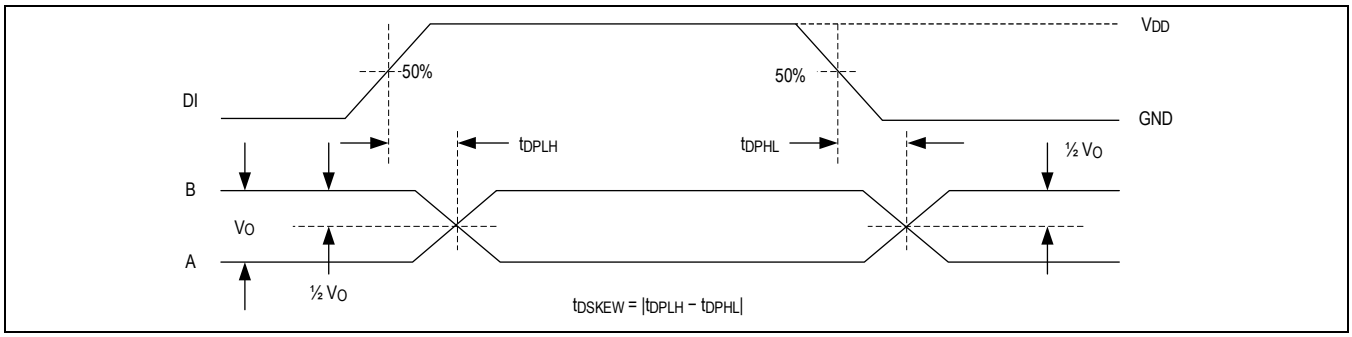


Figure 5. RS-485 Mode Driver Propagation Delays

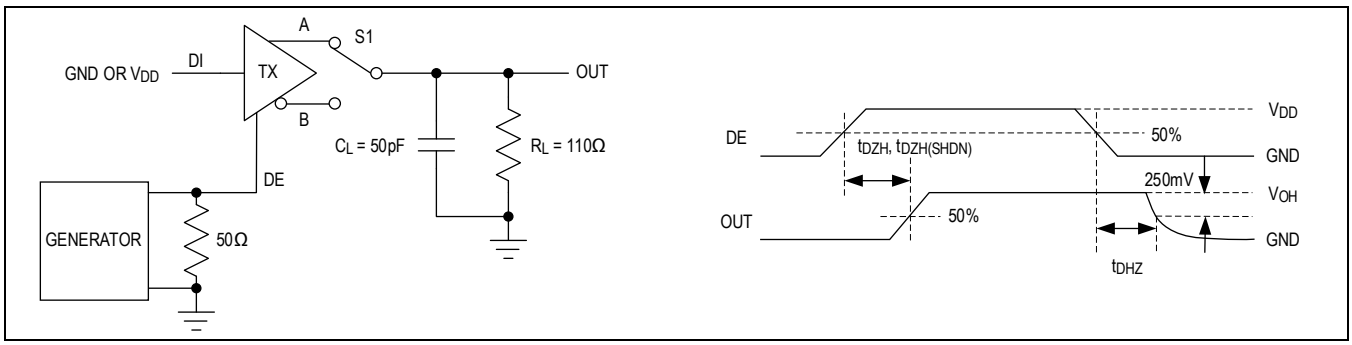


Figure 6. RS-485 Mode Driver Enable and Disable Times (t_{DHZ}, t_{DZH}, $t_{DZH(SHDN)}$)

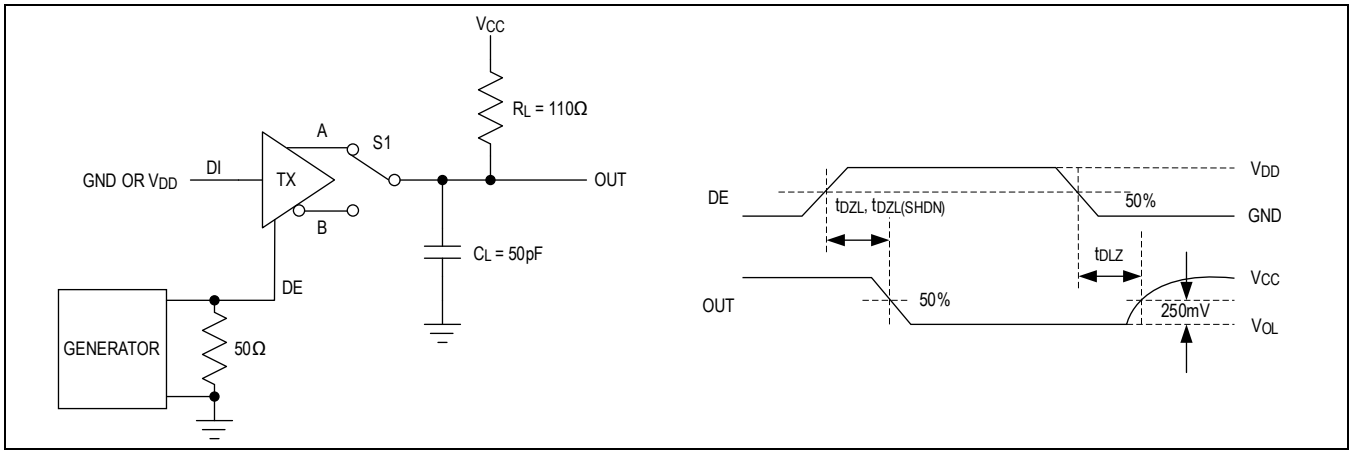


Figure 7. RS-485 Mode Driver Enable and Disable Times (t_{DLZ}, t_{DZL}, $t_{DZL(SHDN)}$)

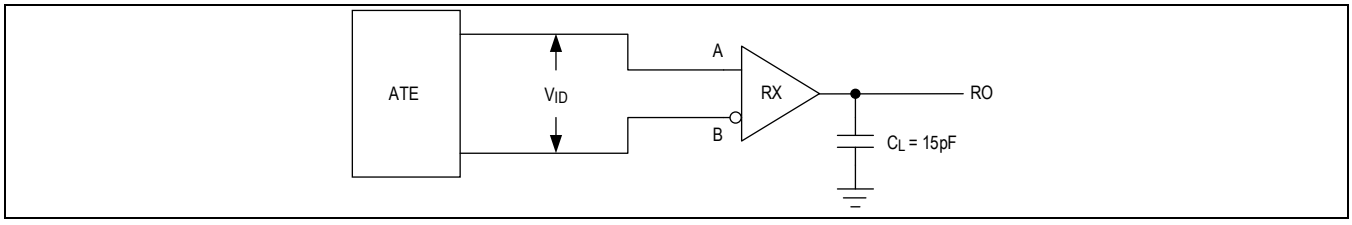


Figure 8. RS-485 Mode Receiver Propagation Delay Test Circuit

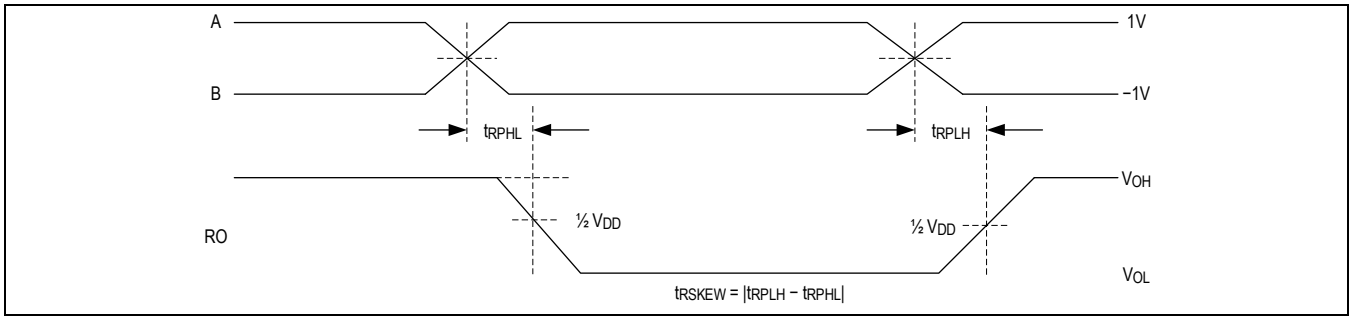


Figure 9. RS-485 Mode Receiver Propagation Delays

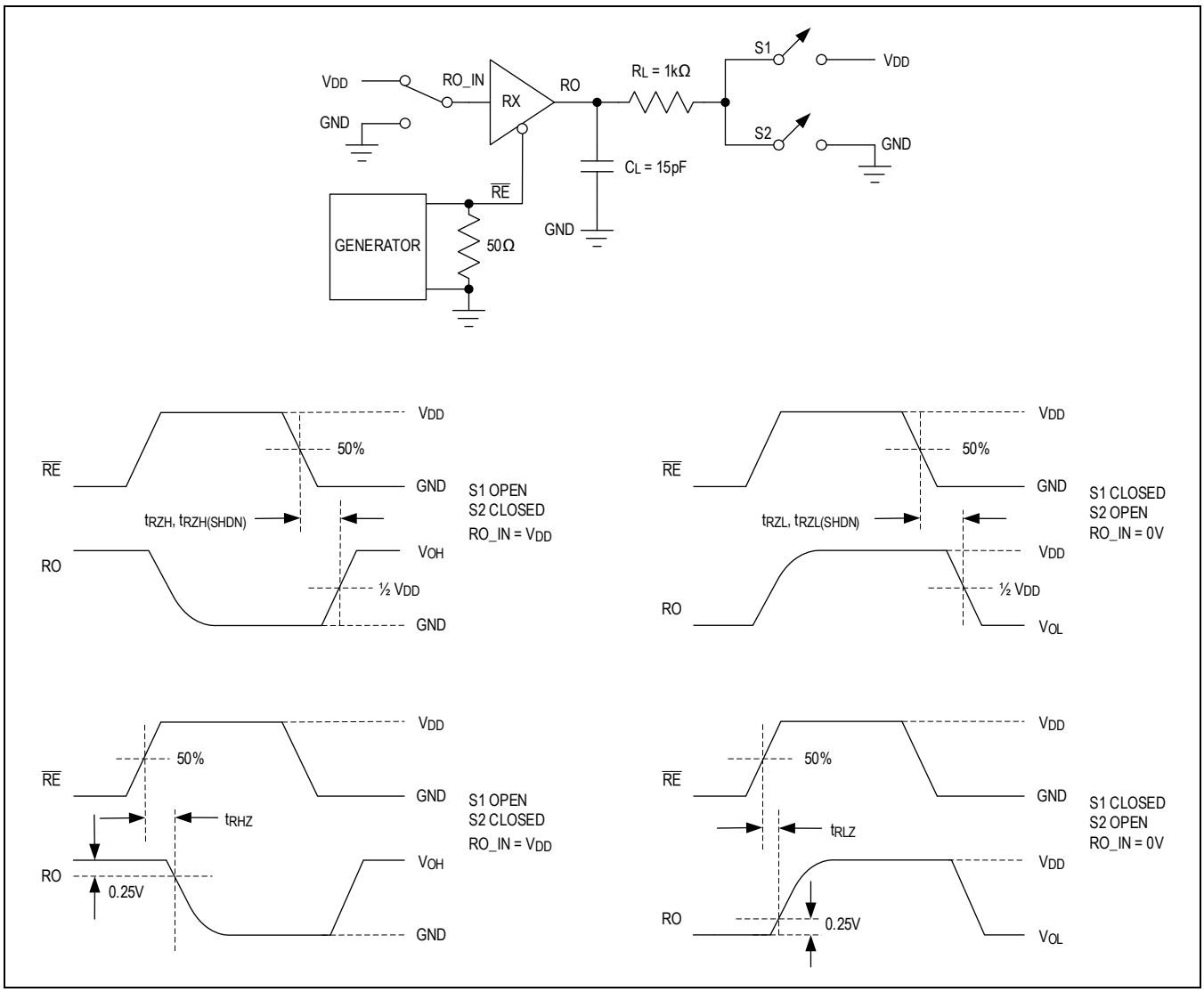


Figure 10. RS-485 Mode Receiver Enable and Disable Times

Test and Timing Diagrams for PoD Modes

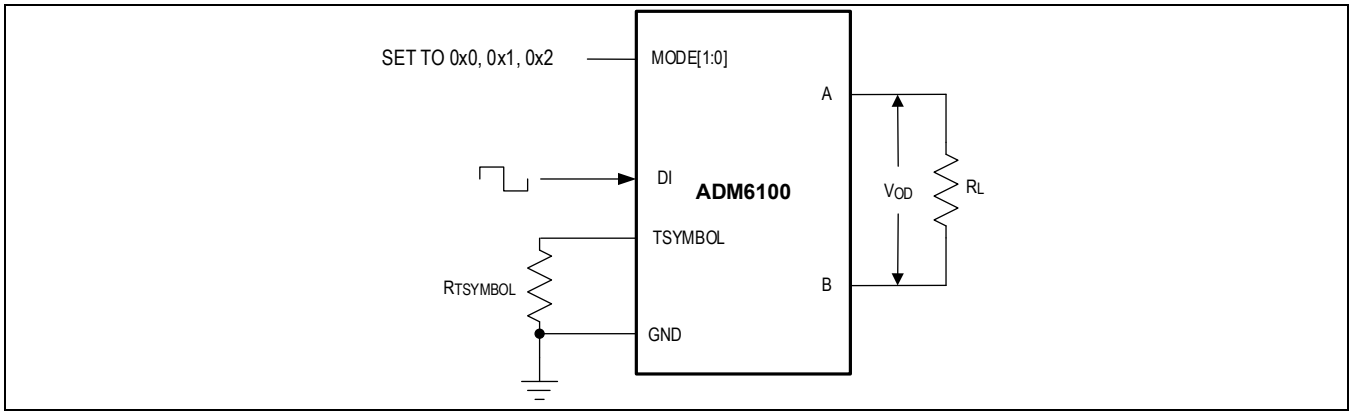


Figure 11. PoD Mode Driver DC Test Load

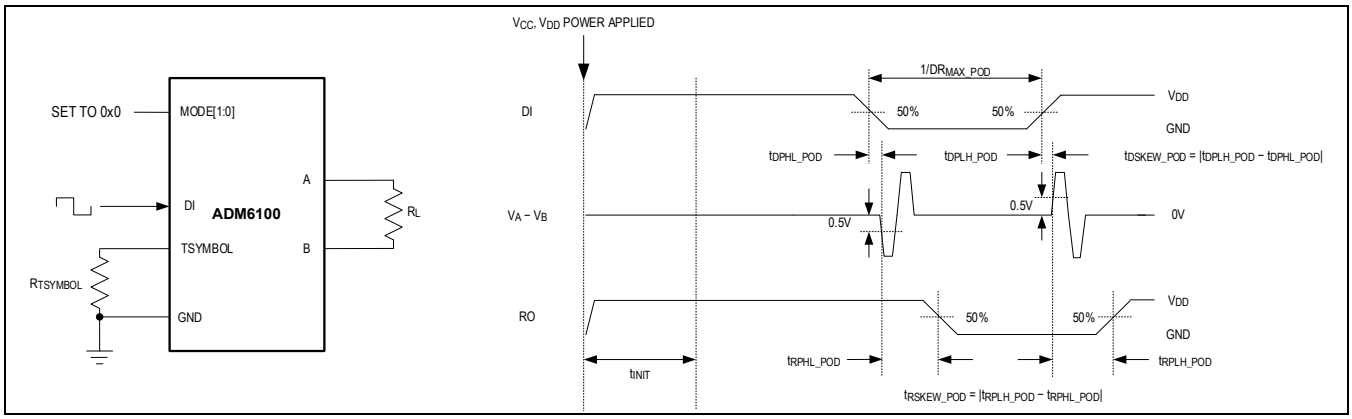


Figure 12. Mode 0 Timing Diagram (POL = 0)

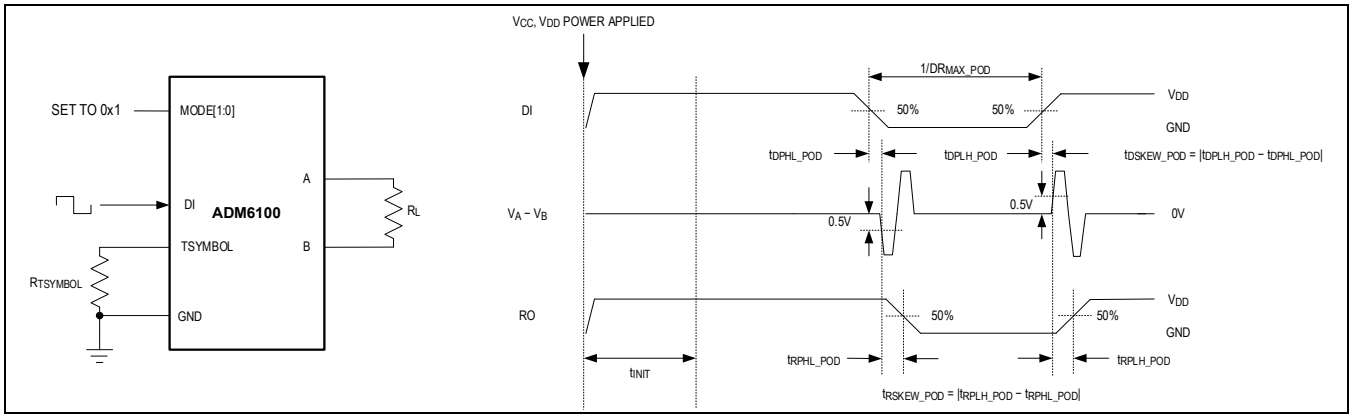


Figure 13. Mode 1 Timing Diagram (POL = 0)

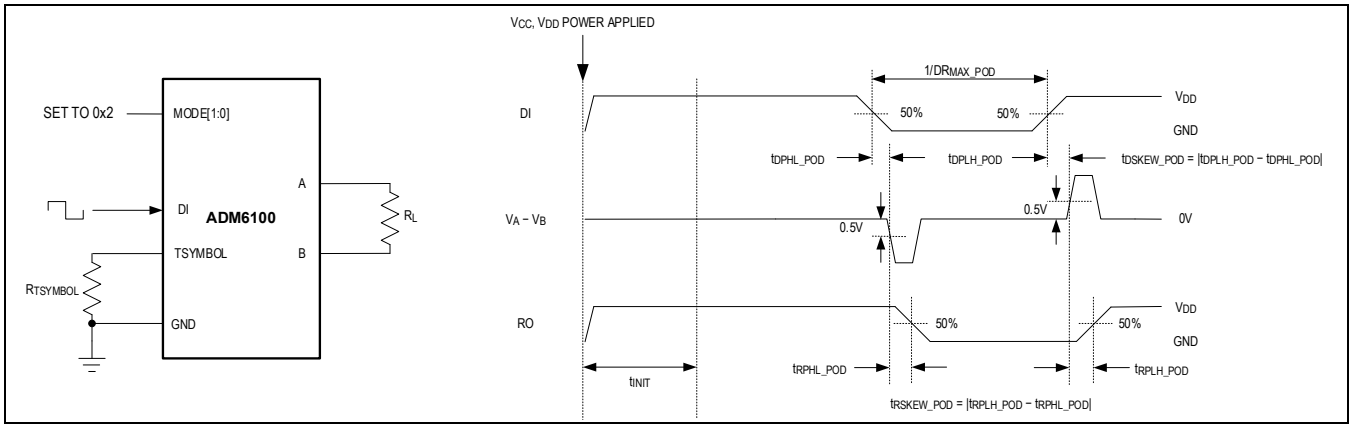


Figure 14. Mode 2 Timing Diagram (POL = 0)

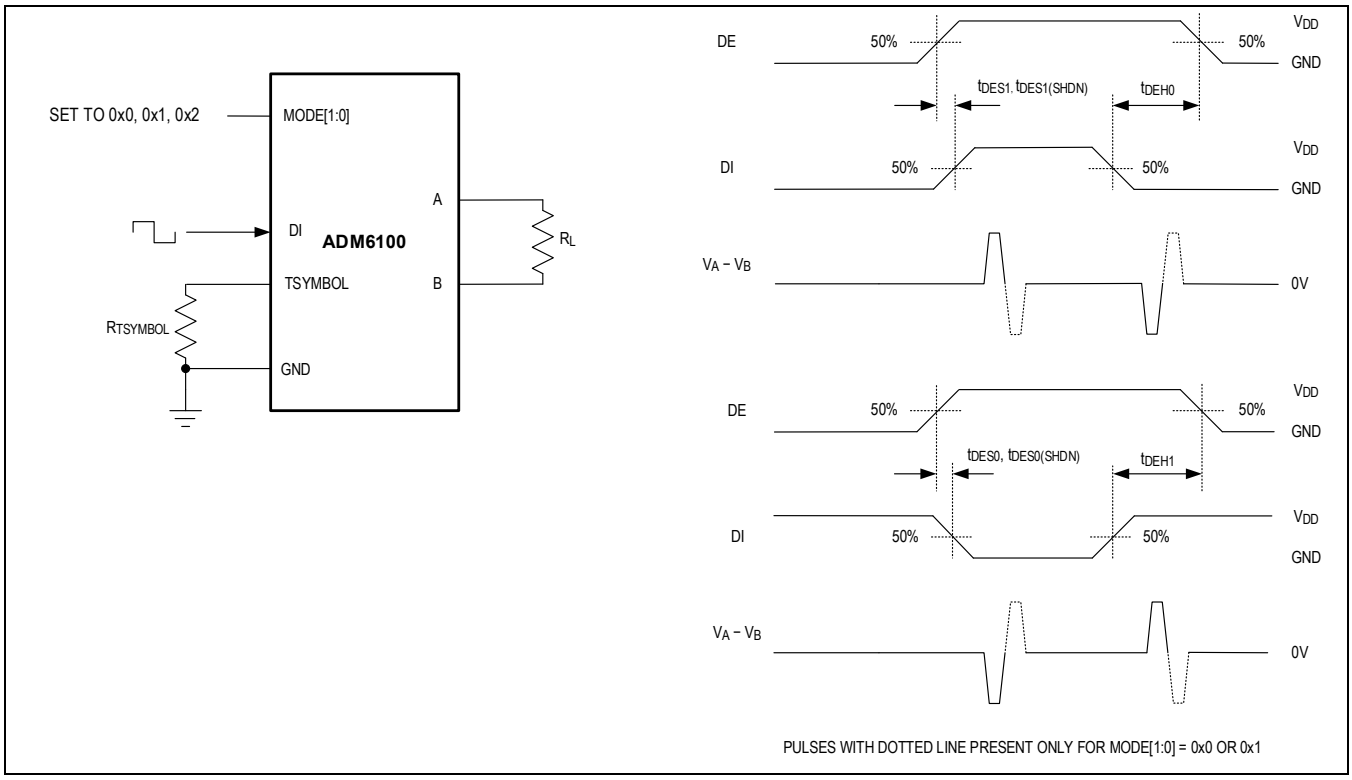


Figure 15. PoD Mode DE Setup and Hold Times (POL = 0)

The DE hold times, t_{DEH0} and t_{DEH1}, are the minimum time from the last DI transition to the falling edge of DE, and are required for the ADM6100 to transmit the last symbol on Pin A and Pin B. DE must remain asserted for at least the duration of DE hold time to allow the generation of the symbol corresponding to the last DI transition. Different factors can affect the hold time, such as the external resistor connected to the TSYMBOL pin, the MODE[1:0] pin settings, the loading on Pin A and Pin B, and the internal propagation delay. The DE hold time is at least the TSYMBOL time.

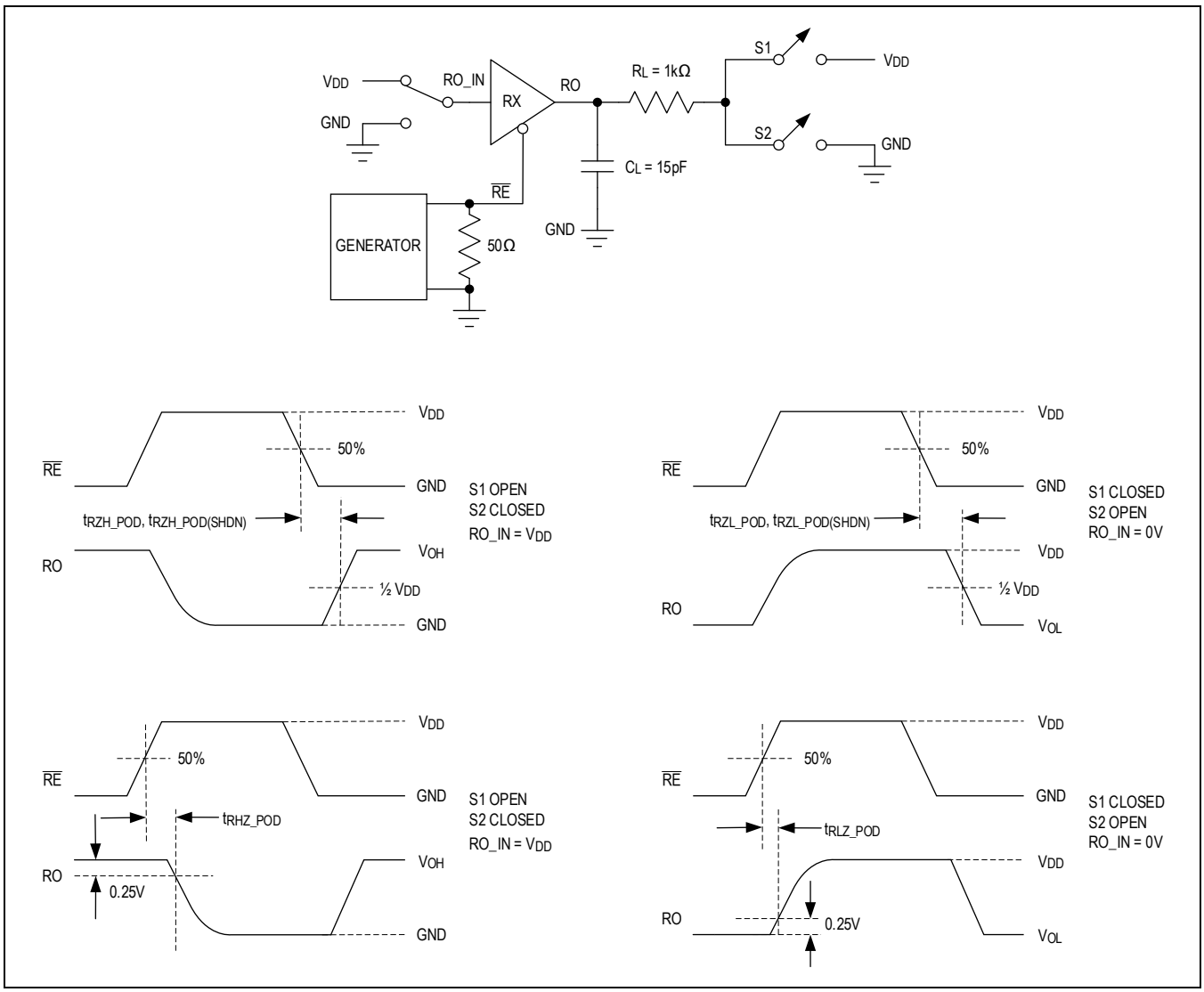


Figure 16. PoD Mode Receiver Enable and Disable Times

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
V_{CC} to GND	−0.3V to +6.0V
V_{DD} to GND	−0.3V to +6.0V
A, B to GND	−30V to +30V
DI, $\overline{RE}$, DE, MODE1, MODE0, POL, PTM, $\overline{RST}$, RXFILTER, AUTO_DIS, GAIN1, GAIN0 to GND	−0.3V to +(V_{DD} + 0.3)V
RO to GND	−0.3V to +(V_{DD} + 0.3)V
$\overline{FAULT}$ to GND	−0.3V to +(V_{DD} + 0.3)V
TSYMBOL to GND	−0.3V to +(V_{CC} + 0.3)V
Continuous Current Into Any Pin	
GND	−250mA to +250mA
A, B, V_{DD}, V_{CC}	−100mA to +100mA
All Other Pins	−50mA to +50mA
Continuous Power Dissipation	
Single-Layer Board (T_A = +70°C, derate 20.8mW/°C above +70°C)	1666.7mW
Multilayer Board (T_A = +70°C, derate 28.6mW/°C above +70°C)	2285.7mW
Temperature Ratings	
Operating Range	−40°C to +125°C
Maximum Junction	+150°C
Storage Range	−60°C to +150°C
Lead (soldering, 10s)	+300°C
Soldering (reflow)	+260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. These are stress ratings only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

PACKAGE TYPE	BOARD TYPE	θ_{JA}	θ_{JC}	UNIT
T2844+1C	Single-Layer Board	48	3	°C/W
T2844+1C	Multilayer Board	35	3	°C/W

For the latest package outline information and land patterns (footprints), go to Package Index. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances are obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to the Thermal Characterization of IC Packages.

Electrostatic Discharge (ESD) Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADM6100

Table 5. ADM6100, 28-Pin TQFN

ESD MODEL	WITHSTAND THRESHOLD (kV)	CLASS
HBM (Pin A and Pin B to GND)	±25	3B
HBM (All Other Pins)	±3	2
CDM	±1.25	C3
Air-Gap Discharge per IEC 61000-4-2 (Pin A and Pin B to GND)	±15	Level 4
Contact Discharge per IEC 61000-4-2 (Pin A and Pin B to GND)	±10	Level 4

ESD Caution



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

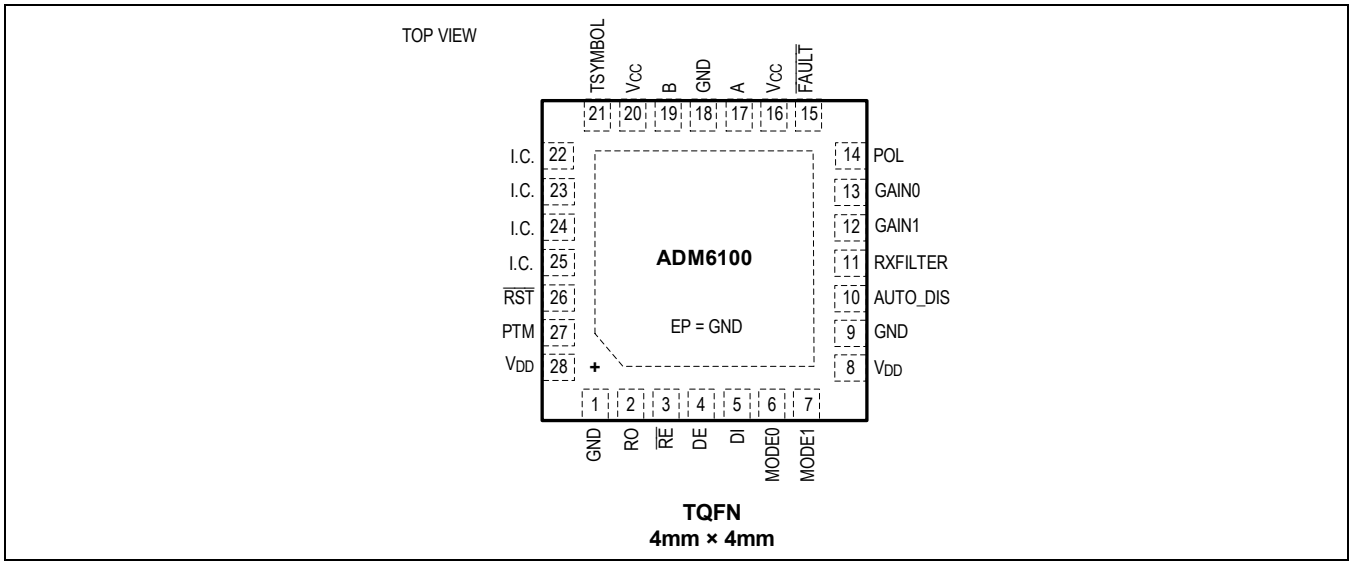


Figure 17. ADM6100 Pin Configuration

Table 6. ADM6100 Pin Function Descriptions

PIN	NAME	DESCRIPTION	REF SUPPLY	Type
1, 9, 18	GND	Ground Reference. Connect to 0V.	GND	Power
2	RO	Receiver Data Output. For more details, see the *Function Tables* section.	VDD	Digital
3	$\overline{RE}$	Receiver Output Enable. Drive $\overline{RE}$ to logic low to enable the receiver. Drive $\overline{RE}$ to logic high to disable the receiver. RO is in high-impedance state when $\overline{RE}$ is set to logic high. Drive $\overline{RE}$ to logic high and DE to logic low to force the device into low-power shutdown mode.	VDD	Digital
4	DE	Driver Output Enable. Drive DE to logic high to enable the driver. Drive DE to logic low to disable the driver. Drive RE to logic high and DE to logic low to force the device into low-power shutdown mode.	VDD	Digital
5	DI	Driver Input. If MODE[1:0] = 0x0, 0x1, or 0x2, DI's logic level transitions are represented by the PD-Link encoding on the Pin A and Pin B. If MODE[1:0] = 0x3, DI is represented by standard RS-485 differential signaling on the Pin A and Pin B.	VDD	Digital
6	MODE0	Encoding Mode. For operation modes details, see *Table 7*. Change the state of Pin MODE1 and Pin MODE0 only when the device is in shutdown mode, powered down, or when $\overline{RST}$ is asserted.	VDD	Digital
7	MODE1	Encoding Mode. For operation modes details, see *Table 7*.	VDD	Digital

		Change the state of Pin MODE1 and Pin MODE0 only when the device is in shutdown mode, powered down, or when $\overline{RST}$ is asserted.		
8, 28	V_{DD}	Digital Interface Supply Voltage Input. Bypass with a 0.1µF ceramic capacitor to ground.	VDD	Power
10	AUTO_DIS	Automatic Polarity Detection and Correction Control. Set to logic high to disable the automatic polarity detection and correction. Set to logic low to enable the automatic polarity detection and correction. For more details, see the *Initialization and Polarity Configuration* section. Change the state of AUTO_DIS only when the part is powered down or when $\overline{RST}$ is asserted.	VDD	Digital
11	RXFILTER	Receiver Filter Control in PoD Modes. Set to logic high to enable the low-pass filter at the receiver input. Set to logic low to disable the low-pass filter at the receiver input.	VDD	Digital
12	GAIN1	Receiver Gain Control in PoD Modes. GAIN[1:0] = 0x0: 0.5x gain. GAIN[1:0] = 0x1: 1x gain. GAIN[1:0] = 0x2: 2x gain. GAIN[1:0] = 0x3: 4x gain.	VDD	Digital
13	GAIN0	Receiver Gain Control in PoD Modes. GAIN[1:0] = 0x0: 0.5x gain. GAIN[1:0] = 0x1: 1x gain. GAIN[1:0] = 0x2: 2x gain. GAIN[1:0] = 0x3: 4x gain.	VDD	Digital
14	POL	Polarity Control. The POL pin determines the idle state of DI and RO. When POL is set to logic low, DI and RO are expected to idle at logic high. When POL is set to logic high, DI and RO are expected to idle at logic low. Changing the state of POL can also swap the role of Pin A and Pin B. For an illustration of the POL pin operation, see *Figure 40* and *Figure 41*.	VDD	Digital
15	$\overline{FAULT}$	Device Ready and Fault Indicator. After the device is powered up and the $\overline{RST}$ pin is deasserted, this open-drain output is held low for a duration of 450ms min and 1000ms max. It is also pulled low after the receiver is first enabled, and remains low until the automatic polarity detection and correction is complete. Finally, it is pulled low when the device temperature exceeds the thermal shutdown threshold. Connect a pull-up resistor to V_{DD}.	VDD	Digital
16, 20	V_{CC}	Supply Voltage Input. Bypass with a 0.1µF ceramic capacitor to ground.	VCC	Power
17	A	Noninverting Receiver Input and Driver Output. For more details, see the *Function Tables* section.	VCC	Analog

19	B	Inverting Receiver Input and Driver Output. For more details, see the *Function Tables* section.	VCC	Analog
21	TSYMBOL	Symbol Duration Control. Connect a resistor between TSYMBOL and GND to control the PD-Link symbol duration. Resistance values between 33kΩ and 412kΩ set the total time of the symbol to between 400ns and 5µs, respectively, for PTM = 0. Setting the PTM pin to logic high doubles the symbol duration. If MODE[1:0] is set to 0x3 (RS-485 mode), the TSYMBOL pin is ignored. Resistor tolerance contributes directly to the pulse duration accuracy. Resistor tolerance of ±1% or better is recommended. For more details, see the *TSYMBOL Configuration* section.	VCC	Analog
26	$\overline{\text{RST}}$	Hardware Reset. When set to logic low, the device is in reset. The polarity detection and correction procedure is repeated after the $\overline{\text{RST}}$ pin is deasserted.	VDD	Digital
27	PTM	Symbol Duration Multiplier. 0x0: Multiplies symbol duration by one. 0x1: Multiplies symbol duration by two. Change the state of PTM only when the device is in shutdown mode, powered down, or when $\overline{\text{RST}}$ is asserted.	VDD	Digital
EP	EP	Exposed Pad. Connect the exposed pad to GND.	GND	Power
22, 23, 24, 25	I.C.	Internally Connected. Do not connect.		

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = +3.3V, V_{CC} = +5V, DE = V_{DD}, $\overline{RE}$ = 0V, RO = no load, $R_{TSYMBOL}$ = 82.5kΩ, PTM = 0, R_{LOAD} = 120Ω, T_A = +25°C, unless otherwise noted)

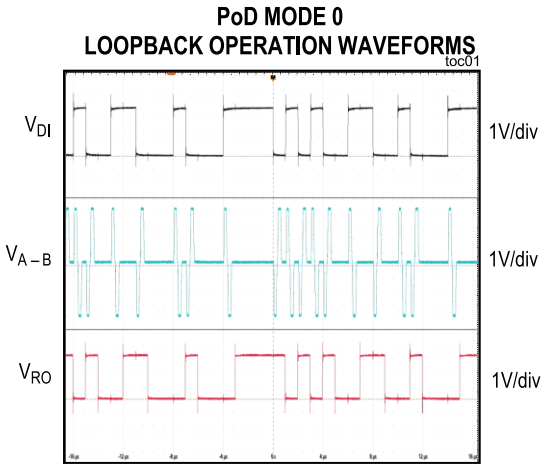


Figure 18. Loopback Operation Waveforms in PoD Mode 0

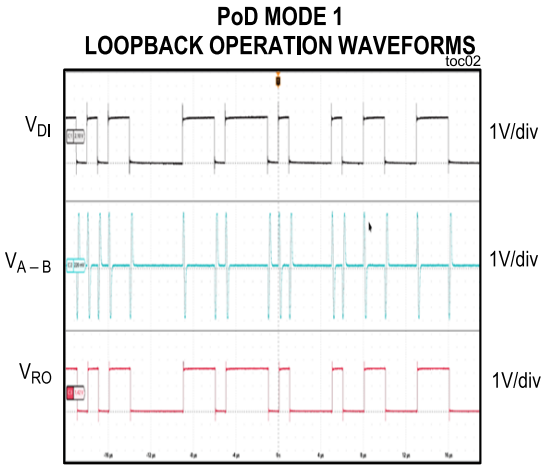


Figure 19. Loopback Operation Waveforms in PoD Mode 1

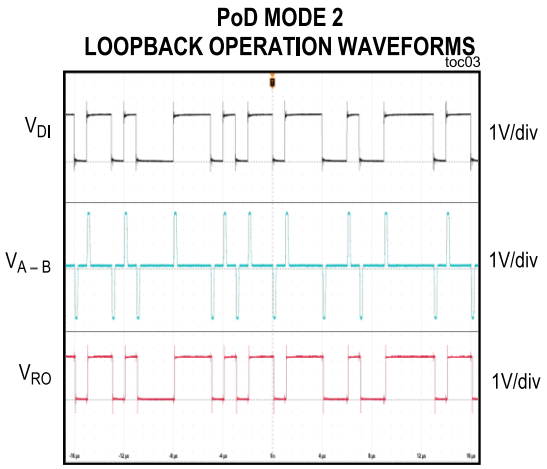


Figure 20. Loopback Operation Waveforms in PoD Mode 2

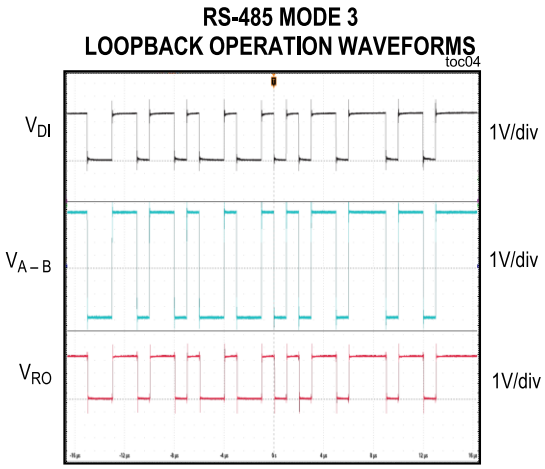


Figure 21. Loopback Operation Waveforms in RS-485 Mode 3

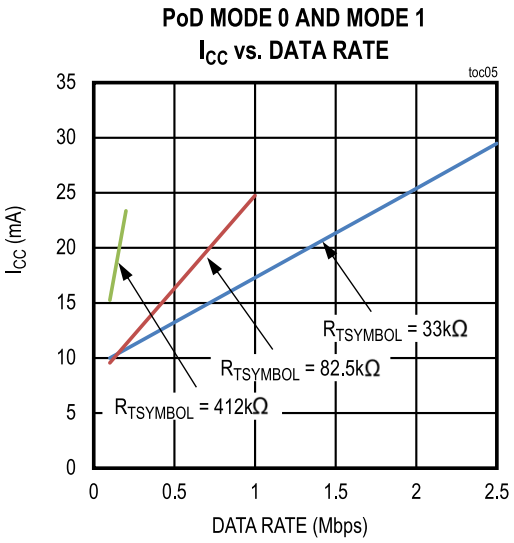


Figure 22. I_{CC} vs. Data Rate in PoD Mode 0 and Mode 1

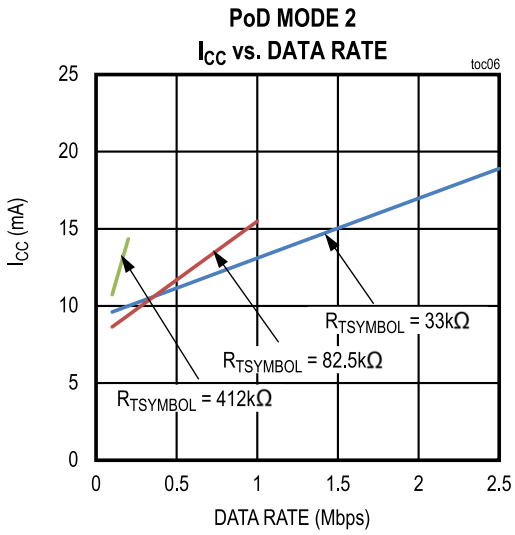


Figure 23. I_{CC} vs. Data Rate in PoD Mode 2

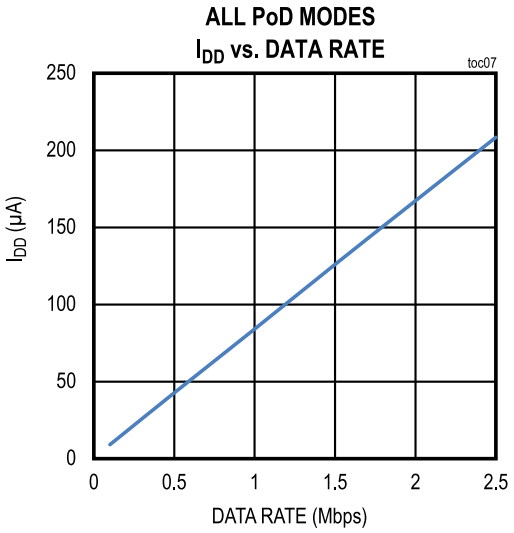


Figure 24. I_{DD} vs. Data Rate in All PoD Modes

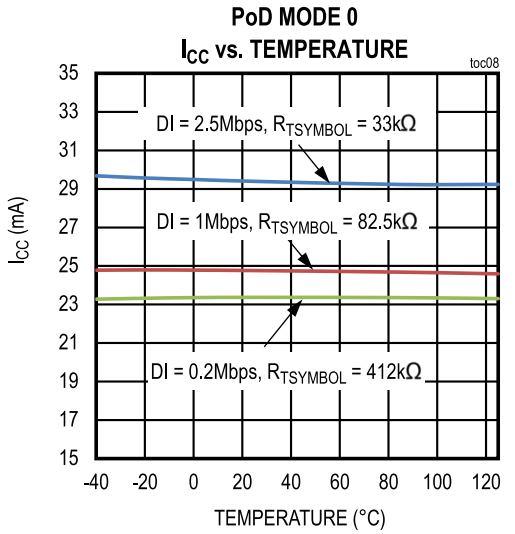


Figure 25. I_{CC} vs. Temperature in PoD Mode 0

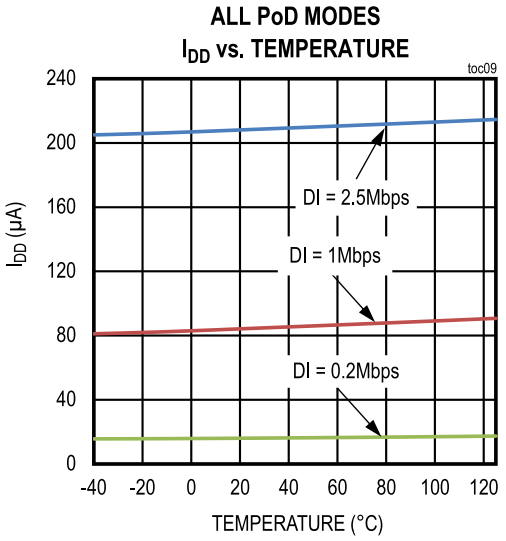


Figure 26. I_{DD} vs. Temperature in All PoD Modes

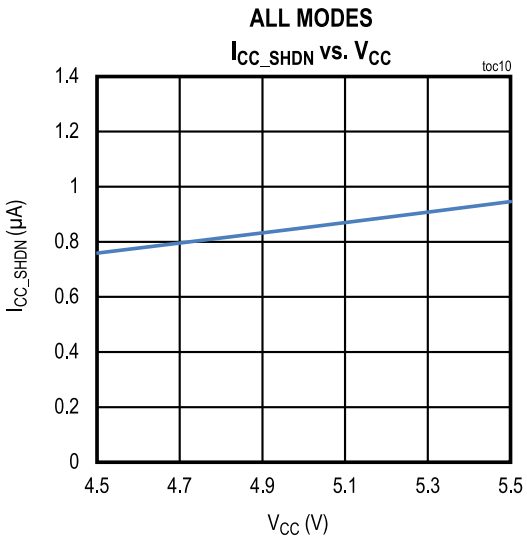


Figure 27. I_{CC_SHDN} vs. V_{CC} in All Modes

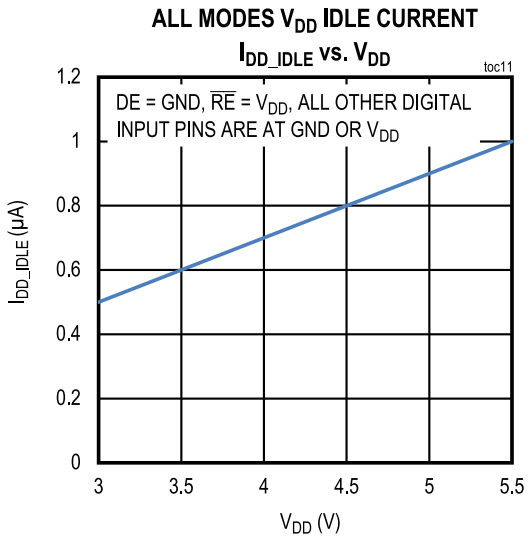


Figure 28. V_{DD} Idle Current I_{DD_IDLE} vs. V_{DD} in All Modes

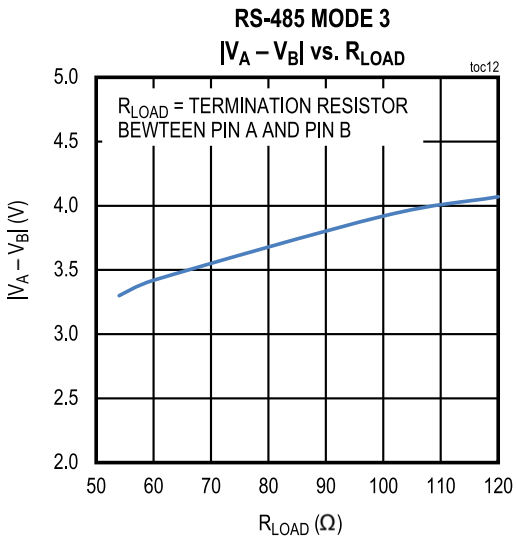


Figure 29. $|V_A - V_B|$ vs. R_{LOAD} in RS-485 Mode 3

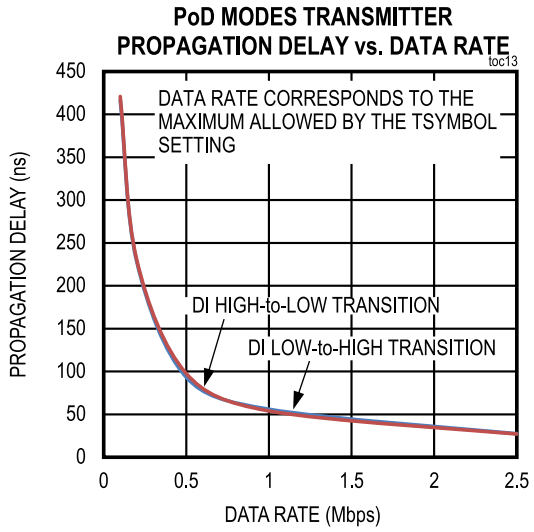


Figure 30. Transmitter Propagation Delay vs. Data Rate in PoD Modes

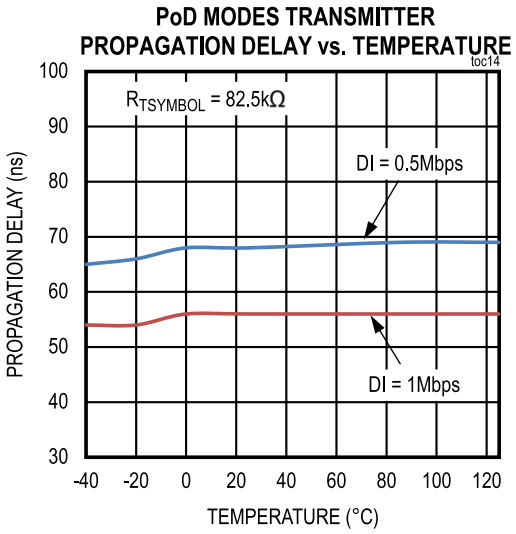


Figure 31. Transmitter Propagation Delay vs. Temperature in PoD Modes

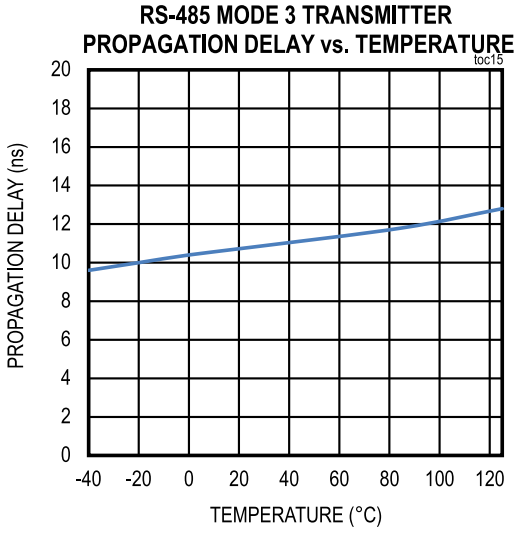


Figure 32. Transmitter Propagation Delay vs. Temperature in RS-485 Mode 3

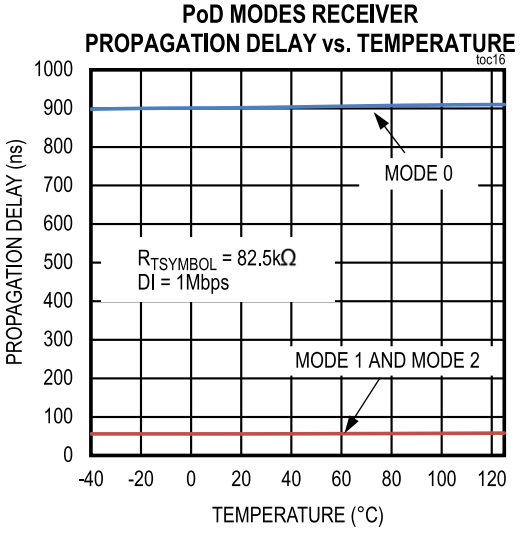


Figure 33. Receiver Propagation Delay vs. Temperature in PoD Modes

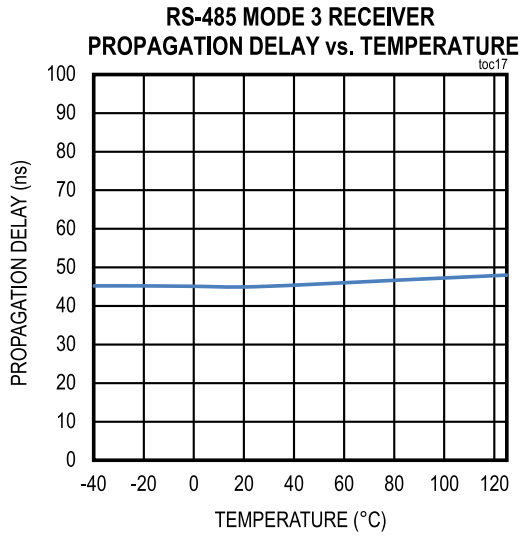


Figure 34. Receiver Propagation Delay vs. Temperature in RS-485 Mode 3

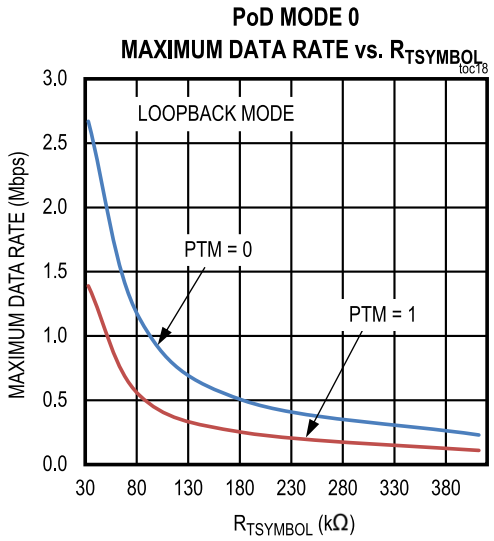


Figure 35. Maximum Data Rate vs. $R_{TSYMBOL}$ in PoD Mode 0

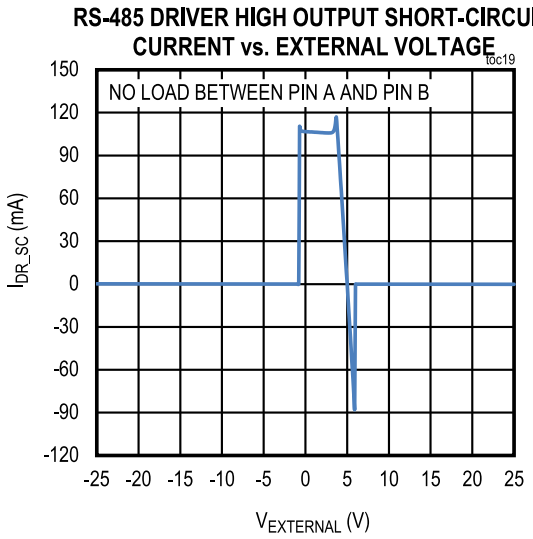


Figure 36. RS-485 Driver High Output Short-Circuit Current vs. External Voltage

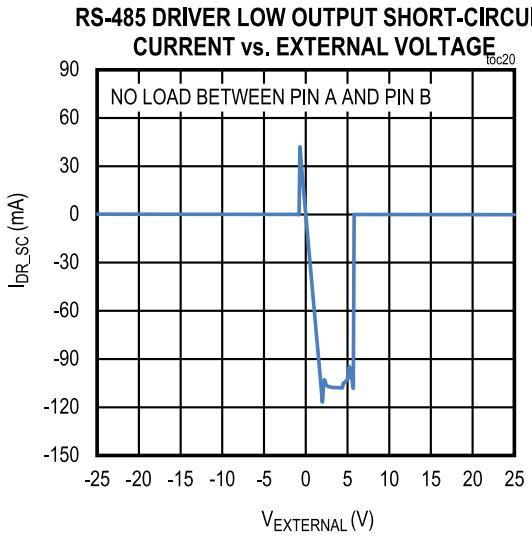


Figure 37. RS-485 Driver Low Output Short-Circuit Current vs. External Voltage

THEORY OF OPERATION

The ADM6100 is a half-duplex PoD transceiver featuring the PD-Link encoding, a physical layer specific robust channel encoding method that enables software-agnostic PoD communications using a single pair of wires while minimizing the size and cost of external components. The ADM6100 features the standard RS-485 mode for the applications that require RS-485 backwards compatibility.

The ADM6100 integrates the following features:

- Resistor controlled channel bandwidth in PoD modes
- Automatic polarity detection and correction
- Receiver gain control in PoD modes
- Receiver filter in PoD modes
- Fault protection on Pin A and Pin B
- Hot-swap inputs
- Fail-safe operation in RS-485 mode
- Low-power shutdown mode
- Thermal shutdown

Power-over-Data (PoD) Operation

The ADM6100 is powered by the system voltages supplied at V_{CC} and V_{DD}. External AC-blocking inductors are required to superimpose the power on the data lines at the supply side. At the load side, AC coupling capacitors separate the data from the power. The AC coupling capacitors are connected to Pin A and Pin B for data transmission. A full-bridge rectifier is optional and only needed for full polarity-agnostic operation. A DC-DC converter is recommended to convert the line voltage to a regulated 5V supply to power the transceiver and the application circuitry. For an example, see *Figure 2*.

The transceiver is suitable for applications where power and data share a single pair of wires. The ADM6100 operates with data rates up to 2.5Mbps in PoD modes. Supported cable length, number of nodes in the network and network topology depend on cable quality, channel bandwidth, and load current drawn by the nodes over the distributed network.

RS-485 Mode

The ADM6100 is compatible with standard RS-485 transceivers by setting the Pin MODE0 and Pin MODE1 to 0x3. In the standard RS-485 mode, the transceiver transmits and receives standard fully-differential signals. For an example, see *Figure 38*. In the RS-485 mode, Pin TSYMBOL, Pin PTM, Pin RXFILTER, Pin GAIN0, and Pin GAIN1 are do not care. It is recommended to connect these digital input pins to V_{DD} or GND, while the TSYMBOL pin can remain unconnected. It is not recommended to use RS-485 mode for PoD operation.

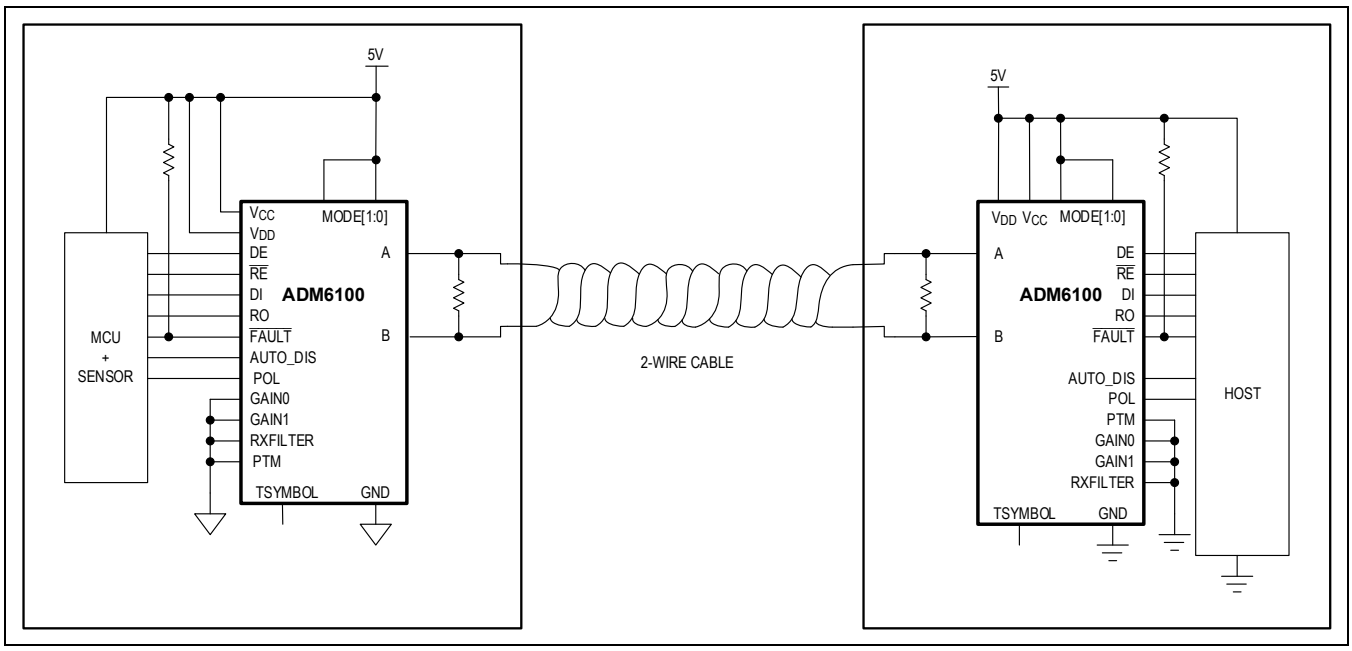


Figure 38. ADM6100 in Standard RS-485 Mode

Power Supply

For normal operation, the ADM6100 must be powered by both the V_{CC} analog supply and V_{DD} digital interface supply. The ADM6100 does not require special power supply sequencing. Users can set the digital interface supply V_{DD} independently from the analog supply V_{CC}. Typically, apply an external 5V supply to V_{CC}, and 3.3V or 5V supply to V_{DD}.

Transceiver Operation

The ADM6100 comes with the standard RS-485 transceiver pins, which include the digital interface Pin DI, Pin RO, Pin DE, and Pin $\overline{RE}$ and transceiver Pin A and Pin B. It is compatible with standard RS-485 transceivers.

Driver and Receiver Enable Pins

The Pin $\overline{RE}$ and Pin DE configure the ADM6100 in three different ways. The first is standard transmission mode, in which the Pin $\overline{RE}$ and Pin DE are connected and used as a single signal for transmitter or receiver enable. To transmit data on the channel, set both Pin DE and Pin $\overline{RE}$ to logic high. This enables the transmitter and disables the receiver. To receive data from the channel, set both Pin DE and Pin $\overline{RE}$ to logic low. This disables the transmitter and enables the receiver.

Disable both the transmitter and receiver simultaneously to set the ADM6100 in the low-power shutdown mode, which is accomplished by setting Pin $\overline{RE}$ to logic high and Pin DE to logic low.

The third configuration, the loopback mode, enables both the transmitter and the receiver. This mode allows the receiver to monitor the transmitter output. The MCU or FPGA connected to the DI and RO can thus verify that the DI input matches the RO output. A mismatch between DI input and RO output may indicate a collision on the bus between two or more transmitters.

Operation Modes

For PoD operation, Pin MODE1 and Pin MODE0 are set to 0x0, 0x1, or 0x2. For standard RS-485 operation, Pin MODE1 and Pin MODE0 are set to 0x3. The ADM6100 supports both point-to-point and multidrop topologies in all modes.

Table 7. Operation Mode Description

ENCODING MODE	PIN MODE1	PIN MODE0	DESCRIPTION
Mode 0	0	0	MODE[1:0] = 0x0: Transceiver represents each transition of DI with two symmetric reverse polarity pulses. The receiver output, RO, is updated after correctly detecting the symbol.
Mode 1	0	1	MODE[1:0] = 0x1: Transceiver represents each transition of DI with two symmetric reverse polarity pulses. The receiver output, RO, is updated after correctly detecting the first pulse only.
Mode 2	1	0	MODE[1:0] = 0x2: Transceiver represents each transition of DI with a single differential pulse. The receiver output, RO, is updated after correctly detecting the pulse.
Mode 3	1	1	MODE[1:0] = 0x3: RS-485 mode.

The PoD modes use PD-Link encoding, which is an edge dependent signaling method that maintains DC balance and data integrity on the line without relying on the software stack for encoding. This method allows the channel bandwidth to be independent of the input data rate and enables the reduction of the cost and size of the associated magnetics needed to couple and decouple power with the data on a 2-wire cable.

In Mode 0, the transmitter sends out two complementary differential pulses per DI edge on Pin A and Pin B. The receiver determines the validity of the received symbol before latching the RO. This mode offers good noise immunity in noisy industrial environments. However, the decoding of the full symbol increases the latency between corresponding DI and RO edges. For Mode 0, this latency depends on the TSYMBOL setting.

In Mode 1, the transmitter drives two complementary differential pulses per DI edge on Pin A and Pin B. The receiver uses only the first pulse of the received symbol to verify its validity. The Pin RO changes state upon the detection of the first pulse. For the Mode 1 operation, see *Figure 13*. This mode has a much shorter DI to RO latency than Mode 0.

In Mode 2, the transmitter sends out only a single differential pulse per DI edge on the Pin A and Pin B. The receiver latches RO upon the detection of the single pulse, thus giving this mode the same latency as that of Mode 1. For the Mode 2 operation, see *Figure 14*. Mode 2 consumes less current than Mode 0 and Mode 1, but the DC balancing is not fully guaranteed.

In Mode 3, the ADM6100 uses standard RS-485 signaling on the Pin A and Pin B. This allows standard RS-485 transceivers to operate on the same bus with the ADM6100. When the bus uses 2- or 4-wire communication without PoD, the ADM6100 communicates with standard RS-485 transceivers properly when configured in Mode 3.

Function Tables

Table 8 and *Table 9* show the ADM6100 operation in the RS-485 mode when MODE[1:0] = 0x3.

Table 8. RS-485 Mode Function Table − Transmitting

INPUTS				OUTPUTS		MODE
POL	$\overline{RE}$	DE	DI	A	B	
0	X	1	1	1	0	Active
0	X	1	0	0	1	Active
1	X	1	1	0	1	Active
1	X	1	0	1	0	Active
X	0	0	X	High impedance		Driver disabled
X	1	0	X	High impedance		Shutdown

Note: AUTO_DIS = 1. Automatic polarity detection and correction feature is disabled. Polarity is only controlled by the Pin POL setting.

X = Do not care.

Table 9. RS-485 Mode Function Table − Receiving

INPUTS				OUTPUT	MODE
POL	$\overline{RE}$	DE	A − B	RO	
0	0	X	≥−50mV	1	Active
0	0	X	≤−200mV	0	Active
0	0	X	Open/Short	1	Active
1	0	X	≥−50mV	0	Active
1	0	X	≤−200mV	1	Active
1	0	X	Open/Short	0	Active
X	1	1	X	High impedance	Receiver disabled
X	1	0	X	High impedance	Shutdown

Note: AUTO_DIS = 1. Automatic polarity detection and correction feature is disabled. Polarity is only controlled by the Pin POL setting.

X = Do not care.

Table 10 and *Table 11* show the ADM6100 operation in the PoD encoding mode when MODE[1:0] = 0x0. When operating in PoD modes, the transceiver responds to the edges rather than states. Specifically, the transmitter responds to transitions on DI while the receiver responds to transitions on A and B. In Mode 0 and Mode 1, two complementary differential pulses are transmitted or received on the Pin A and Pin B, while in Mode 2, the Pin A and Pin B transmit or receive a single differential pulse.

Table 10. Mode 0 Function Table − Transmitting

INPUTS				OUTPUTS		MODE
POL	$\overline{RE}$	DE	DI	A	B	
0	X	1	Rising edge	Positive Pulse + Negative Pulse	Negative Pulse + Positive Pulse	Active
0	X	1	Falling edge	Negative Pulse + Positive Pulse	Positive Pulse + Negative Pulse	Active
1	X	1	Rising edge	Negative Pulse + Positive Pulse	Positive Pulse + Negative Pulse	Active
1	X	1	Falling edge	Positive Pulse + Negative Pulse	Negative Pulse + Positive Pulse	Active
X	0	0	X	High impedance		Driver disabled
X	1	0	X	High impedance		Shutdown

Note: AUTO_DIS = 1. Automatic polarity detection and correction feature is disabled. Polarity is only controlled by the Pin POL setting.

X = Do not care.

Table 11.Mode 0 Function Table − Receiving

INPUTS				OUTPUT	MODE
POL	$\overline{RE}$	DE	A − B	RO	
0	0	X	Positive Pulse + Negative Pulse	1	Active
0	0	X	Negative Pulse + Positive Pulse	0	Active
0	0	X	Open/Short	Keep previous state	Active
1	0	X	Positive Pulse + Negative Pulse	0	Active
1	0	X	Negative Pulse + Positive Pulse	1	Active
1	0	X	Open/Short	Keep previous state	Active
X	1	1	X	High impedance	Receiver disabled
X	1	0	X	High impedance	Shutdown

Note: AUTO_DIS = 1. Automatic polarity detection and correction feature is disabled. Polarity is only controlled by the Pin POL setting.

X = Do not care.

TSYMBOL Configuration

In PoD modes, the length of the pulses is configurable using an external resistor to ground on the Pin TSYMBOL. TSYMBOL is defined as the time for a complete symbol, which includes the first pulse, the second pulse, and a third section at the common-mode.

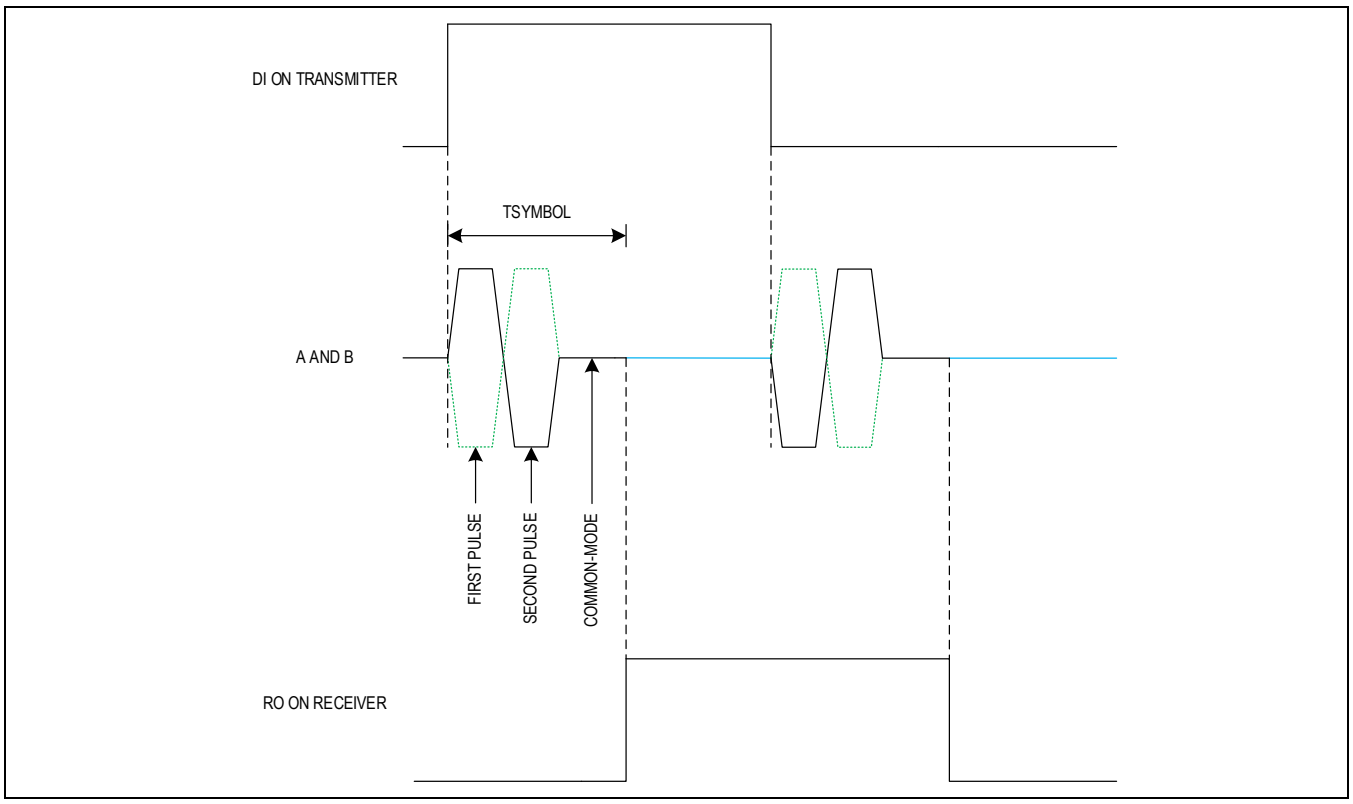


Figure 39. TSYMBOL in PoD Mode 0

In PoD Mode 0 and Mode 1, set the TSYMBOL by using the following equation:

$$TSYMBOL\ (s) = 1.22 \times 10^{-11} \times R_{TSYMBOL}(\Omega) \times (1 + PTM)$$

where $R_{TSYMBOL}$ is the external resistor on the Pin TSYMBOL in ohms and PTM is the Pin PTM setting. Depending on whether the Pin PTM is set to logic high or logic low, PTM is 1 or 0, respectively.

In PoD Mode 2, TSYMBOL is half of the TSYMBOL time in PoD Mode 0 or Mode 1.

The slew rate for all the edges of the A/B waveforms scales with the TSYMBOL setting where the rise/fall times scale to approximately 25% of the first pulse. This automatic adjustment is designed to reduce the EMI of the transmission as much as possible. For an approximation of the edge rise/fall time as it relates to $R_{TSYMBOL}$, use the following equation:

$$t_{R/F}(s) = 0.052 \times (1.22 \times 10^{-11} \times R_{TSYMBOL}(\Omega) \times (1 + PTM))$$

In Mode 0, since RO is changed after detecting the symbol, the DI-to-RO latency scales with the TSYMBOL setting. For Mode 1 and Mode 2, the communication latency is not impacted by the TSYMBOL setting. Thus, Mode 1 or Mode 2 is recommended for minimal latency operation.

Receiver Gain Control in PoD Modes

The ADM6100 receiver integrates a programmable gain amplifier that is used for gain control of the receiver signals in PoD modes. The Pin GAIN1 and Pin GAIN0 are used to select from four possible gain settings (0.5x, 1x, 2x, and 4x). The receiver gain control improves the bit error rate performance in the presence of signal attenuation due to increased cable length or large network loading. To avoid saturating the receiver input stage, it is recommended to select the lowest possible gain that maintains the communication. Choose a higher gain setting only when the received signal is less than the threshold of a lower gain option.

Receiver Filter Operation in PoD Modes

In PoD modes, the ADM6100 receiver uses an optional low-pass filter (LPF) to reduce channel noise in conjunction with the receiver gain stage. Bypass the filter by connecting the Pin RXFILTER to logic low. When the Pin RXFILTER is set to logic high, the input filter is active. The cutoff frequency of the input LPF scales inversely with the symbol time, which is set by the resistor between the Pin TSYMBOL and ground. The use of the filter is a trade-off between lower noise sensitivity and latency.

Initialization and Polarity Configuration

After power-up or release of the Pin $\overline{\text{RST}}$, the ADM6100 requires 450ms to 1000ms before it is ready to transmit or receive on the line. This initialization delay ensures that the network has time to power up and settle. $\overline{\text{FAULT}}$ is driven to logic low during the initialization period. During that time, DI must be set to its idle state, which is determined by the state of POL. If POL is set to logic low, DI must idle high. If POL is set to logic high, DI must idle low. All nodes on the network must have their Pin POL set to the same initial state. For DI, RO, A, and B status with different POL state after initialization, see *Figure 40* and *Figure 41*.

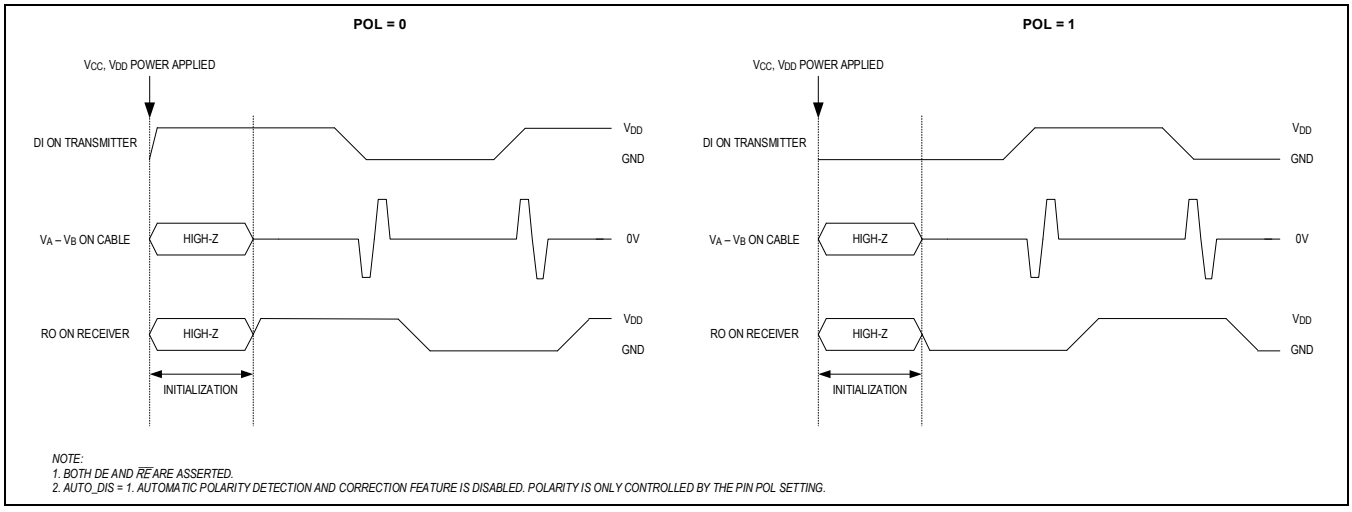


Figure 40. Device Operation After Initialization with Different POL – PoD Mode 0

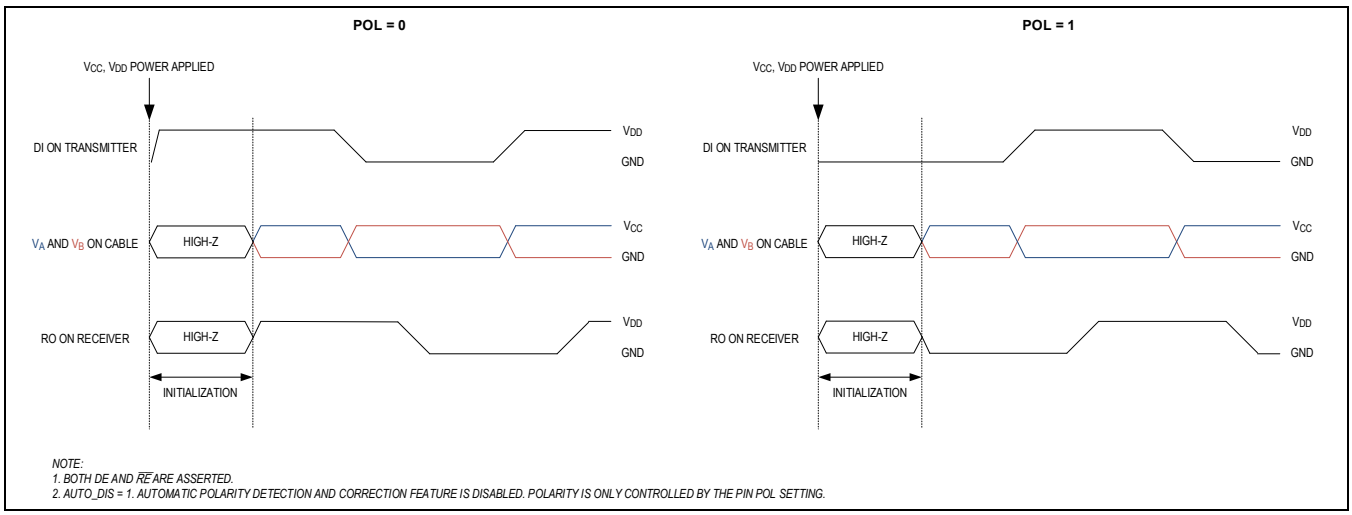


Figure 41. Device Operation After Initialization with Different POL − RS-485 Mode

The ADM6100 can automatically detect and correct any miswiring of the wires to its Pin A and Pin B. To use this feature, set AUTO_DIS to logic high on the initial transmitting node and set AUTO_DIS to logic low on all other nodes. Note that it is not recommended to set the initial transmitter's Pin AUTO_DIS to logic low, as the initial transmitter determines the polarity that all other nodes must follow.

In any PoD mode, configure one node as the initial transmitter and all other nodes as receivers before the initial transmitter sends the first symbol. The first symbol is produced when there is a transition on DI of the initial transmitter. The pulse sequence of the initial symbol is determined by the idle state of DI. Each receiver decodes the first received symbol and determines whether Pin A and Pin B are correctly wired or require internal correction for any miswiring. From this point onward, nodes can communicate normally until the system resets or powers down.

Figure 42 shows the automatic polarity detection and correction when DI idles high (POL = 0). Since DI idles high, POL must be set to logic low on all devices. This ensures the RO output of the receiving nodes is at logic high after initialization. Without any miswiring, after the first transition edge of DI, RO of the receiver nodes is at logic low, as shown in *Figure 42A*. In *Figure 42B*, Node #1 and Node #2 are correctly wired, but Node #1 and Node #3 have a miswiring. When Node #1 transitions from high-to-low, Node #2 correctly decodes it as a high-to-low transition while Node #3 decodes it as a low-to-high transition. Node #3 corrects internally the effect of the miswiring upon decoding the first received symbol. If the device is powered down or reset, this process must be reiterated.

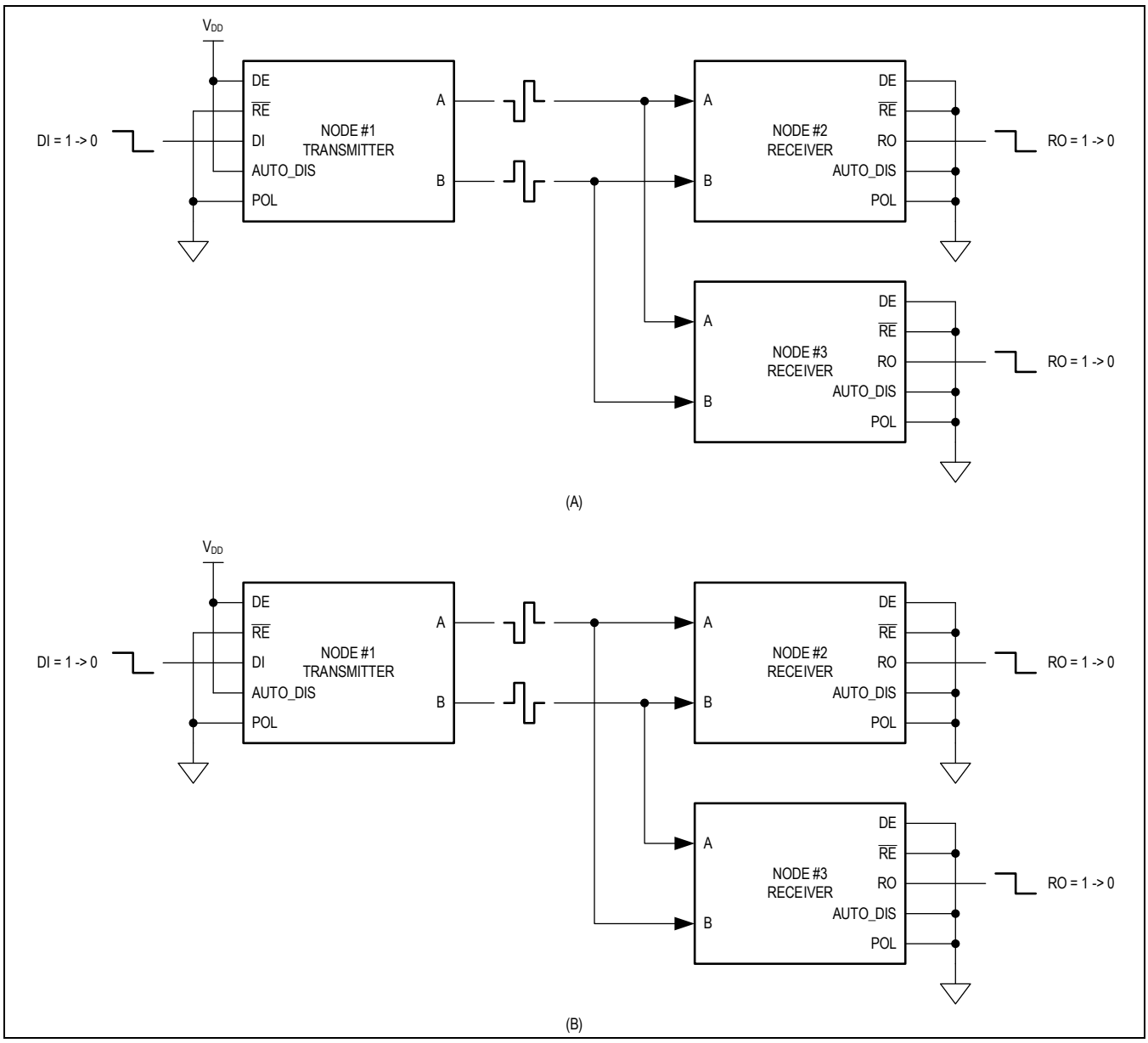


Figure 42. Automatic Polarity Detection and Correction with POL = 0

Figure 43 shows the same scenario with DI idling low (POL = 1).

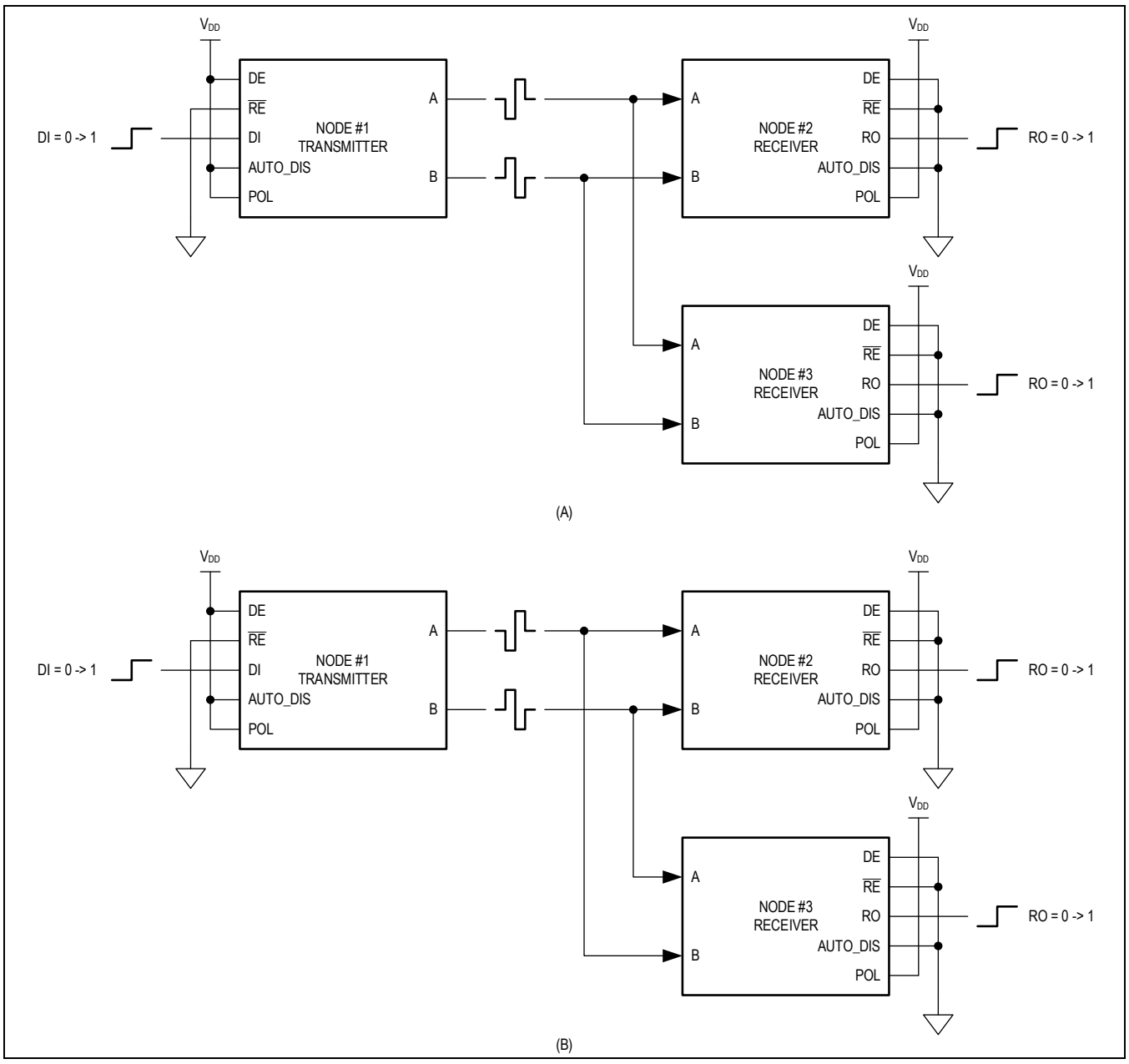


Figure 43. Automatic Polarity Detection and Correction with POL = 1

It is possible for the noise on the bus to corrupt the detection of the first received symbol, thus compromising the outcome of the polarity detection. If the polarity is not detected correctly, invert the state of POL of the affected node to overwrite the outcome of the incorrect polarity correction, while keeping the state of its Pin AUTO_DIS unchanged. If the network resets, restore the state of POL on all nodes to its initial value.

For the receivers, $\overline{\text{FAULT}}$ stays at logic low from the assertion of $\overline{\text{RE}}$ until the first successful symbol decoding. This indicates whether the receiver node detects the first symbol. If $\overline{\text{FAULT}}$ remains asserted beyond the allowed timeframe after the transmitter sends the first symbol, the system host determines that the receiver did not successfully decode the first symbol and did not complete polarity detection and correction. The system host can then adjust the settings, such as receiver gain, and restart the polarity detection and correction routine.

If Pin AUTO_DIS of all nodes is set to logic high, the automatic polarity detection and correction feature is disabled, and user can correct polarity only by manually toggling Pin POL on miswired nodes. Each node's POL state can be kept even after a reset or power cycle, provided the bus connectivity remains unchanged.

In RS-485 mode, the polarity detection assumes that the initial transmitter drives the bus according to the idle state of DI defined by POL. When the receiver is enabled and RO exits its high-impedance state, the device detects the polarity and corrects it in case of miswiring. Pin $\overline{\text{FAULT}}$ deasserts when the polarity detection and correction procedure completes. Once the polarity correction completes, the device retains the polarity decision until it powers down or resets.

$\overline{\text{FAULT}}$ Pin Operation

The Pin FAULT is used for status reporting. FAULT is an active-low open-drain output that requires an external pull-up resistor to VDD. When asserted, FAULT pulls to ground under the following conditions:

- Thermal shutdown: If a thermal shutdown event triggers, FAULT remains low until the temperature drops below the threshold by the thermal shutdown hysteresis amount.
- Initialization wait time: After initial power-up, there is a 450ms to 1000ms wait time to allow the network to settle, followed by the execution of the polarity determination routine. During that wait time, the assertion of the Pin FAULT indicates that the host should wait until FAULT is released before sending data.
- Polarity determination after entering the receive mode for the first time: When the Pin RE is initially set to logic low, the Pin FAULT remains asserted until the first symbol is decoded. Once the Pin FAULT deasserts, the host can proceed with regular data transmission.

Depending on when RE is asserted, the last two FAULT conditions may overlap.

Fault Protection

The ADM6100 Pin A and Pin B feature ±25V of fault protection. The A and B data lines can withstand a continuous short to a voltage between −25V and +25V. This extended overvoltage range makes it suitable for applications where accidental shorts to local power supply lines are possible.

True Fail-Safe

The ADM6100 includes a true fail-safe feature in RS-485 mode that ensures the receiver output (RO) is driven to a known state when the receiver inputs are shorted, open, or connected to a differentially terminated transmission line with all drivers disabled for longer than 10µs (typ). When the differential receiver input voltage ($V_A - V_B$) is greater than or equal to −50mV for more than 10µs (typ), RO is logic high for POL = 0 but logic low for POL = 1, provided the automatic polarity detection and correction feature is disabled (AUTO_DIS = 1). For example, in the case of a terminated bus with all transmitters disabled, POL = 0, and AUTO_DIS = 1, when the receiver's differential input voltage is pulled to 0V by the termination resistor, the device guarantees that RO goes to logic high after 10µs (typ).

In the PoD modes, when the receiver's inputs are shorted, open, or connected to a differentially terminated transmission line with all drivers disabled, the Pin A and Pin B are both at common-mode. Since no edge is present at the receiver inputs, RO remains unchanged.

Hot-Swap Inputs

Inserting circuit boards into a hot or powered backplane can cause voltage transients on DE, $\overline{\text{RE}}$, and receiver inputs A and B, leading to data errors. For example, upon initial circuit board insertion, the host undergoes a power-up sequence. During this period, the host's logic outputs are in a high-impedance state, which makes them unable to drive the enable pins of the ADM6100 to a defined logic level. Meanwhile, leakage currents of up to 10µA

from the high-impedance output, or capacitively coupled noise from V_{DD} or GND can cause an input to drift to an incorrect logic state. To prevent such a condition from occurring, the ADM6100 features an initialization time during which the state of DE and $\overline{RE}$ has no effect on the transceiver operation, and Pin A and Pin B are in high-impedance.

Low-Power Shutdown

The ADM6100 features a low-power shutdown mode to reduce supply current when the transceiver is not active. Drive DE to logic low and $\overline{RE}$ to logic high for at least 1500ns to ensure the device is in low-power shutdown mode. The V_{CC} supply current drops to 10µA (max) when the device is in the shutdown mode. When the device is active, the ADM6100 is guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. A glitch-protection feature ensures that the device does not accidentally enter the shutdown mode when switching between transmit and receive modes.

Thermal Shutdown Protection

The ADM6100 features thermal shutdown protection. When the internal junction temperature exceeds +160°C (typ), the device disables the driver outputs, places RO in high impedance, and asserts Pin $\overline{FAULT}$ to low. The device reenables the driver outputs and receiver inputs when the junction temperature falls below +148°C (typ).

ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the ADM6100 have extra protection against static electricity. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the ADM6100 operates properly without latchup or damage. ESD protection can be tested in various ways. The transmitter outputs and receiver inputs (Pin A and Pin B) of the ADM6100 are protected to the following limits:

- ±25kV HBM
- ±15kV using the Air-Gap Discharge method specified in IEC 61000-4-2
- ±10kV using the Contact Discharge method specified in IEC 61000-4-2

Human Body Model (HBM)

Figure 44 shows the HBM test model and *Figure 45* shows the current waveform generated when ESD stress is discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

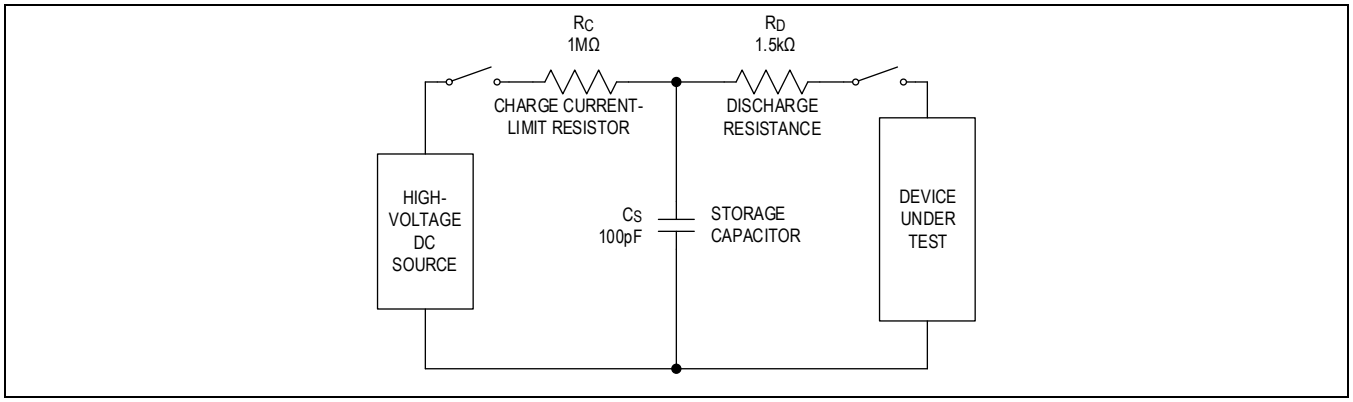


Figure 44. Human Body ESD Test Model

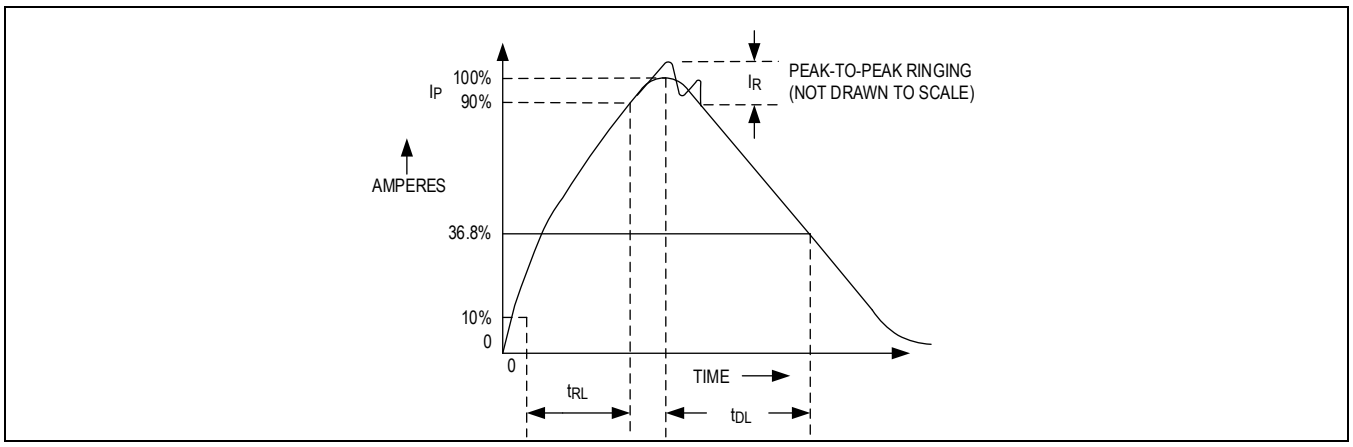


Figure 45. Human Body ESD Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The ADM6100 helps in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components. The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 test model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM. *Figure 46* shows the IEC 61000-4-2 test model and *Figure 47* shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

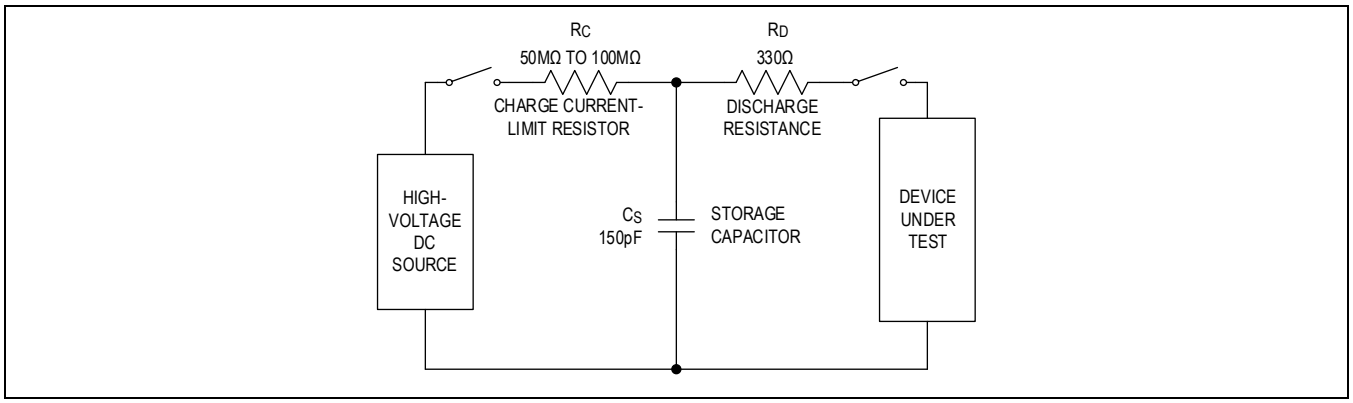


Figure 46. IEC 61000-4-2 ESD Test Model

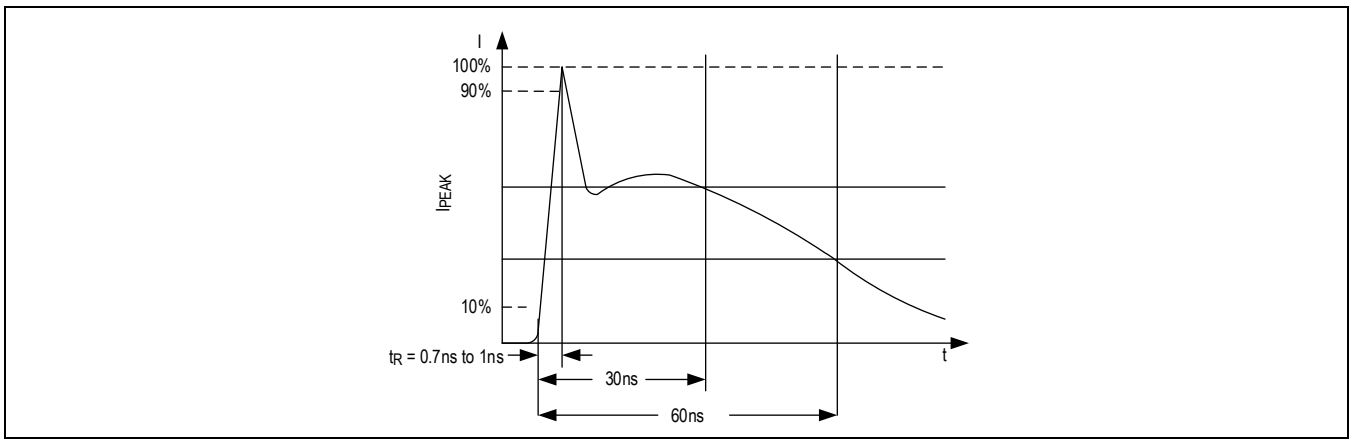


Figure 47. IEC 61000-4-2 ESD Generator Current Waveform

APPLICATIONS INFORMATION

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DD} and V_{CC} with 0.1µF ceramic capacitors to GND, respectively. Place the bypass capacitors as close as possible to the power supply input pins.

PCB Layout Recommendations

The PCB designer should follow some critical recommendations to achieve the best performance from the design:

- Keep the input/output traces as short as possible. To keep signal paths low inductance, avoid using vias.
- Have a solid ground plane underneath the entire EP area with multiple thermal vias for optimal thermal performance.
- Maximize the metal coverage for all layers, especially for top and bottom layer surrounding the A and B signal traces to shield the noise from the sensitive transceiver data signals.
- Although impedance matching is not required on the PoD signal lines, route them together as much as possible to maximize the benefit of differential signaling.
- It is recommended to place and route the two AC blocking inductors in differential mode, such that the magnetic fluxes generated by the two inductors are in opposite direction when passing differential-mode signals. Place the inductors as close to each other as possible to reduce the flux leakage and enhance the mutual differential-mode inductance.
- To ensure proper protection, connect the ground return of the protection diodes directly to the ground plane. Use a star configuration to connect the protection diode ground and device ground at a single point. Place the external protection TVS diodes as close to the connector as possible.

Multidrop Network

The ADM6100 is designed for bidirectional data communications on multidrop bus transmission lines. *Figure 48* shows a typical multidrop application circuit. In general, to minimize reflections, terminate the line at the two furthest nodes in the network with cable characteristic impedance and keep stub lengths off the main lines as short as possible. In practice, the number of nodes in the network, the cable length between the nodes, the cable type, and the power required by each of the power sink nodes limit the network topology.

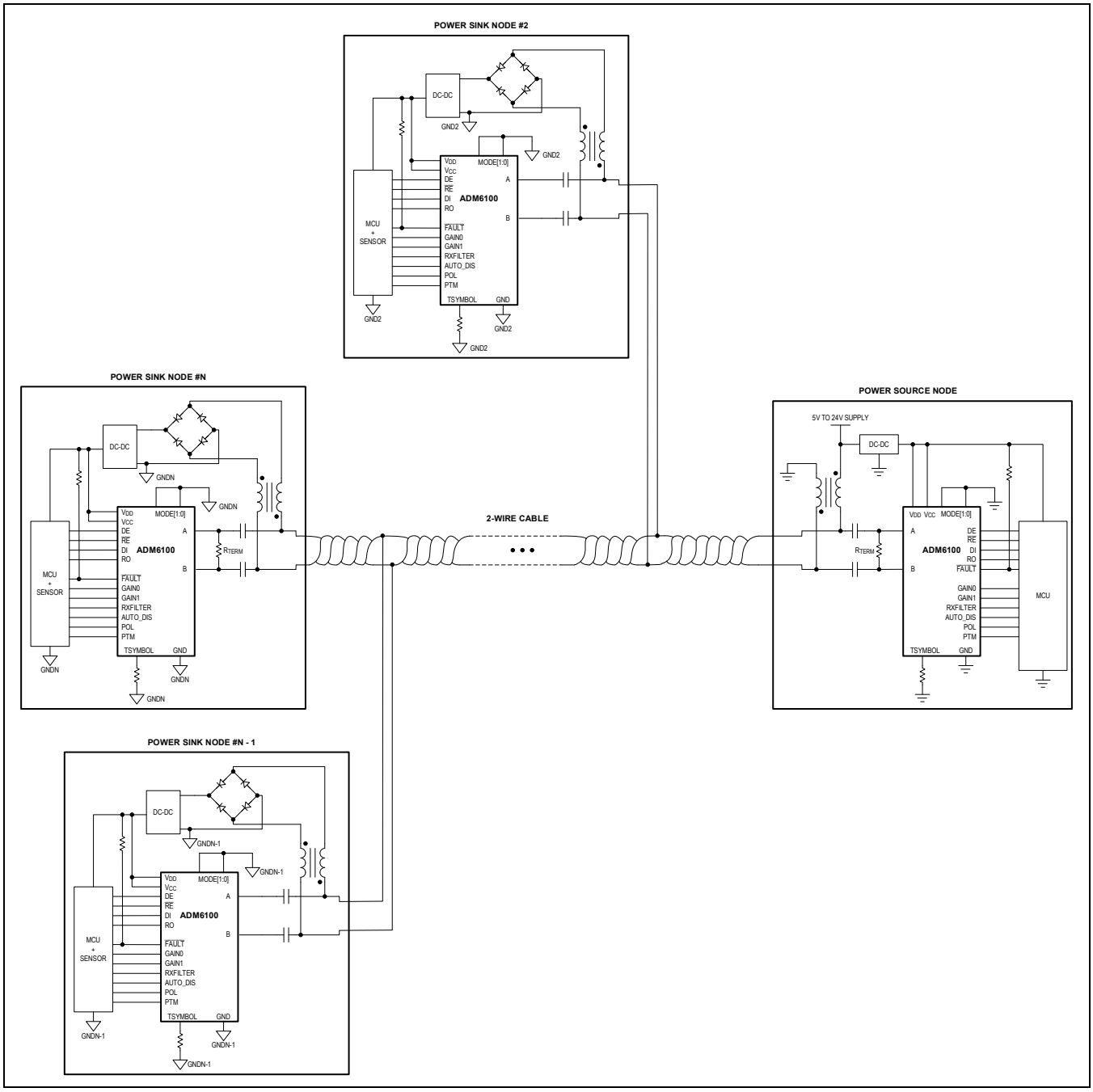


Figure 48. ADM6100 in Multidrop PoD Network

Termination

Termination is required for optimal network performance. Place the termination resistors at the two furthest extents of the network. For an example of termination resistor location in a multidrop network, see *Figure 48*. For a PoD network, place the termination resistor on the transceiver side of the AC coupling capacitors. The termination resistor value is typically between 80Ω and 150Ω. The precise value is dependent on the characteristic impedance of the cable used to connect the network.

AC-Blocking Inductors and AC Coupling Capacitors

The ADM6100 features configurable channel bandwidth, which allows the physical layer channel frequency to exceed the DI data rate. This allows the use of smaller inductors for AC blocking in PoD applications. In applications where small form factor or cost of magnetics is required, choose a smaller TSYMBOL time to minimize the required inductance for AC blocking. In applications where larger network or longer communication reach is required, choose a larger TSYMBOL time to communicate with nodes further away. In addition to the inductance, ensure that the inductors support a current rating high enough to deliver the maximum required current from the power source nodes to all power sink nodes.

The AC coupling capacitors must have low enough impedance to pass the higher channel frequencies while blocking the DC or low frequency AC power supply.

Figure 49 shows the recommended AC blocking inductor value and AC coupling capacitor value in a typical PoD multidrop network where TSYMBOL is set to 1µs to support a maximum DI data rate of 1Mbps.

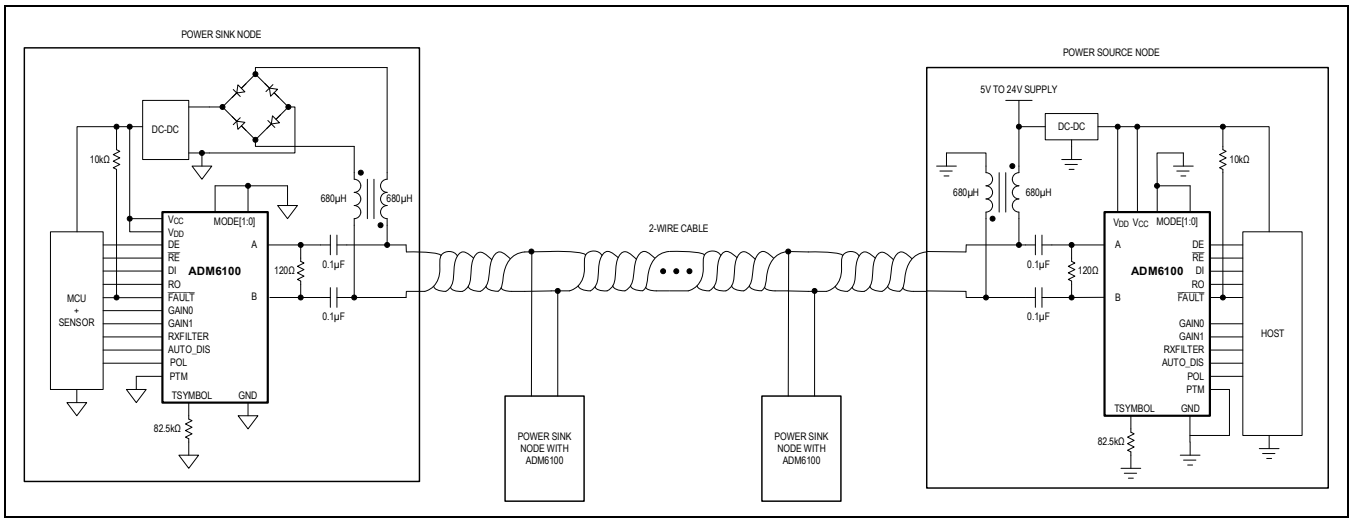
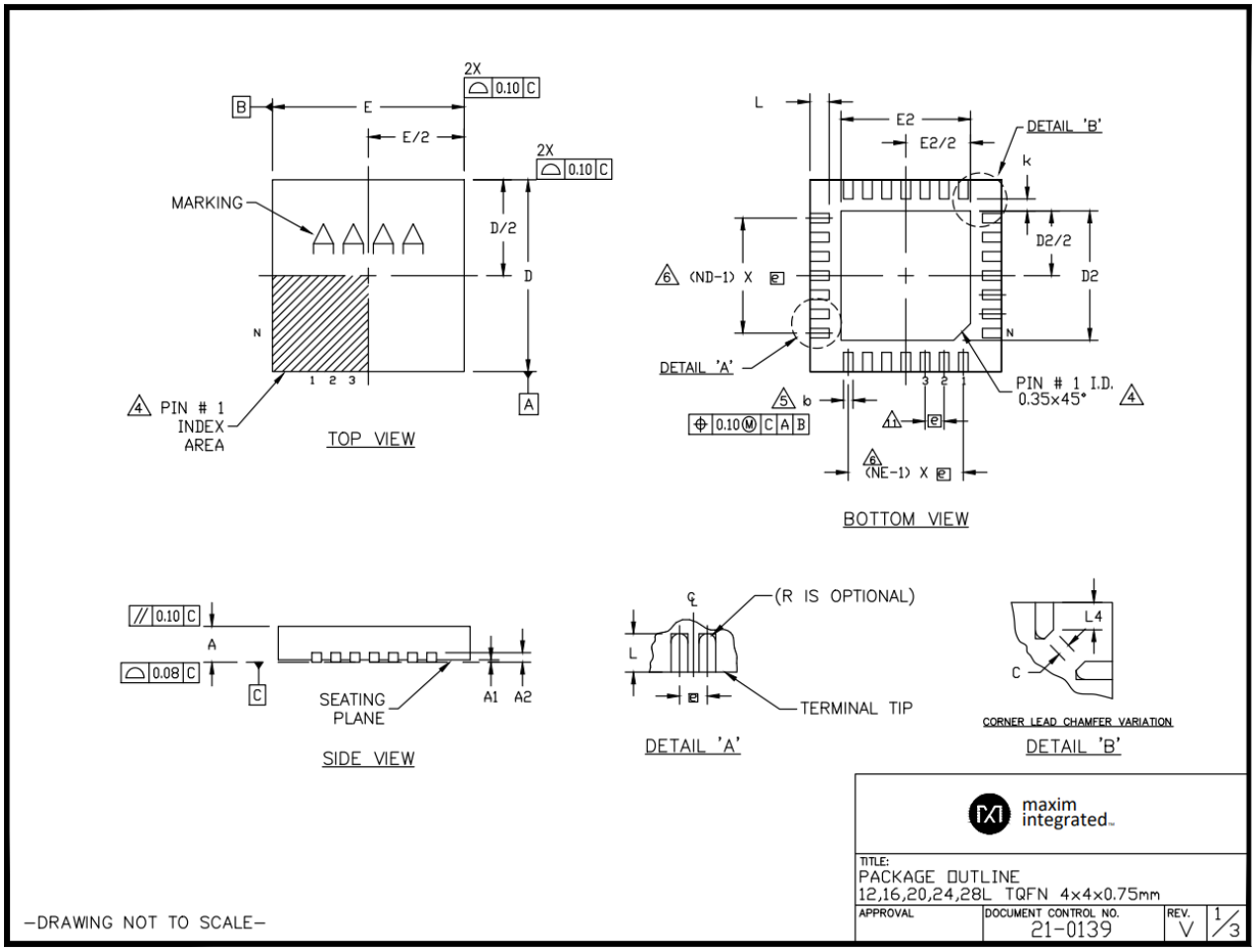


Figure 49. ADM6100 Multidrop Configuration at 1Mbps TSYMBOL Setting

OUTLINE DIMENSIONS



COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
9. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
14. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–

maxim integrated

TITLE:
PACKAGE OUTLINE
12,16,20,24,28L TQFN 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	2/3
	21-0139	V	

DIMENSION VARIATIONS

PKG. CODES	EXPOSED PAD						LEAD				CORNER LEAD CHAMFER	
	D2			E2			L			R (LEAD TIP RADIUS)	C	L4
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	REF.	REF.	REF.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T1244-3C	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T1244-4C	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T1644-3C	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T1644-4A	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T1644-4C	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T2044-2C	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T2044-3C	1.95	2.10	2.25	1.95	2.10	2.25	0.45	0.55	0.65	–	–	–
T2044-4	2.85	2.90	2.95	2.85	2.90	2.95	0.25	0.30	0.35	0.125	–	–
T2044-5	2.60	2.70	2.80	2.60	2.70	2.80	0.35	0.40	0.45	0.203	–	–
T2044-5C	2.60	2.70	2.80	2.60	2.70	2.80	0.35	0.40	0.45	0.203	–	–
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2444-2C	1.95	2.10	2.25	1.95	2.10	2.25	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2444-3C	2.45	2.60	2.63	2.45	2.60	2.63	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2444-4C	2.45	2.60	2.63	2.45	2.60	2.63	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2444MK-1	2.45	2.60	2.63	2.45	2.60	2.63	0.30	0.40	0.50	–	0.120 X 45°	0.31
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	0.30	0.40	0.50	–	–	–
T2844-1C	2.50	2.60	2.70	2.50	2.60	2.70	0.30	0.40	0.50	–	–	–
T2844N-1	2.65	2.70	2.75	2.65	2.70	2.75	0.30	0.40	0.50	–	–	–

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TITLE:
PACKAGE OUTLINE
12,16,20,24,28L TQFN 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	3/3
	21-0139	V	

ORDERING GUIDE

Table 12. Ordering Guide

PART NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING QUANTITY	PACKAGE CODE
ADM6100ATI+	−40°C to +125°C	28-Lead TQFN (4mm × 4mm)	Tray, 490	T2844+1C
ADM6100ATI+T	−40°C to +125°C	28-Lead TQFN (4mm × 4mm)	Reel, 2500	T2844+1C

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Table 13. Evaluation Board

PART NUMBER	DESCRIPTION
ADM6100EVKIT#	Evaluation Kit

#Denotes a RoHS-compliance.

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