Isolated, Single-Channel RS-232 Line Driver/Receiver

FEATURES

- 2.5kV fully isolated (power and data) RS-232 transceiver
- *iso*Power integrated, isolated DC-DC converter
- 460kbps data rate
- 1 Tx and 1 Rx
- Meets EIA/TIA-232E specifications
- ESD protection on R_{IN} and T_{OUT} pins
  - ±8kV: contact discharge
  - ±15kV: air gap discharge
- 0.1µF charge pump capacitors
- High common-mode transient immunity: >25kV/µs
- Safety and regulatory approvals
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 547V peak
  - UL 1577
    - V_{ISO} = 2500V rms for 1 minute
  - IEC/EN/CSA 62368-1
  - IEC/CSA 61010-1
- Operating temperature range: −40°C to +85°C
- Wide body, 20-lead SOIC package

APPLICATIONS

- High noise data communications
- Industrial communications
- General-purpose RS232 data links
- Industrial/telecommunications diagnostic ports
- Medical equipment

GENERAL DESCRIPTION

The ADM3251E is a high speed, 2.5kV fully isolated, single-channel RS-232/V.28 transceiver device that operates from a single 5V power supply. Due to the high ESD protection on the R_{IN} and T_{OUT} pins, the device is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently being plugged and unplugged.

The ADM3251E incorporates dual-channel digital isolators with *iso*Power™ integrated, isolated power. There is no requirement to use a separate isolated DC-DC converter. Chip-scale trans-former *i*Coupler® technology from Analog Devices, Inc., is used both for the isolation of the logic signals as well as for the integrated DC-DC converter. The result is a total isolation solution.

The ADM3251E contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to Application Note AN-0971, *Control of Radiated Emissions with isoPower Devices*, for details on board layout considerations.

The ADM3251E conforms to the EIA/TIA-232E and ITU-T V. 28 specifications and operates at data rates up to 460kbps.

Four external 0.1µF charge pump capacitors are used for the voltage doubler/inverter, permitting operation from a single 5V supply.

The ADM3251E is available in a 20-lead, wide body SOIC package and is specified over the −40°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

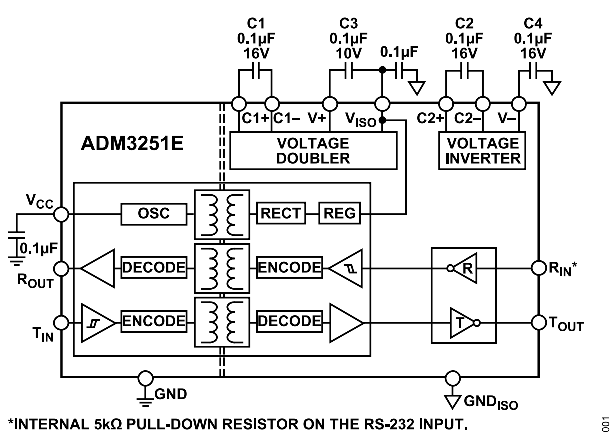

Figure 1. ADM3251E Functional Block Diagram

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.935.5565 |

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REVISION HISTORY

4/2026—Rev. G to Rev. H

Changed dc-to-dc to DC-DC (Throughout) ... 1
Changes to Features Section ... 1
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Changes to Pin Capacitance Parameter, Table 1 ... 3
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Deleted Package Characteristics Section and Table 3; Renumbered Sequentially ... 5
Changed Insulation and Safety-Related Specifications Section to Insulation Specifications Section ... 5
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Deleted DIN EN 60747-5-2 (VDE 0884 TEIL 2): 2003-01 Insulation Characteristics Section and Table 6 ... 6
Changes to Insulation Lifetime Section ... 12
Deleted Figure 18 to Figure 20 ... 12

SPECIFICATIONS

All voltages are relative to their respective ground; all minimum/maximum specifications apply over the entire recommended operating range; T_A = 25°C and V_{CC} = 5.0V (DC-DC converter enabled), unless otherwise noted.

Table 1. Electrical and Timing Characteristics for V_{CC} = 5.0V Operation

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC CHARACTERISTICS					
V_{CC} Operating Voltage Range	4.5		5.5	V	
DC-DC Converter Enable Threshold, $V_{CC(ENABLE)}$[1]	4.5			V	
DC-DC Converter Disable Threshold, $V_{CC(DISABLE)}$[1]			3.7	V	
DC-DC Converter Enabled					
Input Supply Current, $I_{CC(ENABLE)}$			110	mA	V_{CC} = 5.5V, no load
			145	mA	V_{CC} = 5.5V, R_L = 3kΩ
V_{ISO} Output[2]		5.0		V	I_{ISO} = 0µA
LOGIC					
Transmitter Input, T_{IN}					
Logic Input Current, I_{TIN}	−10	+0.01	+10	µA	
Logic Low Input Threshold, V_{TINL}			0.3 V_{CC}	V	
Logic High Input Threshold, V_{TINH}	0.7 V_{CC}			V	
Pin Capacitance		4.0		pF	
Receiver Output, R_{OUT}					
Logic High Output, V_{ROUTH}	V_{CC} − 0.1	V_{CC}		V	I_{ROUTH} = −20µA
	V_{CC} − 0.5	V_{CC} − 0.3		V	I_{ROUTH} = −4mA
Logic Low Output, V_{ROUTL}		0.0	0.1	V	I_{ROUTH} = 20µA
		0.3	0.4	V	I_{ROUTH} = 4mA
RS-232					
Receiver, R_{IN}					
EIA-232 Input Voltage Range[3]	−30		+30	V	
EIA-232 Input Threshold Low	0.6	2.0		V	
EIA-232 Input Threshold High		2.1	2.4	V	
EIA-232 Input Hysteresis		0.1		V	
EIA-232 Input Resistance	3	5	7	kΩ	
Transmitter, T_{OUT}					
Output Voltage Swing (RS-232)	±5	±5.7		V	R_L = 3kΩ to GND
Transmitter Output Resistance	300			Ω	V_{ISO} = 0V
Output Short-Circuit Current (RS-232)		±12		mA	
TIMING CHARACTERISTICS					
Maximum Data Rate	460			kbps	R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF
Receiver Propagation Delay					
t_{PHL}		190		ns	
t_{PLH}		135		ns	
Transmitter Propagation Delay		650		ns	R_L = 3kΩ, C_L = 1000pF
Transmitter Skew		80		ns	
Receiver Skew		70		ns	
Transition Region Slew Rate[3]	5.5	10	30	V/µs	+3V to −3V or −3V to +3V, V_{CC} = +3.3V, R_L = 3kΩ, C_L = 1000pF, T_A = 25°C
AC SPECIFICATIONS					
Output Rise/Fall Time, t_R/t_F (10% to 90%)		2.3		ns	C_L = 15pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[4]	25			kV/µs	V_{CM} = 1kV, transient magnitude = 800V
Common-Mode Transient Immunity at Logic Low Output[4]	25			kV/µs	V_{CM} = 1kV, transient magnitude = 800V
ESD PROTECTION (R_{IN} And T_{OUT} PINS)		±15		kV	Human body model air discharge
		±8		kV	Human body model contact discharge

SPECIFICATIONS

[1] Enable/disable threshold is the VCC voltage at which the internal DC-DC converter is enabled/disabled.

[2] To maintain data sheet specifications, do not draw current from V_{ISO}.

[3] Guaranteed by design.

[4] V_{CM} is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

All voltages are relative to their respective ground; all minimum/maximum specifications apply over the entire recommended operating range; T_A = 25°C, V_{CC} = 3.3V (DC-DC converter disabled), and the secondary side is powered externally by V_{ISO} = 3.3V, unless otherwise noted.

Table 2. Electrical and Timing Characteristics for V_{CC}= V_{ISO}= 3.3V with V_{ISO} Externally Powered

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC CHARACTERISTICS					
V_{CC} Operating Voltage Range	3.0		3.7	V	
DC-DC Converter Disable Threshold, $V_{CC(DISABLE)}$[1]			3.7	V	
DC-DC Converter Disabled					
V_{ISO}[2]	3.0		5.5	V	
Primary Side Supply Input Current, $I_{CC(DISABLE)}$			2.5	mA	No load
Secondary Side Supply Input Current, $I_{ISO(DISABLE)}$			12	mA	V_{ISO} = 5.5V, R_L = 3kΩ
Secondary Side Supply Input Current, $I_{ISO(DISABLE)}$		6.2		mA	R_L = 3kΩ
LOGIC					
Transmitter Input, T_{IN}					
Logic Input Current, I_{TIN}	−10	+0.01	+10	µA	
Logic Low Input Threshold, V_{TINL}			0.3 V_{CC}	V	
Logic High Input Threshold, V_{TINH}	0.7 V_{CC}			V	
Pin Capacitance		4.0		pF	
Receiver Output, R_{OUT}					
Logic High Output, V_{ROUTH}	V_{CC} − 0.1	V_{CC}		V	I_{ROUTH} = −20µA
	V_{CC} − 0.5	V_{CC} − 0.3		V	I_{ROUTH} = −4mA
Logic Low Output, V_{ROUTL}		0.0	0.1	V	I_{ROUTH} = 20µA
		0.3	0.4		I_{ROUTH} = 4mA
RS-232				V	
Receiver, R_{IN}					
EIA-232 Input Voltage Range[3]	−30		+30	V	
EIA-232 Input Threshold Low	0.6	1.3		V	
EIA-232 Input Threshold High		1.6	2.4	V	
EIA-232 Input Hysteresis		0.3		V	
EIA-232 Input Resistance	3	5	7	kΩ	
Transmitter, T_{OUT}					
Output Voltage Swing (RS-232)	±5	±5.7		V	R_L = 3kΩ to GND
Transmitter Output Resistance	300			Ω	V_{ISO} = 0V
Output Short-Circuit Current (RS-232)		±11		mA	
TIMING CHARACTERISTICS					
Maximum Data Rate	460			kbps	R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF
Receiver Propagation Delay					
t_{PHL}		190		ns	
t_{PLH}		135		ns	
Transmitter Propagation Delay		650		ns	R_L = 3kΩ, C_L = 1000pF
Transmitter Skew		80		ns	
Receiver Skew		55		ns	

SPECIFICATIONS

Table 2. Electrical and Timing Characteristics for V_{CC}= V_{ISO}= 3.3V with V_{ISO} Externally Powered (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Transition Region Slew Rate[3]	5.5	10	30	V/µs	+3V to −3V or −3V to +3V, V_{CC} = 3.3V, R_L = 3kΩ, C_L = 1000pF, T_A = 25°C
AC SPECIFICATIONS					
Output Rise/Fall Time, t_R/t_F (10% to 90%)		2.3		ns	C_L = 15pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[4]	25			kV/µs	V_{CM} = 1kV, transient magnitude = 800V
Common-Mode Transient Immunity at Logic Low Output[4]	25			kV/µs	V_{CM} = 1kV, transient magnitude = 800V
ESD PROTECTION (R_{IN} AND T_{OUT} PINS)		±15		kV	Human body model air discharge
		±8		kV	Human body model contact discharge

1 Enable/disable threshold is the VCC voltage at which the internal DC-DC converter is enabled/disabled.

2 To maintain data sheet specifications, do not draw current from V_{ISO}.

3 Guaranteed by design.

4 V_{CM} is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

INSULATION SPECIFICATIONS

The ADM3251E is suitable for "basic electrical insulation" only within the maximum operating ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits.

Table 3. ADM3251E 20-Lead Standard Small Outline Package [SOIC_W] Wide Body (RW-20) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	3.5	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	3.5	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	23	µm	Minimum internal
Comparative Tracking Index	CTI	>400	V	Per IEC 60112
Material Group		II		Per IEC 60664-1
Overvoltage Category per IEC 60664-1		I to IV		Rated mains voltage ≤ 150V rms
		I to III		Rated mains voltage ≤ 300V rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	°C	
Maximum Junction Temperature, Safety	$T_{JMAX,S}$	150	°C	Maximum junction temperature for isolation barrier safety
Maximum Total Power Dissipation	P_{TOT}	2.66	W	$T_A \leq 25°C$, $P_{TOT} = P_{SI} = P_{SO}$
Derating Above Ambient (T_A)		21.3	mW/°C	T_A > 25°C, see Figure 2
Junction-to-Air Thermal Impedance	$θ_{JA}$	47.05	°C/W	
IEC 60747-17 (BASIC INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	547	V peak	
Maximum Isolation Working Voltage	V_{IOWM}	387	V rms	AC voltage, end of life test, f = 60Hz
		547	V peak	DC voltage
Maximum Transient Isolation Voltage	V_{IOTM}	4000	V peak	$V_{TEST} \geq 1.2 \times V_{IOTM}$, t = 1s (100% production)
Maximum Impulse Voltage	V_{IMP}	4000	V peak	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	5200	V peak	$V_{TEST} \geq 1.3 \times V_{IMP}$ (type test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q_{pd}	≤5	pC	Method a (sample test), $V_{ini} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s

SPECIFICATIONS

Table 3. ADM3251E 20-Lead Standard Small Outline Package [SOIC_W] Wide Body (RW-20) Insulation Characteristics (Continued)

Parameter	Symbol	Value	Unit	Test Conditions/Comments
				Method b1 (100% production), $V_{ini} \geq 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s
Resistance (Input to Output)[1]	R_{IO}	$>10^{12}$	Ω	T_A = 25°C, V_{TEST} = 500V DC, t = 60s
	R_{IO_S}	$>10^{9}$	Ω	$T_A = T_S$, V_{TEST} = 500V DC, t = 60s
Capacitance (Input to Output)[1]	C_{IO}	2.2	pF	f_{TEST} = 1MHz
Climatic Category		40/85/21		
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	2500	V rms	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)

[1] Device measured as a 2-terminal device with Pin 1 to Pin 10 connected and Pin 11 to Pin 20 connected.

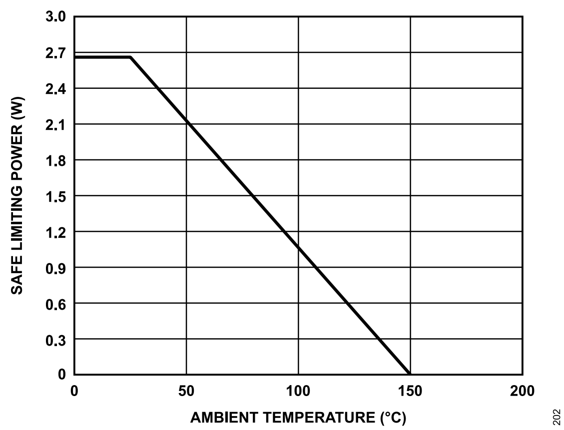

Figure 2. Thermal Derating Curve for 20-Lead Standard Small Outline Package [SOIC_W] Wide Body (RW-20), Dependence of Safety Limiting Power with Ambient Temperature per IEC 60747-17

REGULATORY INFORMATION

The ADM3251E has been approved by the organizations listed in Table 4. Copies of the relevant certificates are available at Safety and Regulatory Certifications for Digital Isolation.

Table 4. ADM3251E 20-Lead Standard Small Outline Package [SOIC_W] Wide Body (RW-20) Package Certifications

Regulatory Agency	Safety Standard/Rating	File or Certificate Number
UL	UL 1577	File E214100
	Single protection, 2500V rms isolation voltage	
CSA[1]	CSA 14-18	File 205078
	CSA/EN/IEC 62368-1	
	Basic insulation at 780V rms	
	Reinforced insulation at 390V rms	
	CSA/IEC 61010-1	
	Basic insulation at 600V rms	
	Reinforced insulation at 300V rms	
VDE	DIN EN IEC 60747-17 (VDE 0884-17)	Certificate 40061310
	Basic insulation at 547V peak	

[1] Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. The ADM3251E case material has been evaluated by CSA as Material Group II.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{CC}, V_{ISO}	−0.3V to +6V
V+	(V_{CC} − 0.3V) to +13V
V−	–13V to +0.3V
Input Voltages	
T_{IN}	−0.3V to (V_{CC} + 0.3V)
R_{IN}	±30V
Output Voltages	
T_{OUT}	±15V
R_{OUT}	−0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration	
T_{OUT}	Continuous
Power Dissipation	
θ_{JA}, Thermal Impedance	47.05°C/W
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature (Soldering, 30 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

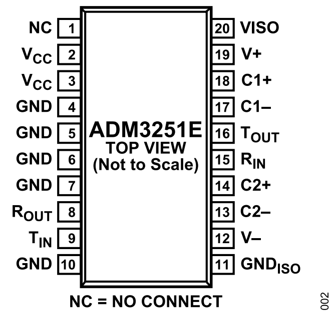

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. This pin should always remain unconnected.
2, 3	V_{CC}	Power Supply Input. A 0.1µF decoupling capacitor is required between V_{CC} and ground. When a voltage between 4.5V and 5.5V is applied to the V_{CC} pin, the integrated DC-DC converter is enabled. If this voltage is lowered to between 3.0V and 3.7V, the integrated DC-DC converter is disabled.
4, 5, 6, 7, 10	GND	Ground.
8	R_{OUT}	Receiver Output. This pin outputs CMOS logic levels.
9	T_{IN}	Transmitter (Driver) Input. This pin accepts CMOS levels.
11	GND_{ISO}	Ground Reference for Isolated RS-232 Side.
12	V−	Internally Generated Negative Supply.
13, 14	C2−, C2+	Positive and Negative Connections for Charge Pump Capacitors. External Capacitor C2 is connected between these pins; a 0.1µF capacitor is recommended, but larger capacitors up to 10µF can be used.
15	R_{IN}	Receiver Input. This input accepts RS-232 signal levels.
16	T_{OUT}	Transmitter (Driver) Output. This outputs RS-232 signal levels.
17, 18	C1−, C1+	Positive and Negative Connections for Charge Pump Capacitors. External Capacitor C1 is connected between these pins; a 0.1µF capacitor is recommended, but larger capacitors up to 10µF can be used.
19	V+	Internally Generated Positive Supply.
20	V_{ISO}	Isolated Supply Voltage for Isolator Secondary Side. A 0.1µF decoupling capacitor is required between V_{ISO} and ground. When the integrated DC-DC converter is enabled, the V_{ISO} pin should not be used to power external circuitry. If the integrated DC-DC converter is disabled, power the secondary side by applying a voltage in the range of 3.0V to 5.5V to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

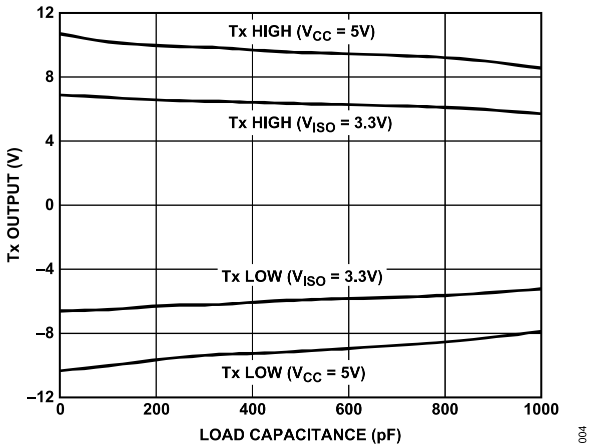

Figure 4. Transmitter Output Voltage High/Low vs. Load Capacitance at 460kbps

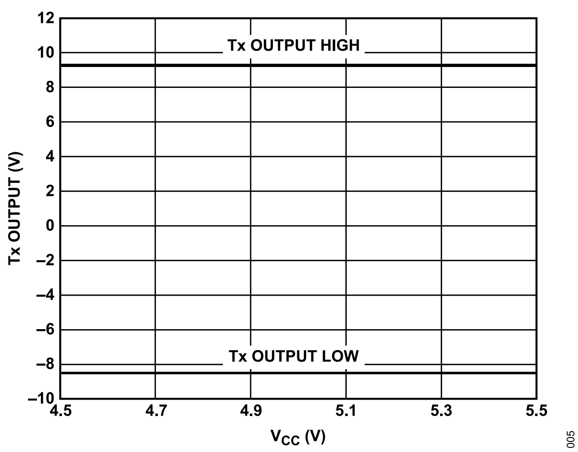

Figure 5. Transmitter Output Voltage High/Low vs. V_{CC}, R_L = 3kΩ

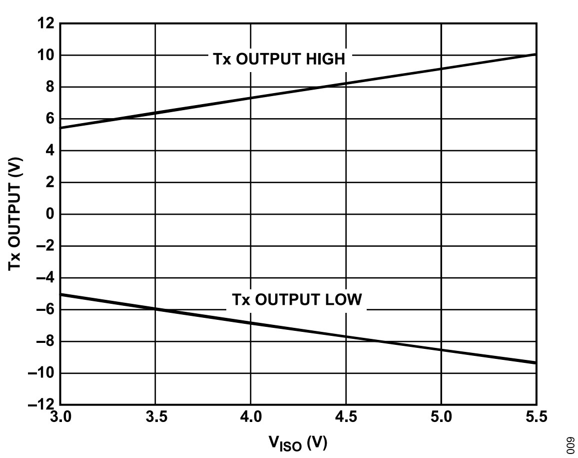

Figure 6. Transmitter Output Voltage High/Low vs. V_{ISO}, R_L = 3kΩ

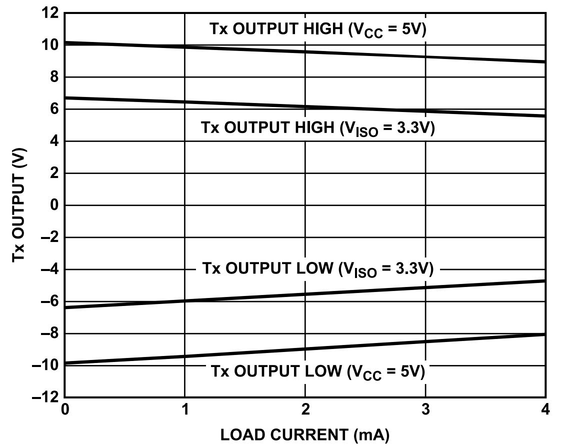

Figure 7. Transmitter Output Voltage High/Low vs. Load Current

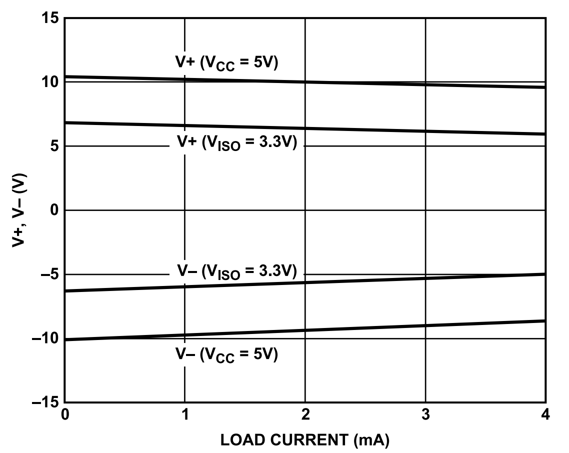

Figure 8. Charge Pump V+, V− vs. Load Current

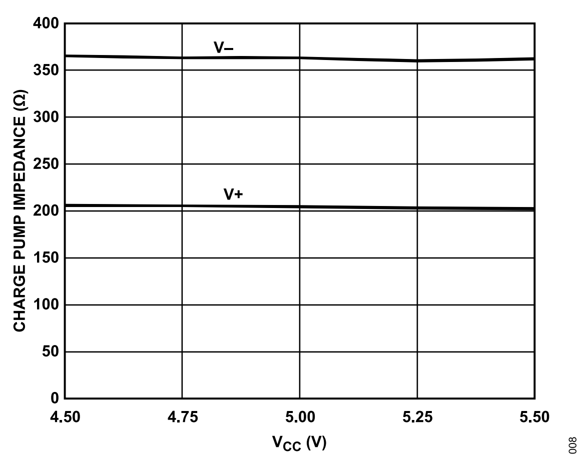

Figure 9. Charge Pump Impedance vs. V_{CC}

TYPICAL PERFORMANCE CHARACTERISTICS

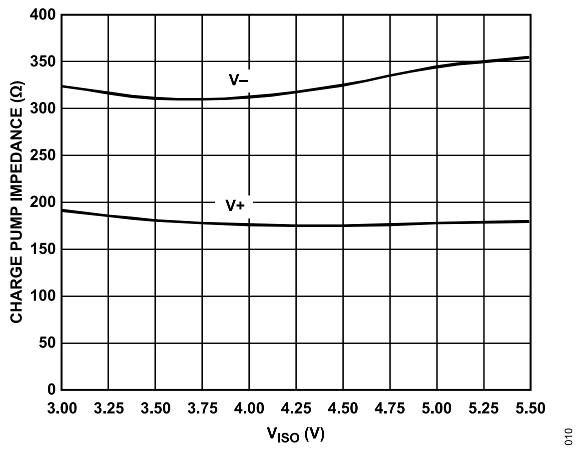

Figure 10. Charge Pump Impedance vs. V_{ISO}

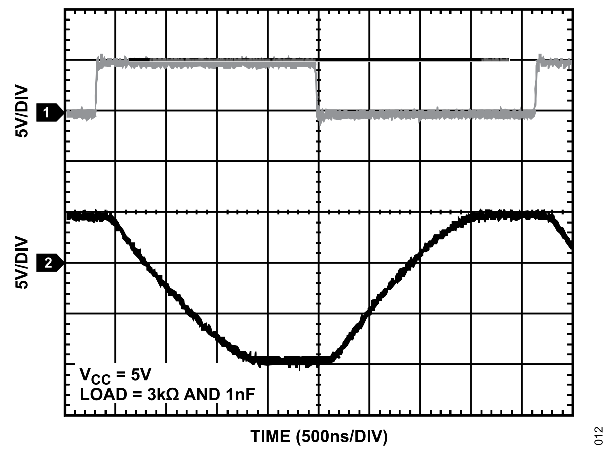

Figure 12. 460kbps Data Transmission

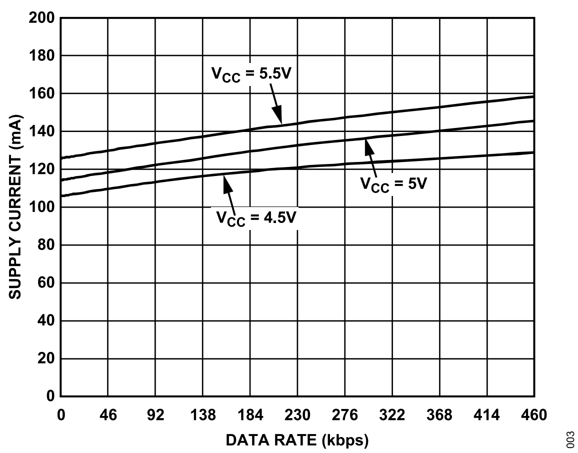

Figure 11. Primary Supply Current vs. Data Rate

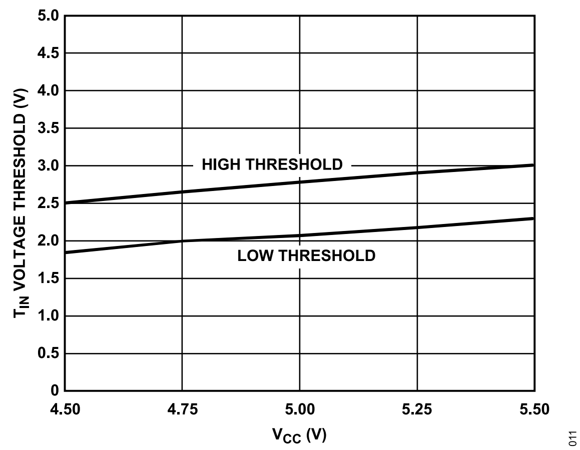

Figure 13. T_{IN} Voltage Threshold vs. V_{CC}

THEORY OF OPERATION

The ADM3251E is a high speed, 2.5kV fully isolated, single-channel RS-232 transceiver device that operates from a single power supply.

The internal circuitry consists of the following main sections:

- Isolation of power and data
- A charge pump voltage converter
- A 5.0 V logic to EIA/TIA-232E transmitter
- A EIA/TIA-232E to 5.0V logic receiver

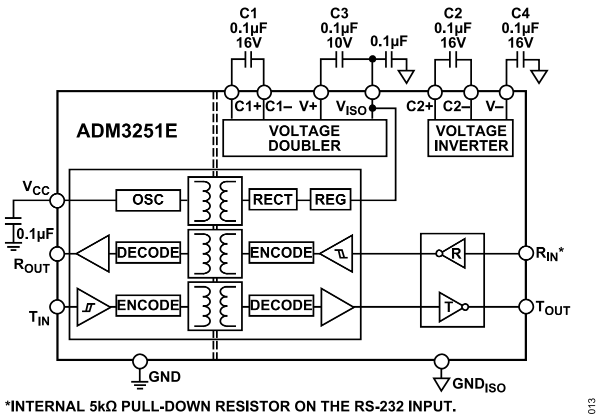

Figure 14. Functional Block Diagram

ISOLATION OF POWER AND DATA

The ADM3251E incorporates a DC-DC converter section, which works on principles that are common to most modern power supply designs. V_{CC} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power is transferred to the secondary side, where it is rectified to a high DC voltage. The power is then linearly regulated to about 5.0V and supplied to the secondary side data section and to the V_{ISO} pin. The V_{ISO} pin should not be used to power external circuitry.

Because the oscillator runs at a constant high frequency independent of the load, excess power is internally dissipated in the output voltage regulation process. Limited space for transformer coils and components also adds to internal power dissipation. This results in low power conversion efficiency.

The ADM3251E can be operated with the DC-DC converter enabled or disabled. The internal DC-DC converter state of the ADM3251E is controlled by the input V_{CC} voltage. In normal operating mode, V_{CC} is set between 4.5V and 5.5V and the internal DC-DC converter is enabled. To disable the DC-DC converter, lower V_{CC} to a value between 3.0V and 3.7V. In this mode, the user must externally supply isolated power to the V_{ISO} pin. An isolated secondary side voltage of between 3.0V and 5.5V and a secondary side input current, I_{ISO}, of 12mA (maximum) is required on the V_{ISO} pin. The signal channels of the ADM3251E then continue to operate normally.

The T_{IN} pin accepts CMOS input levels (and TTL levels at V_{CC} = 3.3V). The driver input signal that is applied to the T_{IN} pin is referenced to logic ground (GND). It is coupled across the isolation barrier, inverted, and then appears at the transceiver section, referenced to isolated ground (GND_{ISO}). Similarly, the receiver input (R_{IN}) accepts RS-232 signal levels that are referenced to isolated ground. The R_{IN} input is inverted and coupled across the isolation barrier to appear at the R_{OUT} pin, referenced to logic ground.

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. Chip-scale transformer windings couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer of the winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

There is hysteresis in the V_{CC} input voltage detect circuit. Once the DC-DC converter is active, the input voltage must be decreased below the turn-on threshold to disable the converter. This feature ensures that the converter does not go into oscillation due to noisy input power.

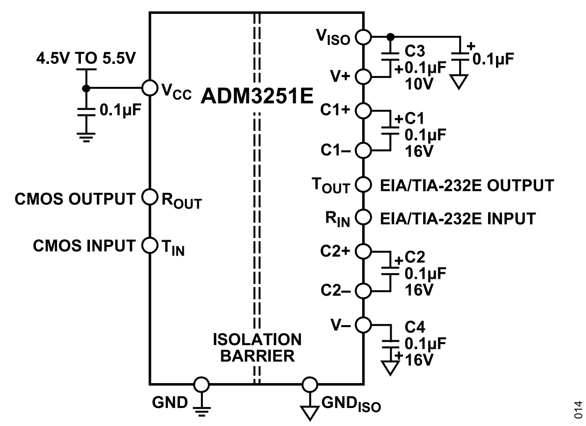

Figure 15. Typical Operating Circuit with the DC-DC Converter Enabled (V_{CC} = 4.5V to 5.5V)

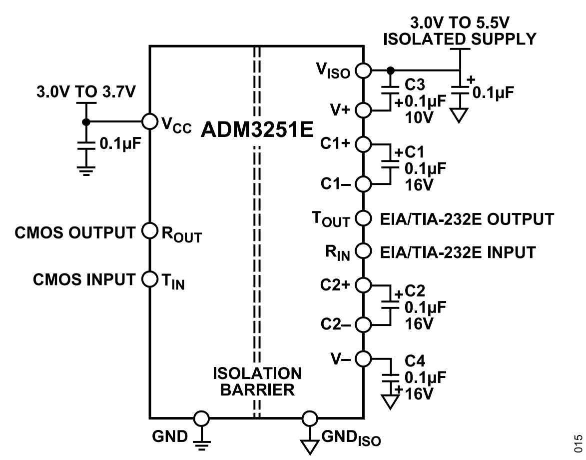

Figure 16. Typical Operating Circuit with the DC-DC Converter Disabled (V_{CC} = 3.0V to 3.7V)

THEORY OF OPERATION

CHARGE PUMP VOLTAGE CONVERTER

The charge pump voltage converter consists of a 200kHz oscillator and a switching matrix. The converter generates a ±10.0V supply from the input 5.0V level. This is done in two stages by using a switched capacitor technique as illustrated in Figure 17 and Figure 18. First, the 5.0V input supply is doubled to 10.0V by using C1 as the charge storage element. The +10.0V level is then inverted to generate −10.0V using C2 as the storage element. C3 is shown connected between V+ and V_{ISO}, but is equally effective if connected between V+ and GND_{ISO}.

Capacitor C3 and Capacitor C4 are used to reduce the output ripple. Their values are not critical and can be increased, if desired. Larger capacitors (up to 10µF) can be used in place of C1, C2, C3, and C4.

5.0V LOGIC TO EIA/TIA-232E TRANSMITTER

The transmitter driver converts the 5.0V logic input levels into RS-232 output levels. When driving an RS-232 load with V_{CC} = 5.0V, the output voltage swing is typically ±10V.

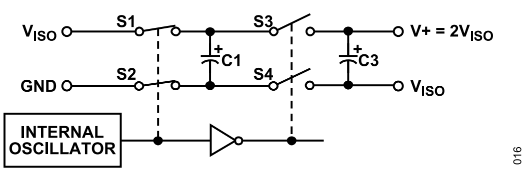

Figure 17. Charge Pump Voltage Doubler

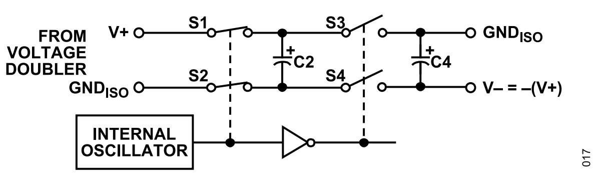

Figure 18. Charge Pump Voltage Inverter

EIA/TIA-232E TO 5V LOGIC RECEIVER

The receiver is an inverting level-shifter that accepts the RS-232 input level and translates it into a 5.0V logic output level. The input has an internal 5kΩ pull-down resistor to ground and is also protected against overvoltages of up to ±30V. An unconnected input is pulled to 0 V by the internal 5kΩ pull-down resistor. This, therefore, results in a Logic 1 output level for an unconnected input or for an input connected to GND. The receiver has a Schmitt-trigger input with a hysteresis level of 0.1V. This ensures error-free reception for both a noisy input and for an input with slow transition times.

HIGH BAUD RATE

The ADM3251E offers high slew rates, permitting data transmission at rates well in excess of the EIA/TIA-232E specifications. The RS-232 voltage levels are maintained at data rates up to 460kbps.

THERMAL ANALYSIS

Each ADM3251E device consists of three internal die, attached to a split-paddle lead frame. For the purposes of thermal analysis, it is treated as a thermal unit with the highest junction temperature reflected in the θ_{JA} value from Table 5. The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4-layer PCB with fine-width traces in still air. Following the recommendations in the PCB Layout section decreases the thermal resistance to the PCB, allowing increased thermal margin at high ambient temperatures.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3251E according to IEC 60747-17.

APPLICATIONS INFORMATION

PCB LAYOUT

The ADM3251E requires no external circuitry for its logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 19). Bypass capacitors are conveniently connected between Pin 3 and Pin 4 for V_{CC} and between Pin 19 and Pin 20 for V_{ISO}. The capacitor value should be between 0.01μF and 0.1μF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20mm.

Because it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipating into the PCB through the ground pins. If the device is used at high ambient temperatures, care should be taken to provide a thermal path from the ground pins to the PCB ground plane. The board layout in Figure 19 shows enlarged pads for Pin 4, Pin5, Pin 6, Pin 7, Pin 10, and Pin 11. Multiple vias should be implemented from each of the pads to the ground plane, which significantly reduce the temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space.

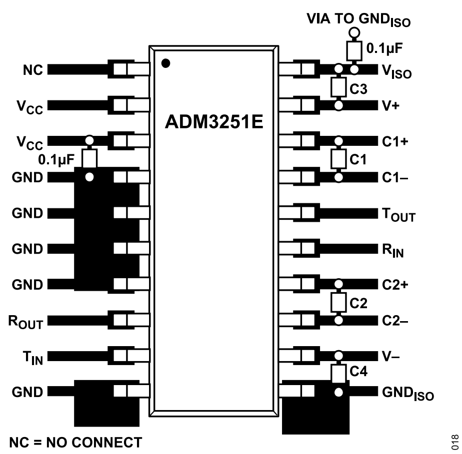

Figure 19. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side.

The power supply section of the ADM3251E uses a 300MHz oscillator frequency to pass power through its chip-scale trans-formers. Operation at these high frequencies may raise concerns about radiated emissions and conducted noise. PCB layout and construction is a very important tool for controlling radiated emissions. Refer to Application Note AN-0971, *Control of Radiated Emissions with isoPower Devices*, for extensive guidance on radiation mechanisms and board layout considerations.

EXAMPLE PCB FOR REDUCED EMI

The choice of how aggressively EMI must be addressed for a design to pass emissions levels depends on the requirements of the design as well as cost and performance trade-offs.

The starting point for this example is a 2-layer PCB. EMI reductions are relative to the emissions and noise from this board. To conform to FCC Class B levels, the emissions at these two frequencies must be less than 46dBμV/m, normalized to 3m antenna distance. As expected, EMI testing confirmed that the largest emissions peaks occur at the tank frequency and rectifier frequency.

A 6-layer PCB that employs edge guarding and buried capacitive bypassing, which are EMI mitigation techniques described in detail in Application Note AN-0971, was manufactured. The stack-up of the 6-layer test PCB is shown in Table 7. PCB layout Gerber files are available upon request.

Table 7. PCB Layers

Layer	Description
Top	Components and ground planes
Inner Layer 1	V_{CC} planes
Inner Layer 2	All tracks
Inner Layer 3	Blank
Inner Layer 4	Buried capacitive plane
Bottom	Ground planes

EMI testing was repeated on the optimized board. The resulting reduction in radiated emissions is shown in Table 8. This board meets FCC Class B standards with no external shielding by utilizing buried stitching capacitors and edge fencing.

Table 8. EMI Test Results

EMI Test Results	300MHz	600MHz
2-Layer PCB Emissions	48dB	53dB
6-Layer PCB Emissions	36dB	32dB
Achieved EMI Reduction	12dB	21dB

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1ns) pulses to be sent to the decoder via the trans-former. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions.

In the absence of logic transitions at the input for more than 1μs, periodic sets of refresh pulses (indicative of the correct input state) are sent to ensure DC correctness at the output. If the decoder receives no internal pulses for more than approximately 5μs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state by the watchdog timer circuit. This situation should occur in the ADM3251E during power-up and power-down operations only.

APPLICATIONS INFORMATION

The limitation on the ADM3251E magnetic field immunity is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The pulses at the transformer output have an amplitude of >1.0V. The decoder has a sensing threshold of about 0.5V, thus establishing a 0.5V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2;\ n = 1, 2, \ldots, N \quad (1)$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n[th] turn in the receiving coil (cm).

Given the geometry of the receiving coil internally and an imposed requirement that the induced voltage be, at most, 50% of the 0.5V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 20.

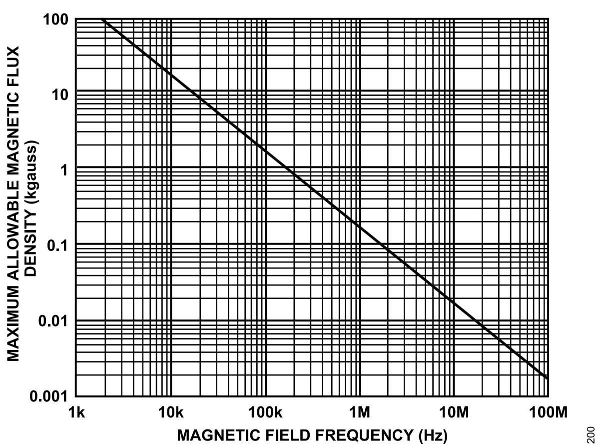

Figure 20. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1MHz, the maximum allowable magnetic field of 0.2kgauss induces a voltage of 0.25V at the receiving coil. This is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), the received pulse is reduced from >1.0V to 0.75V, which is still well above the 0.5V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the trans-formers. Figure 21 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 21, the ADM3251E is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For example, at a magnetic field frequency of 1MHz, a 0.5kA current placed 5mm away from the ADM3251E is required to affect the operation of the component.

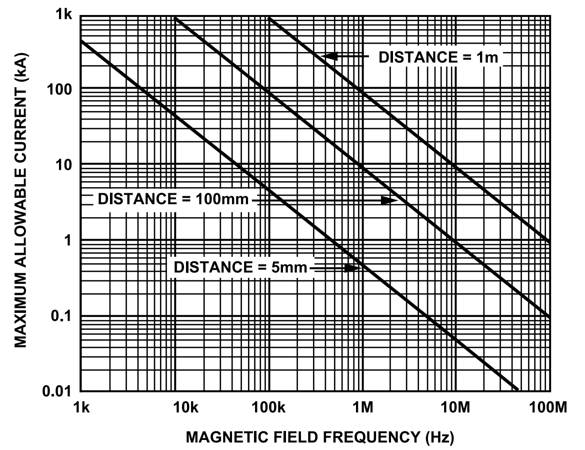

Figure 21. Maximum Allowable Current for Various Current-to-ADM3251E Spacings

In the presence of strong magnetic fields and high frequencies, any loops formed by PCB traces may induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

ISOLATED POWER SUPPLY CIRCUIT

To operate the ADM3251E with its internal DC-DC converter disabled, connect a voltage of between 3.0V and 3.7V to the V_{CC} pin and apply an isolated power of between 3.0V and 5.5V to the V_{ISO} pin, referenced to GND_{ISO}.

A transformer driver circuit with a center-tapped transformer and LDO can be used to generate the isolated supply, as shown in Figure 22. The center-tapped transformer provides electrical isolation of the 5V power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP3330 linear voltage regulator provides a regulated power supply to the bus side circuitry (V_{ISO}) of the ADM3251E.

APPLICATIONS INFORMATION

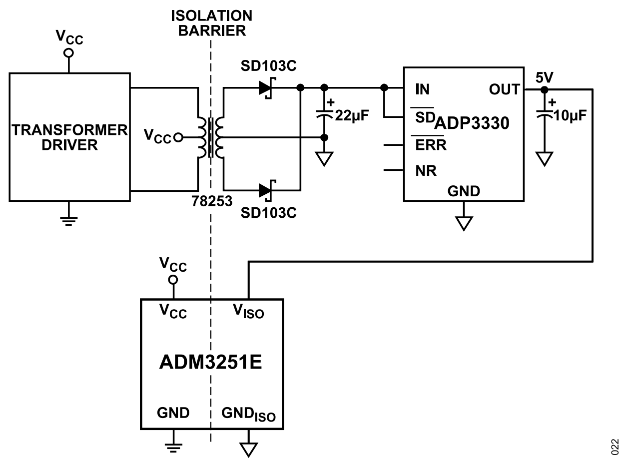

Figure 22. Isolated Power Supply Circuit

OUTLINE DIMENSIONS

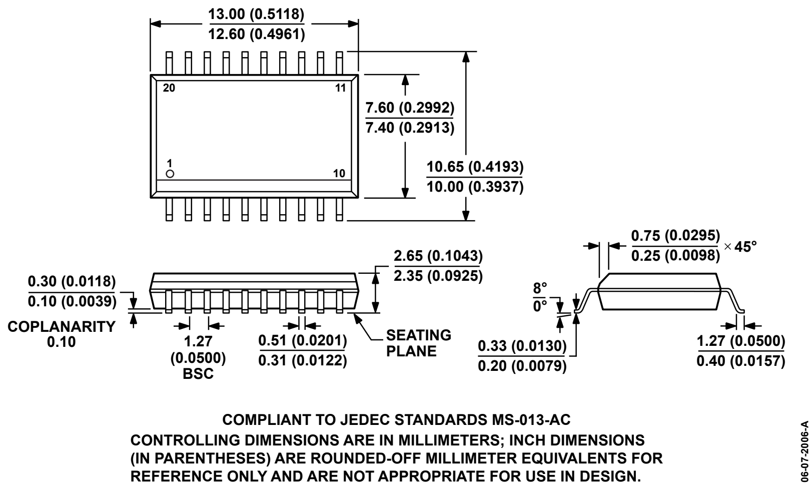

Figure 23. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-20)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3251EARWZ	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADM3251EARWZ-REEL	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADM3251EEB1Z	Evaluation Board

[1] Z = RoHS Compliant Part.