

5.7 kV rms, Signal Isolated, High Working Voltage, CAN FD Transceiver with ± 15 kV IEC ESD

FEATURES

- ▶ 5.7 kV rms signal isolated CAN FD transceiver
- ▶ 1500 V peak and dc working voltage
- ▶ 1.7 V to 5.5 V supply and logic side levels
- ▶ 4.5 V to 5.5 V supply on bus side
- ▶ ISO 11898-2:2016-compliant CAN FD
- ▶ Data rates up to 12 Mbps for CAN FD
- ▶ Low maximum loop propagation delay: 155 ns
- ▶ Extended common-mode range: ± 25 V
- ▶ Bus fault protection (CANH, CANL): ± 40 V
- ▶ ESD protection on the CANH and CANL bus pins
 - ▶ $\geq \pm 8$ kV IEC 61000-4-2 contact discharge
 - ▶ $\geq \pm 15$ kV IEC 61000-4-2 air discharge
- ▶ Passes EN 55022, Class B by 6 dB
- ▶ **Safety and regulatory approvals**
 - ▶ DIN EN IEC 60747-17 (VDE 0884-17)
 - ▶ $V_{IORM} = 1500$ V peak
 - ▶ UL 1577
 - ▶ $V_{ISO} = 5700$ V rms for 1 minute
 - ▶ IEC/EN/CSA 62368-1
 - ▶ IEC/CSA 60601-1
 - ▶ IEC/EN/CSA 61010-1
 - ▶ CQC GB 4943.1
- ▶ High common-mode transient immunity: > 50 kV/ μ s
- ▶ Industrial operating temperature range: -40°C to $+125^{\circ}\text{C}$

APPLICATIONS

- ▶ CANOpen, DeviceNet, and other CAN bus implementations
- ▶ Industrial automation
- ▶ Process control and building control
- ▶ Transport and infrastructure

GENERAL DESCRIPTION

The ADM3058E is a 5.7 kV rms isolated controller area network (CAN) physical layer transceiver with a high performance, basic feature set. The ADM3058E fully meets the CAN flexible data rate (CAN FD) ISO 11898-2:2016 requirements and is further capable of supporting data rates as high as 12 Mbps.

The device employs Analog Devices, Inc., *iCoupler*[®] technology to combine a 2-channel isolator and a CAN transceiver into a single small outline integrated circuit (SOIC) surface-mount package. The ADM3058E is a fully isolated solution for CAN and CAN FD applications. The ADM3058E provides isolation between the CAN controller and physical layer bus. Safety and regulatory approvals

FUNCTIONAL BLOCK DIAGRAM

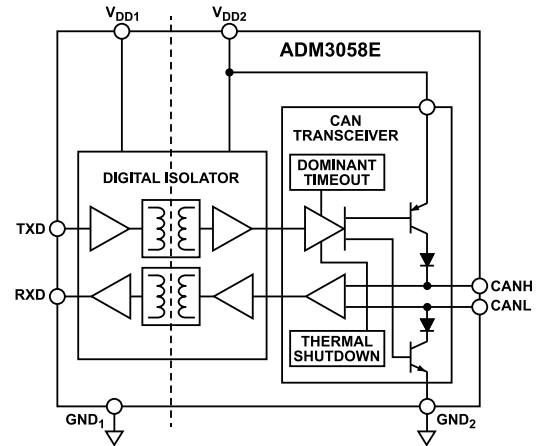


Figure 1.

for a 5.7 kV rms withstand voltage and a 1500 V peak working voltage ensure that the ADM3058E meets application isolation requirements.

Low loop propagation delays and the extended common-mode range of ± 25 V support robust communication on longer bus cables. Dominant timeout functionality protects against bus lock up in a fault condition, and current limiting and thermal shutdown features protect against output short circuits. The CAN bus input and output pins are protected to ± 40 V against accidental connection to a +24 V bus supply. The device is fully specified over the -40°C to $+125^{\circ}\text{C}$ industrial temperature range.

Rev. D

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

11/2025—Rev. C to Rev. D

Changes to Features Section.....	1
Changes to Table 4.....	8
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9/2025—Rev. B to Rev. C

Changes to Features Section.....	1
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Moved Table 1.....	4
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Deleted Insulation and Safety Related Specifications Section, Package Characteristics Section, Table 3, and Table 4; Renumbered Sequentially.....	7
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1/2025—Rev. A to Rev. B

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Changes to Table 3.....7

Changes to Regulatory Information Section and Table 5.....8

Changed DIN V VDE V 0884-11 (VDE V 0884-11) Insulation Characteristics (Pending) Section to DIN
EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics (Pending) Section..... 8

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

All voltages are relative to their respective ground, $1.7\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Typical specifications are at $V_{DD1} = V_{DD2} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Bus Side	I_{DD2}					
Recessive State			5.3	7	mA	TXD high, load resistance (R_L) = 60 Ω
Dominant State			63	75	mA	Limited by transmit dominant timeout (t_{DT}), see the Theory of Operation section, $R_L = 60\ \Omega$
70% Dominant/30% Recessive						Worst case, see the Theory of Operation section, $R_L = 60\ \Omega$
1 Mbps			50	58	mA	
5 Mbps			53	60	mA	
12 Mbps			58	65	mA	
Logic Side iCoupler Current	I_{DD1}			5.5	mA	TXD high, low, or switching
DRIVER						
Differential Outputs						See Figure 17
Recessive State Voltage						TXD high, R_L , and common-mode filter capacitor (C_F) open
CANH, CANL	V_{CANL} , V_{CANH}	2.0		3.0	V	
Differential Output	V_{OD}	-500		+50	mV	
Dominant State Voltage						TXD low, C_F open
CANH	V_{CANH}	2.75		4.5	V	$50\ \Omega \leq R_L \leq 65\ \Omega$
CANL	V_{CANL}	0.5		2.0	V	$50\ \Omega \leq R_L \leq 65\ \Omega$
Differential Output	V_{OD}	1.5		3.0	V	$50\ \Omega \leq R_L \leq 65\ \Omega$
		1.4		3.3	V	$45\ \Omega \leq R_L \leq 70\ \Omega$
		1.5		5.0	V	$R_L = 2240\ \Omega$
Output Symmetry ($V_{DD2} - V_{CANH}$ to V_{CANL})	V_{SYM}	-0.55		+0.55	V	$R_L = 60\ \Omega$, $C_F = 4.7\ \text{nF}$
Short-Circuit Current	$ I_{SC} $					R_L open
Absolute						
CANH				115	mA	$V_{CANH} = -3\ \text{V}$
CANL				115	mA	$V_{CANL} = 18\ \text{V}$
Steady State						
CANH				115	mA	$V_{CANH} = -24\ \text{V}$
CANL				115	mA	$V_{CANL} = 24\ \text{V}$
Logic Input TXD						
Input Voltage						
High	V_{IH}	$0.65 \times V_{DD1}$			V	
Low	V_{IL}			$0.35 \times V_{DD1}$	V	
Capacitance	C_{IN}		4		pF	Logic input TXD pin to GND_1
Complementary Metal-Oxide Semiconductor (CMOS) Logic Input Currents	$ I_{IH} $, $ I_{IL} $			10	μA	Input high or low
RECEIVER						
Differential Inputs						
Differential Input Voltage Range	V_{ID}					See Figure 18 , RXD capacitance (C_{RXD}) open, $-25\ \text{V} < V_{CANL}, V_{CANH} < +25\ \text{V}$
Recessive		-1.0		+0.5	V	
Dominant		0.9		5.0	V	

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Voltage Hysteresis	V_{HYS}		150		mV	
Unpowered Input Leakage Current	$ I_{IN(OFF)} $			10	μA	$V_{CANH}, V_{CANL} = 5 V, V_{DD2} = 0 V$
Input Resistance						
CANH, CANL	R_{INH}, R_{INL}	6		25	k Ω	See Figure 21
Differential	R_{DIFF}	20		100	k Ω	See Figure 20
Input Resistance Matching	m_R	-0.03		+0.03		$m_R = 2 \times (R_{INH} - R_{INL}) / (R_{INH} + R_{INL})$
Input Capacitance						
CANH, CANL	C_{INH}, C_{INL}		35		pF	See Figure 21
Differential	C_{DIFF}		12		pF	See Figure 20
Logic Output (RXD)						
Output Voltage						
Low	V_{OL}		0.2	0.4	V	Output impedance (I_{OUT}) = 2 mA
High	V_{OH}	$V_{DD1} - 0.2$			V	$I_{OUT} = -2 mA$
Short-Circuit Current	I_{OS}	7		85	mA	Output voltage (V_{OUT}) = GND ₁ or V_{DD1}
COMMON-MODE TRANSIENT IMMUNITY ¹						Common-mode voltage (V_{CM}) $\geq 1 kV$, transient magnitude $\geq 800 V$
Input High, Recessive	$ CM_H $	50	100		kV/ μs	Input voltage (V_{IN}) = V_{DD1} (TXD) or CANH/CANL recessive
Input Low, Dominant	$ CM_L $	50	100		kV/ μs	$V_{IN} = 0 V$ (TXD) or CANH/CANL dominant

¹ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining CANH/CANL recessive or $RXD \geq V_{DD1} - 0.2 V$. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining CANH/CANL dominant or $RXD \leq 0.4 V$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

SPECIFICATIONS

TIMING SPECIFICATIONS

All voltages are relative to their respective ground, $1.7\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Typical specifications are at $V_{DD1} = V_{DD2} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		12			Mbps	See Figure 2 and Figure 17, $t_{\text{BIT_TXD}}^1 = 200\text{ ns}$, $R_L = 60\ \Omega$, load capacitance (C_L) = 100 pF
Propagation Delay from TXD to Bus						
Recessive to Dominant	$t_{\text{TXD_DOM}}$		35	60	ns	
Dominant to Recessive	$t_{\text{TXD_REC}}$		45	70	ns	
Transmit Dominant Timeout	t_{DT}	1175		4000	μs	TXD low, see Figure 3
RECEIVER						
Loop Propagation Delay						
Falling Edge (TXD to RXD)	$t_{\text{LOOP_FALL}}$			155	ns	
Rising Edge (TXD to RXD)	$t_{\text{LOOP_RISE}}$			155	ns	
Loop Delay Symmetry (Minimum Recessive Bit Width)	$t_{\text{BIT_RXD}}$					
2 Mbps		450		550	ns	$t_{\text{BIT_TXD}} = 500\text{ ns}$
5 Mbps		160		220	ns	$t_{\text{BIT_TXD}} = 200\text{ ns}$
8 Mbps		85		140	ns	$t_{\text{BIT_TXD}} = 125\text{ ns}$
12 Mbps		50		91.6	ns	$t_{\text{BIT_TXD}} = 83.3\text{ ns}$

¹ $t_{\text{BIT_TXD}}$ is the bit time at the TXD pin as transmitted by the CAN controller.

Timing Diagrams

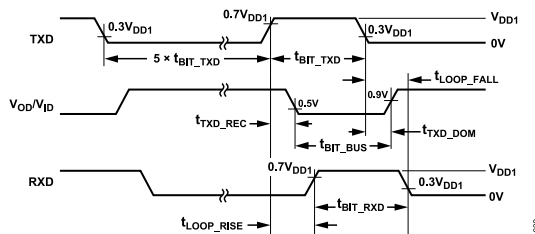


Figure 2. Transceiver Timing Diagram

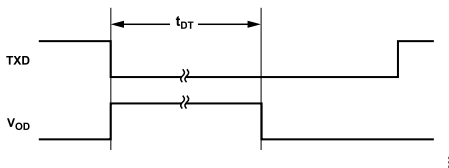


Figure 3. Dominant Timeout, t_{DT}

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INSULATION SPECIFICATIONS

The ADM3058E is suitable for "safe electrical insulation" only within the safety limiting ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits.

Table 3. ADM3058E 8-Lead Increased Creepage SOIC [SOIC_IC] (RI-8-1) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	8.3	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	8.3	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	42	μm	Minimum internal
Comparative Tracking Index	CTI	>600	V	Per IEC 60112
Material Group		I		Per IEC 60664-1
Overvoltage Category per IEC 60664-1		I to IV		Rated mains voltage ≤ 150V rms
		I to IV		Rated mains voltage ≤ 300V rms
		I to IV		Rated mains voltage ≤ 600V rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T _S	150	°C	
Maximum Total Power Dissipation	P _{TOT}	1.28	W	T _A ≤ 25°C, P _{TOT} = P _{SI} = P _{SO}
Derating Above Ambient (T _A)		10.24	mW/°C	T _A > 25°C, see Figure 4
Junction-to-Air Thermal Impedance	θ _{JA}	97	°C/W	See the Thermal Characteristics section
IEC 60747-17 (REINFORCED INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V _{IORM}	1500	V peak	
Maximum Isolation Working Voltage	V _{IOWM}	1061	V rms	AC voltage, end of life test, f = 60 Hz
		1500	V peak	DC voltage
Maximum Transient Isolation Voltage	V _{IOTM}	8000	V peak	V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)
Maximum Impulse Voltage	V _{IMP}	8000	V peak	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V _{IOSM}	10000	V peak	V _{TEST} ≥ 1.3 × V _{IMP} minimum 10 kV (type test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q _{pd}	≤5	pC	Method a (sample test), V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s Method b1 (100% production), V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s, V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s
Resistance (Input to Output) ¹	R _{IO}	>10 ¹²	Ω	T _A = 25°C, V _{TEST} = 500 V dc, t = 60 s
	R _{IO_S}	>10 ⁹	Ω	T _A = T _S , V _{TEST} = 500 V dc, t = 60 s
Capacitance (Input to Output) ¹	C _{IO}	0.9	pF	f _{TEST} = 1 MHz
Climatic Category		40/125/21		
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V _{ISO}	5700	V rms	V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)

¹ Device measured as a 2-terminal device with Pin 1 to Pin 4 connected and Pin 5 to Pin 8 connected.

SPECIFICATIONS

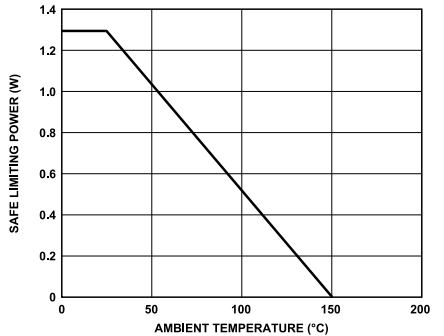


Figure 4. Thermal Derating Curve for 8-Lead Increased Creepage SOIC [SOIC_IC] (RI-8-1) Package, Dependence of Safety Limiting Power with Ambient Temperature per IEC 60747-17

REGULATORY INFORMATION

The ADM3058E has been approved by the organizations listed in [Table 4](#). Copies of the relevant certificates are available at [Safety and Regulatory Certifications for Digital Isolation](#).

Table 4. ADM3058E 8-Lead Increased Creepage SOIC [SOIC_IC] (RI-8-1) Package Certifications

Regulatory Agency	Safety Standard/Rating	File or Certificate Number
UL	UL 1577 component recognition program Single protection, 5700 V rms isolation voltage	File E214100
CSA ¹	CSA/EN/IEC 62368-1 Basic insulation at 830 V rms Reinforced insulation at 415 V rms CSA/IEC 60601-1 1 MOPP at 519 V rms 2 MOPP at 50 V rms CSA/IEC 61010-1 Basic insulation at 600 V rms Reinforced insulation at 300 V rms	File 205078
TÜV SÜD	EN/IEC 62368-1 Basic insulation at 830 V rms Reinforced insulation at 415 V rms EN 61010-1 Basic insulation at 600 V rms Reinforced insulation at 300 V rms	Certificate B 056232 0040
VDE	DIN EN IEC 60747-17 (VDE 0884-17) Reinforced insulation at 1500 V peak	Certificate 40011599
CQC	GB 4943.1 Basic insulation at 820 V rms Reinforced insulation at 410 V rms	Certificate CQC25001466836

¹ Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. ADM3058E case material has been evaluated by CSA as Material Group I.

ABSOLUTE MAXIMUM RATINGS

Pin voltages with respect to the GND_x on same side, unless otherwise noted.

Table 5.

Parameter	Rating
V _{DD1} , V _{DD2}	-0.5 V to +6 V
Logic Side Input and Output: TXD, RXD	-0.5 V to V _{DD1} + 0.5 V
CANH, CANL	-40 V to +40 V
Temperature	
Industrial Operating Range	-40°C to +125°C
Storage Range	-65°C to +150°C
Maximum Junction (T _J)	150°C
Moisture Sensitivity Level (MSL)	3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Thermal resistance and characterization parameter values specified in [Table 6](#) are defined and calculated based on the JEDEC JESD51 standards. For more details on their definition and usage, see JEDEC JESD51-12 and the [Thermal Analysis](#) section.

Table 6. Package Thermal Data

Package Type	θ_{JA}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
RI-8-1 ¹	97	106	73	8.9	°C/W

¹ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias and still air.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD RATINGS FOR ADM3058E

Table 7. ADM3058E, 8-Lead SOIC_IC

ESD Model	Withstand Threshold (V)	Class
HBM ¹	±4 kV	3A
IEC ²	±8 kV (contact discharge) to GND ₂	Level 4
	±15 kV (air discharge) to GND ₂	Level 4
	±8 kV (contact, across isolation barrier) to GND ₁	Level 4

¹ All pins, 1.5 kΩ, 100 pF.

² The CANH and CANL pins only.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

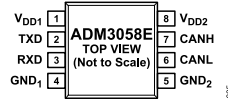


Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Power Supply, Logic Side, 1.7 V to 5.5 V. V _{DD1} requires a 0.1 μ F decoupling capacitor.
2	TXD	Driver Input Data.
3	RXD	Receiver Output Data.
4	GND ₁	Ground, Logic Side.
5	GND ₂	Ground, Bus Side.
6	CANL	CAN Low Input and Output.
7	CANH	CAN High Input and Output.
8	V _{DD2}	Power Supply, Bus Side, 4.5 V to 5.5 V. V _{DD2} requires a 0.1 μ F decoupling capacitor.

Table 9. Operational Truth Table

V _{DD1}	V _{DD2}	TXD	Mode	RXD	CANH or CANL
On	On	Low	Normal	Low	Dominant (limited by t _{DT})
On	On	High	Normal	High per bus	Recessive and set by bus
Off	On	Don't care	Normal	Indeterminate	Recessive and set by bus
On	Off	Don't care	Transceiver off	High	High-Z

TYPICAL PERFORMANCE CHARACTERISTICS

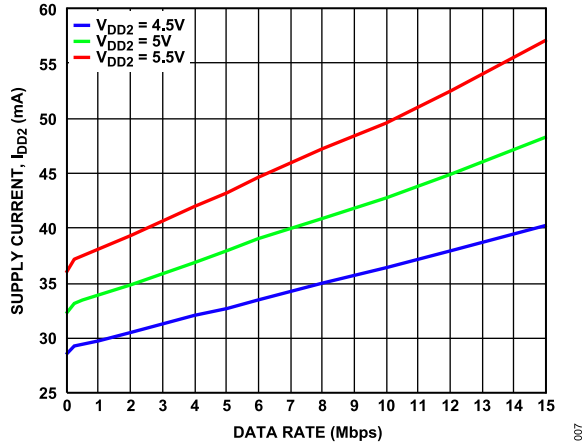


Figure 6. Supply Current (I_{DD2}) vs. Data Rate

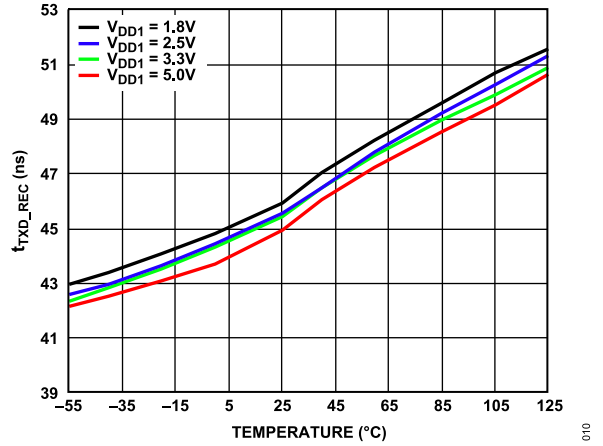


Figure 9. t_{TXD_REC} vs. Temperature

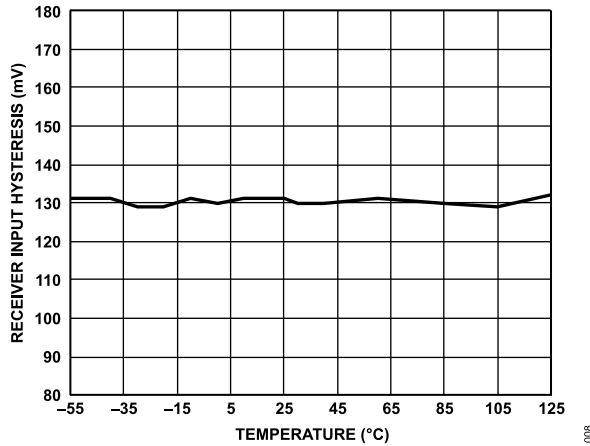


Figure 7. Receiver Input Hysteresis vs. Temperature

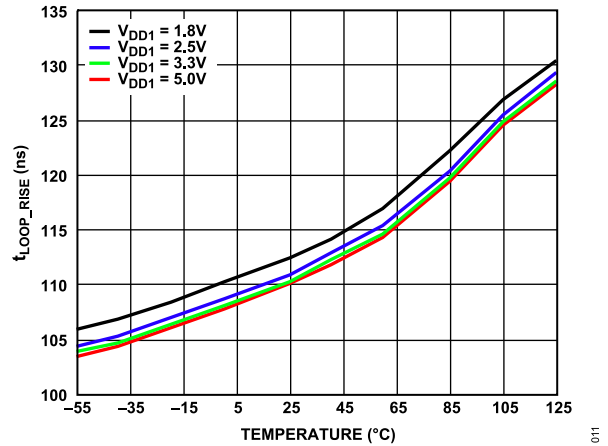


Figure 10. t_{LOOP_RISE} vs. Temperature

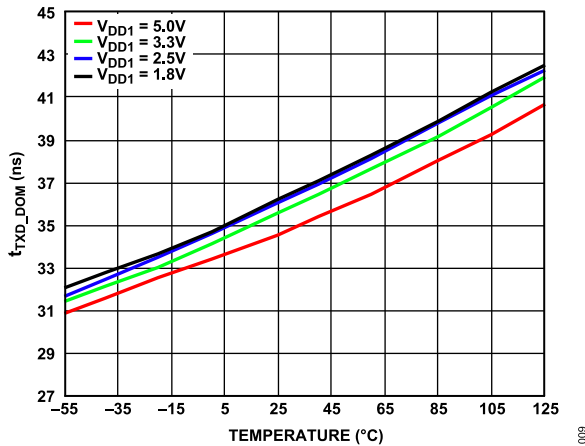


Figure 8. t_{TXD_DOM} vs. Temperature

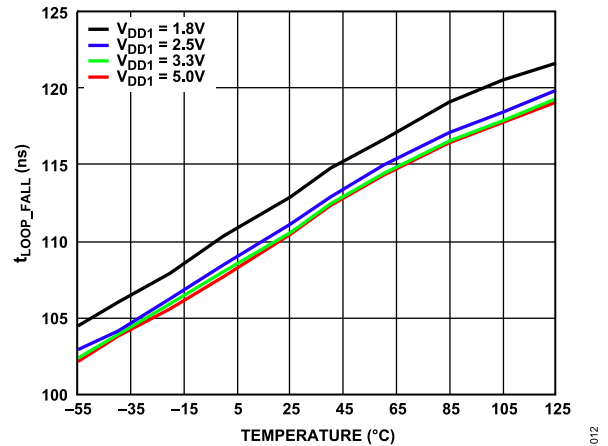


Figure 11. t_{LOOP_FALL} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

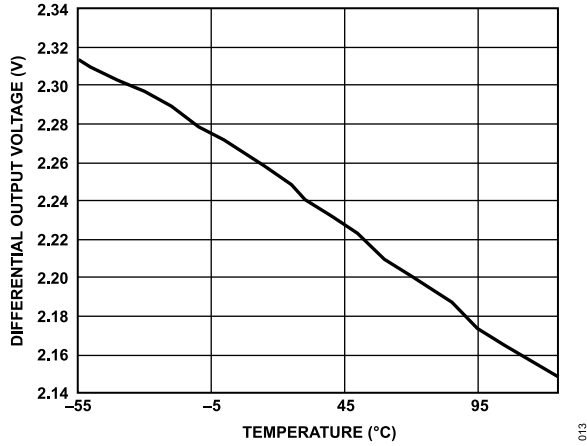


Figure 12. Differential Output Voltage vs. Temperature, $R_L = 60 \Omega$

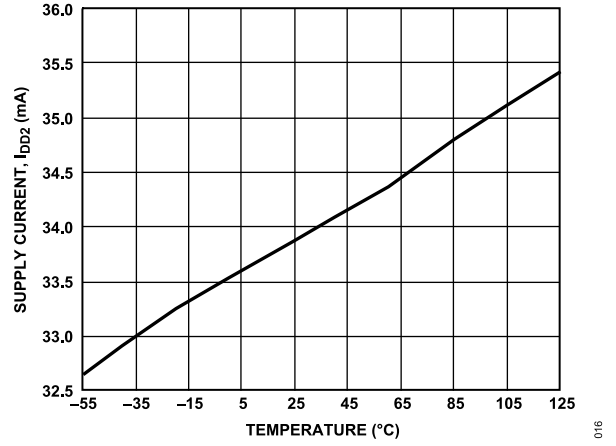


Figure 15. Supply Current (I_{DD2}) vs. Temperature

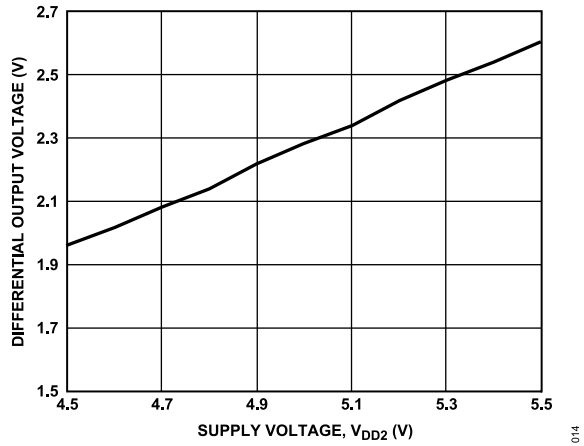


Figure 13. Differential Output Voltage vs. Supply Voltage (V_{DD2}), $R_L = 60 \Omega$

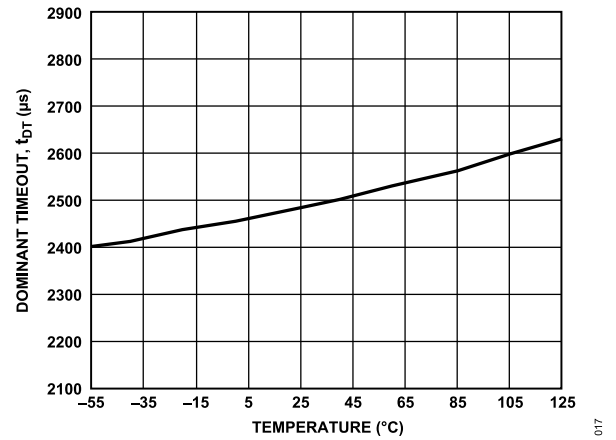


Figure 16. Dominant Timeout (t_{DT}) vs. Temperature

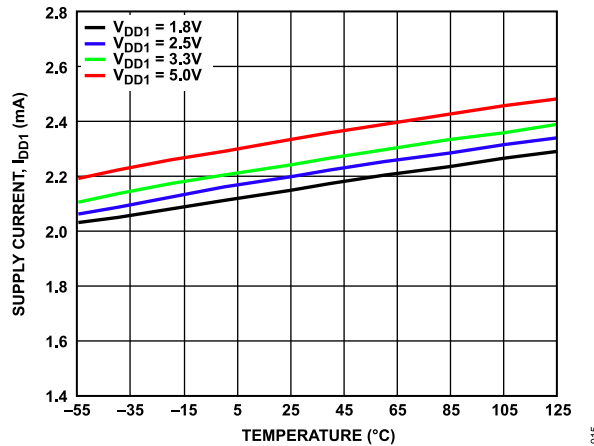


Figure 14. Supply Current (I_{DD1}) vs. Temperature

TEST CIRCUITS

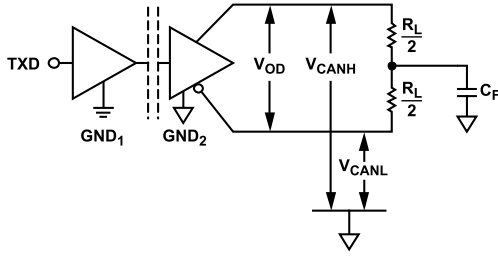


Figure 17. Driver Voltage Measurement

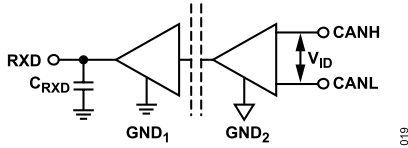
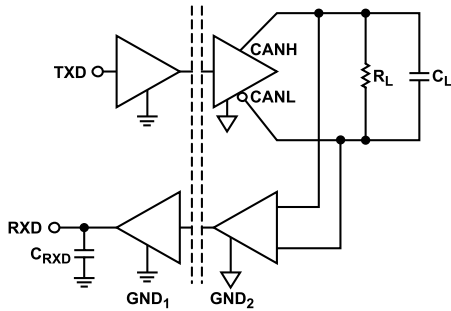


Figure 18. Receiver Voltage Measurement



NOTES
1. 1% TOLERANCE FOR ALL RESISTORS AND CAPACITORS.

Figure 19. Switching Characteristics Measurements

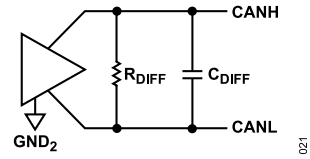


Figure 20. R_{DIFF} and C_{DIFF} Measured in Recessive State, Bus Disconnected

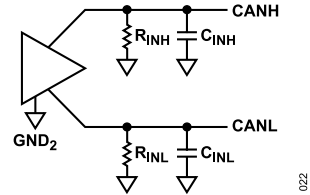


Figure 21. Input Resistance (R_{INX}) and Input Capacitance (C_{INX}) Measured in Recessive State, Bus Disconnected

TERMINOLOGY **I_{DD1}**

I_{DD1} is the current drawn by the V_{DD1} pin.

 I_{DD2}

I_{DD2} is the current drawn by the V_{DD2} pin.

 V_{OD} and V_{ID}

V_{OD} and V_{ID} are the differential voltages from the transmitter or at the receiver on the CANH and CANL pins.

 t_{TXD_DOM}

t_{TXD_DOM} is the propagation delay from a low signal on TXD to transition the bus to a dominant state.

 t_{TXD_REC}

t_{TXD_REC} is the propagation delay from a high signal on TXD to transition the bus to a recessive state.

 t_{LOOP_FALL}

t_{LOOP_FALL} is the propagation delay of a low signal on the TXD pin to the bus dominant. t_{LOOP_FALL} transitions low on the RXD pin.

 t_{LOOP_RISE}

t_{LOOP_RISE} is the propagation delay of a high signal on TXD to the bus recessive. t_{LOOP_RISE} transitions high on the RXD pin.

 t_{BIT_TXD}

t_{BIT_TXD} is the bit time at the TXD pin as transmitted by the CAN controller. See [Figure 2](#) for level definitions.

 t_{BIT_BUS}

t_{BIT_BUS} is the bit time as transmitted by the transceiver to the bus. When compared with a given t_{BIT_TXD} , a measure of bit symmetry from the TXD digital isolation channel and CAN transceiver can be determined. See [Figure 2](#) for level definitions.

 t_{BIT_RXD}

t_{BIT_RXD} is the bit time on the RXD output pin, which can be compared with t_{BIT_TXD} for a round trip measure of pulse width distortion through the TXD digital isolation channel, the CAN transceiver, and back through the RXD isolation channel.

THEORY OF OPERATION

CAN TRANSCEIVER OPERATION

The ADM3058E facilitates communication between a CAN controller and the CAN bus. The CAN controller and the ADM3058E communicate with standard 1.8 V, 2.5 V, 3.3 V, or 5.0 V CMOS levels. The internal transceiver translates the CMOS levels to and from the CAN bus.

The CAN bus has two states: dominant and recessive. The recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. In the recessive state, both the CANH pin and CANL pin are set to high impedance and are loosely biased to a single-ended voltage of 2.5 V. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 1.5 V. The transceiver transmits a dominant state by driving the single-ended voltage of the CANH line to 3.5 V and the CANL pin to 1.5 V. The recessive and dominant states correspond to CMOS high and CMOS low, respectively, on the RXD pin and TXD pin.

A dominant state from another node overwrites a recessive state on the bus. A CAN frame can be set for higher priority by using a longer string of dominant bits to gain control of the CAN bus during the arbitration phase. While transmitting, a CAN transceiver also reads back the state of the bus. When a CAN controller receives a dominant state while transmitting a recessive state during arbitration, the CAN controller surrenders the bus to the node still transmitting the dominant state. The node that gains control during the arbitration phase reads back only its own transmission. This interaction between recessive and dominant states allows competing nodes to negotiate for control of the bus while avoiding contention between nodes.

Industrial applications can have long cable runs. These long runs may have differences in local earth potential. Different sources may also power nodes. The ADM3058E transceiver has a ± 25 V common-mode range (CMR) that exceeds the ISO11898-2 requirement and further increases the tolerance to ground variation.

See the [AN-1123 Application Note](#) for additional information on CAN.

SIGNAL ISOLATION

The ADM3058E device provides galvanic signal isolation implemented on the logic side of the interface. The RXD and TXD channels are isolated using a low propagation delay on/off keying (OOK) architecture with iCoupler digital isolation technology.

The low propagation delay isolation, quick transceiver conversion speeds, and integrated form factor are critical for longer cable lengths, higher data speeds, and reducing the total solution board space. The ADM3058E isolated transceiver reduces solution board space while increasing data transfer rates over discrete optocoupler and transceiver solutions.

INTEGRATED AND CERTIFIED IEC ELECTROMAGNETIC COMPATIBILITY (EMC) SOLUTION

Typically, designers must add protections against harsh operating environments while also making the product as small as possible. To reduce the board space and the design efforts needed to meet system level ESD standards, the ADM3058E isolated transceiver has robust protection circuitry on chip for the CANH and CANL lines.

± 40 V MISWIRE PROTECTION

High voltage miswire events commonly occur when the system power supply is connected directly to the CANH and the CANL bus lines during assembly. Supplies can also be shorted by accidental damage to the field bus cables while the system is operating. Accounting for inductive kick and switching effects, the ADM3058E isolated transceiver CAN bus lines are protected against these miswire or shorting events in systems with up to nominal 24 V supplies. The CANH and CANL signal lines can withstand a continuous supply short with respect to GND₂ or between the CAN bus lines without damage. This level of protection applies when the device is either powered or unpowered.

DOMINANT TIMEOUT

The ADM3058E features a dominant timeout (t_{DT} in [Figure 3](#)). A TXD line shorted to ground or malfunctioning CAN controller are examples of how a single node can indefinitely prevent further bus traffic. t_{DT} limits how long the dominant state can transmit to the CAN bus by the transceiver. The TXD function restores when the line is presented with a logic low.

The t_{DT} minimum also inherently creates a minimum data rate. Under normal operation, the CAN protocol allows five consecutive bits of the same polarity before stuffing a bit of opposite polarity into the transmitting bit sequence. When an error is detected, the CAN controller purposely violates the bit stuffing rules by producing six consecutive dominant bits. At any given data rate, the CAN controller must transmit as many as 11 consecutive dominant bits to effectively limit the ADM3058E minimum data rate to 9600 bps.

FAIL-SAFE FEATURES

In cases where the TXD input pin is allowed to float to prevent bus traffic interruption, the TXD input channel has an internal pull-up to the V_{DD1} pin. The pull-up holds the transceiver in the recessive state.

THERMAL SHUTDOWN

The integrated transceiver is designed with thermal shutdown circuitry to protect the device from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. The circuitry disables the driver

THEORY OF OPERATION

outputs when the die temperature reaches 175°C. The drivers are enabled after the die has cooled.

APPLICATIONS INFORMATION

RADIATED EMISSIONS AND PCB LAYOUT

The ADM3058E isolated CAN transceivers pass EN 55022, Class B by 6 dB on a simple 2-layer PCB design. Neither stitching capacitance nor high voltage surface-mount technology (SMT) safety capacitors are required to meet this emission level.

PCB LAYOUT

The ADM3058E isolated CAN transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the logic input supply (V_{DD1}), and the shared CAN transceiver and digital isolator supply pin (V_{DD2}). The recommended bypass capacitor value is 0.1 μF . Note that low effective series resistance (ESR) bypass capacitors are required and must be placed as close to the chip pads as possible. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.

In applications involving high common-mode transients, minimize board coupling across the isolation barrier. Design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this equal coupling can cause voltage differences between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

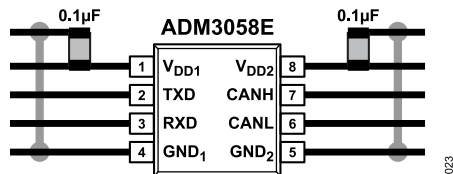


Figure 22. Recommended PCB Layout

THERMAL ANALYSIS

The ADM3058E device consists of three internal die attached to a split lead frame. For the purposes of thermal analysis, the die are treated as a single thermal unit, with the highest junction temperature reflected in the thermal parameter values from Table 6. The thermal parameter values are based on thermal simulations with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air.

θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA} and θ_{JB} can be used for first order approximation of the junction temperature in the system environment.

If an accurate thermal measurement of the board temperature near the device under test or directly on the package top surface operating in the system environment is available along with the corresponding device power dissipation, then using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the junction temperature in the system environment. Use Ψ_{JB} when the temperature measurement point is on the board or Ψ_{JT} when it is on the package top. The junction temperature is estimated using the following equation:

$$T_J = \psi_{Jx} \times P_d + T_x \quad (1)$$

where

P_d is the dissipated power.

T_x is the measured temperature at location x and x is either B for the PCB or T for the package top.

The temperature measurement point for θ_{JB} and Ψ_{JB} is on the PCB between Pin 2 and Pin 3 on the outer edge of the pin footprint. The temperature measurement point for Ψ_{JT} is the center of the top side of the package.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3058E as per IEC 60747-17.

SURFACE TRACKING

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, allowing the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and can therefore provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group.

The material group and creepage for the ADM3058E isolator are listed in Table 3.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RI-8-1	SOIC_IC	8-Lead Standard Small Outline Package, with Increased Creepage Wide Body

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
ADM3058EBRIZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_IC]	Tube, 80	RI-8-1
ADM3058EBRIZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_IC]	Reel, 1500	RI-8-1

¹ Z = RoHS Compliant Part.

EVALUATION BOARDS

Model ¹	Description
EVAL-ADM3058EEBZ	Evaluation Board

¹ Z = RoHS Compliant Part.