5.7 kV rms Signal and Power Isolated Half-Duplex RS-485 Transceiver with Fault Protection

FEATURES

- 5.7kV rms isolated half-duplex RS-485/RS-422 transceiver
- ±60V fault protection on RS-485 A and B pins
- Low radiated emissions, integrated, isolated DC-to-DC converter
- Meets EN 55032 Class B radiated emissions on a 2-layer PCB
- Robust protection on the RS-485 A and B bus pins
  - ≥ ±4kV IEC 61000-4-2 ESD
  - ±10kV HBM ESD
  - ≥ ±4kV IEC 61000-4-4 EFT
- Extended ±25V common-mode range
- Two speed options
  - ADM2895E - low speed 250kbps for EMI control
  - ADM2895E-1 - high speed 20Mbps data rate
- Flexible power supplies
  - Primary input V_{CC} supply of 3.0V to 5.5V
  - Primary logic V_{IO} supply of 1.7V to 5.5V
  - V_{SEL} pin to select isolated V_{ISO} supply of 5V (V_{CC} > 4.5V) or 3.3V
- PROFIBUS compliant for 5V V_{ISO}
- Wide operating temperature range: −40°C to +105°C
- High common-mode transient immunity: 250kV/µs
- Short-circuit, open-circuit, and floating input receiver fail-safe
- Supports >224 bus nodes (112kΩ receiver input impedance)
- Full hot-swap support (glitch free power-up/power-down)
- Safety and regulatory approvals
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - Reinforced V_{IORM} = 595V peak
  - UL 1577
    - V_{ISO}= 5700V rms for 1 minute
  - IEC/EN/CSA 62368-1
  - IEC/CSA 61010-1
  - IEC/CSA 60601-1
  - CQC GB 4943.1
- Complies with ANSI/TIA/EIA-485-A-98 and ISO 8482:1987(E)
- Outline Dimensions with 8.3mm creepage and clearance in standard pinout

APPLICATIONS

- Heating, ventilation, and air conditioning (HVAC) networks
- Industrial field buses
- Building automation
- Utility networks
- Energy meters

GENERAL DESCRIPTION

The ADM2895E/ADM2895E-1 are 5.7kV rms signal and power isolated RS-485 transceivers with ±60V fault protection on the RS-485 A and B pins. These devices are designed for balanced transmission lines and comply with ANSI/TIA/EIA-485-A-98 and ISO 8482:1987(E). The devices can pass radiated emissions testing to the EN 55032 Class B standard with margin on a 2-layer printed circuit board (PCB) with high-frequency decoupling capacitors and two small external 0402 ferrites on isolated power and ground pins. The device features an integrated, low electromagnetic interference (EMI), isolated DC-to-DC converter, which eliminates the need for an external isolated power supply. The isolation barrier provides immunity to system level electromagnetic compatibility (EMC) standards. The devices are suitable for applications that require reinforced insulation against working voltages of 400V rms and 566V DC for the lifetime of the device. The devices are protected against ±4kV contact IEC 61000-4-2 and ±15kV human body model (HBM) electrostatic discharge (ESD) events on the RS-485 A and B pins and ±8kV contact IEC 61000-4-2 ESD across the barrier without latch-up or damage.

The ADM2895E/ADM2895E-1 feature overvoltage protection on the RS-485 A and B pins to withstand up to ±60V DC or AC peak to the transceiver side GND2. This allows for robust protection against transients and accidental connection to ±12V or ±24V power supplies. The common-mode range of the device is extended to ±25V for applications with large ground offsets and long cable runs.

The ADM2895E/ADM2895E-1 are half-duplex transceivers. The ADM2895E has a reduced slew rate with a 250kbps speed for operation over long cable runs with lower emissions. The ADM2895E-1 has a high 20Mbps data rate for maximum data transfer. The high-differential output voltage makes these devices suitable for PROFIBUS® nodes when the V_{ISO} supply is configured for 5V. Two primary supplies allow different supply voltages for the logic pins (V_{IO}: 1.7V to 5.5V) and the isolated supply input (V_{CC}: 3.0V to 5.5V). The ADM2895E/ADM2895E-1 are available in the industry standard 28-lead, wide body, standard SOIC_W package with 8.3mm creepage and clearance.

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.935.5565 |

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12/2024—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

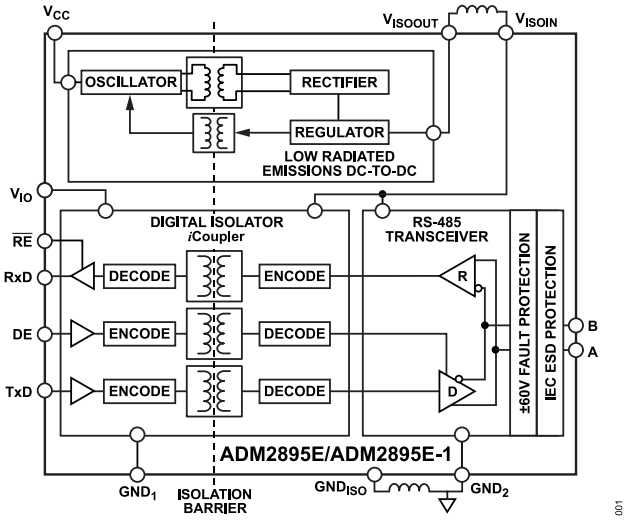

Figure 1. ADM2895E/ADM2895E-1 Functional Block Diagram

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

All voltages are relative to their respective ground, 3.0V ≤ V_{CC} ≤ 5.5V, 1.7V ≤ V_{IO} ≤ 5.5V, and T_A = T_{MIN} (−40°C) to T_{MAX} (+105°C). All minimum and maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = V_{IO} = 5V, V_{ISOOUT} output voltage (V_{ISO}) = 3.3V (V_{SEL} = GND_{ISO}), unless otherwise noted. All parameters are characterized with a BLM15HD182SN1 ferrite bead between the V_{ISOOUT} and V_{ISOIN} pins, and between the GND_{ISO} and GND_2 pins.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PRIMARY SUPPLY CURRENT						
V_{CC} Supply Current-Unloaded	I_{CC}		20	30	mA	V_{SEL} = GND_{ISO}, DE = GND_1
			28	30	mA	V_{CC} ≥ 4.5V, V_{SEL} = V_{ISO}, DE = GND_1
ADM2895E			20	50	mA	V_{SEL} = GND_{ISO}, DE = V_{IO}
ADM2895E			26	50	mA	V_{CC} ≥ 4.5V, V_{SEL} = V_{ISO}, DE = V_{IO}
ADM2895E-1				40	mA	V_{SEL} = GND_{ISO}, DE = V_{IO}
ADM2895E-1				38	mA	V_{CC} ≥ 4.5V, V_{SEL} = V_{ISO}, DE = V_{IO}
V_{IO} Logic Supply Current	I_{IO}		0.65	1	mA	DE = GND_1, TxD = V_{IO}
				5	mA	DE = TxD = GND_1
			5	10	mA	DE = V_{IO}, TxD= GND_1
ISOLATED SUPPLY CURRENT						V_{ISOIN} = 3V to 3.465V, R_L =54Ω, C_L= 100pF, see Figure 54
ADM2895E	I_{ISOIN}		50	60	mA	Data rate = 250kbps
ADM2895E-1			55	65	mA	Data rate = 20Mbps
ISOLATED DC-TO-DC CONVERTER						
V_{ISOOUT} Output Voltage	V_{ISO}	3	3.3	3.465	V	V_{SEL} = GND_{ISO}, I_{ISOOUT} = 10mA minimum to 55mA maximum[1]
		4.5	5.0	5.25	V	V_{CC} ≥ 4.5V, V_{SEL} = V_{ISO}, I_{ISOOUT} = 10mA minimum to 90mA maximum[1]
Output Current Available from V_{ISOOUT} Supply Pin	I_{ISOOUT}	90			mA	V_{CC} ≥ 4.5V, V_{SEL} = V_{ISO}, V_{ISO} ≥ 4.5V
V_{CC} Minimum Start-Up Voltage	V_{START}	3.135			V	DE = GND_1, see the Device Power-Up section
Start-Up Time	t_{START}		10		ms	DE = GND_1, see the Device Power-Up section
DRIVER						
Differential Output Voltage Loaded	$\|V_{OD2}\|$	2.0	2.1	V_{ISO}	V	V_{CC} ≥ 3.0V, V_{SEL} = GND_{ISO}, R_L = 100Ω, see Figure 52
		1.5	1.8	V_{ISO}	V	V_{CC} ≥ 3.0V, V_{SEL} = GND_{ISO}, R_L = 54Ω, see Figure 52
		2.1	3.0	V_{ISO}	V	V_{CC} ≥ 4.5V, V_{SEL} = V_{ISO}, R_L = 54Ω, see Figure 52
Over Common-Mode Range	$\|V_{OD3}\|$	1.5	1.8	V_{ISO}	V	V_{CC} ≥ 3.0V, V_{SEL} = GND_{ISO}, −7V ≤ common-mode voltage (V_{CM}) ≤ 12V, see Figure 53
		2.1	3.0	V_{ISO}	V	V_{CC} ≥ 4.5V, V_{SEL} = V_{ISO}, −7V ≤ V_{CM} ≤ 12V, see Figure 53
Δ$\|V_{OD2}\|$ for Complementary Output States	Δ$\|V_{OD2}\|$			0.2	V	R_L = 54Ω or 100Ω, see Figure 52
Common-Mode Output Voltage	V_{OC}		1.5	3.0	V	R_L = 54Ω or 100Ω, see Figure 52
Δ$\|V_{OC}\|$ for Complementary Output States	Δ$\|V_{OC}\|$			0.2	V	R_L = 54Ω or 100Ω, see Figure 52
Short-Circuit Output Current	I_{OS}	−250		+250	mA	−60V ≤ output voltage (V_O) ≤ +60V
Pin Capacitance (A, B)	C_{IN}		50		pF	Input voltage (V_{IN}) = 0.4sin(10πt × 10^6)
RECEIVER						
Differential Input Threshold Voltage						−25V ≤ V_{CM} ≤ +25V
Positive Threshold	V_{TH+}		+125	+200	mV	
Negative Threshold	V_{TH-}	−200	−125		mV	
Fail-safe Threshold	V_{TFS}	−200	−75	−10	mV	
Input Voltage Hysteresis	V_{HYS}		250		mV	V_{CM} = 0V
Fail-Safe Voltage Hysteresis	V_{HYS_FS}		50		mV	V_{CM} = 0V

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Current (A, B)	I_{IN}			143	µA	DE = GND_1, V_{CC} = powered/unpowered, differential input voltage (V_{ID}) = 12V
		−100			µA	DE = GND_1, V_{CC} = powered/unpowered, V_{ID} = −7V
Pin Capacitance (A, B)	C_{IN}		50		pF	Input voltage (V_{ID}) = 0.4sin(10πt × 10^6)
DIGITAL LOGIC INPUTS						
Input Low Voltage	V_{IL}			0.3 × V_{IO}	V	DE, $\overline{RE}$, and TxD
Input High Voltage	V_{IH}	0.7 × V_{IO}			V	DE, $\overline{RE}$, and TxD
Input Leakage Current	I_{IN}	−1	0.1	2	µA	DE, $\overline{RE}$, TxD, V_{IN} = GND_1 or V_{IO}
Input Capacitance[2]	C_{IN}		3.0		pF	Input capacitance
RxD DIGITAL OUTPUT						
Output Low Voltage	V_{OL}			0.4	V	V_{IO} = 3.6V, output current (I_{OUT}) = 2.0mA, V_{ID} ≤ −0.2V
				0.4	V	V_{IO} = 2.7V, I_{OUT} = 1.0mA, V_{ID} ≤ −0.2V
				0.2	V	V_{IO} = 1.95V, I_{OUT} = 500µA, V_{ID} ≤ −0.2V
Output High Voltage	V_{OH}	2.4			V	V_{IO} = 3.0V, I_{OUT} = −2.0mA, V_{ID} ≥ 0.2V
		2.0			V	V_{IO} = 2.3V, I_{OUT} = −1.0mA, V_{ID} ≥ 0.2V
		V_{IO} − 0.2			V	V_{IO} = 1.7V, I_{OUT} = −500µA, V_{ID} ≥ 0.2V
Three-State Output Leakage Current	I_{OZR}	−1	+0.01	+1	µA	$\overline{RE}$ = V_{IO}, RxD = GND_1 or V_{IO}
COMMON-MODE TRANSIENT IMMUNITY[3]	$\lvert CM_H \rvert$, $\lvert CM_L \rvert$	250			V/ns	V_{CM} ≥ ±1kV, transient magnitude measured at between 20% and 80% of V_{CM}, see Figure 58, $\lvert CM_H \rvert$: TxD = V_{IO}, $\lvert CM_L \rvert$: TxD = GND_1

1 These parameters include the voltage drop across the DC resistance of the BLM15HD182SN1 ferrite beads.

2 Input capacitance is from any input data pin to ground.

3 CMTI is the maximum common-mode voltage slew rate that can be sustained while maintaining specification compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode voltage is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. Guaranteed by design and characterization.

TIMING SPECIFICATIONS

All minimum and maximum specifications apply over the entire recommended operation range, V_{CC} = 3.0V to 5.5V, V_{IO} = 1.7V to 5.5V, T_A = T_{MIN} (−40°C) to T_{MAX} (+105°C). All typical specifications are at T_A = 25°C, V_{CC} = V_{IO} = 5V, V_{ISO} = 3.3V (V_{SEL} = GND_{ISO}). All parameters are characterized with a BLM15HD182SN1 ferrite bead between the V_{ISOOUT} and V_{ISOIN} pins, and between the GND_{ISO} and GND_2 pins.

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER - Slew Rate Limited (ADM2895E)						
Maximum Data Rate[1]		250			kbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		650	1200	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 54
Pulse-Width Distortion	t_{DPWD}		5	150	ns	
Rise Time/Fall Time	t_{DR}, t_{DF}		750	1200	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 54
Enable Time	t_{DZL}, t_{DZH}		400	1000	ns	R_L = 110Ω, C_L = 50pF, see Figure 4 and Figure 55
Disable Time	t_{DLZ}, t_{DHZ}		50	75	ns	R_L = 110Ω, C_L = 50pF, see Figure 4 and Figure 55
DRIVER - High Speed (ADM2895E-1)						
Maximum Data Rate[1]		20			Mbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		40	50	ns	R_L = 54Ω, C_L =100pF, see Figure 2 and Figure 54
Pulse-Width Distortion	t_{DPWD}		1.5	5	ns	
Rise Time/Fall Time	t_{DR}, t_{DF}		10	15	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 54
Enable Time	t_{DZL}, t_{DZH}		35	50	ns	R_L = 110Ω, C_L = 50pF, see Figure 4 and Figure 55

SPECIFICATIONS

Table 2. Timing Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Disable Time	t_{DLZ}, t_{DHZ}		50	66	ns	R_L = 110Ω, C_L = 50pF, see Figure 4 and Figure 55
RECEIVER - Slew Rate Limited (ADM2895E)						
Propagation Delay	t_{RPLH}, t_{RPHL}		400	700	ns	C_L = 15pF, see Figure 3 and Figure 56
Output Pulse-Width Distortion	t_{RPWD}		5	30	ns	C_L = 15pF, see Figure 3 and Figure 56
Fail-Safe Enter Delay	t_{PFSN}		1.5	2.3	µs	C_L = 15pF, see Figure 6 and Figure 59
Fail-Safe Exit Delay	t_{PFSX}		0.7	1.3	µs	C_L = 15pF, see Figure 6 and Figure 59
Enable Time	t_{RZL}, t_{RZH}		10	30	ns	R_L = 1kΩ, C_L = 15pF, see Figure 5 and Figure 56
Disable Time	t_{RLZ}, t_{RHZ}		20	40	ns	R_L = 1kΩ, C_L = 15pF, see Figure 5 and Figure 56
RECEIVER - High Speed (ADM2895E-1)						
Propagation Delay	t_{RPLH}, t_{RPHL}		60	70	ns	C_L = 15pF, see Figure 3 and Figure 56
Output Pulse-Width Distortion	t_{RPWD}		2.5	5	ns	C_L = 15pF, see Figure 3 and Figure 56
Fail-Safe Enter Delay	t_{PFSN}		110	125	ns	C_L = 15pF, see Figure 6 and Figure 59
Fail-Safe Exit Delay	t_{PFSX}		60	70	ns	C_L = 15pF, see Figure 6 and Figure 59
Enable Time	t_{RZL}, t_{RZH}		10	15	ns	R_L = 1kΩ, C_L = 15pF, see Figure 5 and Figure 56
Disable Time	t_{RLZ}, t_{RHZ}		20	25	ns	R_L = 1kΩ, C_L = 15pF, see Figure 5 and Figure 56

[1] Maximum data rate assumes a ratio of t_{DR}:t_{BIT}:t_{DF} equal to 1:1:1, where t_{BIT} is the time duration at which a bit is settled at >90% of the signal amplitude.

TIMING DIAGRAMS

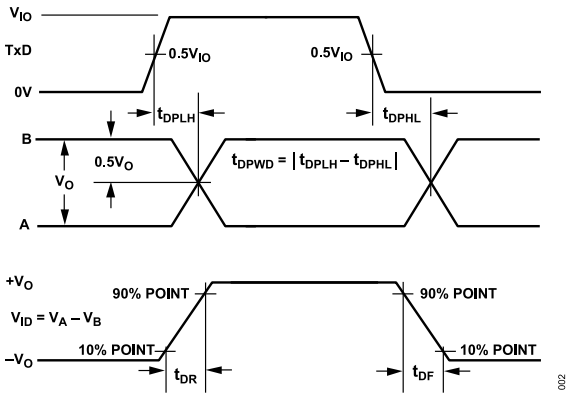

Figure 2. Driver Propagation Delay, Rise/Fall Timing

For test circuit of Figure 2, see Figure 54.

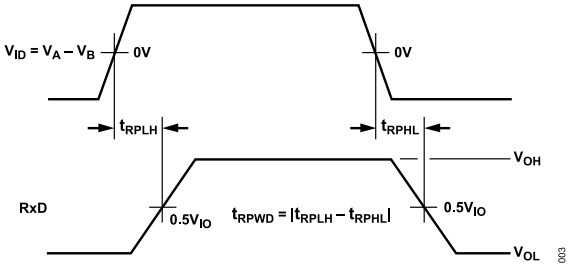

Figure 3. Receiver Propagation Delay

For test circuit of Figure 3, see Figure 56.

SPECIFICATIONS

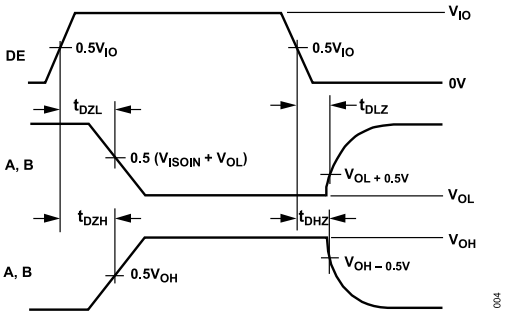

Figure 4. Driver Enable or Disable Timing

For test circuit of Figure 4, see Figure 55.

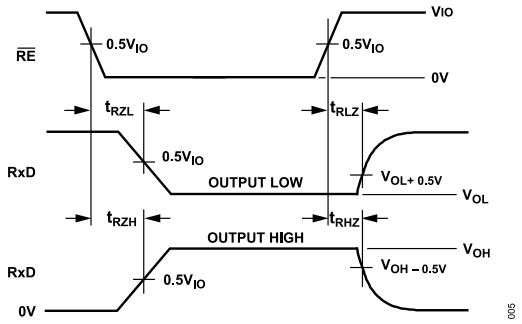

Figure 5. Receiver Enable or Disable Timing

For test circuit of Figure 5, see Figure 57.

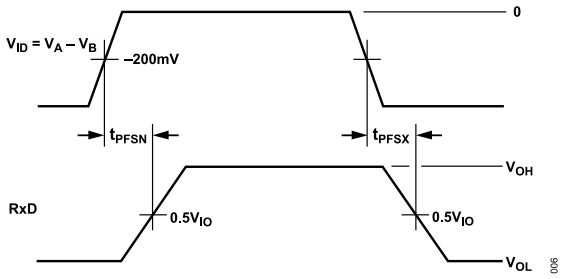

Figure 6. Fail-Safe Entry or Exit Delay Timing

For test circuit of Figure 6, see Figure 59.

SPECIFICATIONS

INSULATION SPECIFICATIONS

The ADM2895E/ADM2895E-1 are suitable for "safe electrical insulation" only within the safety limiting ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits.

Table 3. ADM2895E/ADM2895E-1, 28-Lead Wide-Body Fine Pitch SOIC [SOIC_W_FP] (RN-28-1) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	8.3	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	8.3	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	34	µm	Minimum internal
Comparative Tracking Index	CTI	600	V	Per IEC 60112
Material Group		I		Per IEC 60664-1
Overvoltage Category per IEC 60664-1		I to IV		Rated mains voltage ≤600V rms
		I to III		Rated mains voltage ≤1000V rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	°C	
Maximum Junction Temperature, Safety	$T_{JMAX,S}$	150	°C	Maximum junction temperature for isolation barrier safety
Maximum Total Power Dissipation	P_{TOT}	2.88	W	$T_A \leq 25°C$, $P_{TOT} = P_{SI} = P_{SO}$
Derating Above Ambient (T_A)		23.0	mW/°C	$T_A > 25°C$, see Figure 7
Junction-to-Air Thermal Impedance	θ_{JA}	43.5	°C/W	See Table 6
IEC 60747-17 (REINFORCED INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	595	V_{PEAK}	
Maximum Isolation Working Voltage	V_{IOWM}	421	V_{RMS}	AC voltage, end of life test, f = 60Hz
		595	V_{PEAK}	DC voltage
Maximum Transient Isolation Voltage	V_{IOTM}	8000	V_{PEAK}	$V_{TEST} \geq 1.2 \times V_{IOTM}$, t =1s (100% production)
Maximum Impulse Voltage	V_{IMP}	8000	V_{PEAK}	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	10400	V_{PEAK}	$V_{TEST} \geq 1.3 \times V_{IMP}$ minimum 10kV (sample test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q_{pd}	≤5	pC	Method a (type test): $V_{ini} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s Method b1 (100% production): $V_{ini} \geq 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s
Resistance (Input to Output)[1]	R_{IO}	$>10^{12}$	Ω	$T_A = 25°C$, V_{TEST} = 500V DC, t = 60s
	R_{IO_S}	$>10^9$	Ω	$T_A = T_S$, V_{TEST} = 500V DC, t = 60s
Capacitance (Input to Output)[1]	C_{IO}	2.2	pF	f_{TEST} = 1MHz
Climatic Category		40/105/21		
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	5700	V_{RMS}	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)

[1] Device measured as a 2-terminal device with Pin 1 to Pin 14 connected and Pin 15 to Pin 28 connected.

SPECIFICATIONS

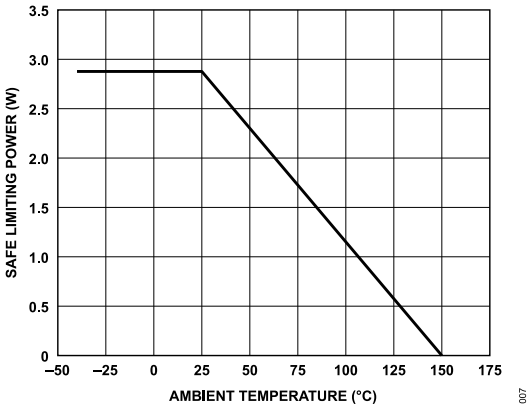

Figure 7. Thermal Derating Curve for 28-Lead Wide-Body Fine Pitch SOIC [SOIC_W_FP] (RN-28-1), Dependence of Safety Limiting Values with Ambient Temperature per IEC 60747-17

REGULATORY INFORMATION

The ADM2895E/ADM2895E-1 have been approved by the organizations listed in Table 4. Copies of the relevant certificates are available at Safety and Regulatory Certifications for Digital Isolation.

Table 4. ADM2895E/ADM2895E-1, 28-Lead Wide-Body Fine Pitch SOIC [SOIC_W_FP] (RN-28-1) Package Certifications

Regulatory Agency	Safety Standard/Rating	File or Certificate Number
UL	UL 1577 Single/Basic protection, 5700V rms isolation voltage	File E214100
CSA[1]	CSA No. 14-18 CSA/EN/IEC 62368-1: Basic insulation at 830V rms Reinforced insulation at 415V rms CSA/IEC 61010-1: Basic insulation at 600V rms Reinforced insulation at 300V rms CSA/IEC 60601-1: 1x MOPP 519V rms 2x MOPP 50V rms	File 205078
VDE	DIN EN IEC 60747-17 (VDE 0884-17): Reinforced insulation at 595V peak	Certificate 40051926
CQC	GB 4943.1: Basic insulation at 830V rms Reinforced insulation at 415V rms	Certificate CQC25001483772
TÜV Süd	EN/IEC 62368-1: Basic insulation at 830V rms Reinforced insulation at 415V rms EN 61010-1: Basic insulation at 600V rms Reinforced insulation at 300V rms	Certificate B 056232 0039

[1] Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. ADM2895E/ADM2895E-1 case material has been evaluated by CSA as Material Group I.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{CC} to GND_1	−0.5V to +6.0V
V_{IO} to GND_1	−0.5V to +7.0V
V_{ISOUT} to GND_{ISO}, V_{ISOIN} to GND_2	−0.5V to +7.0V
Digital Input Voltage (DE, $\overline{RE}$, TxD) to GND_1	−0.3V to V_{IO} + 0.3V
Digital Output Voltage (RxD) to GND_1	−0.3V to V_{IO} + 0.3V
Driver Output/Receiver Input Voltage (A, B) to GND_2	−60V to +60V
V_{SEL} to GND_{ISO}	−0.5V to V_{ISOOUT} + 0.3V
Temperature	
Ambient Operating Range (T_A)	−40°C to +105°C
Storage Range	−55°C to +150°C
Lead	
Soldering (10sec)	260°C
Vapor Phase (60sec)	215°C
Infrared (15sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to PCB design and operating environment. Careful attention to the PCB thermal design is required.

Thermal resistance values specified in Table 6 are defined and calculated based on the JEDEC JESD51 standards. For more details on their definition and usage, see JEDEC JESD51-12 and the Thermal Analysis section.

Table 6. Package Thermal Data

Package Type	θ_{JA}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
RN-28-1[1]	43.45	27.13	21.97	5.47	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

Table 7. ADM2895E/ADM2895E-1, 28-Lead Wide-Body Fine Pitch SOIC [SOIC_W_FP] (RN-28-1) ESD Characteristics

ESD Model	Withstand Threshold (kV)	Class
HBM	≥±4	3A[1]
	±10	3B[2]
CDM	1.25	C5[1]
IEC	≥±4 (contact) to GND_2	Level 2[2]
	≥±8 (contact) to GND_1	Level 4[2, 3]

[1] V_{CC}, V_{ISOOUT}, V_{ISOIN}, RxD, DE, $\overline{RE}$, and TxD only.

[2] Pin A and Pin B only.

[3] Limited by clearance across isolation barrier.

ELECTRICAL FAST TRANSIENTS (EFT) RATINGS

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-4 (IEC) per IEC 61000-4-4.

Table 8. ADM2895E/ADM2895E-1, 28-Lead Wide-Body Fine Pitch SOIC [SOIC_W_FP] (RN-28-1) EFT Characteristics

Model	Withstand Threshold (kV)	Repetition Frequency (kHz)	Class
IEC	≥±4 to GND_2	5 or 100	Exceeds Level 4[1]
	≥±4 to GND_1	5 or 100	Exceeds Level 4[1, 2]

[1] Pin A and Pin B only.

[2] Limited by clearance across isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

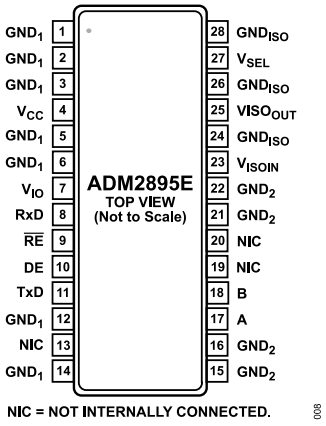

Figure 8. ADM2895E/ADM2895E-1 Pin Configuration

Table 9. ADM2895E/ADM2895E-1 Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 2, 3, 5, 6, 12, 14	GND_1	Ground 1, Logic Side.
4	V_{CC}	3.0V to 3.6V, or 4.5V to 5.5V Logic Side Power Supply. It is recommended that a 10µF and a 0.1µF decoupling capacitor be connected between V_{CC} and GND_1 (Pin 1, Pin 2, and Pin 3).
7	V_{IO}	1.7V to 5.5V Logic Side Flexible I/O Supply. It is recommended that a 0.1µF decoupling capacitor be connected between V_{IO} and GND_1 (Pin 5 and Pin 6).
8	RxD	Receiver Output Data. When the receiver is enabled ($\overline{RE}$ low) this output is high when (A − B) ≥ +200mV and low when (A − B) ≤ −200mV. This output is high when the receiver inputs are shorted, open or connected to a terminated idle bus. This output is tristated when the receiver is disabled by driving the $\overline{RE}$ pin high.
9	$\overline{RE}$	Receiver Enable Input. This pin is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
10	DE	Driver Output Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places these outputs in a high impedance state.
11	TxD	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
13, 19, 20	NIC	Not Internally Connected. This pin is not internally connected and may be left open.
15, 16, 21, 22	GND_2	Isolated Ground 2 for the Integrated RS-485 Transceiver, Bus Side.
17	A	Noninverting Driver Output/Receiver Input.
18	B	Inverting Driver Output/Receiver Input.
23	V_{ISOIN}	Isolated Transceiver Power Supply Input. This pin must be connected externally to V_{ISOOUT} (Pin 25) through one BLM15HD182SN1 ferrite. It is recommended that a reservoir capacitor of 10µF and decoupling capacitors of 10nF and 2.2pF be connected between V_{ISOIN} (Pin 23) and GND_2 (Pin 21). The 2.2pF capacitor must have a self-resonant frequency above 5GHz and be placed <2mm from V_{ISOIN} and GND_2.
24, 26, 28	GND_{ISO}	Isolated Power Supply Ground. These pins must be connected externally together and to GND_2 through one BLM15HD182SN1 ferrite.
25	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN} (Pin 23) through one BLM15HD182SN1 ferrite. It is recommended that a decoupling capacitor of 0.1µF be connected between V_{ISOOUT} and GND_{ISO} (Pin 28).
27	V_{SEL}	Output Voltage Selection. When V_{SEL} = V_{ISOOUT}, the V_{ISO} set point is 5.0V. When V_{SEL} = GND_{ISO}, the V_{ISO} set point is 3.3V.

TYPICAL PERFORMANCE CHARACTERISTICS

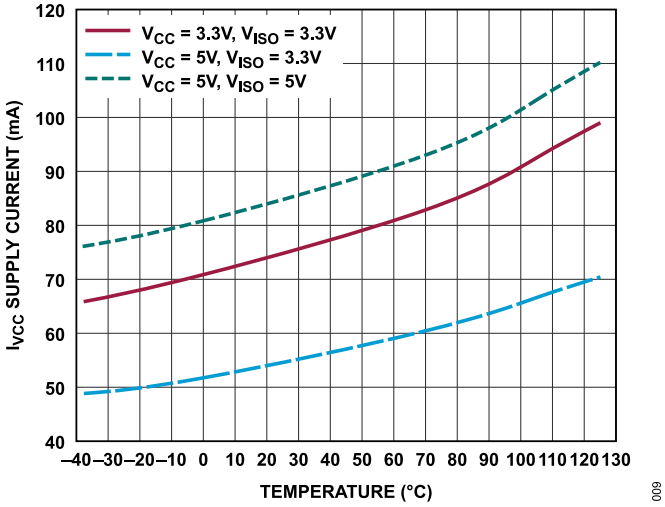

Figure 9. V_{CC} Supply Current vs. Temperature at 250kbps (ADM2895E), Unterminated Bus

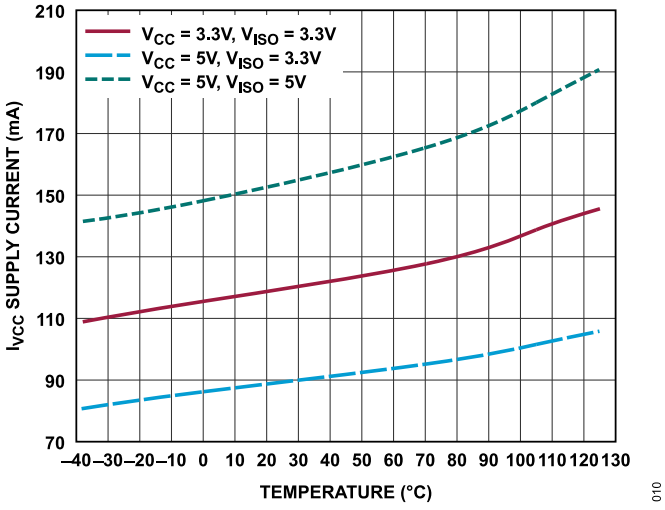

Figure 10. V_{CC} Supply Current vs. Temperature at 250kbps (ADM2895E), 120Ω Termination

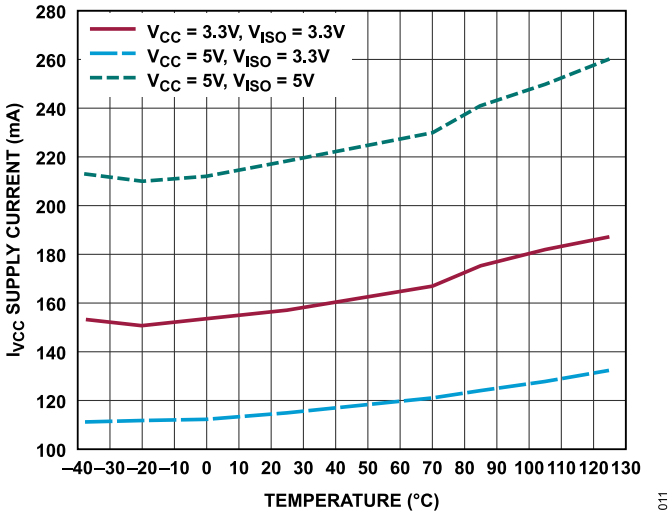

Figure 11. V_{CC} Supply Current vs. Temperature at 250kbps (ADM2895E), 54Ω Termination

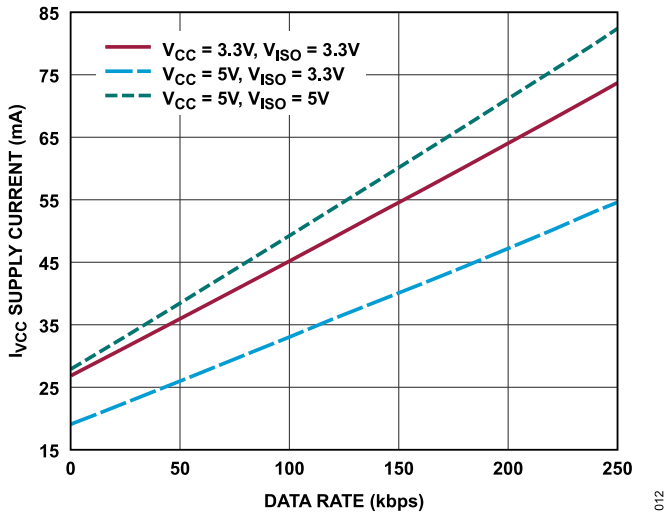

Figure 12. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E), Unterminated Bus

TYPICAL PERFORMANCE CHARACTERISTICS

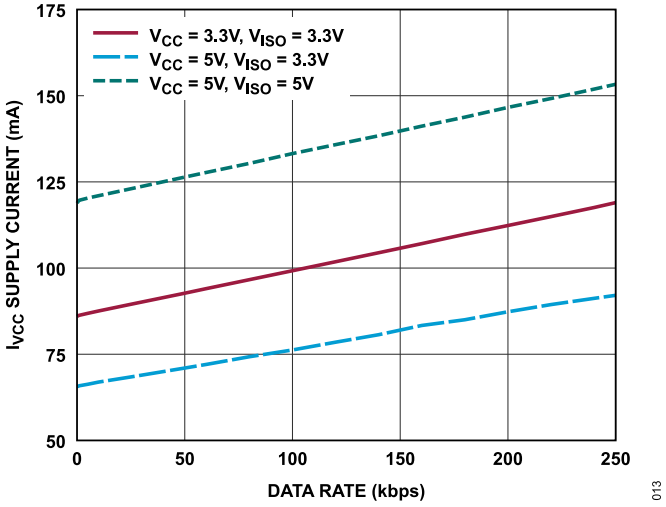

Figure 13. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E), 120Ω Termination

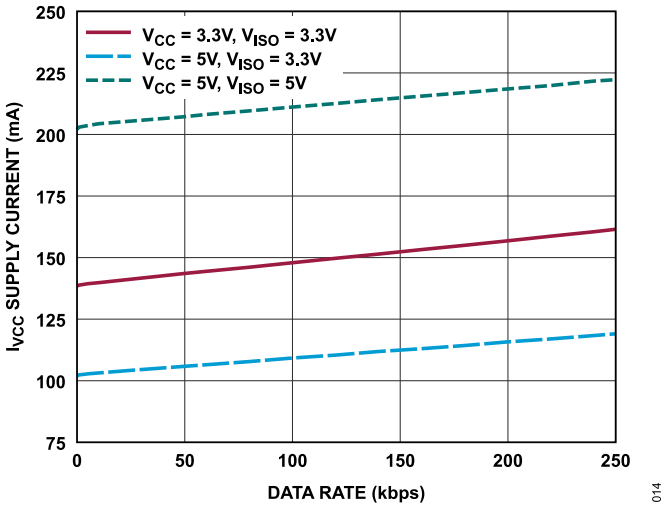

Figure 14. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E), 54Ω Termination

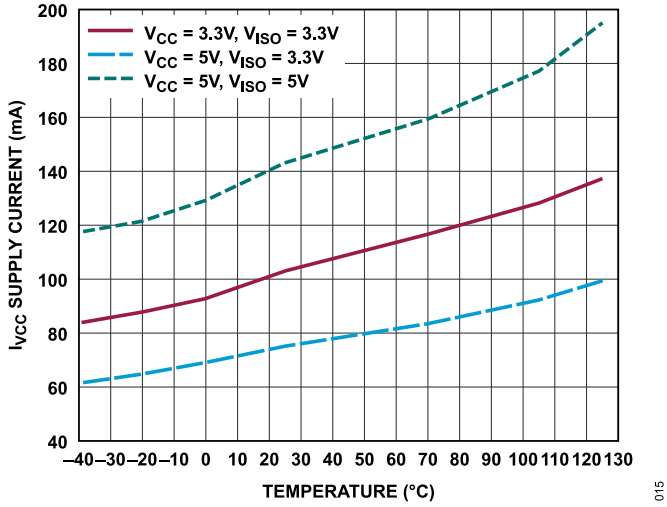

Figure 15. V_{CC} Supply Current vs. Temperature at 20Mbps (ADM2895E-1), Unterminated Bus

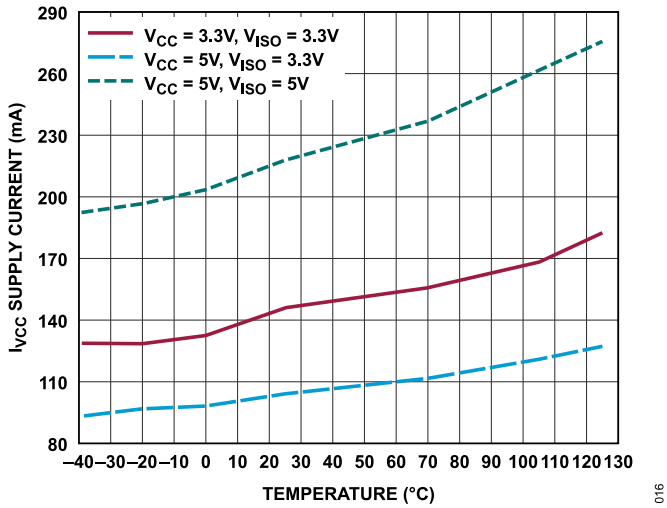

Figure 16. V_{CC} Supply Current vs. Temperature at 20Mbps (ADM2895E-1), 120Ω Termination

TYPICAL PERFORMANCE CHARACTERISTICS

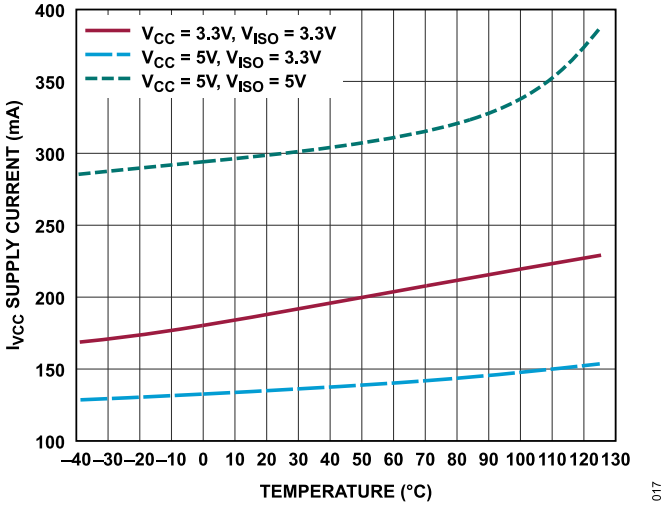

Figure 17. V_{CC} Supply Current vs. Temperature at 20Mbps (ADM2895E-1), 54Ω Termination

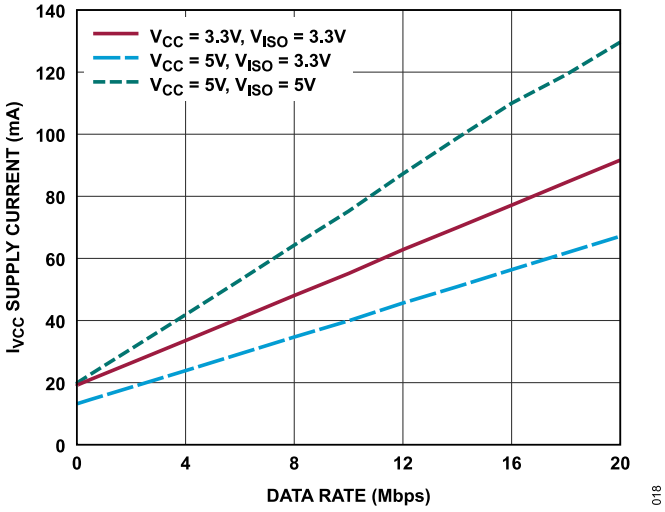

Figure 18. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E-1), Unterminated Bus, Linear Scale

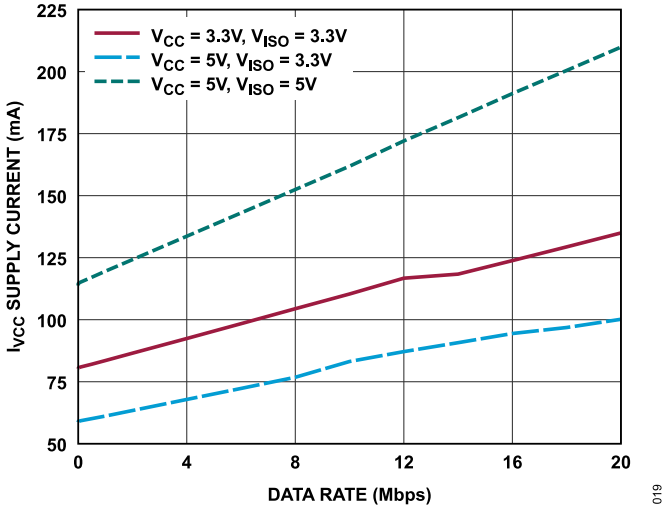

Figure 19. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E-1), 120Ω Termination, Linear Scale

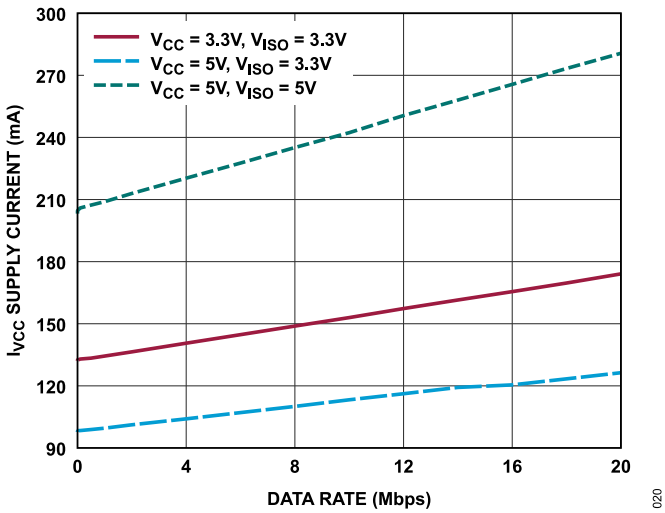

Figure 20. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E-1), 54Ω Termination, Linear Scale

TYPICAL PERFORMANCE CHARACTERISTICS

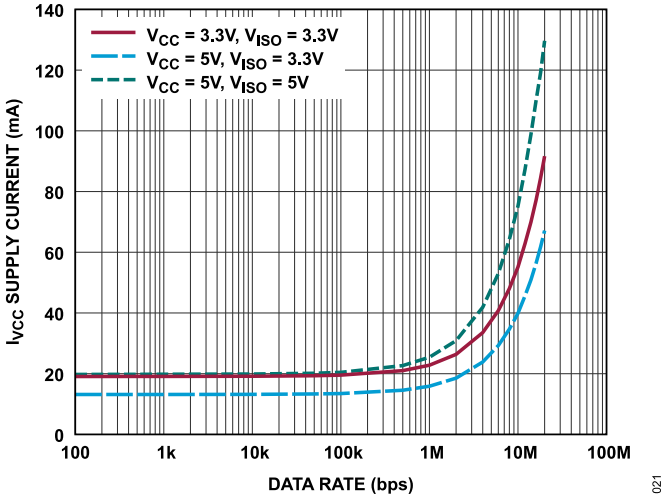

Figure 21. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E-1), Unterminated Bus, Logarithmic Scale

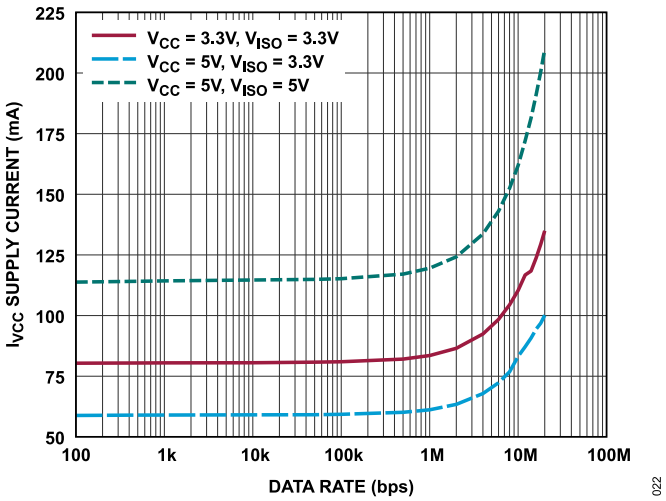

Figure 22. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E-1), 120Ω Termination, Logarithmic Scale

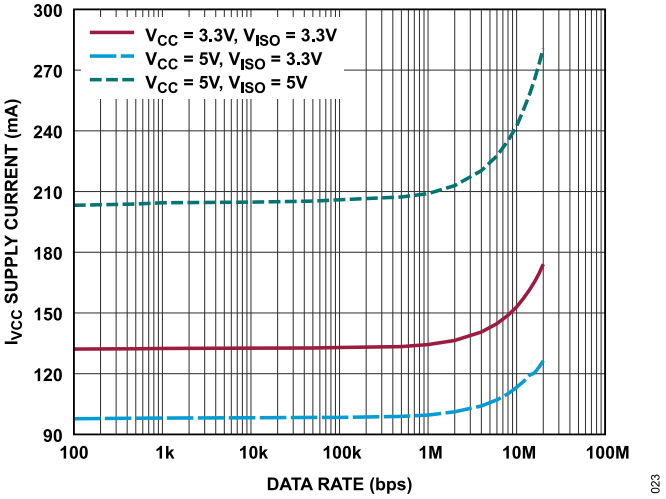

Figure 23. V_{CC} Supply Current vs. Frequency, T_A = 25°C, (ADM2895E-1), 54Ω Termination, Logarithmic Scale

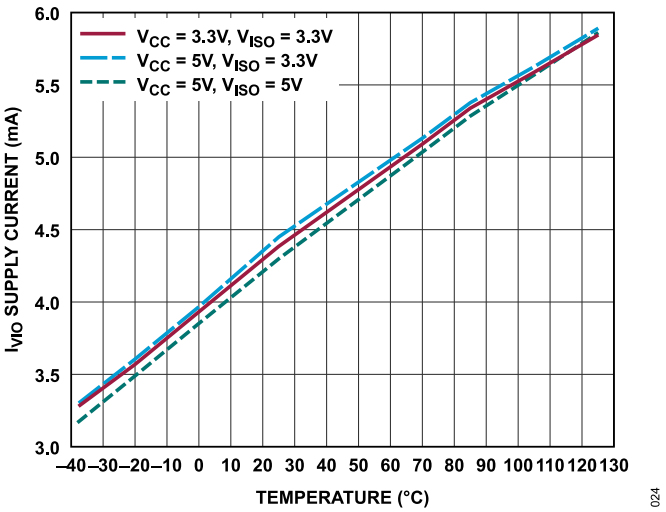

Figure 24. V_{IO} Supply Current vs. Temperature at 250kbps (ADM2895E), Unterminated Bus

TYPICAL PERFORMANCE CHARACTERISTICS

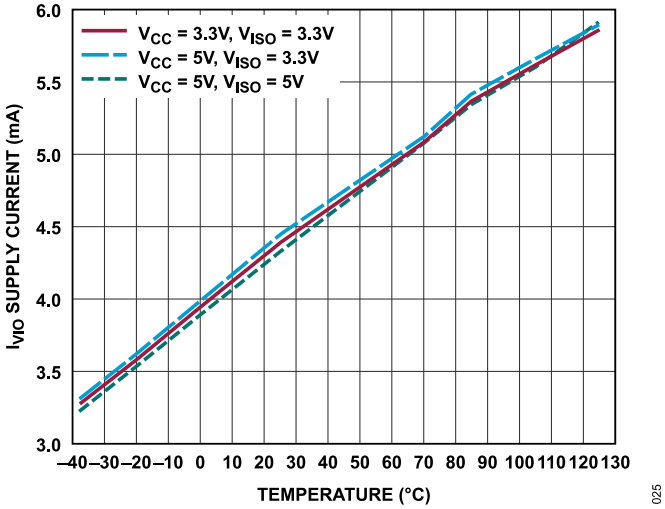

Figure 25. V_{IO} Supply Current vs. Temperature at 250kbps (ADM2895E), 120Ω Termination

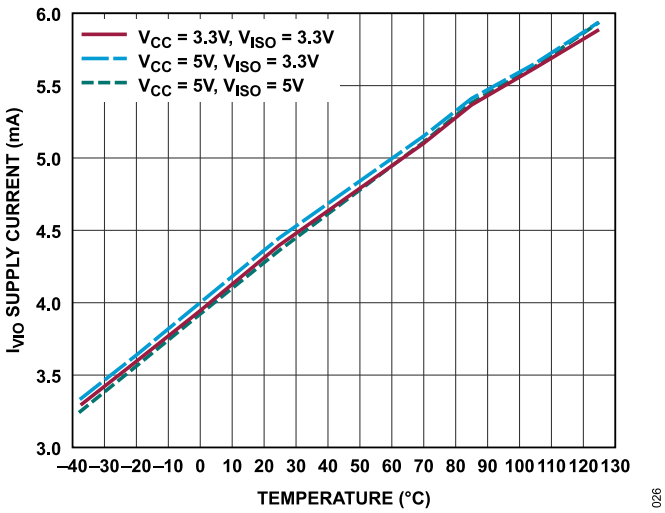

Figure 26. V_{IO} Supply Current vs. Temperature at 250kbps (ADM2895E), 54Ω Termination

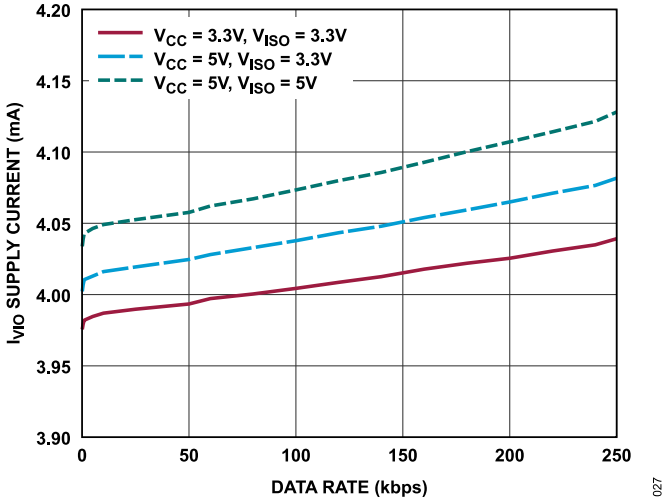

Figure 27. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E), Unterminated Bus

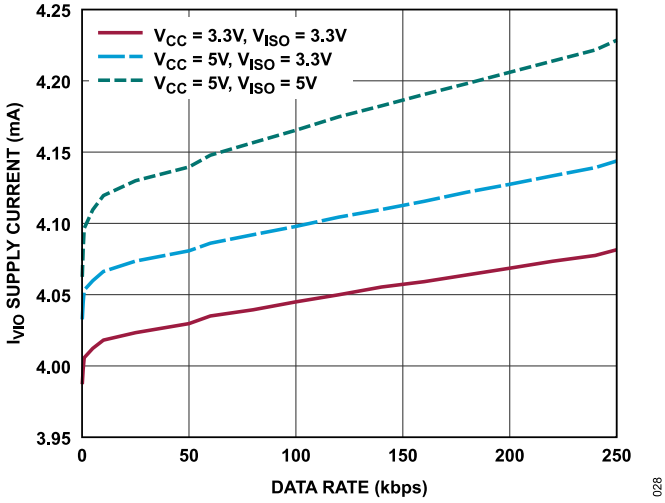

Figure 28. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E), 120Ω Termination

TYPICAL PERFORMANCE CHARACTERISTICS

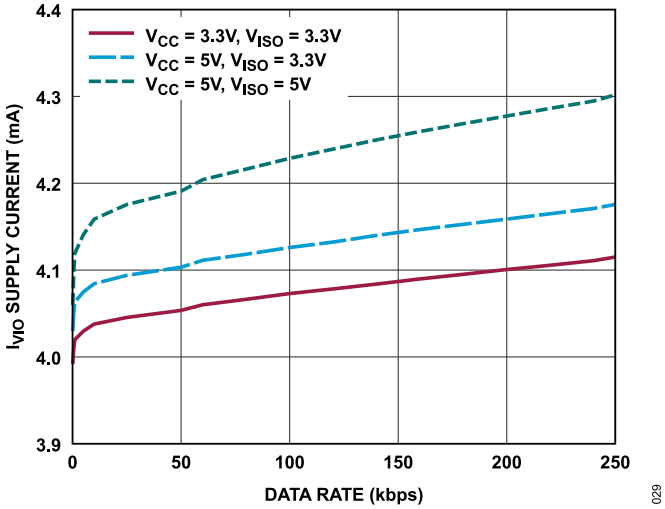

Figure 29. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E), 54 Ω Termination

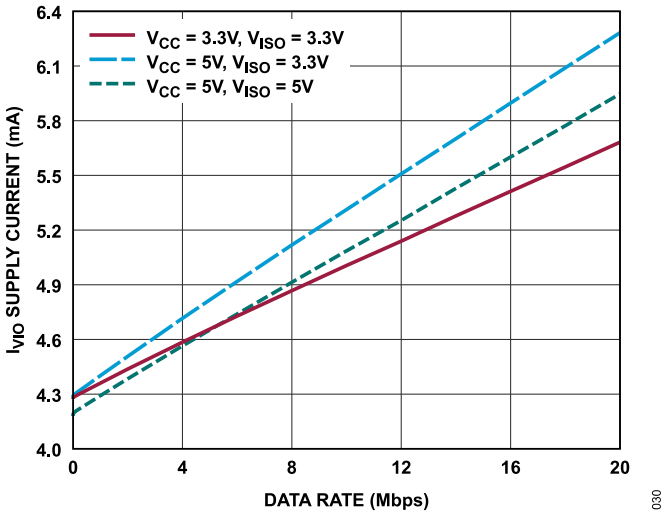

Figure 30. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E-1), Unterminated Bus, Linear Scale

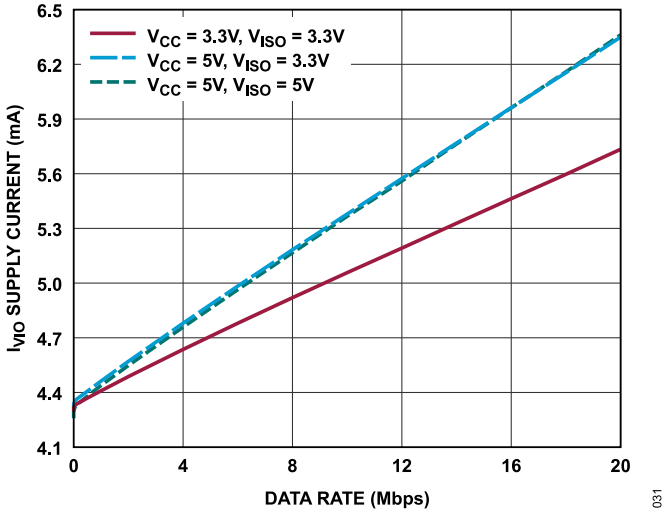

Figure 31. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E-1), 120Ω Termination, Linear Scale

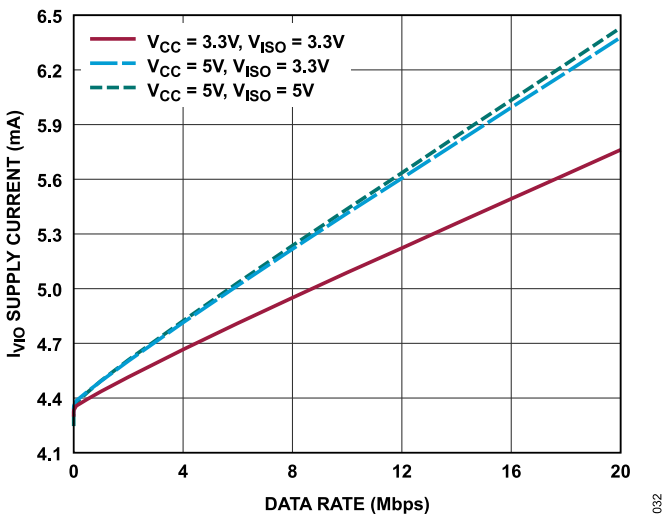

Figure 32. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E-1), 54Ω Termination, Linear Scale

TYPICAL PERFORMANCE CHARACTERISTICS

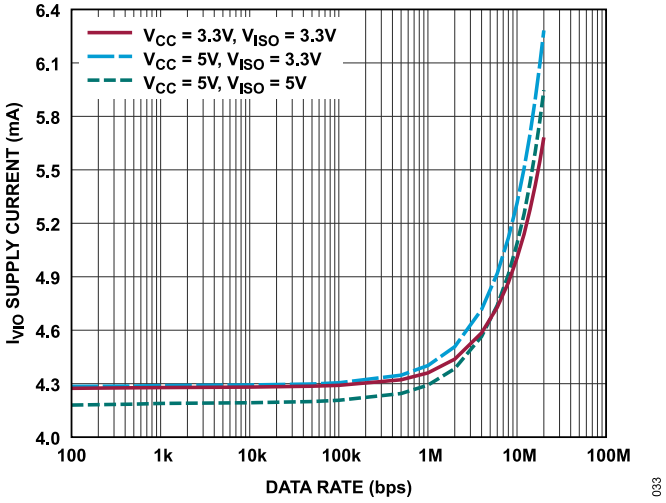

Figure 33. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E-1), Unterminated Bus, Logarithmic Scale

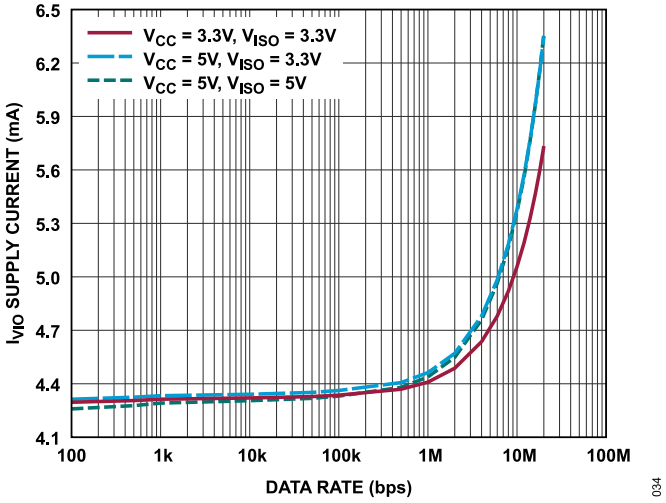

Figure 34. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E-1), 120Ω Termination, Logarithmic Scale

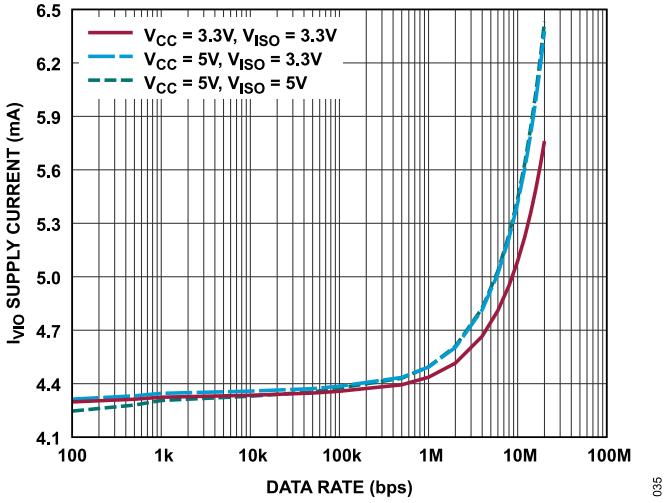

Figure 35. V_{IO} Supply Current vs. Data Rate, T_A = 25°C, (ADM2895E-1), 54Ω termination, Logarithmic Scale

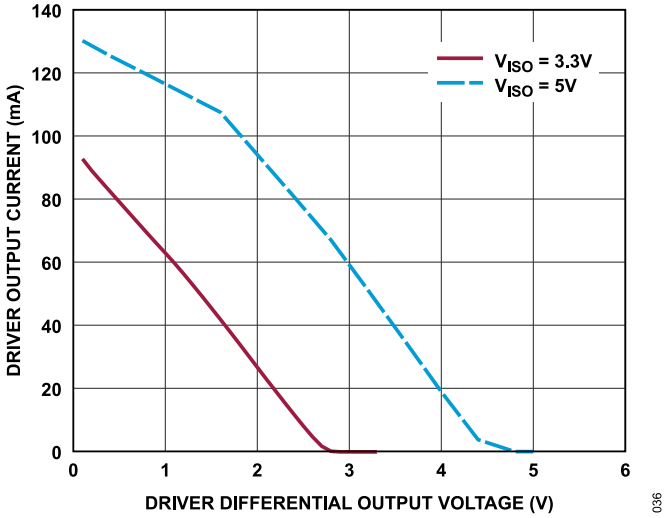

Figure 36. Driver Output Current vs. Driver Differential Output Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

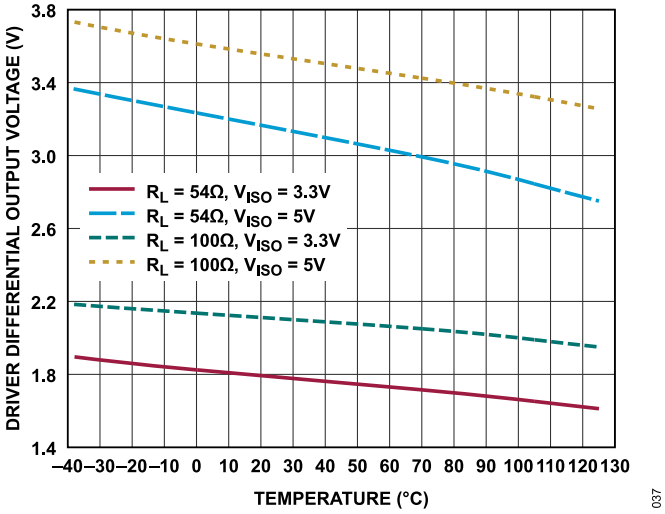

Figure 37. Driver Differential Output Voltage vs. Temperature

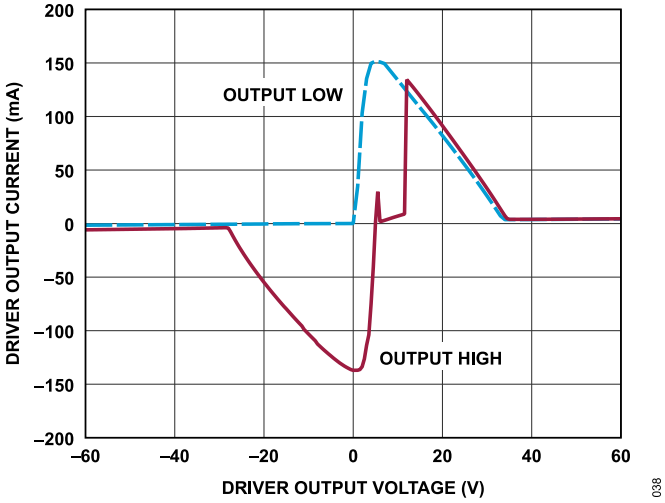

Figure 38. Driver Output Current vs. Driver Output Voltage

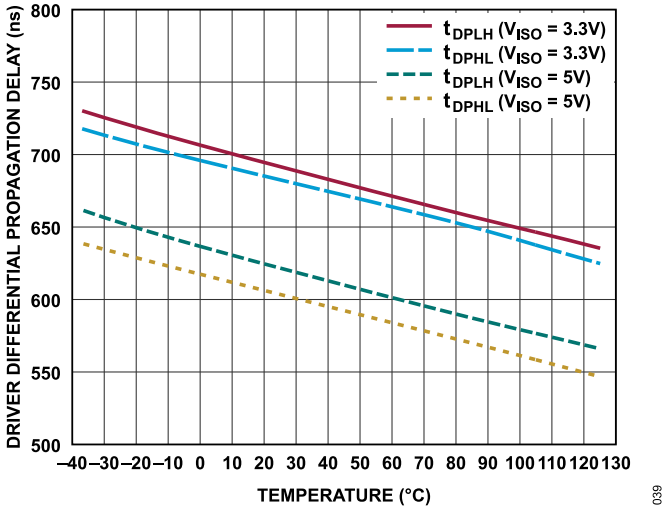

Figure 39. Driver Differential Propagation Delay vs. Temperature, 54Ω Termination (ADM2895E)

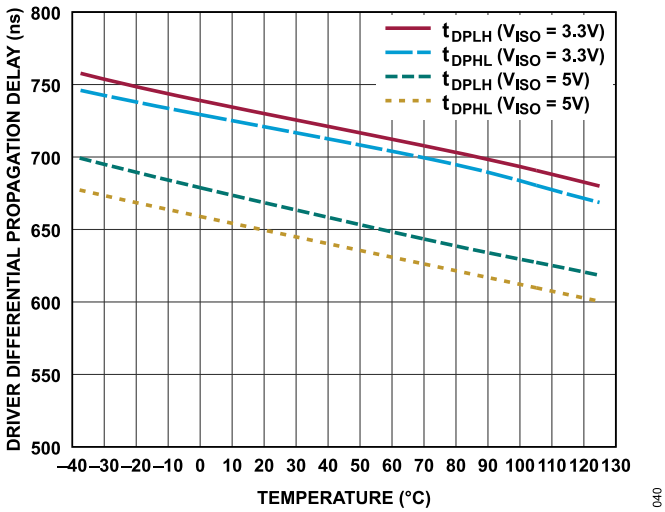

Figure 40. Driver Differential Propagation Delay vs. Temperature, 100Ω Termination (ADM2895E)

TYPICAL PERFORMANCE CHARACTERISTICS

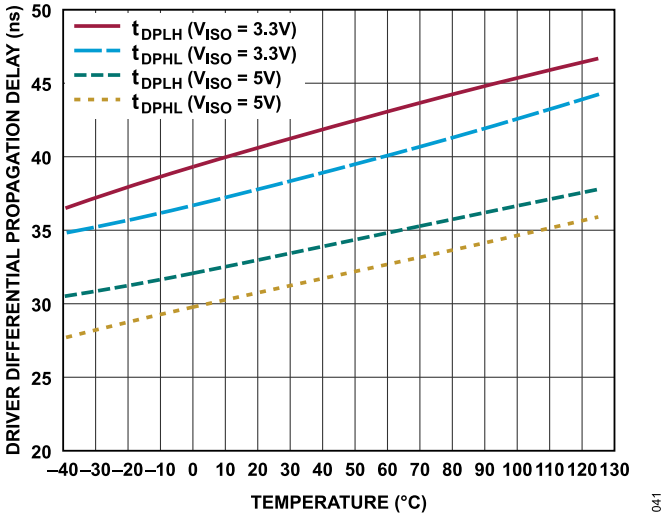

Figure 41. Driver Differential Propagation Delay vs. Temperature, 54Ω Termination (ADM2895E-1)

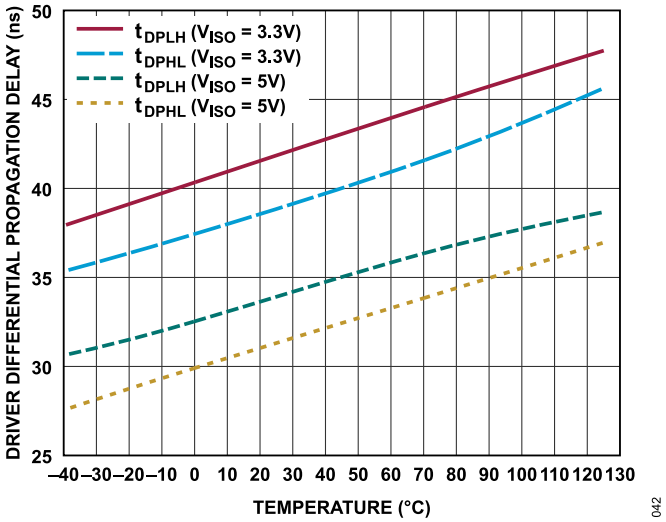

Figure 42. Driver Differential Propagation Delay vs. Temperature, 100Ω Termination (ADM2895E-1)

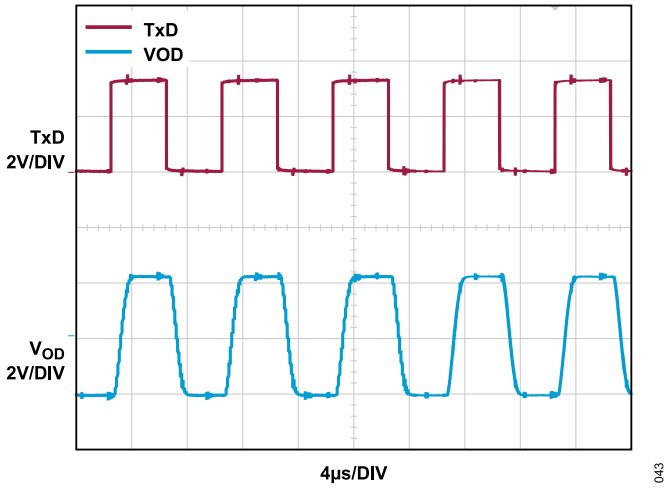

Figure 43. Driver Switching at 250kbps, (ADM2895E)

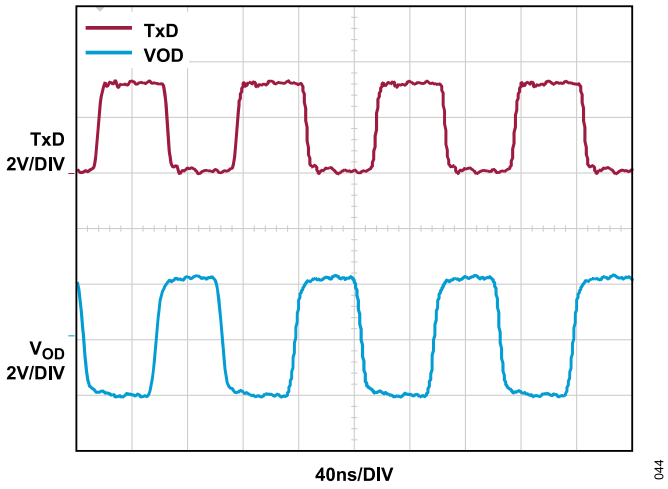

Figure 44. Driver Switching at 20Mbps, (ADM2895E-1)

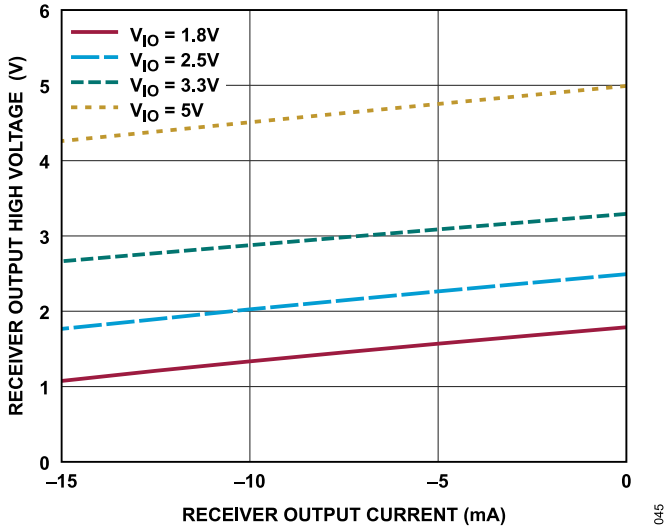

Figure 45. Receiver Output High Voltage vs. Receiver Output Current

TYPICAL PERFORMANCE CHARACTERISTICS

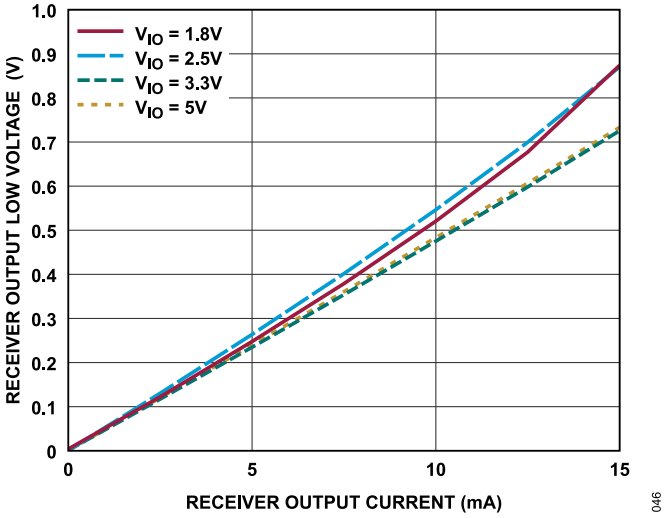

Figure 46. Receiver Output Low Voltage vs. Receiver Output Current

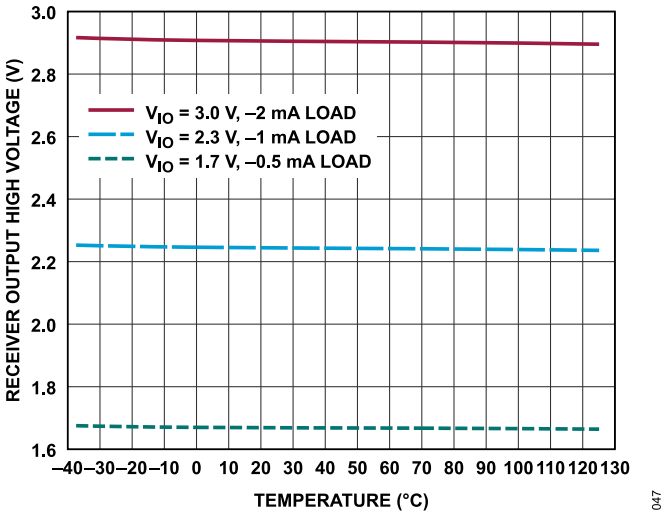

Figure 47. Receiver Output High Voltage vs. Temperature

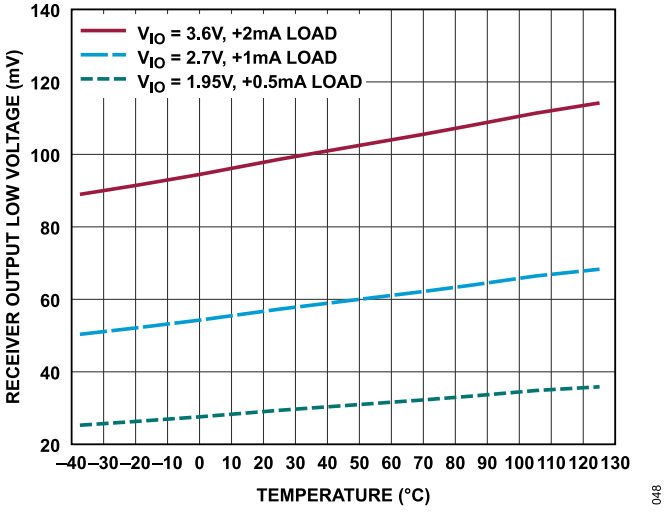

Figure 48. Receiver Output Low Voltage vs. Temperature

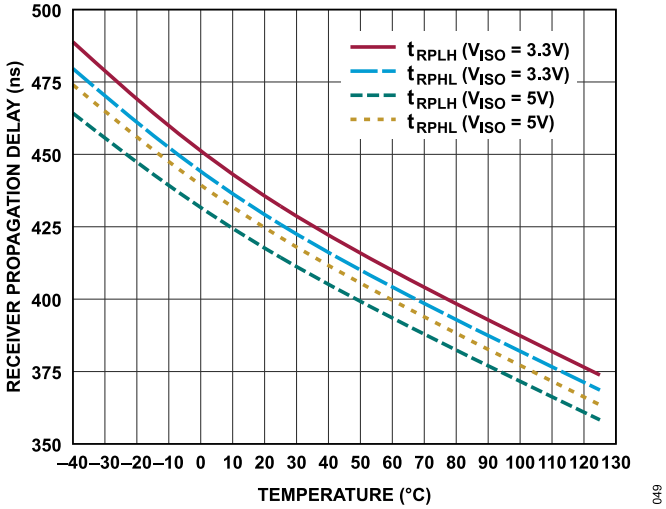

Figure 49. Receiver Propagation Delay vs. Temperature

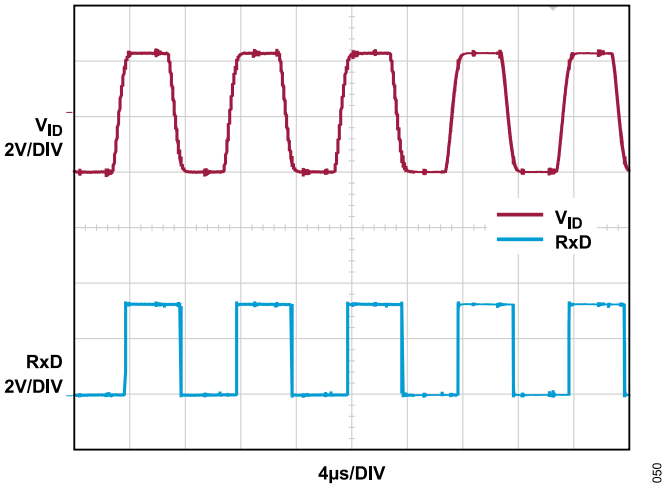

Figure 50. Receiver Switching at 250kbps, (ADM2895E)

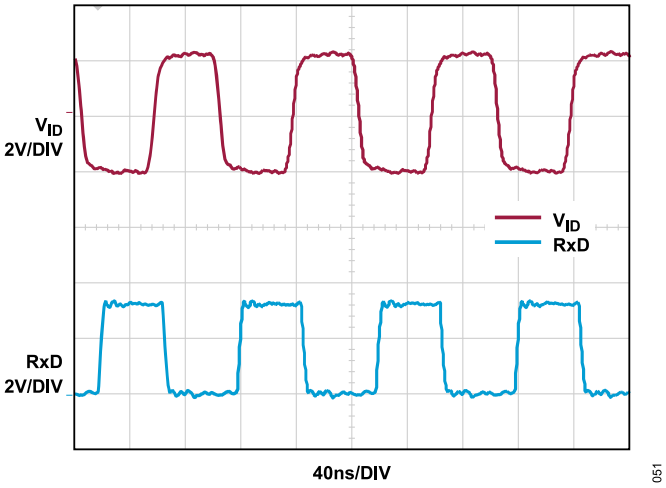

Figure 51. Receiver Switching at 20Mbps, (ADM2895E-1)

TEST CIRCUITS

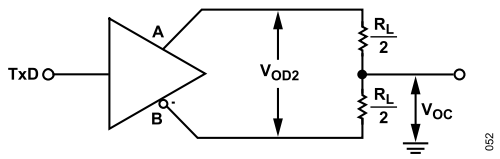

Figure 52. Driver Voltage Measurement, $|V_{OD2}|$

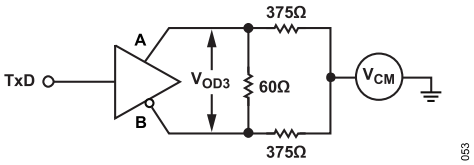

Figure 53. Driver Voltage Measurement over Common-Mode Range, $|V_{OD3}|$

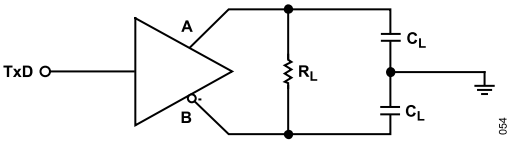

Figure 54. Driver Propagation Delay Measurement

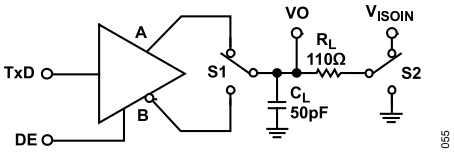

Figure 55. Driver Enable or Disable Time Measurement

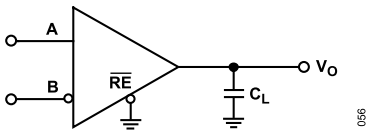

Figure 56. Receiver Propagation Delay Time Measurement

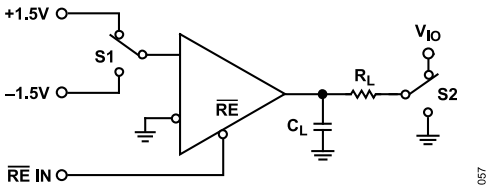

Figure 57. Receiver Enable or Disable Time Measurement

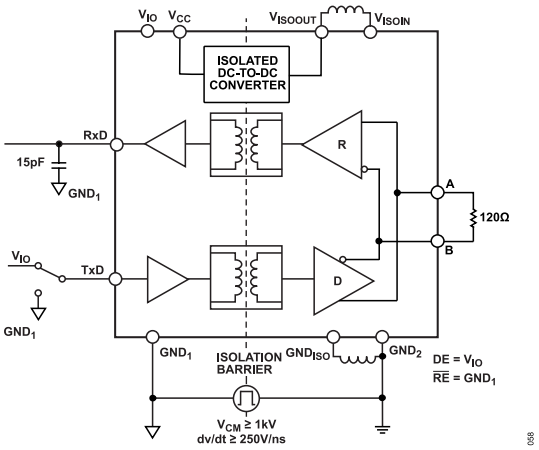

Figure 58. CMTI Test Diagram

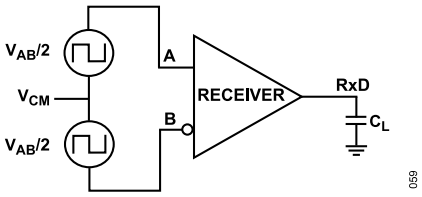

Figure 59. Fail-Safe Delay Measurement

THEORY OF OPERATION

LOW EMI INTEGRATED DC-TO-DC CONVERTER

The ADM2895E/ADM2895E-1 include a flexible integrated DC-to-DC converter optimized for low radiated emissions (EMI). The isolated DC-to-DC converter is constructed with a set of chip scale coplanar coils separated by an insulating material. By exciting the upper coil with an AC signal, power is magnetically coupled across the isolation barrier where it is rectified and regulated. Because no direct electrical connection exists between the top and bottom coils, the primary and secondary sides of the device remain galvanically isolated.

This isolated DC-to-DC converter features a regulated output of either 3.3V or 5V, selectable by the V_{SEL} logic pin, which allows the user to optimize the supply rail of the RS-485 transceiver. For lower power applications, choose a 3.3V supply. For the applications that require a large differential output voltage, such as PROFIBUS, operate the isolated DC-to-DC converter with a 5V output. Table 10 shows the supported supply configurations for the isolated DC-to-DC converter.

Table 10. Isolated DC-to-DC Converter Supply Configuration

V_{SEL} Pin	V_{ISO} Output Supply Voltage	Supported V_{CC} Supply Range
Connected to GND_{ISO}	3.3V	3V to 5.5V
Connected to V_{ISOOUT}	5V	4.5V to 5.5V

The integrated DC-to-DC converter is optimized to minimize radiated EMI. This allows designers to meet the CISPR32 and EN 55032 Class B requirements on a 2-layer PCB with the addition of two low cost, surface-mount device (SMD) ferrites. Follow layout recommendations during PCB design to minimize these emissions. For more details, see the PCB Layout and Electromagnetic Interference (EMI) section.

ROBUST LOW-POWER DIGITAL ISOLATOR

The ADM2895E/ADM2895E-1 feature a low-power digital isolator to galvanically isolate the primary and secondary side of the device. The use of coplanar transformer coils with an on-off keying (OOK) modulation scheme allows high data throughput across the isolation barrier while minimizing radiation emissions. This architecture provides a robust digital isolator with immunity to common-mode transients of greater than 250V/ns across the full temperature and supply range of the device. Figure 60 shows a repeated common-mode transients of 280V/ns being applied at different times relative to the TxD input transitioning from low to high while monitoring the resulting RxD output. The very small variation in the propagation delay and no errors demonstrates the part's robust CMTI performance.

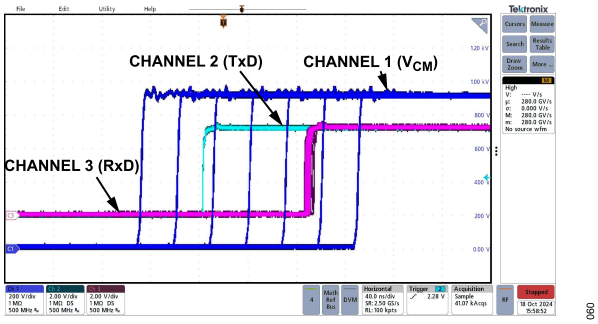

Figure 60. Switching Correctly in the Presence of >250V/ns Common-Mode Transients

Robust ±60V Fault Protection

The ADM2895E/ADM2895E-1 feature an improved overvoltage fault-tolerant RS-485/RS-422 transceiver, which may eliminate field failures due to overvoltage faults without using costly external protection devices. The ±60V fault tolerance on the A and B bus pins provides transceiver protection against field miswiring or cable faults to the common industrial 24V or 48V power supplies, which may be present in the cable.

The ±60V fault protection of the ADM2895E/ADM2895E-1 is achieved by using a high-voltage BiCMOS integrated circuit technology. The naturally high breakdown voltage of this technology provides protection in powered-off and high-impedance conditions. The driver outputs use a progressive foldback current limit design to protect against over voltage faults while still allowing high current output drive.

The high voltage rating of the ADM2895E/ADM2895E-1 makes it simple to extend the overvoltage protection to higher levels using external protection components. Compared to lower voltage RS-485 transceivers, the ADM2895E/ADM2895E-1 allows the use of external protection devices with higher breakdown voltages, so as not to interfere with data transmission in the presence of large common-mode voltages.

HIGH-DRIVER DIFFERENTIAL OUTPUT VOLTAGE

The ADM2895E/ADM2895E-1 feature a proprietary transmitter architecture with a low-driver output impedance, which results in an increased driver differential output voltage. This architecture is particularly useful when operating the device over long cable runs, where the DC resistance of the transmission line dominates signal attenuation. In these applications, the increased differential voltage improves noise margin and allows transmission over longer cable lengths. In addition, when operated as a 5V transceiver (V_{SEL} = V_{ISOOUT}), the ADM2895E/ADM2895E-1 meet or exceed the PROFIBUS requirement of a minimum 2.1V differential output voltage.

THEORY OF OPERATION

IEC 61000-4-2 ESD PROTECTION

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. ESD has the characteristics of high current in a short time period. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 describes testing using two coupling methods: contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT. A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the EUT. Air discharge testing is a more accurate representation of an actual ESD event than contact discharge but is not as repeatable. Therefore, contact discharge is the preferred test method. During testing, the data port is subjected to at least 10 positive and 10 negative single discharges. Selection of the test voltage is dependent on the system end environment. Figure 61 shows the 8kV contact discharge current waveform as described in the IEC 61000-4-2 specification. Some of the key waveform parameters are rise times of less than 1ns and pulse widths of approximately 60ns.

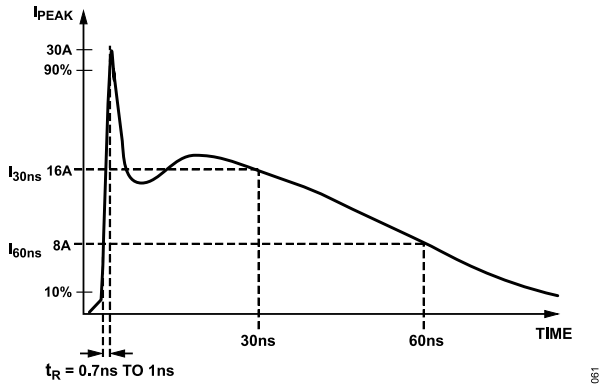

Figure 61. IEC 61000-4-2 ESD Waveform (8kV)

Figure 62 shows the 8kV contact discharge current waveform from the IEC 61000-4-2 standard compared to the HBM ESD 8kV waveform. Figure 62 shows that the two standards specify a different waveform shape and peak current (I_{PEAK}). The peak current associated with an IEC 61000-4-2 8kV pulse is 30A, whereas the corresponding peak current for HBM ESD is more than five times less, at 5.33A. The other difference is the rise time of the initial voltage spike, with the IEC 61000-4-2 ESD waveform having a much faster rise time of 1ns, compared to the 10ns associated with the HBM ESD waveform. The amount of power associated with an IEC ESD waveform is much greater than that of an HBM ESD waveform. The HBM ESD standard requires the EUT to be subjected to three positive and three negative discharges, whereas in comparison, the IEC ESD standard requires 10 positive and 10 negative discharge tests.

The ADM2895E/ADM2895E-1's isolation barrier provides ±8kV contact protection between the bus pins and GND_1. These devices with IEC 61000-4-2 ESD ratings are better suited for operation in harsh environments when compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

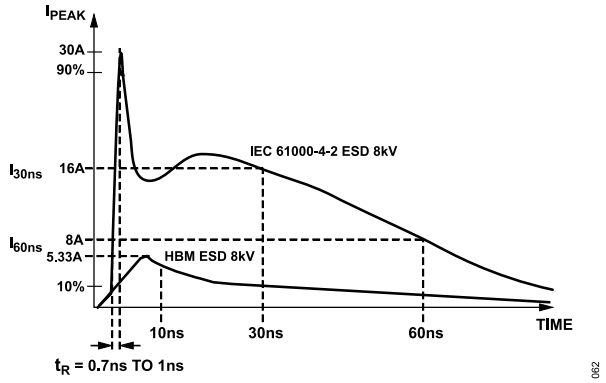

Figure 62. IEC 61000-4-2 ESD 8kV Waveform Compared to HBM ESD 8kV Waveform

TRUTH TABLES

Table 12 and Table 13 use the abbreviations shown in Table 11. V_{IO} supplies the DE, TxD, $\overline{RE}$, and RxD pins only.

Table 11. Truth Table Abbreviations

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Any state
Z	High impedance (off)

Table 12. Transmitting Truth Table

Supply Status		Inputs		Outputs	
V_{CC}	V_{IO}	DE	TxD	A	B
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	X	X	Z	Z
Off	X	X	X	Z	Z

THEORY OF OPERATION

Table 13. Receiving Truth Table

Supply Status		Inputs		Output
V_{CC}	V_{IO}	A − B	$\overline{RE}$	RxD
On	On	≥+0.2V	L	H
On	On	≤−0.2V	L	L
On	On	−0.2V < (A – B) < +0.2V	L	I
On	On	Inputs open/shorted	L	H
X	On	X	H	Z
X	Off	X	X	I
Off	On	X	L	I

RECEIVER FAIL-SAFE

When the absolute value of the differential voltage between the A and B pins is greater than 200mV with the receiver enabled, the state of RO reflects the polarity of (A − B).

These parts have a fail-safe feature that guarantees the receiver output is in a logic 1 state (the idle state) when the inputs are shorted, left open, or terminated but not driven. The delay allows normal data signals to transition through the threshold region without being interpreted as a fail-safe condition. This fail-safe feature is guaranteed to work for inputs spanning the entire common-mode range of –25V to 25V.

Most competing devices achieve the fail-safe function by a simple negative offset of the input threshold voltage. This causes the receiver to interpret a zero differential voltage as a logic 1 state. The disadvantage of this approach is the input offset can introduce duty cycle asymmetry at the receiver output that becomes increasingly worse with low-input signal levels and slow-input edge rates.

Other competing devices use internal biasing resistors to create a positive bias at the receiver inputs in the absence of an external signal. This type of fail-safe biasing is ineffective if the network lines are shorted, or if the network is terminated but not driven by an active transmitter.

The ADM2895E/ADM2895E-1 use a fully symmetric positive and negative receiver thresholds V_{TH-} and V_{TH+} (typically ±125 mV) to maintain good duty-cycle symmetry at low signal levels. The fail-safe operation is performed with a window comparator to determine when the differential input voltage falls above the V_{TFS} fail-safe threshold (typically –75 mV) but below the V_{TH+} threshold. If this condition persists for more than about 40ns for the ADM2895E-1 or 1.2µs for the ADM2895E, the fail-safe condition is asserted and the RxD pin is forced to the logic 1 state. This circuit provides full fail-safe operation and a large dynamic signal hysteresis of ~250mV between V_{TH-} and V_{TH+} with no negative impact to receiver duty-cycle symmetry, as shown in Figure 63. The input signal in Figure 63 is obtained by driving a 10Mbps RS-485 signal through 1000feet of cable, thereby attenuating it to a ±200mV signal with slow rise and fall times. Good duty-cycle symmetry is observed at RxD despite the degraded input signal.

The fail-safe circuit has been enhanced with noise filtering to exit the fail-safe state. In the absence of noise filtering, a noise transient that momentarily forces the A − B differential voltage below the V_{TH-} receiver threshold causes the RxD output to go low, which may be interpreted as a false start character by the microcontroller. The ADM2895E/ADM2895E-1 receiver reduce these false signals by low pass filtering the signal to exit the fail-safe state. The noise filtering in the fail-safe circuit of the ADM2895E is much greater than in the ADM2895E-1, commensurate with its lower data rate. For example, the ADM2895E-1 exits the fail-safe state when a –1V differential pulse of about 3ns duration is applied, while the ADM2895E requires a –1V pulse of about 400ns duration to exit the fail-safe state. The minimum pulse widths to enter or exit the fail-safe state are not tested in production, but the underlying filtering is reflected in the t_{PFSN} and t_{PFSX} measurements.

These features are fully compatible with external fail-safe biasing configurations, which can be used in applications with legacy devices that lack fail-safe support, or in applications where additional noise margin is required. For more details on external fail-safe biasing, refer to the AN-960: *RS-485/RS-422 Circuit Implementation Guide*.

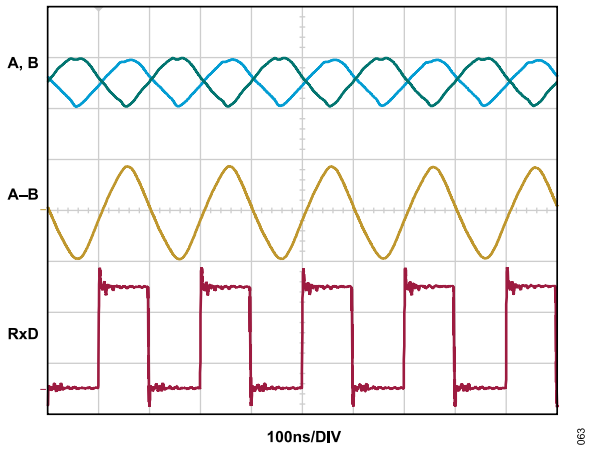

Figure 63. Duty-Cycle of Balanced Receiver with ±200mV, 10Mbps Input Signal

THEORY OF OPERATION

ENHANCED RECEIVER IMMUNITY

An additional benefit of the fully symmetric receiver thresholds is enhanced receiver noise immunity. The differential input signal must go above the positive threshold to register as a logic 1 and go below the negative threshold to register as a logic 0. This provides a hysteresis of 250mV (typical) at the receiver inputs for any valid data signal. An invalid data condition such as a DC sweep of the receiver inputs produces a different observed hysteresis due to the activation of the fail-safe circuit. Competing devices that employ a negative offset of the input threshold voltage generally have a much smaller hysteresis and subsequently have lower receiver noise immunity.

The ADM2895E provides additional noise immunity by adding low-pass filtering to the differential signal in its receiver. Commensurate with its maximum data rate of 250kbps, the ADM2895E receiver attenuates high frequency signals above approximately 660kHz. This low-pass filter removes high-frequency noise transients that might otherwise be interpreted as data. High-frequency noise filtering is not tested in production, but the underlying filtering is reflected in the t_{RPLH} and t_{RPHL} measurements.

HOT-SWAP INPUTS

When a circuit board is inserted in a powered (or hot) backplane, parasitic coupling from supply and ground rails to digital inputs may occur. The ADM2895E/ADM2895E-1 contain circuitry to ensure that the A and B outputs remain in a high impedance state during power-up, and then default to the correct states. For example, when V_{IO} and V_{CC} power up at the same time and the $\overline{RE}$ pin is pulled low, with the DE and TxD pins pulled high, the A and B outputs remain in high impedance until settling at an expected default high state for the A pin and expected default low state for the B pin.

224 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12kΩ (1 unit load), and the standard driver can drive up to 32 unit loads. The ADM2895E/ADM2895E-1 transceiver have less than 1/7 unit load receiver input resistance, which allows over 224 transceivers to be connected in parallel on one communication line. Any combination of these devices and other RS-485 transceivers with a total of 32 unit loads or fewer can be connected to the line.

DRIVER OUTPUT PROTECTION

The ADM2895E/ADM2895E-1 feature two methods to prevent excessive output current and power dissipation caused by faults or by bus contention. Current-limit protection on the output stage provides immediate protection against short-circuits over the entire common-mode voltage range. In addition, a thermal shutdown circuit forces the driver outputs to a high impedance state if the die temperature rises excessively. This circuitry is designed to disable the driver outputs when a die temperature greater than 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

1.7V TO 5.5V V_{IO} LOGIC SUPPLY

The ADM2895E/ADM2895E-1 feature a V_{IO} logic supply pin to allow a flexible digital interface operational to voltages as low as 1.7V. The V_{IO} pin powers the primary side of the signal isolation, the logic inputs, and the RxD output. These input and output pins interface with logic devices such as universal asynchronous receiver/transmitters (UARTs), application specific integrated circuits (ASICs), and microcontrollers. For applications where these devices use I/Os operating at voltages other than the ADM2895E/ADM2895E-1 V_{CC} supply voltage, power the V_{IO} supply from the same supply rail as the logic device. The V_{IO} supply accepts a supply voltage between 1.7V and 5.5V, which allows the communication with 1.8V, 2.5V, 3.3V, and 5V devices.

APPLICATIONS INFORMATION

PCB LAYOUT AND ELECTROMAGNETIC INTERFERENCE (EMI)

The ADM2895E/ADM2895E-1 can be used in designs, which meet the EN 55032 Class B/CISPR32 radiated emissions requirements. Two external surface-mount technology (SMT) ferrite beads and a 2.2pF capacitor are used to pass the Class B limits with margin. No special mitigation techniques, such as stitching capacitance, are needed, which allows system designers to create a compliant design on a 2-layer PCB, without the need for complex and area intensive layouts.

The ADM2895E/ADM2895E-1 feature an internal split paddle lead frame on the bus side. For optimal noise suppression, filter the V_{ISOOUT} signal (Pin 25) and GND_{ISO} signal (Pin 24, Pin 26, and Pin 28) for high frequency currents before routing power to the RS-485 transceiver and other circuitry. Two SMT ferrite beads, L1 and L2, are recommended to achieve this filtering. The size of the V_{ISOOUT} and GND_{ISO} net must also be kept to a minimum. For the recommended PCB layout, see Figure 64.

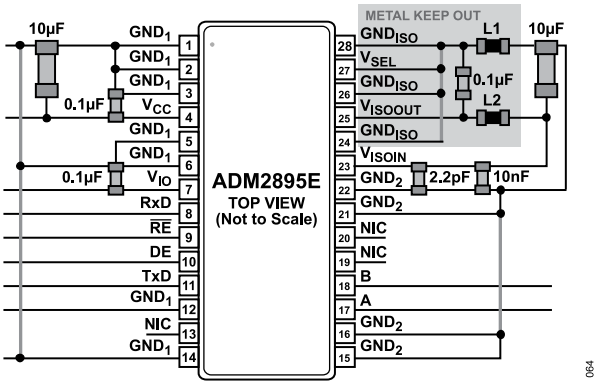

Figure 64. Recommended PCB Layout

The *iso*Power® integrated DC-to-DC converter contains switching frequencies between 180MHz and 400MHz. To effectively filter these frequencies, choose the impedance of the ferrite bead to be approximately 2kΩ within the 100MHz and 1GHz frequency range. Some recommended SMT ferrites are shown in Table 14. Although these ferrite beads are required to achieve compliance to EN 55032 Class B, they are not needed for system functionality. The ADM2895E/ADM2895E-1 have been fully characterized with the recommended BLM15HD182SN1 ferrite beads.

Table 14. Examples of Surface-Mount Ferrite Beads

Manufacturer	Device Number
Murata Electronics	BLM15HD182SN1
Taiyo Yuden	BKH1005LM182-T

The digital isolators for the data isolation of the ADM2895E/ADM2895E-1 use a low power, OOK encoding scheme with switching frequencies of approximately 3.8GHz and 4.2GHz. Proper high-frequency decoupling can achieve compliance to EN 55032 Class B by placing a 2.2pF capacitor between the V_{ISOIN} and GND_2 pins. This capacitor must be located <2mm from the pins and must have a self-resonant frequency above 5GHz. Place the 10nF and optional 10µF capacitors next to the 2.2pF capacitor. Operation with data rates at or above 9.6kbps is recommended for increased margin to EN 55032 Class B limits.

The ADM2895E/ADM2895E-1 can dissipate over 500mW of power when fully loaded. Because it is not possible to apply a heat sink to an isolation device, the devices primarily depend on heat dissipation to the PCB through the GND_x pins. If the devices are used at high ambient temperatures, provide a thermal path from the GND_x pins to the PCB ground plane. The use of a solid GND_1 and GND_2 plane is recommended. Implementing a low thermal impedance between the top ground layers and internal ground layers reduce the temperature inside the chip significantly.

DEVICE POWER-UP

The integrated *iso*Power isolated DC-to-DC converter requires 10ms to power up to the set point of 3.3V or 5V. During this start-up time, it is not recommended to assert the DE driver enable signal.

In applications where the isolated DC-to-DC converter is operated with a 3.3V output voltage (V_{SEL} pin connected to GND_{ISO}), the V_{CC} supply rail must be greater than 3.135V during the power-up sequence. After the 10ms power-up duration, the V_{CC} supply rail can operate across the full 3V to 5.5V range.

MAXIMUM DATA RATE VS. AMBIENT TEMPERATURE

Under a large current load or when operating at high frequency operation, self heating effects within the *iso*Power DC-to-DC converter can limit the maximum ambient temperature achievable while retaining a silicon junction temperature below 150°C. This internal power dissipation is related to application conditions such as supply voltage configuration, switching frequency, effective load on the RS-485 bus, and the amount of time the transceiver is in transmit mode. Thermal performance also depends on the PCB design and thermal characteristics of a system.

In applications with a fully loaded RS-485 bus (equivalent to 54Ω bus resistance) operating with V_{ISO} = 5V, it is recommended to keep the V_{CC} input supply greater than 4.75V. If this is not possible for the ADM2895E-1 (high speed), limit either the maximum ambient temperature to 85°C, or the maximum operating data rate to 6Mbps. If this is not possible for the ADM2895E (slow speed), limit the maximum ambient temperature to 85°C.

ISOLATED PROFIBUS SOLUTION

The ADM2895E/ADM2895E-1 feature a driver that is well suited for meeting the requirements of an isolated PROFIBUS node. When operating the ADM2895E/ADM2895E-1 as a PROFIBUS transceiver, connect the V_{SEL} pin to the V_{ISOOUT} pin to operate the transceiver with a 5V isolated supply voltage. The ADM2895E/ADM2895E-1 feature the following characteristics that make it ideally suited for use in PROFIBUS applications:

APPLICATIONS INFORMATION

- 5V isolated transceiver power supply. The 5V V_{ISO} output supply provides the required current for the RS-485 transceiver at up to 12Mbps (ADM2895E-1) and the additional 5mA required for the PROFIBUS termination network.
- The output driver meets or exceeds the PROFIBUS differential output requirements. To ensure the transmitter differential output does not exceed 7V p-p over all conditions, place 8.2Ω resistors in series with the A and B transmitter outputs.
- High speed timing to operate at 12Mbps with low propagation delay and less than 10% transmitter and receiver skew (ADM2895E-1).

THERMAL ANALYSIS

The ADM2895E/ADM2895E-1 consist of three internal dies attached to a split lead frame with two die attach pads. For the purposes of thermal analysis, the dies are treated as a single thermal unit, with the highest junction temperature reflected in the thermal parameter values from Table 6. The thermal parameter values are based on thermal simulations with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADM2895E/ADM2895E-1 can operate at full load across the full temperature range without derating the output current.

θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA} and θ_{JB} can be used for first order approximation of the junction temperature in the system environment.

If an accurate thermal measurement of the board temperature near the device under test or directly on the package top surface operating in the system environment is available along with the corresponding device power dissipation, then using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the junction temperature in the system environment. Use Ψ_{JB} when the temperature measurement point is on the board or Ψ_{JT} when it is on the package top. The junction temperature is estimated using the following equation:

$$T_J = \psi_{Jx} \times P_d + T_x \quad (1)$$

where:

P_d is the dissipated power.

T_x is the measured temperature at location x and x is either B for the PCB or T for the package top.

The temperature measurement point for θ_{JB} and Ψ_{JB} is between Pin 7 and Pin 8 on the outer edge of the pin footprint. The temperature measurement point for Ψ_{JT} is at the center of the package top side.

ESD, EFT, AND SURGE

In applications where additional levels of protection against IEC 61000-4-2 ESD, IEC 61000-4-4 EFT, or IEC 61000-4-5 surge events are required, add the external protection circuits to further enhance the EMC robustness of these devices. For a recommended protection circuit, which uses a combination of 24V transient voltage suppressor (TVS) diodes and 10Ω pulse proof resistors to achieve in excess of Level 4 IEC 61000-4-2 ESD and IEC 61000-4-4 EFT protection, and Level 2 IEC 61000-4-5 surge protection while still utilizing the wide common-mode voltage range of the ADM2895E/ADM2895E-1, see Figure 65. Table 15 and Table 16 show the recommended components for protection and the protection levels.

Table 15. Recommended Components for ESD, EFT, and Surge Protection

Recommended Components	Part Number
TVS	CDSOT23-T24C
10Ω Pulse Proof Resistors	CRCW060310R0FKEAHP

Table 16. Protection Levels with Recommended Circuit

EMC Standard	Protection Level (kV)
ESD−Contact (IEC 61000-4-2)	≥±30 (exceeds Level 4)
ESD−Air (IEC 61000-4-2)	≥±30 (exceeds Level 4)
EFT (IEC 61000-4-4)	≥±4 (exceeds Level 4)
Surge (IEC 61000-4-5)	≥±1 (Level 2)

APPLICATIONS INFORMATION

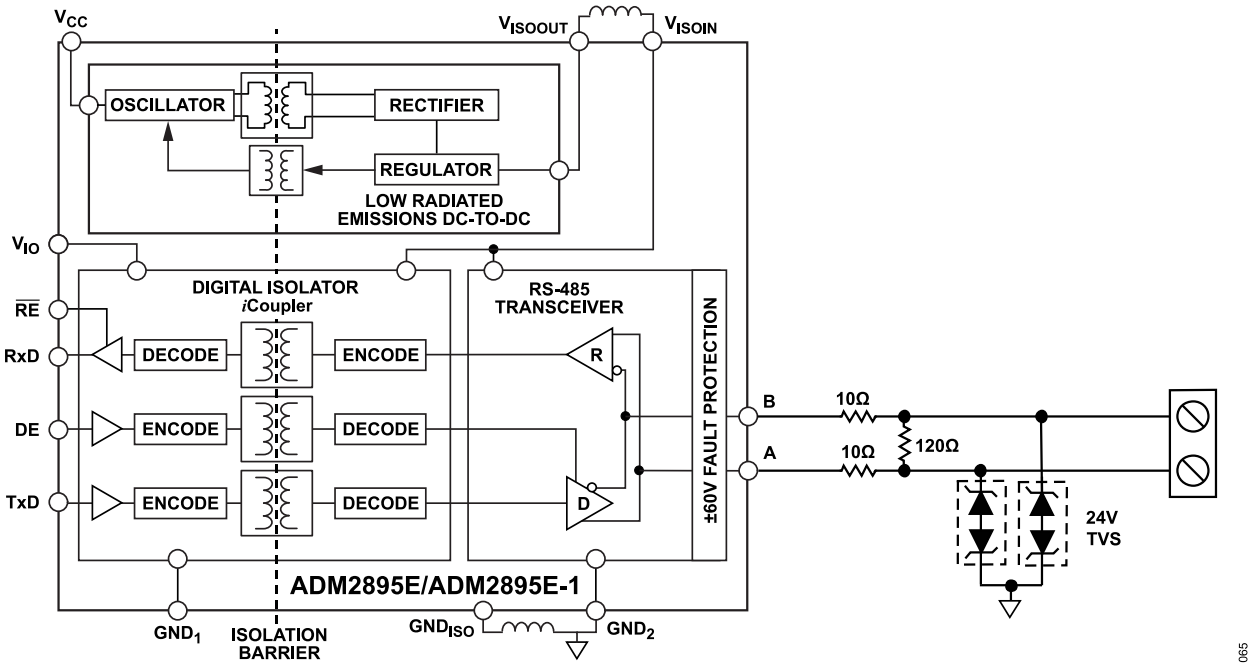

Figure 65. Isolated RS-485 Solution with ESD, EFT, and Surge Protection

TYPICAL APPLICATIONS

An example circuit using the ADM2895E/ADM2895E-1 as a half-duplex RS-485 node is shown in Figure 66. Placement of the termination resistor, R_T, is dependent on the location of the node and the network topology. For guidance on termination, refer to the AN-960: *RS-485/RS-422 Circuit Implementation Guide*. Up to 224 transceivers can be connected to the bus. To minimize reflections, terminate the line at the receiving end in its characteristic impedance and keep stub lengths off the main line as short as possible. For half-duplex operation, this means that both ends of the line must be terminated because either end can be the receiving end.

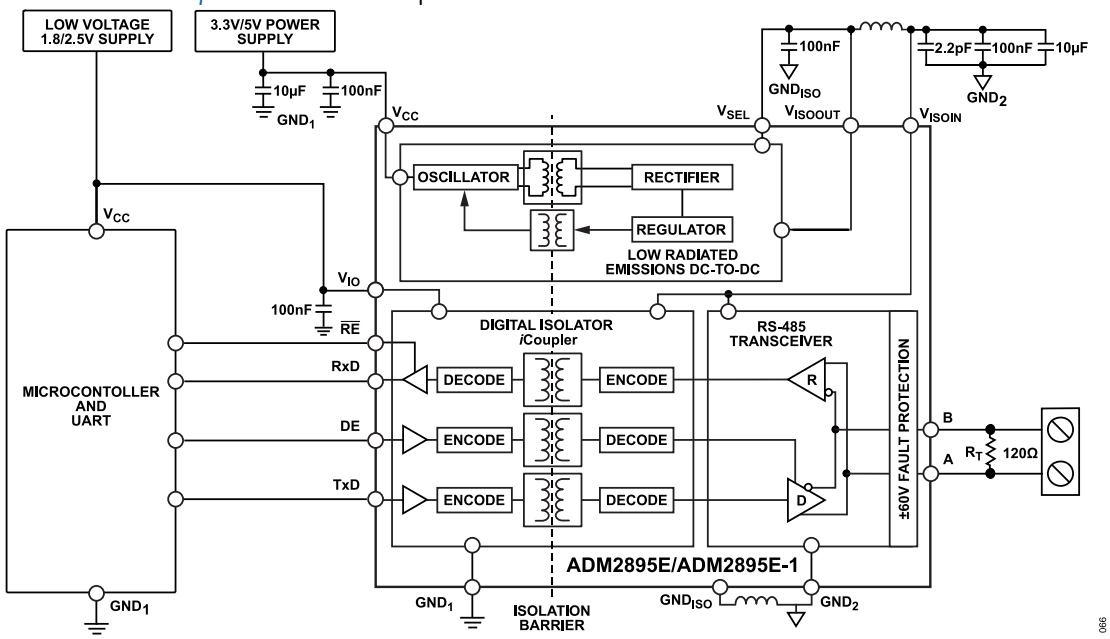

Figure 66. Example Circuit Diagram Using the ADM2895E/ADM2895E-1

OUTLINE DIMENSIONS

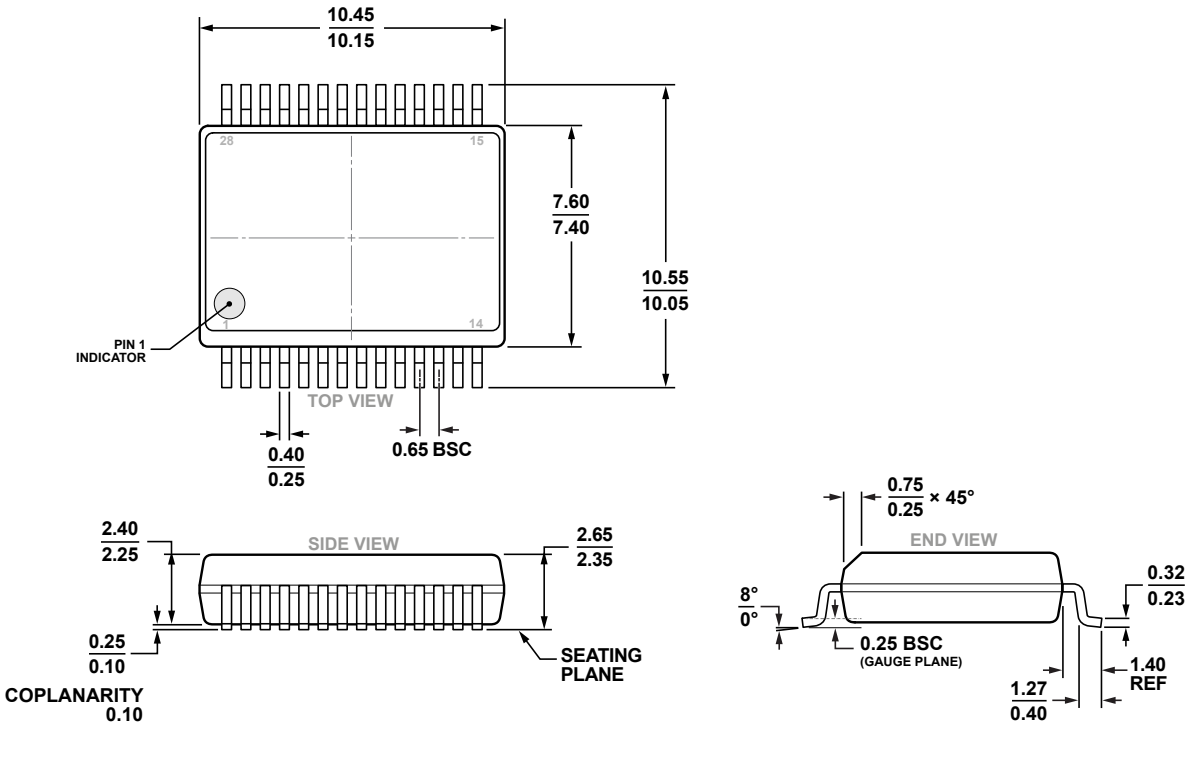

Figure 67. 28-Lead Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP]
(RN-28-1)
Dimensions Shown in millimeters

Updated: November 29, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADM2895EBRNZ-RL7	−40°C to +105°C	28-Lead Standard Small-Outline Package [SOIC_W_FP]	Reel, 400	RN-28-1
ADM2895EBRNZ	−40°C to +105°C	28-Lead Standard Small-Outline Package [SOIC_W_FP]	Tube, 46	RN-28-1
ADM2895E-1BRNZ-RL7	−40°C to +105°C	28-Lead Standard Small-Outline Package [SOIC_W_FP]	Reel, 400	RN-28-1
ADM2895E-1BRNZ	−40°C to +105°C	28-Lead Standard Small-Outline Package [SOIC_W_FP]	Tube, 46	RN-28-1

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADM2895EEBZ	Evaluation Board

[1] Z = RoHS-Compliant Part.