Low Phase Noise Amplifier, 10 MHz to 6 GHz

FEATURES

- Wideband operation: 10 MHz to 6 GHz
- Low residual phase noise
- Single positive supply: 5 V and I_{CQ} of 125 mA
- RBIAS collector current adjustment pin
- Extended operating temperature range: −55°C to +125°C
- RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Telecommunication
- Test and measurement equipment
- Radars
- Local oscillator drivers

GENERAL DESCRIPTION

The ADL8154 is a small form factor, low phase noise amplifier designed for instrumentation, radar, and telecommunications applications. The phase noise from 2 GHz to 5 GHz is −172 dBc/Hz at 1 dB compression (P1dB) and 10 kHz offset.

The ADL8154 operates from a single positive supply (V_{CC}); its bias current (I_{CQ}) is set by a resistor connected between the RBIAS pin and the VCC1 and VCC2 pins. The RF input and RF output are DC-coupled and matched to 50 Ω. A bias inductor is required on the RF output.

The typical gain and noise figure are 16.5 dB and 3.5 dB , respectively, from 2 GHz to 5 GHz. The typical output third-order intercept (OIP3) and output second-order intercept (OIP2) are 34.5 dBm and 53 dBm, respectively, from 2 GHz to 5 GHz. The nominal supply voltage is 5 V, and the supply current is 125 mA.

The ADL8154 is fabricated on gallium arsenide (GaAs), heterojunction bipolar transistor (HBT). The device is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP and is specified for operation from −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

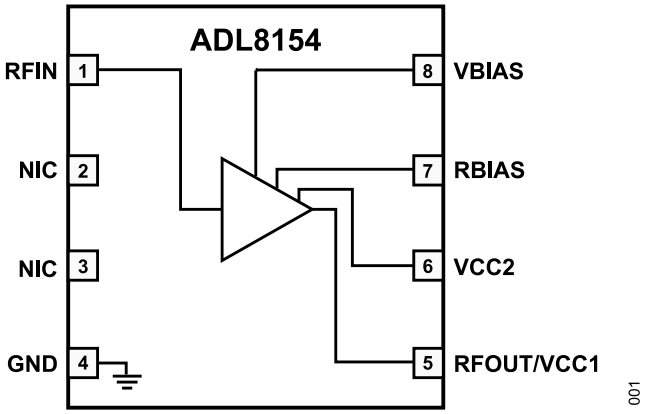

Figure 1. Functional Block Diagram

©2024-2026 Analog Devices, Inc. All rights reserved.

TABLE OF CONTENTS

Features 1
Applications 1
General Description 1
Functional Block Diagram 1
..... 1
Specifications 3
10 MHz to 2 GHz Frequency Range 3
2 GHz to 5 GHz Frequency Range 3
5 GHz to 6 GHz Frequency Range 4
DC Specifications 4
Absolute Maximum Ratings 5
Thermal Resistance 5
Electrostatic Discharge (ESD) Ratings 5
ESD Caution 5
Pin Configuration and Function Descriptions 6
Interface Schematics 6
Typical Performance Characteristics 7
Theory of Operation 19
Applications Information 20
Recommended Bias Sequencing 21
Recommended Power Management Circuit 22
Outline Dimensions 23
Ordering Guide 23
Evaluation Boards 23

REVISION HISTORY

11/2026—Rev. 0 to Rev. A

Changes to Figure 34 and Figure 35 11
Changes to Figure 39 12

11/2024—Revision 0: Initial Version

SPECIFICATIONS

10 MHZ TO 2 GHZ FREQUENCY RANGE

V_{CC} = 5 V, I_{CQ} = 125 mA, bias resistance (R_{BIAS}) = 680 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 10 MHz to 2 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.010		2	GHz	
GAIN (S21)		18		dB	
Gain Variation over Temperature		0.010		dB/°C	
NOISE FIGURE		4		dB	
PHASE NOISE		−172		dBc/Hz	Measurement taken at OP1dB and 10 kHz offset
RETURN LOSS					
Input (S11)		10		dB	
Output (S22)		10		dB	
OUTPUT					
OP1dB	18.5	21		dBm	
Saturated Power (P_{SAT})		22		dBm	
OIP3		38.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 5 dBm
OIP2		58.5		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
POWER ADDED EFFICIENCY (PAE)		25		%	Measured at P_{SAT}

2 GHZ TO 5 GHZ FREQUENCY RANGE

V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 2 GHz to 5 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2		5	GHz	
S21	14.5	16.5		dB	
Gain Variation over Temperature		0.020		dB/°C	
NOISE FIGURE		3.5		dB	
PHASE NOISE		−172		dBc/Hz	Measurement taken at OP1dB and 10 kHz offset
RETURN LOSS					
S11		14		dB	
S22		11		dB	
OUTPUT					
OP1dB	18.5	21		dBm	
P_{SAT}		22.5		dBm	
OIP3		34.5		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
OIP2		53		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
PAE		23.5		%	Measured at P_{SAT}

SPECIFICATIONS

5 GHZ TO 6 GHZ FREQUENCY RANGE

V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 5 GHz to 6 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	5		6	GHz	
S21	12	14.5		dB	
Gain Variation over Temperature		0.025		dB/°C	
NOISE FIGURE		4.5		dB	
PHASE NOISE		−172		dBc/Hz	Measurement taken at OP1dB and 10 kHz offset
RETURN LOSS					
S11		14.5		dB	
S22		12		dB	
OUTPUT					
OP1dB		19		dBm	
P_{SAT}		20.5		dBm	
OIP3		31		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
OIP2		53		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
PAE		15		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 4. DC Specifications

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{CQ}		125		mA
Amplifier Current (I_{CQ_AMP})		123		mA
RBIAS Current (I_{RBIAS})		2		mA
SUPPLY VOLTAGE				
V_{CC}	4	5	5.5	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{CC}	6.5 V
RF Input Power (RFIN)	27 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 14.9 mW/°C Above 85°C)	1.34 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Quiescent Junction (T_{CASE} = 85°C, V_{CC} = 5 V, I_{CQ} = 125 mA, Input Power (P_{IN}) = Off)	127°C
Maximum Junction	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{CASE} = 25°C	59.5	°C/W
Worst Case[2], T_{CASE} = 85°C	67.2	°C/W

[1] Thermal resistance varies with operating conditions.

[2] Across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8154

Table 7. ADL8154, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

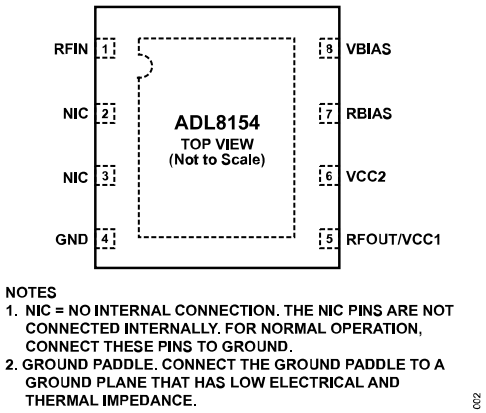

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. The RFIN pin is DC-coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
2, 3	NIC	No Internal Connection. The NIC pins are not connected internally. For normal operation, connect these pins to ground.
4	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 4 for the interface schematic.
5	RFOUT/VCC1	RF Output and Collector Bias Voltage. RFOUT is DC-coupled and also serves as the collector biasing node. For the collector bias (VCC1), connect a DC bias network to provide the collector current (I_{CC}) and AC-couple the RF output path. See Figure 5 for the interface schematic.
6	VCC2	Collector Bias. Connect VCC2 to a common supply with VCC1. See Figure 6 for the interface schematic.
7	RBIAS	Bias Setting Resistor. Connect a resistor between the RBIAS pin and VCC1 and VCC2 pins to set I_{CQ}. See Figure 82 and Table 9 for more details. See Figure 7 for the interface schematic.
8	VBIAS	Bias Setting Voltage Output. VBIAS sets the bias voltage for the RFIN pin. Connect VBIAS to RFIN using an inductor or ferrite bead as shown in Figure 82. See Figure 8 for the interface schematic
	GROUND PADDLE	Ground Paddle. Connect the ground paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

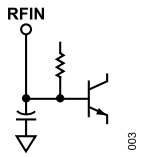

Figure 3. RFIN Interface Schematic



Figure 4. GND Interface Schematic

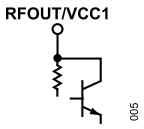

Figure 5. RFOUT/VCC1 Interface Schematic

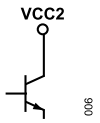

Figure 6. VCC2 Interface Schematic

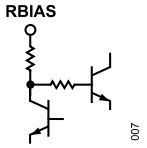

Figure 7. RBIAS Interface Schematic

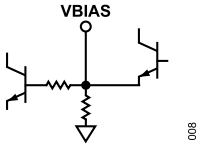

Figure 8. VBIAS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

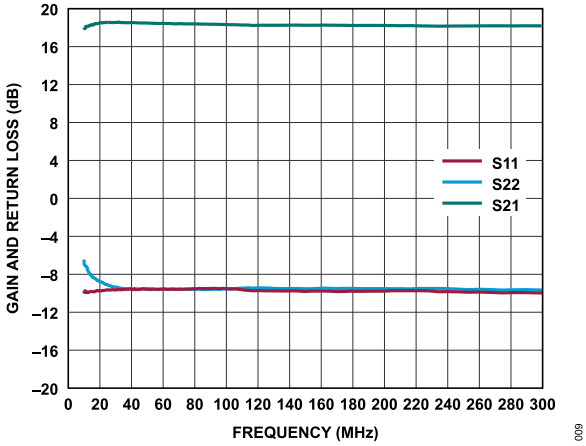

Figure 9. Gain and Return Loss vs. Frequency, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

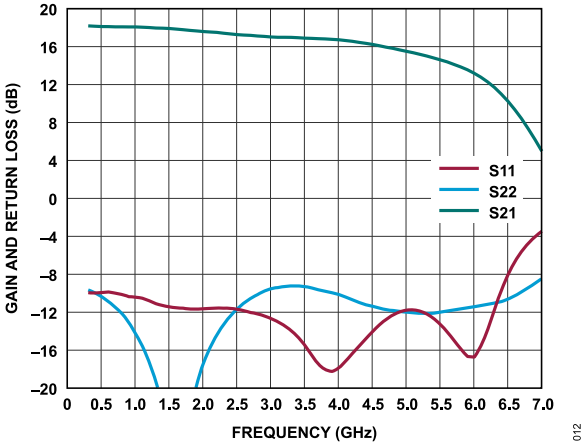

Figure 12. Gain and Return Loss vs. Frequency, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

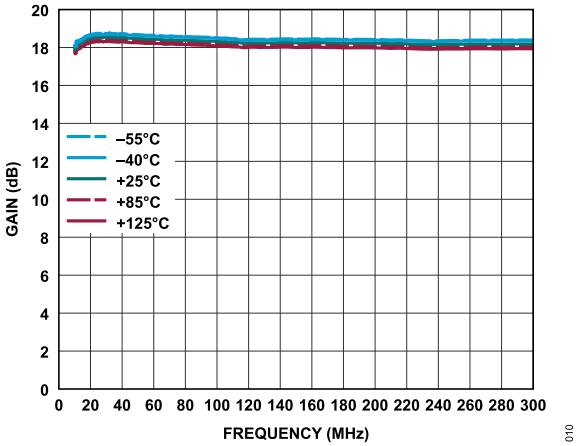

Figure 10. Gain vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

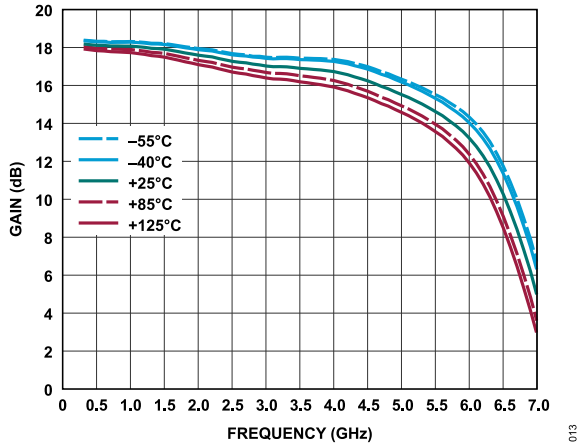

Figure 13. Gain vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

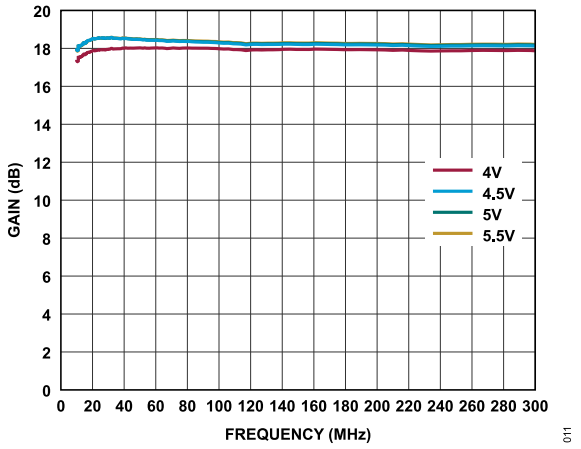

Figure 11. Gain vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

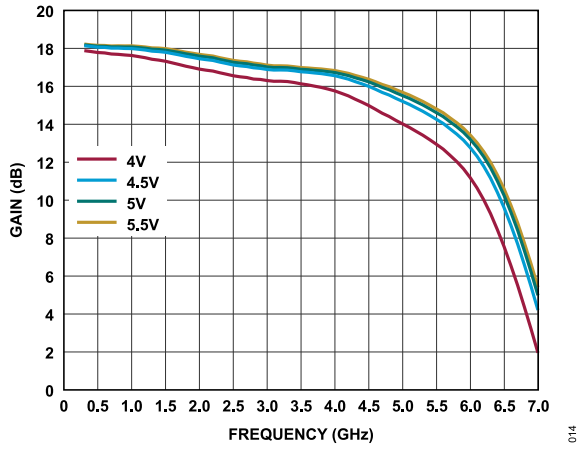

Figure 14. Gain vs. Frequency for Various Supply Voltages 300 MHz to 7 GHz, I_{CQ} = 125 mA

TYPICAL PERFORMANCE CHARACTERISTICS

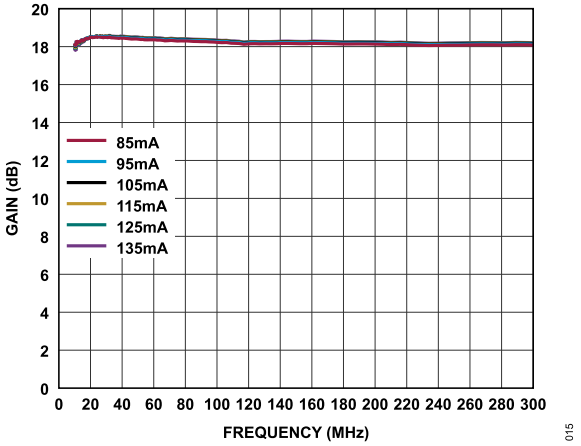

Figure 15. Gain vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

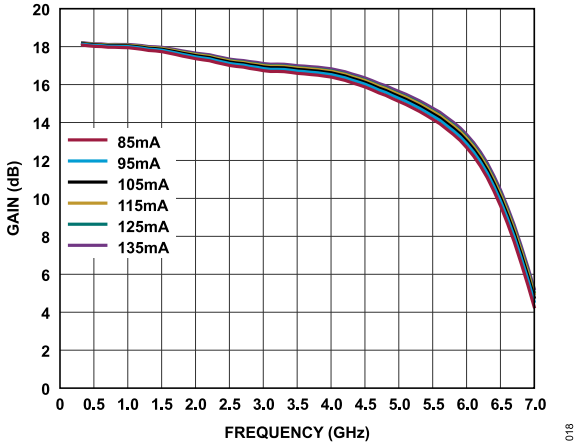

Figure 18. Gain vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

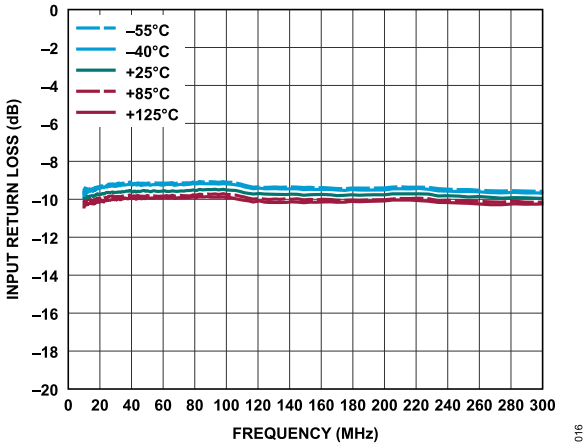

Figure 16. Input Return Loss vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

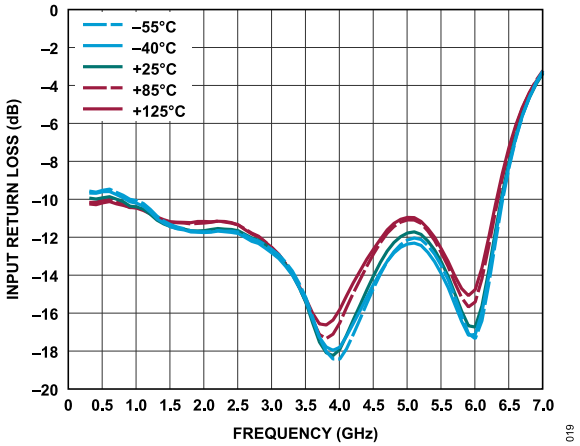

Figure 19. Input Return Loss vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

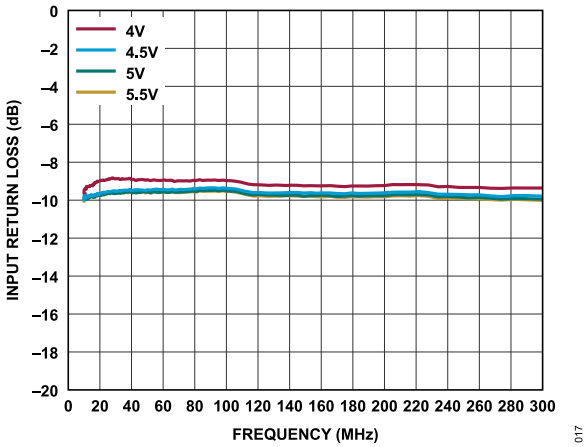

Figure 17. Input Return Loss vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

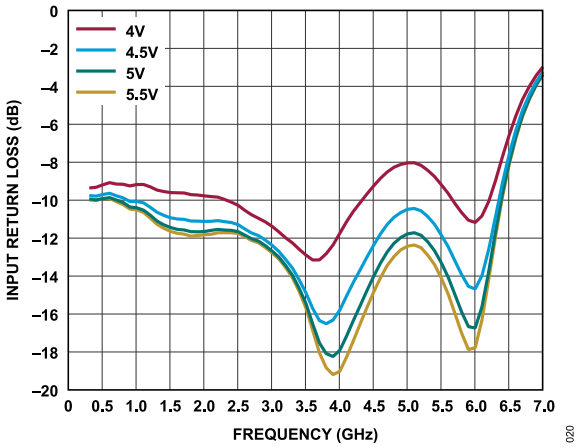

Figure 20. Input Return Loss vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

TYPICAL PERFORMANCE CHARACTERISTICS

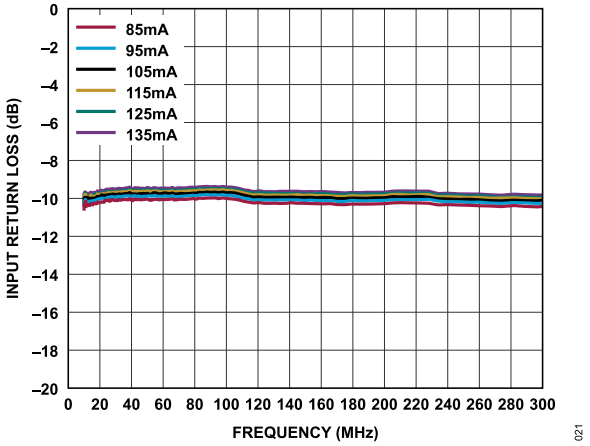

Figure 21. Input Return Loss vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

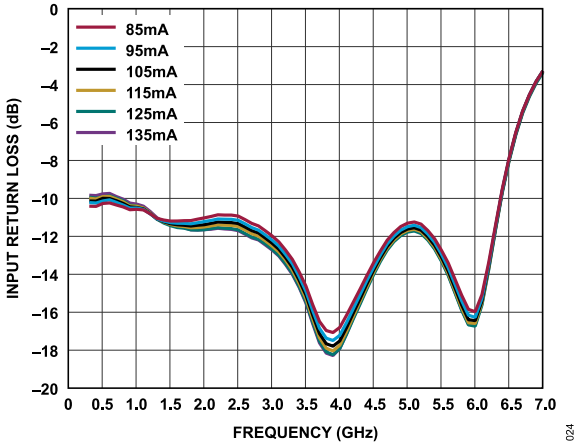

Figure 24. Input Return Loss vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

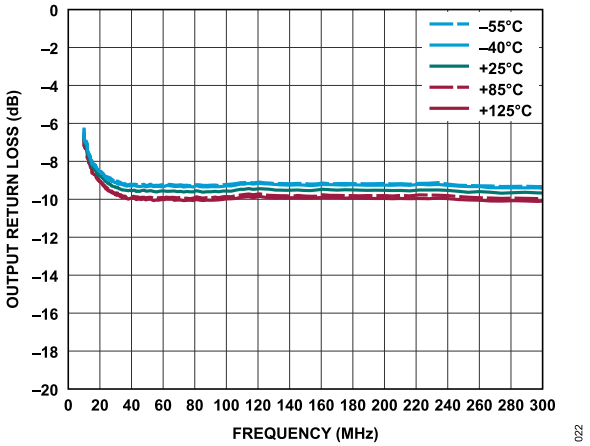

Figure 22. Output Return Loss vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

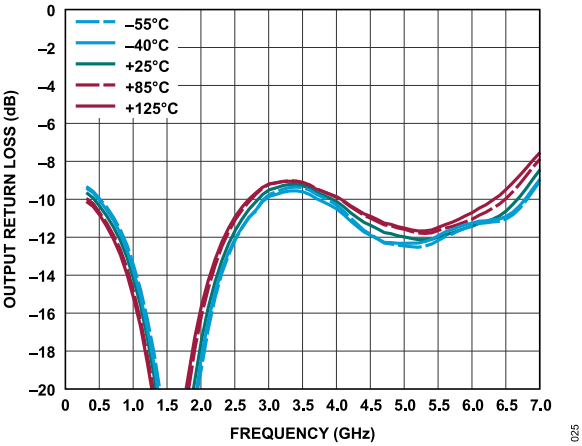

Figure 25. Output Return Loss vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

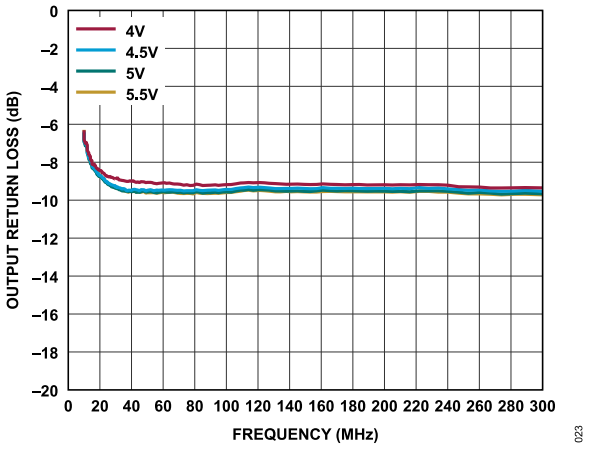

Figure 23. Output Return Loss vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

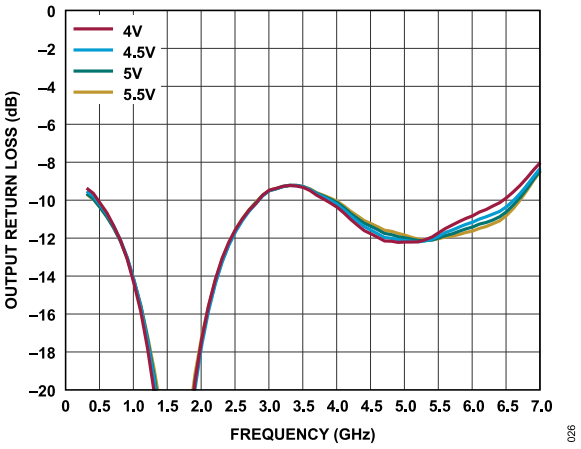

Figure 26. Output Return Loss vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

TYPICAL PERFORMANCE CHARACTERISTICS

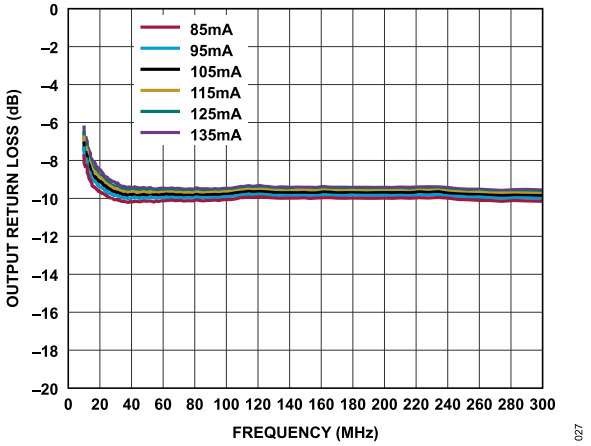

Figure 27. Output Return Loss vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

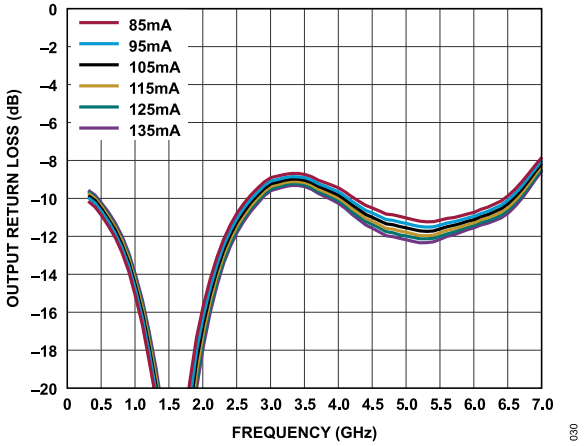

Figure 30. Output Return Loss vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

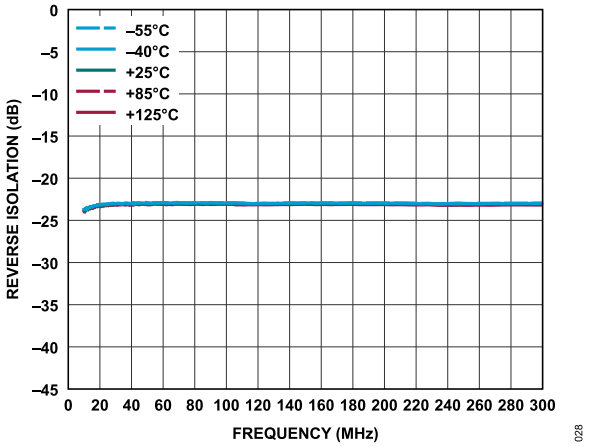

Figure 28. Reverse Isolation vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

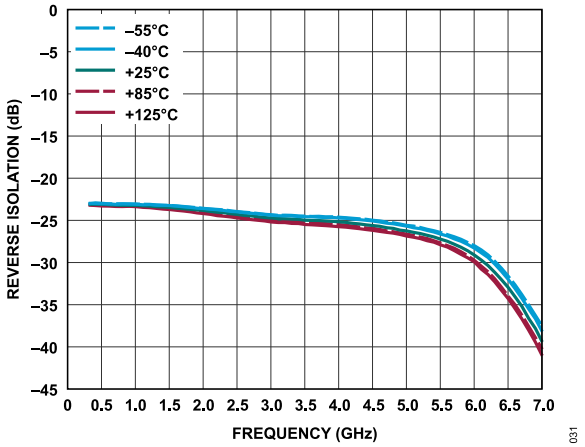

Figure 31. Reverse Isolation vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

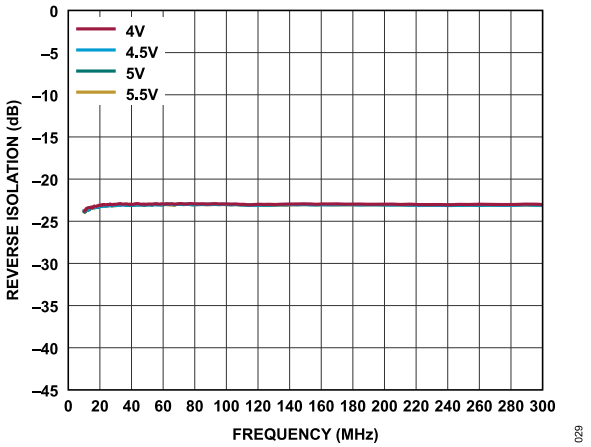

Figure 29. Reverse Isolation vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

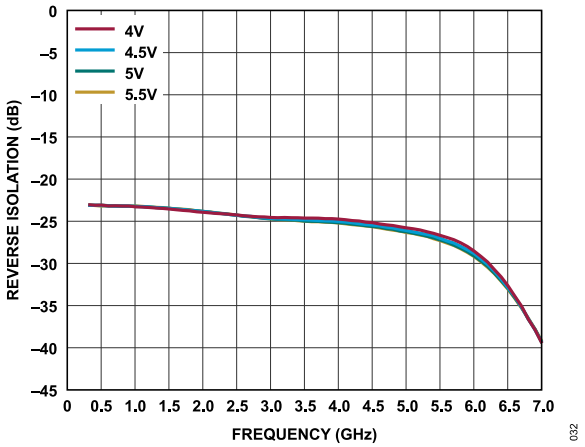

Figure 32. Reverse Isolation vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

TYPICAL PERFORMANCE CHARACTERISTICS

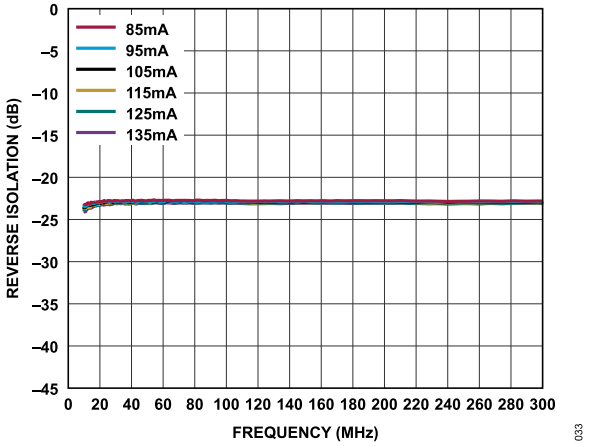

Figure 33. Reverse Isolation vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

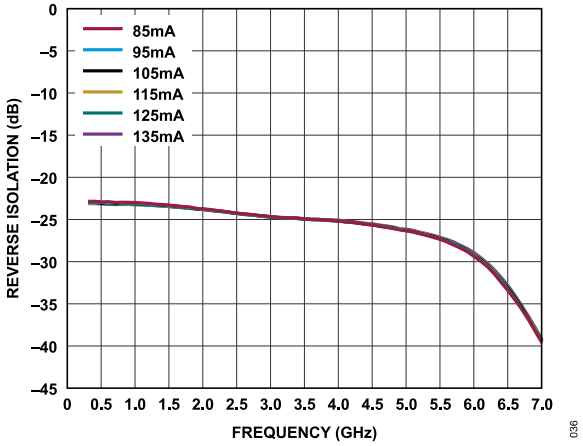

Figure 36. Reverse Isolation vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

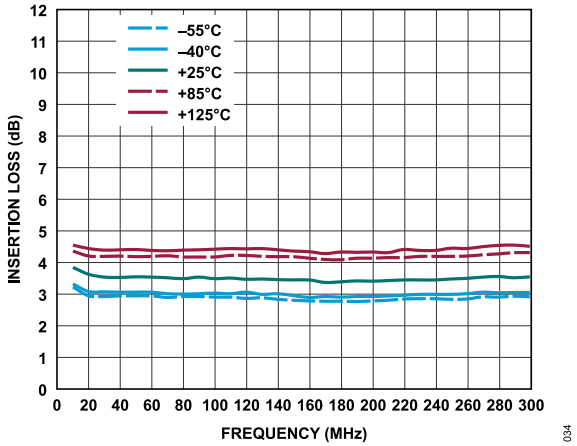

Figure 34. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

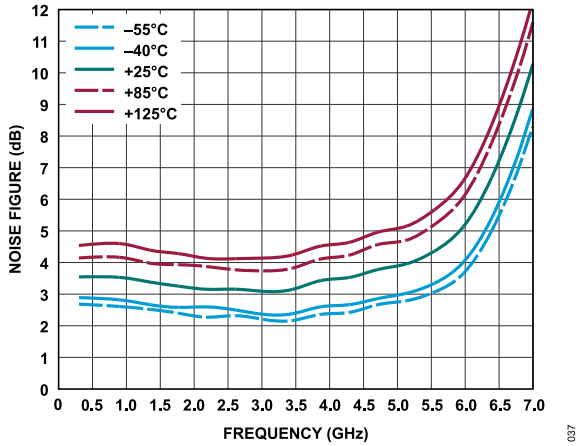

Figure 37. Noise Figure vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

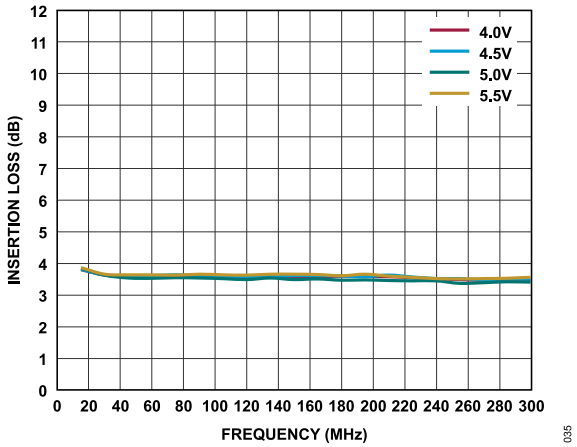

Figure 35. Noise Figure vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

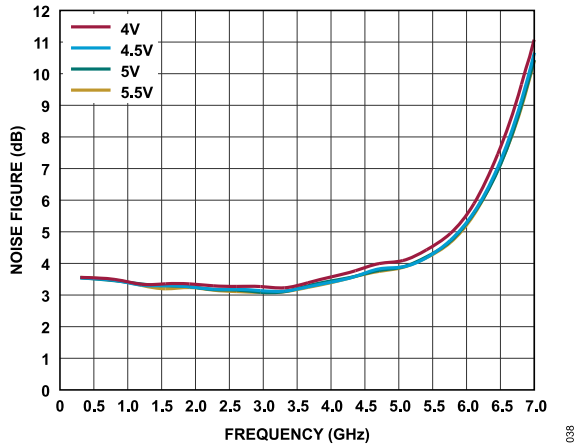

Figure 38. Noise Figure vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

TYPICAL PERFORMANCE CHARACTERISTICS

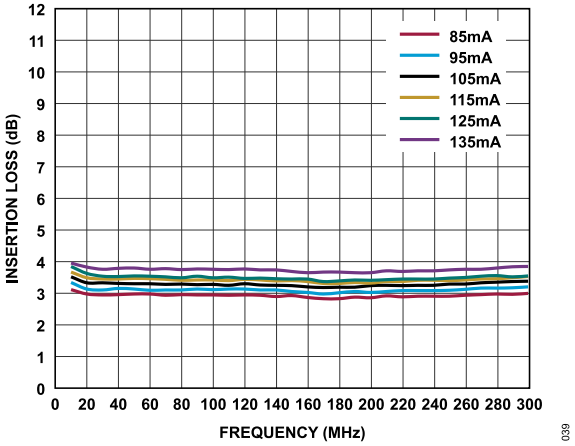

Figure 39. Noise Figure vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

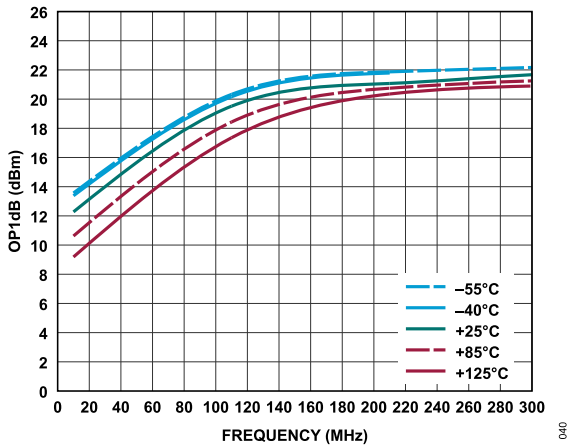

Figure 40. OP1dB vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

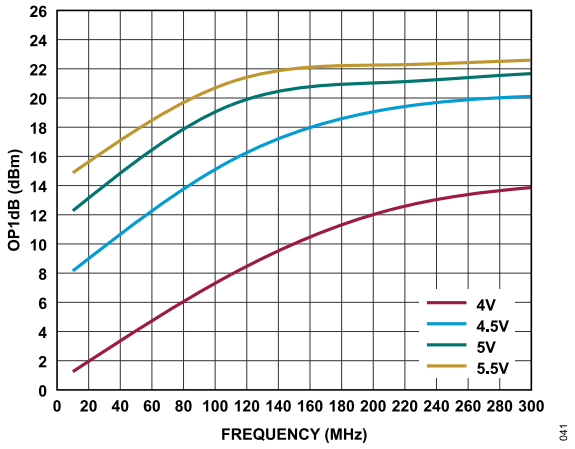

Figure 41. OP1dB vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

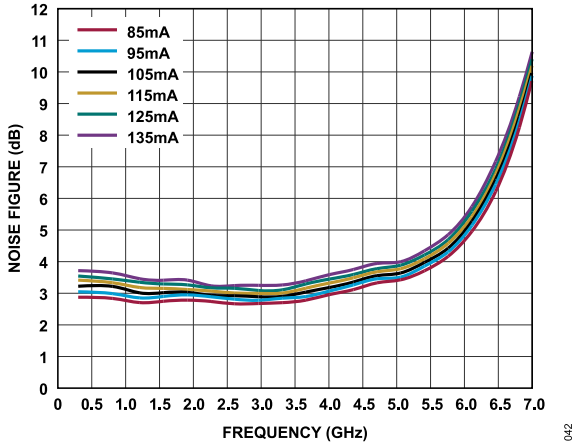

Figure 42. Noise Figure vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

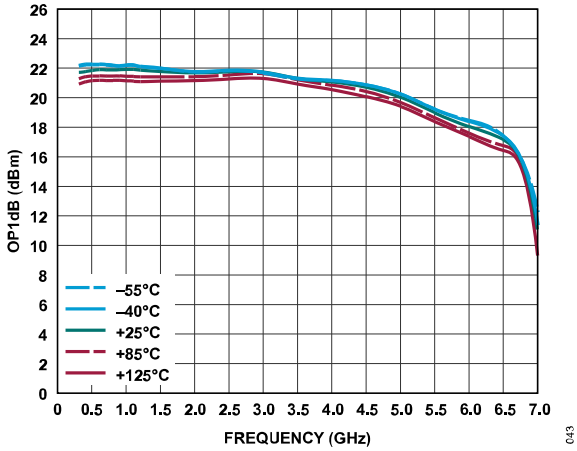

Figure 43. OP1dB vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

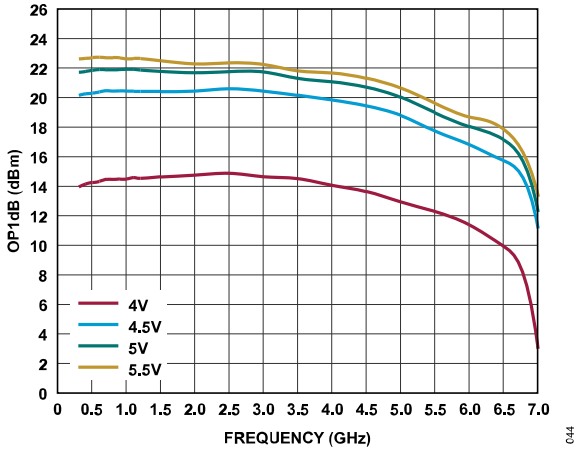

Figure 44. OP1dB vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

TYPICAL PERFORMANCE CHARACTERISTICS

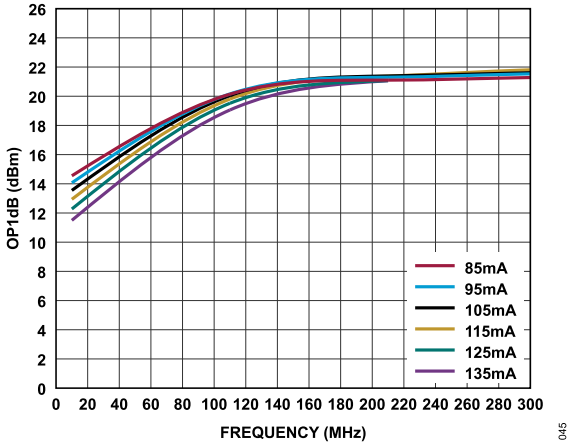

Figure 45. OP1dB vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

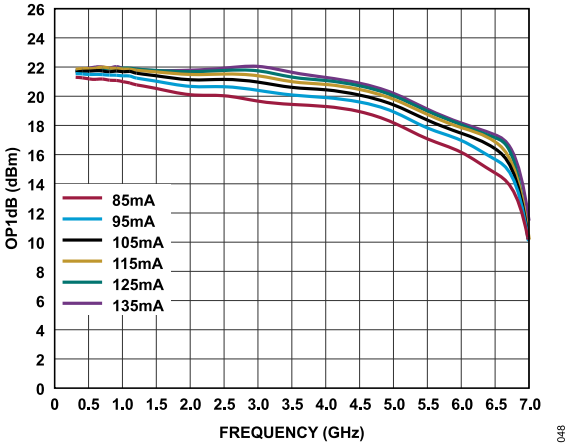

Figure 48. OP1dB vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

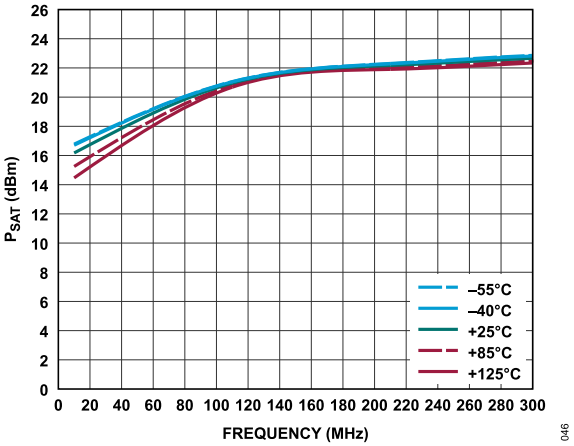

Figure 46. P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

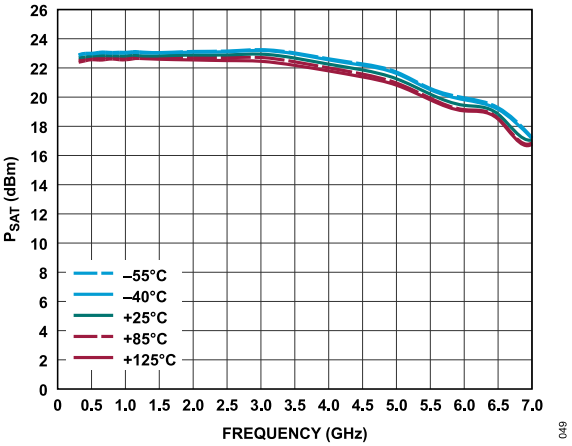

Figure 49. P_{SAT} vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

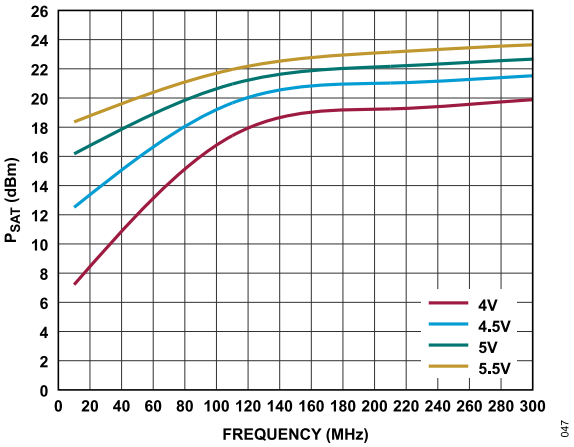

Figure 47. P_{SAT} vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

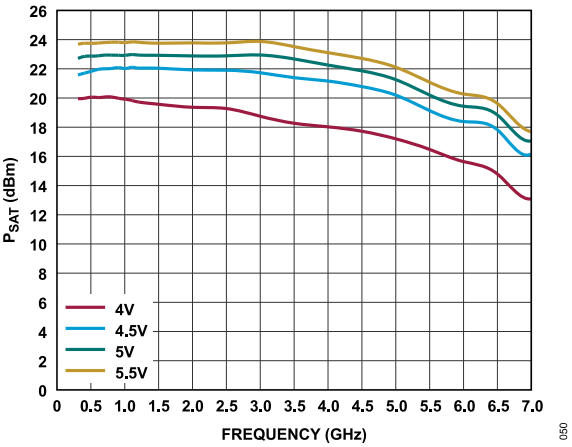

Figure 50. P_{SAT} vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

TYPICAL PERFORMANCE CHARACTERISTICS

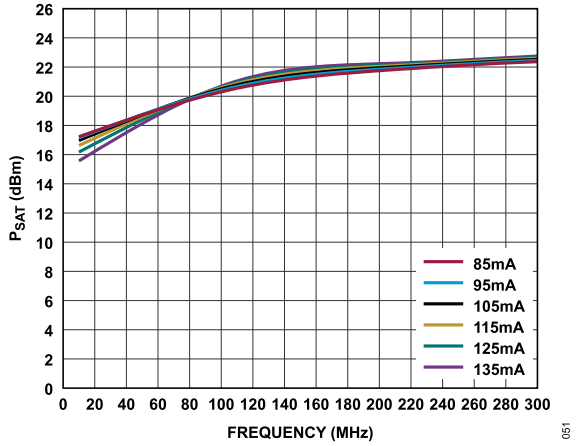

Figure 51. P_{SAT} vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

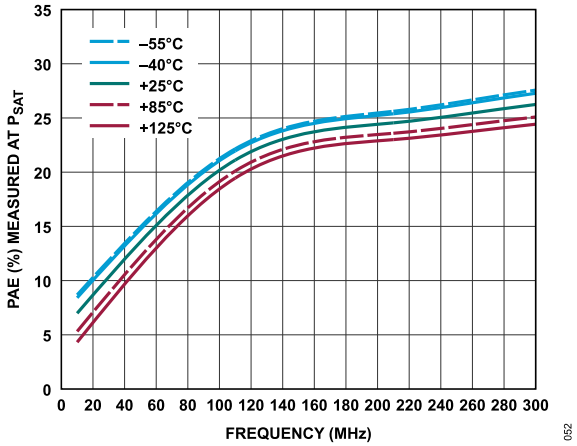

Figure 52. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

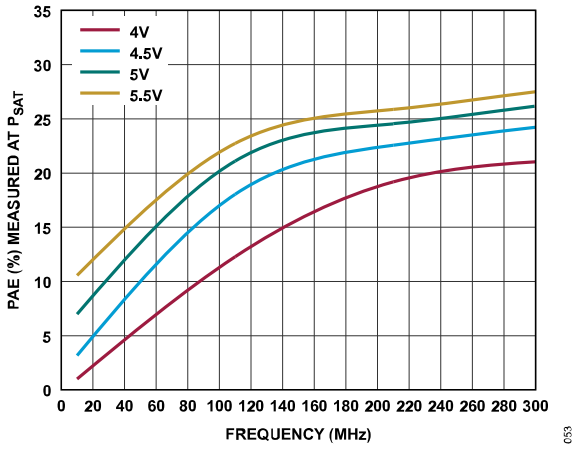

Figure 53. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

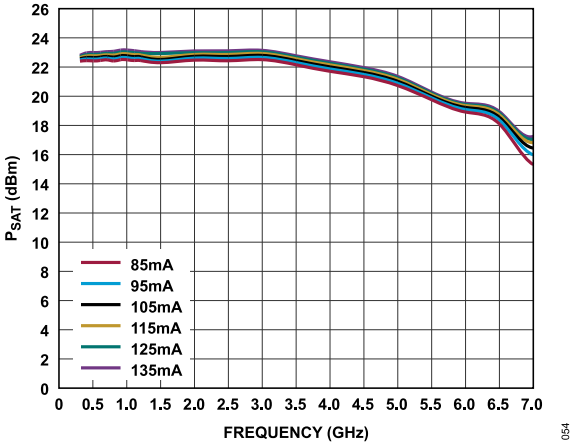

Figure 54. P_{SAT} vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

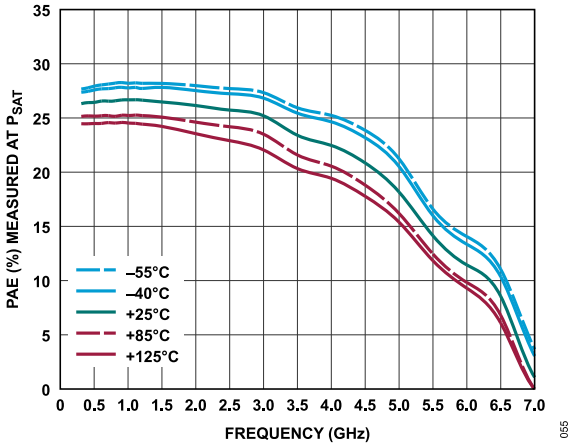

Figure 55. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

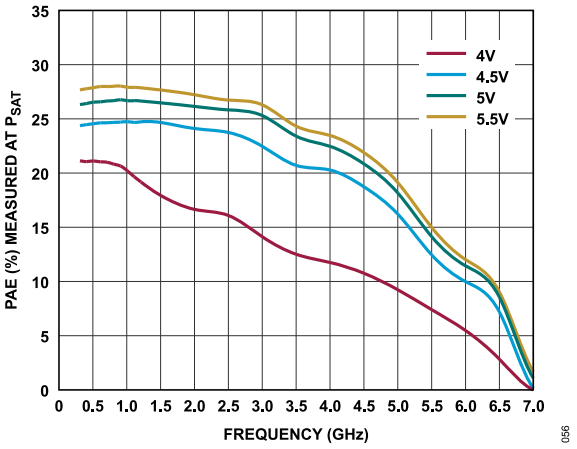

Figure 56. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

TYPICAL PERFORMANCE CHARACTERISTICS

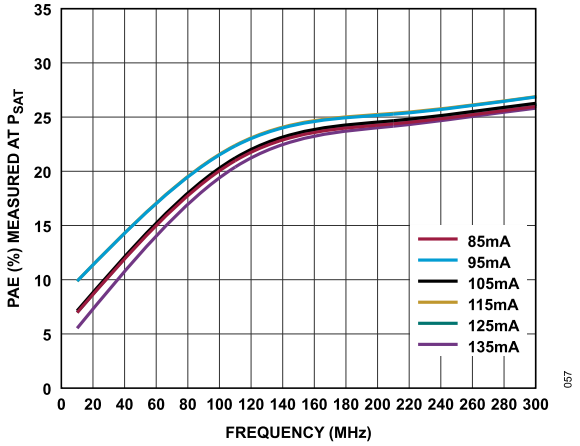

Figure 57. PAE Measured at P_{SAT} vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

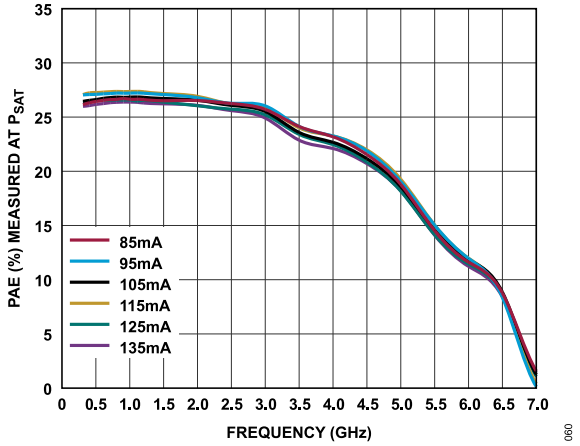

Figure 60. PAE Measured at P_{SAT} vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

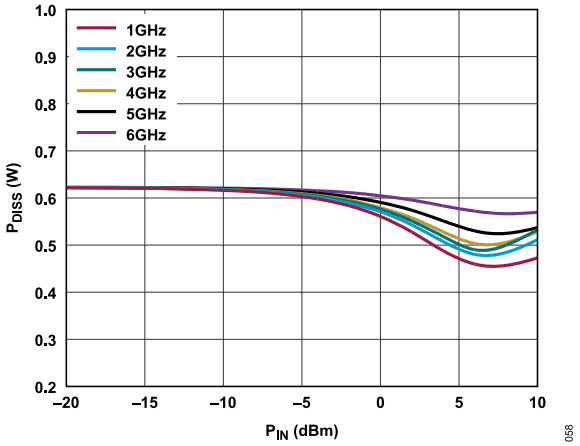

Figure 58. P_{DISS} vs. P_{IN} at Various Frequencies, T_{CASE} = 85°C, V_{CC} = 5 V

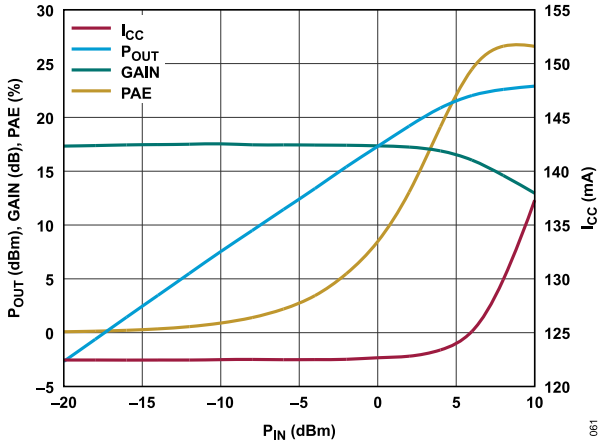

Figure 61. P_{OUT}, GAIN, PAE, and I_{CC} vs. P_{IN}, Power Compression at 2 GHz, V_{CC} = 5 V, R_{BIAS} = 680 Ω

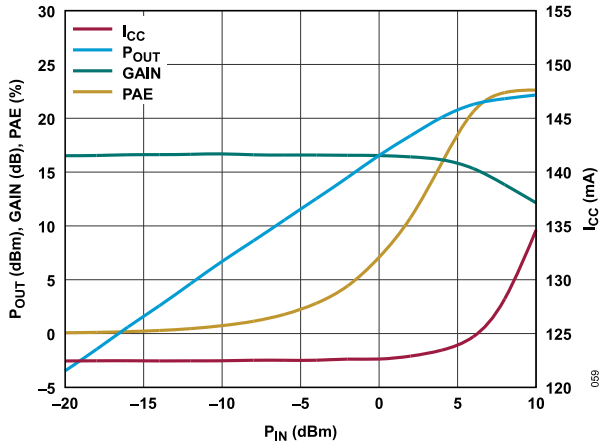

Figure 59. P_{OUT}, GAIN, PAE, and I_{CC} vs. P_{IN}, Power Compression at 4 GHz, V_{CC} = 5 V, R_{BIAS} = 680 Ω

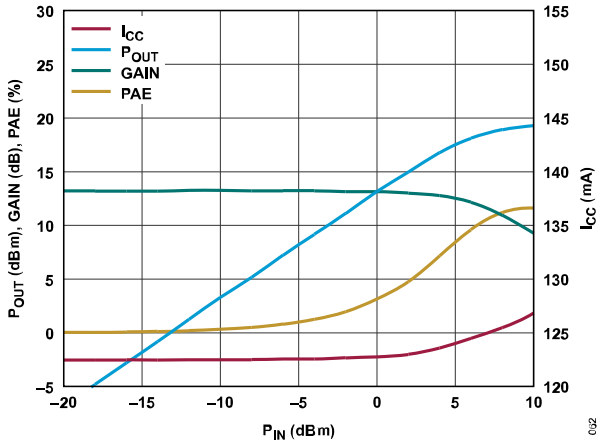

Figure 62. P_{OUT}, GAIN, PAE, and I_{CC} vs. P_{IN}, Power Compression at 6 GHz, V_{CC} = 5 V, R_{BIAS} = 680 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

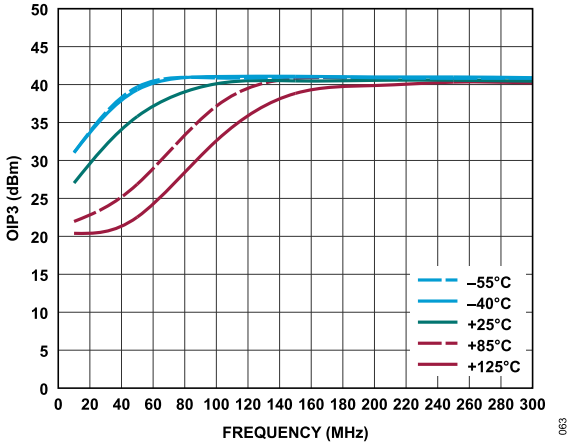

Figure 63. OIP3 vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

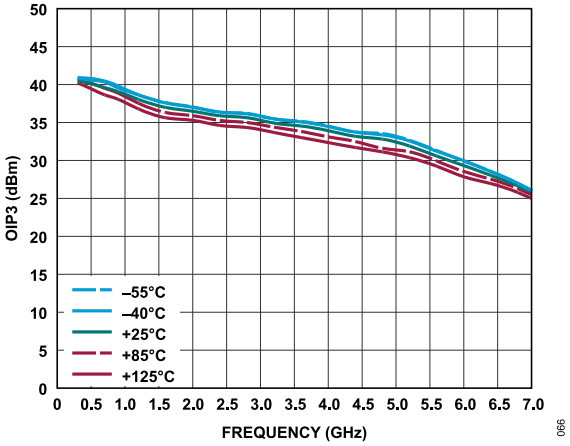

Figure 66. OIP3 vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

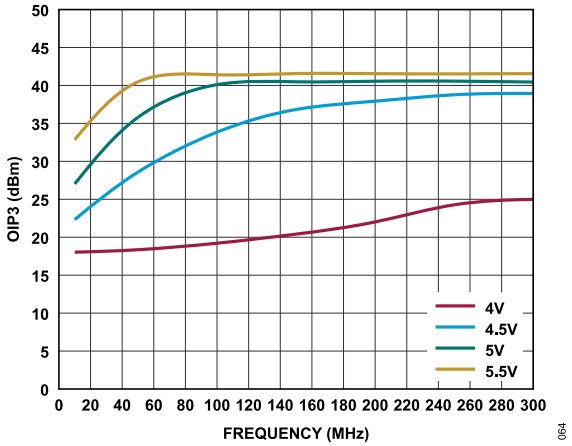

Figure 64. OIP3 vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

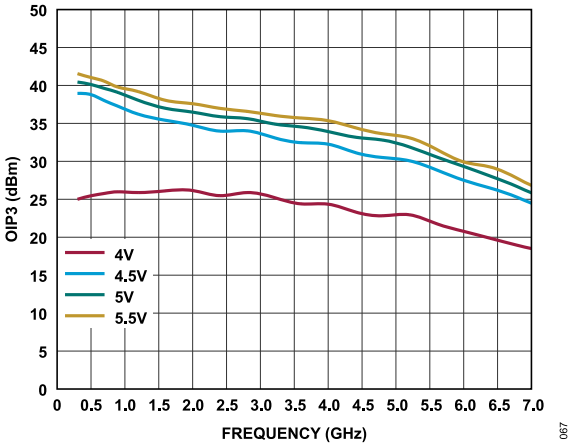

Figure 67. OIP3 vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

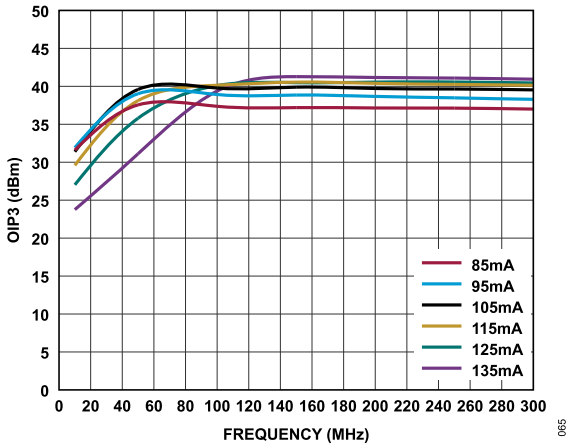

Figure 65. OIP3 vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

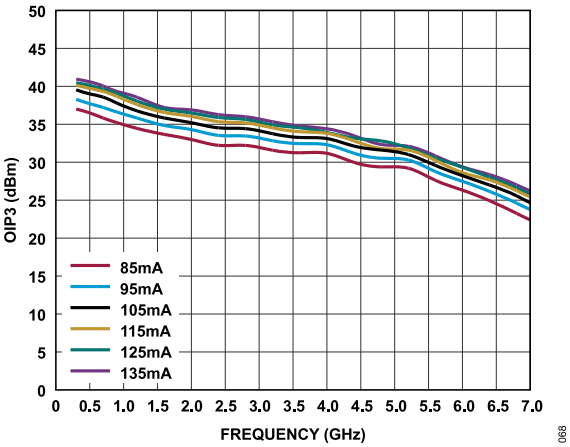

Figure 68. OIP3 vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

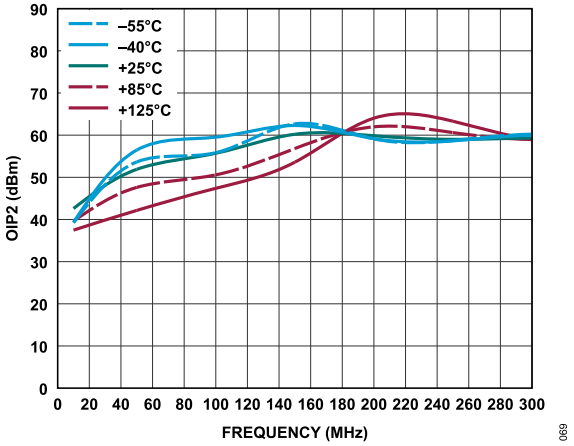

Figure 69. OIP2 vs. Frequency for Various Temperatures, 10 MHz to 300 MHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

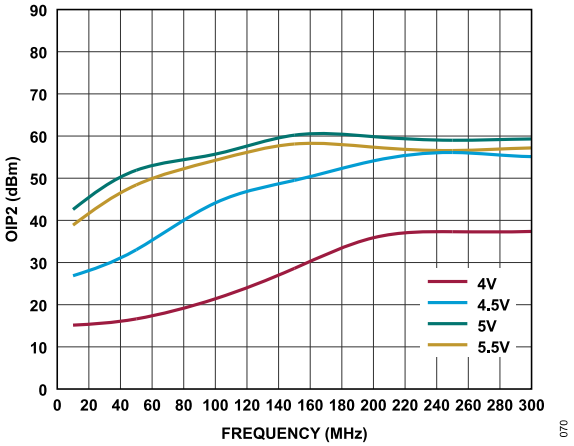

Figure 70. OIP2 vs. Frequency for Various Supply Voltages, 10 MHz to 300 MHz, I_{CQ} = 125 mA

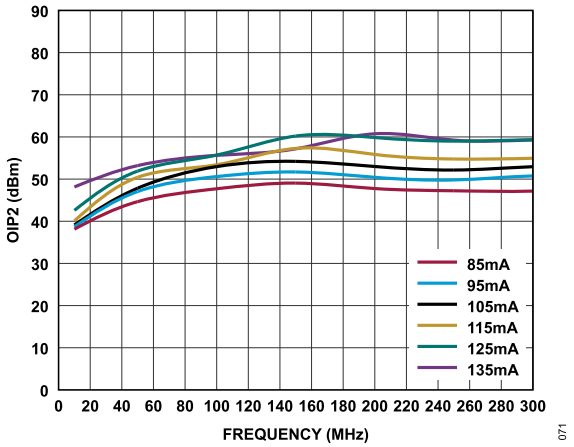

Figure 71. OIP2 vs. Frequency for Various I_{CQ} Values, 10 MHz to 300 MHz, V_{CC} = 5 V

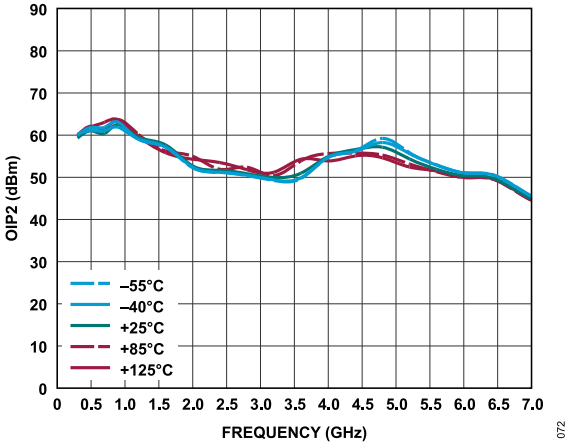

Figure 72. OIP2 vs. Frequency for Various Temperatures, 300 MHz to 7 GHz, V_{CC} = 5 V, I_{CQ} = 125 mA, R_{BIAS} = 680 Ω

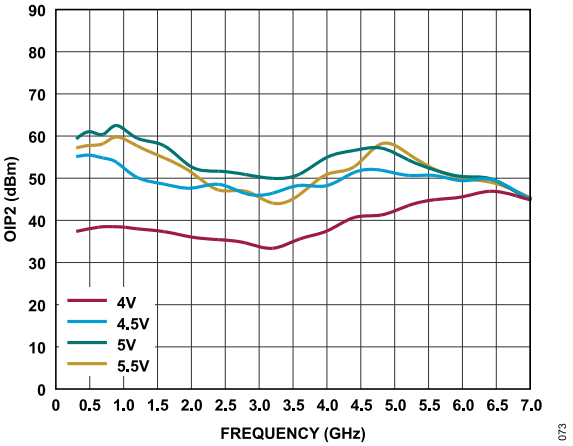

Figure 73. OIP2 vs. Frequency for Various Supply Voltages, 300 MHz to 7 GHz, I_{CQ} = 125 mA

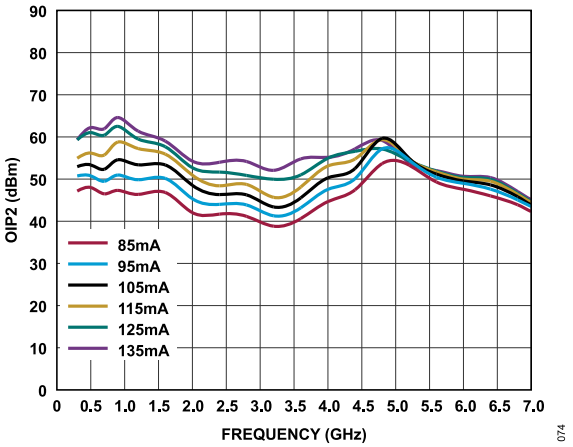

Figure 74. OIP2 vs. Frequency for Various I_{CQ} Values, 300 MHz to 7 GHz, V_{CC} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

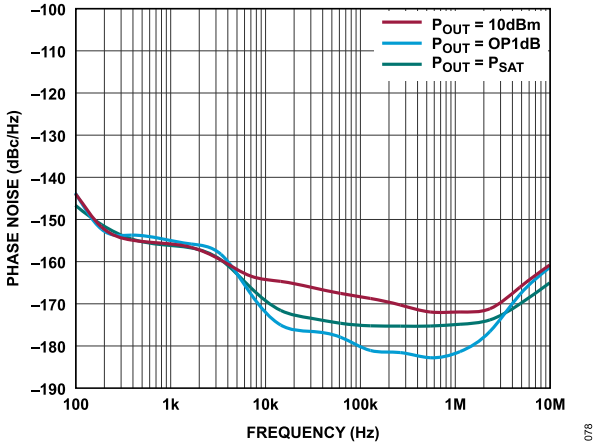

Figure 75. Phase Noise vs. Frequency at 2 GHz for Various P_{OUT} Values

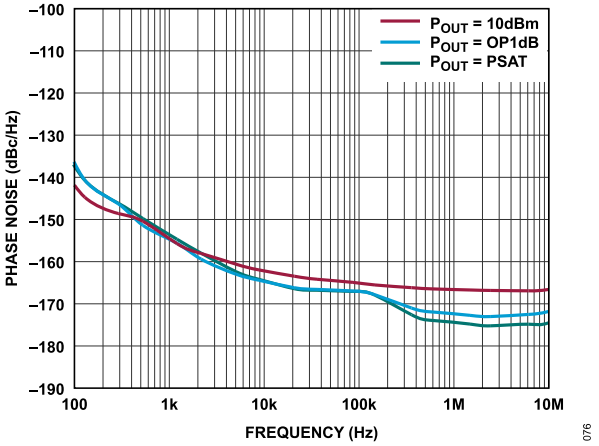

Figure 78. Phase Noise vs. Frequency at 5 GHz for Various P_{OUT} Values

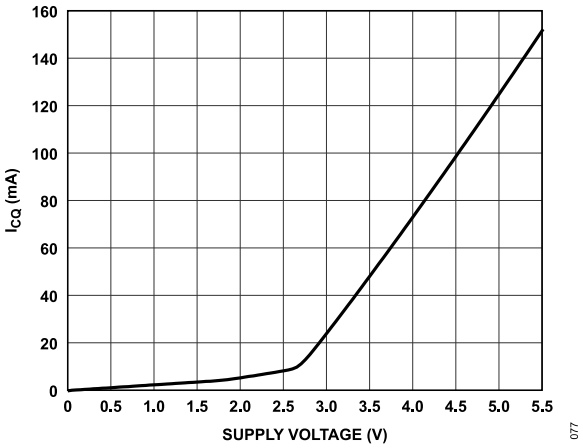

Figure 76. I_{CQ} vs. Supply Voltage, R_{BIAS} = 680 Ω

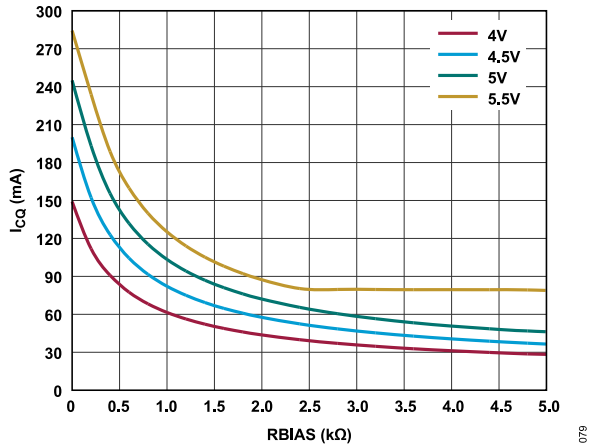

Figure 79. I_{CQ} vs. RBIAS at Various Supply Voltages, 0 Ω to 5 kΩ

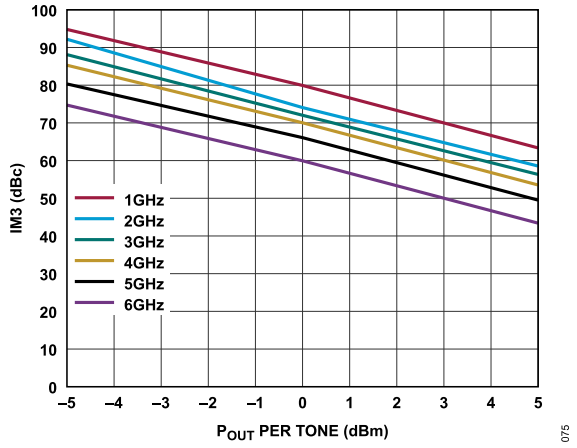

Figure 77. Third-Order Intermodulation Distortion (IM3) vs P_{OUT} per Tone for Various Frequencies, V_{CC} = 5 V, R_{BIAS} = 680 Ω

THEORY OF OPERATION

The ADL8154 is a wideband low phase noise amplifier that operates from 10 MHz to 6 GHz. A simplified block diagram is shown in Figure 80.

The ADL8154 has DC-coupled, single-ended input and output ports with impedances that are nominally equal to 50 Ω over the specified frequency range. No external matching components are required; other than AC input and output coupling capacitors and a bias inductor. To adjust I_{CQ}, connect an external resistor between the RBIAS and VCC1 and VCC2 pins. The VBIAS output voltage provides a DC bias voltage; it connects to RFIN through a ferrite bead. The RFOUT/VCC1 pin provides the I_{CC}. Additional collector biasing is applied through the VCC2 pin.

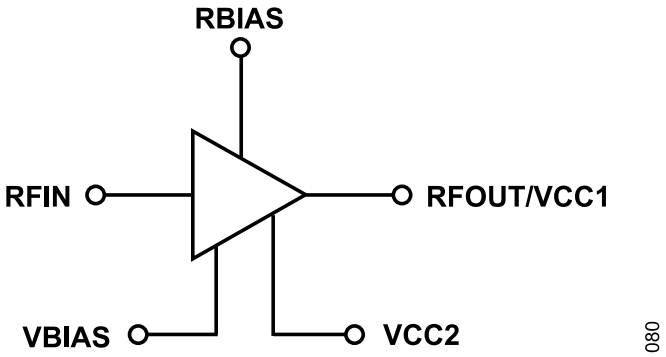

Figure 80. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8154 over the specified frequency range are shown in Figure 82, and it also shows the configuration used to characterize and qualify the ADL8154.

To set I_{CQ}, connect a resistor (R1) between the RBIAS and VCC1 and VCC2 pins. A default value of 680 Ω is recommended, which results in a nominal I_{CQ} of 125 mA. Table 9 shows how the I_{CQ} and I_{CQ_AMP} varies vs. the R_{BIAS}. The RBIAS pin also draws a current that varies with the value of R_{BIAS} (see Table 9). Do not leave the RBIAS pin open.

Figure 83 shows an alternate application circuit for use when there is a requirement to reduce the number of components around the ADL8154 to save space. In this alternate application circuit, the C4 and L2 components are removed, and L1 is changed from a 2.2 kΩ ferrite bead to a 900 nH wire wound inductor (Coilcraft 0402DF-901XJRW). S-parameter performance for the alternate application circuit is shown in Figure 81. Compare Figure 81 to Figure 9 and Figure 12 to see that there is no performance impact on the S-parameters compared to the nominal performance shown in Figure 9 and Figure 12.

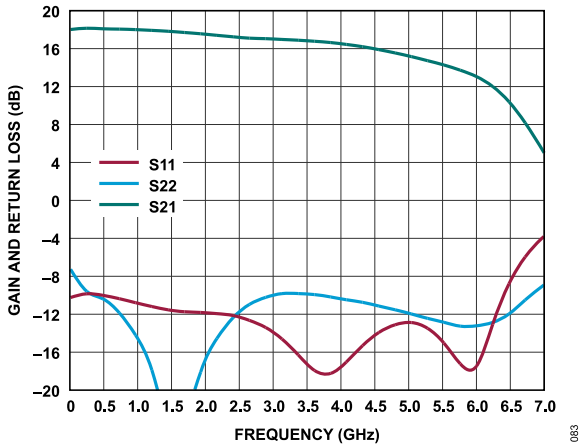

Figure 81. Broadband S-Parameters, L2 and C4 Removed, and L1 Changed from 2.2 kΩ Ferrite Bead to 900 nH Wire Wound Inductor

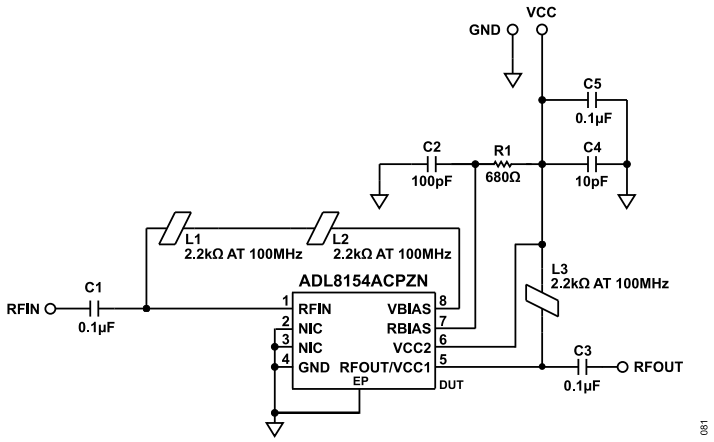

Figure 82. Typical Application Circuit

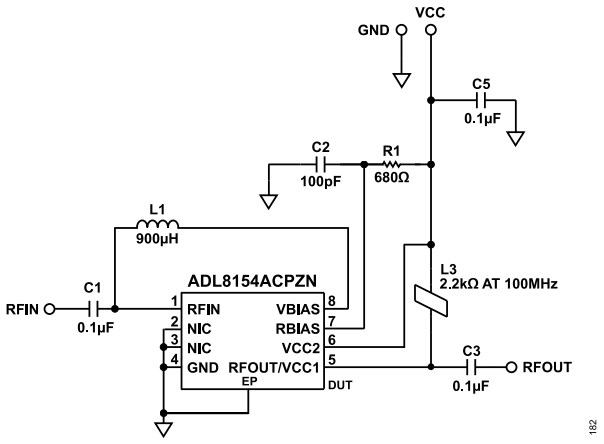

Figure 83. Alternate Application Circuit, C4 and L2 Removed and L1 Changed from 2.2 kΩ Ferrite Bead to 900 nH Wire Wound Inductor

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCING

The correct sequencing of the DC and RF power is required to safely operate the ADL8154. During power-up, apply V_{CC} before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before V_{CC} is powered off.

See the ADL8154-EVALZ user guide for the recommended bias sequencing information.

Table 9. Recommended Bias Resistor Values for Various I_{CQ} Values, V_{CC} = 5 V

R_{BIAS} (Ω)	I_{CQ} (mA)	I_{CQ_AMP} (mA)	I_{RBIAS} (mA)
1470	85	83.8	1.2
1180	95	93.6	1.4
976	105	103.4	1.6
806	115	113.2	1.8
680	125	123	2
562	135	132.7	2.3

Table 10. Recommended Bias Resistor Values for Various Supply Voltages, I_{CQ} = 125 mA

R_{BIAS} (Ω)	V_{CC} (V)
102	4.0
365	4.5
680	5
1000	5.5

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 84 shows a recommended power management circuit for the ADL8154. The LT8607 step-down regulator is used to step down a 12 V rail to 6.5 V, which is then applied to the LT3045 low dropout (LDO) linear regulator to generate a low noise 5 V output. The 5.5 V regulator output (V_{REG}) of the LT8607 is set by the R4A and R5A resistors, according to the following equation:

$$R5A = \frac{R4A}{\left(\left(\frac{V_{REG}}{0.778}\right) - 1\right)}$$

The switching frequency (f_{SW}) is set to 2 MHz by the 18.2 kΩ resistor (R2A) on the RT pin of the LT8607. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.2 MHz.

The output voltage (V_{OUT}) of the LT3045 is set by the R3B resistor connected to the SET pin, according to the following equation:

$$R3B = \frac{V_{OUT}}{(100\ \mu A)}$$

The resistors on the PGFB pins of LT3045 are chosen to trigger the power-good (PG) signal when the output reaches 90% of its target voltage of 5 V. The PG open-collector output is pulled up to the 5 V output to give a convenient 0 V or 5 V output voltage.

Table 11 provides the recommended resistor values to set the V_{OUT} of the LT3045 and the PG threshold at 90% for various V_{OUT} values. Table 11 also provides the required resistor values to set the V_{OUT} of the LT8607 to 500 mV greater than the V_{OUT} of the LT3045. Note that the dropout voltage of the LT3045 can be reduced to a minimum of 350 mA for output currents up to 200 mA.

The LT8607 can source a maximum current of 750 mA, and the LT3045 can source a maximum current of 500 mA. If the 5 V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The LT8608 and LT8609 step-down regulators can source a maximum current to 1.5 A and 3 A, respectively, and these devices are pin compatible with the LT8607.

Table 11. Recommended Resistor Values for Operating at 4 V to 5.5 V

LT3045 LDO V_{OUT} and PG Threshold				LT8607 Regulator V_{OUT}		
V_{OUT} (V)	R3B (kΩ)	R5B (kΩ)	R6B (kΩ)	Recommended V_{REG} (V)	R4A (MΩ)	R5A (kΩ)
4	40.2	453	41.2	4.5	1	210
4.5	45	453	33.6	5.0	1	184
5	49.9	453	32.4	5.5	1	165
5.5	55	453	29.2	6.0	1	149

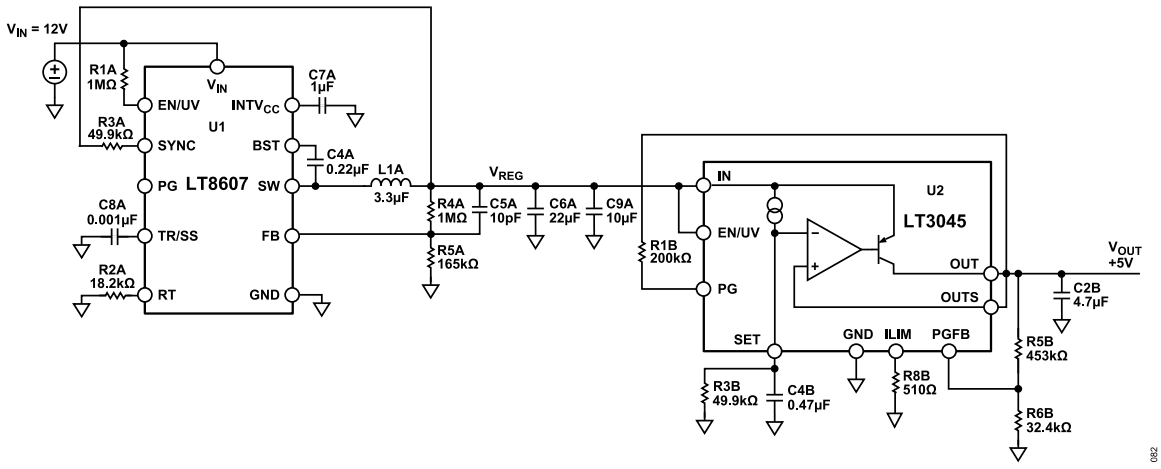

Figure 84. Recommended Power Management Circuit

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CP-8-30	LFCSP	8-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

Updated: November 13, 2026

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8154ACPZN	-55°C to +125°C	8-lead LFCSP 2 mm × 2 mm × 0.85	REEL, 3000	CP-8-30
ADL8154ACPZN-R7	-55°C to +125°C	8-lead LFCSP 2 mm × 2 mm × 0.85	REEL, 3000	CP-8-30

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADL8154-EVALZ	ADL8154 Evaluation Board

[1] Z = RoHS Compliant Part.

Legal Terms and Conditions
Analog Devices, Inc. (“ADI”) believes the information in this data sheet is accurate and reliable as of its date of publication and provides it “as is” without any representation or warranty of any kind. ADI reserves the right to make changes, corrections, modifications, enhancements, improvements, and other updates to the information described in this data sheet, with use of the product subject to ADI’s Terms and Conditions of Sale, available on Analog.com. ANALOG DEVICES word mark and logo, AD, and ADI are registered trademarks and trademarks owned by ADI. This data sheet, trademarks, and its content are owned by ADI and may not be reproduced, distributed, or used except with ADI’s prior written authorization. TO THE MAXIMUM EXTENT PERMITTED BY LAW, IN NO EVENT SHALL ADI BE LIABLE FOR ANY DAMAGES WHATSOEVER, WHETHER DIRECT OR INDIRECT, ARISING OUT OF OR IN CONNECTION WITH THE USE OF, INABILITY TO USE, OR RELIANCE UPON THIS DATA SHEET OR THE INFORMATION CONTAINED HEREIN.