10 kHz to 10 GHz, Wideband, Low Noise Amplifier

FEATURES

- Single positive supply (self biased)
- Resistor-programmable bias setting
- Positive gain slope vs. frequency
- Wideband operation: 10 kHz to 10 GHz
- Extended operating temperature range: −55°C to +125°C
- RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Telecommunications
- Instrumentation
- Radar
- Electronic warfare

GENERAL DESCRIPTION

The ADL8122 is a wideband low noise amplifier (LNA) that operates from 10 kHz to 10 GHz. Typical gain and noise figure are 17 dB and 2 dB, respectively, from 2 GHz to 6 GHz. Output power for 1 dB compression (OP1dB), output third-order intercept (OIP3), and output second-order intercept (OIP2) are 20 dBm, 33.5 dBm, and 37 dBm, respectively, from 2 GHz to 6 GHz. The nominal quiescent current (I_{DQ}), which can be adjusted, is 95 mA from a 5 V supply voltage (V_{DD}). The internally matched, DC-coupled RF input and output pins require external AC coupling capacitors along with a bias inductor on RFOUT. In addition, the RF input is biased through an external inductor connected between the VBIAS pin and the RFIN pin.

The ADL8122 is fabricated on a pseudomorphic, high electron mobility transistor (pHEMT) process. The device is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP and is specified for operation from −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

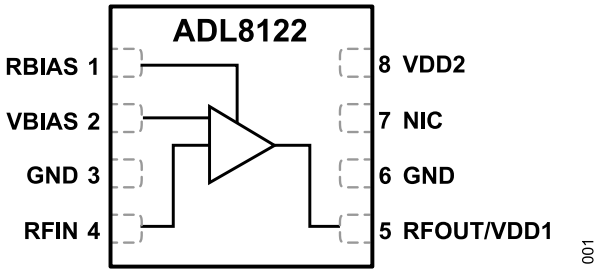


Figure 1. Functional Block Diagram

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REVISION HISTORY

10/2026—Rev. 0 to Rev. A

Changes to Figure 35 and Figure 36 ... 11
Changes to Figure 40 ... 12

6/2024—Revision 0: Initial Version

SPECIFICATIONS

10 KHZ TO 2 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 95 mA, bias resistance (R_{BIAS}) = 620 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 10 kHz to 2 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.00001		2	GHz	Refer to the Low Frequency Bias Tee section for the parameter coverage and operation down to 10 kHz range
GAIN		16		dB	
Gain Variation over Temperature		0.053		dB/°C	
NOISE FIGURE		1.7		dB	
RETURN LOSS					
Input (S11)		14.5		dB	
Output (S22)		12.5		dB	
OUTPUT					
OP1dB	18	20.5		dBm	
Saturated Power (P_{SAT})		22.5		dBm	
OIP3		35		dBm	Measurement taken at output power (P_{OUT}) per tone = 5 dBm
OIP2		43.5		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
POWER ADDED EFFICIENCY (PAE)		26.5		%	Measured at P_{SAT}

2 GHZ TO 6 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 2 GHz to 6 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2		6	GHz	
GAIN	15	17		dB	
Gain Variation over Temperature		0.006		dB/°C	
NOISE FIGURE		2		dB	
RETURN LOSS					
S11		17		dB	
S22		13		dB	
OUTPUT					
OP1dB	17.5	20		dBm	
P_{SAT}		22		dBm	
OIP3		33.5		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
OIP2		37		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
PAE		26		%	Measured at P_{SAT}

SPECIFICATIONS

6 GHZ TO 10 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 6 GHz to 10 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	6		10	GHz	
GAIN	15	17.5		dB	
Gain Variation over Temperature		0.022		dB/°C	
NOISE FIGURE		2.5		dB	
RETURN LOSS					
S11		14		dB	
S22		15		dB	
OUTPUT					
OP1dB		17		dBm	
P_{SAT}		19		dBm	
OIP3		31.5		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
OIP2		48		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
PAE		16.5		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 4. DC Specifications

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		95		mA
Amplifier Current (I_{DQ_AMP})		90		mA
RBIAS Current (I_{RBIAS})		5		mA
SUPPLY VOLTAGE				
V_{DD}	3	5	6	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	7 V
RF Input Power (RFIN)	See Figure 2
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 13.7 mW/°C Above 85°C)	1.23 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Quiescent Channel (T_{CASE} = 85°C, V_{DD} = 5 V, I_{DQ} = 95 mA, Input Power (P_{IN}) = Off)	119.7°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

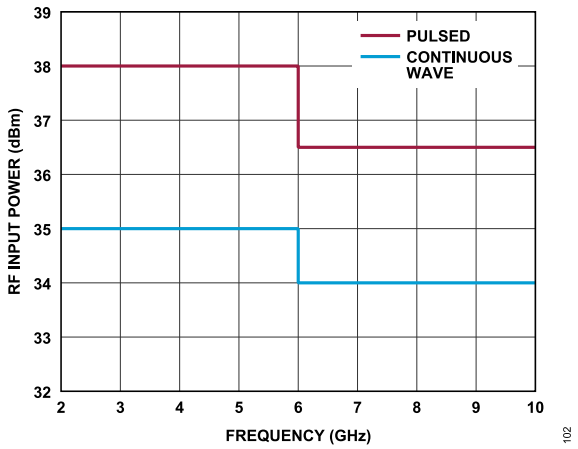


Figure 2. RF Input Power Absolute Maximum Ratings for Pulsed and Continuous Wave vs. Frequency, T_{CASE} = 85°C

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance.

Table 6. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{CASE} = 25°C	61.8	°C/W
Worst Case[2], T_{CASE} = 85°C	73	°C/W

1 Thermal resistance varies with operating conditions.

2 Across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8122

Table 7. ADL8122, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±350	1A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

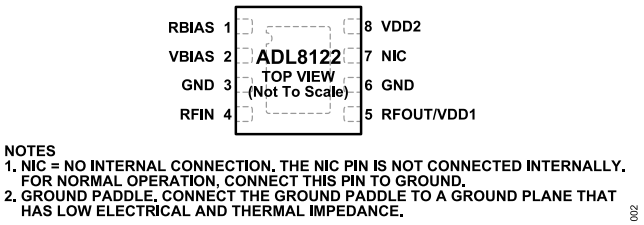


Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDDx to set I_{DQ}. See Figure 94 and Table 9 for more details. See Figure 4 for the interface schematic.
2	VBIAS	Bias Setting Voltage Output. VBIAS sets the bias voltage for the RFIN pin. Connect VBIAS to RFIN using an inductor or ferrite bead as shown in Figure 94. See Figure 5 for the interface schematic.
3, 6	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 6 for the interface schematic.
4	RFIN	RF Input. The RFIN pin is DC-coupled and matched to 50 Ω. See Figure 7 for the interface schematic.
5	RFOUT/VDD1	RF Output and Drain Bias Voltage. The RF output is DC-coupled and also serves as the drain biasing node. For the drain bias voltage, connect a DC bias network to provide the drain current and AC-couple the RF output path. See Figure 8 for the interface schematic.
7	NIC	No Internal Connection. The NIC pin is not connected internally. For normal operation, connect this pin to ground.
8	VDD2	Drain Bias. Connect the VDD2 pin to a common supply with VDD1. See Figure 9 for the interface schematic.
	GROUND PADDLE	Ground Paddle. Connect the ground paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

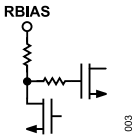


Figure 4. RBIAS Interface Schematic

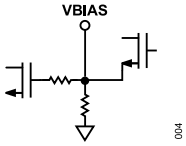


Figure 5. VBIAS Interface Schematic



Figure 6. GND Interface Schematic

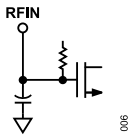


Figure 7. RFIN Interface Schematic

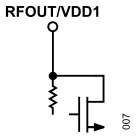


Figure 8. RFOUT/VDD1 Interface Schematic



Figure 9. VDD2 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

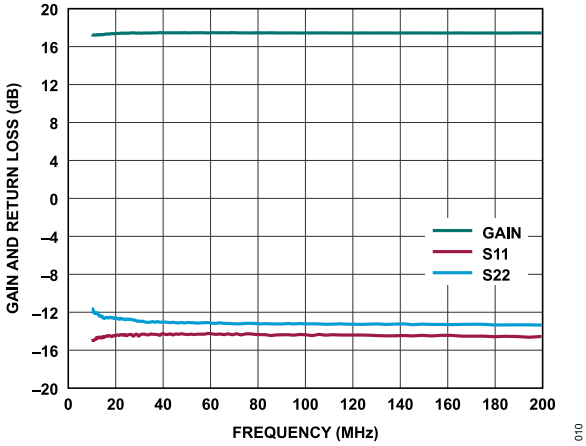


Figure 10. Gain and Return Loss vs. Frequency, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

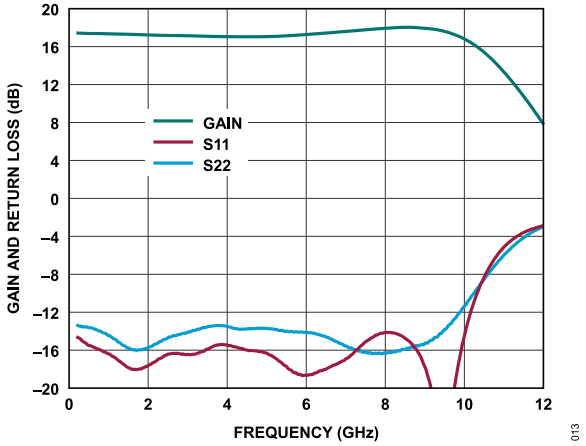


Figure 13. Gain and Return Loss vs. Frequency, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

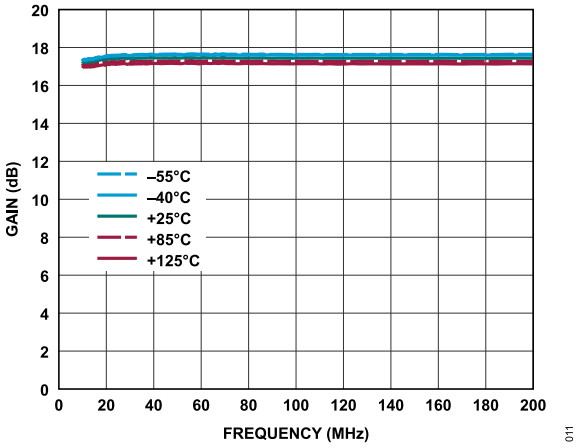


Figure 11. Gain vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

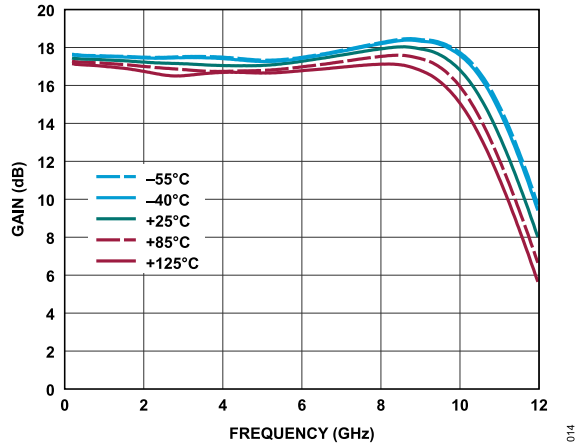


Figure 14. Gain vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

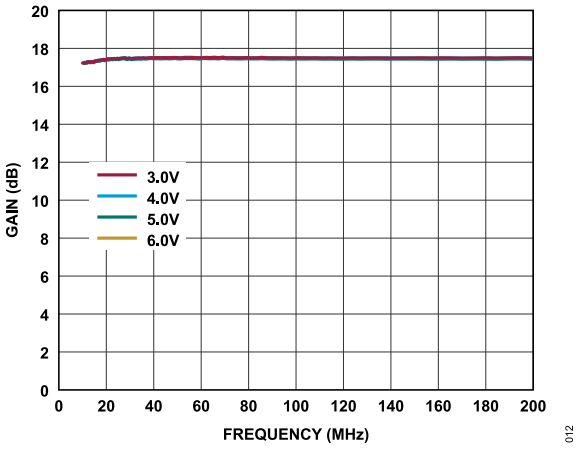


Figure 12. Gain vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

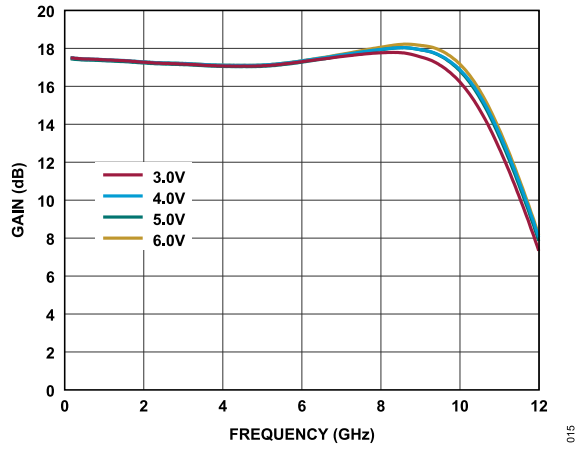


Figure 15. Gain vs. Frequency for Various Supply Voltages 200 MHz to 12 GHz, I_{DQ} = 95 mA

TYPICAL PERFORMANCE CHARACTERISTICS

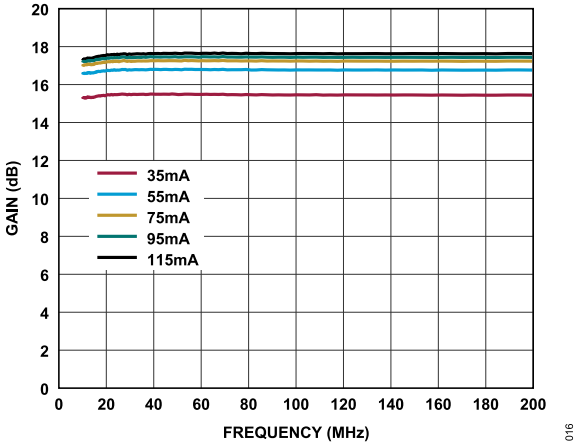


Figure 16. Gain vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

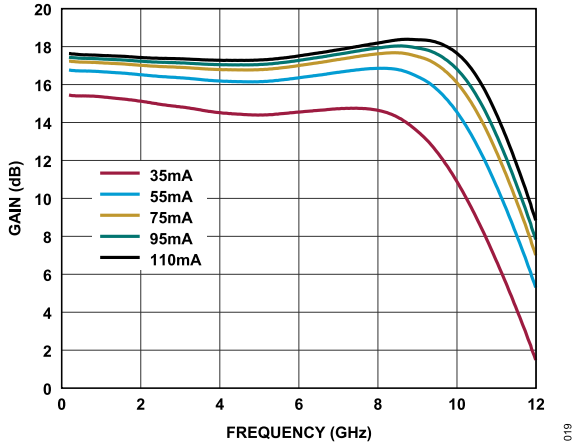


Figure 19. Gain vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

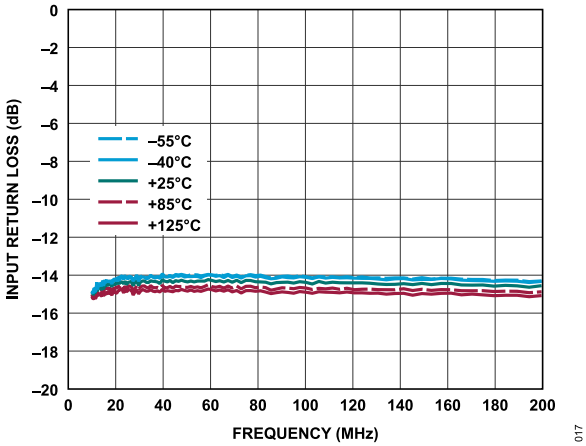


Figure 17. Input Return Loss vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

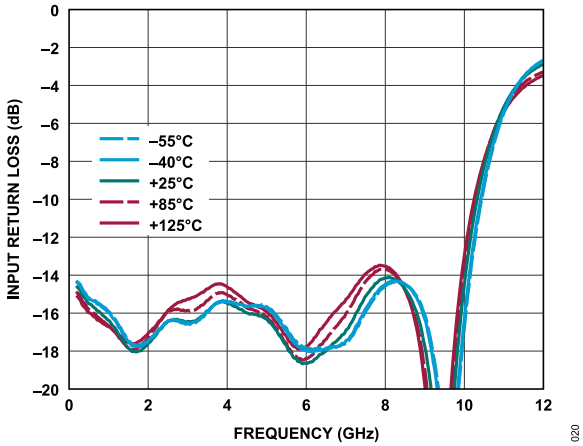


Figure 20. Input Return Loss vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

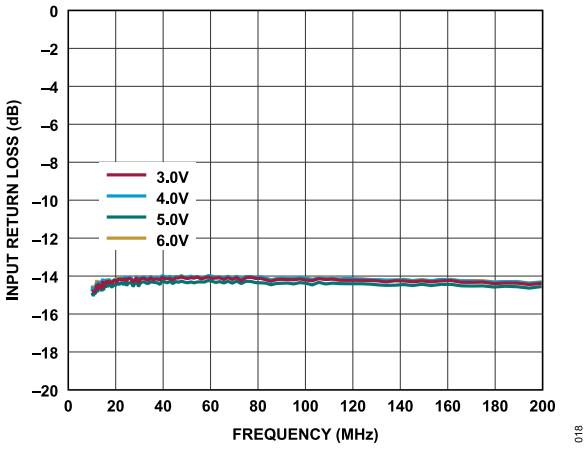


Figure 18. Input Return Loss vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

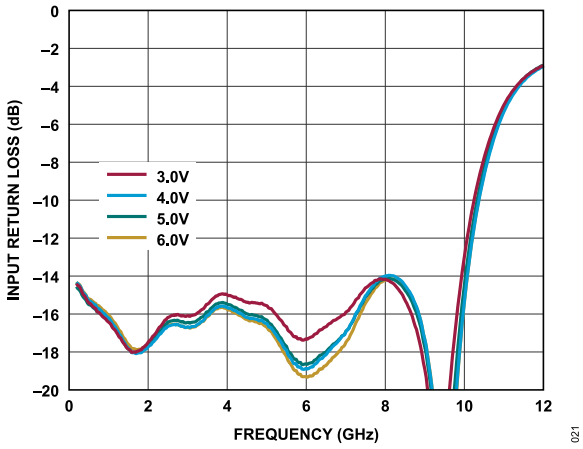


Figure 21. Input Return Loss vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

TYPICAL PERFORMANCE CHARACTERISTICS

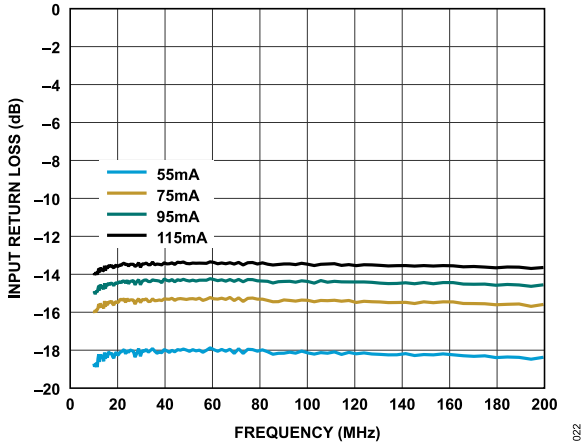


Figure 22. Input Return Loss vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

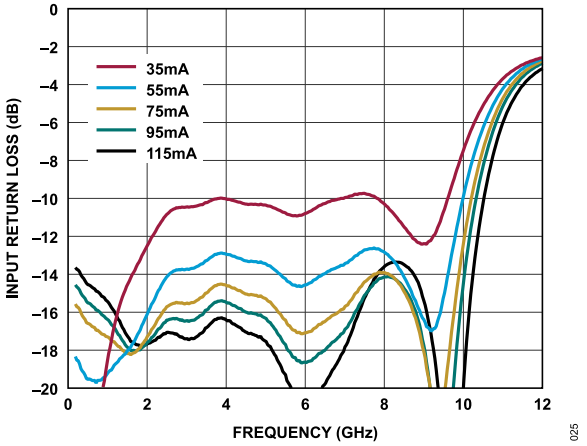


Figure 25. Input Return Loss vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

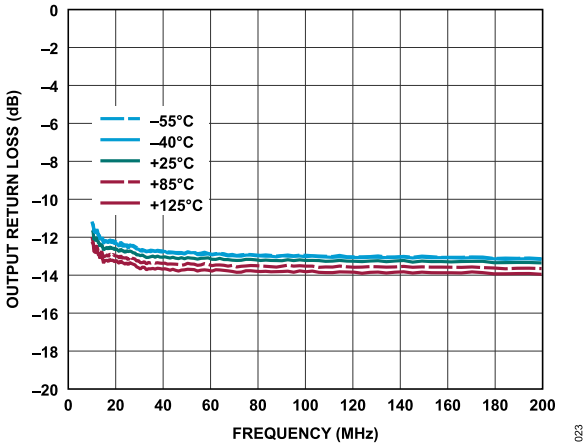


Figure 23. Output Return Loss vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

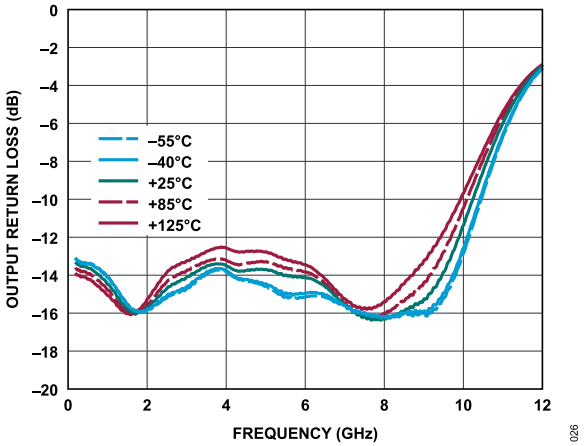


Figure 26. Output Return Loss vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

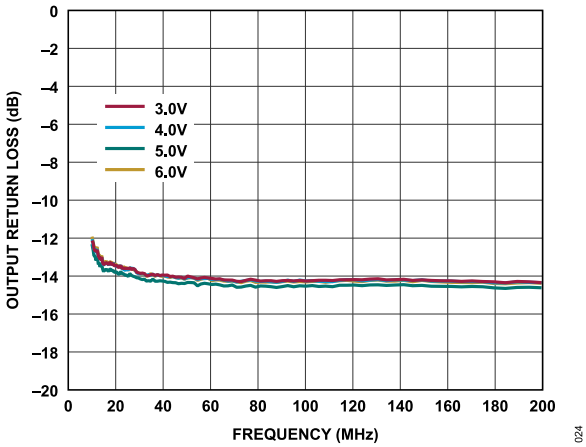


Figure 24. Output Return Loss vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

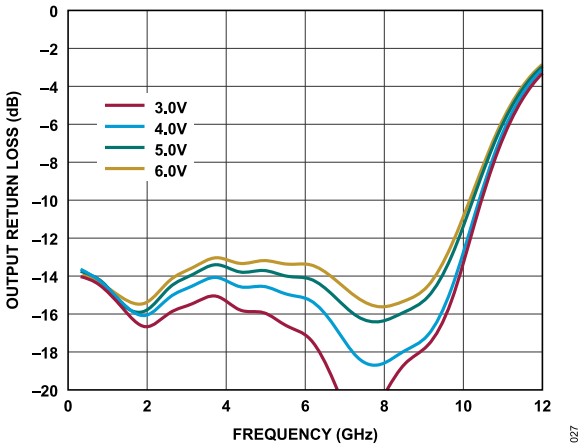


Figure 27. Output Return Loss vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

TYPICAL PERFORMANCE CHARACTERISTICS

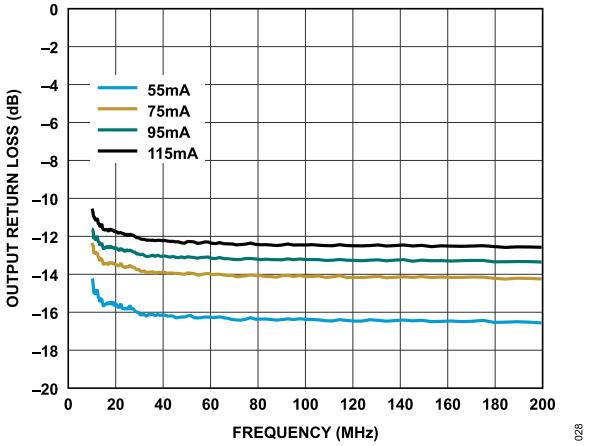


Figure 28. Output Return Loss vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

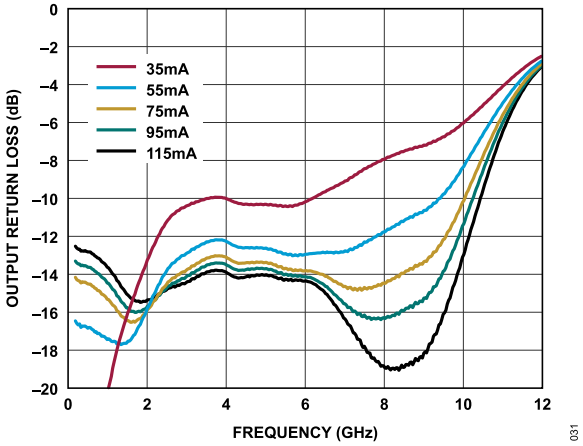


Figure 31. Output Return Loss vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

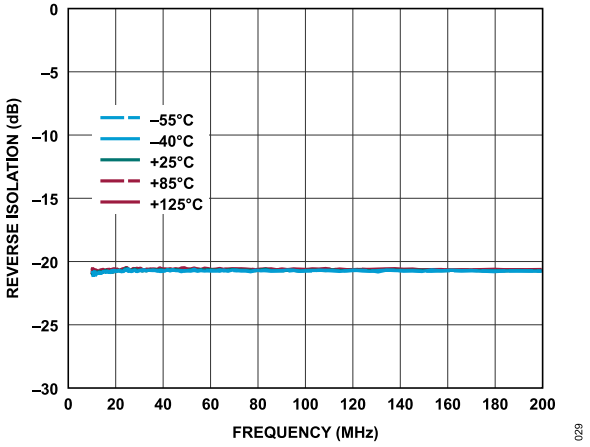


Figure 29. Reverse Isolation vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

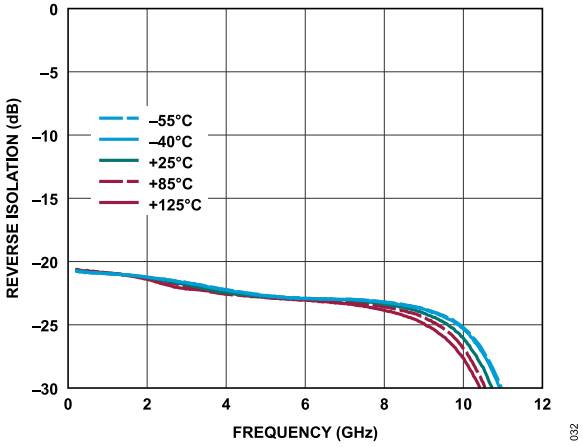


Figure 32. Reverse Isolation vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

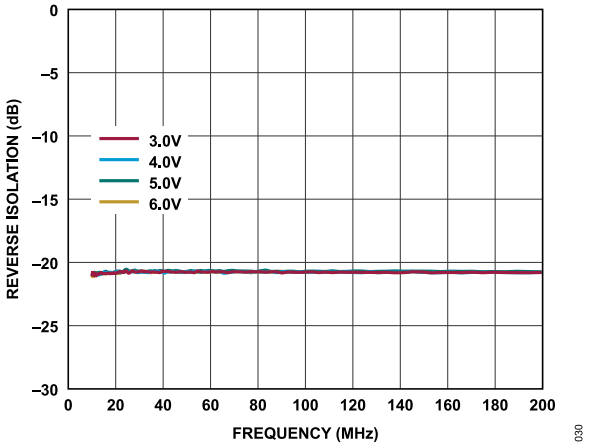


Figure 30. Reverse Isolation vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

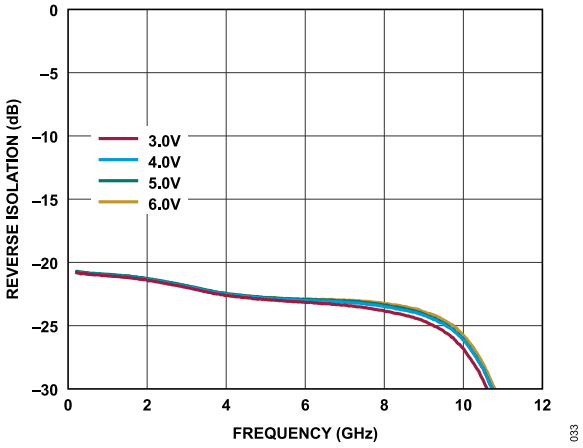


Figure 33. Reverse Isolation vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

TYPICAL PERFORMANCE CHARACTERISTICS

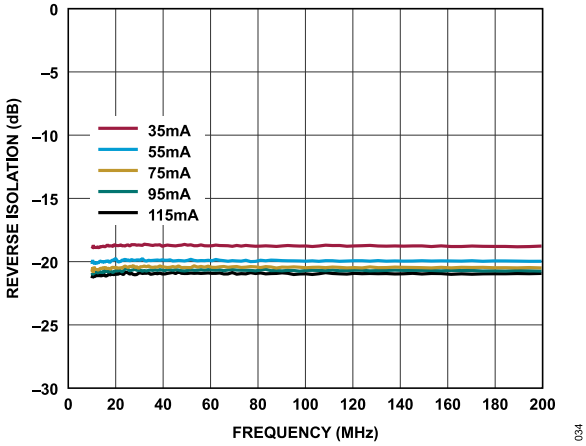


Figure 34. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

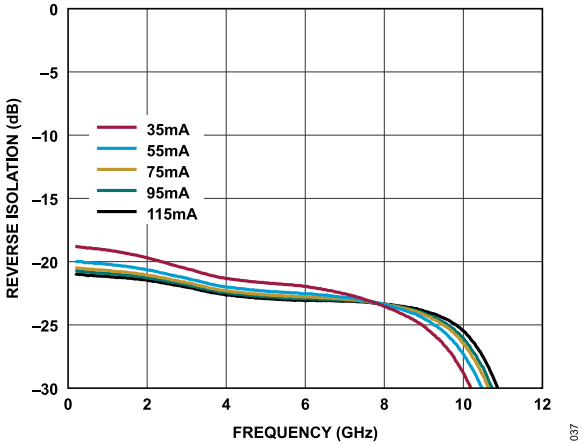


Figure 37. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

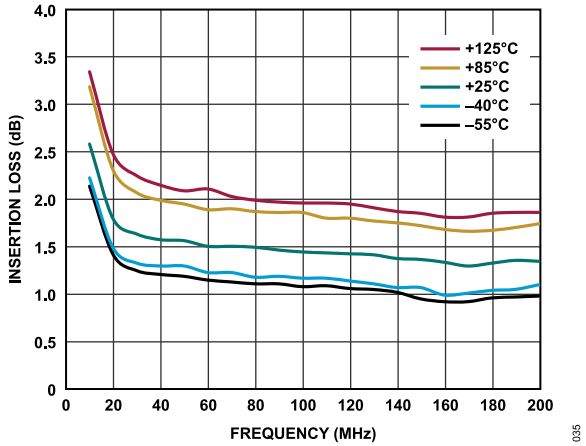


Figure 35. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

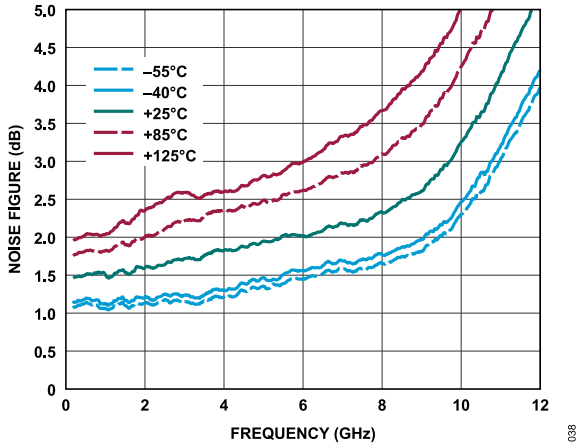


Figure 38. Noise Figure vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

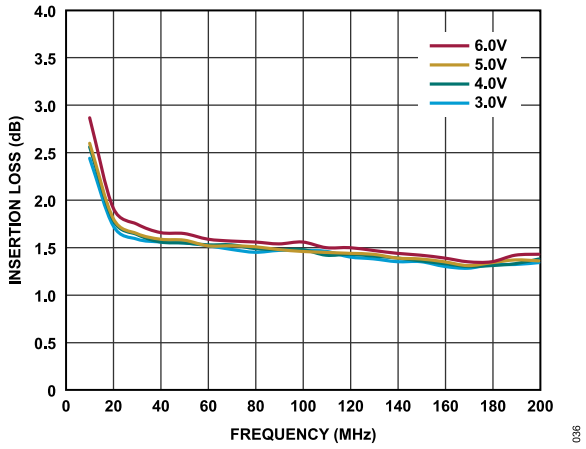


Figure 36. Noise Figure vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

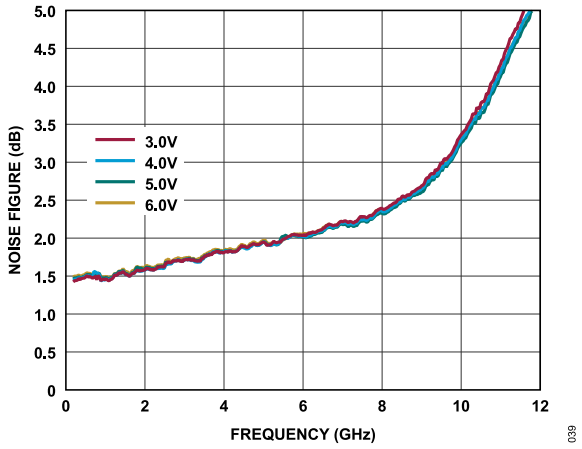


Figure 39. Noise Figure vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

TYPICAL PERFORMANCE CHARACTERISTICS

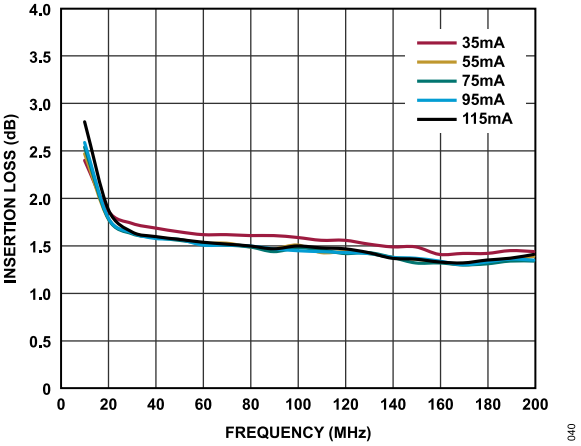


Figure 40. Noise Figure vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

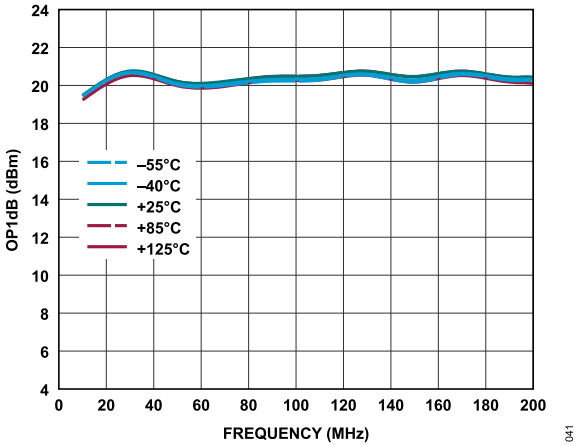


Figure 41. OP1dB vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

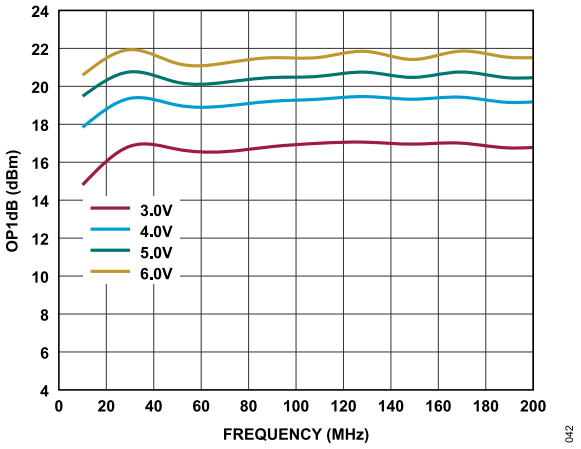


Figure 42. OP1dB vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

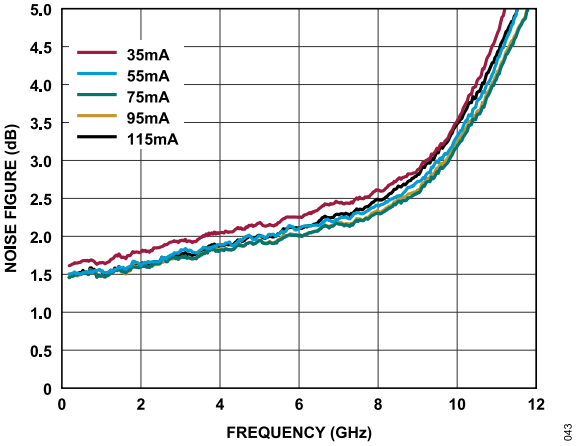


Figure 43. Noise Figure vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

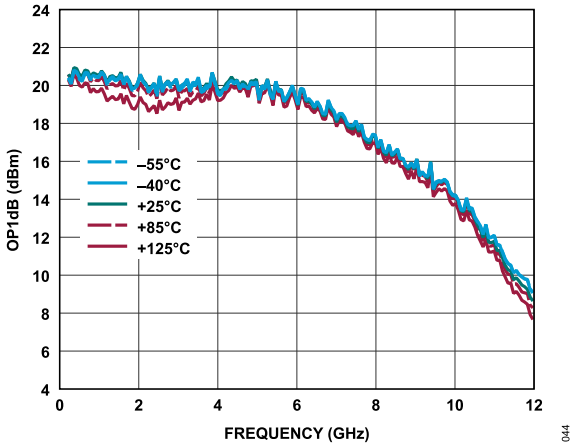


Figure 44. OP1dB vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

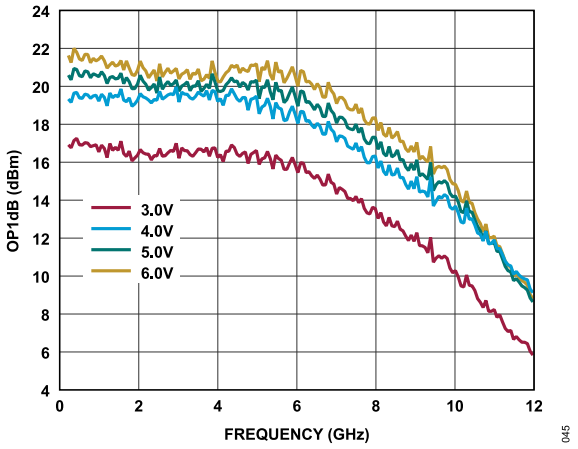


Figure 45. OP1dB vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

TYPICAL PERFORMANCE CHARACTERISTICS

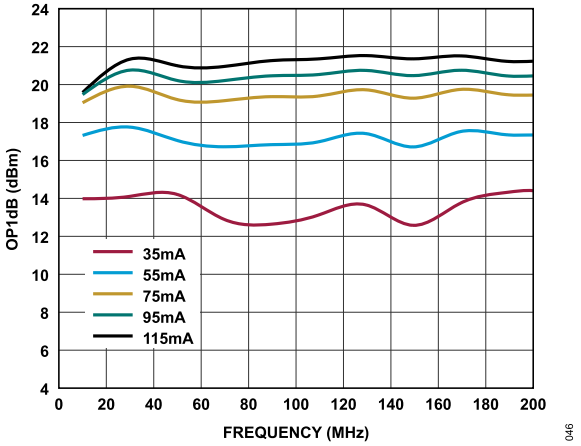


Figure 46. OP1dB vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

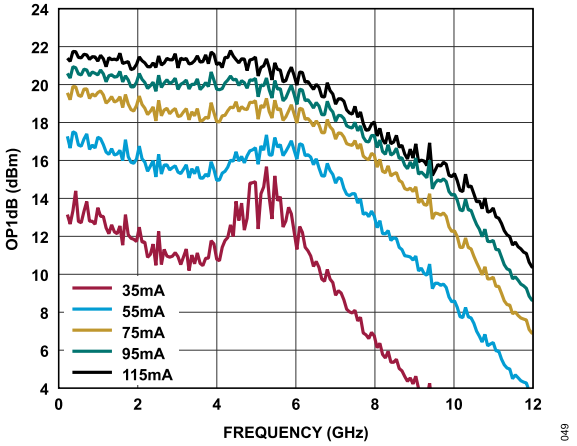


Figure 49. OP1dB vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

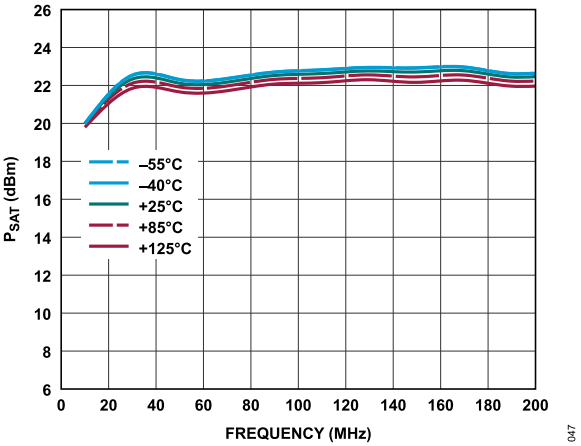


Figure 47. P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

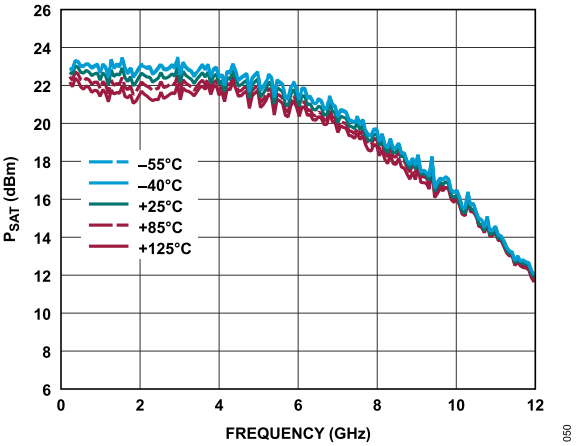


Figure 50. P_{SAT} vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

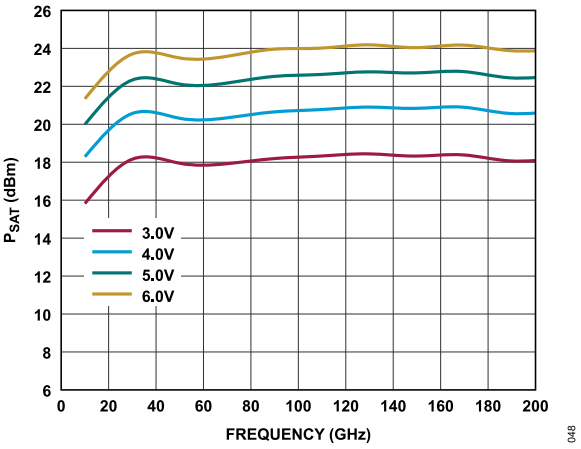


Figure 48. P_{SAT} vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

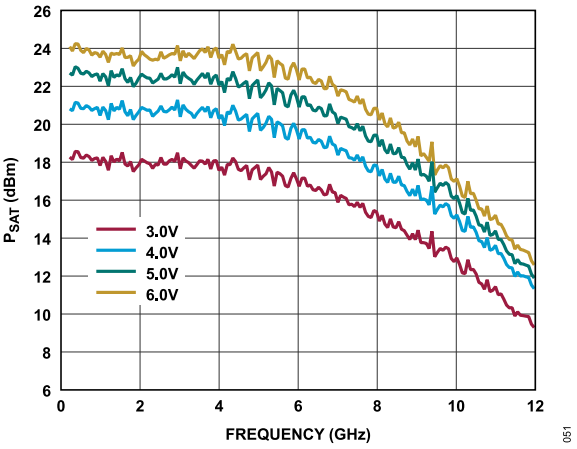


Figure 51. P_{SAT} vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

TYPICAL PERFORMANCE CHARACTERISTICS

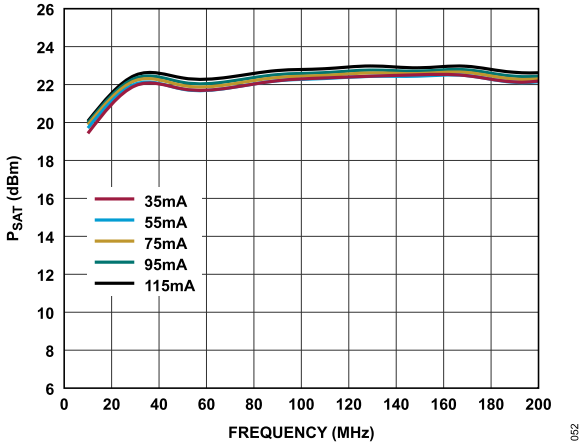


Figure 52. P_{SAT} vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

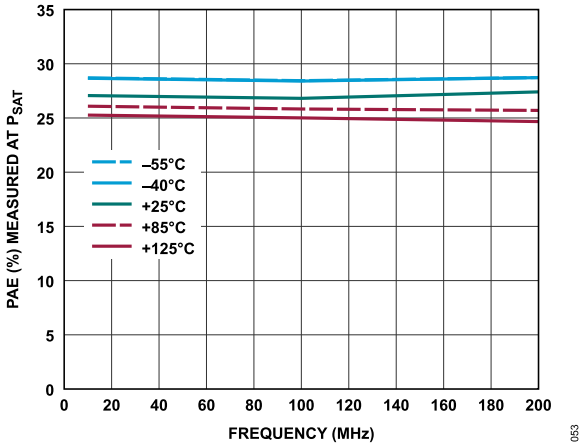


Figure 53. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

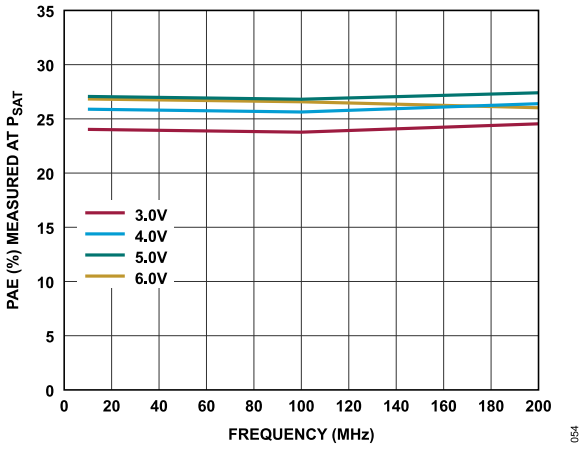


Figure 54. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

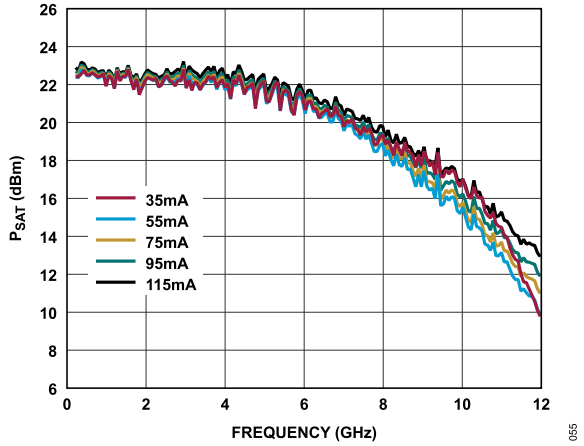


Figure 55. P_{SAT} vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

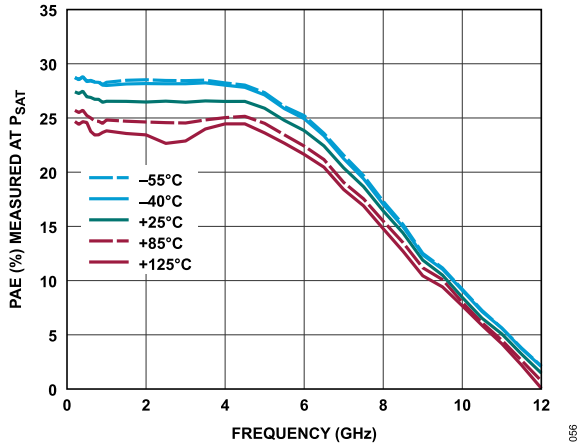


Figure 56. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

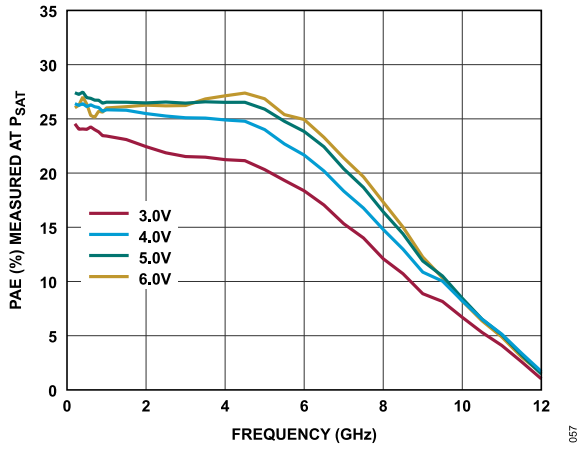


Figure 57. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

TYPICAL PERFORMANCE CHARACTERISTICS

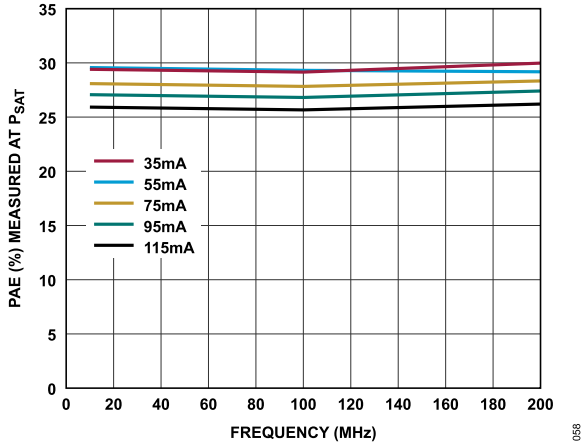


Figure 58. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

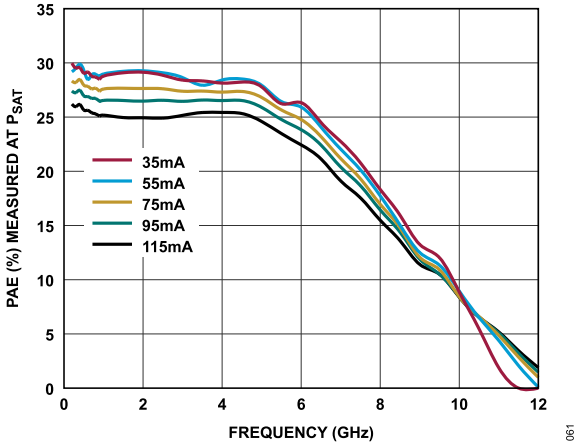


Figure 61. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

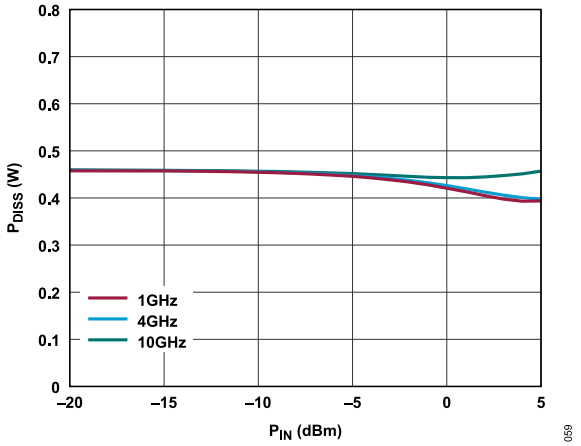


Figure 59. P_{DISS} vs. P_{IN} at Various Frequencies, T_{CASE} = 85°C, V_{DD} = 5 V

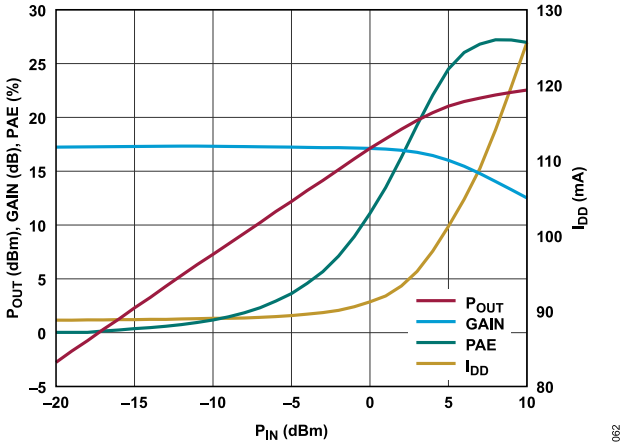


Figure 62. P_{OUT}, GAIN, PAE, and I_{DD} vs. P_{IN}, Power Compression at 1 GHz, V_{DD} = 5 V, R_{BIAS} = 620 Ω

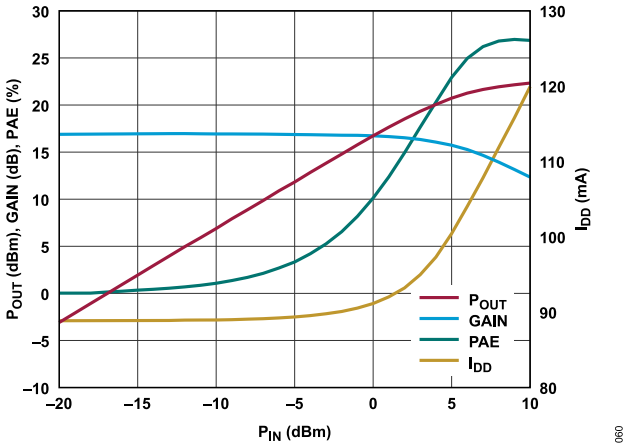


Figure 60. P_{OUT}, GAIN, PAE, and I_{DD} vs. P_{IN}, Power Compression at 4 GHz, V_{DD} = 5 V, R_{BIAS} = 620 Ω

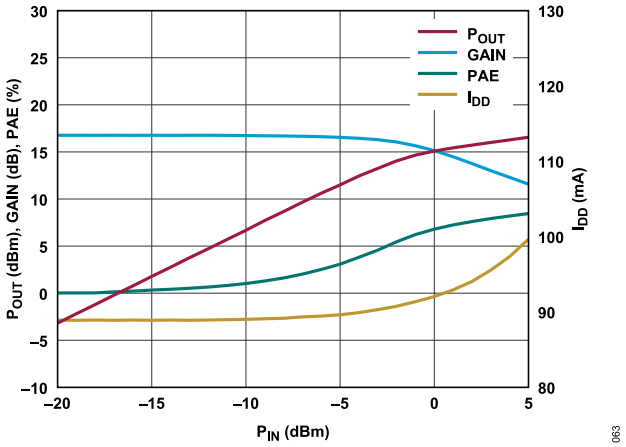


Figure 63. P_{OUT}, GAIN, PAE, and I_{DD} vs. P_{IN}, Power Compression at 10 GHz, V_{DD} = 5 V, R_{BIAS} = 620 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

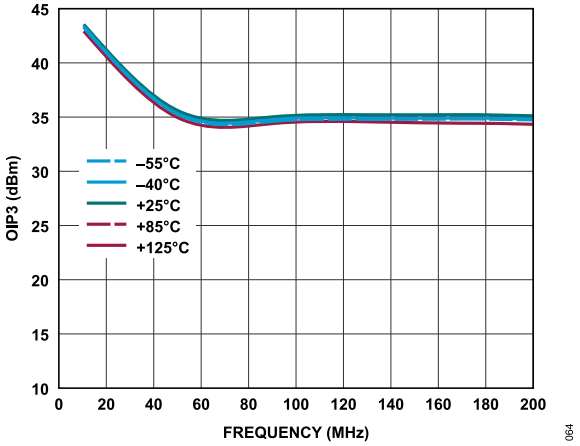


Figure 64. OIP3 vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

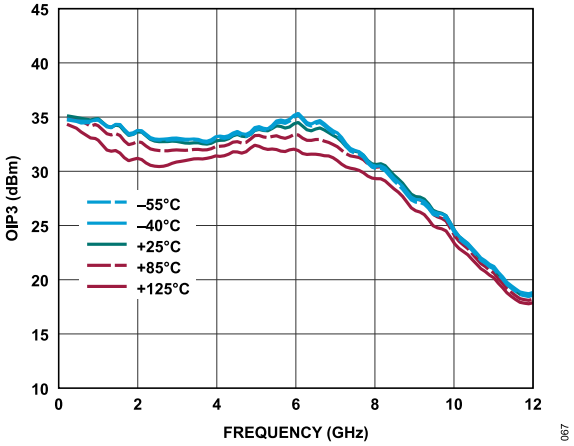


Figure 67. OIP3 vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

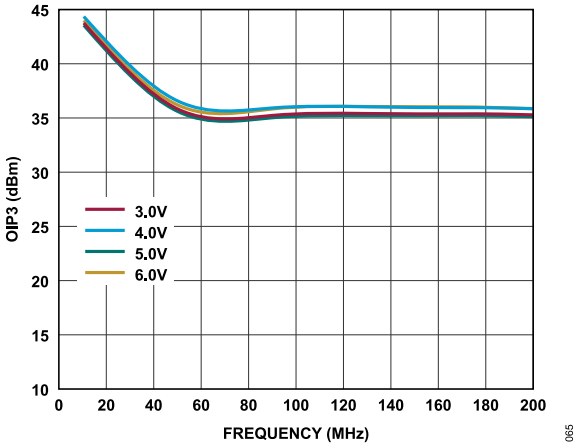


Figure 65. OIP3 vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

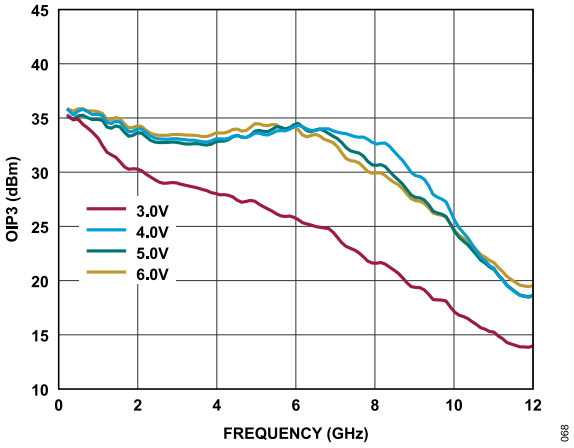


Figure 68. OIP3 vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

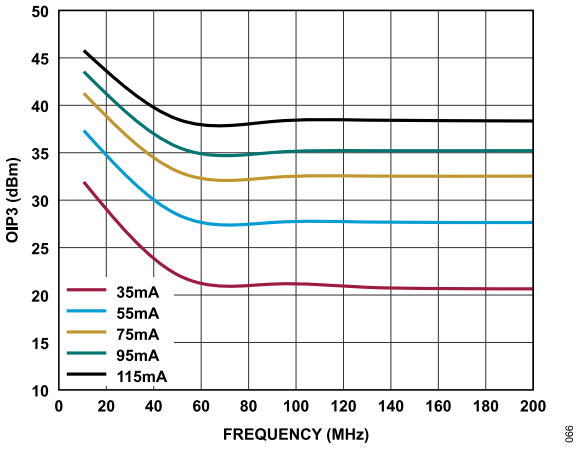


Figure 66. OIP3 vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

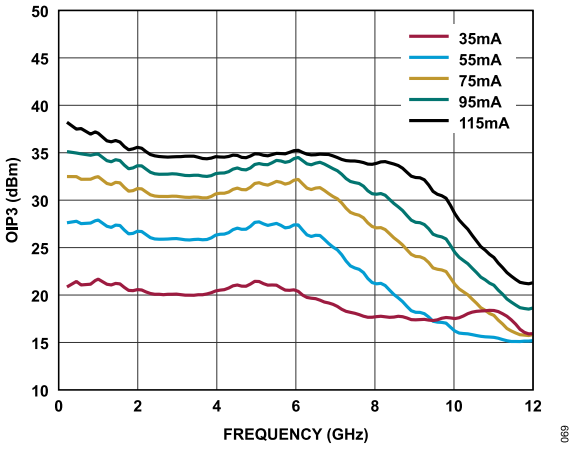


Figure 69. OIP3 vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

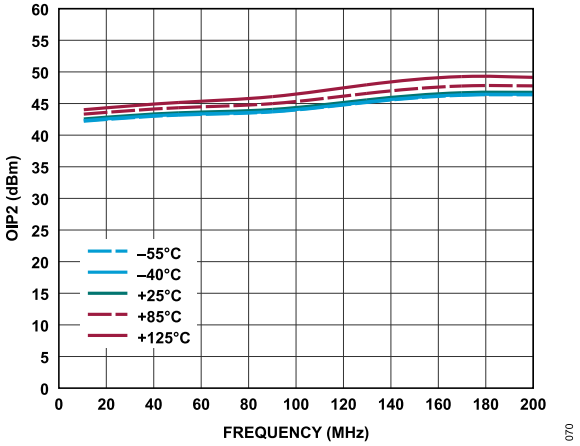


Figure 70. OIP2 vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

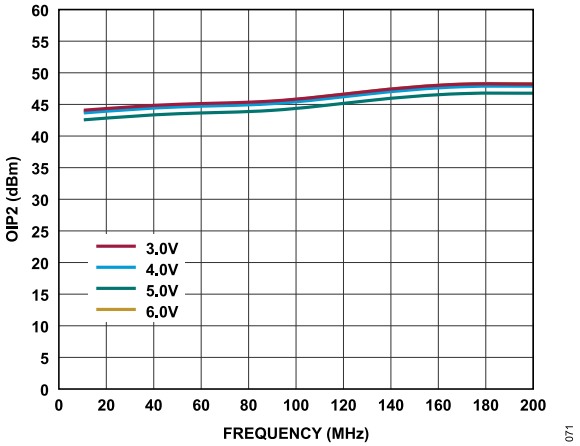


Figure 71. OIP2 vs. Frequency for Various Supply Voltages, 10 MHz to 200 MHz, I_{DQ} = 95 mA

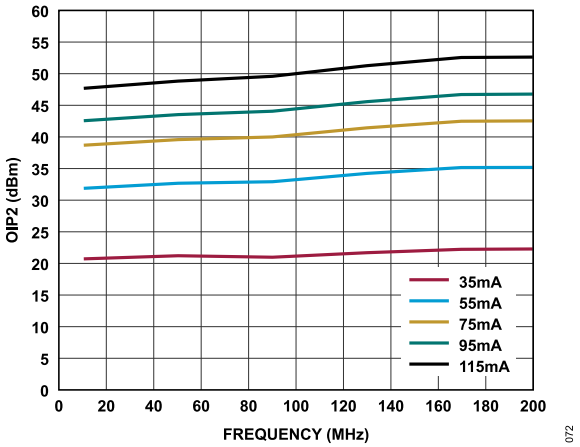


Figure 72. OIP2 vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

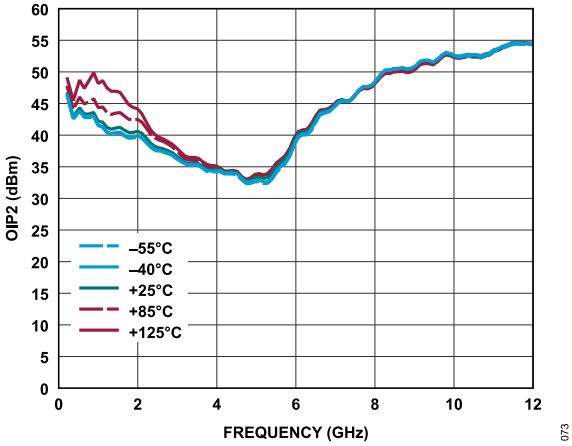


Figure 73. OIP2 vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

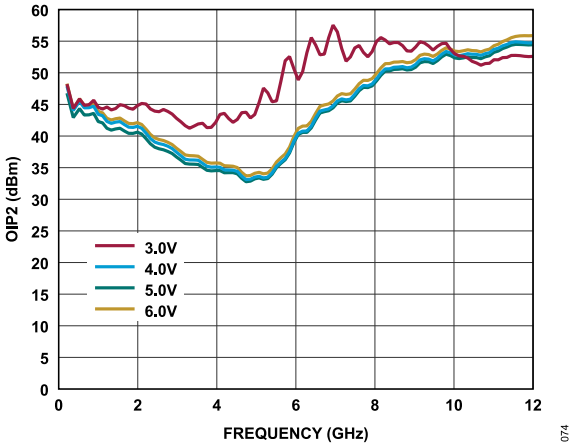


Figure 74. OIP2 vs. Frequency for Various Supply Voltages, 200 MHz to 12 GHz, I_{DQ} = 95 mA

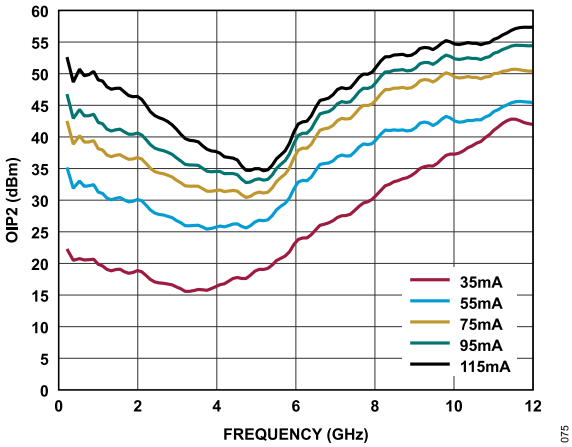


Figure 75. OIP2 vs. Frequency for Various I_{DQ} Values, 200 MHz to 12 GHz, V_{DD} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

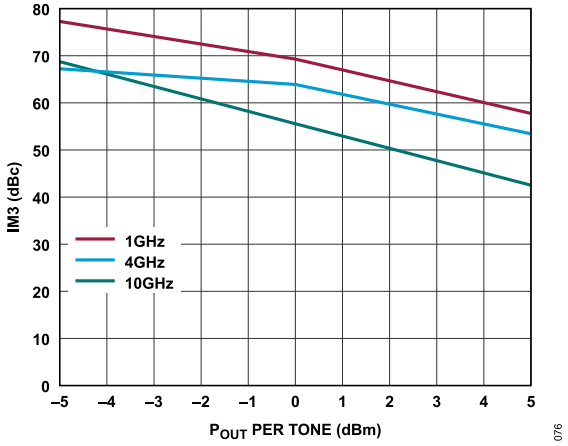


Figure 76. Third-Order Intermodulation Distortion (IM3) vs P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V, R_{BIAS} = 620 Ω

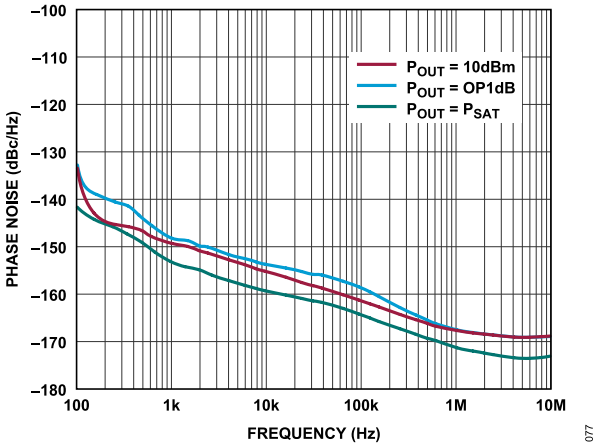


Figure 77. Phase Noise vs. Frequency at 5 GHz for Various P_{OUT} Values

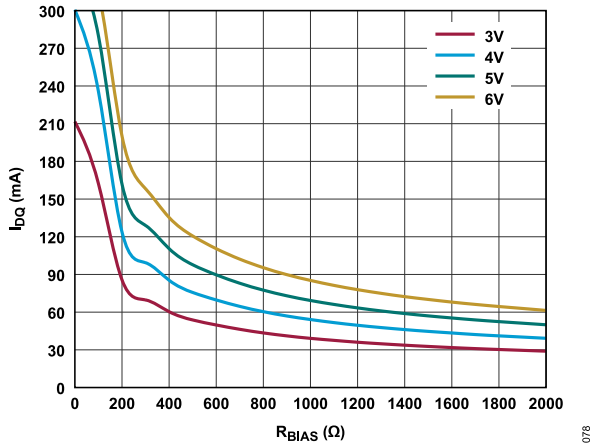


Figure 78. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0 Ω to 2000 Ω

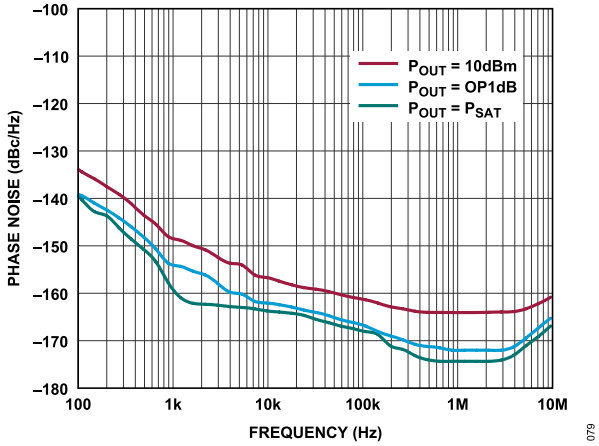


Figure 79. Phase Noise vs. Frequency at 2 GHz for Various P_{OUT} Values

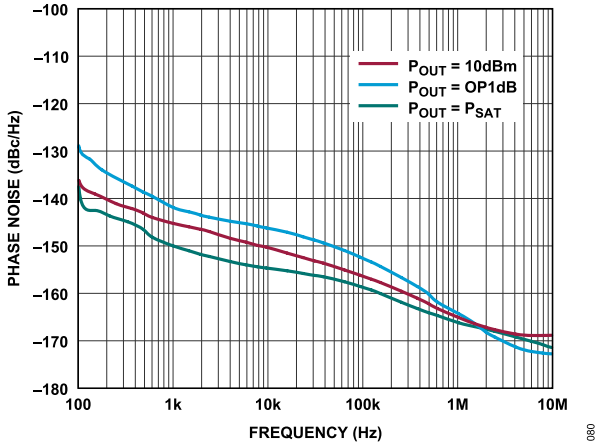


Figure 80. Phase Noise vs. Frequency at 8 GHz for Various P_{OUT} Values

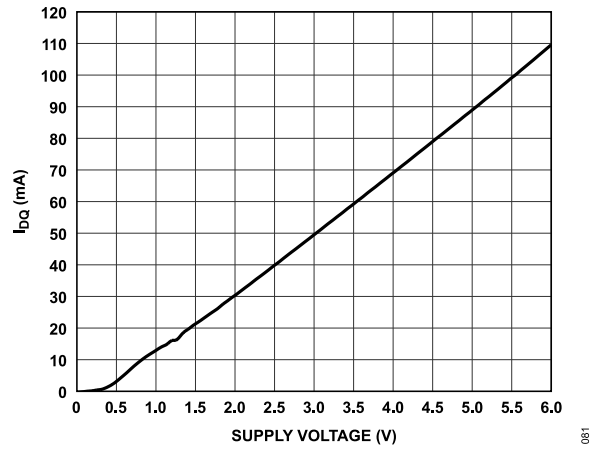


Figure 81. I_{DQ} vs. Supply Voltage, R_{BIAS} = 620 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

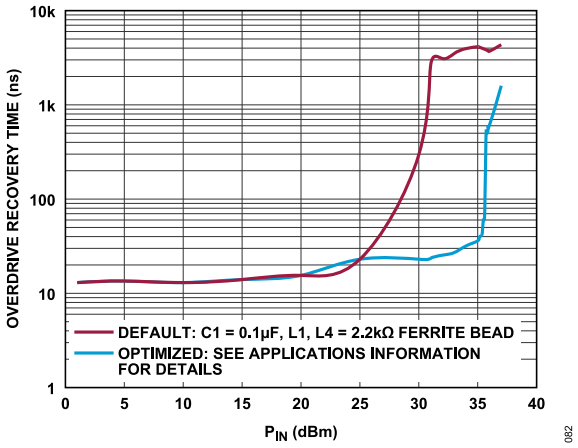


Figure 82. Overdrive Recovery Time vs. P_{IN} at 6 GHz, Recovery Time to Within 90% of Small Signal Gain Value, V_{DD} = 5 V, R_{BIAS} = 620 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

LOW FREQUENCY BIAS TEE

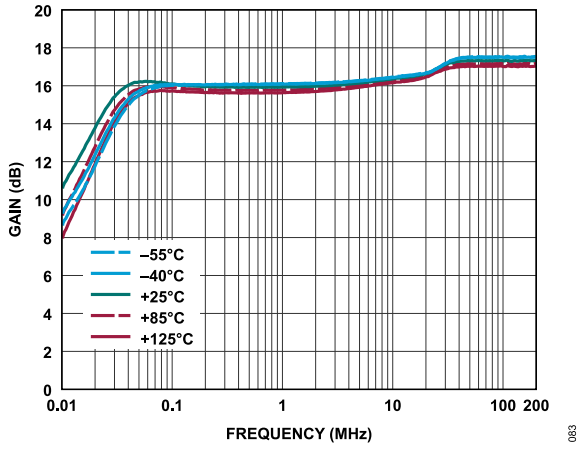


Figure 83. Gain vs. Frequency for Various Temperatures, 10 kHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

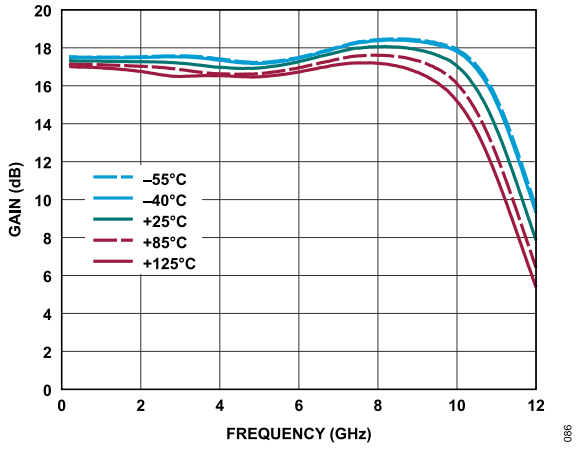


Figure 86. Gain vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

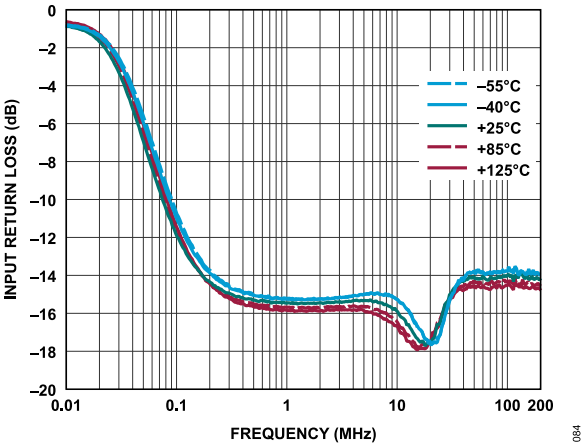


Figure 84. Input Return Loss vs. Frequency for Various Temperatures, 10 kHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

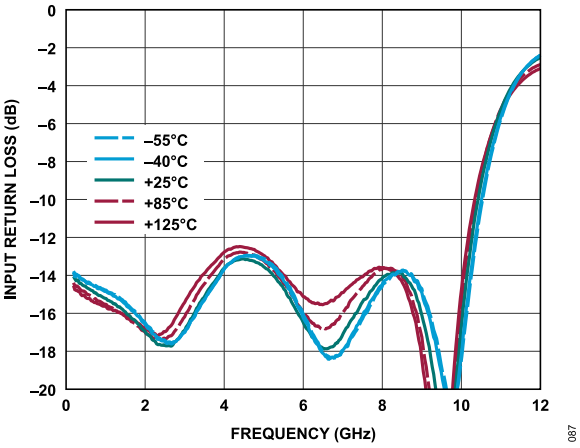


Figure 87. Input Return Loss vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

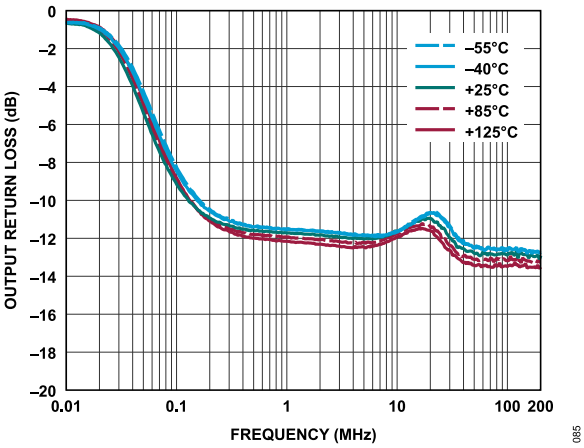


Figure 85. Output Return Loss vs. Frequency for Various Temperatures, 10 kHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

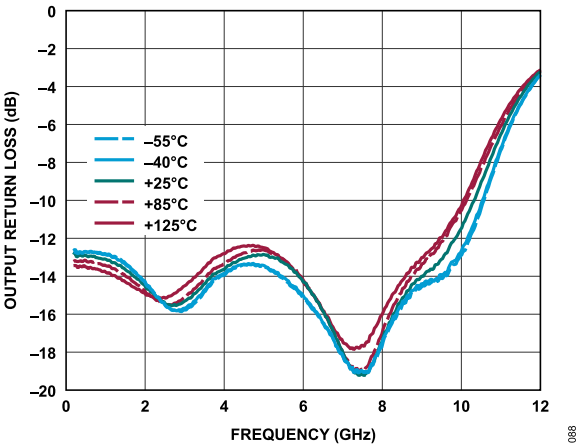


Figure 88. Output Return Loss vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

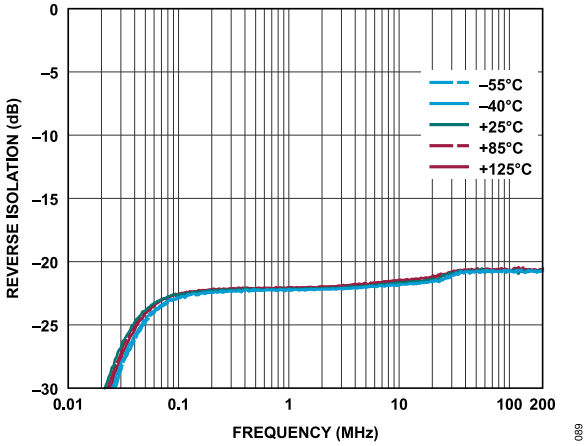


Figure 89. Reverse Isolation vs. Frequency for Various Temperatures, 10 kHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

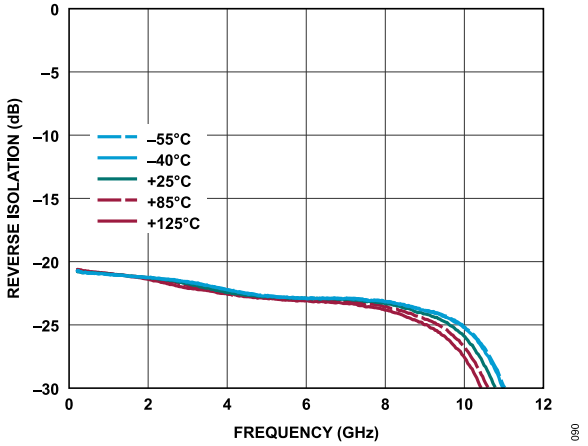


Figure 90. Reverse Isolation vs. Frequency for Various Temperatures, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

THEORY OF OPERATION

The ADL8122 is a wideband LNA that operates from 10 kHz to 10 GHz. A simplified block diagram is shown in Figure 91.

The ADL8122 has DC-coupled, single-ended input and output ports with impedance that is nominally equal to 50 Ω over the specified frequency range. No external matching components are required; other than, AC input and output coupling capacitors and a bias inductor. To adjust I_{DQ}, connect an external resistor between the RBIAS and VDDx pins. The VBIAS output voltage provides a DC bias voltage; it connects to RFIN through a ferrite bead. The RFOUT/VDD1 pin provides the drain current. Additional drain biasing is applied through the VDD2 pin.

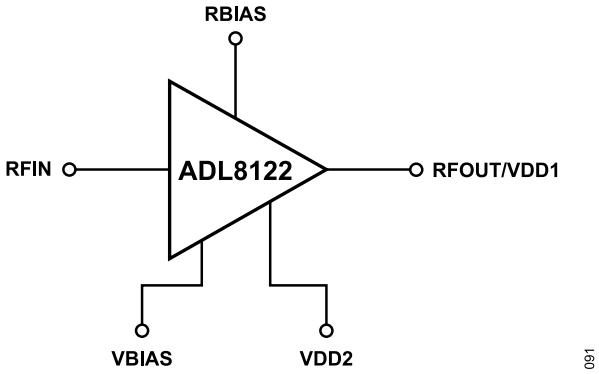


Figure 91. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8122 from 10 MHz to 10 GHz are shown in Figure 94. AC-couple the input and output of the ADL8122 with appropriately sized capacitors (such as American Technical Ceramics Part Number 560L104YTRN). Connect a ferrite bead between the VBIAS pin and the RFIN pin to provide a DC bias voltage to the RF input. A 5 V DC bias is provided to the amplifier using two ferrite beads connected to the RFOUT/VDD1 pin. The recommended bias inductor is a TDK Corporation MMZ1005A222ET000 2.2 kΩ at 100 MHz.

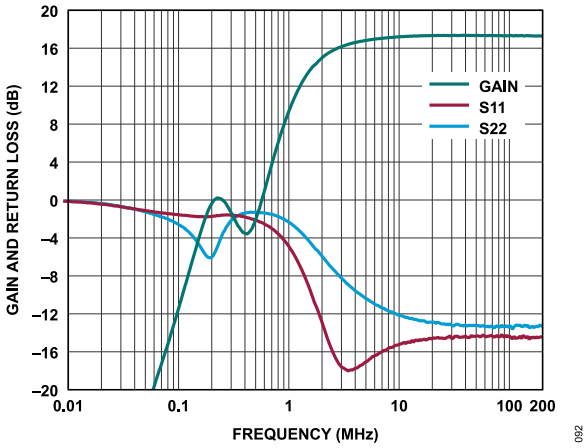


Figure 92. Gain and Return Loss vs. Frequency of 10 MHz to 12 GHz Application Circuit, 10 kHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

The 5 V DC bias voltage must also be connected to the VDD2 pin. The bias conditions, V_{DD} = 5 V and I_{DQ} = 95 mA, are the recommended operating point to achieve specified performance. The gain and return loss of this circuit are shown in Figure 92 and Figure 93 across frequencies. To set other bias conditions, adjust the R_{BIAS} value. Table 9 shows the recommended R_{BIAS} values and their associated I_{DQ} values.

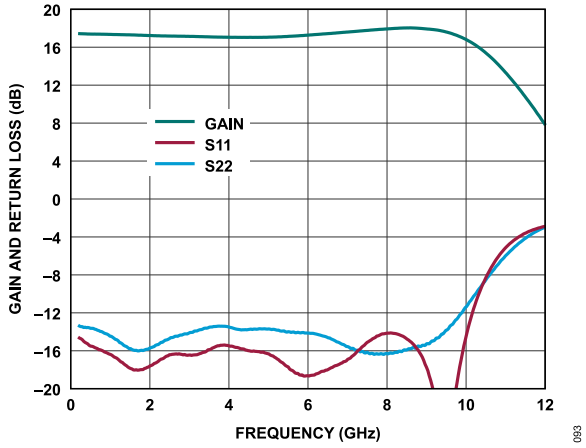


Figure 93. Gain and Return Loss vs. Frequency of 10 MHz to 12 GHz Application Circuit, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

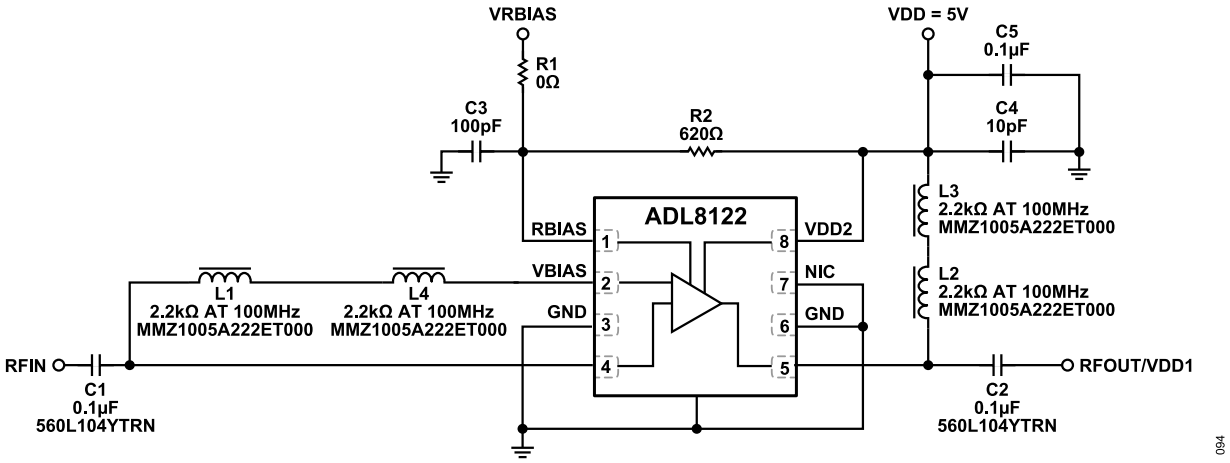


Figure 94. Typical Application Circuit for Operation from 10 MHz to 10 GHz

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCING

The correct sequencing of the DC and RF power is required to safely operate the ADL8122. During power-up, apply V_{DD} before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before V_{DD} is powered off.

For more information on using the evaluation board, refer to the ADL8122-EVALZ user guide.

Table 9. Recommended Bias Resistor Values for Various I_{DQ} Values, V_{DD} = 5 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
8280	35	34.8	0.2
1920	55	53	2
925	75	71	4
620	95	90	5
379	115	107	8

Table 10. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 95 mA

R_{BIAS} (Ω)	V_{DD} (V)
164	3.0
340	4.0
620	5.0
811	6.0

APPLICATIONS INFORMATION

OPERATION FROM 10 KHZ TO 10 GHZ

Figure 97 shows the application circuit that was used to extend operation down to 10 kHz. Note that additional components, R2 and R3 = 300 Ω, L5 and L6 = 680 µH, C5 = 1 µF, and L4 = 2.2 kΩ at 100 MHz, have been added to support low frequency operation. The gain and the return loss of this circuit are shown in Figure 95 and Figure 96.

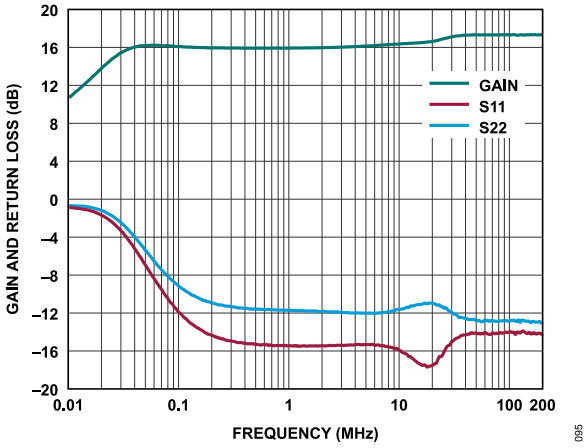


Figure 95. Gain and Return Loss vs. Frequency of 10 kHz to 10 GHz Application Circuit, 10 kHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

Further adjustments can be made to the external components of the device to operate at even lower frequencies. Specifically, the DC blocking capacitor values can be increased because these components are the limiting factor causing the low frequency cutoff.

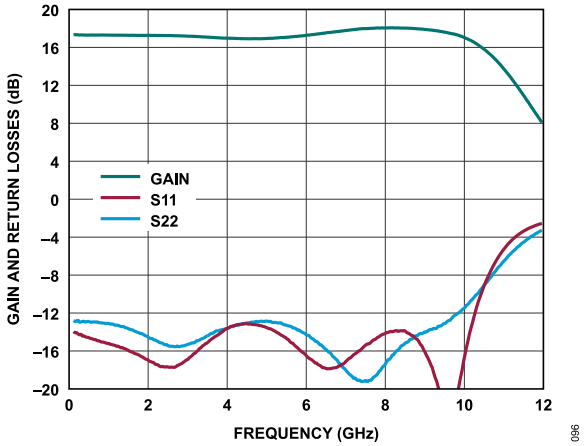


Figure 96. Gain and Return Loss vs. Frequency of 10 kHz to 10 GHz Application Circuit, 200 MHz to 12 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS} = 620 Ω

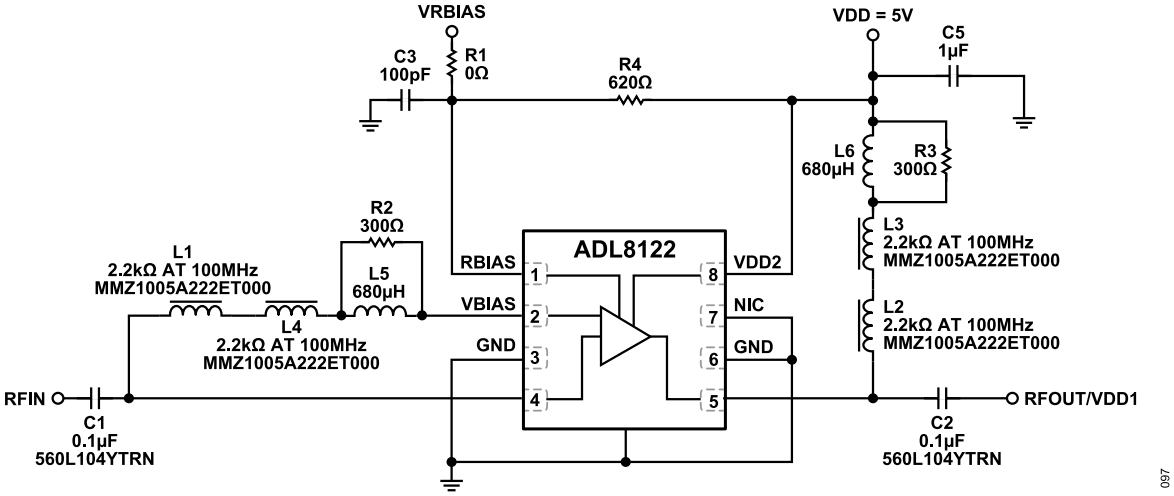


Figure 97. Typical Application Circuit for Operation from 10 kHz to 10 GHz

APPLICATIONS INFORMATION

OVERDRIVE RECOVERY OPTIMIZATION

The overdrive recovery performance of the 10 MHz to 10 GHz circuit (see Figure 94) can be improved by adjusting the C1 and L1 values shown in Figure 99. Figure 82 is the overdrive recovery time performance comparison of the baseline ADL8122-EVALZ configuration vs. the optimized ADL8122-EVALZ. The reduced value of the input DC blocking capacitor, C1, has the most impact on the improved overdrive recovery. However, by using a smaller C1 value, the minimum frequency of operation was adjusted from 10 MHz to 350 MHz. For optimum performance, the VDD2 voltage (5 V) must come from a separate supply other than V_{DD} (5 V). The bypass capacitor on VDD2 is incorporated to limit any power supply related noise from entering the device.

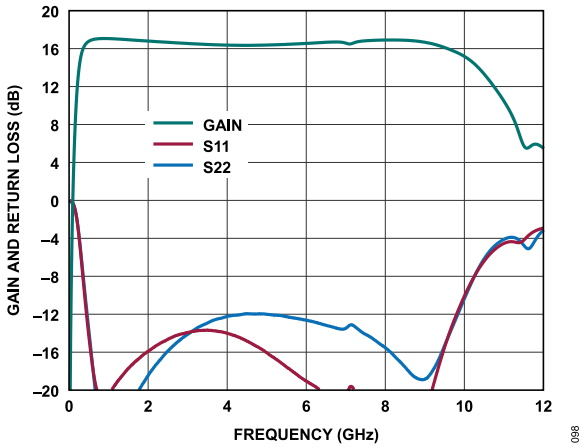


Figure 98. Gain and Return Loss vs. Frequency for ADL8122-EVALZ Overdrive Recovery Time Optimized Circuit, 10 MHz to 12 GHz, V_{DD} = 5 V, R_{BIAS} = 620 Ω

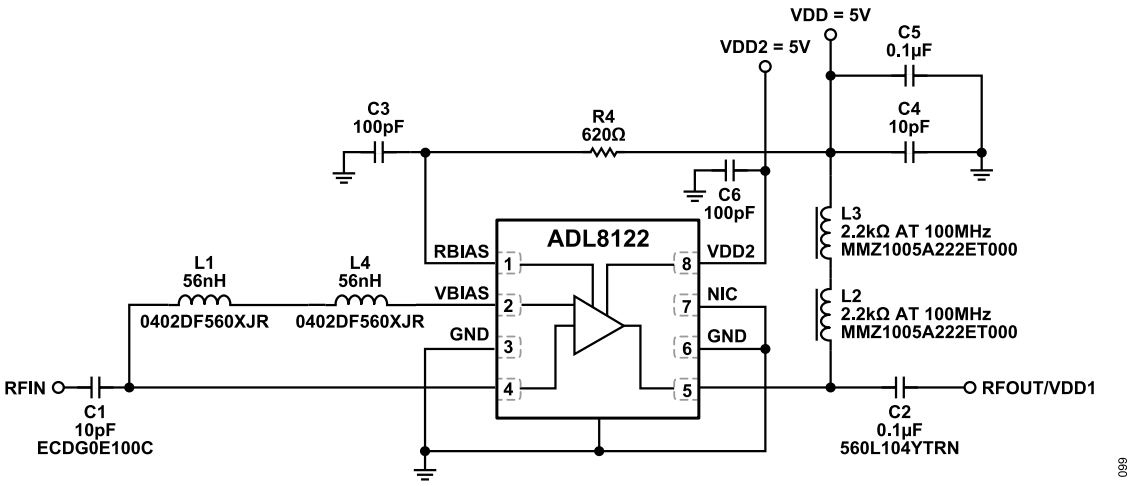


Figure 99. Application Circuit for ADL8122-EVALZ Optimized Overdrive Recovery Time

APPLICATIONS INFORMATION

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 100 shows a recommended power management circuit for the ADL8122. The LT8607 step-down regulator is used to step down a 12 V rail to 6.77 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 5 V output. Even though the circuit shown in Figure 100 has an input voltage (VIN) of 12 V, the input range to the LT8607 can be as high as 42 V.

The 6.77 V regulator output of the LT8607 is set by the R2 and R3 resistors, according to the following equation:

$R2 = R3((VOUT/0.778\ V) - 1)$, where VOUT is the output voltage.

The switching frequency (f_{SW}) is set to 2 MHz by the 18.2 kΩ resistor (R1) on the RT pin. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.2 MHz.

The output voltage of the LT3042 is set by the R4 resistor connected to the SET pin, according to the following equation:

$VOUT = 100\ \mu A \times R4$

The resistors on the PGFB pins of the LT3042 are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 5 V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more (5%). Therefore, putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 5 V output to give a convenient 0 V to 5 V voltage range. Table 11 provides the recommended resistor values for operation at 6 V to 3 V.

Table 11. Recommended Resistor Values for Operating at 6 V to 3 V

LDO VOUT (V)	R4 (kΩ)	R7 (kΩ)	R8 (kΩ)
6	60.4	620	30.1
5	49.9	442	30.1
4	40.2	301	30.1
3	30.1	225	30.1

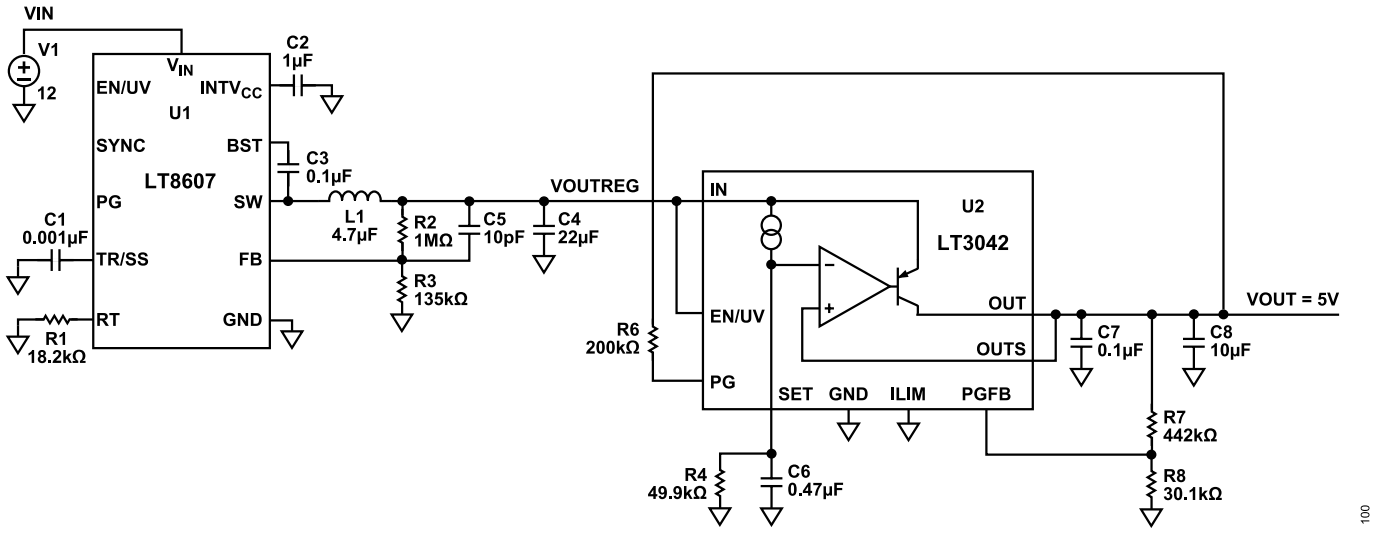


Figure 100. Recommended Power Management Circuit

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CP-8-30	LFCSP	8-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8122ACPZN	−55°C to +125°C	8-lead LFCSP, 2 mm × 2 mm × 0.85 mm	Tape, 1	CP-8-30
ADL8122ACPZN-R7	−55°C to +125°C	8-lead LFCSP, 2 mm × 2 mm × 0.85 mm	Reel, 3000	CP-8-30

[1] Z = RoHS Compliant Part.

[2] The lead finish of the ADL8122ACPZN and ADL8122ACPZN-R7 is nickel palladium gold.

EVALUATION BOARDS

Model[1]	Description
ADL8122-EVALZ	ADL8122 Evaluation Board for 10 MHz to 10 GHz
ADL8122-EVAL1Z	ADL8122 Evaluation Board for 10 kHz to 10 GHz

[1] Z = RoHS Compliant Part.

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