Data Sheet

ADIS16607

Precision, Miniature MEMS IMU

FEATURES

- Triaxial digital gyroscope
  - ±480°/sec typical and ±2000°/s minimum dynamic range models (ADIS16607-2 and ADIS16607-3)
  - 2.3°/hr in-run bias stability, 1σ (ADIS16607-2)
  - 0.19°/√hr angular random walk, 1σ (ADIS16607-2)
  - 1.0°/hr/g^2 vibration rectified error, 1σ
- Triaxial digital accelerometer, ±40*g* minimum dynamic range
  - 13µ*g* in-run bias stability, 1σ, z-axis
  - 0.1m*g*/g^2 vibration rectified error
- Factory calibrated sensitivity, bias, and axial alignment
  - Calibration temperature range: −40°C to +85°C
  - ±0.2°/sec gyroscope bias error over temperature, 1σ (ADIS16607-2)
  - ±1m*g* accelerometer bias error over temperature, 1σ
  - ±0.02° axis to axis orthogonality error, 1σ
- SPI- and I^2C-compatible data communications
- Programmable operation and control
  - Data ready indicator for synchronous data acquisition
  - External sync modes: direct (1000Hz to 8000Hz input) and scaled (0.8Hz to 400Hz input)
  - FIFO, 1024 words
  - On demand self-test of inertial sensors
- Single-supply operation (VDD): 3.1V to 3.6V
- 5000*g* mechanical shock survivability, any axis powered
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Navigation, stabilization, and instrumentation
- Unmanned and autonomous vehicles
- Smart agriculture and construction machinery
- Factory and industrial automation, robotics
- Virtual and augmented reality
- Internet of Moving Things

GENERAL DESCRIPTION

The ADIS16607 is a precision, miniature microelectromechanical system (MEMS), inertial measurement unit (IMU) that includes a triaxial gyroscope and a triaxial accelerometer. Each inertial sensor in the ADIS16607 is combined with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, and alignment. As a result, each sensor has dynamic compensation formulas that provide accurate sensor measurements over a broad set of conditions. Additionally, the sensor provides strong vibration immunity for robust operation in challenging environments.

The ADIS16607 provides a simplified, cost-effective method for integrating accurate, multiaxis inertial sensing into systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interfaces (SPI and I^2C) and register structure provide a simple interface for data collection and configuration control.

The ADIS16607 is available in a hermetic, 18-terminal, ceramic leadless chip carrier that is approximately 6.9mm × 6.9mm × 2.85mm.

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REVISION HISTORY

10/2026—Rev. 0 to Rev. A

Changes the Gravity, 1 g Section....16
Changes to Table 52 and Table 53....41
Changes to Table 54, Table 55, Table 56, and Table 57....42

9/2026—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

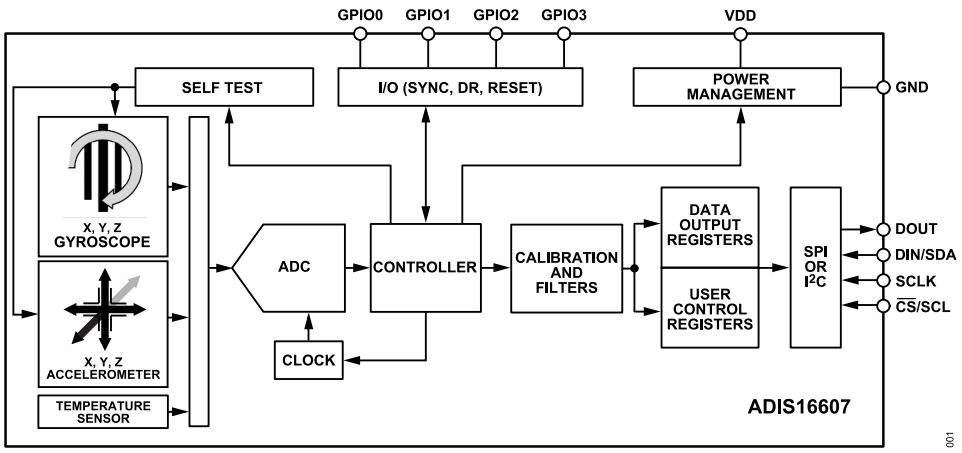


Figure 1. Functional Block Diagram

SPECIFICATIONS

T_C = 25°C, VDD = IOVDD = 3.3V, angular rate = 0°/sec, and dynamic range = ±2000°/sec, unless otherwise noted. 1*g* is the acceleration due to gravity and is assumed to be 9.797464m/sec^2.

Table 1. Specifications Table

Parameters	Test Conditions/Comments	Min	Typ	Max	Units
GYROSCOPE					
Dynamic Range	ADIS16607-2	±470	±480	±490	°/sec
	ADIS16607-3	±2000			°/sec
Sensitivity	ADIS16607-2, 16-bit data format		62.5		LSB/°/sec
	ADIS16607-3, 16-bit data format		15.625		LSB/°/sec
	ADIS16607-2, 24-bit data format		16000		LSB/°/sec
	ADIS16607-3, 24-bit data format		4000		LSB/°/sec
Initial Sensitivity Error	ADIS16607-2, 25°C, postsolder, 1σ		±0.2		%
	ADIS16607-3, 25°C, postsolder, 1σ		±0.35		%
Repeatability[1]			±1.0		%FS
Error vs. Temperature	Postsolder, x-axis and y-axis, , −40°C ≤ T_C ≤ +85°C, 1σ		±0.35		%
	Postsolder, z-axis, −40°C ≤ T_C ≤ +85°C, 1σ		±0.6		%
Axis-to-Axis Orthogonality Error	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.02		Degrees
Nonlinearity [2]	ADIS16607-2, FS = 480°/sec, 1σ		0.35		%FS
	ADIS16607-3, FS = 2000°/sec, 1σ		0.6		%FS
Bias					
Initial Bias Error	25°C, postsolder, 1σ		±0.2		°/sec
Repeatability[3]	−40°C ≤ T_C ≤ +85°C, 1σ		0.64		°/sec
Error over Temperature	Postsolder, ADIS16607-2, −40°C ≤ T_C ≤ +85°C, 1σ		±0.2		°/sec
	Postsolder, ADIS16607-3, −40°C ≤ T_C ≤ +85°C, 1σ		±0.3		°/sec
In-Run Bias Stability	ADIS16607-2, 1σ		2.3		°/hr
	ADIS16607-3, 1σ		7.5		°/hr
Angular Random Walk	ADIS16607-2, 1σ		0.19		°/√hr
	ADIS16607-3, 1σ		0.25		°/√hr
Linear Acceleration Effect	Any direction, 1σ		20		°/hr/*g*
Vibration Rectified Error (VRE)	Random vibration, 4*g* RMS, 50Hz to 2kHz, 1σ		1.0		°/hr/g^2
Self Test Delta	X-axis, y-axis, and z-axis				
	ADIS16607-2	5200		10400	LSB
	ADIS16607-3	1300		2600	LSB
Output Noise	No filtering, 25°C, 1σ				
	ADIS16607-2		0.17		°/sec RMS
	ADIS16607-3		0.21		°/sec RMS
Rate Noise Density	Frequency = 10Hz to 40Hz, no filtering, 1σ				
	ADIS16607-2		4.5×10^{-3}		°/sec/√Hz
	ADIS16607-3		5.3×10^{-3}		°/sec/√Hz
3dB Bandwidth	No filtering		1211		Hz
Sensor Resonant Frequency		64	78	88	kHz

SPECIFICATIONS

Table 1. Specifications Table (Continued)

Parameters	Test Conditions/Comments	Min	Typ	Max	Units
ACCELEROMETER					
Dynamic Range		±40			*g*
Sensitivity	16-bit data format		781.25		LSB/*g*
	24-bit data format		200000		LSB/*g*
Initial Sensitivity Error	25°C, postsolder, 1σ		±0.04		%
Error over Temperature	Postsolder, −40°C ≤ T_C ≤ +85°C, 1σ		±0.06		%
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1σ		±0.125		%
Axis-to-Axis Orthogonality Error	−40°C ≤ T_C ≤ +85°C, 1σ		±0.02		Degrees
Nonlinearity[2]	FS = 40*g*, stimulus = ±10*g*, 1σ		0.03		%
	FS = 40*g*, stimulus = ±20*g*, 1σ		0.12		%
	FS = 40*g*, stimulus = ±40*g*, 1σ		0.8		%
Bias					
Initial Bias Error	25°C, postsolder, 1σ		±2.5		m*g*
Repeatability[3]	−40°C ≤ T_C ≤ +85°C, 1σ		6		m*g*
Error over Temperature	Postsolder, −40°C ≤ T_C ≤ +85°C, 1σ		±1		m*g*
In-Run Bias Stability	1σ				
X-Axis and Y-Axis			9		μ*g*
Z-Axis			13		μ*g*
Velocity Random Walk	1σ				
X-Axis and Y-Axis			0.045		m/sec/√hr
Z-Axis			0.042		m/sec/√hr
Vibration Rectified Error (VRE)	Random vibration, 4*g* RMS, 50Hz to 2kHz, 1σ		0.1		m*g*/*g*^{2}
Self Test Delta					
X-Axis and Y-Axis		100		260	LSB
Z-Axis		2000		3100	LSB
Output Noise	No filtering, 25°C, 1σ				
X-Axis and Y-Axis			3.9		m*g* RMS
Z-Axis			3.6		m*g* RMS
Noise Density	f = 10Hz to 40Hz, no filtering, 1σ				
X-Axis and Y-Axis			105		μ*g*/√Hz
Z-Axis			96		μ*g*/√Hz
3dB Bandwidth	No filtering		1075		Hz
Sensor Resonant Frequency	X-axis and y-axis		5.34		kHz
	Z-axis		4.81		kHz
Quality Factor	X-axis and y-axis		2.75		
	Z-axis		0.79		
TEMPERATURE SENSOR					
Scale Factor			0.005		°C/LSB
Offset			25		°C
FUNCTIONAL TIMES[4]					
Power-On Start-Up Time[5]			130		ms
Reset Recovery Time[6]			50		ms
Inertial Settling Time[7]			40		ms
Self Test Time[8]			15		ms

SPECIFICATIONS

Table 1. Specifications Table (Continued)

Parameters	Test Conditions/Comments	Min	Typ	Max	Units
CONVERSION RATE, f_S[9]		8000	9750	11000	SPS
Internal Clock Drift over Temperature	−40°C ≤ T_C ≤ +85°C		0.25		%
External Sync Input Clock, f_{SYNC}					
Direct Input Sync Mode		1000		8000	Hz
Scaled Sync Mode		0.8		400	Hz
POWER SUPPLY (V_{DD})	Operating voltage range	3.1		3.6	V
Device Current Consumption	V_{DD} = 3.3V				
Start-Up	From power on to t = 15ms		35		mA
Normal Operation			15	20	mA
DIGITAL INTPUT AND OUTPUT SUPPLY (IO_{VDD})	Operating voltage range	2.0		VDD	V

1 Sensitivity repeatability is the root sum of squares (RSS) combination of the following sources of drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000hours, +105°C).

2 This measurement is based on the deviation from a linear model calculated over 20%FS (±96°/sec or ±400°/sec for the ADIS16607-2 and ADIS16607-3 gyroscopes, respectively, and ±8*g* for the accelerometer).

3 Bias repeatability is the RSS combination of the following sources of drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000 hours, +105°C).

4 These times do not include thermal settling and internal filter response times, which may affect overall accuracy.

5 From VDD ≥ 3.1V to all DIAG_STAT flags cleared.

6 From software reset command or short (10µs) hardware $\overline{\text{RESET}}$ pulse to all DIAG_STAT flags cleared. Recovery after a long hardware $\overline{\text{RESET}}$ pulse behaves similarly to power-on start-up.

7 From all DIAG_STAT flags cleared to when the gyroscope outputs reach ±0.3°/sec of settled values.

8 The self test time is measured as the time for the gyroscope outputs to settle after applying self test stimuli. See the On-Demand Self Test section.

9 The internal conversion rate is proportional to the gyroscope sensor resonant frequency.

SPECIFICATIONS

SPI TIMING SPECIFICATIONS

T_A = 25°C, VDD = 3.3V, and 2.0V ≤ IOVDD ≤ VDD, unless otherwise noted.

Table 2. SPI Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCLK}	SPI operating frequency	0.1	10	MHz
t_{CHS}	Clock (SCLK) high time	45		ns
t_{CLS}	Clock (SCLK) low time	45		ns
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	20		ns
t_{DAV}	DOUT valid after SCLK edge		36	ns
t_{DSU}	DIN setup time before SCLK rising edge	20		ns
t_{DHD}	DIN hold time after SCLK rising edge	20		ns
t_{SFS}	Last SCLK edge to $\overline{CS}$ deassertion	20		ns
t_{DSHI}	$\overline{CS}$ deassertion to DOUT high impedance	0	25	ns
t_{STALL}	Time between frames		10	ns

Table 3. SPI Digital Input and Output Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
DIGITAL INPUT					
Low Level Input Voltage (V_{IL})	DIN, $\overline{CS}$, SCLK			0.2 × IOVDD	V
High Level Input Voltage (V_{IH})	DIN, $\overline{CS}$, SCLK	0.8 × IOVDD			V
Input Leakage Current (I_{IL})	DIN, SCLK, at V_{IL} = 0V	−250		+250	nA
	DIN, SCLK, at V_{IL} = IOVDD	−250		+250	nA
Internal Pull-Up Current (I_{PU})	IOVDD = 2.0V, $\overline{CS}$ = 0.15 × IOVDD		8	12	µA
DIGITAL OUTPUT					
Low Level Output Voltage (V_{OL})	DOUT, current = 3mA			0.2 × IOVDD	V
High Level Output Voltage (V_{OH})	DOUT, current = −2mA	0.8 × IOVDD			V
Output Leakage Current (I_{OL})	DOUT	−250		+250	nA
Capacitive Load (C_L)				20	pF

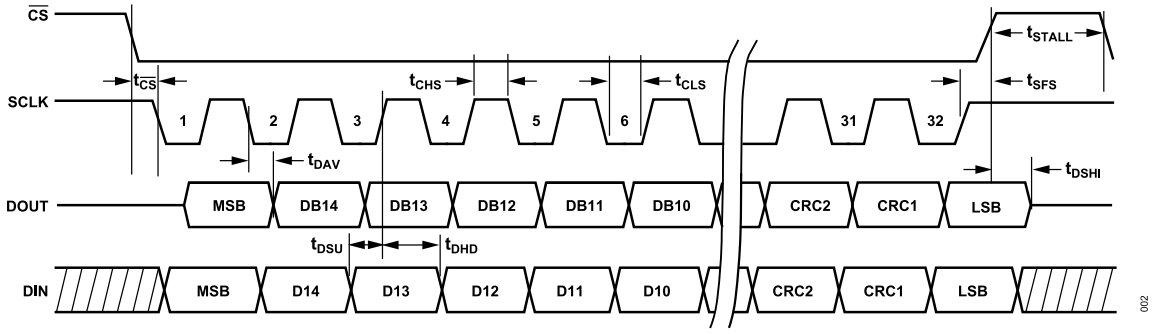


Figure 2. SPI Timing Diagram

SPECIFICATIONS

I²C TIMING SPECIFICATIONS

T_A = 25°C, VDD = 3.3V, and IOVDD = 3.3V, unless otherwise noted.

Table 4. I²C Timing Specifications in Fast Mode Plus

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC INPUT LEVELS						
Input Voltage						
Low Level	V_{IL}				0.3 × IOVDD	V
High Level	V_{IH}		0.7 × IOVDD			V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05 × IOVDD			V
Input Current	I_{IL}	0.1 × IOVDD < V_{IN} < 0.9 × IOVDD	−10		+10	µA
DC OUTPUT LEVELS						
Output Voltage						
Low Level	V_{OL}	I_{OL} = 7mA			0.4	V
Output Current						
Low Level	I_{OL}	V_{OL} = 0.42V	20			mA
AC INPUT LEVELS						
SCLK Frequency			10		1000	kHz
SCL High Time	t_{HIGH}		260			ns
SCL Low Time	t_{LOW}		500			ns
Start Setup Time	t_{SUSTA}		260			ns
Start Hold Time	t_{HDSTA}		260			ns
SDA Setup Time	t_{SUDAT}		50			ns
SDA Hold Time	t_{HDDAT}		10			ns
Stop Setup Time	t_{SUSTO}		260			ns
Bus Free Time	t_{BUF}		500			ns
Capacitive Load for Each Bus Line	C_B				500	pF
SCL Input Rise Time	t_{RCL}				120	ns
SCL Input Fall Time	t_{FCL}				120	ns
SDA Input Rise Time	t_{RDA}				120	ns
SDA Input Fall Time	t_{FDA}				120	ns
Width of Spikes to Suppress	t_{SP}	Not shown in Figure 3			50	ns
AC OUTPUT LEVELS						
Propagation Delay		C_{LOAD} = C_B (maximum)				
Data	t_{VDDAT}		97		450	ns
Acknowledge	t_{VDACK}				450	ns
Output Fall Time	t_F	Not shown in Figure 3	20 × (IOVDD/5.5)		300	ns

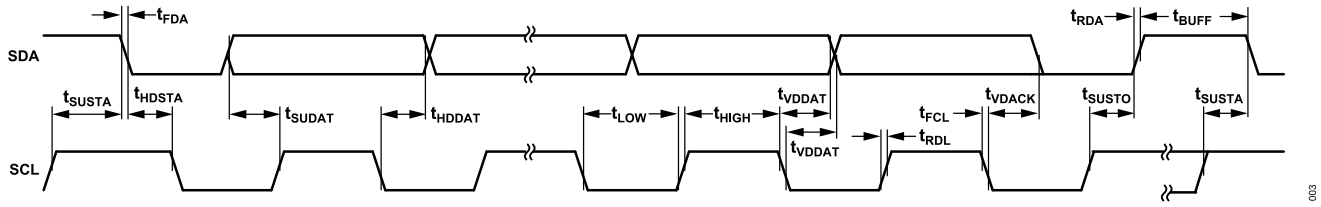


Figure 3. I²C Interface Timing Diagram

SPECIFICATIONS

DIRECT SYNC MODE TIMING

Table 5. Input Clock Timing Specifications, Direct Sync Mode

Parameters	Description	Min	Typ	Max	Unit
t_1	Input sync pulse width	125			ns
t_2	Input sync pulse period	125			µs
t_{STDR}	Input sync to data ready (DR) valid transition	62		210	µs
t_{NV}	Data invalid time		6		µs

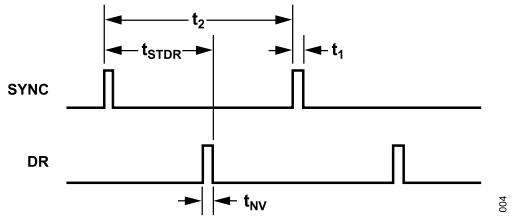


Figure 4. Input Clock Timing Diagram, Direct Sync Mode

FUNCTIONAL TIMES

Table 6. Functional Times

Parameter	Description	Min[1]	Typ	Max	Unit
PROCESSING TIME					
Sync Scale	Configure input clock scale factor	125			µs
Decimate	Configure decimation rate	125	(DEC_RATE + 2) × 125		µs
Configuration	Configure miscellaneous functions	125			µs
Gyroscope Infinite Impulse Response (IIR) Filter	Configure gyroscope IIR filter (does not include filter settling)	125			µs
Accelerometer IIR Filter	Configure accelerometer IIR filter (does not include filter settling)	125			µs

[1] Monitoring the DR signal for the return of regular pulsing can help minimize system wait times.

ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute Maximum Ratings

Parameter	Rating
Mechanical Shock Survivability	
Any Axis, Powered	5000*g*, 0.5ms pulse width
Any Axis, Unpowered	10000*g*, 0.5ms pulse width
VDD to GND	−0.3V to +4.2V
IOVDD to GND	−0.5V to VDD
Digital Input Voltage to GND	−0.3V to IOVDD + 0.2V
Digital Output Voltage to GND	−0.3V to IOVDD + 0.2V
Temperature Range	
Calibration	−40°C to +85°C
Operating	−40°C to +105°C
Storage[1]	−55°C to +150°C
Barometric Pressure	2 bar

[1] Extended exposure to temperatures that are lower than −40°C or higher than +85°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

The ADIS16607 is a multichip module that includes many active components. The values in Table 8 identify the thermal response of the hottest component inside of the ADIS16607 with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either T_A or T_C.

For example, assuming that θ_{JA} is 28.9°C/W, when T_A is 70°C, the hottest T_J inside of the ADIS16607 is 74.8°C.

$$T_J = \theta_{JA} \times VDD \times Supply\ Current\ (I_{DD}) + 70°C$$

$$T_J = 28.9°C/W \times 3.3V \times 0.05A + 70°C$$

$$T_J = 74.8°C$$

Table 8. Package Characteristics

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	Device Weight	Thermal Expansion Coefficient
E-18-5	28.9°C/W	1.6°C/W	0.398g	7.1ppm/K

[1] Thermal impedance values come from direct observation of the hottest temperature inside of the ADIS16607 when it is attached to an FR4-08 PCB that has two metal layers and has a thickness of 0.063 inches.

[2] θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

[3] θ_{JC} is the junction to case thermal resistance. The case bottom is used here.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

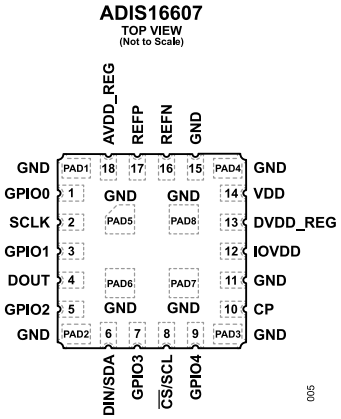


Figure 5. Pin Assignment, Top View

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	GPIO0	CMOS input/ output	General-Purpose Input and Output 0. This pin is a reconfigurable input and output pin whose default function is active low reset ($\overline{\text{RESET}}$). The functionality is controlled by the USER_GPIO_CFG1 register. The voltage level is set by the IOVDD pin. This pin has an internal 140kΩ pull-up resistor at power-up.
2	SCLK	CMOS input	SPI Mode Serial Clock.
3	GPIO1	CMOS input/ output	General-Purpose Input and Output 1. This pin is a reconfigurable input and output pin whose default function is wake. The functionality is controlled by the USER_GPIO_CFG1 register. The voltage levels are set by the IOVDD pin. This pin has an internal 140kΩ pull-up resistor at power-up.
4	DOUT	CMOS output	Serial Data Output. Clocks output on the SCLK falling edge.
5	GPIO2	CMOS input/ output	General-Purpose Input and Output 2. This pin is a reconfigurable input and output pin that can be mapped as sync signal input. The functionality is controlled by the USER_GPIO_CFG1 register. The voltage levels are set by the IOVDD pin. This pin defaults to idle and has an internal 140kΩ pull-up resistor at power-up.
6	DIN/SDA	CMOS input	SPI Serial Data In (DIN). SPI Data Input (SDA). In I^2C mode, this pin is the serial data line.
7	GPIO3	CMOS input/ output	General-Purpose Input and Output 3. This pin is a reconfigurable input and output pin that can be mapped as the DR output signal. The functionality is controlled by the USER_GPIO_CFG1 register. The voltage levels are set by the IOVDD pin. This pin defaults to idle and has an internal 140kΩ pull-up resistor at power-up.
8	$\overline{\text{CS}}$/SCL	CMOS input	Chip Select (Active Low) when in SPI Mode ($\overline{\text{CS}}$) and Serial Clock when in I^2C Mode (SCL). This pin has an internal 140kΩ pull-up resistor.
9	GPIO4	CMOS input/ output	General-Purpose Input and Output 4. This pin is a reconfigurable input and output pin that can be mapped as a device not OK (DEV_NOK) output signal. The functionality is controlled by the USER_GPIO_CFG1 register. The voltage levels are set by the IOVDD pin. This pin defaults to idle and has an internal 140kΩ pull-up resistor at power-up.
10	CP	Output	High-Voltage Charge Pump Output. Connect this pin to a 0.047µF capacitor rated to 100V in parallel and to ground.
11, 15	GND	Supply	Power Ground.
12	IOVDD	Supply	Input and Output Power Supply, 2.0V to 3.6V. This power supply determines the voltage level of the serial port and GPIO pins. Connect this pin to a 1µF capacitor and to ground.
13	DVDD_REG	Output	Digital Power Supply Voltage Regulator Output. Connect this pin to a 1µF capacitor and to ground.
14	VDD	Supply	Power Supply, 3.1V to 3.6V . Connect this pin to a 1µF capacitor in parallel and to ground.
16	REFN	Output	Negative Side of Internal ADC Reference Voltage. Connect the REFN pin to ground.
17	REFP	Output	Positive Side of Internal ADC Reference Voltage. Connect a 4.7µF capacitor across the REFP and REFN pins.
18	AVDD_REG	Output	Analog Power Supply Voltage Regulator Output. Connect this pin to the REFP pin.
PAD1 to PAD8	GND	Supply	Ground. These pins are internally connected to Pin 11 (GND).

TYPICAL PERFORMANCE CHARACTERISTICS

GYROSCOPES

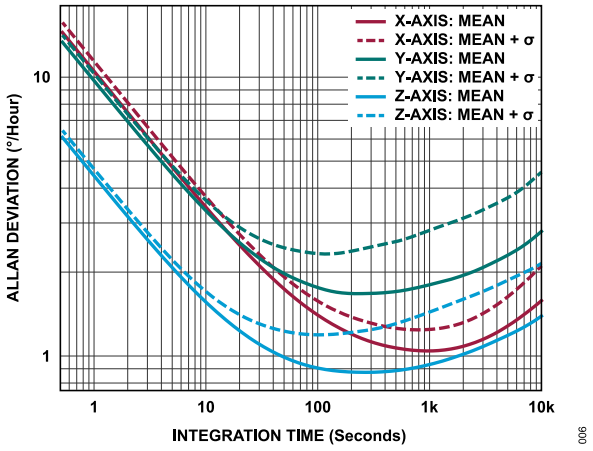


Figure 6. Gyroscope Allan Deviation, T_C = 25°C, ADIS16607-2

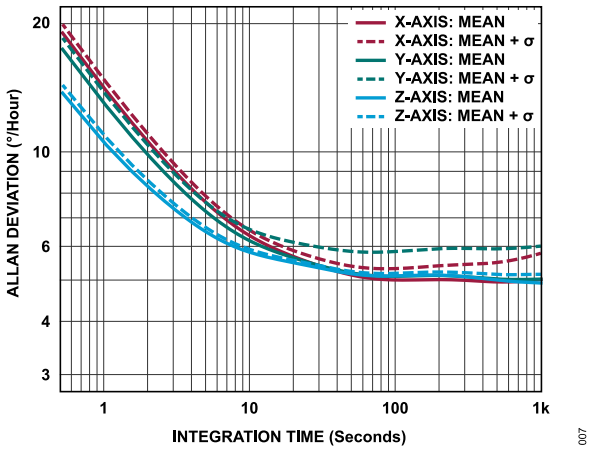


Figure 7. Gyroscope Allan Deviation, T_C = 25°C, ADIS16607-3

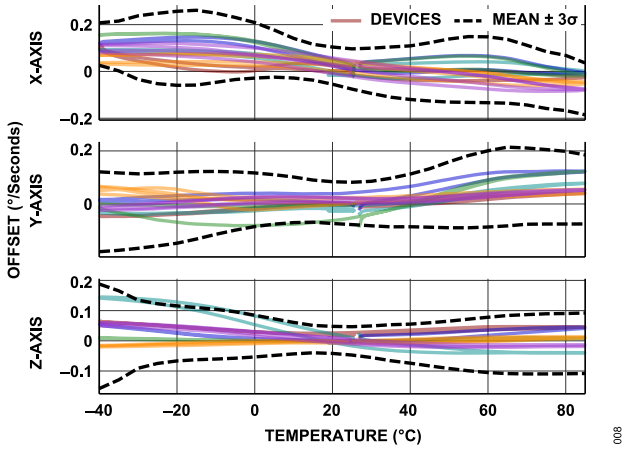


Figure 8. Gyroscope Bias Error vs. Temperature, ADIS16607-2

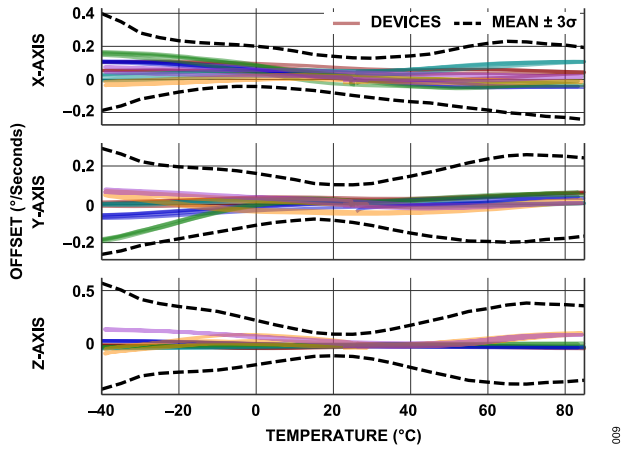


Figure 9. Gyroscope Bias Error vs. Temperature, ADIS16607-3

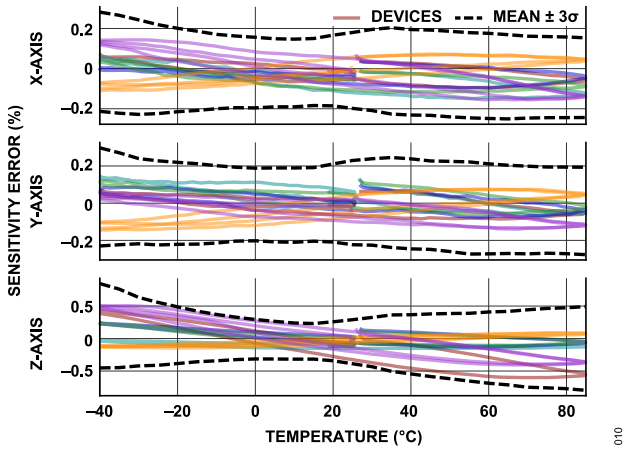


Figure 10. Gyroscope Sensitivity Error vs. Temperature, ADIS16607-2

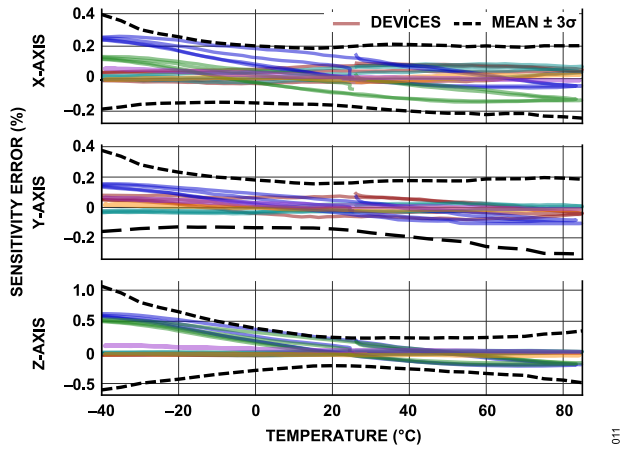


Figure 11. Gyroscope Sensitivity Error vs. Temperature, ADIS16607-3

TYPICAL PERFORMANCE CHARACTERISTICS

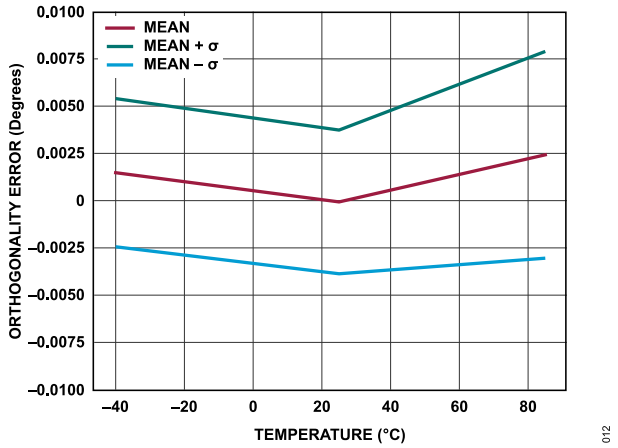


Figure 12. Axis to Axis Gyroscope Orthogonality Error vs. Temperature, All Axes

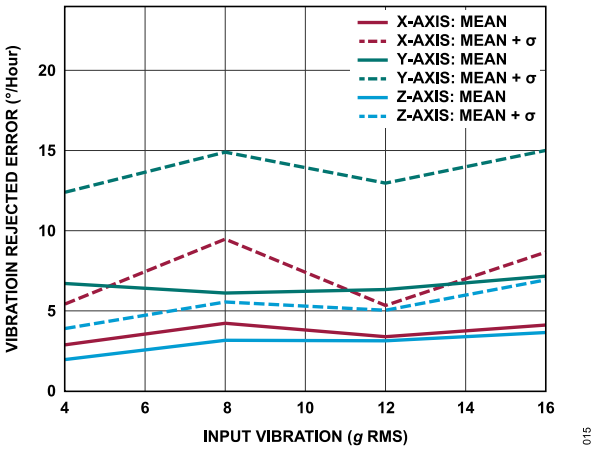


Figure 15. Gyroscope Vibration Rectified Error, T_C = 25°C

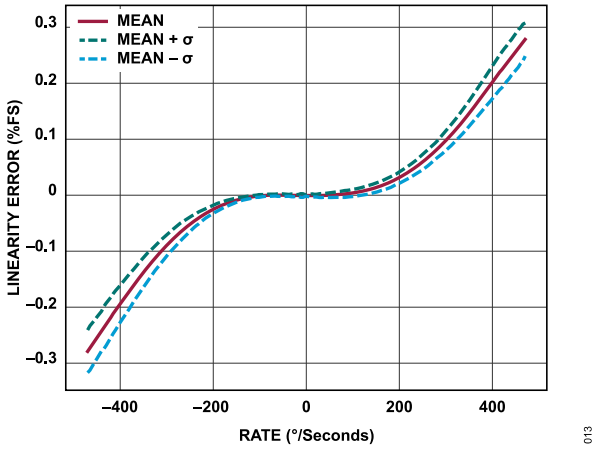


Figure 13. Gyroscope Linearity Error, T_C = 25°C, ADIS16607-2, All Axes

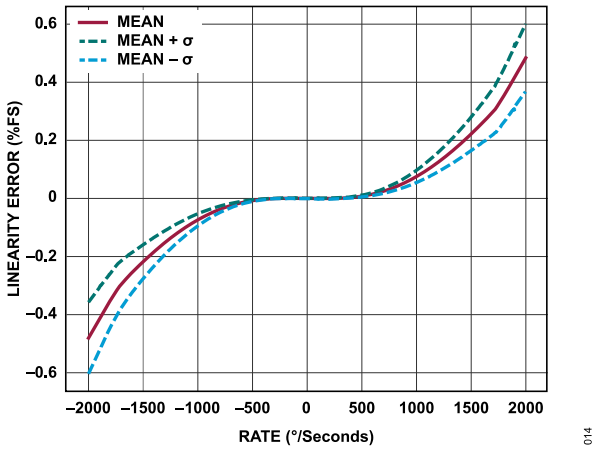


Figure 14. Gyroscope Linearity Error, T_C = 25°C, ADIS16607-3, All Axes

TYPICAL PERFORMANCE CHARACTERISTICS

ACCELEROMETERS

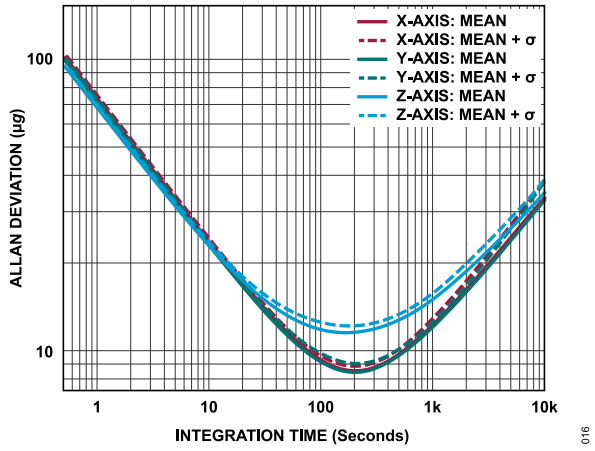


Figure 16. Accelerometer Allan Deviation, T_C = 25°C

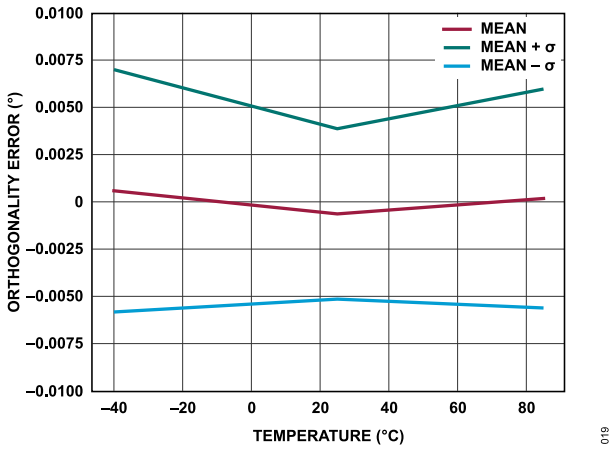


Figure 19. Accelerometer Orthogonality Error vs. Temperature, All Axes

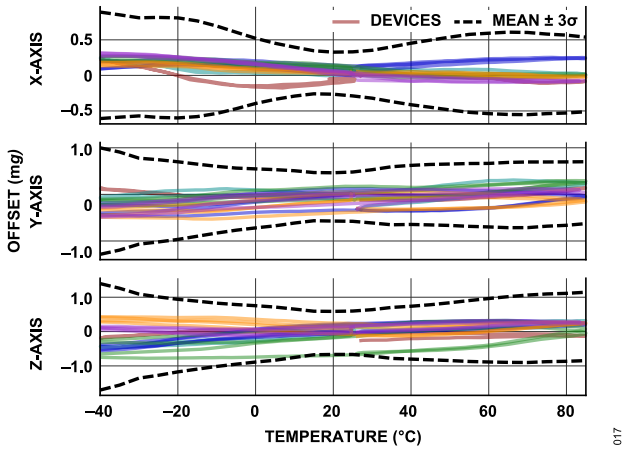


Figure 17. Accelerometer Bias Error vs. Temperature

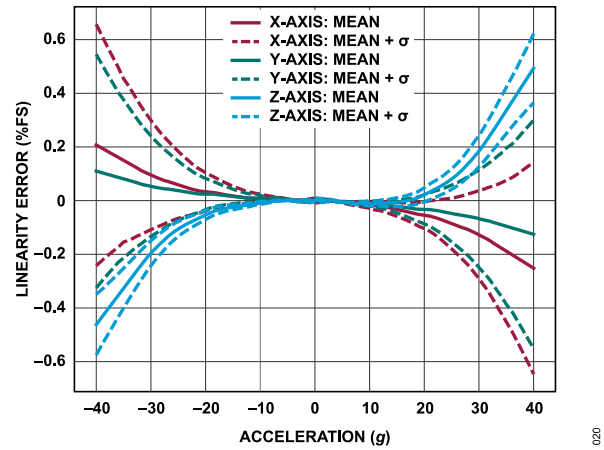


Figure 20. Accelerometer Linearity Error

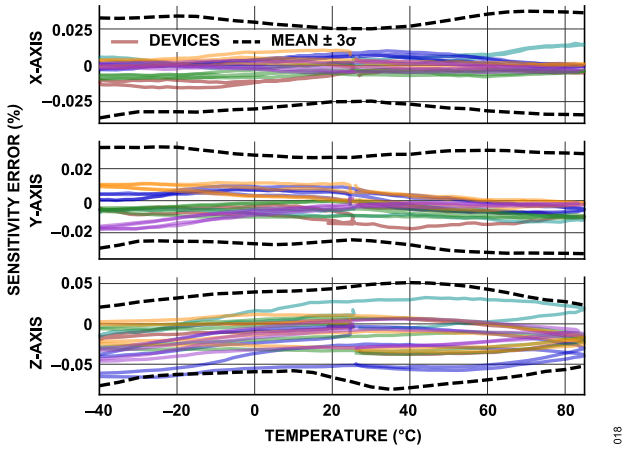


Figure 18. Accelerometer Sensitivity Error vs. Temperature

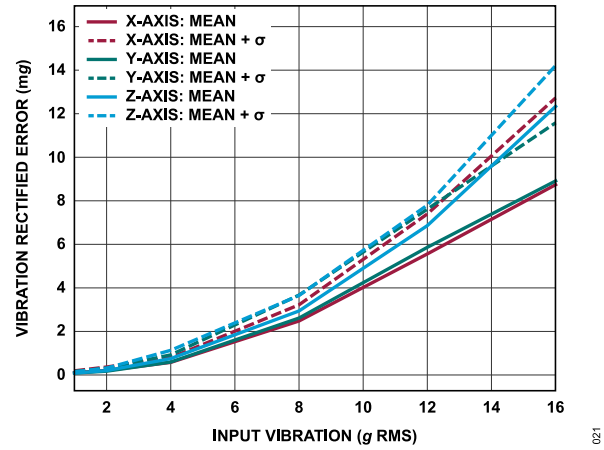


Figure 21. Accelerometer Vibration Rectified Error, T_C = 25°C

TERMINOLOGY

Gravity, 1*g*

In this data sheet, gravitational acceleration is defined as follows:

$1g = 9.797464(m/s^2)$ (1)

This value can be used to convert specifications from *g* to m/sec^2 throughout this data sheet.

It is important to keep in mind that the gravitational acceleration varies slightly across the surface of the earth. Consider the following factors when calculating the precise acceleration due to gravity at a specific location on Earth:

- Elevation (gravity decreases as elevation increases).
- Latitude. Earth is an oblate spheroid (gravity is weaker on the equator and stronger at the poles).
- Earth's rotation (gravity is weaker on the equator due to rotational velocity and conservation of momentum).

In certain cases, small variations in gravitational acceleration are important. It is important for the user to account for this and realize that the output of an accelerometer slightly varies as a result of this.

Table 10. Gravitational Acceleration Examples

Location	Latitude (°)	Elevation (m)	Effective Gravitational Acceleration (m/sec^2)[1]
Equator	0	0	9.780325
North or South Pole	+90 or −90	0	9.832185
Analog Devices, Inc., Factory	36.063	251	9.797464

[1] Accounts for elevation, Earth's rotation, and oblateness of Earth.

Use the following formula to determine the effective gravitational acceleration at a specific location on Earth (at sea level):

$$g_0 = \frac{r_{EQ}g_{EQ}\cos^2(LAT) + r_{POL}g_{POL}\sin^2(LAT)}{\sqrt{r^2{}_{EQ}\cos^2(LAT) + r^2{}_{POL}\sin^2(LAT)}} \quad (2)$$

where:
g_0 is the effective gravitational acceleration.
LAT is the latitude in degrees.
r_{EQ} is the Earth's radius at the equator (6,378,137m).
r_{POL} is the Earth's radius at the poles (6,356,752m).
g_{EQ} is the effective acceleration at the equator (9.780325m/s^2).
g_{POL} is the effective acceleration at the poles (9.832185m/s^2).

The previous equation accounts for latitude and Earth's rotation; however, it does not account for the elevation. To correct for elevation, use the following approximation:

$$\Delta g = g_H - g_0 \cong GM\left(\frac{1}{r_H{}^2} - \frac{1}{r_0{}^2}\right) \quad (3)$$

$$r_0 = \sqrt{\frac{\left(r^2{}_{EQ}\cos(LAT)\right)^2 + \left(r^2{}_{POL}\sin(LAT)\right)^2}{\left(r_{EQ}\cos(LAT)\right)^2 + \left(r_{POL}\sin(LAT)\right)^2}} \quad (4)$$

where:
g_H is the gravitational acceleration at elevation r_H.
g_0 is the gravitational acceleration at sea level.*G* the gravitational constant (6.6743 × 10^{-11} (Nm^2/kg^2).
M is the mass of Earth (5.972365 × 10^{24}(kg)).
r_0 is the radius of Earth at specific latitude.
$r_H = r_0$ + Elevation in Meters.

The effective gravitational acceleration including elevation, g_H, is equal to $g_0 + \Delta g$.

Output Full-Scale Range

The output full-scale range is the guaranteed angular rate and acceleration measurement range at the output of the signal chain. The output full-scale range is guaranteed across all conditions. When specified as a minimum value, angular rate and acceleration measurement may be possible beyond this value; however, performance characteristics are not guaranteed.

Bias

Bias represents the output of the gyroscopes and accelerometers under a zero angular rate and acceleration.

To reduce the influence of external physical stimuli that may exist in the measurement system, average bias over a sufficiently long time window.

Gyroscope = Ω_{MEAS} (Ω_{IN} = 0°/sec)

To calculate accelerometer bias, take measurements at orientations of +1*g* and −1*g* and calculate the average value of the two measurements.

$$XL = \frac{ACC_{MEAS}(g_{IN} = +1g) + ACC_{MEAS}(g_{IN} = -1g)}{2} \quad (5)$$

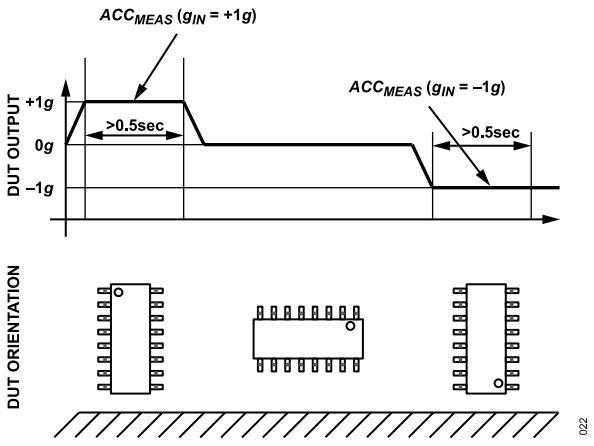


Figure 22. Acceleration Sensitivity Measurement Process

TERMINOLOGY

Bias Error over Temperature

Bias error over temperature is the change in bias directly attributed to changes in temperature. Bias error over temperature is measured relative to the bias at 25°C. Figure 23 shows the bias error over temperature expected for a device with a bias at 25°C equivalent to the initial (start of life) bias.

Bias drift over life can cause the offset measured at 25°C to diverge from the initial (start of life) bias measured during module manufacture. Figure 24 shows how the bias error over temperature limits are adjusted to accommodate divergence of the bias at 25°C and the initial bias.

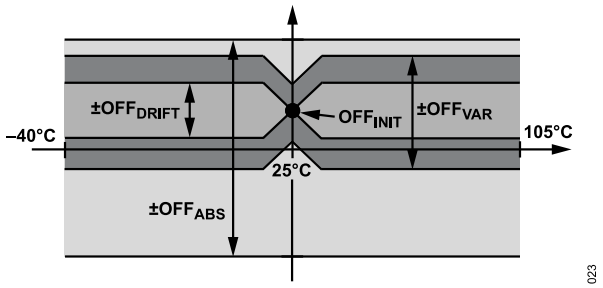


Figure 23. Bias Error over Temperature, $OFF_{INIT} = OFF_{AT_25°C}$

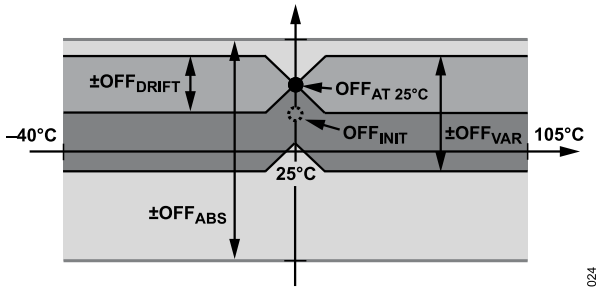


Figure 24. Bias Error over Temperature, $OFF_{INIT} \neq OFF_{AT_25°C}$ (Change $OFF_{AT_25°C}$ to $OFF_{AT_25°C}$)

In-Run Bias Stability

In-run bias stability represents the observability of the bias under constant temperature and static inertial conditions. It is defined as the minimum of the Allan deviation (ADEV) curve as shown in Figure 25.

$$ADEV_{XL}(\tau) = \sqrt{\frac{1}{2(n-1)}\sum_i \left(ACC_{MEAS}(\tau)_{i+1} - ACC_{MEAS}(\tau)_i\right)^2} \quad (6)$$

$$ADEV_{GYRO}(\tau) = \sqrt{\frac{1}{2(n-1)}\sum_i \left(\Omega_{MEAS}(\tau)_{i+1} - \Omega_{MEAS}(\tau)_i\right)^2} \quad (7)$$

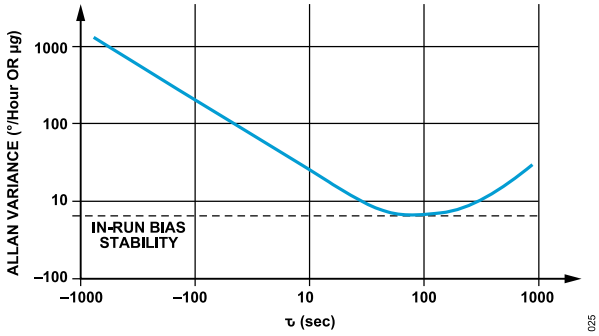


Figure 25. Example Allan Deviation Plot

Inertial Data Format

Inertial data format is the digital representation of the angular rate or acceleration information output by the ADIS16607. Both the angular rate and acceleration information is transmitted as 16-bit (or 24-bit), twos complement values. Nominal sensitivity and nominal scale factor define the relationship for converting from the digital 16-bit (or 24-bit) value to either acceleration or angular rate.

Sensitivity

Sensitivity is the slope of the angular rate and acceleration transfer functions of the ADIS16607. The sensitivity defines the change in output (LSB) per unit change of input (*g* or °/sec).

Scale Factor

The scale factor is the inverse of the sensitivity. The scale factor describes the change in input (*g* or °/sec) per change in the device output (LSB).

TERMINOLOGY

Sensitivity and Scale Factor Tolerance

The sensitivity and scale factor tolerance is the allowable variation between the applied angular rate or acceleration and the digital output (LSB). The following equations show an example of how acceleration sensitivity can be validated at inputs of ±1*g*, and the angular rate sensitivity can be validated at any inputs of ±50°/sec:

$$Acceleration = \frac{ACC_{MEAS}(g_{IN} = +1g) - ACC_{MEAS}(g_{IN} = -1g)}{2g} \quad (8)$$

$$Gyroscope = \frac{\Omega_{MEAS}(\Omega_{IN} = +50°/sec) - \Omega_{MEAS}(\Omega_{IN} = -50°/sec)}{100°/sec} \quad (9)$$

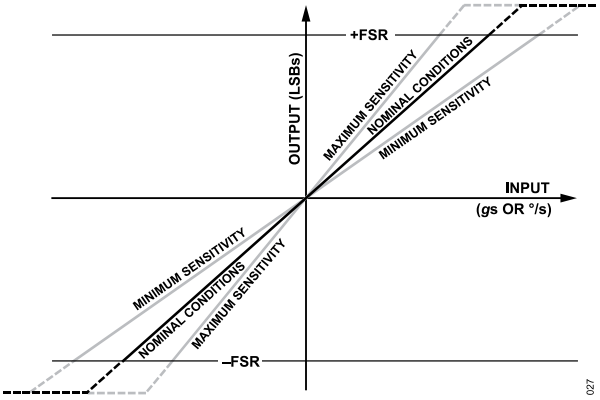


Figure 26. Sensitivity and Scale Factor Transfer Function

Cross-Axis Sensitivity

Cross axis sensitivity is the measured output of the device in response to input stimuli orthogonal to the measurement axis. It is measured as a percentage of the applied orthogonal acceleration or rotation rate.

Axis-to-axis orthogonality error is one contributor to cross-axis sensitivity and represents the deviation from perfect perpendicularity between axes.

Nonlinearity

Nonlinearity is the maximum linearity error or deviation of sensor data points ($\Omega_{MEAS}(\Omega_n)$ or $ACC_{MEAS}(g_n)$) from a purely linear model. Linearity error is mathematically expressed as follows:

Gyroscope = $\Omega_{MEAS}(\Omega_n) - \Omega_{CALC}(\Omega_n)$

Acceleration = $ACC_{MEAS}(g_n) - ACC_{CALC}(g_n)$

where:
Ω_{MEAS} is the measured angular rate at Ω_n.
Ω_{CALC} is the linear fit calculation of the angular rate at Ω_n.
ACC_{MEAS} is the measured acceleration at g_n.
ACC_{CALC} is the linear fit calculation of acceleration at g_n.

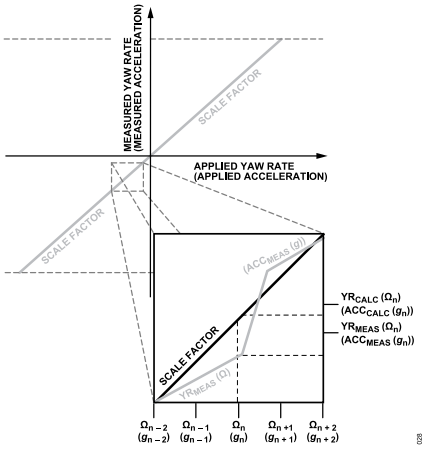


Figure 27. Linearity Error Characteristic

Cutoff (−3dB) Frequency

For applied AC acceleration and angular rates, the cutoff (−3dB) frequency is the frequency at which the input stimulus is attenuated in amplitude by 29.3% (1 − √2 ÷ 2) at the output of the signal chain. The −3dB corner is set according to the electrical signal chain filter settings selected by the user.

RMS Noise

RMS noise is the standard deviation of the acceleration or angular rate output without an applied inertial stimulus. RMS noise can be specified at either room temperature (25°C ± 5°C) or over the entire operating temperature range (−40°C to +105°C). The calculation method to assess the RMS noise is the same, regardless of the temperature range. Take this measurement with a sufficiently high sample rate and sufficiently long duration to ensure that adequate accuracy and repeatability are achieved according to the requirements of the measurement system.

$$\sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(x_i - \bar{x})^2} \quad (10)$$

where:
n is the number of sample values.
x_i is the individual sample value.
$\bar{x}$ is the mean value of the population.

Resonant Frequency

The resonant frequency represents the primary mode in the sensing structure. When subjected to vibration at (or near) this frequency, performance may suffer.

Quality Factor

The quality factor of the accelerometer is a measure of the mechanical gain of the MEMS sensor at its resonant frequency. Use this number to quantify the reduction in accelerometer measurement range for vibration at this frequency.

TERMINOLOGY

Sensitivity to Linear Acceleration

Sensitivity to linear acceleration is the change in the angular rate output of the ADIS16607 in response to an applied linear acceleration. It is measured in °/sec/*g*. Reduced sensitivity to linear acceleration improves the angular rate signal accuracy in harsh environments where shock and vibration are present.

Vibration Rectified Error (VRE)

VRE is the DC offset generated at the sensor output when the device is subject to AC linear vibration.

THEORY OF OPERATION

INTRODUCTION

The ADIS16607 provides the basic signal chain for the accelerometers and gyroscopes of the device. When using the factory default configuration, the ADIS16607 initializes itself at power-up and automatically starts a continuous process of sampling, processing, and loading calibrated sensor data into its output registers.

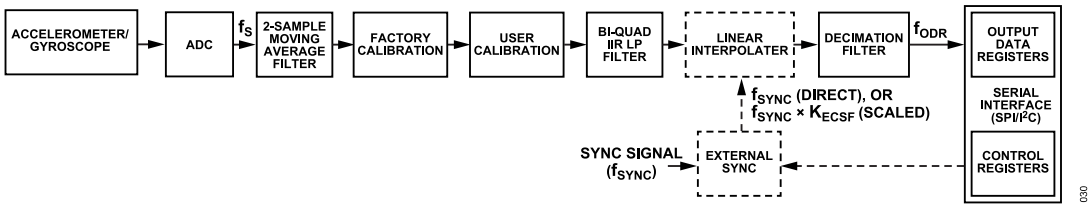


Figure 28. Sensor Signal Chain

THEORY OF OPERATION

CLOCK CONTROL

The ADIS16607 provides three modes of operation with respect to the source of the sampling and processing clock: internal, direct input sync, and scaled sync.

Internal Clock Mode

The ADIS16607 defaults to internal clock mode. In this mode, the ADIS16607 uses an internally generated clock to drive sampling and data processing at the internal conversion rate f_S (see the Specifications section) for each sensor and the associated signal chain.

Direct Input Sync Mode

Setting the SYNC_TYPE bit (Bit 15 of the USER_SYNC register, Address 0x0033) = 0 and the CFG_GPIO_2 bits (Bits[8:6] of the USER_GPIO_CFG1 register, Address 0x002F) = 001 configures the IMU to operate in direct input sync mode with GPIO2 acting as the external SYNC input. For example, the user can provide a crystal oscillator clock signal at the GPIO2 pin. In this mode, internal sampling is still driven at the conversion rate, f_S, but samples are interpolated to the external clock frequency, f_{SYNC}. See the Linear Interpolation section for additional information on the interpolation function. The ADIS16607 performs best when $f_{SYNC} \leq f_S$.

Scaled Sync Mode

Setting the SYNC_TYPE bit (Bit 15 of the USER_SYNC register, Address 0x0033) = 1 selects scaled sync mode, which supports the use of an external sync clock between 1Hz and 400Hz that can come from video systems or global positioning systems (GPS). The user must also set the CFG_GPIO_2 bits (Bits[8:6] of the USER_GPIO_CFG1 register, Address 0x002F) = 001 to allow the GPIO2 pin to act as the external sync input. As in direct input sync mode, internal sampling is driven at the conversion rate f_S, and synchronization is achieved through linear interpolation. In scaled sync mode, the interpolation clock is generated by a clock multiplication phase-locked loop (PLL) that multiplies the frequency of the external sync input (f_{SYNC}) by the sync scale factor, K_{ECSF} (from the SYNC_SCALE_FACTOR bits, Bits[14:0] of the USER_SYNC register, Address 0x0033). In scaled sync mode, the ADIS16607 performs best when $K_{ECSF} \times f_{SYNC} \leq f_S$.

For example, when using a 1Hz input signal, set the SYNC_SCALE_FACTOR bits = 0x1F40 (8000 decimal) to establish an output data rate of 8000SPS.

In scaled sync mode, the TIME_STAMP register indicates the time since the last external sync pulse for each interpolated sample, which can be useful for sensor fusion applications where precise time synchronization of different measurements is required.

Any change to the USER_SYNC register value resets the clock multiplication PLL and restarts the locking process. The locking process starts with an input reference clock edge resetting the feedback clock edge, and lock is declared when time differences between these two edges is ≤100µs.

Notice that in this mode, the IMU continues to generate data even if the external sync signal is lost. For this reason, it is recommended to check the SYNC_LOST (Bit 2) and DPLL_UNLOCKED (Bit 1) flags of the DIAG_STAT register (Address 0x0005) after every DR pulse.

LINEAR INTERPOLATION

When external synchronization is enabled (either direct or scaled), internal measured samples are linearly interpolated to generate the synchronized output samples. Calculate linear interpolation by using the following equation:

$$x_{SYNC} = (1 - \alpha) \times x(z - 1) + \alpha \times x(z) \quad (11)$$

where:
x(z − 1) and *x(z)* are the two measured samples.
$\alpha = t_{SYNC}/2304$, and t_{SYNC} is the number of system clocks from the first measured sample when the sync interpolation rising edge occurs, and the 2304 value represents the total time in system clocks between the two samples.

Because the interpolation method requires the second measured sample to follow the sync interpolation edge, the user has to wait for the next sample before getting the interpolated result. As a result, the DR output from the IMU is still synchronous with the final sample, which means that the DR appears to walk or jump relative to the external sync of the user (see Figure 29). In other words, the sync to DR time (t_{STDR}) has jitter of up to one full internal sample period ($1/f_S$), as detailed in the Direct Sync Mode Timing section.

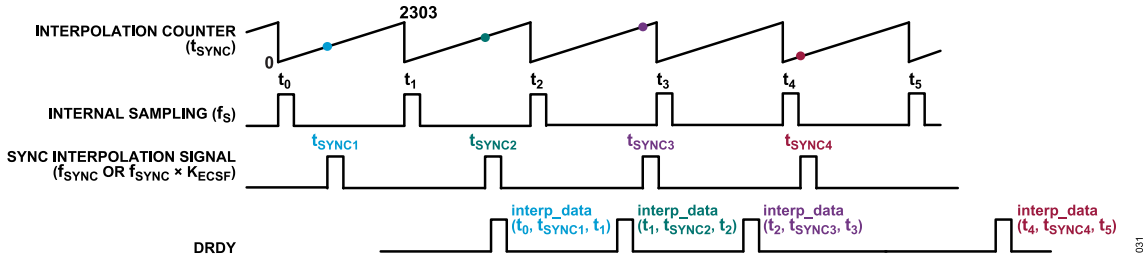


Figure 29. Timing Diagram Example Demonstrating Linear Interpolation

THEORY OF OPERATION

BI-QUAD IIR LOW-PASS FILTER

The low-pass filter in the ADIS16607 is a bi-quad IIR low-pass filter with four settings. The FILT_BW bit field, Bits[8:9], in the MSC_CTRL register (Address 0x0039) provides the configuration controls for this filter. The IIR filter coefficients are preset to select between nominal cutoff frequencies of 500Hz, 100Hz, or 20Hz, or the filter can be disabled (see Table 74 for more information). The same filter settings are applied to the outputs of all three gyroscopes and all three accelerometers. Note that, if all filtering is disabled, the 3dB bandwidth of the sensor is specified in Table 1.

CALIBRATION

The inertial sensor calibration function for the gyroscopes and the accelerometers has two components: factory calibration and user calibration.

The factory calibration of the gyroscope applies the following correction formulas to the data of each gyroscope:

$$\begin{pmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{pmatrix} = \begin{pmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{pmatrix} \times \left(\begin{pmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{pmatrix} + \begin{pmatrix} b_X \\ b_Y \\ b_Z \end{pmatrix} \right) \quad (12)$$

where:
ω_{XC}, ω_{YC}, and ω_{ZC} are the gyroscope outputs (post calibration).
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} provide scale and alignment correction.
ω_X, ω_Y, and ω_Z are the gyroscope outputs (precalibration).
b_X, b_Y, and b_Z provide bias correction.

The correction factors previously listed come from direct observation of the response of each gyroscope at multiple temperatures over the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the one-time programmable (OTP) memory bank, but they are not available for observation or configuration.

The gyroscope BIAS registers (XG_BIAS, YG_BIAS, ZG_BIAS) provide the user-configurable option for calibration of the gyroscopes. See the Gyroscope Bias Calibration section for more details.

The factory calibration of the accelerometer applies the following correction formulas to the data of each accelerometer:

$$\begin{pmatrix} a_{XC} \\ a_{YC} \\ a_{ZC} \end{pmatrix} = \begin{pmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{pmatrix} \times \left(\begin{pmatrix} a_X \\ a_Y \\ a_Z \end{pmatrix} + \begin{pmatrix} b_X \\ b_Y \\ b_Z \end{pmatrix} \right) \quad (13)$$

where:
a_{XC}, a_{YC}, and a_{ZC} are the accelerometer outputs (post calibration).
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} provide scale and alignment correction.
a_X, a_Y, and a_Z are the accelerometer outputs (precalibration).
b_X, b_Y, and b_Z provide bias correction.

The correction factors previously listed come from direct observation of the response of each accelerometer at multiple temperatures, over the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the OTP memory bank; however, these factors are not available for observation or configuration.

The accelerometer BIAS registers (XA_BIAS, YA_BIAS, ZA_BIAS) provide the user-configurable option for calibration of the accelerometers. See the Accelerometer Bias Calibration section for more details.

DECIMATION FILTER

The decimation filter averages multiple samples together to produce each downsampled register update. The number of samples in the average, D, is equal to the reduction in the update rate (f_{ODR}) for the output data registers (see Figure 30). The DEC_RATE register (see the Decimation Rate Register section) provides the configuration controls for this filter (D = DEC_RATE + 1). Decimation can be applied in internal clock mode, direct input sync mode, or scaled sync mode. In internal clock mode, $f_{ODR} = f_S/D$. In direct input or scaled sync mode, decimation is performed on synchronized samples from the output linear interpolator, such that $f_{ODR} = f_{SYNC}/D$ (direct) or $f_{ODR} = f_{SYNC} \times K_{ECSF}/D$ (scaled).

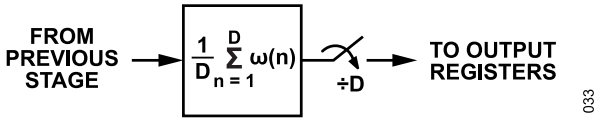


Figure 30. Decimating Filter Diagram

THEORY OF OPERATION

LATENCY

Table 11 contains the latency for each inertial sensor when the ADIS16607 is operating in internal clock mode with decimation disabled.

Table 11. Signal Path Latency in Internal Clock Mode

Delay Contribution	Accelerometer (ms)	Gyroscope (ms)
Analog Filter Delay	0.166	0.126
IIR Filter Group Delay	See Table 12	See Table 12
Processing Delay	0.064	0.064
Total Latency (FILT_BW = 0b00)	0.28	0.24

Table 12. IIR Filter Group Delay

FILT_BW	Group Delay (ms)
0b00	0.05
0b01	0.54
0b10	2.75
0b11	13.34

In this context, latency represents the time between the motion (linear acceleration and/or angular rate of rotation) and the time that the representative data is available in the output data register. In internal clock mode, each DR pulse indicates the output data corresponding to the motion that occurred Δt_{TOTAL} prior to the DR pulse, where Δt_{TOTAL} is the sum of the analog filter delay, IIR filter group delay, and processing delay in Table 11. In scaled sync mode, the output data corresponds to the motion that occurred $\Delta t_{MOTION\ TO\ SYNC}$ before the interpolation time recorded in the TIMESTAMP register (see the Timestamp Data Register section), where $\Delta t_{MOTION\ TO\ SYNC}$ is the sum of the analog filter delay and the IIR filter group delay in Table 11. Note that both the processing delay and IIR filter group delay are inversely proportional to the internal conversion rate, f_S. The delay values in Table 11 and Table 12 are for typical f_S, as specified in Table 1.

When the DEC_RATE register is not equal to 0, the decimation filter contributes additional group delay of (D + 1)/2 sample periods to the total latency.

Data Acquisition

The signal path latency detailed in Table 11 does not include data acquisition latency, which represents the time it takes the system processor to read the data from the output registers of the ADIS16607. The latency of the serial communications depends on the reading mode and SCLK speed.

REGISTER STRUCTURE

All communication between the ADIS16607 and an external processor involves either reading the contents of an output register or writing configuration and command information to a control register. The output data registers include the latest sensor data, error flags, and identification information. The control registers include sample rate, filtering, calibration, and diagnostic options. Each user-accessible register has 16 bits. See the Register Map Summary section for a detailed list of the user registers, along with their addresses.

DATA READY (DR)

The user must configure the GPIO3 pins for the DR function. When a GPIO3 pin is configured for the DR function, that pin pulses when the output data registers are updating. Connect the GPIO3 pin to an input pin on the embedded processor and configure this pin to trigger data collection on the falling edge of the pulse on the GPIO3. The USER_GPIO_CFG1 register controls the function of the GPIO pins.

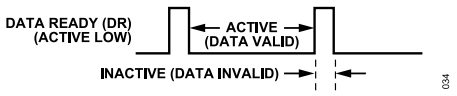


Figure 31. DR Signal

SPI COMMUNICATION PROTOCOL

SPI PORT CONNECTIONS

Figure 32 shows the most common connections between the ADIS16607 and a SPI controller device, which is often an embedded processor that is SPI compatible. In the example shown in Figure 32, the SPI controller uses an interrupt service routine to collect data every time the DR signal pulses. The user must configure GPIO3 for the DR function. Additional information on SPI usage can be found in the Applications Information section.

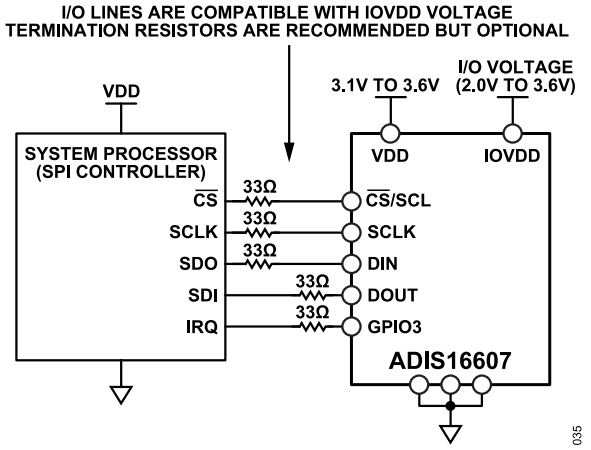


Figure 32. Electrical Connection Diagram (In This Configuration, GPIO3 Is Configured as DR)

Table 13 provides an example list of pin names for the SPI port in an embedded processor.

Table 13. Generic SPI Controller Pin Names and Functions

Mnemonic	Function
$\overline{CS}$	Chip select
SCLK	Serial clock
SDO	Serial data output
SDI	Serial data input
IRQ	Interrupt request

Embedded processors typically configure their serial ports for communicating with devices such as the ADIS16607 by using control registers on the processor itself. Table 14 lists the SPI protocol settings for the ADIS16607.

Table 14. Generic SPI Controller Settings

Processor Setting	Description
Controller	ADIS16607 operates as a peripheral
SCLK ≤ f_{SCLK}	Serial clock rate (10MHz maximum)
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence
16-Bit Mode	Shift register and data length

SUPPORTED OPERATING MODES

The supported operating modes of the ADIS16607 are the following:

- Full-duplex, 4-wire with cyclic redundancy check (CRC); autoincrement is not supported
- Half-duplex, 4-wire without CRC; autoincrement and burst reads (see the Burst Read Function section) are supported by leaving the $\overline{CS}$ pin low and reading additional registers

The SPI controller must lock the ADIS16607 to either full-duplex mode or half-duplex mode during initialization by writing to the SPI_FULLDUPLEX_KEY or SPI_HALFDUPLEX_KEY register as the first SPI command (see the IMU Initialization section for detailed examples). Once locked, the ADIS16607 can only support transactions formatted according to the selected mode. Note that switching SPI modes after initial locking is also supported via writes to the SPI_FULLDUPLEX_KEY or SPI_HALFDUPLEX_KEY register.

SPI Full-Duplex Mode with CRC

A full-duplex controller must lock the IMU to full-duplex mode by writing 0xB3B3 to the SPI_FULLDUPLEX_KEY register at Address 0x0031. Writing this value also resets the SPI_HALFDUPLEX_KEY register at Address 0x0032.

The transaction length for full-duplex mode is 32-bits. The ADIS16607 receives commands on DIN during one 32-bit frame and transmits the associated response on DOUT during the following 32-bit frame. Therefore, the ADIS16607 can receive requests on DIN while simultaneously transmitting data corresponding to the previous request on DOUT (see Figure 33). Burst reads and writes are not possible on SPI full duplex.

Safety features of SPI full-duplex mode include the following:

- CRC4 on DIN
- State vector, transaction counter, and CRC4 on DOUT

For SPI writes, DIN provides the 16-bit data to be written (D[15:0]), along with the address of the register to be written (A[6:0]). The ADIS16607 performs a readback after writing to the register and transmits the results as D[15:0] of DOUT in the following transaction frame.

For SPI reads, the address field of DIN (A[6:0]) specifies the address of the register to be read. After receiving the read command frame, the ADIS16607 transmits the requested register value as D[15:0] of DOUT in the following transaction frame.

SPI COMMUNICATION PROTOCOL

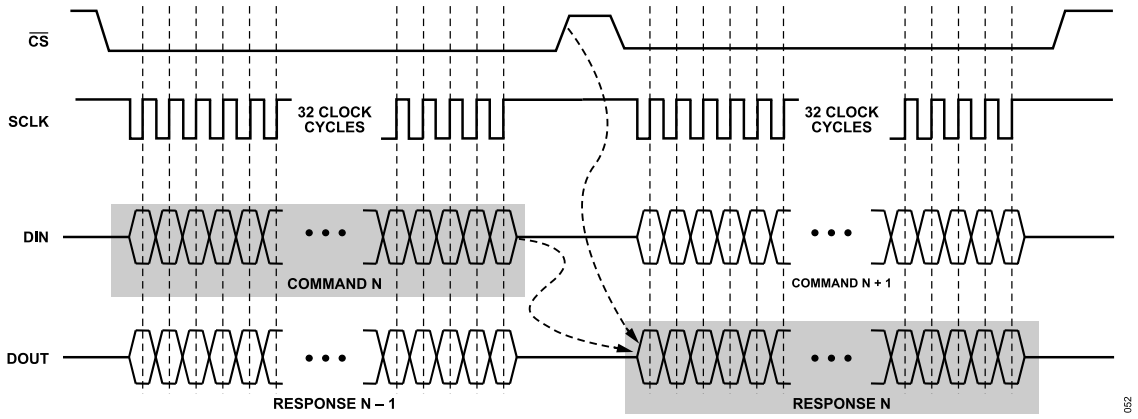


Figure 33. Full-Duplex SPI Transactions

Table 15. SPI Command and Response Format in Full Duplex with CRC Mode

Command	Bits															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIN	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DOUT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 16. Continuation of SPI Command and Response Format in Full Duplex with CRC Mode

Command	Bits															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	0	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$	NE	NE	NE	CRC3	CRC2	CRC1	CRC0
DOUT	0	A6	A5	A4	A3	A2	A1	A0	SV1	SV0	TC1	TC0	CRC3	CRC2	CRC1	CRC0

Table 17. Full-Duplex DIN Response Bit Definitions

Bit Name	Position	Description	Definition
D[15:0]	31 … 16	Data field	Write command: The 16-bit data field contains the data to be written to the register addressed in Bits A[6:0]. Read command: no function, contents are ignored.
0	15	Zero	Must always be zero.
A[6:0]	14 … 8	Address field	The address of the register to be written to or read from.
R/$\overline{W}$	7	Read/write	Differentiates the DIN command as either read or write. 0: read. 1: write.
NE	6 ... 4	No effect	These bits can have any value. Note that they are included in the CRC calculation.
CRC[3:0]	3 … 0	Cyclic redundancy check	4-bit CRC check. See the CRC4 section for more information. Polynomial: $x^4 + 1$. Seed value: 1010. Calculation order: MSB to LSB. The CRC calculation includes Bits[31:4] of the DIN command.

SPI COMMUNICATION PROTOCOL

Table 18. Full-Duplex DOUT Response Bit Definitions

Bit Name	Position	Description	Definition
D[15:0]	31 … 16	Data field	The 16-bit data field contains the data from the register addressed in Bits A[6:0] of the previous DIN command frame.
0	15	Zero	Must always be zero.
A[6:0]	14 … 8	Address field	Contains the address associated with the data in D[15:0]. The system can compare this value to the address issued in the previous DIN command to ensure data integrity.
SV[1:0]	7, 6	State vector	Indicates the condition of the ADIS16607 at the time data is issued. See the State Vector section for more information. 00: Incomplete Initialization (bootloader active). 01: Run phase—device OK (DEV_OK). 10: Run phase—DEV_NOK. 11: SPI error.
TC[1:0]	5, 4	Transaction counter	A 2-bit rollover counter that is incremented when the transmitted data is fresher than the previously transmitted data. See the Transaction Counter section for more information.
CRC[3:0]	3 … 0	Cyclic redundancy check	4-bit CRC check. See the CRC4 section for more information. Polynomial: $x^4 + 1$. Seed value: 1010. Calculation order: MSB to LSB. The CRC calculation includes Bits[31:4] of the DOUT response.

SPI COMMUNICATION PROTOCOL

SPI Half-Duplex Mode

A half-duplex controller must lock the IMU to half-duplex mode by writing 0xB4B4 to the SPI_HALFDUPLEX_KEY register at Address 0x0032. Writing this value also resets the SPI_FULLDUPLEX_KEY register at Address 0x0031.

In half-duplex mode, DOUT is always high impedance while DIN is active, and the DIN bits are ignored while DOUT is driving data. Responses to read commands are transmitted during the same frame.

SPI writes are structured as 24-bit frames, where DIN provides the address of the register to be written (A[6:0]), followed by the 16-bit data to be written (D[15:0]). No response is provided on DOUT, which remains high impedance during the transaction.

SPI reads are structured as 32-bit frames, where DIN provides the address of the register to be read (A[6:0]), and the ADIS16607 provides the requested register contents on DOUT (D[15:0]) in the second half of the frame.

Burst reads are also supported when the ADIS16607 is locked to SPI half-duplex mode, see the Burst Read Function section for more information.

Table 19. SPI Write Command and Response Format in Half-Duplex, 4-Wire Without CRC Mode

	Bit																							
Command	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DIN	0	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DOUT	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ

Table 20. Half-Duplex SPI Write DIN Command Bit Definitions

Bit Name	Position	Description	Definition
R/W	23	Read/write	Differentiates the DIN command as either read or write. Use 0 for write commands.
A[6:0]	22 … 16	Address field	Defines the address of the register to which data is written.
D[15:0]	15 … 0	Data field	Contains the data to be written to the register specified in A[6:0].

Table 21. SPI Read Command and Response Format in Half-Duplex, 4-Wire Without CRC Mode

	Bit															
Command	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DIN	1	A6	A5	A4	A3	A2	A1	A0	NE	NE	NE	NE	NE	NE	NE	NE
DOUT	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	S7	S6	S5	S4	S3	S2	S1	S0

Table 22. Continuation of SPI Read Command and Response Format in Half-Duplex, 4-Wire Without CRC Mode

	Bit															
Command	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DIN	NE	NE	NE	NE	NE	NE	NE	NE	NE	NE	NE	NE	NE	NE	NE	NE
DOUT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 23. Half-Duplex SPI Read DIN Command Bit Definitions

Bit Name	Position	Description	Definition
R/W	31	Read/write	Differentiates the DIN command as either read or write. Use 1 for read commands.
A[6:0]	30 … 24	Address field	Defines the address of the register from which data is read.
NE	23 … 0	No effect	These bit values have no effect.

Table 24. Half-Duplex SPI Read DOUT Response Bit Definitions

Bit Name	Position	Description	Definition
HZ	31 … 24	High impedance	Undriven bits.

SPI COMMUNICATION PROTOCOL

Table 24. Half-Duplex SPI Read DOUT Response Bit Definitions (Continued)

Bit Name	Position	Description	Definition
S[7:0]	23 … 16	Status field	Status bits. Bit 7: reads 1 if bootloader busy, or write lock disabled. Bit 6: reads 1 if fault detected. Bits[5:0]: unused, always read 0.
D[15:0]	15 … 0	Data field	The 16-bit data field contains the data from the register addressed in Bits A[6:0] of the issued DIN command.

CRC4

In full-duplex mode, a 4-bit CRC must be calculated for all DIN commands sent to the ADIS16607. If the CRC is not properly calculated in the DIN command, the resulting DOUT response indicates an SPI error (SV[1:0] = 11), and the write command is blocked. The CRC is necessary to ensure the integrity of the command received by the ADIS16607.

The DOUT response also contains a 4-bit CRC calculated with the same polynomial and seed value used for the DIN command. For safety critical applications, it is strongly recommended that the controller validate the DOUT CRC before applying the inertial data to any system level algorithms.

State Vector

In full-duplex mode, the state vector is implemented as a method for communicating the state of the ADIS16607 as it relates to the data stored in D[15:0] of the DOUT response.

Table 25. State Vector

SV[1:0]	ADIS16607 State
00	Incomplete Initialization (bootloader active)
01	Run phase—DEV_OK
10	Run phase—DEV_NOK
11	SPI error

The initialization phase is the default state of ADIS16607 at the conclusion of its reset release routine. During the initialization phase, the bootloader configures the controller memories and appropriate registers. Because these operations have the capability to affect the inertial data output, the ADIS16607 flags all SPI transactions conducted during this phase with SV[1:0] = 00. Inertial data acquired during the initialization phase must not be applied to any safety critical applications.

The user must set the WRITE_LOCK_STATUS bit (Bit 0 of the WRITE_LOCK register, Address 0x002D) after programming the ADIS16607 to use the SV bits. The state vector remains at the value 2'b00 if either the bootloader is busy or if the write lock bit is not set. Once the bootloader has fully run through the OTP contents and the write lock bit is set, the ADIS16607 moves to the run phase. If no error flag is raised, the state vector goes to 2'b01, and data is valid for any system algorithms, which represents the typical steady state operational phase of the ADIS16607. If a fault is present and detected, the state vector transitions to 2'b10. Data obtained during this phase can also be fully applied to any system algorithms.

SPI COMMUNICATION PROTOCOL

Transaction Counter

In full-duplex mode, a 2-bit transaction counter increments according to the following two criteria:

- The transmitted inertial data is fresh, meaning it occurs later in time than the previous DOUT response.
- A previous SPI transaction has been executed.

By linking these two events, the transaction counter provides coverage for two unique scenarios. First, linkage to the ADIS16607 internal clock oscillator is achieved through this implementation. Faults that can result in the output data registers becoming frozen are immediately identified by the system because TC[1:0] ceases to increment. Second, inadvertent SPI commands cause unexpected increments to the TC[1:0] value, which are also immediately detected at the system level.

Figure 34 illustrates the events that lead to TC increments. The lower trace shows the DR signal, the upper trace shows the state of the $\overline{CS}$ signal, and the transaction counter associated with each $\overline{CS}$ is directly beneath the active portion of the $\overline{CS}$ trace. The upper group of transactions shows that the TC increments for each $\overline{CS}$ activation when $\overline{CS}$ is no faster than DR. Arrows trace back to the events and/or edges that trigger each increment. When TC = 0, the data and TC were determined when SPI data was latched at the end of the read request in the previous SPI communication (TC = 3). The SPI data that gets latched when TC = 3 is newer than the preceding communication because of the indicated DR signal that occurred prior to the latching of data. Consider the case when TC increments to 2, there are two DR events that occur before the SPI data is latched; however, TC increments by only one as previously described.

The lower group of transactions shows what happens when SPI is running faster than DR. When multiple SPI transactions occur between DR pulses, TC does not increment every time. Consider the read request occurring the second time TC = 3. When the read request is parsed and executed as $\overline{CS}$ goes high, SPI data for the response is latched and it is known that the latched data is newer than the previous transaction because a DR pulse has occurred. The incremented TC = 0 is communicated out as another read request is parsed and more SPI data is latched. Notice that a DR pulse did not occur prior to this request, the TC is not incremented, and a second TC = 0 is communicated on the subsequent transaction.

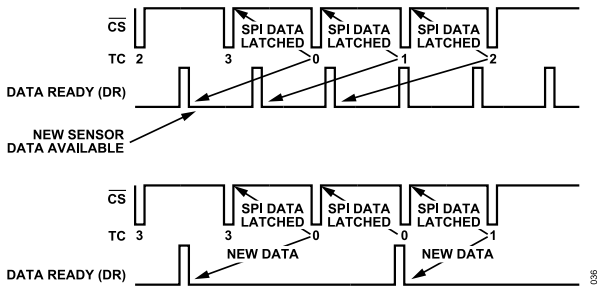


Figure 34. Edges That Trigger TC Increments

Figure 35 shows the behavior of the transaction counter when the chip select rate is appreciably faster relative to the data update rate. It is important to note that in full-duplex mode, inertial data is latched on the rising edge of the chip select pin, $\overline{CS}$. Figure 35 shows that the transaction counter only increments when the rising edge of $\overline{CS}$ occurs after a new data update event so that the next sequential response contains a fresh sample of data.

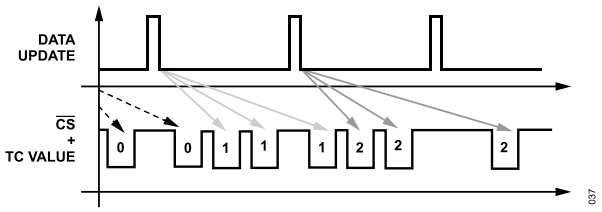


Figure 35. Transaction Counter (TC)—Fast $\overline{CS}$ Rate

The behavior presented in Figure 36 is expected for systems where the chip select rate is much slower than the data update rate. As each rising edge of the $\overline{CS}$ signal occurs after an internal data update event, the transaction counter updates sequentially with every new SPI exchange.

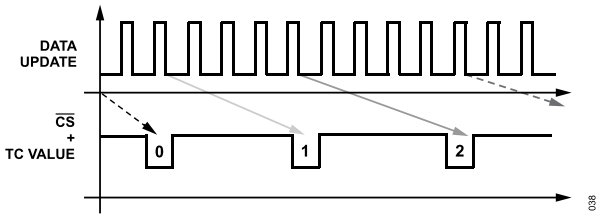


Figure 36. Transaction Counter (TC)—Slow $\overline{CS}$ Rate

SPI errors do not affect the behaviors shown in Figure 35 and Figure 36. Although the SPI command payload is not valid, the rising edge of $\overline{CS}$ is still used to latch new data into the SPI output registers. If fresh data is latched during this event, then the transaction counter updates accordingly. Inadvertent blips on the $\overline{CS}$ line are detected as they may induce an increment to the transaction counter.

I²C COMMUNICATION PROTOCOL

The ADIS16607 I²C interface conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, available from NXP Semiconductor.

The ADIS16607 supports fast mode (400kHz) and fast mode plus (up to 1MHz) data transfer modes when the bus parameters in Table 4 are met. There is no minimum SCL frequency, with the exception that, when reading data, the clock must be fast enough to read an entire sample set before new data overwrites it. Single-byte or multiple-byte reads and writes are supported.

There are four different I²C addresses that can be selected by tying the SCLK and DOUT pins to either VDD or GND, as shown in Table 26.

Table 26. I²C Device Address

DOUT	SCLK	Device Address
GND	GND	0x38
GND	VDD	0x39
VDD	GND	0x3A
VDD	VDD	0x3B

There are no internal pull-up or pull-down resistors for any unused pins. Therefore, there is no known state or default state for the pins if left floating or unconnected.

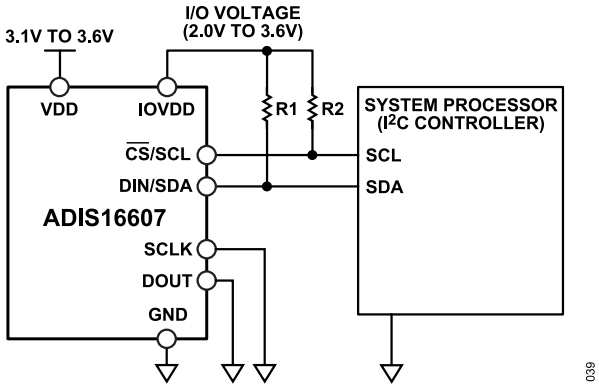


Figure 37. Typical I²C Connection Diagram (Address 0x38)

REGISTER MAP SUMMARY

Table 27. ADIS16607 Register Map Summary

Address	Name	Description	Default[1]	Access[1]
0x0000	DEV_ID	ADI MEMS ID.	0x6000	R
0x0001	REV_ID	Revision and Firmware ID.	Varies	R
0x0002	SERIAL_NUMBER_0	Serial Number 0.	Varies	R
0x0003	SERIAL_NUMBER_1	Serial Number 1.	Varies	R
0x0004	SERIAL_NUMBER_2	Serial Number 2.	Varies	R
0x0005	DIAG_STAT	Diagnostic Status Flags.	0x0000	R
0x0006	X_ACCEL_HIGH	X-Channel Accelerometer Data (High).	N/A	R
0x0007	X_ACCEL_LOW	X-Channel Accelerometer Data (Low).	N/A	R
0x0008	Y_ACCEL_HIGH	Y-Channel Accelerometer Data (High).	N/A	R
0x0009	Y_ACCEL_LOW	Y-Channel Accelerometer Data (Low).	N/A	R
0x000A	Z_ACCEL_HIGH	Z-Channel Accelerometer Data (High).	N/A	R
0x000B	Z_ACCEL_LOW	Z-Channel Accelerometer Data (Low).	N/A	R
0x000C	X_GYRO_HIGH	X-Channel Gyroscope Data (High).	N/A	R
0x000D	X_GYRO_LOW	X-Channel Gyroscope Data (Low).	N/A	R
0x000E	Y_GYRO_HIGH	Y-Channel Gyroscope Data (High).	N/A	R
0x000F	Y_GYRO_LOW	Y-Channel Gyroscope Data (Low).	N/A	R
0x0010	Z_GYRO_HIGH	Z-Channel Gyroscope Data (High).	N/A	R
0x0011	Z_GYRO_LOW	Z-Channel Gyroscope Data (Low).	N/A	R
0x0012	X_DELTVEL_HIGH	X-Channel Delta Velocity Data (High).	N/A	R
0x0013	X_DELTVEL_LOW	X-Channel Delta Velocity Data (Low).	N/A	R
0x0014	Y_DELTVEL_HIGH	Y-Channel Delta Velocity Data (High).	N/A	R
0x0015	Y_DELTVEL_LOW	Y-Channel Delta Velocity Data (Low).	N/A	R
0x0016	Z_DELTVEL_HIGH	Z-Channel Delta Velocity Data (High).	N/A	R
0x0017	Z_DELTVEL_LOW	Z-Channel Delta Velocity Data (Low).	N/A	R
0x0018	X_DELTANG_HIGH	X-Channel Delta Angle Data (High).	N/A	R
0x0019	X_DELTANG_LOW	X-Channel Delta Angle Data (Low).	N/A	R
0x001A	Y_DELTANG_HIGH	Y-Channel Delta Angle Data (High).	N/A	R
0x001B	Y_DELTANG_LOW	Y-Channel Delta Angle Data (Low).	N/A	R
0x001C	Z_DELTANG_HIGH	Z-Channel Delta Angle Data (High).	N/A	R
0x001D	Z_DELTANG_LOW	Z-Channel Delta Angle Data (Low).	N/A	R
0x001E	RESERVED	Reserved.	N/A	N/A
0x001F	RESERVED	Reserved.	N/A	N/A
0x0020	TEMP_OUT	Temperature Channel Data.	N/A	R
0x0021	TIME_STAMP	Timestamp Data.	N/A	R
0x0022	DATA_CNTR	Data Counter.	N/A	R
0x0023 to 0x0028	RESERVED	Reserved.	N/A	N/A
0x0029	FIFO_DATA	First-In, First-Out (FIFO) Data.	N/A	R
0x002A	FIFO_CH_INDEX	FIFO Channel Index.	N/A	R
0x002B	FIFO_WORD_CNT	FIFO Word Count.	N/A	R
0x002C	RESERVED	Reserved.	N/A	N/A
0x002D	WRITE_LOCK	Write Lock.	0x0000	R/W
0x002E	USER_BOOT	User Boot.	0x0000	R/W
0x002F	USER_GPIO_CFG1	User GPIO Configuration 1.	0x0009	R/W
0x0030	USER_GPIO_CFG2	User GPIO Configuration 2.	0x0002	R/W
0x0031	SPI_FULLDUPLEX_KEY	Enables Full-Duplex SPI.	0x0000	R/W
0x0032	SPI_HALFDUPLEX_KEY	Enables Half-Duplex SPI.	0x0000	R/W
0x0033	USER_SYNC	External Sync Configuration.	0x0000	R/W

REGISTER MAP SUMMARY

Table 27. ADIS16607 Register Map Summary (Continued)

Address	Name	Description	Default[1]	Access[1]
0x0034	USER_DATA_CFG	User Data Configurations.	0x1FFF	R/W
0x0035	USER_FIFO_CFG	FIFO Configuration.	0x0000	R/W
0x0036	SOFT_RESET	Software Reset.	0x0000	R/W
0x0038	RESERVED	Reserved.	N/A	N/A
0x0039	MSC_CTRL	User Offset Configuration.	0x0000	R/W
0x003A	DEC_RATE	Decimation Rate.	0x0000	R/W
0x003B	XA_BIAS	Accelerometer X Offset.	0x0000	R/W
0x003C	YA_BIAS	Accelerometer Y Offset.	0x0000	R/W
0x003D	ZA_BIAS	Accelerometer Z Offset.	0x0000	R/W
0x003E	XG_BIAS	Gyroscope X Offset.	0x0000	R/W
0x003F	YG_BIAS	Gyroscope Y Offset.	0x0000	R/W
0x0040	ZG_BIAS	Gyroscope Z Offset.	0x0000	R/W
0x0041	MODEL_ID	Model Identification.	Varies	R
0x0042 to 0x004D	RESERVED	Reserved.	N/A	N/A
0x004E	DIGITAL_STATUS	Digital Status Register.	0x0000	R

[1] N/A stands for not applicable.

USER REGISTER DEFINITIONS

PART IDENTIFICATION

Address 0x0000 to Address 0x0004 contain the ADIS16607 part identification registers.

ADI MEMS ID REGISTER

Address: 0x0000, Default: 0x6000, Name: DEV_ID

Table 28. Bit Descriptions for DEV_ID

Bits	Bit Name	Description	Default	Access
[15:0]	DEV_ID	ADI ID Register.	0x6000	R

REV ID REGISTER

Address: 0x0001, Default: Varies, Name: REV_ID

Table 29. Bit Descriptions for REV_ID

Bits	Bit Name	Description	Default	Access
[15:8]	FIRMWARE_ID	ADI Firmware Revision ID.	Varies	R
[7:0]	REV_ID	ADI Revision ID.	Varies	R

SERIAL NUMBER 0 REGISTER

Address: 0x0002, Default: Varies, Name: SERIAL_NUMBER_0

Table 30. Bit Descriptions for SERIAL_NUMBER_0

Bits	Bit Name	Description	Default	Access
[15:0]	SERIAL_NUMBER[15:0]	ADI Serial Number.	Varies	R

SERIAL NUMBER 1 REGISTER

Address: 0x0003, Default: Varies, Name: SERIAL_NUMBER_1

Table 31. Bit Descriptions for SERIAL_NUMBER_1

Bits	Bit Name	Description	Default	Access
[15:0]	SERIAL_NUMBER[31:16]	ADI Serial Number.	Varies	R

SERIAL NUMBER 2 REGISTER

Address: 0x0004, Default: 0x0000, Name: SERIAL_NUMBER_2

Table 32. Bit Descriptions for SERIAL_NUMBER_2

Bits	Bit Name	Description	Default	Access
[15:0]	SERIAL_NUMBER[47:32]	ADI Serial Number.	Varies	R

USER REGISTER DEFINITIONS

DIAG_STAT REGISTER

Address: 0x0005, Default: 0x0000, Name: DIAG_STAT

These bits are cleared when read.

Table 33. Bit Descriptions for DIAG_STAT

Bits	Bit Name	Description	Default	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	FAULT_GYRO	Gyroscope Fault. The gyroscope sensor has been disabled.	0x0	R
12	FAULT_XL	Accelerometer Overload and Fault. The accelerometer has been disabled.	0x0	R
11	FAULT_PWR	Fault in Any of the Power Supplies.	0x0	R
10	FAULT_DIGITAL	Digital Faults.	0x0	R
9	FAULT_BL	Bootloader Fault.	0x0	R
8	FAULT_FW	Firmware Faults.	0x0	R
[7:3]	RESERVED	Reserved.	0x0	R
2	SYNC_LOST	Digital phase-locked loop (PLL) has lost its sync input.	0x0	R
1	DPLL_UNLOCKED	Status of the DPLL.	0x0	R
0	FIFO_THRESH_MET	FIFO Threshold Met. 1 Indicates that the FIFO contains at least the desired number of samples, as set in FIFO_THRESHOLD.	0x0	R

USER REGISTER DEFINITIONS

ACCELEROMETER DATA

The accelerometers in the ADIS16607 measure both dynamic and static (response to gravity) acceleration along the same three orthogonal axes that define the axes of rotation for the gyroscopes (x, y, and z). Figure 38 shows the orientation of each accelerometer axis along with the direction of acceleration that produces a positive response in each of their measurements.

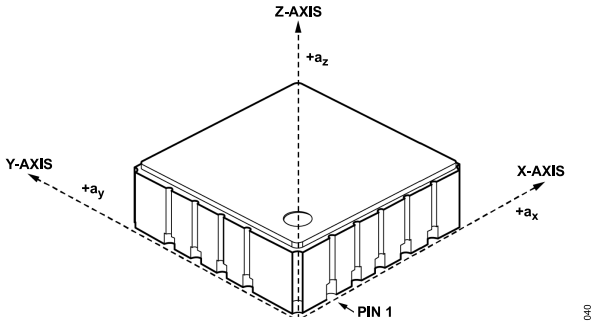


Figure 38. Accelerometer Axis and Polarity Assignments

Each accelerometer has two output data registers. Figure 39 shows how these two registers combine to support a 24-bit, left-justified, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y-axis and z-axis. Note that only the 16-bit values in the high registers are significant if the user is not using decimation or filtering. The upper 8 bits in the low registers are for bit growth while using filtering and decimation, and the lower 8 bits in the low registers are not used and are always zero.

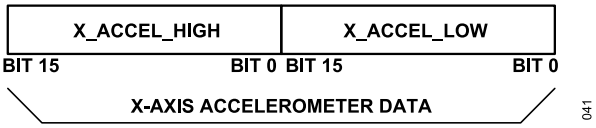


Figure 39. Accelerometer Output Data Structure

X-CHANNEL ACCELEROMETER DATA (HIGH) REGISTER

Address: 0x0006, Default: N/A, Name: X_ACCEL_HIGH

Table 34. Bit Descriptions for X_ACCEL_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	X_ACCEL_HIGH	X-Axis Accelerometer Output.	N/A	R

X-CHANNEL ACCELEROMETER DATA (LOW) REGISTER

Address: 0x0007, Default: N/A, Name: X_ACCEL_LOW

Table 35. Bit Descriptions for X_ACCEL_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	X_ACCEL_LOW	X-Axis Accelerometer Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

Y-CHANNEL ACCELEROMETER DATA (HIGH) REGISTER

Address: 0x0008, Default: N/A, Name: Y_ACCEL_HIGH

Table 36. Bit Descriptions for Y_ACCEL_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	Y_ACCEL_HIGH	Y-Axis Accelerometer Output.	N/A	R

USER REGISTER DEFINITIONS

Y-CHANNEL ACCELEROMETER DATA (LOW) REGISTER

Address: 0x0009, Default: N/A, Name: Y_ACCEL_LOW

Table 37. Bit Descriptions for Y_ACCEL_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	Y_ACCEL_LOW	Y-Axis Accelerometer Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

Z-CHANNEL ACCELEROMETER DATA (HIGH) REGISTER

Address: 0x000A, Default: N/A, Name: Z_ACCEL_HIGH

Table 38. Bit Descriptions for Z_ACCEL_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	Z_ACCEL_HIGH	Z-Axis Accelerometer Output.	N/A	R

Z-CHANNEL ACCELEROMETER DATA (LOW) REGISTER

Address: 0x000B, Default: N/A, Name: Z_ACCEL_LOW

Table 39. Bit Descriptions for Z_ACCEL_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	Z_ACCEL_LOW	Z-Axis Accelerometer Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

USER REGISTER DEFINITIONS

GYROSCOPE DATA

The gyroscopes in the ADIS16607 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 40 shows the orientation of each gyroscope axis along with the direction of rotation that produces a positive response in each of their measurements.

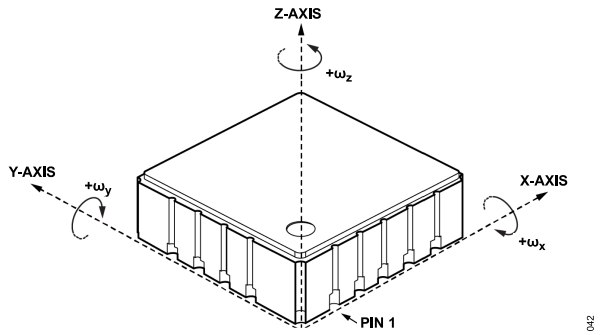


Figure 40. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 41 shows how these two registers combine to support a 24-bit, left-justified, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y-axis and z-axis. Note that only the 16-bit values in the high registers are significant if the user is not using decimation or filtering. The upper 8 bits in the low registers are for bit growth while using filtering and decimation, and the lower 8 bits in the low registers are not used and are always zero.

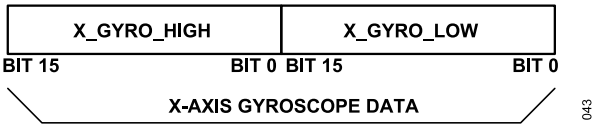


Figure 41. Gyroscope Output Data Structure

X-CHANNEL GYROSCOPE DATA (HIGH) REGISTER

Address: 0x000C, Default: N/A, Name: X_GYRO_HIGH

Table 40. Bit Descriptions for X_GYRO_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	X_GYRO_HIGH	X-Axis Gyroscope Output.	N/A	R

X-CHANNEL GYROSCOPE DATA (LOW) REGISTER

Address: 0x000D, Default: N/A, Name: X_GYRO_LOW

Table 41. Bit Descriptions for X_GYRO_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	X_GYRO_LOW	X-Axis Gyroscope Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

Y-CHANNEL GYROSCOPE DATA (HIGH) REGISTER

Address: 0x000E, Default: N/A, Name: Y_GYRO_HIGH

Table 42. Bit Descriptions for Y_GYRO_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	Y_GYRO_HIGH	Y-Axis Gyroscope Output.	N/A	R

Y-CHANNEL GYROSCOPE DATA (LOW) REGISTER

Address: 0x000F, Default: N/A, Name: Y_GYRO_LOW

Table 43. Bit Descriptions for Y_GYRO_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	Y_GYRO_LOW	Y-Axis Gyroscope Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

USER REGISTER DEFINITIONS

Z-CHANNEL GYROSCOPE DATA (HIGH) REGISTER

Address: 0x0010, Default: N/A, Name: Z_GYRO_HIGH

Table 44. Bit Descriptions for Z_GYRO_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	Z_GYRO_HIGH	Z-Axis Gyroscope Output.	N/A	R

Z-CHANNEL GYROSCOPE DATA (LOW) REGISTER

Address: 0x0011, Default: N/A, Name: Z_GYRO_LOW

Table 45. Bit Descriptions for Z_GYRO_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	Z_GYRO_LOW	Z-Axis Gyroscope Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

USER REGISTER DEFINITIONS

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16607 also provides delta velocity measurements that represent a calculation of linear velocity change between each sample update. The delta velocity axis and polarity with respect to the package orientation is shown the Figure 42.

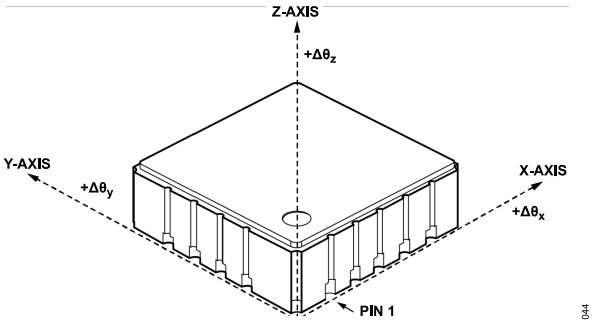


Figure 42. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V\left(\frac{m}{s}\right) = \sum_{d=0}^{D-1}\left(\frac{a_{x,d} + a_{x,d-1}}{2}\right)\Delta t \quad (14)$$

where:
D is the decimation rate (DEC_RATE+1).
a_x is the x-axis acceleration in m/sec^2.
d is the incremental variable in the summation formula.
Δt is the time between two consecutive samples. When using the internal sample clock, $\Delta t = 1/f_S$, where f_S is the internal conversion rate found in Table 1. In direct sync mode, $\Delta t = 1/f_{SYNC}$, and in scaled sync mode, $\Delta t = 1/(f_{SYNC} \times K_{ECSF})$.

The maximum delta velocity that can be measured is as follows:

$$\Delta V_{MAX} = a_{MAX} \times min(\Delta t, \Delta t_{MAX}) \times D \quad (15)$$

where:
a_{MAX} is the maximum acceleration the sensor can measure.
$\Delta t_{MAX} = 4/f_S$. Note that when using an external sync clock, delta velocity outputs are only valid if $\Delta t < \Delta t_{MAX}$.

Each axis of the delta velocity measurements has two output data registers. Figure 43 shows how these two registers combine to support 24-bit, left-justified, twos complement data format for the delta velocity measurements along the x-axis. This format also applies to the y-axis and z-axis.

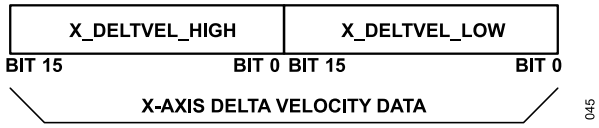


Figure 43. Delta Velocity Output Data Structure

To calculate the delta velocity scale use the following equation:

$$\Delta V_{SCALE}\left(\frac{m/sec}{LSB}\right) = XL_{SCALE}\left(\frac{g}{LSB}\right) \times 9.797464\left(\frac{m/sec^2}{g}\right) \times \frac{2^{13}}{f_S(Hz) \times 2304} \times D \quad (16)$$

where:
XL_{SCALE} is the accelerometer scale factor.
D the decimation rate (DEC_RATE + 1).
f_S is the internal conversion rate. For example, for the 24-bit data format (XL_{SCALE} = 1/200000 g/LSB), D = 1, and f_S = 9.75kHz, the ΔV_{SCALE} = 17.86 × 10^{-9}*m/sec*/LSB. f_S for any given device can be measured by observing the DR rate in internal sync mode (which is f_S/D).

X-CHANNEL DELTA VELOCITY DATA (HIGH) REGISTER

Address: 0x0012, Default: N/A, Name: X_DELTVEL_HIGH

Table 46. Bit Descriptions for X_DELTVEL_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	X_DELTVEL_HIGH	X-Axis Delta Velocity Output.	N/A	R

X-CHANNEL DELTA VELOCITY DATA (LOW) REGISTER

Address: 0x0013, Default: N/A, Name: X_DELTVEL_LOW

Table 47. Bit Descriptions for X_DELTVEL_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	X_DELTVEL_LOW	X-Axis Delta Velocity Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

USER REGISTER DEFINITIONS

Y-CHANNEL DELTA VELOCITY DATA (HIGH) REGISTER

Address: 0x0014, Default: N/A, Name: Y_DELTVEL_HIGH

Table 48. Bit Descriptions for Y_DELTVEL_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	Y_DELTVEL_HIGH	Y-Axis Delta Velocity Output.	N/A	R

Y-CHANNEL DELTA VELOCITY DATA (LOW) REGISTER

Address: 0x0015, Default: N/A, Name: Y_DELTVEL_LOW

Table 49. Bit Descriptions for Y_DELTVEL_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	Y_DELTVEL_LOW	Y-Axis Delta Velocity Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

Z-CHANNEL DELTA VELOCITY DATA (HIGH) REGISTER

Address: 0x0016, Default: N/A, Name: Z_DELTVEL_HIGH

Table 50. Bit Descriptions for Z_DELTVEL_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	Z_DELTVEL_HIGH	Z-Axis Delta Velocity Output.	N/A	R

Z-CHANNEL DELTA VELOCITY DATA (LOW) REGISTER

Address: 0x0017, Default: N/A, Name: Z_DELTVEL_LOW

Table 51. Bit Descriptions for Z_DELTVEL_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	Z_DELTVEL_LOW	Z-Axis Delta Velocity Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

USER REGISTER DEFINITIONS

DELTA ANGLES

The ADIS16607 also provides delta angle measurements that represent the computation of angular displacement between each sample update. The delta angle axis and polarity with respect to the package orientation is shown the Figure 44.

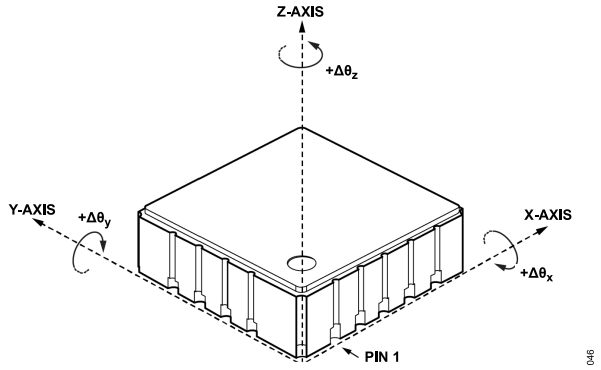


Figure 44. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta(^\circ) = \sum_{d=0}^{D-1}\left(\frac{\omega_{x,d}+\omega_{x,d-1}}{2}\right)\Delta t \quad (17)$$

where:
D is the decimation rate (DEC_RATE + 1).
ω_x is the x-axis rate of rotation in degrees per second.
d is the incremental variable in the summation formula.
Δt is the time between two consecutive samples before decimation. When using the internal sample clock, $\Delta t = 1/f_S$, where f_S is the internal conversion rate found in Table 1. In direct sync mode, $\Delta t = 1/f_{SYNC}$, and in scaled sync mode, $\Delta t = 1/(f_{SYNC} \times K_{ECSF})$.

Use the following equation to measure the maximum delta angle:

$$\Delta\theta_{max} = \omega_{max} \times min(\Delta t, \Delta t_{max}) \times D \quad (18)$$

where:
ω_{max} is the maximum rate of rotation the gyroscope can measure.
$\Delta t_{max} = 4/f_S$. Note that when using an external sync clock, delta angle outputs are only valid if $\Delta t < \Delta t_{max}$.

Each axis of the delta angle measurements has two output data registers. Figure 45 shows how these two registers combine to support 24-bit, left-justified, twos complement data format for the delta angle measurements about the x-axis. This format also applies to the y-axis and z-axis.

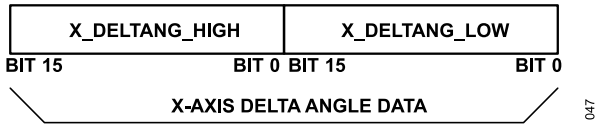


Figure 45. Delta Angle Output Data Structure

To calculate the delta angle scale use the following equation:

$$\Delta\theta_{SCALE}\left(\frac{^\circ}{LSB}\right) = Gyro_{SCALE}\left(\frac{^\circ/sec}{LSB}\right) \times \frac{2^{13}}{f_S(Hz) \times 2304} \times D \quad (19)$$

where:
$Gyro_{SCALE}$ is the gyroscope scale factor.
D the decimation rate (DEC_RATE + 1).
f_S is the internal conversion rate. For example, for the ±2000°/s range, 24-bit data format ($Gyro_{SCALE}$= 1/4000dps/LSB), D = 1, and f_S = 9.75kHz, the $\Delta\theta_{SCALE}$= = 91.17 × 10^{-9}°/LSB. f_S for any given part can be measured by observing the DR rate in internal sync mode (which is f_S/D).

X-CHANNEL DELTA ANGLE DATA (HIGH) REGISTER

Address: 0x0018, Default: N/A, Name: X_DELTANG_HIGH

Table 52. Bit Descriptions for X_DELTANG_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	X_DELTANG_HIGH	X-Axis Delta Angle Output.	N/A	R

X-CHANNEL DELTA ANGLE DATA (LOW) REGISTER

Address: 0x0019, Default: N/A, Name: X_DELTANG_LOW

Table 53. Bit Descriptions for X_DELTANG_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	X_DELTANG_LOW	X-Axis Delta Angle Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

USER REGISTER DEFINITIONS

Y-CHANNEL DELTA ANGLE DATA (HIGH) REGISTER

Address: 0x001A, Default: N/A, Name: Y_DELTANG_HIGH

Table 54. Bit Descriptions for Y_DELTANG_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	Y_DELTANG_HIGH	Y-Axis Delta Angle Output.	N/A	R

Y-CHANNEL DELTA ANGLE DATA (LOW) REGISTER

Address: 0x001B, Default: N/A, Name: Y_DELTANG_LOW

Table 55. Bit Descriptions for Y_DELTANG_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	Y_DELTANG_LOW	Y-Axis Delta Angle Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

Z-CHANNEL DELTA ANGLE DATA (HIGH) REGISTER

Address: 0x001C, Default: N/A, Name: Z_DELTANG_HIGH

Table 56. Bit Descriptions for Z_DELTANG_HIGH

Bits	Bit Name	Description	Default	Access
[15:0]	Z_DELTANG_HIGH	Z-Axis Delta Angle Output.	N/A	R

Z-CHANNEL DELTA ANGLE DATA (LOW) REGISTER

Address: 0x001D, Default: N/A, Name: Z_DELTANG_LOW

Table 57. Bit Descriptions for Z_DELTANG_LOW

Bits	Bit Name	Description	Default	Access
[15:0]	Z_DELTANG_LOW	Z-Axis Delta Angle Output Extended. These bits are additional resolution bits to avoid roundoff errors during decimation and filtering. Bits[7:0] are always zero.	N/A	R

TEMPERATURE SENSOR DATA REGISTER

Address: 0x0020, Default: N/A, Name: TEMP_OUT

Table 58. Bit Descriptions for TEMP_OUT

Bits	Bit Name	Description	Default	Access
[15:0]	TEMP_OUT	Temperature Read Back Value. This register provides the output of the temperature sensor inside the ADIS16607. This sensor is the most useful for monitoring relative changes in the thermal environment. The data is structured as twos complement, with 1 LSB = 0.005°C. Therefore, the formula to convert this register data to temperature follows: $\mathrm{T}(^{\circ}C) = \frac{TWOS_COMPLEMENT(TEMP_OUT(LSB))}{200(LSB/^{\circ}C)} + \mathrm{Offset}(^{\circ}C)$ where the offset is typically 25°C; however, it can vary device to device.	N/A	R

USER REGISTER DEFINITIONS

TIMESTAMP DATA REGISTER

Address: 0x0021, Default: N/A, Name: TIME_STAMP

Table 59. Bit Descriptions for TIME_STAMP

Bits	Bit Name	Description	Default	Access
[15:0]	TIME_STAMP	Timestamp Value Used in Scaled Sync Mode. Time from the rising edge of the last external pulse on the SYNC pin to the interpolation edge used to generate the output data sample; offset binary format. The formula to convert the register value to seconds is as follows: $\Delta t_{TIME_STAMP}(sec) = \frac{1024}{f_S(Hz) \times 2304} \times TIME_STAMP(LSB)$ where f_S is the internal conversion rate in the Specifications section. For example, using the typical f_S = 9.75kHz, 1 LSB = 45.6µs. The timestamp value resets to zero after every external sync pulse. As another example, if f_{SYNC} = 100Hz and K_{ECSF} = 70, the timestamp sequence is: 0 LSB, 3 LSB, 6 LSB … 216 LSB. If the decimation filter is enabled, the TIME_STAMP contains the time associated with the last sample in each data update.	N/A	R

DATA COUNTER REGISTER

Address: 0x0022, Default: N/A, Name: DATA_CNTR

Table 60. Bit Descriptions for DATA_CNTR

Bits	Bit Name	Description	Default	Access
[15:0]	DATA_CNTR	Data Update Counter, Offset Binary Format. When the ADIS16607 goes through its power-on sequence or when it recovers from a reset command, DATA_CNTR starts with a value of 0x0000 and increments every time new data loads into the output registers. When the DATA_CNTR value reaches 0xFFFF, the next data update causes it to wrap back around to 0x0000 where it continues to increment every time new data loads into the output registers. The rate that this occurs is the IMU sample rate divided by the decimation rate.	N/A	R

FIFO DATA REGISTER

Address: 0x0029, Default: N/A, Name: FIFO_DATA

Table 61. Bit Descriptions for FIFO_DATA

Bits	Bit Name	Description	Default	Access
[15:0]	FIFO_DATA	FIFO Data. This register contains data in the FIFO to be read by the user.	N/A	R

FIFO CHANNEL INDEX REGISTER

Address: 0x002A, Default: N/A, Name: FIFO_CH_INDEX

Table 62. Bit Descriptions for FIFO_CH_INDEX

Bits	Bit Name	Description	Default	Access
[15:7]	RESERVED	Reserved.	N/A	R
[6:0]	FIFO_CH_INDEX	FIFO Channel Index. These bits indicates which output channel was last read from the FIFO. See Table 85.	N/A	R

FIFO WORD COUNT REGISTER

Address: 0x002B, Default: N/A, Name: FIFO_WORD_CNT

Table 63. Bit Descriptions for FIFO_WORD_CNT

Bits	Bit Name	Description	Default	Access
[15:11]	RESERVED	Reserved.	N/A	R
[10:0]	FIFO_WORD_COUNT	Number of Words Currently Stored in the FIFO.	N/A	R

USER REGISTER DEFINITIONS

WRITE LOCK REGISTER

This register allows the user to disables SPI writes to the register map. Write 0x5555 and then 0xAAAA to the WRITE_LOCK address to lock writes to the configuration registers of the ADIS16607. Note that when this is set to lock that even the software reset command does not respond. Write 0xAAAA and then 0x5555 to unlock it.

Address: 0x002D, Default: 0x0000, Name: WRITE_LOCK

Table 64. Bit Descriptions for WRITE_LOCK

Bits	Bit Name	Description	Default	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	WRITE_LOCK_STATUS	Write Lock Status. This bit reads 1 when SPI write is locked.	0x0	R/W

USER BOOT REGISTER

Address: 0x002E, Default: 0x0000, Name: USER_BOOT

Table 65. Bit Descriptions for USER_BOOT

Bits	Bit Name	Description	Default	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	NVM_LOAD	Nonvolatile Memory (NVM) Load. When set to 1, this bit triggers self booting from the NVM.	0x0	R/W

USER GPIO CONFIGURATION REGISTER 1

Address: 0x002F, Default: 0x0009, Name: USER_GPIO_CFG1

Table 66. Bit Descriptions for USER_GPIO_CFG1

Bits	Bit Name	Description	Default	Access
15	RESERVED	Reserved.	0x0	R
[14:12]	CFG_GPIO_4	GPIO4 Pin Function Selection. These bits allow selecting of which function is applied to the GPIO4 pin. 000: idle. The GPIO is idle with a weak pull up. 001: DEV_NOK. The GPIO is asserted if any DIAG_STAT flag is nonzero; otherwise, the GPIO outputs low. 010: Reserved. 011: Reserved.	0x0	R/W
[11:9]	CFG_GPIO_3	GPIO3 Pin Function Selection. These bits allow selection of which function is applied to the GPIO3 pin. 000: idle. The GPIO is idle with a weak pull up. 001: DATA_RDY. The GPIO outputs the DR signal. 010: Reserved. 011: Reserved.	0x0	R/W
[8:6]	CFG_GPIO_2	GPIO2 Pin Function Selection. These bits allow selection of which function is applied to the GPIO2 pin. 000: idle. The GPIO is idle with a weak pull up. 001: sync. The GPIO accepts a sync input timing signal (pull up is disabled). 010: Reserved. 011: Reserved.	0x0	R/W
[5:3]	CFG_GPIO_1	GPIO1 Pin Function Selection. These bits allow selection of which function is applied to the GPIO1 pin. 000: idle. The GPIO is idle with a weak pull up. 001: wake. The GPIO delays initialization of the ADIS16607 when pulled low. 010: Reserved. 011: Reserved.	0x1	R/W

USER REGISTER DEFINITIONS

Table 66. Bit Descriptions for USER_GPIO_CFG1 (Continued)

Bits	Bit Name	Description	Default	Access
[2:0]	CFG_GPIO_0	GPIO0 Pin Function Selection. These bits allow selection of which function is applied to the GPIO0 pin. 000: idle. The GPIO is idle with a weak pull up. 001: $\overline{\text{RESET}}$. The GPIO resets the device when pulled low. 010: Reserved. 011: Reserved.	0x1	R/W

USER GPIO CONFIGURATION REGISTER 2

Address: 0x0030, Default: 0x0002, Name: USER_GPIO_CFG2

Table 67. Bit Descriptions for USER_GPIO_CFG2

Bits	Bit Name	Description	Default	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:1]	CFG_DPLL_LOCK	DPLL Lock Configuration. Use these bits to configure to number of clocks required to lock the DPLL. 00: allows the DPLL to lock after 1 clock. 01: allows the DPLL to lock after 2 clocks. 10: allows the DPLL to lock after 3 clocks. 11: allows the DPLL to lock after 4 clocks.	0x1	R/W
0	DPLL_UNLOCK_EN	DPLL Unlock. Enables the unlock feature of the DPLL.	0x0	R/W

ENABLE FULL-DUPLEX SPI REGISTER

Address: 0x0031, Default: 0x0000, Name: SPI_FULLDUPLEX_KEY

Table 68. Bit Descriptions for SPI_FULLDUPLEX_KEY

Bits	Bit Name	Description	Default	Access
[15:0]	SPI_FULLDUPLEX_KEY	SPI Full-Duplex Key. Writing 0xB3B3 to this register locks the ADIS16607 to full-duplex SPI mode. In full-duplex SPI mode, the SPI response appears in the next SPI transaction.	0x0	R/W

ENABLE HALF-DUPLEX SPI REGISTER

Address: 0x0032, Default: 0x0000, Name: SPI_HALFDUPLEX_KEY

Table 69. Bit Descriptions for SPI_HALFDUPLEX_KEY

Bits	Bit Name	Description	Default	Access
[15:0]	SPI_HALFDUPLEX_KEY	SPI Half-Duplex Key. Writing 0xB4B4 to this register locks the ADIS16607 to half-duplex SPI mode. In half-duplex SPI mode, the SPI response appears in the same SPI transaction.	0x0	R/W

USER REGISTER DEFINITIONS

USER SYNC REGISTER

Address: 0x0033, Default: 0x0000, Name: USER_SYNC

Table 70. Bit Descriptions for USER_SYNC

Bits	Bit Name	Description	Default	Access
15	SYNC_TYPE	Selects Sync Operation Mode. 0: direct sync mode. External sync clock multiplication is disabled (default). 1: scaled sync mode. The external sync clock frequency, f_{SYNC}, is multiplied by the value of the SYNC_SCALE_FACTOR bits in this register. See Table 1 for the allowable external sync clock frequencies in this mode.	0x0	R/W
[14:0]	SYNC_SCALE_FACTOR	Sync Scale Factor, K_{ECSF}. The sync scale factor multiplies the speed of f_{SYNC} to generate a higher frequency clock for the digital PLL. For example, if K_{ECSF} = 64 and f_{SYNC} = 125Hz, the resulting sample rate = 125Hz × 64 = 8kHz.	0x0	R/W

USER DATA CONFIGURATION REGISTER

This register configures which IMU data appears in the FIFO and burst transfer modes. Note that the live registers containing the corresponding data continue to update and are not affected by the settings of this register.

Address: 0x0034, Default: 0x1FFF, Name: USER_DATA_CFG

Table 71. Bit Descriptions for USER_DATA_CFG

Bits	Bit Name	Description	Default	Access
15	WORD_SIZE	Word Size. Use this bit to select a 16-bit or 24-bit output word length. 1: 24-bit output length; the low registers are included. 0: 16-bit output length; the low registers are not included	0x0	R/W
14	DATA_CNTR_EN	Data Counter Value Output Enable. Use this bit to enable the output data counter. 1: DATA_CNTR is written into the FIFO. 0: DATA_CNTR is not written into the FIFO.	0x0	R/W
13	TIME_STAMP_EN	Time Stamp Value Output Enable.	0x0	R/W
12	TEMPERATURE_EN	Enable Temperature Sensor. Temperature output enable. 1: the temperature is written into the FIFO. 0: the temperature is not written into the FIFO.	0x1	R/W
11	Z_DELTANG_EN	Yaw Axis Gyroscope Output Enable (Default).	0x1	R/W
10	Y_DELTANG_EN	Roll Axis Gyroscope Output Enable (Default).	0x1	R/W
9	X_DELTANG_EN	Pitch Axis Gyroscope Output Enable (Default).	0x1	R/W
8	Z_DELTVEL_EN	Z-Axis Accelerometer Output Enable (Default).	0x1	R/W
7	Y_DELTVEL_EN	Y-Axis Accelerometer Output Enable (Default).	0x1	R/W
6	X_DELTVEL_EN	X-Axis Accelerometer Output Enable (Default).	0x1	R/W
5	Z_GYRO_EN	Yaw Axis Gyroscope Output Enable (Default).	0x1	R/W
4	Y_GYRO_EN	Roll Axis Gyroscope Output Enable (Default).	0x1	R/W
3	X_GYRO_EN	Pitch Axis Gyroscope Output Enable (Default).	0x1	R/W
2	Z_ACCEL_EN	Z-Axis Accelerometer Output Enable (Default).	0x1	R/W
1	Y_ACCEL_EN	Y-Axis Accelerometer Output Enable (Default).	0x1	R/W
0	X_ACCEL_EN	X-Axis Accelerometer Output Enable (Default).	0x1	R/W

USER REGISTER DEFINITIONS

FIFO CONFIGURATION REGISTER

Address: 0x0035, Default: 0x0000, Name: USER_FIFO_CFG

Table 72. Bit Descriptions for USER_FIFO_CFG

Bits	Bit Name	Description	Default	Access
15	CLEAR_FIFOB	FIFO Reset. Use this bit to reset the FIFO by clearing the FIFO pointers.	0x0	W
[14:11]	RESERVED	Reserved.	0x0	R
[10:0]	FIFO_THRESHOLD	Threshold Value Where FIFO Word Count Triggers an Interrupt. A value of 0 (default) disables the FIFO. To enable the FIFO, enter a nonzero threshold value. If FIFO_THRESHOLD ≤ 1024, a DIAG_STAT flag (FIFO_THRESH_MET, Bit 0, of Register 0x0005) is raised once the FIFO word count reaches the threshold value. Note that if GPIO4 is configured to output DEV_NOK and no other DIAG_STAT flags are present, an interrupt generates on GPIO4 when the FIFO threshold is met. If FIFO_THRESHOLD > 1024, the FIFO runs without generating flags or interrupts.	0x0	R/W

SOFTWARE RESET

Address: 0x0036, Default: 0x0000, Name: SOFT_RESET

Table 73. Bit Descriptions for SOFT_RESET

Bits	Bit Name	Description	Default	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	REG_RESET	Software Reset. Writing 1b to this bit field issues a reset to the control logic of the ADIS16607.	0x0	R/W

MSC_CTRL REGISTER

Address: 0x0039, Default: 0x0000, Name: MSC_CTRL

Table 74. Bit Descriptions for MSC_CTRL

Bits	Bit Name	Description	Default	Access
[15:10]	RESERVED	Reserved.	0x0	R
[9:8]	FILT_BW	Filter Bandwidth Select. Low-pass IIR cutoff frequency. The cutoff frequencies (f_C) that follow are −3dB and scale with the internal sample clock frequency (values shown are for typical f_S, as specified in Table 1). 0b00 (default): filter disabled. 0b01: f_C = 500Hz. 0b10: f_C = 100Hz. 0b11: f_C = 20Hz.	0x0	R/W
7	ST2	Self Test Force Enable. This bit enables the self test force.	0x0	R/W
6	ST1	Self Test Mode Enable. This bit enables the self test mode.	0x0	R/W
[5:3]	GYRO_USER_OFFSET	Gyroscope User Offset Gain. This bit field setting allows the user to reduce the effective bias gain in the XG_BIAS, YG_BIAS, and ZG_BIAS registers. Using these feature gives the user increased precision when the amount of bias correction required is small. The gain reduction is in powers of two. For example, a value of 2 divides the user offset by 2^2.	0x0	R/W
[2:0]	ACCEL_USER_OFFSET	Accelerometer User Offset Gain. This bit field setting allows the user to reduce the effective bias gain in the XA_BIAS, YA_BIAS, and ZA_BIAS registers. Using these feature gives the user increased precision when the amount of bias correction required is small. The gain reduction is in powers of two. For example, a value of 2 divides the user offset by 2^2.	0x0	R/W

USER REGISTER DEFINITIONS

DECIMATION RATE REGISTER

Address: 0x003A, Default: 0x0000, Name: DEC_RATE

Table 75. Bit Descriptions for DEC_RATE

Bits	Bit Name	Description	Default	Access
[15:0]	DECIMATE_VALUE	Decimation Value. The actual decimation rate, D, is the DEC_RATE + 1, where DEC_RATE is the value stored in this register. Note that when changing the decimation rate, it is recommended to first reset DEC_RATE to 0x000 before entering the new value, which allows the decimation accumulator to reset.	0x0	R/W

USER REGISTER DEFINITIONS

ACCELEROMETER BIAS CALIBRATION

Each inertial sensor on every ADIS16607 is factory calibrated over a temperature range of −40°C to +85°C. The calibration compensates for bias, sensitivity, and alignment errors. Although the factory calibration correction factors are not user accessible, users can apply independent bias adjustments to each sensor. For accelerometers, user bias correction is configured using the XA_BIAS, YA_BIAS, and ZA_BIAS registers for the x-, y-, and z-axis, respectively. In addition, the ACCEL_USER_OFFSET bit field (the MSC_CTRL register, Bits[2:0]) provides optional gain reduction for the user accelerometer bias correction factors. User bias correction is applied immediately following the factory derived correction formulas in the signal chain, as shown in Figure 46.

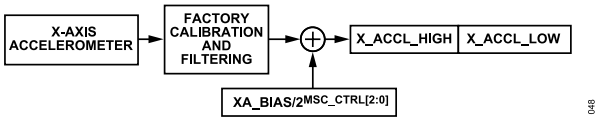


Figure 46. User Calibration Signal Path, Accelerometers

XA_BIAS REGISTER

Address: 0x003B, Default: 0x0000, Name: XA_BIAS

Table 76. Bit Descriptions for XA_BIAS

Bits	Bit Name	Description	Default	Access
[15:0]	XA_BIAS	X-Axis Accelerometer User Offset Correction.	0x0	R/W

YA_BIAS REGISTER

Address: 0x003C, Default: 0x0000, Name: YA_BIAS

Table 77. Bit Descriptions for YA_BIAS

Bits	Bit Name	Description	Default	Access
[15:0]	YA_BIAS	Y-Axis Accelerometer User Offset Correction.	0x0	R/W

ZA_BIAS REGISTER

Address: 0x003D, Default: 0x0000, Name: ZA_BIAS

Table 78. Bit Descriptions for ZA_BIAS

Bits	Bit Name	Description	Default	Access
[15:0]	ZA_BIAS	Z-Axis Accelerometer User Offset Correction.	0x0	R/W

USER REGISTER DEFINITIONS

GYROSCOPE BIAS CALIBRATION

Using the same principles as in the Accelerometer Bias Calibration section, users can apply bias correction to the gyroscope outputs using the XG_BIAS, YG_BIAS, and ZG_BIAS registers for the x-, y-, and z-axis, respectively. The GYRO_USER_OFFSET bit field (the MSC_CTRL register, Bits[5:3]) provides optional gain reduction for the user gyroscope bias correction factors, as shown in Figure 47.

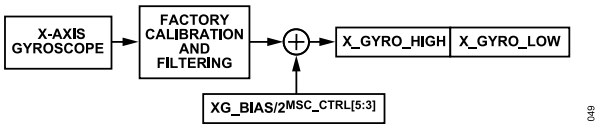


Figure 47. User Calibration Signal Path, Gyroscopes

XG_BIAS REGISTER

Address: 0x003E, Default: 0x0000, Name: XG_BIAS

Table 79. Bit Descriptions for XG_BIAS

Bits	Bit Name	Description	Default	Access
[15:0]	XG_BIAS	X-Axis Gyroscope User Offset Correction.	0x0	R/W

YG_BIAS REGISTER

Address: 0x003F, Default: 0x0000, Name: YG_BIAS

Table 80. Bit Descriptions for YG_BIAS

Bits	Bit Name	Description	Default	Access
[15:0]	YG_BIAS	Y-Axis Gyroscope User Offset Correction.	0x0	R/W

ZG_BIAS REGISTER

Address: 0x0040, Default: 0x0000, Name: ZG_BIAS

Table 81. Bit Descriptions for ZG_BIAS

Bits	Bit Name	Description	Default	Access
[15:0]	ZG_BIAS	Z-Axis Gyroscope User Offset Correction.	0x0	R/W

MODEL_ID REGISTER

Address: 0x0041, Default: Varies, Name: MODEL_ID

Table 82. Bit Descriptions for MODEL_ID

Bits	Bit Name	Description	Default	Access
[15:0]	MODEL_ID	Identification Code Corresponding to the IMU Model (Accelerometer and Gyroscope Range). ADIS16607-2: 6072 (0x17B8). ADIS16607-3: 6073 (0x17B9).	Varies	R

USER REGISTER DEFINITIONS

DIGITAL STATUS REGISTER

Address: 0x004E, Default: 0x0000, Name: DIGITAL_STATUS

Table 83. Bit Descriptions for DIGITAL_STATUS

Bits	Bit Name	Description	Default	Access
[15:9]	RESERVED	Reserved.	0x0	R
8	ADC_ERR	ADC Failed to Complete Conversion(s). This bit is set when the ADC fails to complete the requested conversions during any ODR period.	0x0	R
7	RESERVED	Reserved.	0x0	R
6	DATAMEM_PAR_ERR	Data Memory Parity Error.	0x0	R
5	PROGMEM_PAR_ERR	Program Memory Parity Error.	0x0	R
4	PARAMMEM_PAR_ERR	Parameter Memory Parity Error.	0x0	R
[3:1]	RESERVED	Reserved.	0x0	R
0	BOOTLOAD_BUSY	Status Bit for Bootloader Activity. When it returns a 1, program is in the process of loading; therefore, wait until it is 0.	0x0	R

APPLICATIONS INFORMATION

ASSEMBLY AND HANDLING TIPS

Package Attributes

The ADIS16607 is a multichip module packaged in an 18-terminal, ceramic, leadless chip carrier (LCC), excluding the index pads. This package has three basic attributes that influence its handling and assembly to the PCB of the system: the lid, the substrate, and the land pattern.

All electrical and physical connections are through the 18 terminals (see the Outline Dimensions section for additional information). It is recommended to ground all of the index pads for additional strength attaching the ADIS16607 to the PCB of the user.

Assembly Tips

When attaching the ADIS16607 to a PCB, follow these guidelines:

- The ADIS16607 supports solder reflow attachment processes in accordance with J-STD-020E.
- Multiple reflow passes are acceptable, provided that no rework occurs during these reflow operations.
- Manage moisture exposure prior to the solder reflow processing in accordance with J-STD-033, Moisture Sensitivity Level 1.
- Avoid exposing the ADIS16607 to mechanical shock that exceeds the absolute maximum rating in Table 7. In standard PCB processing, high-speed handling equipment and panel separation processes often present the most risk of introducing harmful levels of mechanical shock.

PCB Layout Suggestions

Figure 48 shows the recommended PCB land pattern for the ADIS16607.

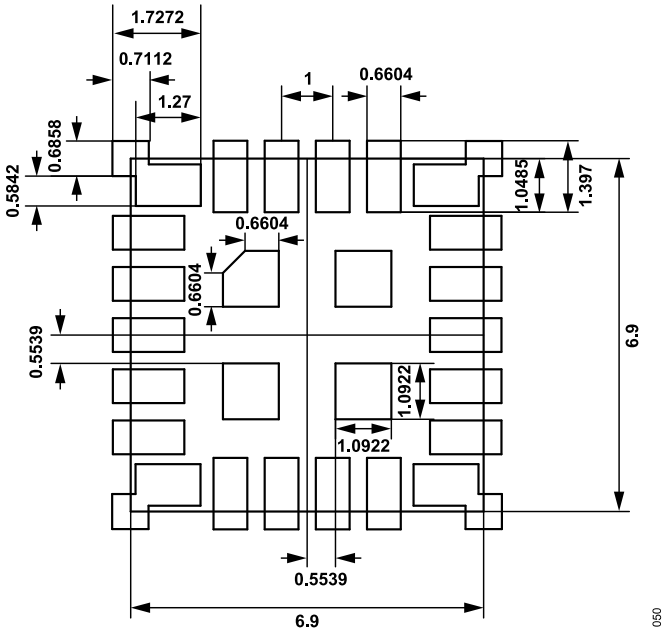


Figure 48. Recommended PCB Land Pattern

Underfill

Underfill can be a useful technique in managing certain threats to the integrity of the solder joints of the ADIS16607, including peeling stress and extended exposure to vibration. When selecting underfill material and developing an application and curing process, ensure that the material fills the gap between each surface (the ADIS16607 substrate and system PCB) and adheres to both surfaces. The ADIS16607 does not require the use of underfill materials in applications that do not anticipate exposure to these types of mechanical stresses and when the coefficient of thermal expansion (CTE) of the system PCB is close to the same value as the CTE of the substrate of the ADIS16607 (see Table 8).

Process Validation and Control

These guidelines provide a starting point for developing a process for attaching the ADIS16607 to a system PCB. Because each system and situation can present unique requirements for this attachment process, ensure that the process supports optimal solder joint integrity, verify that the final system meets all environmental test requirements, and establish observation and control strategies for all key process attributes (for example, peak temperatures, dwell times, and ramp rates).

APPLICATIONS INFORMATION

IMU INITIALIZATION

The sequence shown in Table 84 is used to initialize the ADIS16607, and the steps in Table 84 can be summarized as follow:

1. Lock the SPI mode to either full-duplex or half-duplex mode.
2. Configure the ADIS16607 as follows:
   a. GPIO configuration (including the DR signal)
   b. External synchronization
   c. Decimation and/or averaging
   d. Burst read mask setup (select which registers appear in a burst)
3. Set the write lock bit.
4. Begin reading data when the DR signal is active.

Table 84. SPI IMU Initialization

		SPI Mode	
Step	**Description**	**Full-Duplex**	**Half-Duplex**
1	Apply power.	Not applicable	Not applicable
2	Wait 200ms for the device to come out of reset and bootloader to complete.	Not applicable	Not applicable
3	Lock the SPI mode.	0xB3B33180	0x32B4B4
4	Read DIAG_STAT to clear possible false errors.	0x0000050F	0x85000000
5	Read DIAG_STAT and ensure it is 0x0000.	0x0000050F	0x85000000
6	Read DIGITAL_STATUS and ensure that the BOOTLOAD_BUSY bit (Bit 0) is low.	0x00004E00	0xCE000000
7	Configure the GPIOx pins (GPIO0 as $\overline{\text{RESET}}$, GPIO1 as wake, and GPIO3 as DR) on USER_GPIO_CFG1	0x02092F84	0x2F0209
8	Configure burst mode (optional).	Varies	Varies
9	Configure decimation (optional).	Varies	Varies
10	Disables SPI writes to the register map using WRITE_LOCK. To activate writes, it requires two SPI writes.	0x55552D8D, 0xAAAA2D8D	0x2D5555, 0x2DAAAA
11	Read WRITE_LOCK, if locked, it returns 1.	0x00002D05	0xAD000000
12	Read DIAG_STAT to clear possible false errors.	0x0000050F	0x85000000
13	Read DIAG_STAT and ensure it is 0x0000.	0x0000050F	0x85000000
14	Begin reading data when DR is active.	Varies	Varies

APPLICATIONS INFORMATION

BURST READ FUNCTION

The burst read function provides a way to read a batch of output data registers using a continuous stream of registers while the chip select ($\overline{CS}$) pin is held low. Note that burst read mode only works in SPI half-duplex mode, as well as I^2C mode.

The burst transfer contents are configured in the USER_DATA_CFG register at Address 0x0034. This register allows the user to transfer either 16-bit or 24-bit data and to select which data is included in the burst.

A burst transfer is initiated by reading the DIAG_STAT register at Address 0x05 and keeping the $\overline{CS}$ pin low while reading all registers in the sequence out of DOUT. The user terminates the burst by raising the $\overline{CS}$ pin high. Although the user can terminate the burst read at any time, it is logical to read all the registers specified in the USER_DATA_CFG register plus one additional 16-bit read for the checksum. The burst transfer can be terminated early by deactivating the $\overline{CS}$ line.

If the DIAG_STAT register is not 0x0000, the data outputs are not guaranteed to be valid and must be discarded.

The checksum computation only uses registers that are enabled in the burst read stream. The formula can be represented as the sum of each 16-bit word included in the burst.

For example, if USER_DATA_CFG = 0xF249, the burst data includes the following:

1. DIAG_STAT
2. X_ACCEL_HIGH
3. X_ACCEL_LOW
4. X_GYRO_HIGH
5. X_GYRO_LOW
6. X_DELTVEL_HIGH
7. X_ DELTVEL_LOW
8. X_DELTANG_HIGH
9. X_ DELTANG_LOW
10. TEMP_OUT
11. TIME_STAMP
12. DATA_CNTR
13. CHECKSUM

CHECKSUM, Bits[15:0], is a 16-bit number that is the 16-bit word sum of the following registers:

1. DIAG_STAT, Bits[15:8], 0x00
2. DIAG_STAT, Bits[7:0], 0x00
3. X_ACCEL_HIGH, Bits[15:8], 0x12
4. X_ACCEL_HIGH, Bits[7:0], 0x82
5. X_ACCEL_LOW, Bits[15:8], 0x80
6. X_ACCEL_LOW, Bits[7:0], 0x00
7. Y_ACCEL_HIGH, Bits[15:8], 0x01
8. Y_ACCEL_HIGH, Bits[7:0], 0xF6
9. Y_ACCEL_LOW, Bits[15:8], 0xC0
10. Y_ACCEL_LOW, Bits[7:0], 0x00
11. Z_ACCEL_HIGH, Bits[15:8], 0x04
12. Z_ACCEL_HIGH, Bits[7:0], 0x0C
13. Z_ACCEL_LOW, Bits[15:8], 0x20
14. Z_ACCEL_LOW, Bits[7:0], 0x00
15. X_GYRO_HIGH, Bits[15:8], 0x02
16. X_GYRO_HIGH, Bits[7:0], 0x35
17. X_GYRO_LOW, Bits[15:8], 0x50
18. X_GYRO_LOW, Bits[7:0], 0x00
19. Y_GYRO_HIGH, Bits[15:8], 0x01
20. Y_GYRO_HIGH, Bits[7:0], 0xC1
21. Y_GYRO_LOW, Bits[15:8], 0x30
22. Y_GYRO_LOW, Bits[7:0], 0x00
23. Z_GYRO_HIGH, Bits[15:8], 0x02
24. Z_GYRO_HIGH, Bits[7:0], 0x71
25. Z_GYRO_LOW, Bits[15:8], 0x2D
26. Z_GYRO_LOW, Bits[7:0], 0x00
27. TEMP_OUT, Bits[15:8], 0xF9
28. TEMP_OUT, Bits[7:0], 0xBC
29. TIME_STAMP, Bits[15:8], 0x00
30. TIME_STAMP, Bits[7:0], 0x00
31. DATA_CNTR, Bits[15:8], 0x3C
32. DATA_CNTR, Bits[7:0], 0x88

To illustrate the checksum value calculation, note that, the previous list (not including CHECKSUM) includes typical values that result with a checksum value of 0x622F.

CHECKSUM is a part of the burst transfer that appears after the final value in the burst. However, it does not appear in any register.

It is possible to continue reading after CHECKSUM; however, the data is meaningless.

APPLICATIONS INFORMATION

CONFIGURE AND READ THE FIFO

The FIFO provides temporary storage for the enabled sensor outputs produced at each DR signal. Each stored word contains a channel index (prepended and/or encoded) and a 16-bit data field. The memory is implemented as 1024 words using a dual-port architecture so that new data writes and host FIFO reads proceed without contention. The following summarizes key attributes of the FIFO:

- **Depth/width:** 1024 words
- **Writer:** on each DR event (frame).
- **Reader:** Host via control port (SPI/I^{2}C).
- **Channel selection:** governed by the USER_DATA_CFG register. The enabled channels define the data frame.
- **Full condition:** if capacity is insufficient for an entire data frame, new entries overwrite the oldest entries. If capacity is not sufficient for an entire frame, data discontinuity or data loss occurs.

Functional Operation

Enqueuing and dequeuing functional operation follows:

Enqueuing (DR → FIFO): on each DR pulse, the FIFO controller pushes all enabled outputs as follows.

- For 24-bit channels, data are split into two words:

  Every word comes with a compact channel index. The index is made available to the host in a companion register (FIFO_CH_INDEX, Address 0x002A) after each data read, allowing the host to reconstruct per-channel streams. See the Data Format and Channel Index section for more information.

  - **High word:** upper 16 bits of the 24-bit value.
  - **Low word:** lower 8 bits padded to 16 bits (presence controlled by the WORD_SIZE bit, Bit 15 of the USER_DATA_CFG register, Address 0x0034).

Dequeuing (FIFO → Host) as follows:

- **FIFO data port:** reading the FIFO_DATA register (Address 0x0029) returns the next word and advances the read pointer.
- **Channel index port:** reads the FIFO_CH_INDEX (Address 0x002A) companion register to obtain the decoded channel index for the last word read.
- **Empty response:** when empty, reads return 0xFFFF.

Configuration

Configure the FIFO prior to streaming by doing the following:

- **Select channels:** set the USER_DATA_CFG and USER_FIFO_CFG registers (Address 0x0034 and Address 0x0035) to include the required outputs.
- **Enable FIFO and set FIFO threshold:** program the FIFO_THRESHOLD bits (Bits[10:0] of Address 0x0035) to the desired value (any nonzero value enables FIFO operation). When occupancy reaches or exceeds this value, a threshold condition asserts (readable via the FIFO_THRESH_MET bit, Bit 0, of the DIAG_STAT register (Address 0x0005)) and is routable to GPIO4 as the DEV_NOK interrupt.
- **Clear FIFO (optional):** set the CLEAR_FIFOB bit (Bit 15 of the USER_FIFO_CFG register, Address 0x0035) to 1 to reset the read and write pointers and clear the occupancy. Note that this setting also clears the threshold indication.

Reading the FIFO

Use the FIFO read port continuously until empty or until the required number of words are dequeued. The access model depends on the control-port mode as follows:

- **SPI half-duplex/ I^{2}C:** performs a burst read at the FIFO_DATA register (Address 0x0029). The device returns the next word on each 16-bit read while $\overline{CS}$ remains low (SPI) or while the multibyte read continues (I^{2}C). (Half-duplex autoincrementing is overridden for this address.) Note that burst reads on the FIFO_DATA register do not include a checksum value, unlike the standard burst read function performed at the DIAG_STAT register (Address 0x0005).
- **SPI full-duplex:** issues repeated read commands to the FIFO_DATA register. Each command returns the next word. If desired, after each data read, fetch the FIFO_CH_INDEX register (Address 0x002A) to identify the channel. Note that in SPI full-duplex mode, the channel index of the final word in the FIFO is always zero (it does not read the expected index value).

Note that if using the DEV_NOK interrupt to monitor the FIFO_THRESH_MET bit (Bit 0 of the DIAG_STAT register, Address 0x0005), a DIAG_STAT register read must be performed after receiving the DEV_NOK interrupt to check which flags are raised and to clear the status.

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Data Format and Channel Index

Each popped FIFO entry is a 16-bit data field that is identifiable using the channel index from the FIFO_CH_INDEX register (Address 0x002A). Table 85 shows how the channel index values correspond to the output registers that can be enabled by the USER_DATA_CFG register (Address 0x0034). The low channels appear for inertial data if 24-bit output length is selected by the WORD_SIZE bit (Bit 15, Register USER_DATA_CFG). Note that, 24-bit outputs can be reconstructed as Value[23:0] = (High[15:0], Low[15:8]).

Table 85. FIFO Channel Index Decoding Table

Decoding Index	Data
0	X-Channel Accelerometer Data High
1	X-Channel Accelerometer Data Low
2	Y-Channel Accelerometer Data High
3	Y-Channel Accelerometer Data Low
4	Z-Channel Accelerometer Data High
5	Z-Channel Accelerometer Data Low
6	X-Channel Gyroscope Data High
7	X-Channel Gyroscope Data Low
8	Y-Channel Gyroscope Data High
9	Y-Channel Gyroscope Data Low
10	Z-Channel Gyroscope Data High
11	Z-Channel Gyroscope Data Low
12	X-Channel Delta Velocity Data High
13	X-Channel Delta Velocity Data Low
14	Y-Channel Delta Velocity Data High
15	Y-Channel Delta Velocity Data Low
16	Z-Channel Delta Velocity Data High
17	Z-Channel Delta Velocity Data Low
18	X-Channel Delta Angle Data High
19	X-Channel Delta Angle Data Low
20	Y-Channel Delta Angle Data High
21	Y-Channel Delta Angle Data Low
22	Z-Channel Delta Angle Data High
23	Z-Channel Delta Angle Data Low
26	Temperature Data
27	Timestamp Data
28	Data Counter Data

Register Summary

Table 86 lists the registers most relevant to FIFO operation.

Table 86. FIFO-Related Register

Register/Bit(s)	Address	Access	Description
FIFO_DATA, Bits[15:0]	0x0029	R	Returns next FIFO word and advances read pointer. Returns 0xFFFF when empty. Burst readable in SPI half-duplex/I^2C; repeated commands in SPI full-duplex.
FIFO_CH_INDEX, Bits[6:0]	0x002A	R	Decoded logical channel index for the most recently read FIFO_DATA word. Use to bind data-words to channels and to distinguish the high and low segments.
FIFO_WORD_CNT, Bits[10:0]	0x002B	R	Current FIFO occupancy in words (0…1024). Useful for polling-based service in addition to threshold interrupts.
USER_FIFO_CFG, Bit 15, CLEAR_FIFOB	0x0035	W	Set to 1 to reset read and write pointers, clear the FIFO memory, and deassert threshold indication.
USER_FIFO_CFG, Bits[10:0], FIFO_THRESHOLD	0x0035	R/W	Programmable threshold; nonzero enables threshold detection and associated interrupt signaling.
USER_DATA_CFG, Bit 15, WORD_SIZE	0x0034	R/W	Controls the word size of the inertial outputs written into the FIFO for each frame (presence of low words for 24-bit channels).
USER_DATA_CFG, Bits[14:0]	0x0034	R/W	Selects outputs written into the FIFO each frame.

APPLICATIONS INFORMATION

ON-DEMAND SELF TEST

The ADIS16607 incorporates an on-demand self test feature that effectively tests the mechanical and electronic system. During self test, an electrical stimulus is applied internally to emulate motion on the sensing elements and verify the signal path. The test must be performed when the sensor is at rest because any physical motion during self test can affect the results.

The on-demand self test must be performed manually by the user by taking the following steps:

1. Enable ST mode by setting the ST1 bit (Bit 6 of the MSC_CTRL register, Address 0x0039) to 1.
2. Wait at least the self test time specified in Table 1 to allow outputs to settle.
3. Read the inertial output registers and record the measured values.
4. Enable the ST force by setting the ST2 bit (Bit 7 of the MSC_CTRL register, Address 0x0039) to 1.
5. Wait at least the self test time specified in Table 1 to allow outputs to settle.
6. Read the inertial output registers and record the measured values.
7. Calculate the difference of inertial values from Step 3 (ST1 = 1 and ST2 = 0) and Step 6 (ST1 = ST2 = 1).
8. Confirm the results are within the self test delta values provided in Table 1.

After the self test measurement is complete, set both the ST1 and ST2 bits low to resume normal operation.

WAKE FUNCTIONALITY

After a software or hardware reset, setting GPIO1 high triggers the bootloader to read the NVM and load its contents. The GPIO1 is idle with a weak pull up, by default, which results in a fully functional device after reset.

On the other hand, holding the GPIO1 pin low after reset prevents the bootloading process. The user can then trigger the bootloader by a SPI command, if desired, by setting the NVM_LOAD bit (Bit 0 of the USER_BOOT register, Address 0x002E) to 1, waiting ~10ms for the bootloading to finish, and then clearing the NVM_LOAD bit.

EVALUATION TOOLS

Breakout Boards

The ADIS16607 has breakout boards that provide a simple way to connect an ADIS16607 model and an existing embedded processor platform.

Table 87 provides a list of the model numbers for each breakout board along with the ADIS16607 model that is on each breakout board. See the EVAL-ADIS16607 user guide for additional information.

Table 87. Breakout Board Models

Breakout Board Model	ADIS16607 Model
ADIS16607-2/PCBZ	ADIS16607-2LEZ
ADIS16607-3/PCBZ	ADIS16607-3LEZ

PC-Based Evaluation, EVAL-ADIS-FX3

In addition to supporting quick prototype connections between the ADIS16607 and an embedded processing system, J1 on the breakout boards also connect directly to the EVAL-ADIS-FX3.

The EVAL-ADIS-FX3 is an open-source evaluation platform for Windows®-based systems. The application program interface (API) of the EVAL-ADIS-FX3 manages all the complex USB transactions and implements all the necessary tools to begin capturing high-speed, high-performance data in custom applications. This .NET-compatible API, written in VB.NET and C#, includes data streaming features tailored to reliably capturing inertial sensor data at the maximum data rate. The API is also a fully documented open-source and is licensed under the MIT license. The API also includes a wrapper library, allowing users to use the same API in any development environment with support for .NET (such as, MATLAB, LabVIEW, and Python).

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
E-18-5	LCC	18-Terminal Ceramic Leadless Chip Carrier

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16607-2LEZ	−40°C to +105°C	18-Terminal Ceramic Leadless Chip Carrier [LCC]	E-18-5
ADIS16607-3LEZ	−40°C to +105°C	18-Terminal Ceramic Leadless Chip Carrier [LCC]	E-18-5

[1] Z = RoHS-Compliant Part.

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