ADIS16575/ADIS16576/ADIS16577

Precision MEMS IMU Module

FEATURES

- Triaxial digital angular rate (gyroscope) sensing
  - ±450°/sec and ±2000°/sec range options
  - 2.0°/hr in-run bias stability (±450°/sec range)
  - 0.2°/√hr angular random walk (±450°/sec range)
  - ±0.05° axis to axis misalignment error
- Triaxial digital accelerometer sensing
  - ±8 *g* (ADIS16575), ±14 *g* (ADIS16576), ±40 *g* (ADIS16577)
  - 2.9 μ*g* in-run bias stability (±8 *g* range)
- Triaxial delta angle and delta velocity outputs
- Factory-calibrated sensitivity, bias, and axial alignment
  - Calibration temperature range: −40°C to +85°C
- SPI-compatible data communications
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Data ready indicator for synchronous data acquisition
  - External synchronization of data sampling/processing
  - On-demand self test of inertial sensors
  - On-demand self test of flash memory
  - Continuous real-time health monitoring of SRAM and sensors
  - FIFO, 512 samples, up to 4 kHz sample rate
- Single-supply operation (VDD): 3.0 V to 3.6 V
- 2000 *g* mechanical shock survivability
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Navigation, stabilization, and instrumentation
- Unmanned and autonomous vehicles
- Smart agriculture and construction machinery
- Factory and industrial automation
- Smart munitions
- Autonomous industrial robotics

GENERAL DESCRIPTION

The ADIS16575/ADIS16576/ADIS16577 are a precision, microelectromechanical system (MEMS) inertial measurement unit (IMU) that includes a triaxial gyroscope and a triaxial accelerometer. Each inertial sensor in the ADIS16575/ADIS16576/ADIS16577 integrates signal conditioning to optimize dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, and alignment. Therefore, each sensor has dynamic compensation formulas that provide accurate sensor measurements over a broad set of conditions.

The ADIS16575/ADIS16576/ADIS16577 provide a simple, cost effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared to the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control.

The ADIS16575/ADIS16576/ADIS16577 are in an aluminum module package that is approximately 24.30 mm × 22.40 mm × 13.70 mm with a 14-lead connector interface.

FUNCTIONAL BLOCK DIAGRAM

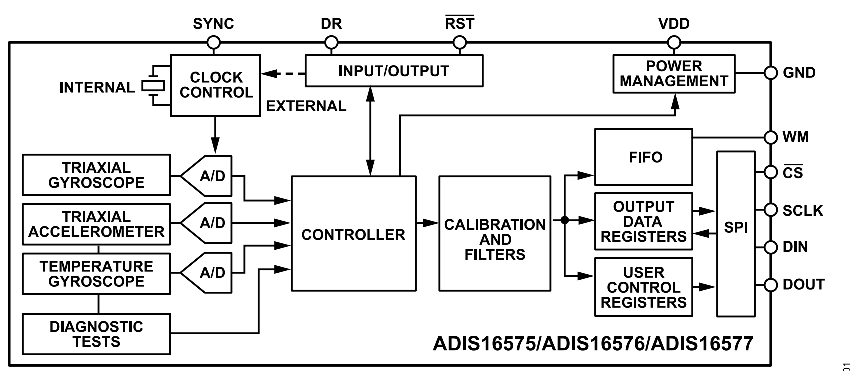

Figure 1. Functional Block Diagram

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

10/2024—Revision 0: Initial Version

SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, angular rate = 0°/sec, and dynamic range = ±2000°/sec ± 1*g*, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range	ADIS16575-2, ADIS16576-2, ADIS16577-2	±450			°/sec
	ADIS16576-3, ADIS16577-3	±2000			°/sec
ACCELEROMETERS					
Dynamic Range	ADIS16575		±8		*g*
	ADIS16576			±14	*g*
	ADIS16577		±40		*g*
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 0°C (±5°C)		0.1		°C/LSB
LOGIC INPUTS[1]					
Input Voltage					
High, V_{IH}		2.5			V
Low, V_{IL}				0.45	V
Pulse Width		1			µs
Input Current					
Logic 1, I_{IH}	V_{IH} = 3.3 V			0.15	µA
Logic 0, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{\text{RST}}$				10	µA
$\overline{\text{RST}}$ Pin			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output Voltage					
High, V_{OH}	Source current (I_{SOURCE}) = 0.5 mA	2.65			V
Low, V_{OL}	Sink current (I_{SINK}) = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[2]	100,000			Cycles
Data Retention[3]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[4]	Time until data is available				
Power-On Start-Up Time			282		ms
Reset Recovery Time	Register GLOB_CMD, Bit 7 = 1 (see Table 128)		241		ms
	$\overline{\text{RST}}$ pulled low, then restored to high[5]		275		ms
Factory Calibration Restore	Register GLOB_CMD, Bit 1 = 1 (see Table 128)		48		ms
Flash Memory Backup	Register GLOB_CMD, Bit 3 = 1 (see Table 128)		48		ms
Flash Memory Test Time	Register GLOB_CMD, Bit 4 = 1 (see Table 128)		15		ms
Self Test Time	Register GLOB_CMD, Bit 2 = 1 (see Table 128)		19		ms
CONVERSION RATE, f_{SM}			4000		SPS
Initial Clock Accuracy			3		%
Synchronization Input Clock		1.9 [6]		4.1	kHz
Scaled Input Clock		0.8		400	Hz
POWER SUPPLY, VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[7]	Normal mode, VDD = 3.3 V		30		mA

1 The digital input and output signals use a 3.3 V system.

2 Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.

3 The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.

4 These times do not include thermal settling and internal filter response times, which may affect overall accuracy.

5 The $\overline{\text{RST}}$ line must be in a low state for at least 10 µs to ensure a proper reset initiation and recovery.

SPECIFICATIONS

6 These devices function at lower synchronization input clock rates; however, these rates may result in performance degradation and reduced flexibility in filtering vibration and other transient responses.

7 Power supply current transients can reach 100 mA during initial startup or reset recovery.

GYROSCOPE PERFORMANCE SPECIFICATIONS

Table 2. For ±450°/sec (ADIS16575-2, ADIS16576-2, and ADIS16577-2)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±450			°/sec
Sensitivity	16 bit		40		LSB/°/sec
	32 bit		2,621,440		LSB/°/sec
Repeatability[1]	$-40°C \le T_C \le +85°C$, 1 σ		±0.13		%
Error over Temperature	$-40°C \le T_C \le +85°C$, 1 σ		±0.08		%
Misalignment Error	Axis to axis (orthogonality error), 1 σ		±0.05		Degrees
	Axis to package, 1 σ		±0.25		Degrees
Linearity Error[2]	Full-scale range (FSR) = 450°/sec, angular rate = ±225°/sec, 1 σ		0.035		% FS
	FSR = 450°/sec, angular rate = ±450°/sec, 1 σ		0.45		% FS
Bias					
Repeatability[3]	$-40°C \le T_C \le +85°C$, 1 σ		300		°/hr
In-Run Stability[4]	1 σ		2.0		°/hr
Angular Random Walk	1 σ		0.2		°/√hr
Error over Temperature	$-40°C \le T_C \le +85°C$, 1 σ		±180		°/hr
Linear Acceleration Effect	Any direction, 1 σ		±2		°/hr/*g*
Vibration Rectification Error (VRE)	Random vibration, 8 *g* RMS, bandwidth = 20 Hz to 2 kHz		12		°/hr
Noise					
Output Noise (All Axes)	1 σ, no filtering, 25°C		0.11		°/sec RMS
Rate Noise Density[5]	1 σ		0.004		°/sec/√Hz
Bandwidth					
−3 dB			649		Hz
90° Phase Shift			192		Hz
Sensor Resonant Frequency			78		kHz

1 Sensitivity repeatability is the root sum square (RSS) combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000 hours, +105°C).

2 This measurement is based on the deviation from a best fit linear model.

3 Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000 hours, +105°C).

4 In run stability is the minimum of the Allan deviation curve.

5 Specified for 10 Hz to 40 Hz, at a nominal f_{SM} sample rate, and no digital filtering.

Table 3. For ±2000°/sec (ADIS16576-3 and ADIS16577-3)

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±2000			°/sec
Sensitivity	16 bit		10		LSB/°/sec
	32 bit		655,360		LSB/°/sec
Repeatability [1]	$-40°C \le T_C \le +85°C$, 1 σ		±0.16		%
Error over Temperature	$-40°C \le T_C \le +85°C$, 1 σ		±0.072		%

SPECIFICATIONS

Table 3. For ±2000°/sec (ADIS16576-3 and ADIS16577-3) (Continued)

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
Misalignment Error	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis (orthogonality error), 1 σ		±0.05		Degrees
	Axis to package		±0.25		Degrees
Linearity Error[2]	1 σ, FSR = 2000°/sec, angular rate = ±1000°/sec		0.04		% FS
	1 σ, FSR = 2000°/sec, angular rate = ±2000°/sec		0.5		% FS
Bias					
Repeatability[3]	−40°C ≤ T_C ≤ +85°C, 1 σ		340		°/hr
In-Run Stability[4]	1 σ		7.5		°/hr
Angular Random Walk	1 σ		0.35		°/√hr
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±200		°/hr
Linear Acceleration Effect	Any direction, 1 σ		±2		°/hr/*g*
VRE	Random vibration, 8 *g* RMS, bandwidth = 20 Hz to 2 kHz		55		°/hr
Noise					
Output Noise (All Axes)	1 σ, no filtering, 25°C		0.17		°/sec RMS
Rate Noise Density[5]	1 σ		0.006		°/sec/√Hz
Bandwidth					
−3 dB			649		Hz
90° Phase Shift			192		Hz
Sensor Resonant Frequency			78		kHz

1 Sensitivity repeatability is the RSS combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000hours, +105°C).

2 This measurement is based on the deviation from a best fit linear model.

3 Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000 hours, +105°C).

4 In run stability is the minimum of the Allan deviation curve.

5 Specified for 10 Hz to 40 Hz, at a nominal f_{SM} sample rate, and no digital filtering.

ACCELEROMETER PERFORMANCE SPECIFICATIONS

Table 4. For ±8 g (ADIS16575)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCELEROMETERS					
Dynamic Range		±7	±8		*g*
Sensitivity	32 bit		262,144,000		LSB/*g*
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1 σ		± 0.11		%
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.005		%
Misalignment Error	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis (orthogonality error)		±0.05		Degrees
	Axis to package		±0.25		Degrees
Linearity Error[2]	Best fit straight line				
	1 σ, FSR = ±8 *g*, stimulus = ±4 *g*		0.4		% FS
	1 σ, FSR = ±8 *g*, stimulus = ±8 *g*		3		% FS
Bias					
Repeatability[3]	−40°C ≤ T_C ≤ +85°C, 1 σ		1.4		m*g*
In-Run Bias Stability	±8 *g*, 1 σ		2.9		μ*g*
Velocity Random Walk	1 σ		0.0087		m/sec/√hr
Error over Temperature[4]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.3		m*g*
VRE	Random vibration, 2 *g* RMS, 50 Hz to 1 kHz		9		m*g*

SPECIFICATIONS

Table 4. For ±8 g (ADIS16575) (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Noise					
Output Noise	1 σ, no filtering, 25°C		0.48		*mg* RMS
Rate Noise Density[5]	1 σ		14.9		μ*g*/√Hz RMS
Bandwidth					
−3 dB			750		Hz
90° Phase Shift			187		Hz
Sensor Resonant Frequency			2.4		kHz
Quality Factor (Q)	X-axis and Y-axis		7.4		
	Z-axis		1.5		

[1] Sensitivity repeatability is the RSS combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000 hours, +105°C).

[2] This measurement is based on the deviation from a best fit linear model.

[3] Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C) and high temperature operating life (1000 hours, +105°C).

[4] Bias error over temperature indicates bias variation from the 25°C reference.

[5] Specified for 10 Hz to 40 Hz, at a nominal f_{SM} sample rate, and no digital filtering.

Table 5. For ±14 g (ADIS16576)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCELEROMETERS					
Dynamic Range		±14			*g*
Sensitivity	32 bit		52,428,800		LSB/*g*
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1 σ		± 0.2		%
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.006		%
Misalignment Error	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis (orthogonality error)		±0.05		Degrees
	Axis to package		±0.25		Degrees
Linearity Error[2]	1 σ, FSR = ±14 *g*, stimulus = ±7 *g*		0.3		% FS
	1 σ, FSR = ±14 *g*, stimulus = ±14 *g*		1.2		% FS
Bias					
Repeatability[3]	−40°C ≤ T_C ≤ +85°C, 1 σ		3.0		m*g*
In-Run Bias Stability			13		μ*g*
Velocity Random Walk	1 σ		0.037		m/sec/√hr
Error over Temperature[4]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.67		m*g*
VRE	Random vibration, 4 *g* RMS, 50 Hz to 1 kHz		1.3		m*g*
Noise					
Output Noise	1 σ, no filtering, 25°C		2.56		m*g* RMS
Rate Noise Density[5]	1 σ		80		μ*g*/√Hz RMS
Bandwidth					
−3dB			750		Hz
90° Phase Shift			187		Hz
Sensor Resonant Frequency			5.5		kHz
Quality Factor (Q)	X-axis and Y-axis		1.9		
	Z-axis		0.7		

[1] Sensitivity repeatability is the RSS combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000hours, +105°C).

[2] This measurement is based on the deviation from a best fit linear model.

SPECIFICATIONS

3 Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C) and high temperature operating life (1000 hours, +105°C).

4 Bias error over temperature indicates bias variation from the 25°C reference.

5 Specified for 10 Hz to 40 Hz, at a nominal f_{SM} sample rate, and no digital filtering.

Table 6. For ±40 g (ADIS16577)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCELEROMETERS					
Dynamic Range			±40		g
Sensitivity	32 bit		52,428,800		LSB/*g*
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.2		%
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		0.008		%
Misalignment Error	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis (orthogonality error)		±0.05		Degrees
	Axis to package		±0.25		Degrees
Linearity Error[2]	1 σ, FSR = ±40 *g*, stimulus = ±20 *g*		0.3		% FS
	1 σ, FSR = ±40 *g*, stimulus = ±40 *g*		5		% FS
Bias					
Repeatability[3]	−40°C ≤ T_C ≤ +85°C, 1 σ		6		m*g*
In-Run Stability	1 σ		16		μ*g*
Velocity Random Walk	1 σ		0.05		m/sec/√hr
Error over Temperature[4]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.7		m*g*
VRE	Random vibration, 8 *g* RMS, 50 Hz to 1 kHz		6.5		m*g*
Noise					
Output Noise	1 σ, no filtering, 25°C		2.7		m*g* RMS
Noise Density[5]	1 σ		82		μ*g*/√Hz RMS
Bandwidth					
−3 dB			750		Hz
90° Phase Shift			187		Hz
Sensor Resonant Frequency			5.5		kHz
Quality Factor (Q)	X-axis and Y-axis		1.9		
	Z-axis		0.7		

1 Sensitivity repeatability is the RSS combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C), and high temperature operating life (1000 hours, +105°C).

2 This measurement is based on the deviation from a best fit linear model.

3 Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +105°C) and high temperature operating life (1000 hours, +105°C).

4 Bias error over temperature indicates bias variation from the 25°C reference.

5 Noise density specified for 10 Hz to 40 Hz, at a nominal f_{SM} sample rate, and no digital filtering.

TIMING SPECIFICATIONS

T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

Table 7. Timing Specifications

		Normal Mode			Burst Read Mode			
Parameter	Description	Min	Typ	Max	Min[1]	Typ	Max	Unit
f_{SCLK}	Serial clock	0.1		15	0.1		8	MHz
t_{STALL}	Stall period between data	5			N/A			μs
$t_{READRATE}$	Read rate	10						μs
$t_{\overline{CS}}$	Chip select to SCLK edge	200			200			ns

SPECIFICATIONS

Table 7. Timing Specifications (Continued)

		Normal Mode			Burst Read Mode			
Parameter	Description	Min	Typ	Max	Min[1]	Typ	Max	Unit
t_{DAV}	DOUT valid after SCLK edge			25			25	ns
t_{DSU}	DIN setup time before SCLK rising edge	25			25			ns
t_{DHD}	DIN hold time after SCLK rising edge	50			50			ns
t_{SCLKR}, t_{SCLKF}	SCLK rise and fall times		5	12.5		5	12.5	ns
t_{DR}, t_{DF}	DOUT rise and fall times		5	12.5		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			0			ns
t_{STDR}	Input sync to data ready valid transition		240					µs
	Direct sync mode, Register MSC_CTRL, Bits[3:2] = 01 (binary, see Table 120)		256			256		µs
t_{NV}	Data invalid time		12			12		µs
t_1	Input sync pulse width	5			5			µs
t_2	Input sync period[2]	244			1/(Sync Input Clock)		1/(Sync Input Clock)	µs

1 N/A means not applicable.

2 This specification is rounded up from the cycle time that comes from the maximum input clock frequency (4100 Hz).

Timing Diagrams

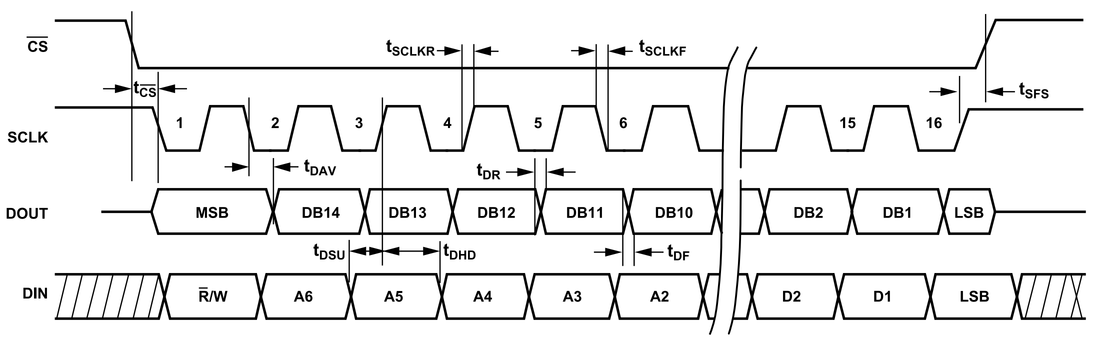

Figure 2. SPI Timing and Sequence Diagram

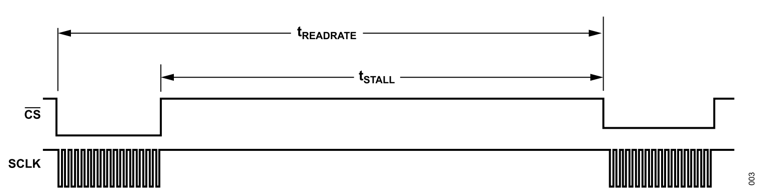

Figure 3. Stall Time and Data Rate Timing Diagram

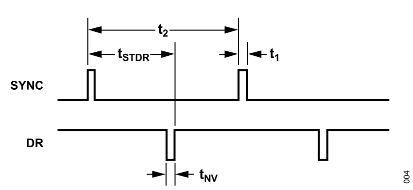

Figure 4. Input Clock Timing Diagram, External Sync Mode, Register MSC_CTRL, Bits[4:2] = 101 (Binary)

ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
Mechanical Shock Survivability	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Temperature	
Calibration Range	−40°C to +85°C
Operating Range	−40°C to +105°C
Storage Range[1]	−55°C to +150°C
Barometric Pressure	2 bar

[1] Extended exposure to temperatures lower than −40°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Pay careful attention to PCB thermal design.

The ADIS16575/ADIS16576/ADIS16577 are a multichip module, which includes many active components. The values Table 9 in identify the thermal response of the hottest component inside of the ADIS16575/ADIS16576/ADIS16577, with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the T_C = 29.3°C (case temperature of the hottest component), the hottest junction inside of the ADIS16575/ADIS16576/ADIS16577 is 29.33°C.

$$T_J = \theta_{JC} \times P_D + 29.3°C$$

$$T_J = 1°C/W \times 0.027\ W + 29.3°C$$

$$T_J = 29.33°C$$

Table 9. Package Characteristics

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	Mass (g)
ML-14-10	53.3°C/W	7.27°C/W	<11

[1] Thermal impedance simulated values come from a case when 4 M2 × 0.4 mm machine screws (torque = 20 inch ounces) secure the ADIS16575/ADIS16576/ADIS16577 to the PCB.

[2] θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

[3] θ_{JC} is the junction to case thermal resistance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

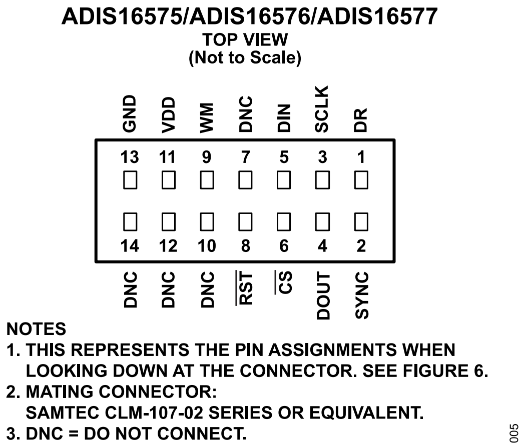

Figure 5. Pin Assignment Package Level View

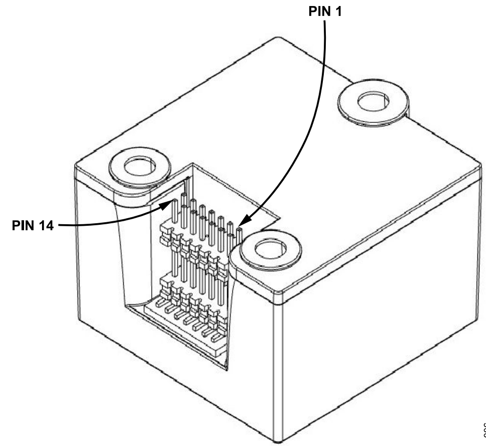

Figure 6. Pin Assignment, Bottom View

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DR	Output	Data Ready Indicator.
2	SYNC	Input and output	External Sync Input and Output, per MSC_CTRL. See Table 120.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. The DOUT pin clocks the output on the SCLK falling edge.
5	DIN	Input	SPI Data Input. The DIN pin clocks the input on the SCLK rising edge.
6	$\overline{\text{CS}}$	Input	SPI Chip Select.
7	DNC	Not applicable	Do Not Connect. Do not connect to the DNC pin.
8	$\overline{\text{RST}}$	Input	Reset (Active Low).
9	WM	Output	Watermark Interrupt Signal That Tracks the First In, First Out (FIFO) Level.
10	DNC	Not applicable	Do Not Connect. Do not connect to the DNC pin.
11	VDD	Supply	Power Supply.
12	DNC	Not applicable	Do Not Connect. Do not connect to the DNC pin.
13	GND	Supply	Power Ground.
14	DNC	Not applicable	Do Not Connect. Do not connect to the DNC pin.

TYPICAL PERFORMANCE CHARACTERISTICS

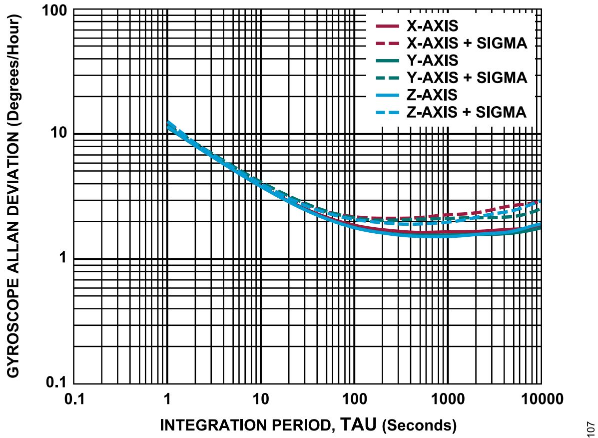

Figure 7. Gyroscope Allan Deviation, T_C = 25°C, ADIS16575-2, ADIS16576-2, and ADIS16577-2

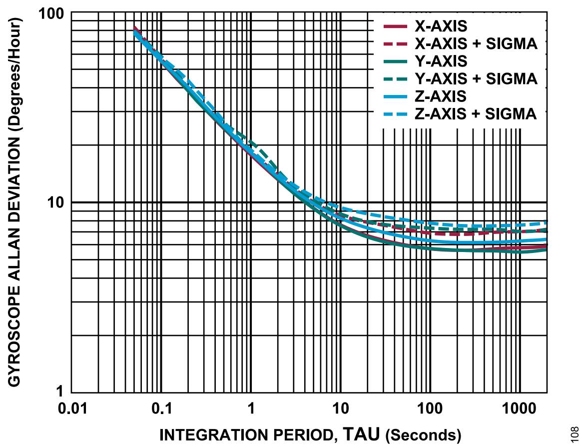

Figure 8. Gyroscope Allan Deviation, T_C = 25°C, ADIS16576-3 and ADIS16577-3

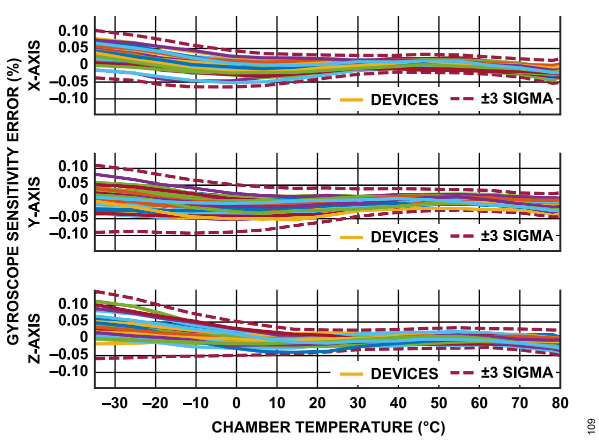

Figure 9. Gyroscope Sensitivity Error vs. Chamber Temperature, ADIS16575-2, ADIS16576-2, and ADIS16577-2

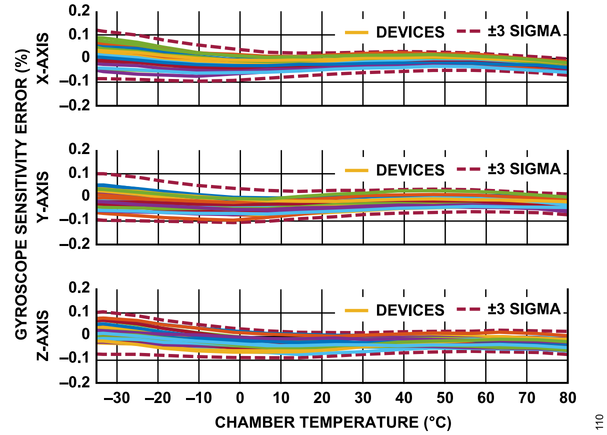

Figure 10. Gyroscope Sensitivity Error vs. Chamber Temperature, ADIS16576-3 and ADIS16577-3

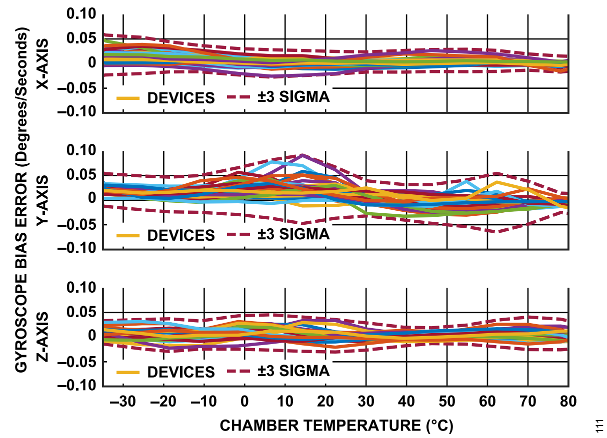

Figure 11. Gyroscope Bias Error vs. Chamber Temperature, ADIS16575-2, ADIS16576-2, and ADIS16577-2

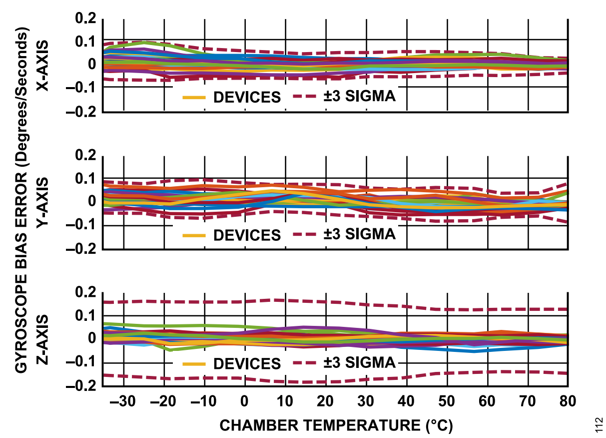

Figure 12. Gyroscope Bias Error vs. Chamber Temperature, ADIS16576-3 and ADIS16577-3

TYPICAL PERFORMANCE CHARACTERISTICS

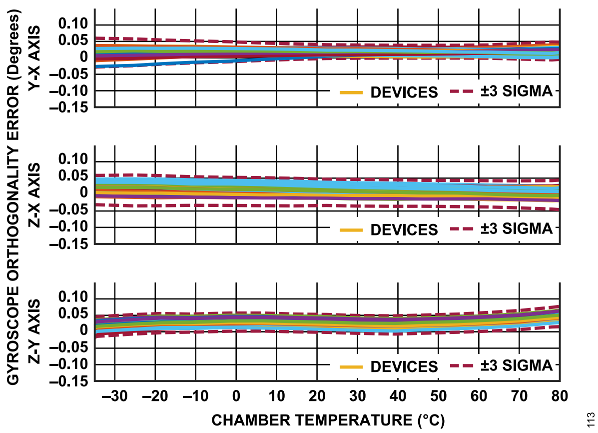

Figure 13. Gyroscope Orthogonality Error vs. Chamber Temperature, ADIS16575-2, ADIS16576-2, and ADIS16577-2

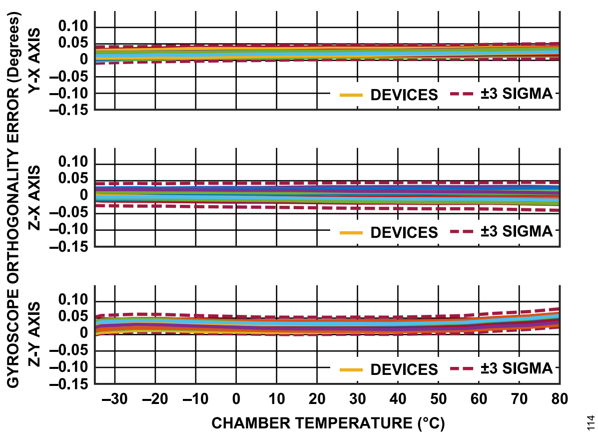

Figure 14. Gyroscope Orthogonality Error vs. Chamber Temperature, ADIS16576-3 and ADIS16577-3

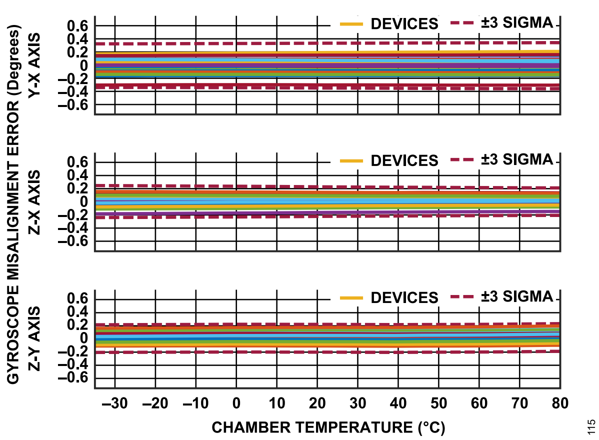

Figure 15. Gyroscope Misalignment Error vs. Chamber Temperature, ADIS16575-2, ADIS16576-2, and ADIS16577-2

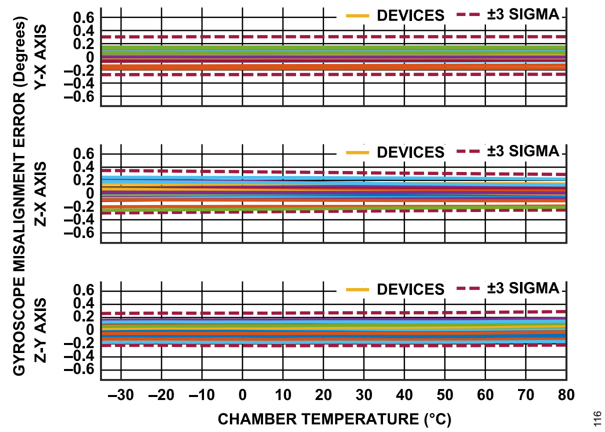

Figure 16. Gyroscope Misalignment Error vs. Chamber Temperature, ADIS16576-3 and ADIS16577-3

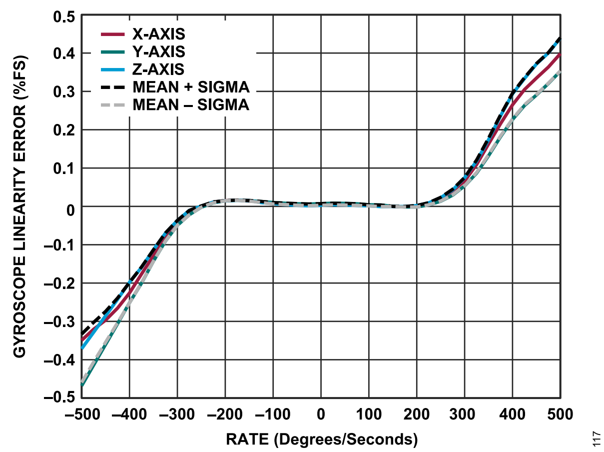

Figure 17. Gyroscope Linearity Error, T_C = 25°C, ADIS16575-2, ADIS16576-2, and ADIS16577-2

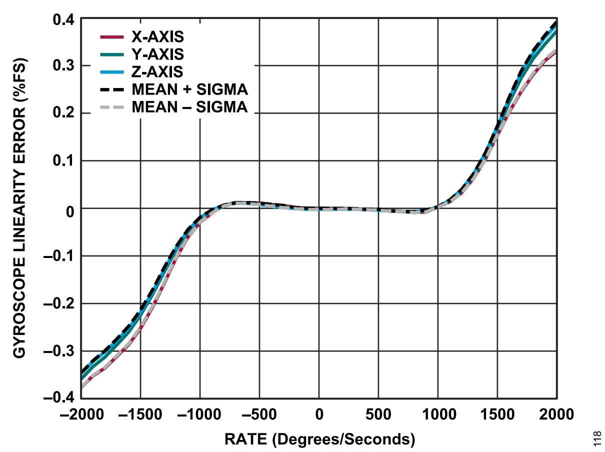

Figure 18. Gyroscope Linearity Error, T_C = 25°C, ADIS16576-3 and ADIS16577-3

TYPICAL PERFORMANCE CHARACTERISTICS

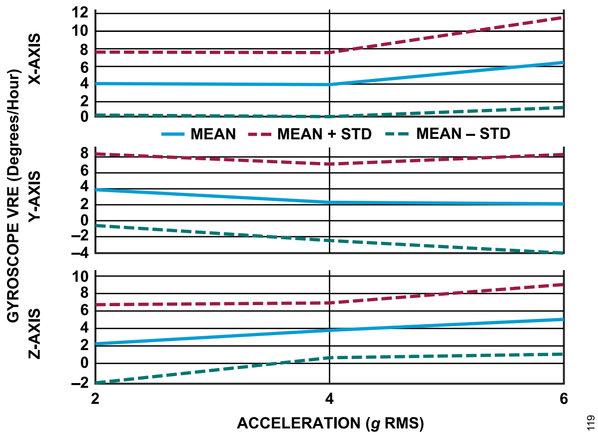

Figure 19. Gyroscope VRE, T_C = 25°C, ADIS16575-2, ADIS16576-2, and ADIS16577-2

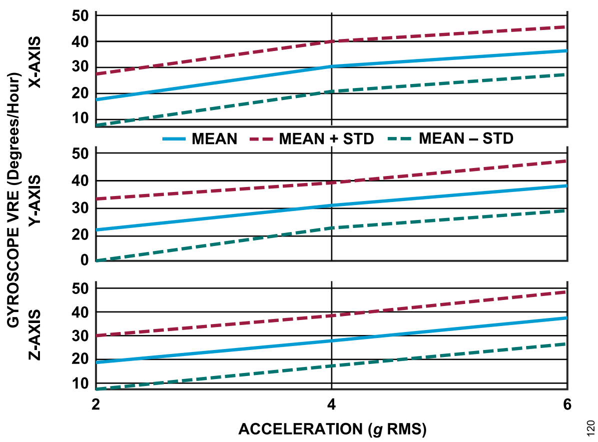

Figure 20. Gyroscope VRE, T_C = 25°C, ADIS16576-3 and ADIS16577-3

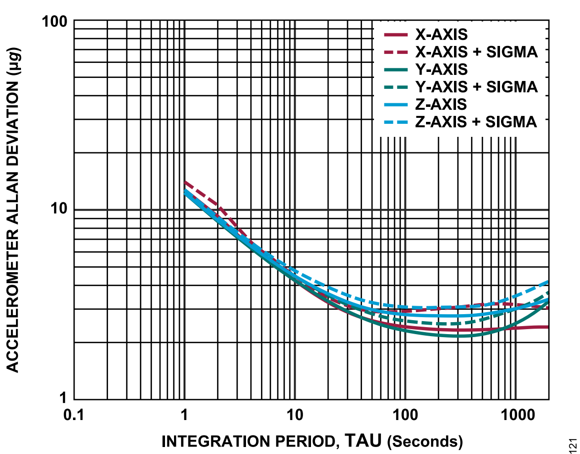

Figure 21. Accelerometer Allan Deviation, T_C = 25°C, ADIS16575

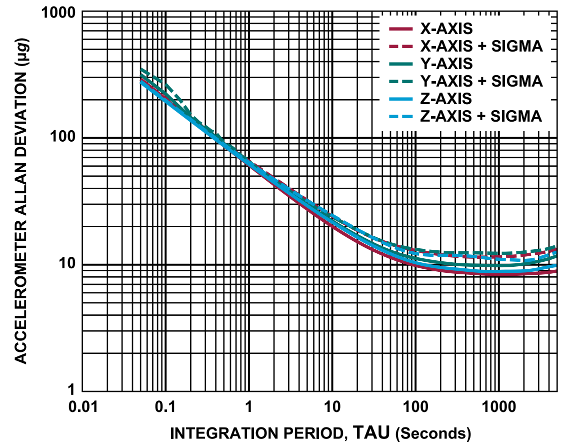

Figure 22. Accelerometer Allan Deviation, T_C = 25°C, ADIS16576

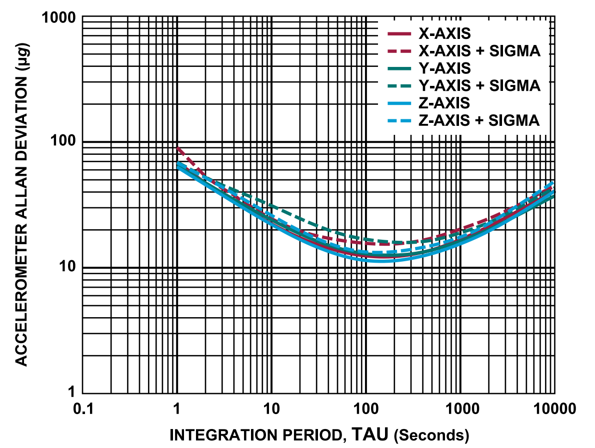

Figure 23. Accelerometer Allan Deviation, T_C = 25°C, ADIS16577

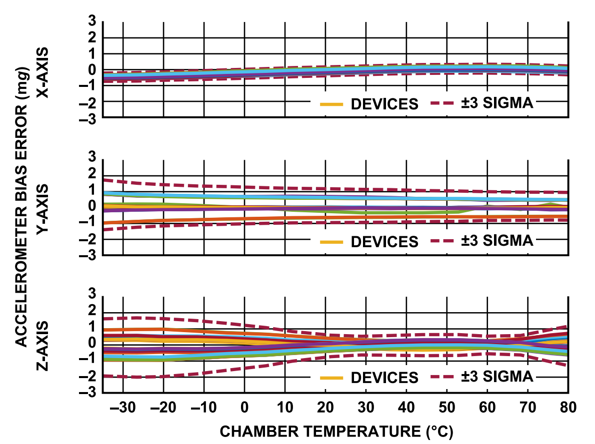

Figure 24. Accelerometer Bias Error vs. Chamber Temperature, ADIS16575

TYPICAL PERFORMANCE CHARACTERISTICS

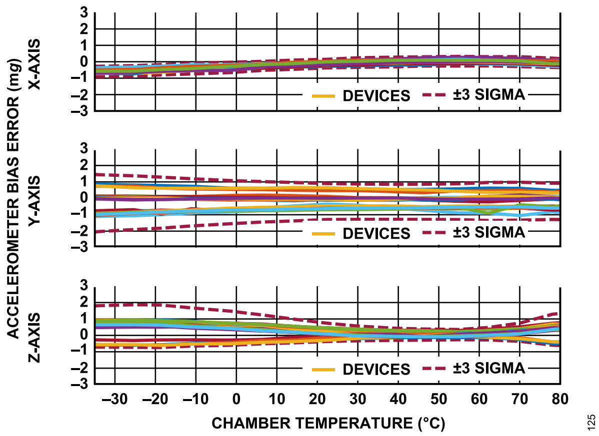

Figure 25. Accelerometer Bias Error vs. Chamber Temperature, ADIS16576

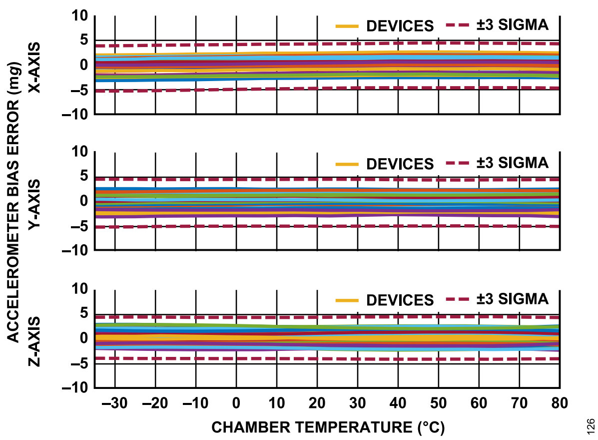

Figure 26. Accelerometer Bias Error vs. Chamber Temperature, ADIS16577

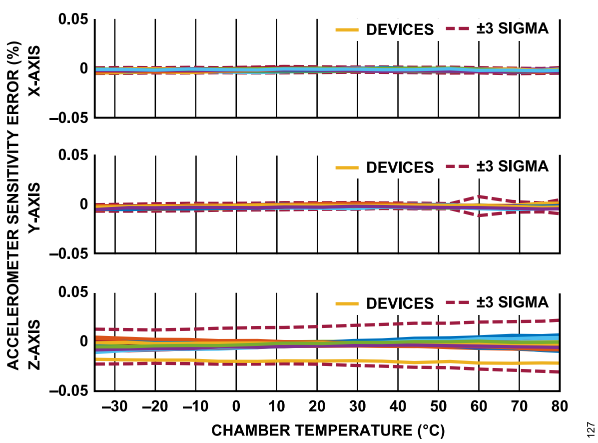

Figure 27. Accelerometer Sensitivity Error vs. Chamber Temperature, ADIS16575

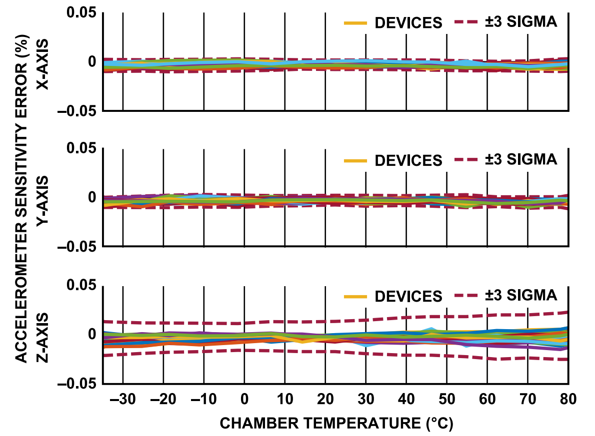

Figure 28. Accelerometer Sensitivity Error vs. Chamber Temperature, ADIS16576

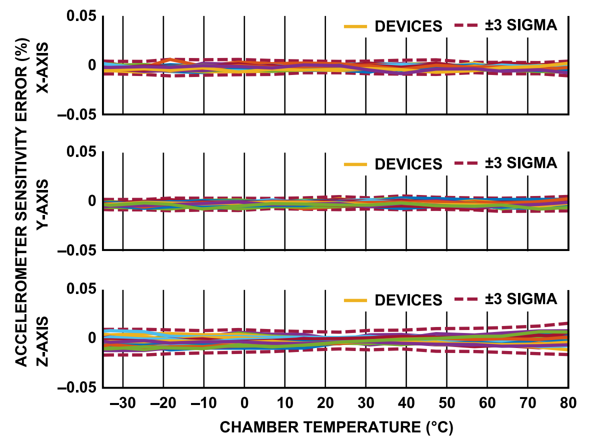

Figure 29. Accelerometer Sensitivity Error vs. Chamber Temperature, ADIS16577

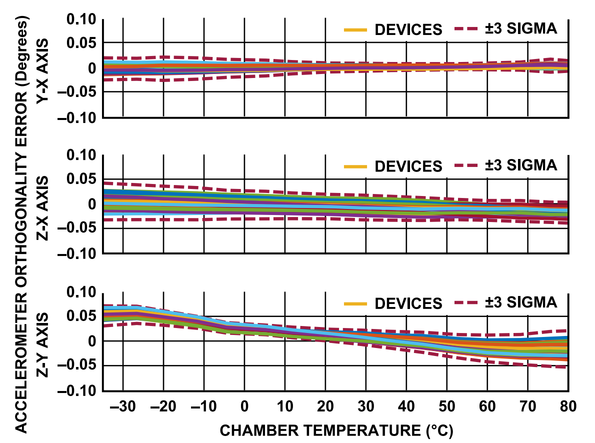

Figure 30. Accelerometer Orthogonality Error vs. Chamber Temperature, ADIS16575

TYPICAL PERFORMANCE CHARACTERISTICS

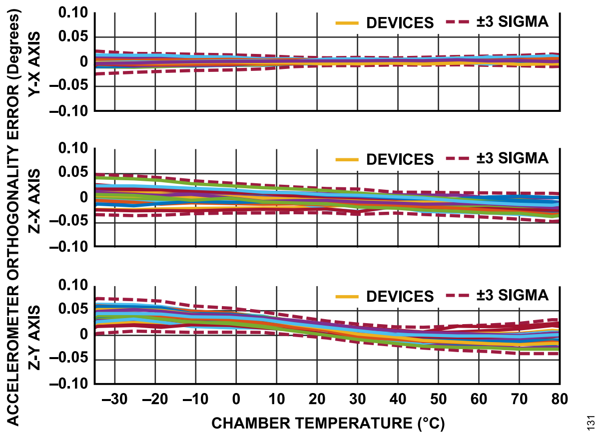

Figure 31. Accelerometer Orthogonality Error vs. Chamber Temperature, ADIS16576

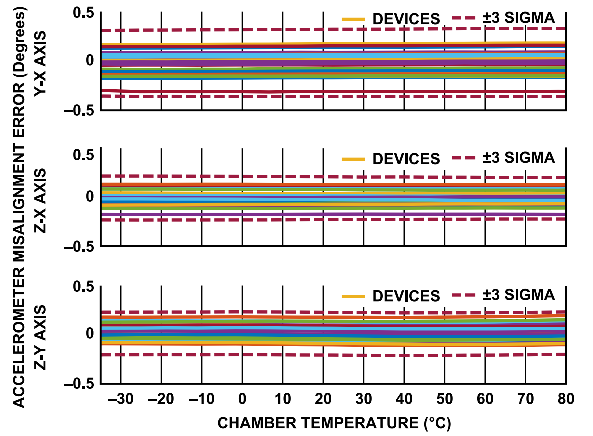

Figure 34. Accelerometer Misalignment Error vs. Channel Temperature, ADIS16576

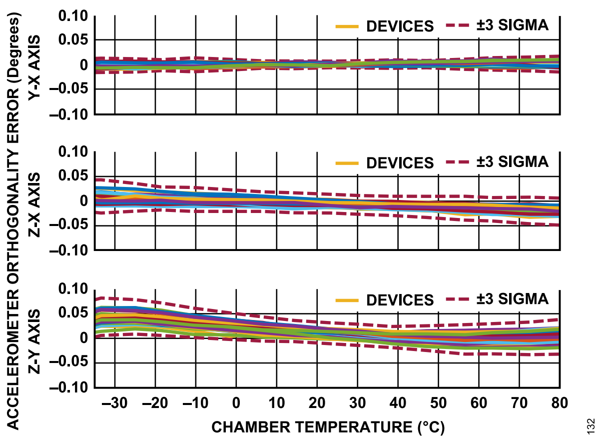

Figure 32. Accelerometer Orthogonality Error vs. Chamber Temperature, ADIS16577

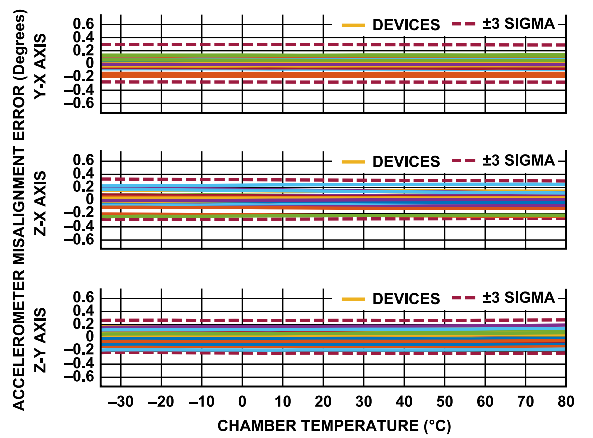

Figure 35. Accelerometer Misalignment Error vs. Chamber Temperature, ADIS16577

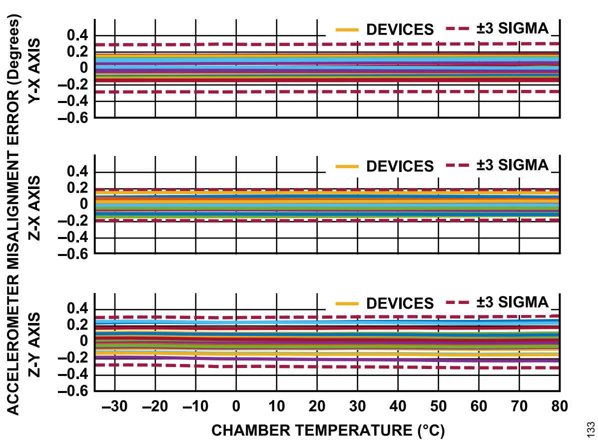

Figure 33. Accelerometer Misalignment Error vs. Chamber Temperature, ADIS16575

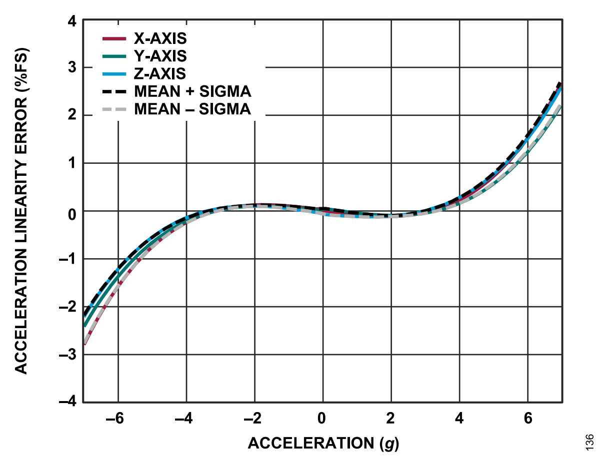

Figure 36. Accelerometer Linearity Error, ADIS16575

TYPICAL PERFORMANCE CHARACTERISTICS

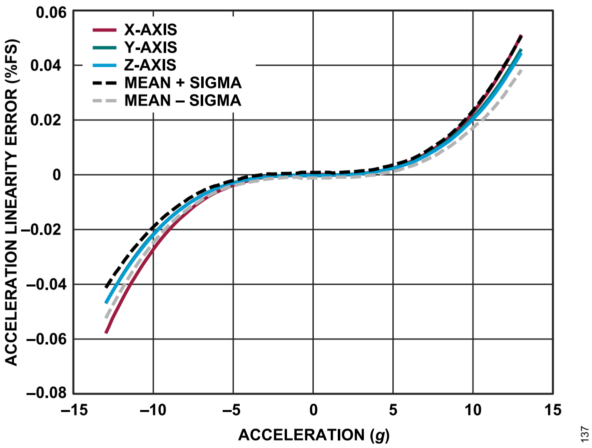

Figure 37. Accelerometer Linearity Error, ADIS16576

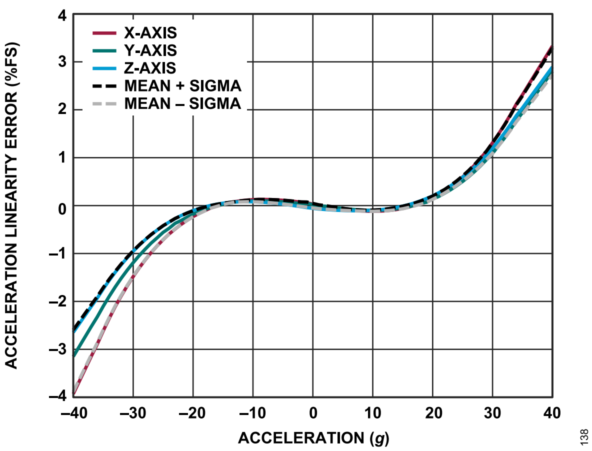

Figure 38. Accelerometer Linearity Error, ADIS16577

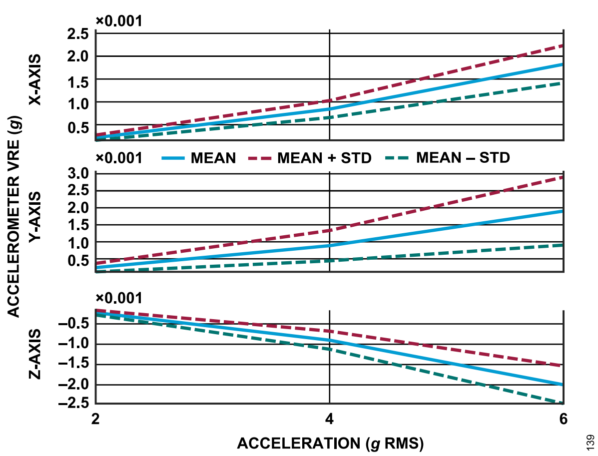

Figure 39. Accelerometer Vibration Rectification Error, T_C = 25°C, ADIS16576

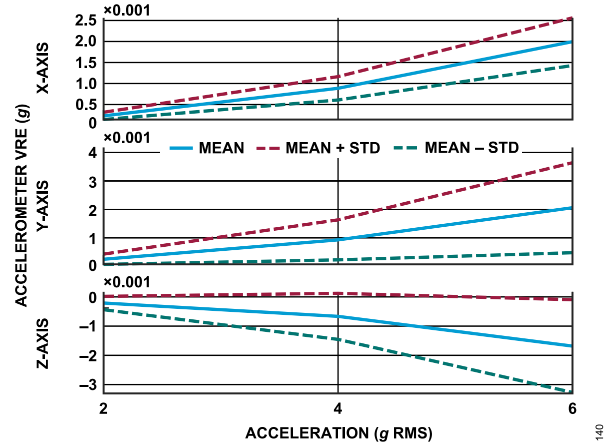

Figure 40. Accelerometer Vibration Rectification Error, T_C = 25°C, ADIS16577

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INTRODUCTION

Upon power-up or reset, with all control registers set to their factory defaults, the IMU automatically starts continuous sampling, processing, and loading of calibrated sensor data into the output registers at a rate of 2000 SPS. If the SYNC_4KHZ mode is enabled (controlled by MSC_CTRL, Bit 11, Table 120), an internal sampling rate of 4000 SPS is available. During the initial power-on or after a reset, the IMU performs a series of diagnostic tests, including sensor-level self tests and cyclic redundancy check (CRC) computations of the program memory that is loaded from the flash into random access memory (RAM), ensuring the integrity of the system before beginning data sampling and processing.

INERTIAL SENSOR SIGNAL CHAIN

Figure 41 shows the basic signal chain for the inertial sensors in the IMU. When operating in internal clock mode (the factory default setting, see Register MSC_CTRL, Bits [3:2], Table 120), the nominal output data rate (ODR) is 2000 SPS.

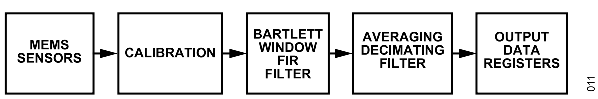

Figure 41. Signal Processing Diagram, Inertial Sensors

Gyroscope Data Sampling

The three gyroscopes produce angular rate measurements around three mutually orthogonal axes (x, y, and z). Figure 42 shows the data sampling plan for each gyroscope when the ADIS16575/ADIS16576/ADIS16577 operate in internal clock mode (default, see Register MSC_CTRL, Bits[3:2] in Table 120). Each gyroscope has an analog-to-digital converter (ADC) and sample clock (f_{SG}) that drives data sampling at a fixed rate, based on the gyroscope resonator (nominally 4 kHz). The ADC output is fed into the cascaded, integrator-comb (CIC) interpolator, which synchronizes with the IMU sample clock. The interpolation filter enables all inertial sensor measurements to be captured synchronously.

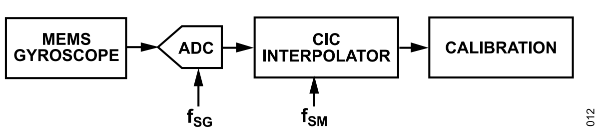

Figure 42. Gyroscope Data Sampling

Accelerometer Data Sampling

The three accelerometers produce linear acceleration measurements along the same mutually orthogonal axes (x, y, and z) as the gyroscopes. Figure 43 shows the data sampling plan for each accelerometer when the ADIS16575/ADIS16576/ADIS16577 operate in internal clock mode (default, see Register MSC_CTRL, Bits[3:2] in Table 120). Like the gyroscopes, each accelerometer is equipped with an ADC and a sample clock that drives data sampling at a fixed rate. The ADC output is fed into the CIC interpolator, which synchronizes with the IMU sample clock. The interpolation filter enables all inertial sensor measurements to be captured synchronously.

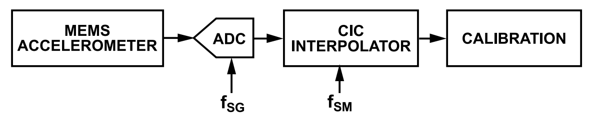

Figure 43. Accelerometer Data Sampling

External Clock Options

The ADIS16575/ADIS16576/ADIS16577 provide three different modes of operation that support these devices using an external clock to control the internal processing rate (f_{SM} in Figure 42 and Figure 43) through the SYNC pin. The MSC_CTRL register (see Table 120) provides the configuration options for these external clock modes in Bits[3:2].

Inertial Sensor Calibration

The inertial sensor calibration function for the gyroscopes and the accelerometers has two components: factory calibration and user calibration (see Figure 41).

The factory calibration of the gyroscope applies the following correction formulas to the data of each gyroscope:

$$\begin{pmatrix}\omega_{XC}\\ \omega_{YC}\\ \omega_{ZC}\end{pmatrix} = \begin{pmatrix} m_{11} & m_{12} & m_{13}\\ m_{21} & m_{22} & m_{23}\\ m_{31} & m_{32} & m_{33}\end{pmatrix} \times \left(\begin{pmatrix}\omega_X\\ \omega_Y\\ \omega_Z\end{pmatrix} + \begin{pmatrix}b_X\\ b_Y\\ b_Z\end{pmatrix}\right)$$

where:
ω_{XC}, ω_{YC}, and ω_{ZC} are the gyroscope outputs (post calibration).
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} provide scale and alignment correction.
ω_X, ω_Y, and ω_Z are the gyroscope outputs (precalibration).
b_X, b_Y, and b_Z provide bias correction.

All of the correction factors in this relationship come from direct observation of the response of each gyroscope at multiple temperatures over the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but these factors are not available for observation or configuration. See

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Figure 68 for more details on the user calibration options available for the gyroscopes.

The factory calibration of the accelerometer applies the following correction formulas to the data of each accelerometer:

$$\begin{pmatrix} a_{XC} \\ a_{YC} \\ a_{ZC} \end{pmatrix} = \begin{pmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{pmatrix} \times \left(\begin{pmatrix} a_X \\ a_Y \\ a_Z \end{pmatrix} + \begin{pmatrix} b_X \\ b_Y \\ b_Z \end{pmatrix} \right) + \begin{pmatrix} 0 & p_{12} & p_{13} \\ p_{21} & 0 & p_{23} \\ p_{31} & p_{32} & 0 \end{pmatrix} \times \begin{pmatrix} \omega^2{}_{XC} \\ \omega^2{}_{YC} \\ \omega^2{}_{ZC} \end{pmatrix}$$

where:
a_{XC}, a_{YC}, and a_{ZC} are the accelerometer outputs (post calibration).
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} provide scale and alignment correction.
a_X, a_Y, and a_Z are the accelerometer outputs (precalibration).
b_X, b_Y, and b_Z provide bias correction.
p_{12}, p_{13}, p_{21}, p_{23}, p_{31}, and p_{32} provide a point of percussion alignment correction (see Figure 71).
$\omega^2{}_{XC}$, $\omega^2{}_{YC}$, *and* $\omega^2{}_{ZC}$ are the square of the gyroscope outputs (post calibration).

All of the correction factors in this relationship come from direct observation of the response of each accelerometer at multiple temperatures over the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but these factors are not available for observation or configuration. Register MSC_CTRL, Bit 6 (see Table 120) provides the only user configuration option for the factory calibration of the accelerometers: an on/off control for the point of percussion, alignment function. See Figure 69 for more details on the user calibration options available for the accelerometers.

Bartlett Window FIR Filter

The Bartlett window finite impulse response (FIR) filter (see Figure 44) contains two averaging filter stages in a cascade configuration. The FILT_CTRL register (see Table 116) provides the configuration controls for this filter.

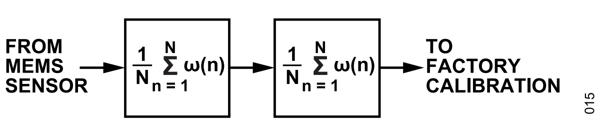

Figure 44. Bartlett Window FIR Filter Signal Path

Averaging and Decimating Filter

The second digital filter averages multiple samples together to produce each register update. In this type of filter structure, the number of samples in the average is equal to the reduction in the update rate for the output data registers. The DEC_RATE register (see Table 124) provides the configuration controls for this filter.

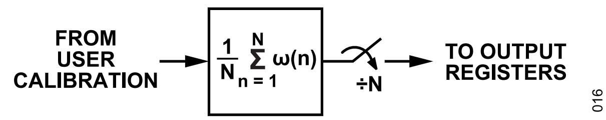

Figure 45. Averaging and Decimating Filter Diagram

REGISTER STRUCTURE

All communication between the ADIS16575/ADIS16576/ADIS16577 and an external processor involves either reading the contents of an output register or writing configuration or command information to a control register. The output data registers include the latest sensor data, error flags, and identification information. The control registers include sample rate, filtering, calibration, and diagnostic options. Each user accessible register has two bytes (upper and lower), each of which has a unique address. See Table 13 for a detailed list of all user registers and their corresponding addresses.

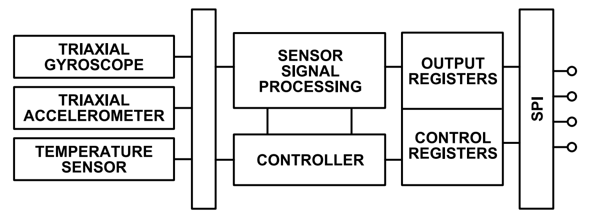

Figure 46. Basic Operation of the ADIS16575/ADIS16576/ADIS16577

SPI

The SPI provides access to the user registers (see Table 13). Figure 47 shows the most common connections between the ADIS16575/ADIS16576/ADIS16577 and an SPI main device, which is often an embedded processor with an SPI-compatible interface. In this example, the SPI main uses an interrupt service routine to collect data every time the data ready (DR) signal pulses.

Additional information on the SPI of the ADIS16575/ADIS16576/ADIS16577 can be found in the SPI Operation section.

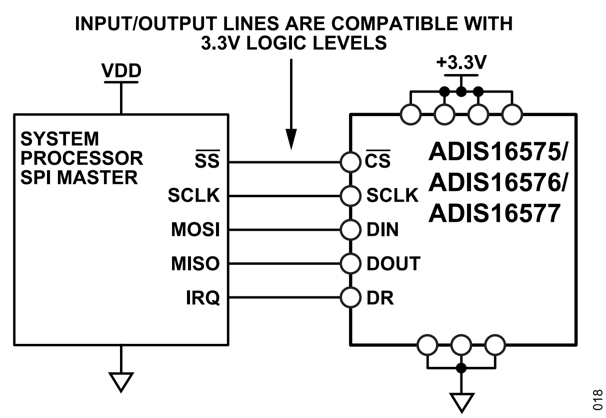

Figure 47. Electrical Connection Diagram

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Table 11. Generic Host Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Device select
SCLK	Serial clock
MOSI	Host output, peripheral input
MISO	Host input, peripheral output
IRQ	Interrupt request

Embedded processors typically use control registers to configure their serial ports for communicating with SPI serial devices, such as the ADIS16575/ADIS16576/ADIS16577. Table 12 provides a list of settings that describe the SPI protocols of the ADIS16575/ ADIS16576/ADIS16577. The initialization routine of the central processor typically establishes these settings using firmware commands to write parameters such as SPI mode, clock polarity (CPOL), clock phase (CPHA), bit order, and clock frequency into the control registers, ensuring proper communication between the processor and the IMU.

Table 12. Generic Master Processor SPI Settings

Processor Setting	Description
Host Controller	IMU operates as peripheral
SCLK ≤ 15 MHz[1]	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence, see Figure 53 for coding
16-Bit Mode	Shift register and data length

1 A burst mode read requires this value to be ≤8 MHz (see Table 7 for more information).

DR

The factory default configuration provides users with a DR signal on the DR pin (see Table 10) that pulses when the output data registers update. Connect the DR pin to a pin on the embedded processor to trigger data collection on the second edge of this pulse. Register MSC_CTRL, Bit 0 (see Table 120), controls the polarity of this signal. In Figure 48, Register MSC_ CTRL, Bit 0 = 1, meaning data collection must start on the rising edges of the DR pulses.

Figure 48. Data Ready When Register MSC_CTRL, Bit 0 = 1 (Default)

During the start-up and reset recovery processes, the DR signal may exhibit transient behavior before data production begins. Figure 49 shows an example of the DR behavior during startup, and Figure 50 and Figure 51 provide examples of the DR behavior during recovery from reset commands.

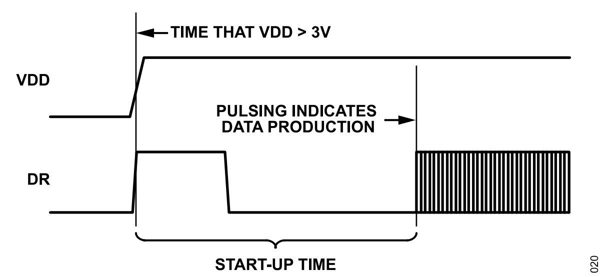

Figure 49. Data Ready Response During Startup

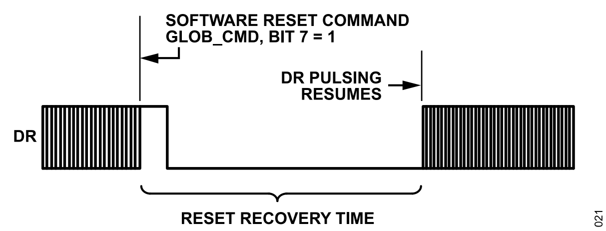

Figure 50. Data Ready Response During Reset (Register GLOB_CMD, Bit 7 = 1) Recovery

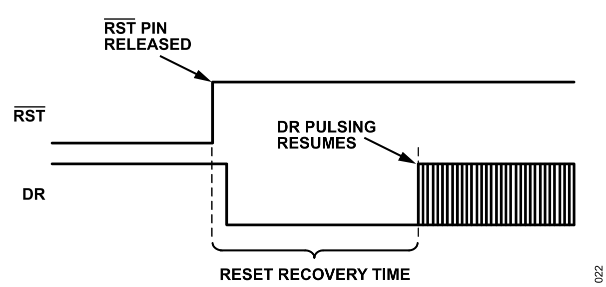

Figure 51. Data Ready Response During Reset ($\overline{RST}$ = 0) Recovery

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READING SENSOR DATA

Reading a single register requires two 16-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 16-bit command code (see Figure 53) for a read request on the SPI has three parts: the read bit ($\overline{R}$/W = 0), either address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. Figure 52 shows an example that includes two register reads in succession. This example starts with DIN = 0x0C00 to request the contents of the Z_GYRO_LWR register, and follows with 0x0E00 to request the contents of the Z_GYRO_UPR register. The sequence in Figure 52 also shows a full duplex mode of operation, meaning that the ADIS16575/ADIS16576/ADIS16577 can receive requests on DIN while also transmitting data out on DOUT within the same 16-bit SPI cycle.

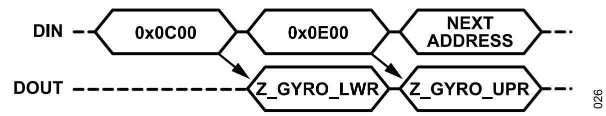

Figure 52. SPI Read Example

Figure 54 shows an example of the four SPI signals in a repeating pattern when reading the PROD_ID register (see Table 136) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI setup and communications because the signals are the same for each 16-bit sequence, except during the first cycle.

Note that the read and write functions of the SPI are always 16 bits long. The only exception is the burst read function described in the Burst Read Function section.

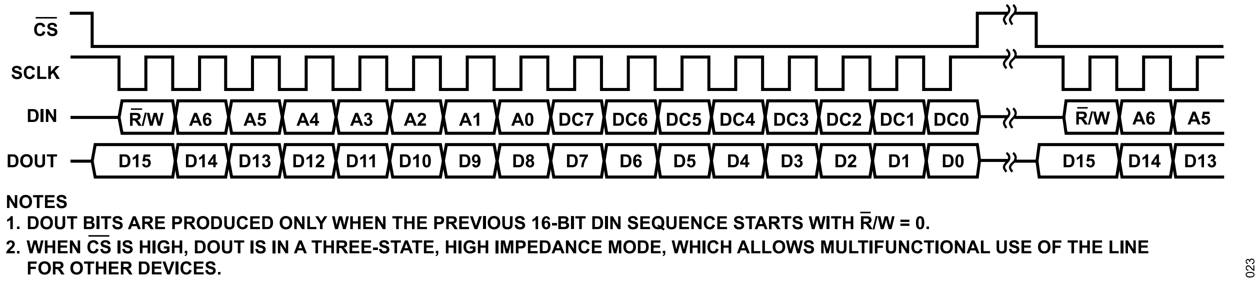

Figure 53. SPI Communication Bit Sequence

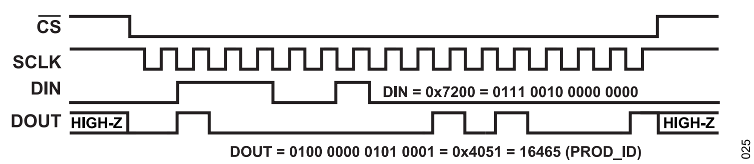

Figure 54. SPI Signal Pattern, Repeating Read of the PROD_ID Register

THEORY OF OPERATION

Burst Read Function

The burst read function provides a method to read a batch of output data registers using a continuous stream of bits, without requiring a stall time between 16-bit communication frames (see Figure 3) at an SCLK rate of up to 8 MHz. To start this mode, set DIN = 0x6800 and then read each register in the sequence out of DOUT while keeping $\overline{\text{CS}}$ low for the entire sequence.

The burst mode data format and length depends on three user-configuration settings: scaled sync mode on or off (Bits[3:2], Table 120), the BURST_32 bit enabled or disabled (Bit 9, see Table 120), or the OUT_SEL bit = 0 or the OUT_SEL bit = 1 (Bit 8, see Table 120), which results in eight possible burst data formats.

Figure 55 shows the 16-bit burst sequence, detailing the data registers transmitted in each burst and the position of the checksum.

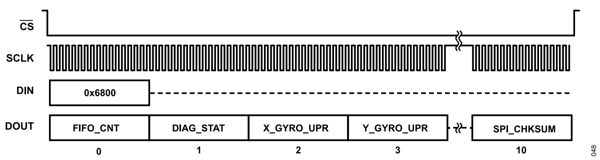

Figure 55. 16-Bit SPI Burst Sequence

Figure 56 captures the 32-bit burst sequence, showing the data flow from FIFO_CNT, DIAG_STAT, and sensor registers, followed by the SPI_CHKSUM

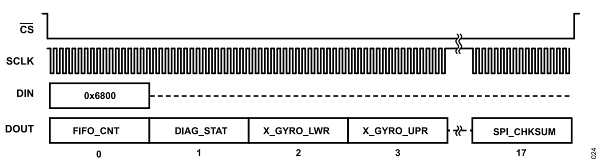

Figure 56. 32-BIt SPI Burst Sequence

Figure 57 illustrates a 16-bit burst sequence, showing how the 0x6800 command initiates the burst and the subsequent data output. Figure 57 shows that 0x6800 was transmitted during the first set of clock pulses and starts outputting data words in the following frame upon receiving any SPI command. (Note that in Figure 57, 0x6800 is shown requesting the next burst).

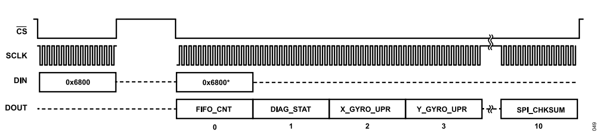

Figure 57. 16-Bit SPI Burst Sequence with Command Example

Scaled Sync Mode Enabled vs. Disabled

The only differences in the burst data format between enabled and disabled are the final two bytes in the burst read response. In scaled sync mode, the final two bytes are the values of the TIME_STAMP_LWR and TIME_STAMP_UPR registers. When scaled sync mode is disabled, the final two bytes are the values in the DATA_CNTR register. Note that, in both modes, Bits[15:8] appear before Bits[7:0].

16-Bit Burst Mode with OUT_SEL = 0

In 16-bit burst mode with OUT_SEL = 0, a burst contains calibrated gyroscope and accelerometer data in 16-bit format. Refer to Table 88 for the detailed burst read sequence and corresponding registers. Use the 16-bit mode when using no filtering (decimation or Bartlett) in the signal path.

To ensure the integrity of data from a burst read, calculate the checksum of the received data (excluding the FIFO_CNT register) and compare it with the 16-bit checksum value provided in the burst read. For an example of how to calculate the checksum, refer to the SPI Checksum (SPI_CHKSUM) section.

Note that this mode is compatible with the legacy burst mode of the ADIS16460, ADIS16465, and ADIS16467 IMUs.

16-Bit Burst Mode with OUT_SEL = 1

In 16-bit burst mode with OUT_SEL = 1, a burst contains calibrated delta angle and delta velocity data in 16-bit format. Refer to Table 88 for the detailed burst read sequence and corresponding registers. Use the 16-bit mode when no filtering (decimation or Bartlett) is applied in the signal path.

To ensure the integrity of data from a burst read, calculate the checksum of the received data (excluding the FIFO_CNT register) and compare it with the 16-bit checksum value provided in the burst read. For an example of how to calculate the checksum, refer to the SPI Checksum (SPI_CHKSUM) section.

32-Bit Burst Mode with OUT_SEL = 0

In 32-bit burst mode with OUT_SEL = 0, the burst includes calibrated gyroscope and accelerometer data in 32-bit format. Refer to Table 88 for the detailed burst read sequence and corresponding registers. Use the 32-bit mode when averaging (decimation) and/or low-pass data filtering is applied, and higher precision is required.

To ensure the integrity of data from a burst read, calculate the checksum of the received data (excluding the FIFO_CNT register) and compare it with the 16-bit checksum value provided in the burst read. For an example of how to calculate the checksum, refer to the SPI Checksum (SPI_CHKSUM) section.

32-Bit Burst Mode with OUT_SEL = 1

In 32-bit burst mode with OUT_SEL = 1, a burst contains calibrated delta angle and delta velocity data in 32-bit format. Refer to Table 88 for the detailed burst read sequence and corresponding registers. Use the 32-bit mode when averaging (decimation) or low-pass data filtering is applied, and higher precision is required.

To ensure the integrity of data from a burst read, calculate the checksum of the received data (excluding the FIFO_CNT register)

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and compare it with the 16-bit checksum value provided in the burst read. For an example of how to calculate the checksum, refer to the SPI Checksum (SPI_CHKSUM) section.

DEVICE CONFIGURATION

Each configuration register contains 16 bits (two bytes). Bits[7:0] contain the low byte, and Bits[15:8] contain the high byte of each register. Each byte has a unique address in the user register map (see Table 13). Updating the contents of a register requires writing to both bytes in the following sequence: low byte first and high byte second.

The three parts to coding an SPI command (see Table 13) that writes a new byte of data to a register include the following:

1. The write bit ($\overline{R}$/W = 1),
2. The address of the byte, [A6:A0],
3. The new data for that location, [DC7:DC0].

For example, Figure 58 shows a coding example for writing 0x0004 to the FILT_CTRL register (see Table 116). The 0xDC04 command writes 0x04 to Address 0x5C (the lower byte), and the 0xDD00 command writes 0x00 to Address 0x5D (the upper byte).

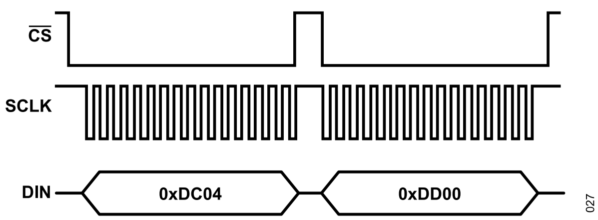

Figure 58. SPI Sequence for Writing 0x0004 to FILT_CTRL

Note that writing to the control registers may trigger internal processing on the ADIS16575/ADIS16576/ADIS16577. The new register value may not be available immediately for readback until this processing is complete, and the value is fully applied. Consider this behavior when verifying register writes.

Memory Structure

Figure 59 shows a functional diagram for the dual memory structure of the ADIS16575/ADIS16576/ADIS16577. The flash memory bank contains the operational code, unit-specific calibration coefficients, and user configuration settings. The static random access memory (SRAM) supports high-speed, real-time operation. Two copies of this data reside in flash memory for redundancy and error recovery. During initialization (power application or reset recovery), the firmware loads the most recent copy of the configuration data from the flash memory into the SRAM, which supports all normal operation, including register access through the SPI.

Writing to a configuration register using the SPI updates the corresponding SRAM location but does not automatically update the settings in the flash memory bank. To save these settings to flash memory, the manual flash memory update command (Register GLOB_CMD, Bit 3, see Table 128) must be used. This command updates both copies of the data in the flash memory sequentially, ensuring that at least one valid copy is always available.

Registers that have flash memory backup display **Yes** in the Flash Backup column of Table 13.

During power-on or reset recovery, the ADIS16575/ADIS16576/ADIS16577 perform a CRC on the factory register data and user register data stored in flash memory. The firmware uses this check to determine which copy of the register data to load. If a CRC mismatch is detected, the memory error bit in the DIAG_STAT register (Bit 6) is set. Note that there is no redundancy for the operational code itself; corruption in the code also results in the MEM bit being set in the DIAG_STAT register.

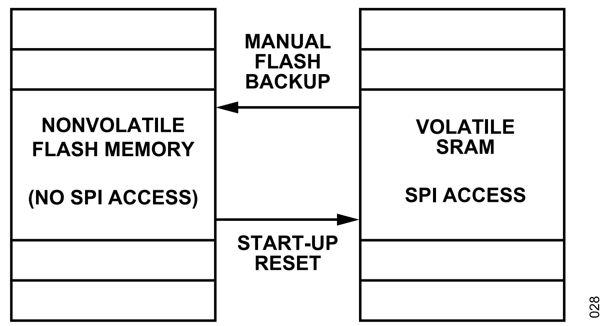

Figure 59. SRAM and Flash Memory Diagram

USER REGISTER MEMORY MAP

Table 13. User Register Memory Map (N/A Means Not Applicable)

Name	R/W	Flash Backup	Address	Default	Register Description
PAGE_ID	N/A	N/A	0x00, 0x01	N/A	Reserved
DIAG_STAT	R	No	0x02, 0x03	0x0000	Output, diagnostic flags
X_GYRO_LWR	R	No	0x04, 0x05	N/A	Output, x-axis gyroscope, low word
X_GYRO_UPR	R	No	0x06, 0x07	N/A	Output, x-axis gyroscope, high word
Y_GYRO_LWR	R	No	0x08, 0x09	N/A	Output, y-axis gyroscope, low word
Y_GYRO_UPR	R	No	0x0A, 0x0B	N/A	Output, y-axis gyroscope, high word
Z_GYRO_LWR	R	No	0x0C, 0x0D	N/A	Output, z-axis gyroscope, low word
Z_GYRO_UPR	R	No	0x0E, 0x0F	N/A	Output, z-axis gyroscope, high word
X_ACCL_LWR	R	No	0x10, 0x11	N/A	Output, x-axis accelerometer, low word
X_ACCL_UPR	R	No	0x12, 0x13	N/A	Output, x-axis accelerometer, high word
Y_ACCL_LWR	R	No	0x14, 0x15	N/A	Output, y-axis accelerometer, low word
Y_ACCL_UPR	R	No	0x16, 0x17	N/A	Output, y-axis accelerometer, high word
Z_ACCL_LWR	R	No	0x18, 0x19	N/A	Output, z-axis accelerometer, low word
Z_ACCL_UPR	R	No	0x1A, 0x1B	N/A	Output, z-axis accelerometer, high word
TEMP	R	No	0x1C, 0x1D	N/A	Output, temperature
TIME_STAMP_LWR	R	No	0x1E, 0x1F	N/A	Output, time stamp, low word
TIME_STAMP_UPR	R	No	0x20, 0x21	N/A	Output, time stamp, high word
DATA_CNTR	R	No	0x22, 0x23	N/A	New data counter
X_DELTANG_LWR	R	No	0x24, 0x25	N/A	Output, x-axis delta angle, low word
X_DELTANG_UPR	R	No	0x26, 0x27	N/A	Output, x-axis delta angle, high word
Y_DELTANG_LWR	R	No	0x28, 0x29	N/A	Output, y-axis delta angle, low word
Y_DELTANG_UPR	R	No	0x2A, 0x2B	N/A	Output, y-axis delta angle, high word
Z_DELTANG_LWR	R	No	0x2C, 0x2D	N/A	Output, z-axis delta angle, low word
Z_DELTANG_UPR	R	No	0x2E, 0x2F	N/A	Output, z-axis delta angle, high word
X_DELTVEL_LWR	R	No	0x30, 0x31	N/A	Output, x-axis delta velocity, low word
X_DELTVEL_UPR	R	No	0x32, 0x33	N/A	Output, x-axis delta velocity, high word
Y_DELTVEL_LWR	R	No	0x34, 0x35	N/A	Output, y-axis delta velocity, low word
Y_DELTVEL_UPR	R	No	0x36, 0x37	N/A	Output, y-axis delta velocity, high word
Z_DELTVEL_LWR	R	No	0x38, 0x39	N/A	Output, z-axis delta velocity, low word
Z_DELTVEL_UPR	R	No	0x3A, 0x3B	N/A	Output, z-axis delta velocity, high word
FIFO_CNT	R	No	0x3C, 0x3D	N/A	Output, FIFO sample count
SPI_CHKSUM	R	No	0x3E, 0x3F	N/A	Output, current sample SPI checksum
XG_BIAS_LWR	R/W	Yes	0x40, 0x41	0x0000	Calibration, offset, gyroscope, x-axis, low word
XG_BIAS_UPR	R/W	Yes	0x42, 0x43	0x0000	Calibration, offset, gyroscope, x-axis, high word
YG_BIAS_LWR	R/W	Yes	0x44, 0x45	0x0000	Calibration, offset, gyroscope, y-axis, low word
YG_BIAS_UPR	R/W	Yes	0x46, 0x47	0x0000	Calibration, offset, gyroscope, y-axis, high word
ZG_BIAS_LWR	R/W	Yes	0x48, 0x49	0x0000	Calibration, offset, gyroscope, z-axis, low word
ZG_BIAS_UPR	R/W	Yes	0x4A, 0x4B	0x0000	Calibration, offset, gyroscope, z-axis, high word
XA_BIAS_LWR	R/W	Yes	0x4C, 0x4D	0x0000	Calibration, offset, accelerometer, x-axis, low word
XA_BIAS_UPR	R/W	Yes	0x4E, 0x4F	0x0000	Calibration, offset, accelerometer, x-axis, high word
YA_BIAS_LWR	R/W	Yes	0x50, 0x51	0x0000	Calibration, offset, accelerometer, y-axis, low word
YA_BIAS_UPR	R/W	Yes	0x52, 0x53	0x0000	Calibration, offset, accelerometer, y-axis, high word
ZA_BIAS_LWR	R/W	Yes	0x54, 0x55	0x0000	Calibration, offset, accelerometer, z-axis, low word
ZA_BIAS_UPR	R/W	Yes	0x56, 0x57	0x0000	Calibration, offset, accelerometer, z-axis, high word
Reserved	N/A	N/A	0x58 to 0x59	N/A	Reserved
FIFO_CTRL	R/W	Yes	0x5A, 0x5B	N/A	Control, output FIFO and watermark interrupt
FILT_CTRL	R/W	Yes	0x5C, 0x5D	0x0000	Control, Bartlett window FIR filter
RNG_MDL	R	No	0x5E, 0x5F	N/A[1]	Measurement range (model specific) identifier
MSC_CTRL	R/W	Yes	0x60, 0x61	0x00C1	Control, input, output, and other miscellaneous options

USER REGISTER MEMORY MAP

Table 13. User Register Memory Map (N/A Means Not Applicable) (Continued)

Name	R/W	Flash Backup	Address	Default	Register Description
UP_SCALE	R/W	Yes	0x62, 0x63	0x07D0	Control, scale factor for input clock, PPS mode
DEC_RATE	R/W	Yes	0x64, 0x65	0x0000	Control, decimation filter (ODR)
NULL_CTRL	R/W	Yes	0x66, 0x67	0x070A	Control, bias estimation period
GLOB_CMD	W	No	0x68, 0x69	N/A	Control, global commands
Reserved	N/A	N/A	0x6A to 0x6B	N/A	Reserved
FW_REV	R	No	0x6C, 0x6D	N/A	Identification, firmware revision
DAY_MONTH	R	No	0x6E, 0x6F	N/A	Identification, date code, day and month
YEAR	R	No	0x70, 0x71	N/A	Identification, date code, year
PROD_ID	R	No	0x72, 0x73	0x40BF[2]	Identification, device number
SERIAL_NUM	R	No	0x74, 0x75	N/A	Identification, serial number
USER_SCR_1	R/W	Yes	0x76, 0x77	N/A	User Scratch Register 1
USER_SCR_2	R/W	Yes	0x78, 0x79	N/A	User Scratch Register 2
USER_SCR_3	R/W	Yes	0x7A, 0x7B	N/A	User Scratch Register 3
FLSHCNT_LWR	R	No	0x7C, 0x7D	N/A	Output, flash memory write cycle counter, lower word
FLSHCNT_UPR	R	No	0x7E, 0x7E	N/A	Output, flash memory write cycle counter, upper word

[1] See Table 117 for the default value in this register, which is model specific.

[2] 0x40BF is the default value for the ADIS16575, 0x40C0 is the default value for the ADIS16576, and 0x40C1 is the default value for the ADIS16577.

USER REGISTER DEFINITIONS

STATUS AND ERROR FLAG INDICATORS (DIAG_STAT)

Table 14. DIAG_STAT Register Definition

Addresses	Default	Access	Flash Backup
0x02, 0x03	0x0000	R	No

The DIAG_STAT register is unique in that it triggers the following special processing when read:

1. Any read of the DIAG_STAT register clears the DIAG_STAT register.
2. Any read of the DIAG_STAT register when in FIFO mode (FIFO_CTRL, Bit 0 = 1) triggers a FIFO pop, loading a single sample from the FIFO to the output registers, which includes reading the DIAG_STAT register through the burst read function.

In addition, the DIAG_STAT register updates asynchronously because fault conditions are detected. Other volatile registers update during the DR invalid period only.

Table 15. DIAG_STAT Bit Descriptions

Bit	Description
15	Microcontroller Fault. A 1 indicates that a fault occurred in the microcontroller. In response to this fault, the system issues a software reset. Upon the subsequent power-up, the system sets this bit.
14	Not Used.
13	Z-Axis Accelerometer Failure. 1 = error condition. This flag can be set by the on-demand self test command or by the continuous consistency checker.
12	Y-Axis Accelerometer Failure. 1 = error condition. This flag can be set by the on-demand self test command or by the continuous consistency checker.
11	X-Axis Accelerometer Failure. 1 = error condition. This flag can be set by the on-demand self test command or by the continuous consistency checker.
10	Z-Axis Gyroscope Failure. 1 = error condition. This flag can be set by the on-demand self test command or by the continuous gyroscope status monitor
9	Y-Axis Gyroscope Failure. 1 = error condition. This flag can be set by the on-demand self test command or by the continuous gyroscope status monitor.
8	X-Axis Gyroscope Failure. 1 = error condition. This flag can be set by the on-demand self test command or by the continuous gyroscope status monitor.
7	Scaled Sync Unlock Flag. A 1 indicates that the scaled sync, digital phased-lock loop (DPLL) controller is unlocked. This diagnostic is only active when the IMU is configured to operate in scaled sync mode.
6	Memory Error (Corrupted Factory Data Failure). A 1 indicates a memory error due to corrupted factory register data in either the flash memory or SRAM or a corrupted factory program detected during the flash memory test (initiated by Register GLOB_CMD, Bit 4, see Table 128). This failure is identified through a CRC comparison between the current data in memory and the data from the time of initial programming during production. If this error occurs, it is recommended to repeat the test. If the error persists, the ADIS16575/ADIS16576/ADIS16577 may need to be replaced.
5	Self-Test Diagnostics Failure. A 1 indicates that the sensor, self test routine failed. The specific failed sensor can be determined by reading the six self test result bits. Continuous monitoring of the sensors, which does not involve an applied stimulus, does not set this flag.
4	Power Supply Monitor. A 1 indicates that the voltage across VDD and GND is <2.9 V, which causes data processing to stop. When VDD ≥ 2.9 V for 250 ms, the ADIS16575/ADIS16576/ADIS16577 reinitialize and start producing data again.
3	SPI Communication Error. A 1 indicates that the total number of SCLK cycles is not 16. This error can detect issues such as being off by a single bit. When this error occurs, repeat the previous communication sequence. Persistence in this error may indicate a weakness in the SPI service that the ADIS16575/ADIS16576/ADIS16577 is receiving from the system it is supporting.
2	Flash Memory Update Failure. A 1 indicates that the most recent flash memory update (Register GLOB_CMD, Bit 3, see Table 128) failed. If this error occurs, ensure that VDD ≥ 3 V and repeat the update attempt. If this error persists, replace the ADIS16575/ADIS16576/ADIS16577.
1	Datapath Processing Overrun. A 1 indicates that one of the datapaths experienced an overrun condition, which can occur due to excessive SPI traffic, or if the sample clock rate is too high. If this error occurs, reduce the SPI traffic, or adjust the sample clock rate, to prevent future overruns. Note that a reset is not necessary for recovery. For more details on conditions that may cause this bit to be set to 1, see the SPI Operation section.
0	Sensor Initialization Failure. A 1 indicates that the inertial sensors failed to initialize properly. When this failure occurs, the sensors shut down, and the IMU is placed into safe mode. Upon the subsequent power-up, if this error persists, replace the ADIS16575/ADIS16576/ADIS16577.

The DIAG_STAT register (see Table 14 and Table 15) provides error flags for monitoring the integrity and operation of the ADIS16575/ADIS16576/ADIS16577. Reading this register causes all of the bits to return to 0. The error flags in STATUS are sticky, meaning that when the flags rise to 1, these flags remain there until a read request clears them. If an error condition persists, the flag (bit) automatically returns to a value of 1.

USER REGISTER DEFINITIONS

GYROSCOPE DATA

The gyroscopes in the ADIS16575/ADIS16576/ADIS16577 measure the angular rotation rate around three orthogonal axes (x, y, and z). Figure 60 show the orientation of each gyroscope axis and the direction of rotation that produces a positive response in each measurement.

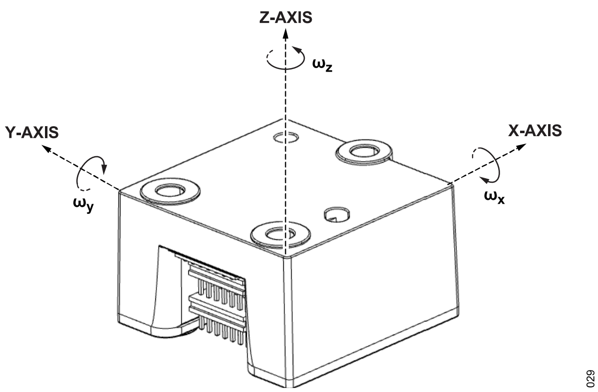

Figure 60. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 61 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y-axis and z-axis.

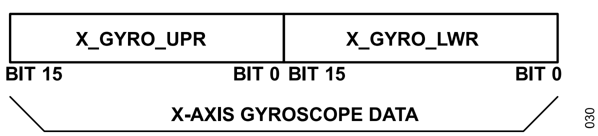

Figure 61. Gyroscope Output Data Structure

Gyroscope Data Formatting

Table 16 through Table 19 offer various numerical examples that demonstrate the format of the rotation rate data in both 16-bit and 32-bit formats using the generic measurement range (ω_{MAX}) and scale factor (K_G) definitions from Table 20.

Table 16. 16-Bit Gyroscope Data Format Examples (ADIS16575-2, ADIS16576-2, and ADIS16577-2)

Rotation Rate (°/sec)	Decimal	Hexadecimal	Binary
$+\omega_{MAX}$	+18,000	0x4650	0100 0110 0101 0000
$+2/K_G$	+2	0x0002	0000 0000 0000 0010
$+1/K_G$	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
$-1/K_G$	−1	0xFFFF	1111 1111 1111 1111
$-2/K_G$	−2	0xFFFE	1111 1111 1111 1110
$-\omega_{MAX}$	−18,000	0xB9B0	1011 1001 1011 0000

Table 17. 16-Bit Gyroscope Data Format Examples (ADIS16576-3 and ADIS16577-3)

Rotation Rate(°/sec)	Decimal	Hexadecimal	Binary
$+\omega_{MAX}$	+20,000	0x4E20	0100 1110 0010 0000
$+2/K_G$	+2	0x0002	0000 0000 0000 0010
$+1/K_G$	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
$-1/K_G$	−1	0xFFFF	1111 1111 1111 1111
$-2/K_G$	−2	0xFFFE	1111 1111 1111 1110
$-\omega_{MAX}$	−20,000	0xB1E0	1011 0001 1110 0000

Table 18. 32-Bit Gyroscope Data Format Examples (ADIS16575-2, ADIS16576-2, and ADIS16577-2)

Rotation Rate (°/sec)	Decimal	Hexadecimal
$+\omega_{MAX}$	+1,179,648,000	0x46500000
$+2/(K_G \times 2^{16})$	+2	0x00000002
$+1/(K_G \times 2^{16})$	+1	0x00000001
0	0	0x0000000
$-1/(K_G \times 2^{16})$	−1	0xFFFFFFFF
$-2/(K_G \times 2^{16})$	−2	0xFFFFFFFE
$-\omega_{MAX}$	−1,179,648,000	0xB9B00000

Table 19. 32-Bit Gyroscope Data Format Examples (ADIS16576-3 and ADIS16577-3)

Rotation Rate (°/sec)	Decimal	Hexadecimal
$+\omega_{MAX}$	+1,310,720,000	0x4E200000
$+2/(K_G \times 2^{16})$	+2	0x00000002
$+1/(K_G \times 2^{16})$	+1	0x00000001
0	0	0x0000000
$-1/(K_G \times 2^{16})$	−1	0xFFFFFFFF
$-2/(K_G \times 2^{16})$	−2	0xFFFFFFFE
$-\omega_{MAX}$	−1,310,720,000	0xB1E00000

USER REGISTER DEFINITIONS

Gyroscope Measurement Range and Scale Factor

Table 20 provide the measurement range ($\pm\omega_{MAX}$) and scale factor (K_G) for the gyroscope in each ADIS16575/ADIS16576/ADIS16577 model.

Table 20. Gyroscope Measurement Range and Scale Factors (16-Bit)

Model	Range, $\pm\omega_{MAX}$ (°/sec)	Scale Factor, K_G (LSB/°/sec)
ADIS16575-2, ADIS16576-2, ADIS16577-2	±450	40
ADIS16576-3, ADIS16577-3	±2000	10

X-Axis Gyroscope (X_GYRO_LWR and X_GYRO_UPR)

Table 21. X_GYRO_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x04, 0x05	Not applicable	R	No

Table 22. X_GYRO_LWR Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data; low word; additional resolution bits

Table 23. X_GYRO_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x06, 0x07	Not applicable	R	No

Table 24. X_GYRO_UPR Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = $1/K_G$ (see Table 20 for K_G)

The X_GYRO_LWR (see Table 21 and Table 22) and X_GYRO_UPR (see Table 23 and Table 24) registers contain the gyroscope data for the x-axis.

Y-Axis Gyroscope (Y_GYRO_LWR and Y_GYRO_UPR)

Table 25. Y_GYRO_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x08, 0x09	Not applicable	R	No

Table 26. Y_GYRO_LWR Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data; low word; additional resolution bits

Table 27. Y_GYRO_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x0A, 0x0B	Not applicable	R	No

Table 28. Y_GYRO_UPR Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = $1/K_G$ (see Table 20 for K_G)

The Y_GYRO_LWR (see Table 25 and Table 26) and Y_GYRO_UPR (see Table 27 and Table 28) registers contain the gyroscope data for the y-axis.

Z-Axis Gyroscope (Z_GYRO_LWR and Z_GYRO_UPR)

Table 29. Z_GYRO_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x0C, 0x0D	Not applicable	R	No

Table 30. Z_GYRO_LWR Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data; low word; additional resolution bits

Table 31. Z_GYRO_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x0E, 0x0F	Not applicable	R	No

Table 32. Z_GYRO_UPR Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = $1/K_G$ (see Table 20 for K_G)

The Z_GYRO_LWR (see Table 29 and Table 30) and Z_GYRO_UPR (see Table 31 and Table 32) registers contain the gyroscope data for the z-axis.

ACCELERATION DATA

The accelerometers in the ADIS16575/ADIS16576/ADIS16577 measure both dynamic and static acceleration (such as response to gravity) along the same three orthogonal axes that define the axes of rotation for the gyroscopes (x, y, and z). Figure 62 show the orientation of each accelerometer axis and the direction of acceleration that produces a positive response in each measurement.

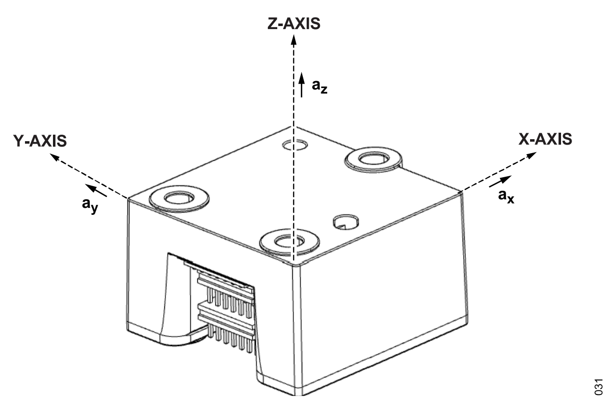

Figure 62. Accelerometer Axis and Polarity Assignments

USER REGISTER DEFINITIONS

Each accelerometer has two output data registers. Figure 63 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y- and z-axes.

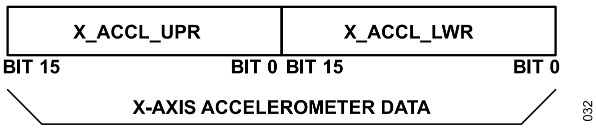

Figure 63. Accelerometer Output Data Structure

Accelerometer Data Formatting

Table 33 and Table 34 show various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats using the generic measurement range (A_{MAX}) and scale factor (K_A) definitions from Table 35.

Table 33. 16-Bit Accelerometer Data Format Examples

Acceleration (*g*)	Decimal	Hexadecimal	Binary
$+A_{MAX}$	+32,000	0x7D00	0111 1101 0000 0000
$+2/K_A$	+2	0x0002	0000 0000 0000 0010
$+1/K_A$	+1	0x0001	0000 0000 0000 0001
0 *g*	0	0x0000	0000 0000 0000 0000
$-2/K_A$	−1	0xFFFF	1111 1111 1111 1111
$-1/K_A$	−2	0xFFFE	1111 1111 1111 1110
$-A_{MAX}$	−32,000	0x8300	1000 0011 0000 0000

Table 34. 32-Bit Accelerometer Data Format Examples

Acceleration (*g*)	Decimal	Hexadecimal
$+A_{MAX}$	+2,097,152,000	0x7D000000
$+2/(K_A \times 2^{16})$	+2	0x00000002
$+1/(K_A \times 2^{16})$	+1	0x00000001
0	0	0x00000000
$-1/(K_A \times 2^{16})$	−1	0xFFFFFFFF
$-2/(K_A \times 2^{16})$	−2	0xFFFFFFFE
$-A_{MAX}$	−2,097,152,000	0x83000000

Accelerometer Measurement Range and Scale Factor

Table 35 provide the measurement range ($\pm A_{MAX}$) and scale factor (K_A) for the accelerometer in each ADIS16575/ADIS16576/ADIS16577 model.

Table 35. Accelerometer Measurement Range and Scale Factors

Model	Range, $\pm A_{MAX}$ (g)	Scale Factor, K_A (LSB/g)
ADIS16575	±8	4000
ADIS16576	±40	800
ADIS16577	±40	800

X-Axis Accelerometer (X_ACCL_LWR and X_ACCL_UPR)

Table 36. X_ACCL_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x10, 0x11	Not applicable	R	No

Table 37. X_ACCL_LWR Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer data; low word; additional resolution bits

Table 38. X_ACCL_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x12, 0x13	Not applicable	R	No

Table 39. X_ACCL_UPR Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer data, high word; twos complement, 0 *g* = 0x0000, 1 LSB = $1/K_A$ (see Table 35 for K_A)

The X_ACCL_LWR (see Table 36 and Table 37) and X_ACCL_UPR (see Table 38 and Table 39) registers contain the accelerometer data for the x-axis.

Y-Axis Accelerometer (Y_ACCL_LWR and Y_ACCL_UPR)

Table 40. Y_ACCL_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x14, 0x15	Not applicable	R	No

Table 41. Y_ACCL_LWR Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data; low word; additional resolution bits

Table 42. Y_ACCL_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x16, 0x17	Not applicable	R	No

Table 43. Y_ACCL_UPR Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data, high word; twos complement, 0 *g* = 0x0000, 1 LSB = $1/K_A$ (see Table 35 for K_A)

The Y_ACCL_LWR (see Table 40 and Table 41) and Y_ACCL_UPR (see Table 42 and Table 43) registers contain the accelerometer data for the y-axis.

Z-Axis Accelerometer (Z_ACCL_LWR and Z_ACCL_UPR)

Table 44. Z_ACCL_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x18, 0x19	Not applicable	R	No

USER REGISTER DEFINITIONS

Table 45. Z_ACCL_LWR Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data; low word; additional resolution bits

Table 46. Z_ACCL_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x1A, 0x1B	Not applicable	R	No

Table 47. Z_ACCL_UPR Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data, high word; twos complement, 0 *g* = 0x0000, 1 LSB = $1/K_A$ (see Table 35 for K_A)

The Z_ACCL_LWR (see Table 44 and Table 45) and Z_ACCL_UPR (see Table 46 and Table 47) registers contain the accelerometer data for the z-axis.

INTERNAL TEMPERATURE (TEMP)

Table 48. TEMP Register Definition

Addresses	Default	Access	Flash Backup
0x1C, 0x1D	Not applicable	R	No

Table 49. TEMP Bit Definitions

Bits	Description
[15:0]	Temperature data; twos complement, 1 LSB = 0.1°C, 0°C = 0x0000

The TEMP register (see Table 48 and Table 49) provides a coarse measurement of the temperature inside of the ADIS16575/ADIS16576/ADIS16577. This data is most helpful in monitoring relative changes in the thermal environment.

Table 50. TEMP Data Format Examples

Temperature (°C)	Decimal	Hexadecimal	Binary
+105	+1050	0x041A	0000 0100 0001 1010
+25	+250	0x00FA	0000 0000 1111 1010
+0.2	+2	0x0002	0000 0000 0000 0010
+0.1	+1	0x0001	0000 0000 0000 0001
+0	0	0x0000	0000 0000 0000 0000
+0.1	−1	0xFFFF	1111 1111 1111 1111
+0.2	−2	0xFFFE	1111 1111 1111 1110
−40	−400	0xFE70	1111 1110 0111 0000

TIMESTAMP (TIME_STAMP_LWR AND TIME_STAMP_UPR)

Table 51. TIME_STAMP_LWR and TIME_STAMP_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x1E, 0x1F	Not applicable	R	No
0x20, 0x21	Not applicable	R	No

The sample timestamp 32-bit output register represents the timestamp of the current inertial sample relative to the external sync edge.

The timestamp represents the delay between the internal interpolation pulse for the sample and the user-provided external sync edge. The timestamp functionality is active in all four sync modes:

- Internal sync and output sync: the timestamp is a free-running timer.
- Direct external sync: the timestamp measures the delay between the external sync clock and the corresponding internal interpolation pulse.
- Scaled external sync: the timestamp measures the latency from the previous external sync edge to the internal interpolation pulse of the current sample.

The resolution of this register depends on the TS_32 bit in the MSC_CTRL register (see Bit 10 in Table 120). By default, TS_32 is cleared, giving the timestamp a resolution of 49.02 μs/LSB and limiting the TIME_STAMP bit width to 16 bits. If TS_32 is set, all 32 bits of the TIME_STAMP register are utilized, with a resolution of 0.01923 μs/LSB. If the decimation filter is enabled, the timestamp contains the time associated with the last sample in each data update.

As an example, if UP_SCALE = 20, DEC_RATE = 0, TS_32 = 0, and the external SYNC rate is 100 Hz, the result is the following timestamp sequence: 0 LSB, 10 LSB, 21 LSB, 31 LSB, 41 LSB, 51 LSB, 61 LSB, 72 LSB, …, 194 LSB for the 20th sample, which translates to 0 μs, 490 μs, …, 9510 μs and is the time from the previous sync edge.

Another example, if TS_32 = 1, UP_SCALE = 20, DEC_RATE = 0, and an external SYNC rate of 100 Hz the result is the following timestamp sequence: 0 LSB, 26000 LSB, 52000 LSB, 78000 LSB, 104000 LSB, 130000 LSB, 156000 LSB, 182000 LSB, …, 494000 LSB for the 20th sample, which translates to 0 μs, 500 μs, 1000 μs, 1500 μs, 2000 μs, 2500 μs, 3000 μs, 3500 μs, …, 9500 μs and is the time from the previous sync edge.

DATA UPDATE COUNTER (DATA_CNTR)

Table 52. DATA_CNTR Register Definition

Addresses	Default	Access	Flash Backup
0x22, 0x23	Not applicable	R	No

Table 53. DATA_CNTR Bit Definitions

Bits	Description
[15:0]	Data update counter, offset binary format

When the ADIS16575/ADIS16576/ADIS16577 go through the power-on sequence or when these devices recover from a reset command, DATA_CNTR (see Table 52 and Table 53) starts with a value of 0x0000 and increments every time new data loads into the output registers. When the DATA_CNTR value hits 0xFFFF, the next data update makes it wrap back around to 0x0000, where the data continues to increase each time new data loads into the output registers.

USER REGISTER DEFINITIONS

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16575/ADIS16576/ADIS16577 also provide delta angle measurements that calculate angular displacement between each sample update.

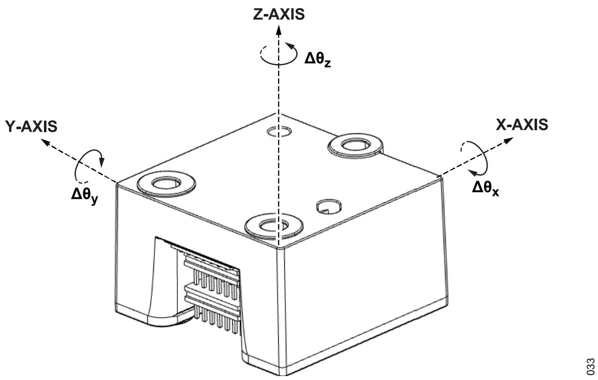

Figure 64. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,\,nD} = \frac{1}{2\times f_S}\times\sum_{d=0}^{D-1}\left(\omega_{x,\,nD+d}+\omega_{x,\,nD+d-1}\right)$$

where:
x is the x-axis.
n is the sample time before the decimation filter.
D is the decimation rate (DEC_RATE + 1, see Table 124).
f_S is the sample rate.
d is the incremental variable in the summation formula.
ω_X is the x-axis rate of rotation (gyroscope).

When using the internal sample clock, f_S equals a nominal rate of selected 2000 SPS or 4000 SPS. For better precision in this measurement, measure the internal f_S using the data ready signal on the DR pin (DEC_RATE = 0x0000, see Table 123), divide each delta angle result (from the delta angle output registers) by the data ready frequency, and multiply it by 2000. Each axis of the delta angle measurements has two output data registers. Figure 65 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y-axis and z-axis.

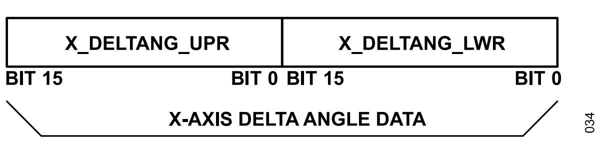

Figure 65. Delta Angle Output Data Structure

Delta Angle Measurement Range

Table 54 shows the measurement range for each ADIS16575/ADIS16576/ADIS16577 model.

Table 54. Delta Angle Measurement Range

Model	Measurement Range, $\pm\Delta\theta_{MAX}$ (°)
ADIS16575-2, ADIS16576-2, ADIS16577-2	±720
ADIS16576-3, ADIS16577-3	±2160

X-Axis Delta Angle (X_DELTANG_LWR and X_DELTANG_UPR)

Table 55. X_DELTANG_LWR Register Definitions

Addresses	Default	Access	Flash Backup
0x24, 0x25	Not applicable	R	No

Table 56. X_DELTANG_LWR Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; low word

Table 57. X_DELTANG_UPR Register Definitions

Addresses	Default	Access	Flash Backup
0x26, 0x27	Not applicable	R	No

Table 58. X_DELTANG_UPR Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; high word; twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 54 for $\Delta\theta_{MAX}$)

The X_DELTANG_LWR (see Table 55 and Table 56) and X_DELTANG_UPR (see Table 57 and Table 58) registers contain the delta angle data for the x-axis.

Y-Axis Delta Angle (Y_DELTANG_LWR and Y_DELTANG_UPR)

Table 59. Y_DELTANG_LWR Register Definitions

Addresses	Default	Access	Flash Backup
0x28, 0x29	Not applicable	R	No

Table 60. Y_DELTANG_LWR Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; low word

Table 61. Y_DELTANG_UPR Register Definitions

Addresses	Default	Access	Flash Backup
0x2A, 0x2B	Not applicable	R	No

Table 62. Y_DELTANG_UPR Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; high word; twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 54 for $\Delta\theta_{MAX}$)

The Y_DELTANG_LWR (see Table 59 and Table 60) and Y_DELTANG_UPR (see Table 61 and Table 62) registers contain the delta angle data for the y-axis.

USER REGISTER DEFINITIONS

Z-Axis Delta Angle (Z_DELTANG_LWR and Z_DELTANG_UPR)

Table 63. Z_DELTANG_LWR Register Definitions

Addresses	Default	Access	Flash Backup
0x2C, 0x2D	Not applicable	R	No

Table 64. Z_DELTANG_LWR Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; low word

Table 65. Z_DELTANG_UPR Register Definitions

Addresses	Default	Access	Flash Backup
0x2E, 0x2F	Not applicable	R	No

Table 66. Z_DELTANG_UPR Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; high word; twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 54 for $\Delta\theta_{MAX}$)

The Z_DELTANG_LWR (see Table 63 and Table 64) and Z_DELTANG_UPR (see Table 65 and Table 66) registers contain the delta angle data for the z-axis.

Delta Angle Data Formatting

Table 67 and Table 68 show various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 67. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex.	Binary
$\Delta\theta_{MAX} \times (2^{15}-1)/2^{15}$	+32,767	0x7FFF	0111 1111 1110 1111
$+\Delta\theta_{MAX}/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+\Delta\theta_{MAX}/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-\Delta\theta_{MAX}/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-\Delta\theta_{MAX}/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
$-\Delta\theta_{MAX}$	−32,768	0x8000	1000 0000 0000 0000

Table 68. 32-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex.
$+\Delta\theta_{MAX} \times (2^{31}-1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+\Delta\theta_{MAX}/2^{30}$	+2	0x00000002
$+\Delta\theta_{MAX}/2^{31}$	+1	0x00000001
0	0	0x00000000
$-\Delta\theta_{MAX}/2^{31}$	−1	0xFFFFFFFF
$-\Delta\theta_{MAX}/2^{30}$	−2	0xFFFFFFFE
$-\Delta\theta_{MAX}$	−2,147,483,648	0x80000000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16575/ADIS16576/ADIS16577 also provide delta velocity measurements that calculate the linear velocity change between each sample update.

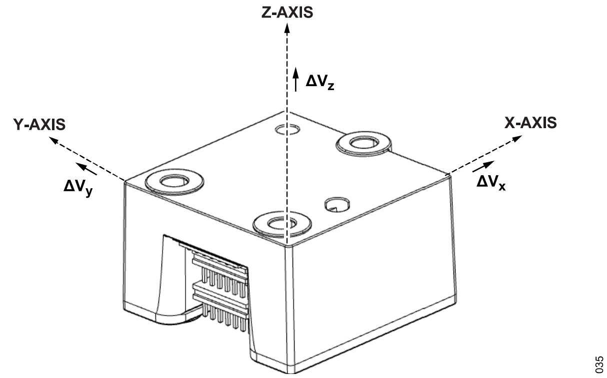

Figure 66. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and uses the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,\ nD} = \frac{1}{2 \times f_S} \times \sum_{d=0}^{D-1} \left(a_{x,\ nD+d} + a_{x,\ nD+d-1}\right)$$

where:
x is the x-axis.
n is the sample time before the decimation filter.
D is the decimation rate (DEC_RATE + 1, see Table 124).
f_S is the sample rate.
d is the incremental variable in the summation formula.
a_X is the x-axis acceleration.

When using the internal sample clock, f_S equals a nominal rate of selected 2000 SPS or 4000 SPS. For better precision in this measurement, measure the internal f_S using the data ready signal on the DR pin (DEC_RATE = 0x0000, see Table 123), divide each delta angle result (from the delta angle output registers) by the data ready frequency, and multiply it by the unit sample rate. Each axis of the delta velocity measurements has two output data registers. Figure 67 shows how these two registers combine to support a 32-bit, twos complement data format for the delta velocity measurements along the x-axis. This format also applies to the y-axis and z-axes.

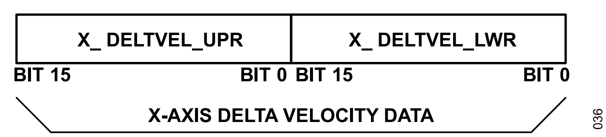

Figure 67. Delta Velocity Output Data Structure

Delta Velocity Measurement Range

Table 69 shows the measurement range for each ADIS16575/ADIS16576/ADIS16577 model.

Table 69. Delta Velocity Measurement Range

Model	Measurement Range, $\pm\Delta V_{MAX}$ (m/sec)
ADIS16575	±100
ADIS16576	±125

USER REGISTER DEFINITIONS

Table 69. Delta Velocity Measurement Range (Continued)

Model	Measurement Range, $\pm\Delta V_{MAX}$ (m/sec)
ADIS16577	±400

X-Axis Delta Velocity (X_DELTVEL_LWR and X_DELTVEL_UPR)

Table 70. X_DELTVEL_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x30, 0x31	Not applicable	R	No

Table 71. X_DELTVEL_LWR Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data; low word; additional resolution bits

Table 72. X_DELTVEL_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x32, 0x33	Not applicable	R	No

Table 73. X_DELTVEL_UPR Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data; high word; twos complement, 0 m/sec = 0x0000; 1 LSB = $\Delta V_{MAX} \div 2^{15}$ (see Table 69 for ΔV_{MAX})

The X_DELTVEL_LWR (see Table 70 and Table 71) and X_DELTVEL_UPR (see Table 72 and Table 73) registers contain the delta velocity data for the x-axis.

Y-Axis Delta Velocity (Y_DELTVEL_LWR and Y_DELTVEL_UPR)

Table 74. Y_DELTVEL_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x34, 0x35	Not applicable	R	No

Table 75. Y_DELTVEL_LWR Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data; low word; additional resolution bits

Table 76. Y_DELTVEL_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x36, 0x37	Not applicable	R	No

Table 77. Y_DELTVEL_UPR Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data; high word; twos complement, 0 m/sec = 0x0000; 1 LSB = $\Delta V_{MAX} \div 2^{15}$ (see Table 69 for ΔV_{MAX})

The Y_DELTVEL_LWR (see Table 74 and Table 75) and Y_DELTVEL_UPR (see Table 76 and Table 77) registers contain the delta velocity data for the y-axis.

Z-Axis Delta Velocity (Z_DELTVEL_LWR and Z_DELTVEL_UPR)

Table 78. Z_DELTVEL_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x38, 0x39	Not applicable	R	No

Table 79. Z_DELTVEL_LWR Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data; low word; additional resolution bits

Table 80. Z_DELTVEL_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x3A, 0x3B	Not applicable	R	No

Table 81. Z_DELTVEL_UPR Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data; high word; twos complement, 0 m/sec = 0x0000; 1 LSB = $\Delta V_{MAX} \div 2^{15}$ (see Table 69 for ΔV_{MAX})

The Z_DELTVEL_LWR (see Table 78 and Table 79) and Z_DELTVEL_UPR (see Table 80 and Table 81) registers contain the delta velocity data for the z-axis.

Delta Velocity Data Formatting

Table 82 and Table 83 offer various numerical examples that demonstrate the format of the delta velocity data in both 16-bit and 32-bit formats.

Table 82. 16-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hexadecimal	Binary
$+\Delta V_{MAX} \times (2^{15} - 1)/2^{15}$	+32,767	0x7FFF	0111 1111 1111 1111
$+\Delta V_{MAX}/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+\Delta V_{MAX}/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-\Delta V_{MAX}/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-\Delta V_{MAX}/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
$-\Delta V_{MAX}$	−32,768	0x8000	1000 0000 0000 0000

Table 83. 32-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hexadecimal
$+\Delta V_{MAX} \times (2^{31} - 1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+\Delta V_{MAX}/2^{30}$	+2	0x00000002
$+\Delta V_{MAX}/2^{31}$	+1	0x00000001
0	0	0x00000000
$-\Delta V_{MAX}/2^{31}$	−1	0xFFFFFFFF
$-\Delta V_{MAX}/2^{30}$	−2	0xFFFFFFFE
$-\Delta V_{MAX}$	+2,147,483,648	0x80000000

USER REGISTER DEFINITIONS

FIFO COUNT (FIFO_CNT)

Table 84. FIFO_CNT Register Definition

Addresses	Default	Access	Flash Backup
0x3C, 0x3D	N/A	R	NO

Table 85. FIFO_CNT Bit Definitions

Bits	Description
[15:0]	FIFO Sample Count. This 16-bit value represents the number of inertial data samples queued in the output FIFO. This register is valid only when the IMU is operating in FIFO mode, as indicated by the FIFO_CTR register, Bit 0, being set to 1.

Note that issuing a FIFO_FLUSH command clears the current output FIFO contents and resets this register to zero.

SPI CHECKSUM (SPI_CHKSUM)

Table 86. SPI_CHKSUM Register Definition

Addresses	Default	Access	Flash Backup
0x3E, 0x3F	N/A	R	No

Table 87. SPI_CHKSUM Bit Definitions

Bits	Description
[15:0]	SPI Transaction Checksum. This 16-bit value represents the current checksum calculated for all register data transmitted during the current sample period.

The SPI dynamic checksum register at Address 0x3E and Address 0x3F is continuously updated with the checksum for all register data transmitted during the current sample period. The checksum uses the same byte-wise sum algorithm as the burst read function, enabling simple integration with host systems. SPI_CHKSUM resets to 0x0000 when a fresh sample data is loaded to the output registers (either from the datapath in direct output mode or from the output FIFO in FIFO mode) and then updates continuously as the user reads the fresh sample data.

The SPI_CHKSUM register allows the user to read any arbitrary sequence of registers per sample and to validate the integrity of the read. This scheme provides increased flexibility compared to the burst read function, which offers a checksum but only allows for reading a specific register sequence. The user can assess SPI read integrity by calculating the byte-wise sum of all received read data for a given sample and then comparing the calculated checksum with the received SPI_CHKSUM register value for that same sample. A checksum mismatch indicates one of two conditions:

1. Compromised SPI communications between the IMU and host (for example, bit slip, incorrect address)
2. A register read sequence split across multiple samples, causing SPI_CHKSUM to reset midread

Detecting these errors ensures the inertial sample data received by the host system is both time coherent and valid (transmitted data matches received data).

To illustrate how this checksum calculation works in practice, here is a specific example using the byte-wise sum algorithm. This example demonstrates the process a host system uses to validate the integrity of received data. This algorithm adds all bytes in the data sequence as follows:

1. Initialize a 16-bit sum to 0.
2. For each 16-bit register value in the sequence,
   a. Add the high byte (Bits[15:8]) to the sum.
   b. Add the low byte (Bits[7:0]) to the sum.
3. The final 16-bit sum is the checksum.

For this example, consider the following data for the first few registers in 32-bit burst mode:

- X_GYRO_LWR = 0x1234
- X_GYRO_UPR = 0x5678
- Y_GYRO_LWR = 0x9ABC

To calculate the checksum, take the following steps:

1. Initialize sum = 0.
2. Add bytes from X_GYRO_LWR: Sum = 0x12 + 0x34 = 0x46.
3. Add bytes from X_GYRO_UPR: Sum = 0x46 + 0x56 + 0x78 = 0x114.
4. Add bytes from Y_GYRO_LWR: Sum = 0x114 + 0x9A + 0xBC = 0x26A.

Note that the final checksum is 0x026A. This checksum can then be compared with the checksum received in the burst read or the value read from the SPI_CHKSUM register to verify the integrity of the data transfer.

Table 88 illustrates the complete burst read SPI communication sequence, showing the order of register reads for both 16-bit and 32-bit modes, and highlighting the position of the SPI_CHKSUM at the end of the sequence.

Table 88. Burst Read SPI Communication Sequence with Checksum

16-Bit SPI Word	16-Bit Burst Register	32-Bit Burst Registers	Comments
0	FIFO_CNT	FIFO_CNT	Not included in checksum.
1	DIAG_STAT	DIAG_STAT	Not included in checksum.
2	X_GYRO_UPR or X_DELTANG_UPR	X_GYRO_LWR or X_DELTANG_LWR	OUT_SEL determines which channel is transmitted.
3	Y_GYRO_UPR or Y_DELTANG_UPR	X_GYRO_UPR or X_DELTANG_UPR	Not applicable.
4	Z_GYRO_UPR or Z_DELTANG_UPR	Y_GYRO_LWR or Y_DELTANG_LWR	Not applicable.
5	X_ACCL_UPR or X_DELTVEL_UPR	Y_GYRO_UPR or Y_DELTANG_UPR	Not applicable.

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Table 88. Burst Read SPI Communication Sequence with Checksum (Continued)

16-Bit SPI Word	16-Bit Burst Register	32-Bit Burst Registers	Comments
6	Y_ACCL_UPR or Y_DELTVEL_UPR	Z_GYRO_LWR or Z_DELTANG_LWR	Not applicable.
7	Z_ACCL_UPR or Z_DELTVEL_UPR	Z_GYRO_UPR or Z_DELTANG_UPR	Not applicable.
8	TEMP	X_ACCL_LWR or X_DELTVEL_LWR	Not applicable.
9	DATA_CNTR or TIMESTAMP_LWR	X_ACCL_UPR or X_DELTVEL_UPR	Not applicable.
10	SPI_CHKSUM	Y_ACCL_LWR or Y_DELTVEL_LWR	Not applicable.
11	Not applicable	Y_ACCL_UPR or Y_DELTVEL_UPR	Not applicable.
12	Not applicable	Z_ACCL_LWR or Z_DELTVEL_LWR	Not applicable.
13	Not applicable	Z_ACCL_UPR or Z_DELTVEL_UPR	Not applicable.
14	Not applicable	TEMP	Not applicable.
15	Not applicable	DATA_CNTR or TIMESTAMP_LWR	DATA_CNTR or TIMESTAMP_LWR. When scaled sync mode is disabled, DATA_CNTR is transmitted. When scaled sync mode is enabled, TIMESTAMP_LWR replaces DATA_CNTR.
16	Not applicable	0s or TIMESTAMP_UPR	TIMESTAMP_UPR bit width selected by TS_32 in the MSC_CTRL register
17	Not applicable	SPI_CHKSUM	Not applicable

As indicated in Table 88, the the SPI_CHKSUM value follows the 0s and the TIME_STAMP_UPR value in the burst read sequence. Once all sensor data and timestamp information is read, an additional 16-bit transaction is required to read the checksum. It is important to note that the checksum calculation does not include FIFO_CNT and DIAG_STAT registers, as mentioned in the not included in checksum comments in Table 88.

This implementation of SPI_CHKSUM provides a robust method for ensuring data integrity in SPI communications with the IMU, allowing for flexible read sequences while maintaining the ability to detect transmission errors.

CALIBRATION, BIAS ADJUSTMENT, AND CONTINUOUS BIAS ESTIMATION (CBE)

The ADIS16575/ADIS16576/ADIS16577 employ a comprehensive approach to calibration and bias management for its inertial sensors (accelerometers and gyroscopes). Each sensor's signal chain includes unique correction formulas derived from extensive characterization of bias, sensitivity, alignment, and point of percussion (for accelerometers) over the −40°C to +85°C temperature range.

While the factory-derived correction formulas are not user accessible, the devices provide the following registers for individual sensor bias adjustment:

1. Gyroscope bias registers: XG_BIAS_LWR, XG_BIAS_UPR, YG_BIAS_LWR, YG_BIAS_UPR, ZG_BIAS_LWR, and ZG_BIAS_UPR
2. Accelerometer bias registers: XA_BIAS_LWR, XA_BIAS_UPR, YA_BIAS_LWR, YA_BIAS_UPR, ZA_BIAS_LWR, and ZA_BIAS_UPR

Each axis uses two 16-bit registers (xx_BIAS_LWR and (xx_BIAS_UPR) to form a 32-bit bias adjustment value, matching the format and scaling of the sensor output registers. These user-adjustable corrections are applied after the factory-derived formulas in the signal chain, which processes at a user-defined rate of 2000 Hz or 4000 Hz with the internal sample clock.

To enhance long-term stability, the ADIS16575/ADIS16576/ADIS16577 feature CBE. The NULL_CNFG register controls CBE, with Bits[13:8] enabling and disabling CBE for each axis and Bits[3:0] setting the estimation time base. The bias correction update command (GLOB_CMD, Bit 0) applies the latest CBE estimates to the bias adjustment registers.

Users can adjust bias through the following two methods:

1. Manual adjustment. Direct writing to bias registers for immediate correction.
2. Automatic adjustment. Configuring NULL_CNFG for CBE and periodically applying updates.

This integrated approach to calibration and bias management, combining factory calibration, user-accessible adjustments, and continuous estimation, provides powerful tools to optimize the ADIS16575/ADIS16576/ADIS16577 performance across varying conditions and applications.

Calibration, Gyroscope Bias (XG_BIAS_LWR and XG_BIAS_UPR)

Table 89. XG_BIAS_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x40, 0x41	0x0000	R/W	Yes

Table 90. XG_BIAS_LWR Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction; lower word

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Table 91. XG_BIAS_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x42, 0x43	0x0000	R/W	Yes

Table 92. XG_BIAS_UPR Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction factor, upper word

The XG_BIAS_LWR (see Table 89 and Table 90) and XG_BIAS_UPR (see Table 91 and Table 92) registers combine to allow users to adjust the bias of the x-axis gyroscopes. The data format examples in Table 16 also apply to the XG_BIAS_UPR register, and the data format examples in Table 19 apply to the 32-bit combination of the XG_BIAS_LWR and XG_BIAS_UPR registers. See Figure 68 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

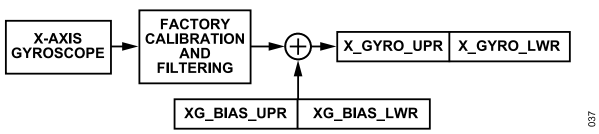

Figure 68. User Calibration Signal Path, Gyroscopes

Calibration, Gyroscope Bias (YG_BIAS_LWR and YG_BIAS_UPR)

Table 93. YG_BIAS_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x44, 0x45	0x0000	R/W	Yes

Table 94. YG_BIAS_LWR Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction; lower word

Table 95. YG_BIAS_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x46, 0x47	0x0000	R/W	Yes

Table 96. YG_BIAS_UPR Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction factor, upper word

The YG_BIAS_LWR (see Table 93 and Table 94) and YG_BIAS_UPR (see Table 95 and Table 96) registers combine to allow users to adjust the bias of the y-axis gyroscopes. The data format examples in Table 16 also apply to the YG_BIAS_UPR register, and the data format examples in Table 19 apply to the 32-bit combination of the YG_BIAS_LWR and YG_BIAS_UPR registers. These registers influence the y-axis gyroscope measurements in the same manner that the XG_BIAS_LWR and XG_BIAS_UPR registers influence the x-axis gyroscope measurements (see Figure 68).

Calibration, Gyroscope Bias (ZG_BIAS_LWR and ZG_BIAS_UPR)

Table 97. ZG_BIAS_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x48, 0x49	0x0000	R/W	Yes

Table 98. ZG_BIAS_LWR Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction; lower word

Table 99. ZG_BIAS_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x4A, 0x4B	0x0000	R/W	Yes

Table 100. ZG_BIAS_UPR Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction factor, upper word

The ZG_BIAS_LWR (see Table 97 and Table 98) and ZG_BIAS_UPR (see Table 99 and Table 100) registers combine to allow users to adjust the bias of the z-axis gyroscopes. The data format examples in Table 16 also apply to the ZG_BIAS_UPR register, and the data format examples in Table 19 apply to the 32-bit combination of the ZG_BIAS_LWR and ZG_BIAS_UPR registers. These registers influence the z-axis gyroscope measurements in the same manner that the XG_BIAS_LWR and XG_BIAS_UPR registers influence the x-axis gyroscope measurements (see Figure 68).

Calibration, Accelerometer Bias (XA_BIAS_LWR and XA_BIAS_UPR)

Table 101. XA_BIAS_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x4C, 0x4D	0x0000	R/W	Yes

Table 102. XA_BIAS_LWR Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction; lower word

Table 103. XA_BIAS_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x4E, 0x4F	0x0000	R/W	Yes

Table 104. XA_BIAS_UPR Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction, upper word

The XA_BIAS_LWR (see Table 101 and Table 102) and XA_BIAS_UPR (see Table 103 and Table 104) registers combine to allow users to adjust the bias of the x-axis accelerometers. The data format examples in Table 33 also apply to the XA_BIAS_ UPR register and the data format examples in Table 34 apply to the 32-bit combination of the XA_BIAS_LWR and XA_BIAS_UPR registers. See Figure 69 for an illustration of how these two registers combine and influence the x-axis accelerometer measurements.

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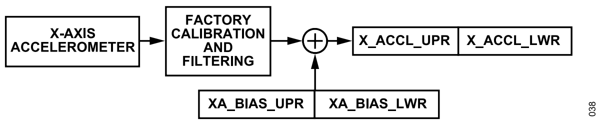

Figure 69. User Calibration Signal Path, Accelerometers

Note that these registers can be programmed directly for immediate bias adjustment or set by using the CBE and bias update command.

Calibration, Accelerometer Bias (YA_BIAS_LWR and YA_BIAS_UPR)

Table 105. YA_BIAS_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x50, 0x51	0x0000	R/W	Yes

Table 106. YA_BIAS_LWR Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction; lower word

Table 107. YA_BIAS_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x52, 0x53	0x0000	R/W	Yes

Table 108. YA_BIAS_UPR Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, upper word

The YA_BIAS_LWR (see Table 105 and Table 106) and YA_BIAS_UPR (see Table 107 and Table 108) registers combine to allow users to adjust the bias of the y-axis accelerometers. The data format examples in Table 33 also apply to the YA_BIAS_UPR register, and the data format examples in Table 34 apply to the 32-bit combination of the YA_BIAS_LWR and YA_BIAS_UPR registers. These registers influence the y-axis accelerometer measurements in the same manner that the XA_BIAS_LWR and XA_BIAS_UPR registers influence the x-axis accelerometer measurements (see Figure 69).

Calibration, Accelerometer Bias (ZA_BIAS_LWR and ZA_BIAS_UPR)

Table 109. ZA_BIAS_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x54, 0x55	0x0000	R/W	Yes

Table 110. ZA_BIAS_LWR Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction; lower word

Table 111. ZA_BIAS_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x56, 0x57	0x0000	R/W	Yes

Table 112. ZA_BIAS_UPR Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, upper word

The ZA_BIAS_LWR (see Table 109 and Table 110) and ZA_BIAS_UPR (see Table 111 and Table 112) registers combine to allow users to adjust the bias of the z-axis accelerometers. The data format examples in Table 33 also apply to the ZA_BIAS_UPR register and the data format examples in Table 34 apply to the 32-bit combination of the ZA_BIAS_LWR and ZA_BIAS_UPR registers. These registers influence the z-axis accelerometer measurements in the same manner that the XA_BIAS_LWR and XA_BIAS_UPR registers influence the x-axis accelerometer measurements (see Figure 69).

FIFO CONTROL (FIFO_CTRL) AND WATERMARK INTERRUPT

The output FIFO control register (Address 0x5A and Address 0x5B) configure the IMU output mode, FIFO overflow behavior, and watermark interrupt properties.

Table 113. FIFO_CTRL Register Definition

Address	Default	Access	Flash Backup
0x5A, 0x5B	N/A	R/W	Yes

Table 114. FIFO_CTRL Bit Definitions

Bits	Name	Description
[15:4]	WM_LVL	Watermark Threshold Level. Defines the number of samples that must be enqueued into the FIFO to trigger the watermark interrupt. A value of 0 means the watermark triggers once a single sample is enqueued.
3	WM_POL	Watermark Interrupt Polarity. 0 = active low. 1 = active high.
2	WM_EN	Watermark Interrupt Enable. 0 = disabled. 1 = enabled.
1	OVERFLOW	Output FIFO Overflow Behavior. 0 = stop enqueueing. 1 = overwrite oldest.
0	FIFO_EN	Output FIFO Mode Enable. 0 = direct output mode. 1 = FIFO output mode.

The FIFO_CTRL register configures the IMU output mode, FIFO overflow behavior, and watermark interrupt properties. The ADIS16575/ADIS16576/ADIS16577 IMU supports the following two output modes:

- Direct Output Mode. Inertial sample data is loaded directly to the output registers after processing. The data-ready signal pulses to indicate fresh data availability.

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- FIFO Output Mode. Fresh sample data is enqueued into an internal 512 sample FIFO. The data ready signal toggles during enqueue, allowing sampling rate monitoring. The host system can asynchronously pop the oldest sample data to the output registers by reading the DIAG_STAT register.

The FIFO contains six channels of 32-bit inertial data (direct or delta outputs as per the MSC_CTRL register, OUT_SEL bit, Bit 8), TEMP, DATA_CNTR, and TIME_STAMP. Status flags update continuously in both modes.

FIFO mode facilitates integration with nonreal-time systems like embedded Linux, preventing data loss. This mode offers flexibility in data reading timing and can buffer approximately 256 ms of samples at 4 kHz ODR. The buffering window can be extended using the decimation filter.

The watermark interrupt allows FIFO-level monitoring without reading FIFO_CNT. When enabled, this interrupt triggers based on the samples enqueued vs. the set threshold. This interrupt supports batch reading of multiple samples. When disabled, the WM pin is high-Z to prevent potential damage.

FILTER CONTROL REGISTER (FILT_CTRL)

Table 115. FILT_CTRL Register Definition

Addresses	Default	Access	Flash Backup
0x5C, 0x5D	0x0000	R/W	Yes

Table 116. FILT_CTRL Bit Definitions

Bits	Description
[15:3]	Not used
[2:0]	Filter Size Variable B; number of taps in each stage; $N = 2^B$

The FILT_CTRL register (see Table 115 and Table 116) provides user controls for the Bartlett window FIR filter (see Figure 44), which contains two cascaded averaging filters.

For example, use the following sequence to set Register FILT_CTRL, Bits[2:0], = 100, which sets each stage to have 16 taps: 0xCC04 and 0xCD00.

For example, if the user wants each filter stage to have 16 taps, the number of taps must be determined by using the $N = 2^B$ formula, where B is the value in Bits[2:0] of the FILT_CTRL register. To solve for B, calculate B = log2(16) = 4. In binary, this value represents 100.

To set this value in the register, follow this sequence:

1. Write 0xCC04 to the FILT_CTRL register. The 04 value sets Bits[2:0] to 100, corresponding to B = 4. As a result, each stage of the filter has 16 taps.
2. Write 0xCD00 to the FILT_CTRL register. This value completes the sequence and confirms the previous setting.

After completing these steps, each stage of the filter has 16 taps, which affects the characteristics of the filter, including its frequency response, delay, and noise reduction capability.

Figure 70 provides the frequency response for several settings in the FILT_CTRL register.

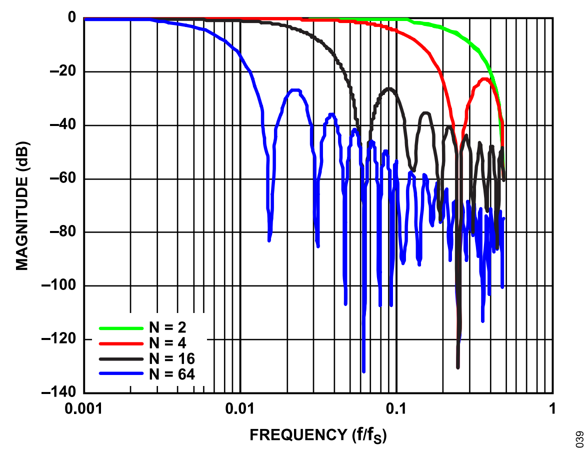

Figure 70. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

RANGE IDENTIFIER (RNG_MDL)

Table 117. RNG_MDL Register Definition

Addresses	Default	Access	Flash Backup
0x5E, 0x5F	Not applicable	R	No

Table 118. RNG_MDL Bit Definitions

Bits	Description
[15:3]	Not used
[3:2]	Gyroscope measurement range 01 = ±450°/sec (ADIS16575-2, ADIS16576-2, and ADIS16577-2) 10 = reserved 00 = reserved 11 = ±2000°/sec (ADIS16576-3, and ADIS16577-3)
[1:0]	Reserved, binary value = 11

MISCELLANEOUS CONTROL REGISTER (MSC_CTRL)

Table 119. MSC_CTRL Register Definition

Addresses	Default	Access	Flash Backup
0x60, 0x61	0x00C1	R/W	Yes

Table 120. MSC_CTRL Bit Definitions

Bits	Name	Description
[15:13]	RESERVED	Not used
12	SENS_BW	Internal Sensor Bandwidth Selection. This bit allows the selection between two different bandwidths for the IMUs internal sensors. 0 = wide bandwidth: 639 Hz (gyroscope) and 750 Hz (accelerometer), 1= medium bandwidth: ~370 Hz on accelerometers and gyroscopes.

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Table 120. MSC_CTRL Bit Definitions (Continued)

Bits	Name	Description
		Setting SENS_BW = 1 reprograms the sensor filters to 370 Hz, increasing the group delay by 0.17 ms for gyroscopes and 0.63 ms for accelerometers.
11	SYNC_4KHZ	4 kHz Internal Sync Enable Bit. By default, the IMU internal sample clock operates at 2 kHz. 0 = 2 kHz internal sample clock. 1 = 4 kHz internal sample clock. For 2 kHz operation with improved noise performance, set SYNC_4KHZ = 0 and enable a single average decimation filter (DEC_RATE = 1).
10	TS_32	Timestamp Bit Width. This bit controls the width of the timestamp register. 0 = 16-bit timestamp with 49.02 μs/LSB resolution. 1 = 32-bit timestamp with 0.01923 μs/LSB resolution.
9	BURST_32	32-Bit Burst Mode Enable. This bit enables 32-bit inertial outputs within the burst stream. The user must wait for a complete DR cycle before the burst array updates with the intended data type. 0 = 16-bit outputs. 1 = 32-bit inertial outputs in burst stream.
8	OUT_SEL	Output Selection: Chooses the specific type of inertial data transmitted during a burst read or added to the FIFO when operating in FIFO mode. 0 = the output incorporates gyroscope and accelerometer readings (default). 1 = the output comprises delta angle and delta velocity measurements.
7	GSEN_EN	G-Sensitivity Compensation Enable. This bit applies factory-calibrated linear acceleration (g-sensitivity) compensation data to the gyroscope outputs. 0 = disable. 1 = enable.
6	POP_EN	Point of Percussion Enable. This bit adjusts the acceleration sensors to a common point of percussion on the package corner, taking into account angular rotations on all three axes. 0 = disable. 1 = enable.
5		Reserved (do not use).
4		Reserved (do not use).
[3:2]	SYNC_M1 and SYNC_M0	Sync Mode Selection: Enables the synchronization mode. 00 = the internal clock drives the system sampling in the internal sync mode. The SYNC_4KHZ bit in the MSC_CTRL sets the internal clock rate to either 2 kHz or 4 kHz. 01 = direct external sync mode, where the system sample rate directly follows an external clock source with sync enabled as an input. For ideal operation, provide a 4 kHz sync input to maintain system synchronization. Only a single edge of the pulse is used for detection; therefore, the duty cycle can vary.
		10 = eternal sync mode with UP_SCALE, translating an external clock into an internal system sample rate. 11 = the internal sync drives the sampling clock, and the sync signal operates as an output.
1	SYNC_POL	Sync Polarity. This bit determines the sync signal behavior when used as an input or output. For an external sync (input), 1 = rising edge sensitive. 0 = falling edge sensitive. For an internal sync output), 1 = sampling is taking place. 0 = sampling is not taking place.
0	DR_POL	Data-Ready Polarity. This bit determines the stability of the output data. 1 = the output data is stable when the DR pin is logic high. 0 = the output data is stable when the DR pin is logic low.

Point of Percussion

Register MSC_CTRL, Bit 6 (see Table 120) offers an on or off control for the point of percussion alignment function, which maps the accelerometer sensors to the corner of the package shown in Figure 71. The factory default setting in the MSC_CTRL register activates this function. To turn this function off while retaining the rest of the factory default settings in the MSC_CTRL register, set Register MSC_CTRL, Bit 6 = 0, using the following command sequence on the DIN pin: 0xE041, then 0xE100.

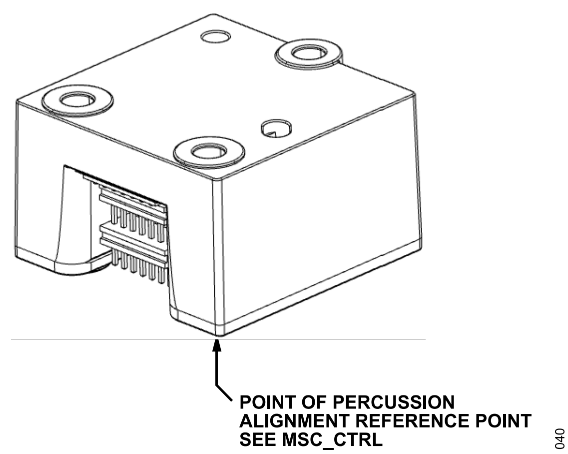

Figure 71. Point of Percussion Reference Point

Internal Clock Mode

Register MSC_CTRL, Bits[3:2] (see Table 120), provide four different configuration options for controlling the clock (f_{SM}; see Figure 42 and Figure 43), which controls data acquisition and processing for the inertial sensors. The default setting for Register MSC_CTRL,

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Bits[3:2] is 00 (binary), which places the ADIS16575/ADIS16576/ADIS16577 in internal clock mode. In this mode, an internal clock controls inertial sensor data acquisition and processing at a nominal rate of 2000 Hz (4 kHz if SYNC_4KHZ is enabled). All sensors are sampled at the IMU sample rate, ensuring synchronized data collection across the system.

Scaled Sync Mode

When Register MSC_CTRL, Bits[3:2] = 10, the ADIS16575/ADIS16576/ADIS16577 operate in scaled sync mode, supporting a frequency range of 0.8 Hz to 400 Hz for the clock signal on the SYNC pin. This mode is advantageous for synchronizing data processing with signals from other systems, such as a Global Navigation Satellite Systems (GNSS) PSS signal. In scaled sync mode, the sample clock frequency is determined by the product of the external clock scale factor (K_{ECSF}), set in the UP_SCALE register (see Table 121 and Table 122), and the frequency of the clock signal on the SYNC pin.

For example, to set up a sample rate of 2000 SPS using a 1 Hz input signal, configure the UP_SCALE register with a value of 0x07D0, which corresponds to a K_{ECSF} value of 2000 in decimal. This configuration results in a sample rate of 2000 SPS for both the inertial sensors and the signal processing. To achieve this setup, send the sequence 0xE2D0 followed by 0xE307 to the DIN pin.

Table 121. UP_SCALE Register Definition

Addresses	Default	Access	Flash Backup
0x62, 0x63	0x07D0	R/W	Yes

Table 122. UP_SCALE Bit Definitions

Bits	Description
[15:0]	K_{ECSF}; binary format

Output Sync Mode

When Register MSC_CTRL, Bits[3:2] = 11, the ADIS16575/ADIS16576/ADIS16577 operate in output sync mode, which is the same as internal clock mode with one exception: the SYNC pin pulses when the internal processor collects data from the inertial sensors. Figure 72 provides an example of this signal.

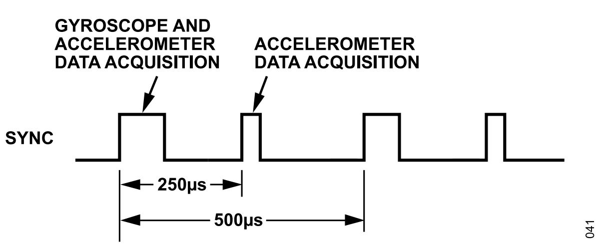

Figure 72. Sync Output Signal, Register MSC_CTRL, Bits[3:2] = 11

Data Update Rate in External Sync Modes

When using the input sync option in scaled sync mode (Register MSC_CTRL, Bits[3:2] = 10, see Table 120), the ODR is equal to

$$(f_{SYNC} \times K_{ECSF})/(DEC\_RATE + 1)$$

where:
f_{SYNC} is the clock signal frequency on the SYNC pin.
K_{ESCF} is the value from the UP_SCALE register (see Table 122).

In direct sync mode, the UP_SCALE register is not used, and the ODR directly follows the frequency of the external sync signal on the SYNC pin without any scaling.

DECIMATION FILTER (DEC_RATE)

Table 123. DEC_RATE Register Definition

Addresses	Default	Access	Flash Backup
0x64, 0x65	0x0000	R/W	Yes

Table 124. DEC_RATE Bit Definitions

Bits	Description
[15:11]	Don't care
[10:0]	Decimation rate, binary format, maximum = 1999

The DEC_RATE register (see Table 123 and Table 124) gives users control over the averaging decimating filter. This filter averages and decimates the data from the gyroscope and accelerometer, and it also extends the tracking time between each update for the delta angle and delta velocity. When operating the ADIS16575/ADIS16576/ADIS16577 in the default internal clock mode (refer to the Bits[3:2] in Table 120), users can calculate the nominal ODR using the following formula:

$$f_S/(DEC\_RATE + 1)$$

where f_S is the unit user-selected (2000 or 4000) sample rate. For example, to lower the output sample rate to 100 SPS (2000 ÷ 20), set the DEC_RATE to 0x0013. To do this setting, send the following sequence to the DIN pin: first 0xE413, then 0xE500.

CONTINUOUS BIAS ESTIMATION (NULL_CNFG)

Table 125. NULL_CNFG Register Definition

Addresses	Default	Access	Flash Backup
0x66, 0x67	0x070A	R/W	Yes

Table 126. NULL_CNFG Bit Definitions

Bits	Description
[15:14]	Not used
13	Z-axis accelerometer bias correction enable (1 = enabled)
12	Y-axis accelerometer bias correction enable (1 = enabled)
11	X-axis accelerometer bias correction enable (1 = enabled)
10	Z-axis gyroscope bias correction enable (1 = enabled)
9	Y-axis gyroscope bias correction enable (1 = enabled)
8	X-axis gyroscope bias correction enable (1 = enabled)
[7:4]	Not used
[3:0]	Time base control (TBC), range: 0 to 12 (default = 10); $t_B = 2^{TBC}/f_S$, f_S = the internal sample clock frequency (either 2000 Hz or 4000 Hz

USER REGISTER DEFINITIONS

Table 126. NULL_CNFG Bit Definitions (Continued)

Bits	Description
	depending on the configuration), time base; $t_A = 64 \times t_B$, average time.

The NULL_CNFG register (see Table 125 and Table 126) provides configuration controls for the CBE, which is associated with the bias correction update command in Register GLOB_CMD, Bit 0 (see Table 128). The CBE tracks a moving average of the sensor output for each enabled channel (gyroscope or accelerometer) over a programmable time window defined by Bits[3:0] of the NULL_CNFG register.

This moving average is calculated continuously and represents the estimated bias for each sensor axis. The resulting bias values are automatically written to the corresponding user offset registers, where they are applied to correct the sensor outputs in real time. Bits[13:8] of the NULL_CNFG register control whether bias correction is enabled for each specific sensor axis.

The factory default configuration for the NULL_CNFG register enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets the average null time to approximately 32 seconds.

GLOBAL COMMANDS (GLOB_CMD)

Table 127. GLOB_CMD Register Definition

Addresses	Default	Access	Flash Backup
0x68, 0x69	Not applicable	W	No

Table 128. GLOB_CMD Bit Definitions

Bits	Description
[15:8]	Not used
7	Software reset
6	Not used
5	FIFO flush
4	Flash memory test
3	Flash memory update
2	Sensor self-test
1	Factory calibration restore
0	Bias correction update

The GLOB_CMD register (see Table 127 and Table 128) provides trigger bits for several operations. Writing a 1 to the appropriate bit in the GLOB_CMD register initiates the corresponding function. During the execution of the flash memory update and factory calibration restore commands, data production stops, pulsing on the DR pin halts, and the SPI does not respond to requests. For other commands, the SPI remains accessible. Refer to the Table 1 for the execution time of each GLOB_CMD command.

Software Reset

Use the following DIN sequence to set Register GLOB_CMD, Bit 7 = 1, which triggers a reset: 0xE880, then 0xE900. This reset clears all data, reinitializes the inertial sensors, and then restarts data sampling and processing. This function provides a firmware alternative to toggling the $\overline{\text{RST}}$ pin (see Table 10, Pin 8).

FIFO Flush

Use the following DIN sequence to set Register GLOB_CMD, Bit 5 = 1, which triggers a FIFO flush: 0xEA80, then 0xEB00. This command clears all data currently stored in the FIFO buffer, ensuring that subsequent data reads start with fresh data. The FIFO flush operation is particularly useful when resetting the FIFO after an error condition or before starting a new data acquisition session. Unlike some other global commands, the SPI remains active and responsive during the execution of the FIFO flush command.

Flash Memory Test

Use the following DIN sequence to set Register GLOB_CMD, Bit 4 = 1, which tests the flash memory: 0xE810, then 0xE900. The command performs a CRC computation on the flash memory, including program memory and factory register data (excluding user register locations) and compares it to the original CRC value from the factory configuration process. If the current CRC value does not match the original CRC value, Register DIAG_STAT, Bit 6 (see Table 15), rises to 1, indicating a failing result.

Flash Memory Update

Use the following DIN sequence to set Register GLOB_CMD, Bit 3 = 1, which triggers a backup of all user-configurable registers in the flash memory: 0xE808, then 0xE900. Register DIAG_ STAT, Bit 2 (see Table 15), identifies success (0) or failure (1) in completing this process.

Sensor Self Test

Use the following DIN sequence to set Register GLOB_CMD, Bit 2 = 1, which triggers the self test routine for the inertial sensors: 0xE804, then 0xE900. The self test routine uses the following steps to validate the integrity of each inertial sensor:

1. Test communications to each sensor.
2. Measure the output on each sensor.
3. Activate an internal stimulus on the mechanical elements of each sensor to move them predictably and create an observable response.
4. Measure the output response on each sensor.
5. Deactivate the internal stimulus on each sensor.
6. Calculate the difference between the sensor measurements from Step 2 (stimulus is off) and Step 4 (stimulus is on).
7. Compare the difference with internal pass and fail criteria.
8. Report the pass and fail results to the DIAG_STAT register, Bit 5 (see Table 15).

USER REGISTER DEFINITIONS

Note that the motion during the execution of this test can lead to false failure results because the self test is designed to detect changes caused by the internal stimulus only.

Factory Restore

Use the following DIN sequence to set Register GLOB_CMD, Bit 1 = 1: 0xE802, then 0xE900. This command restores the factory default settings for the MSC_CTRL, DEC_RATE, UP_SCALE, FIFO_CTRL, FILT_CTRL, and NULL_CTRL registers and clears all user-configurable bias correction settings.

Executing this command also writes 0x0000 to the following bias registers: XG_BIAS_LWR, XG_BIAS_UPR, YG_BIAS_LWR, YG_BIAS_UPR, ZG_BIAS_LWR, ZG_BIAS_UPR, XA_BIAS_LWR, XA_BIAS_UPR, YA_BIAS_LWR, YA_BIAS_UPR, ZA_BIAS_LWR, and ZA_BIAS_UPR. Additionally, this command resets the control registers to their default values, as specified in the default value column in the corresponding register tables.

The factory restore command also automatically triggers a flash memory update, ensuring that the restored default settings persist through subsequent resets.

Bias Correction Update

Use the following DIN pin sequence to set Register GLOB_CMD, Bit 0 = 1, to trigger a bias correction, using the correction factors from the CBE (see Table 126): 0xE801, then 0xE900.

FIRMWARE REVISION (FW_REV)

Table 129. FW_REV Register Definition

Addresses	Default	Access	Flash Backup
0x6C, 0x6D	Not applicable	R	No

Table 130. FW_REV Bit Definitions

Bits	Description
[15:0]	Firmware revision, binary coded decimal (BCD) format

The FW_REV register (see Table 129 and Table 130) provides the firmware revision for the internal firmware. This register uses a BCD format, where each nibble represents a digit. For example, if FW_REV = 0x0104, the firmware revision is 1.04.

CALIBRATION DAY AND MONTH (DAY_MONTH)

Table 131. DAY_MONTH Register Definition

Addresses	Default	Access	Flash Backup
0x6E, 0x6F	Not applicable	R	No

Table 132. DAY_MONTH Bit Definitions

Bits	Description
[15:8]	Factory calibration month, BCD format
[7:0]	Factory calibration day, BCD format

The FIRM_DM register (see Table 131 and Table 132) contains the month and day of the factory calibration date. The DAY_MONTH register, Bits[15:8], contain digits representing the factory calibration month. For example, November is the 11th month in a year and is represented by the DAY_MONTH register, Bits[15:8] = 0x11. The DAY_MONTH register, Bits[7:0], contain the day of the factory configuration. For example, the 27th day of the month is represented by the DAY_MONTH register, Bits[7:0] = 0x27.

FIRMWARE REVISION YEAR (FIRM_YEAR)

Table 133. FIRM_YEAR Register Definition

Addresses	Default	Access	Flash Backup
0x70, 0x71	Not Applicable	R	No

Table 134. FIRM_YEAR Bit Definition

Bits	Descriptions
[15:0]	Factory Calibration Year, BCD format

The FIRM_YEAR register (see Table 133 and Table 134) contains the year of the factory calibration in BCD format. For example, the year 2023 is represented by the FIRM_YEAR register, Bits[15:0] = 0x2023.

PRODUCT IDENTIFICATION (PROD_ID)

Table 135. PROD_ID Register Definition

Addresses	Default[1]	Access	Flash Backup
0x72, 0x73	0x40BF 0x40C0 0x40C1	R	No

[1] 0x40BF is the default value for the ADIS16575, 0x40C0 is the default value for the ADIS16576, and 0x40C1 is the default value for the ADIS16577.

Table 136. PROD_ID Bit Definitions

Bits	Description
[15:0]	Product identification = 0x40BF (16575), 0X40C0 (16576), 0X40C1 (16577)

The PROD_ID register (see Table 135 and Table 136) contains the numerical portion of the device number (16575, 16576, or 16577). See Figure 54 for an example of how to use a looping read of this register to validate the integrity of the communication.

SERIAL NUMBER (SERIAL_NUM)

Table 137. SERIAL_NUM Register Definition

Addresses	Default	Access	Flash Backup
0x74, 0x75	Not applicable	R	No

Table 138. SERIAL_NUM Bit Definitions

Bits	Description
[15:0]	Lot specific serial number

USER REGISTER DEFINITIONS

SCRATCH REGISTERS (USER_SCR_1 TO USER_SCR_3)

Table 139. USER_SCR_1 Register Definition

Addresses	Default	Access	Flash Backup
0x76, 0x77	Not applicable	R/W	Yes

Table 140. USER_SCR_1 Bit Definitions

Bits	Description
[15:0]	User defined

Table 141. USER_SCR_2 Register Definition

Addresses	Default	Access	Flash Backup
0x78, 0x79	Not applicable	R/W	Yes

Table 142. USER_SCR_2 Bit Definitions

Bits	Description
[15:0]	User defined

Table 143. USER_SCR_3 Register Definition

Addresses	Default	Access	Flash Backup
0x7A, 0x7B	Not applicable	R/W	Yes

Table 144. USER_SCR_3 Bit Definitions

Bits	Description
[15:0]	User defined

The USER_SCR_1 (see Table 139 and Table 140), USER_SCR_2 (see Table 141 and Table 142), and USER_SCR_3 (see Table 143 and Table 144) registers provide three locations for the user to store information. To ensure that the stored information is retained after a power cycle, execute a flash memory update command (Register GLOB_CMD, Bit 3; see Table 128) after writing to these registers.

FLASH MEMORY ENDURANCE COUNTER (FLSHCNT_LWR AND FLSHCNT_UPR)

Table 145. FLSHCNT_LWR Register Definition

Addresses	Default	Access	Flash Backup
0x7C, 0x7D	Not applicable	R	No

Table 146. FLSHCNT_LWR Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, low word

Table 147. FLSHCNT_UPR Register Definition

Addresses	Default	Access	Flash Backup
0x7E, 0x7F	Not applicable	R	No

Table 148. FLSHCNT_UPR Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, high word

The FLSHCNT_LWR (see Table 145 and Table 146) and FLSHCNT_UPR (see Table 147 and Table 148) registers combine to provide a 32-bit binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on T_J. Figure 73 guides estimating the retention life for the flash memory at specific T_J values. T_J is approximately 7°C more than T_C.

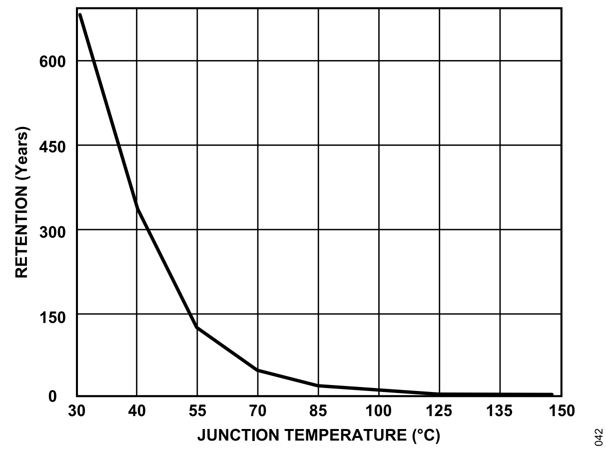

Figure 73. Flash Memory Retention

APPLICATIONS INFORMATION

ASSEMBLY AND HANDLING TIPS

Mounting Tips

The ADIS16575/ADIS16576/ADIS16577 package supports installation onto a PCB or rigid enclosure using three M2 or 2-56 machine screws, with a recommended torque between 20 inch ounces and 40 inch ounces. The devices feature three mounting holes located at three corners of the package, as well as two smaller alignment holes. These alignment holes, positioned near the top right and bottom left corners, aid in precise positioning during installation.

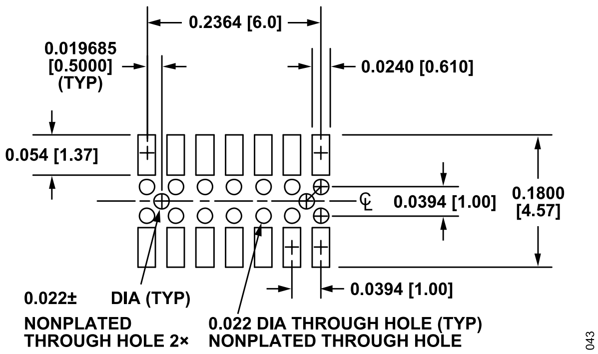

Figure 74. Mating Connector Design Detail

When designing a mechanical interface for the ADIS16575/ADIS16576/ADIS16577, use the alignment holes to ensure accurate placement and avoid placing unnecessary translational stress on the electrical connector because it can influence the bias repeatability behaviors of the inertial sensors.

For installations where the mating PCB also includes the electrical connector, pass-through holes for the mounting screws may be required. Figure 74 provides a detailed view of the PCB pad design when using one of the connector variants in the CLM-107-02 family.

Figure 75 shows the top view of the ADIS16575/ADIS16576/ADIS16577, showing mounting screw holes and alignment holes.

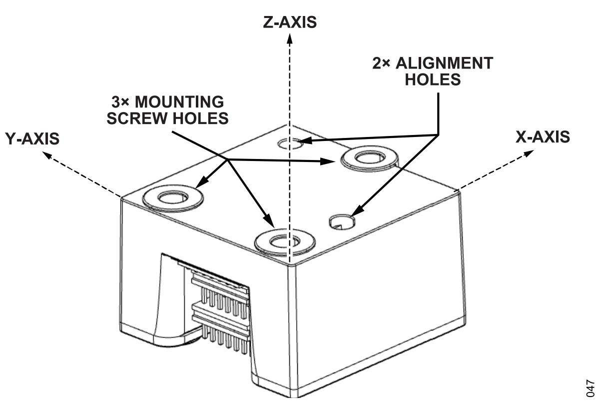

Figure 75. Mounting and Alignment Holes

POWER SUPPLY CONSIDERATIONS

The ADIS16575/ADIS16576/ADIS16577 contain 11.5 µF of decoupling capacitance across the VDD and GND pins. When the VDD voltage rises from 0 V to 3.3 V, the charging current for this capacitor bank imposes the following current profile (in amperes):

$$I_{DD}\left(t\right) = C\frac{\mathrm{d}\,V_{DD}(t)}{\mathrm{d}\,t} = 11.5 \times 10^{-6} \times \frac{\mathrm{d}\,V_{DD}(t)}{\mathrm{d}\,t}$$

where:
$I_{DD}(t)$ is the current demand on the VDD pin during the initial power supply ramp with respect to time.
C is the internal capacitance across the VDD and GND pins (11.5 µF).
$V_{DD}(t)$ is the voltage on the VDD pin with respect to time.

For example, if VDD follows a linear ramp from 0 V to 3.3 V in 66 µs, the charging current is 575 mA for that time frame. The ADIS16575/ADIS16576/ADIS16577 also contain embedded processing functions that present transient current demands during initialization or reset recovery operations. During these processes, the peak current demand reaches 250 mA and occurs approximately 80 ms after VDD reaches 3.0 V (or ~80 ms after initiating a reset sequence).

APPLICATIONS INFORMATION

EVALUATION TOOLS

Breakout Board, ADIS16IMU5/PCBZ

The ADIS16IMU5/PCBZ breakout board provides a ribbon cable interface for a simple connection to an embedded processor development system. Figure 76 shows the electrical schematic, and Figure 78 shows a top view for this breakout board. J2 mates directly to the electrical connector on the ADIS16575/ADIS16576/ADIS16577, and J1 easily mates to a 1 mm ribbon cable system.

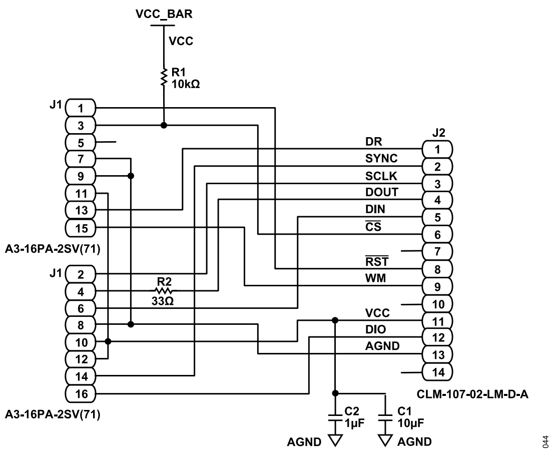

Figure 76. ADIS16IMU5/PCBZ Electrical Schematic

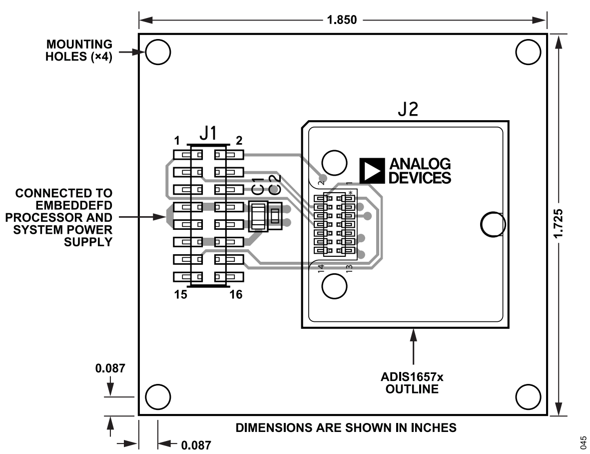

Figure 77. ADIS16IMU5/PCBZ Top View

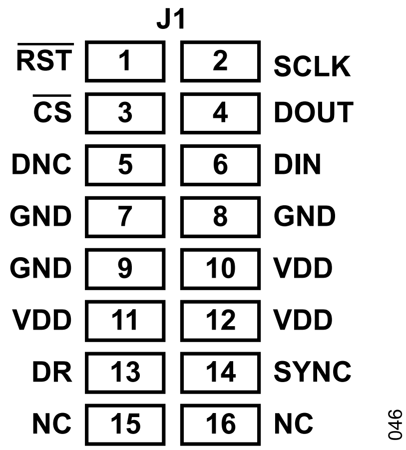

Figure 78. ADIS16IMU5/PCBZ J1 Pin Assignments

EVAL-ADIS-FX3 PC-Based Evaluation

The ADIS16IMU5/PCBZ provides a simple way to connect the ADIS16575/ADIS16576/ADIS16577 to the EVAL-ADIS-FX3 evaluation system, which provides a PC-based method for evaluating essential function and performance. For more information, visit the EVAL-ADIS-FX3 Wiki Guide.

SPI OPERATION

Validating SPI Communications

The ADIS16575/ADIS16576/ADIS16577 provide multiple mechanisms to validate and verify SPI transactions, ensuring reliable communication.

SPI Error Bit

The DIAG_STAT register includes an SPI communication error bit (Bit 3). This bit is set to 1 when an SPI communication error is detected, such as an incorrect number of clock cycles (see Table 15). Regularly checking this bit can help identify communication issues.

Burst Read Checksum

When performing a burst read operation, a 16-bit checksum is included at the end of the data stream. This checksum allows the host system to verify the integrity of the received data. To validate this checksum, take the following steps:

- Calculate the checksum of the received data (excluding FIFO_CNT).
- Compare this checksum with the checksum value received in burst read mode.
- If these checksums match, the data transfer was likely successful.

APPLICATIONS INFORMATION

SPI_CHKSUM Register

The SPI_CHKSUM register (Address 0x3E and Address, 0x3F) provides a running checksum of all register data transmitted during the current sample period. This checksum allows for validation of arbitrary register read sequences. To use the SPI_CHKSUM register for validation, follow these steps:

1. Read the desired registers.
2. Calculate the byte-wise sum of all received data.
3. Read and compare the value with the SPI_CHKSUM register value.

Note that a mismatch indicates potential data corruption or a read sequence split across multiple samples.

Best practices for SPI communication validation include the following:

- Regularly monitoring the SPI error bit in the DIAG_STAT register.
- Using burst read checksums for efficient validation of bulk data transfers.
- Utilizing the SPI_CHKSUM register to verify the integrity of custom register read sequences.

By employing these validation methods, users can ensure robust and reliable SPI communication with the ADIS16575/ADIS16576/ADIS16577 devices.

DIGITAL RESOLUTION OF GYROSCOPES AND ACCELEROMETERS

Gyroscope Data Width (Digital Resolution)

The gyroscope data in the ADIS16575/ADIS16576/ADIS16577 is provided in a 32-bit format, split across two 16-bit registers for each axis (X_GYRO_UPR, X_GYRO_LWR, Y_GYRO_UPR, Y_GYRO_LWR, Z_GYRO_UPR, and Z_GYRO_LWR).

It is recommended to always read both the x_GYRO_UPR and x_GYRO_LWR registers for each axis to obtain the full 32-bit gyroscope data. This approach ensures that the complete resolution of the gyroscope measurements, even at full ODR, is captured.

The decimation filter (DEC_RATE register, see Table 124) and Bartlett window filter (FILT_CTRL register, see Table 116) can further increase the effective resolution of the gyroscope data when applied.

Accelerometer Data Width (Digital Resolution)

The accelerometer data in the ADIS16575/ADIS16576/ADIS16577 is provided in a 32-bit format, split across two 16-bit registers for each axis (X_ACCL_UPR, X_ACCL_LWR, Y_ACCL_UPR, Y_ACCL_LWR, Z_ACCL_UPR, and Z_ACCL_LWR).

It is recommended to always read both x_ACCL_UPR and x_ACCL_LWR registers for each axis to obtain the full 32-bit accelerometer data. This approach ensures that the complete resolution of the accelerometer measurements, even at full ODR, is captured.

The decimation filter (DEC_RATE register, Table 124) and Bartlett window filter (FILT_CTRL register, see Table 116) can further increase the effective resolution of the accelerometer data when applied.

OUTLINE DIMENSIONS

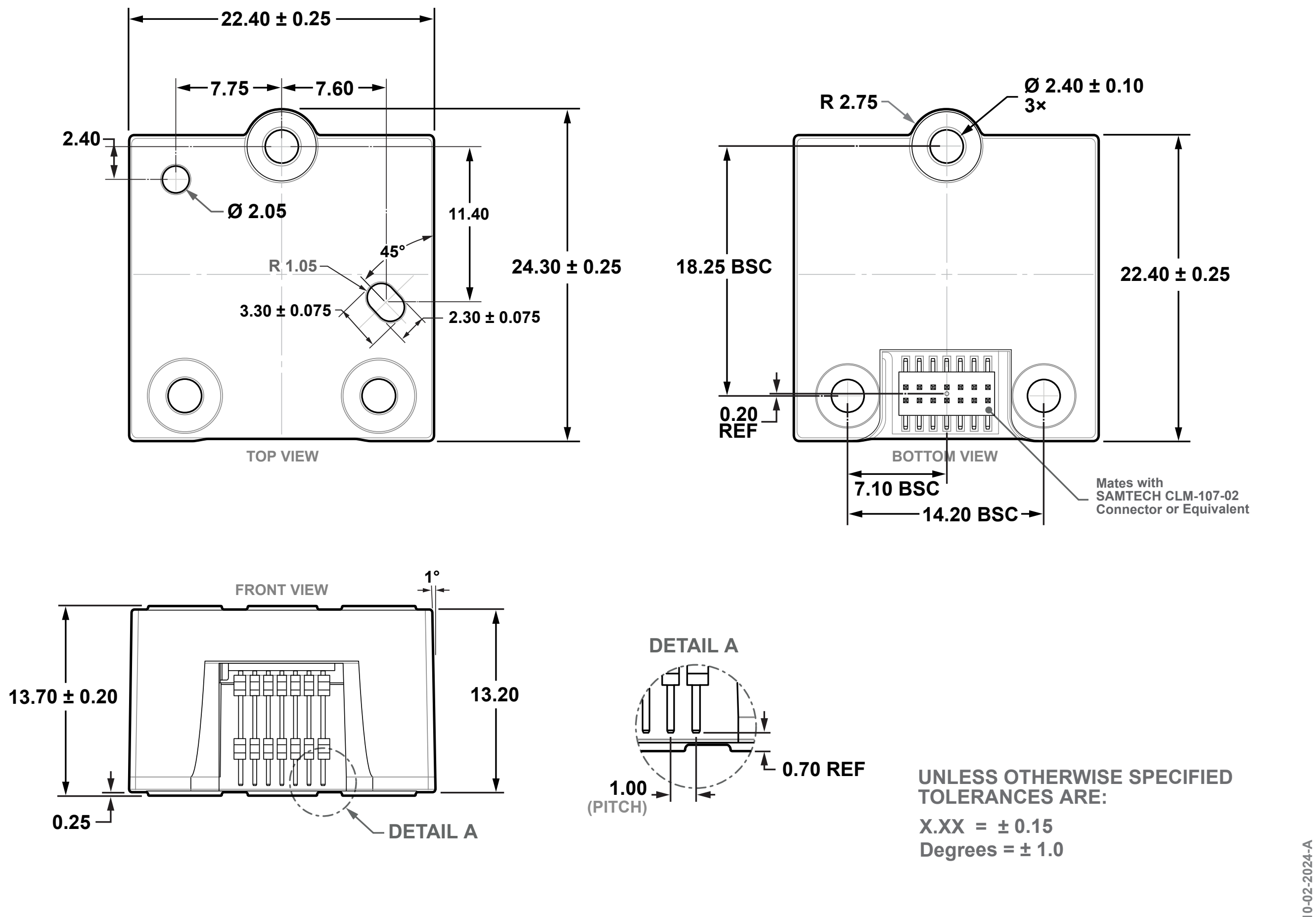

Figure 79. 14-Lead Module with Connector Interface [MODULE]
(ML-14-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16575-2BMLZ	−40°C to +105°C	14-Lead Module with Connector Interface [MODULE]	ML-14-10
ADIS16576-2BMLZ	−40°C to +105°C	14-Lead Module with Connector Interface [MODULE]	ML-14-10
ADIS16576-3BMLZ	−40°C to +105°C	14-Lead Module with Connector Interface [MODULE]	ML-14-10
ADIS16577-2BMLZ	−40°C to +105°C	14-Lead Module with Connector Interface [MODULE]	ML-14-10
ADIS16577-3BMLZ	−40°C to +105°C	14-Lead Module with Connector Interface [MODULE]	ML-14-10

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Table 149. Evaluation Boards

Model[1]	Description
ADIS16IMU5/PCBZ	ADIS16IMU5/PCBZ Evaluation Board
EVAL-ADIS-FX3Z	EVAL-ADIS-FX3Z Evaluation Board

[1] Z = RoHS-Compliant Part.

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