Robust, Industrial, Low Latency and Low Power 10/100/1000 Mbps Ethernet PHY with Copper and Fiber Interface

FEATURES

- 1Gb Ethernet PHY IEEE 802.3 compliant
  - Support copper and fiber Interface
  - 10BASE-T/100BASE-TX/1000BASE-T
  - 100BASE-FX/1000BASE-X, and 1000BASE-KX
  - Media converter mode between copper and fiber
  - Bridge mode between RGMII and SGMII
- MII, RMII, RGMII, and SGMII MAC interfaces
- Low latency performance
  - 1000BASE-T RGMII latency transmit <70ns, receive <230ns
  - 100BASE-TX MII latency transmit <55ns, receive <250ns
- Wake-on-LAN (WoL)
- EEE in accordance with IEEE 802.3az
- EMC tests standards
  - IEC 61000-4-5 surge (Class A ±4kV)
  - IEC 61000-4-4 electrical fast transient (EFT) (Class A ±1kV, Class B ±4kV)
  - IEC 61000-4-2 ESD (Class A ±2kV, Class B ±8kV contact discharge)
  - IEC 61000-4-6 conducted immunity (Class A: 10V)
  - IEC 61000-4-3 radiated immunity
    - 80MHz to 1GHz (Class A: 10V/m)
    - 1GHz to 3.2GHz (Class A: 3V/m)
    - 3.2GHz to 6GHz (Class A: 1V/m)
  - EN55032 radiated emissions (Class B)
  - EN55032 conducted emissions (Class B)
- Unmanaged configuration using multilevel pin strapping
- MDIO/MDC management interface and interrupt pin
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Voltage mode MDI drivers, eliminates termination resistors
- Automatic polarity and pair swap correction
- Cable diagnostics (TDR and signal analysis)
- Frame generator and checker, multiple loopback modes
- 3 × Configurable LEDs
- 48-lead, 7mm × 7mm LFCSP small package, at −40°C to +105°C ambient operation
- Low power consumption
  - 95mW for 1000BASE-X
  - 339mW for 1000BASE-T
  - 3.3V/2.5V/1.8V MDIO and MAC interface VDDIO supply
  - Integrated power supply monitoring and POR

APPLICATIONS

- Energy distribution and energy automation
- Robotics/motion control
- Factory automation and industrial automation
- Test and measurement

GENERAL DESCRIPTION

The ADIN1320 is a low-power, single port Gigabit Ethernet transceiver that supports copper, fiber, and backplane Ethernet connectivity. Its key features include low latency and energy efficient operation, making it an excellent choice for a wide range of industrial Ethernet applications where performance and power efficiency are critical.

It integrates a high performance energy efficient Ethernet (EEE) PHY core along with a robust SerDes subsystem, enabling operation over 10BASE-T, 100BASE-TX, 1000BASE-T, 100BASE-FX, 1000BASE-X, and 1000BASE-KX physical layers. The device supports multiple MAC-side interfaces including SGMII, RGMII, RMII, and MII; and enables a variety of operating modes such as SGMII/RGMII/RMII/MII to Copper, RGMII/RMII/MII to fiber, RGMII/RMII/MII to copper or fiber automatic media selection, copper to fiber media conversion, and SGMII to RGMII bridging. This versatility allows the ADIN1320 to function as a copper PHY, fiber PHY, mixed-media PHY, media converter, or MAC-interface bridge depending on system requirements.

The MII management interface (MDIO) provides a 2-wire serial connection between a host processor or MAC and the ADIN1320, enabling access to control and status registers within the PHY Core, SerDes subsystem, and GE subsystem. It supports both IEEE 802.3 Clause 22 and Clause 45 frame structures, ensuring compatibility with a wide range of Ethernet controllers and systems.

The ADIN1320 is offered in a compact 7mm × 7mm, 48-lead lead frame chip scale package (LFCSP) making it suitable for space-constrained designs. It operates from two power supplies (0.9V and 3.3V), with flexible VDDIO options (1.8V, 2.5V, or 3.3V) for MDIO and MAC interfaces. On power-up, the device remains in hardware reset until all supply voltages exceed their required thresholds. Integrated brownout protection holds the device in reset if supply voltages fall below minimum levels, and it resumes operation automatically once conditions are restored.

The ADIN1320 supports copper cables up to 150m at 1Gbps and 180m at 100Mbps or 10Mbps. Note that throughout this data sheet, multifunction pins, such as XTAL_I/CLK_IN/REF_CLK, are referred to either by the entire pin name or by a single function of the pin, for example, XTAL_I/CLK_IN, when only that function is relevant.

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REVISION HISTORY

7/2026—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

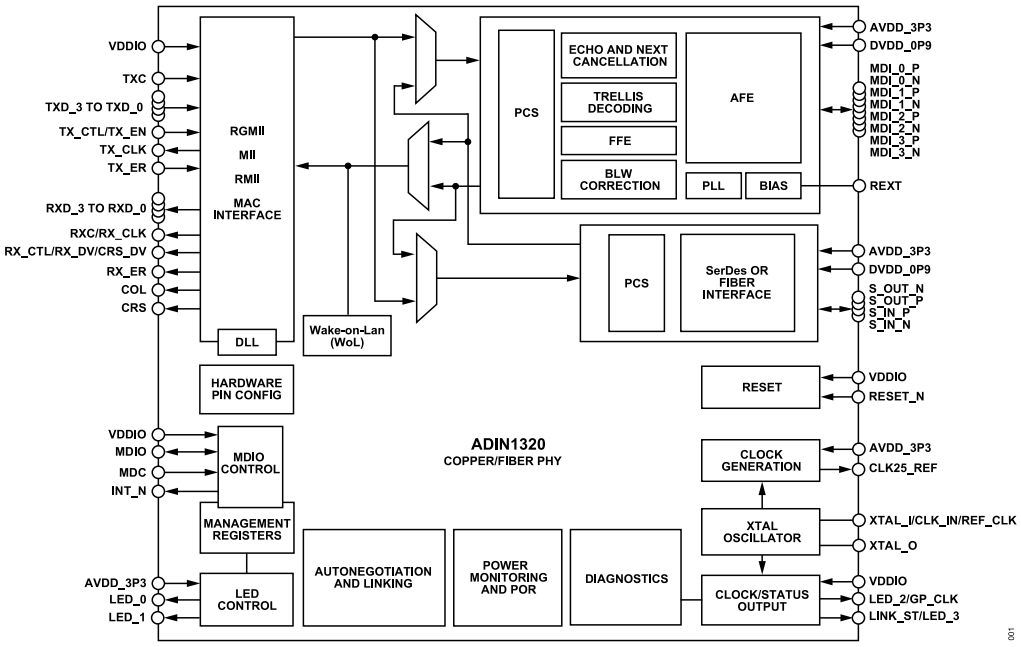


Figure 1. ADIN1320 Functional Block Diagram

SPECIFICATIONS

AVDD_3P3 = 3.3V, VDDIO = 1.8V, DVDD_0P9 = 0.9V, all specifications at −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltages					
AVDD_3P3	3.135	3.3	3.465	V	
DVDD_0P9	0.855	0.9	0.945	V	
VDDIO	3.135	3.3	3.465	V	
	2.25	2.5	2.75	V	
	1.71	1.8	1.89	V	
POWER CONSUMPTION[1]					100% data throughput, full activity
Supply Current RGMII 1000BASE-T					
AVDD_3P3 Current (I_{AVDD_3P3})		70.5		mA	
DVDD_0P9 Current (I_{DVDD_0P9})		44		mA	
VDDIO Current (I_{VDDIO})		49		mA	VDDIO = 3.3V
		42		mA	VDDIO = 2.5V
		37		mA	VDDIO = 1.8V
Total Power		434		mW	VDDIO = 3.3V
		377		mW	VDDIO = 2.5V
		339		mW	VDDIO = 1.8V
Supply Current SGMII 1000BASE-T, 1G Media Converter					
I_{AVDD_3P3}		74		mA	
I_{DVDD_0P9}		65		mA	
I_{VDDIO}		24		mA	VDDIO = 3.3V
		24		mA	VDDIO = 2.5V
		24		mA	VDDIO = 1.8V
Total Power		382		mW	VDDIO = 3.3V
		363		mW	VDDIO = 2.5V
		346		mW	VDDIO = 1.8V
Supply Current RGMII 1000BASE-X					
I_{AVDD_3P3}		12		mA	
I_{DVDD_0P9}		33		mA	
I_{VDDIO}		26		mA	VDDIO = 3.3V
		19		mA	VDDIO = 2.5V
		14		mA	VDDIO = 1.8V
Total Power		155		mW	VDDIO = 3.3V
		117		mW	VDDIO = 2.5V
		95		mW	VDDIO = 1.8V
Supply Current RGMII 100BASE-TX					
I_{AVDD_3P3}		39		mA	
I_{DVDD_0P9}		14		mA	
I_{VDDIO}		11		mA	VDDIO = 3.3V
		10		mA	VDDIO = 2.5V
		9		mA	VDDIO = 1.8V
Total Power		178		mW	VDDIO = 3.3V

SPECIFICATIONS

Table 1. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
		166		mW	VDDIO = 2.5V
		158		mW	VDDIO = 1.8V
Supply Current SGMII 100BASE-TX					
I_{AVDD_3P3}		43		mA	
I_{DVDD_0P9}		34		mA	
I_{VDDIO}		7		mA	VDDIO = 3.3V
		7		mA	VDDIO = 2.5V
		7		mA	VDDIO = 1.8V
Total Power		196		mW	VDDIO = 3.3V
		190		mW	VDDIO = 2.5V
		185		mW	VDDIO = 1.8V
Supply Current RGMII 100BASE-FX					
I_{AVDD_3P3}		14		mA	
I_{DVDD_0P9}		31		mA	
I_{VDDIO}		5		mA	VDDIO = 3.3V
		4		mA	VDDIO = 2.5V
		3		mA	VDDIO = 1.8V
Total Power		91		mW	VDDIO = 3.3V
		84		mW	VDDIO = 2.5V
		80		mW	VDDIO = 1.8V
Supply Current, SGMII - RGMII Bridge Mode, 1G					
I_{AVDD_3P3}		13		mA	
I_{DVDD_0P9}		27		mA	
I_{VDDIO}		26		mA	VDDIO = 3.3V
		19		mA	VDDIO = 2.5V
		14		mA	VDDIO = 1.8V
Total Power		153		mW	VDDIO = 3.3V
		115		mW	VDDIO = 2.5V
		92		mW	VDDIO = 1.8V
TIMING/LATENCY[2]					
1000BASE-T RGMII					
Transmit	60	64	68	ns	
Receive			226	ns	
Total	286	290	294	ns	
100BASE-TX MII					
Transmit			52	ns	
Receive			248	ns	
Total			300	ns	
100BASE-TX RGMII[3]					
Transmit	84	88	92	ns	
Receive			250	ns	
Total	334	338	342	ns	
100BASE-TX RGMII[4]					
Transmit	84	104	124	ns	
Receive			250	ns	

SPECIFICATIONS

Table 1. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total	334	354	374	ns	
100BASE-TX RMII[5]					
Transmit	72		92	ns	
Receive	328	348	368	ns	
Total	400	430	460	ns	
1000BASE-T SGMII					
Transmit	183		191	ns	
Receive	303		319	ns	
Total	486		510	ns	
100BASE-TX SGMII					
Transmit	259		331	ns	
Receive	575		623	ns	
Total	834		954	ns	
1000BASE-X RGMII					
Transmit	79		95	ns	
Receive	142		150	ns	
Total	221		245	ns	
100BASE-FX RGMII					
Transmit	200		240	ns	
Receive			264	ns	
Total			504	ns	
100BASE-FX RMII					
Transmit	116		144	ns	
Receive	345		385	ns	
Total	461		529	ns	
100BASE-FX MII					
Transmit	54.4		62.4	ns	
Receive			225	ns	
Total			287.4	ns	
DIGITAL INPUTS/OUTPUTS					Applies to MAC interface, MDC pin, MDIO pin, and INT_N pin
VDDIO = 3.3V					
Input Low Voltage (V_{IL})			0.8	V	
Input High Voltage (V_{IH})	2.0			V	
Output Low Voltage (V_{OL})			0.4	V	Output low current (I_{OL}) (min) = 4mA
Output High Voltage (V_{OH})	2.4			V	Output high current (I_{OH}) (min) = 4mA
VDDIO = 2.5V					
V_{IL}			0.7	V	
V_{IH}	1.7			V	
V_{OL}			0.4	V	I_{OL} (min) = 4mA
V_{OH}	2.0			V	I_{OH} (min) = 2mA
	1.7				I_{OH} (min) = 4mA
VDDIO = 1.8V					
V_{IL}			0.35 × VDDIO	V	

SPECIFICATIONS

Table 1. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
V_{IH}	0.65 × VDDIO			V	
V_{OL}			0.45	V	I_{OL} (min) = 2mA
V_{OH}	VDDIO − 0.45			V	I_{OH} (min) = 2mA
AVDD_3P3					Applies to COL/TX_ER function of the LED_1/COL/TX_ER/ LSFLD_CFG pin
V_{IL}			0.8	V	
V_{IH}	2.0			V	
V_{OL}			0.4	V	I_{OL} (min) = 4mA
V_{OH}	2.4			V	I_{OH} (min) = 4mA
Input Leakage Current High (I_{IH}) and Input Leakage Current Low (I_{IL})			10	µA	Except pins with internal pull-down resistors
LED OUTPUT					Applies to LED_0 and LED_1
Output Drive Current	8			mA	AVDD_3P3 = 3.3V
SGMII					AC-coupled; S_OUT_P, S_OUT_N, S_IN_P, S_IN_N
Transmit Output Differential Voltage	0.15		0.4	V	SGMII mode per Version 1.8 to copper small form-factor pluggable (SFP) or PHY
	0.8		1.6	V_{p-p}	1000BASE-KX
	0.5		2.4	V_{p-p}	1000BASE-X, 100BASE-FX
Receiver Input Differential Voltage	0.175		2.0	V_{p-p}	AC-coupled; S_IN_P and S_IN_N; DC level biased in receiver
Receiver Input Impedance	80	100	120	Ω	Differential, integrated on chip
CLOCKS					
External Crystal (XTAL)					Requirements for external crystal used on XTAL_I pin and XTAL_O pin
Crystal Frequency		25		MHz	
Crystal Frequency Tolerance	−50		+50	ppm	
Crystal Frequency Stability	-30		+30	ppm	
Crystal Output Drive Level		<200		µW	
Crystal ESR		20	100	Ω	
Crystal Load Capacitance (C_L)[6]		10		pF	
XTAL_I Jitter			80	ps	Over frequency range 10kHz to 5MHz
Clock Input Frequency (CLK_IN)		25		MHz	Requirements for external clock applied to XTAL_I pin, MII, RGMII modes
		50		MHz	RMII mode
Clock Input Voltage Range (CLK_IN)	1.62		3.63	V	

[1] MAC interface capacitive load of 5pF, REFCLK is disabled.

[2] Guaranteed by design. The DPTH_MII_BYTE register defines whether the programmed transmit first in, first out (FIFO) depth is bytes or nibbles for MII modes (10BASE-T and 100BASE-TX). The register defaults to 1, which corresponds to bytes. In 10BASE-T and 100BASE-TX, because the MAC-PHY interface is nibble based, the internal prefill in the transmit FIFO is larger and is observed as longer latency times. The latency specifications in Table 1 have this bit set to 0.

[3] This 100BASE-TX RGMII transmit latency is where the transit FIFO is programmed for synchronous operation (MAC transmit clock must be synchronous with the ADIN1320 reference clock), see the FIFO_SYNC register.

[4] This 100BASE-TX RGMII transmit latency is where the MAC transmit clock does not have to be synchronous with the ADIN1320 reference clock and the transmit FIFO takes care of any phase difference.

[5] The RMII transmit latency depends on the phase relationship between the 50MHz reference clock and the internal 25MHz clock. The transmit latency is fixed for a given link.

SPECIFICATIONS

[6] Where load capacitance (C_L) = ((C1 × C2)/(C1 + C2) + C_{STRAY}), where C_{STRAY} is the stray capacitance including routing and package parasitics.

TIMING CHARACTERISTICS

Rise and fall time specifications are defined from 10% to 90%, unless otherwise noted.

Power-Up Timing

Table 2. Power-Up Timing

Parameter	Description	Min	Typ	Max	Unit
t_{RAMP}	Power supply ramp time			40	ms
t_1	Minimum time interval to internal power good[1]		6.8		ms
t_2	XTAL_I crystal settling time		1.5	2	ms
	XTAL_I external clock settling time			20	µs
t_3	Hardware configuration latch time			64	µs
t_4	Management interface active			5	ms

[1] The minimum time interval is referenced to the last supply to reach its rising threshold. There is no specific power supply sequencing required.

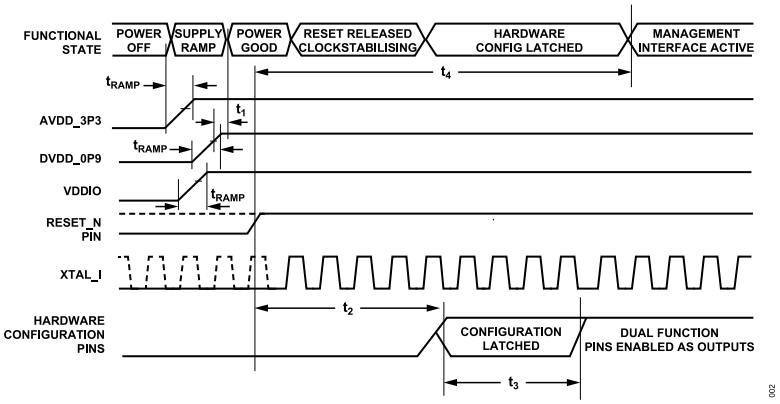


Figure 2. Power-Up Timing

Hardware Reset Timing

Table 3. Hardware Reset Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	RESET_N low time	10			µs
t_2	XTAL_I crystal settling time		1.5		ms
	XTAL_I external clock settling time		0		ms
t_3	Hardware configuration latch time			64	µs
t_4	Management interface active			5	ms

SPECIFICATIONS

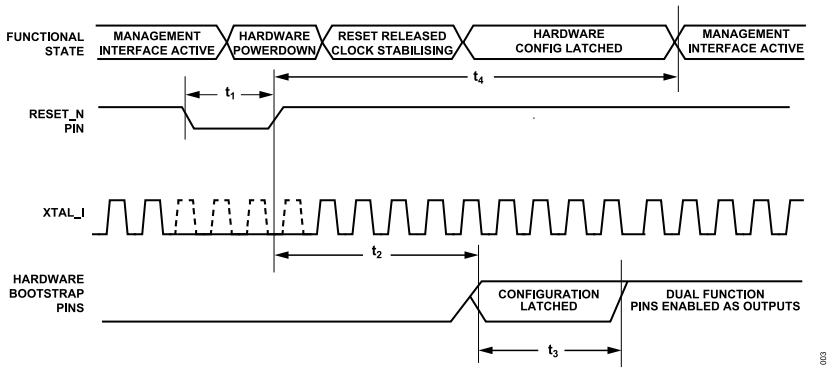


Figure 3. Hardware Reset Timing

Management Interface Timing

Table 4. Management Interface Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	MDC period	180			ns
t_2	MDC high time	70			ns
t_3	MDC low time	70			ns
t_4	MDC rise/fall time			5	ns
t_5	MDIO signal setup time to MDC	10			ns
t_6	MDIO signal hold time to MDC	10			ns
t_7	MDIO delay time to MDC	0		60	ns

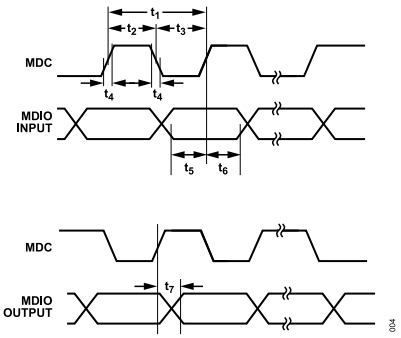


Figure 4. Management Interface Timing

MII Transmit and Receive Timing

Table 5. MII 100Mbps Transmit Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	TX_CLK period		40		ns
t_2	TX_CLK high time	14	20	26	ns
t_3	TX_CLK low time	14	20	26	ns
t_4	TX_CLK rise/fall time		5		ns
t_5	MII input signal (TXD_0 to TXD_3, TX_EN, TX_ER) setup time to TX_CLK	10			ns
t_6	MII input signal (TXD_0 to TXD_3, TX_EN, TX_ER) hold time to TX_CLK	0			ns

SPECIFICATIONS

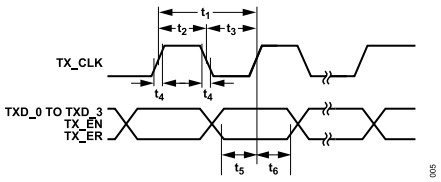


Figure 5. MII Transmit Timing

Table 6. MII 100Mbps Receive Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	RX_CLK period		40		ns
t_2	RX_CLK high time	16	20	24	ns
t_3	RX_CLK low time	16	20	24	ns
t_4	RX_CLK rise/fall time			1	ns
t_5	MII output signal (RXD_0 to RXD_3, RX_DV, RX_ER) setup time to RX_CLK	10			ns
t_6	MII output signal (RXD_0 to RXD_3, RX_DV, RX_ER) hold time to RX_CLK	10			ns

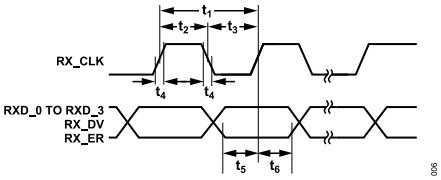


Figure 6. MII Receive Timing

Table 7. MII 10Mbps Transmit Timing (See Figure 5)

Parameter	Description	Min	Typ	Max	Unit
t_1	TX_CLK period		400		ns
t_2	TX_CLK high time	140	200	260	ns
t_3	TX_CLK low time	140	200	260	ns
t_4	TX_CLK rise/fall time		1		ns
t_5	MII input signal (TXD_0 to TXD_3, TX_EN, TX_ER) setup time to TX_CLK	10			ns
t_6	MII input signal (TXD_0 to TXD_3, TX_EN, TX_ER) hold time to TX_CLK	0			ns

Table 8. MII 10Mbps Receive Timing (See Figure 6)

Parameter	Description	Min	Typ	Max	Unit
t_1	RX_CLK period		400		ns
t_2	RX_CLK high time	140	200	260	ns
t_3	RX_CLK low time	140	200	260	ns
t_4	RX_CLK rise/fall time		1	1	ns
t_5	MII output signal (RXD_0 to RXD_3, RX_DV, RX_ER) setup time to RX_CLK	10			ns
t_6	MII output signal (RXD_0 to RXD_3, RX_DV, RX_ER) hold time to RX_CLK	10			ns

RGMII Transmit/Receive

Table 9. RGMII Timing

Parameter[1, 2]	Description	Min	Typ	Max	Unit
t_1	Data to clock output skew (at transmitter)[3]	−500	0	+500	ps
t_2	Data to clock input skew (at receiver)[3]	1	1.8	2.6	ns

SPECIFICATIONS

Table 9. RGMII Timing (Continued)

Parameter[1, 2]	Description	Min	Typ	Max	Unit
t_3	Data to clock output setup time (at transmitter – internal delay)[4]	1.2	2.0		ns
t_4	Clock to data output hold time (at transmitter – internal delay)[4]	1.2	2.0		ns
t_5	Data to clock input setup time (at receiver – internal delay)[4]	1.0	2.0		ns
t_6	Clock to data input hold time (at receiver – internal delay)[4]	1.0	2.0		ns
t_{CYC}	Clock cycle duration[5]	7.2	8	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10Mbps/100Mbps	40	50	60	%
t_R/t_F	Rise/fall time (20% to 80%)			0.75	ns

1 Timing specifications as per RGMII v2.0 standard.

2 Refer to example diagrams in the RGMII Timing Examples section.

3 When operating without RGMII internal delay, the printed circuit board (PCB) design requires clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns is added to the associated clock signal. For 10Mbps/100Mbps, the max value is unspecified.

4 Hardware and software programmable internal delay may be enabled or disabled.

5 For 10Mbps and 100Mbps, t_{CYC} scales to 400ns ± 40ns and 40ns ± 4ns, respectively.

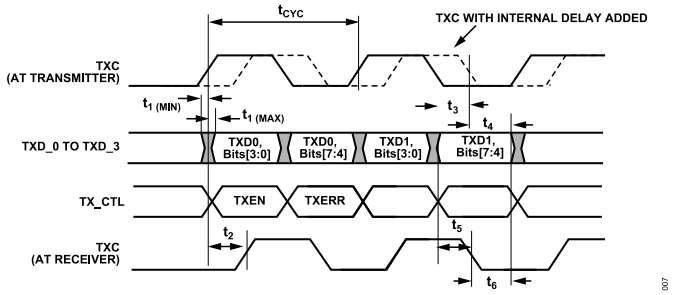


Figure 7. RGMII Transmit Timing

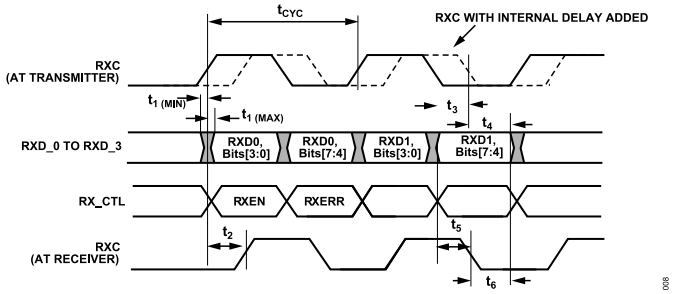


Figure 8. RGMII Receive Timing

RMII Transmit/Receive

Table 10. RMII Timing

Parameter	Description	Min	Typ	Max	Unit
REF_CLK Frequency[1]	Frequency of the REF_CLK		50		MHz
REF_CLK Duty Cycle	Duty Cycle of the REF_CLK	35		65	%
t_1	TXD_0, TXD_1, TX_EN, RXD_0, RXD_1, CRS_DV, RX_ER data setup to REF_CLK rising edge	4			ns

SPECIFICATIONS

Table 10. RMII Timing (Continued)

Parameter	Description	Min	Typ	Max	Unit
t_2	TXD_0, TXD_1, TX_EN, RXD_0, RXD_1, CRS_DV, RX_ER data hold from REF_CLK rising edge	2			ns
t_3	Output rise/fall time	1		5	ns

[1] ADIN1320 offers a mode to run RMII using 5MHz REF_CLK for 10Mbps speed.

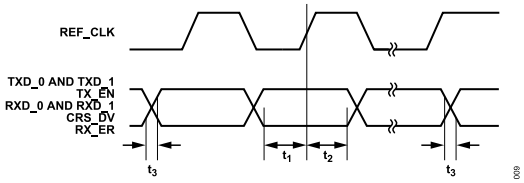


Figure 9. RMII Timing

SGMII Serial Interface Transmit and Receive Timing

Table 11. Serial Interface Transmit and Receive Timing

Parameter	Description	Min	Typ	Max	Unit
	SGMII/1000BASE-KX/LX/SX Signaling Speed		1.25		GBd
	100BASE-FX Signaling Speed		0.125		GBd
t_1	SGMII Rise Time (20% to 80%)			200	ps
	1000BASE-KX Rise Time			320	
t_2	SGMII Fall Time (20% to 80%)			200	ps
	1000BASE-KX Fall Time			320	ps
t_3	S_OUT Output Differential Skew (S_OUT_P vs. S_OUT_N)			20	ps
t_4	S_OUT Total Jitter			0.24	UI
t_5	S_IN Total Jitter tolerated			0.748	UI

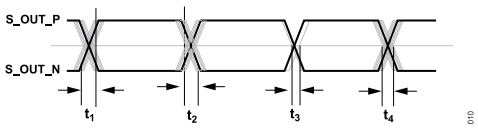


Figure 10. SGMII Transmit Timing

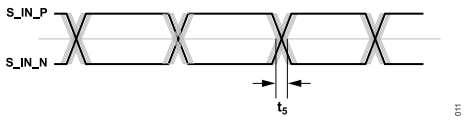


Figure 11. SGMII Receive Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 12.

Parameter	Rating
VDDIO to GND	−0.3V to +3.63V
DVDD_0P9 to GND, DVDD_0P9 to GND	−0.3V to +1.1V
AVDD_3P3 to GND, AVDD_3P3 to GND	−0.3V to +3.63V
MAC Interface to GND	−0.3V to VDDIO + 0.3V
LINK_ST, LED_2/GP_CLK to GND	−0.3V to VDDIO + 0.3V
RESET_N, MACIF_SEL2 to GND	−0.3V to VDDIO + 0.3V
MDIO, MDC, INT_N to GND	−0.3V to VDDIO + 0.3V
MDI_x_x to GND	−0.3V to AVDD_3P3 + 0.3V
S_OUT_x, S_IN_x to GND	−0.1V to DVDD_0P9 + 0.15V
LED_0, LED_1, XTAL_I/CLK_IN/REF_CLK, XTAL_O, CLK25_REF to GND	−0.3V to AVDD_3P3 + 0.3V
Operating Temperature Range (T_A)	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	125°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Lead Temperature	JEDEC industry-standard
Soldering	J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	
MDI_x_x Pins	4kV
All Other Pins	2kV
Field Induced Charged Device Model (FICDM)	1.25kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 13. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-48-29	34[1]	25[2]	°C/W
	31[3]		°C/W

[1] Based on simulated data using a JEDEC 2s2p thermal test board with a 3 × 3 array of thermal vias in a JEDEC natural convection environment. See JEDEC specification JESD-51 for details.

[2] Based on simulated data using a JEDEC 1s0p thermal test board with no thermal vias in a JEDEC natural convection environment. See JEDEC specification JESD-51 for details.

[3] Test Condition 1: thermal impedance measured on Analog Devices, Inc., hardware.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

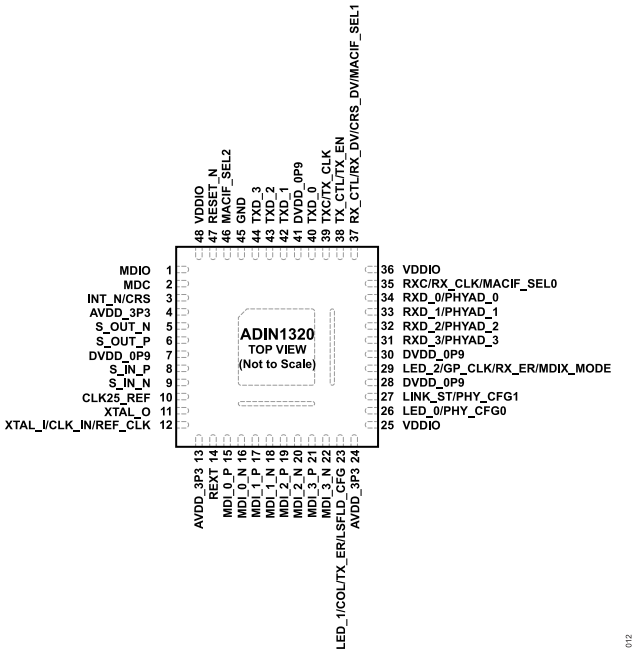


Figure 12. Pin Configuration

Table 14. Pin Function Descriptions

Pin No.	Mnemonic	Supply Domain	Description
Clock Interface			
11	XTAL_O	AVDD_3P3	Second Terminal for Crystal Connection. If using a single-ended reference clock on XTAL_I/CLK_IN/REF_CLK, leave XTAL_O open circuit.
12	XTAL_I/CLK_IN/REF_CLK	AVDD_3P3	Input for Crystal (XTAL_I). Single-Ended 25MHz Reference Clock (CLK_IN). 50MHz RMII Reference Clock Input in RMII Mode (REF_CLK).
Management Interface			
3	INT_N/CRS	VDDIO	Management Interface Interrupt Pin Open-Drain Output (INT_N). Active low output. A low on INT_N indicates an unmasked management interrupt. This pin requires a 1.5kΩ pull-up resistor to VDDIO. MII Carrier Sense Output (CRS). Indicates the presence of a carrier to MAC.
2	MDC	VDDIO	Management Data Clock Input up to 5.5MHz.
1	MDIO	VDDIO	Management Data Open-Drain Input/Output Synchronous to the MDC Clock. This pin requires a 1.5kΩ pull-up resistor to VDDIO.
Reset			
47	RESET_N	VDDIO	Active Low Input. Hold low for >10µs. This pin requires a 1kΩ pull-up resistor to VDDIO.
Media Dependent Interface (MDI)			
15	MDI_0_P	AVDD_3P3	Transmit/Receive Differential Pair 0 Supporting 10Mbps, 100Mbps, and 1Gbps.
16	MDI_0_N	AVDD_3P3	Transmit/Receive Differential Pair 0 Supporting 10Mbps, 100Mbps, and 1Gbps.
17	MDI_1_P	AVDD_3P3	Transmit/Receive Differential Pair 1 Supporting 10Mbps, 100Mbps, and 1Gbps.
18	MDI_1_N	AVDD_3P3	Transmit/Receive Differential Pair 1 Supporting 10Mbps, 100Mbps, and 1Gbps.
19	MDI_2_P	AVDD_3P3	Transmit/Receive Differential Pair 2 for 1000BASE-T Mode. Unused in other modes.
20	MDI_2_N	AVDD_3P3	Transmit/Receive Differential Pair 2 for 1000BASE-T Mode. Unused in other modes.
21	MDI_3_P	AVDD_3P3	Transmit/Receive Differential Pair 3 for 1000BASE-T Mode. Unused in other modes.
22	MDI_3_N	AVDD_3P3	Transmit/Receive Differential Pair 3 for 1000BASE-T Mode. Unused in other modes.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 14. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Supply Domain	Description
SGMII/Fiber			
5	S_OUT_N	DVDD_0P9	SGMII or Fiber Transmit Differential Pair Negative.
6	S_OUT_P	DVDD_0P9	SGMII or Fiber Transmit Differential Pair Positive.
8	S_IN_P	DVDD_0P9	SGMII or Fiber Receive Differential Pair Positive.
9	S_IN_N	DVDD_0P9	SGMII or Fiber Receive Differential Pair Negative.
MAC Interface			
31	RXD_3/PHYAD_3[1]	VDDIO	RGMII/MII Receive Data 3 Output (RXD_3). See the MAC Interface section. PHY Address Hardware Configuration Pin (PHYAD_3).
32	RXD_2/PHYAD_2[1]	VDDIO	RGMII/RMII/MII Receive Data 2 Output (RXD_2). See the MAC Interface section. PHY Address Hardware Configuration Pin (PHYAD_2).
33	RXD_1/PHYAD_1[1]	VDDIO	RGMII/RMII/MII Receive Data 1 Output (RXD_1). See the MAC Interface section. PHY Address Hardware Configuration Pin (PHYAD_1).
34	RXD_0/PHYAD_0[1]	VDDIO	RGMII/RMII/MII Receive Data 0 Output (RXD_0). See the MAC Interface section. PHY Address Hardware Configuration Pin (PHYAD_0).
35	RXC/RX_CLK/ MACIF_SEL0[1]	VDDIO	RGMII Receive Clock Output (RXC). 125MHz at 1Gbps, 25MHz at 100Mbps, 2.5MHz at 10Mbps. MII Receive Clock Output (RX_CLK). 25MHz at 100 Mbps, 2.5MHz at 10Mbps. MAC Interface Selection Hardware Configuration Pin (MACIF_SEL0). See Table 26.
37	RX_CTL/RX_DV/CRS_DV/ MACIF_SEL1[1]	VDDIO	RGMII Receive Control Signal (RX_CTL). This is a combination of the RX_DV and RX_ER signals using both edges of RXC. MII Mode Received Data Valid Output (RX_DV). When asserted high, it indicates that valid data is present on the RXD_0 pin to RXD_3 pin in MII mode. RMII Mode Carrier Sense/Received Data Valid Signal (CRS_DV). This is a combination of the CRS and RX_DV signals and is asserted while the receive medium is nonidle. See the RMII Interface Mode section. MAC Interface Selection Hardware Configuration Pin (MACIF_SEL1). See Table 26.
38	TX_CTL/TX_EN	VDDIO	RGMII Transmit Control Signal (TX_CTL). This is a combination of the TX_EN and TX_ER signals using both edges of TXC. RMII/MII Mode Transmit Enable Input from the MAC to the PHY (TX_EN). This indicates that transmission data is available on the TXD_x lines.
39	TXC/TX_CLK	VDDIO	RGMII Transmit Clock Input (TXC). 125MHz at 1Gbps, 25MHz at 100Mbps, 2.5MHz at 10Mbps from MAC to PHY. MII Output Clock from PHY to MAC (TX_CLK). The TX_CLK frequency is 2.5MHz in 10BASE-T mode and 25MHz in 100BASE-TX mode. TX_CLK has a constant phase relationship to the XTAL_I/CLK_IN clock.
40	TXD_0	VDDIO	RGMII/RMII/MII Transmit Data 0 Input. See the MAC Interface section.
42	TXD_1	VDDIO	RGMII/RMII/MII Transmit Data 1 Input. See the MAC Interface section.
43	TXD_2	VDDIO	RGMII/RMII/MII Transmit Data 2 Input. See the MAC Interface section.
44	TXD_3	VDDIO	RGMII/RMII/MII Transmit Data 3 Input. See the MAC Interface section.
LED Interface			
23	LED_1/COL/TX_ER/ LSFLD_CFG[1]	AVDD_3P3	Programmable LED Indicator for General-Purpose LED with 8mA Drive Capability (LED_1). The LED can be active high or active low. Recommended use is active low. The ADIN1320 automatically senses the connection of the LED during power-up and reset. By default, LED_1 is on when a 1Gb link is established (this behavior can be changed by software). MII Collision Detect Output (COL). This indicates a collision condition. MII Transmit Error Detected Input from the MAC to the PHY (TX_ER). Only available by default when EEE advertisement is enabled using the hardware pin configuration (see Table 27). 4-Level Hardware Configuration Pin for LSFLD (LSFLD_CFG).
26	LED_0/PHY_CFG0[1]	AVDD_3P3	Programmable LED Indicator for General-Purpose LED with 8mA Drive Capability (LED_0). The LED can be active high or active low. Recommended use is active low. The ADIN1320 automatically senses the connection of the LED during power-up and reset. By default, LED_0 is

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 14. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Supply Domain	Description
			on when a link is established and blinking when there is activity (this behavior can be changed by software).
			4-Level Hardware Configuration Pin for PHY Configuration (PHY_CFG0) (see Table 27).
29	LED_2/GP_CLK/RX_ER/ MDIX_MODE[1]	VDDIO	Programmable LED Indicator for General-Purpose LED with 4mA Drive Capability (LED_2). The LED can be active high or active low. Recommended use is active low. The ADIN1320 automatically senses the connection of the LED during power-up and reset. By default, LED_2 is on when a 100Mb link is established (this behavior can be changed by software).
			General-Purpose Output on which PHY Clocks can be Made Available (GP_CLK).
			RMII/MII Mode Receive Error Detected Output (RX_ER). When asserted high, it indicates that the PHY has detected a receive error.
			4-Level Hardware Configuration Pin for Auto-MDIX Configuration (MDIX_MODE)
Other Pins			
10	CLK25_REF	AVDD_3P3	Analog Reference Clock Output. The 25MHz, 3.3V reference clock from the crystal oscillator is available on the CLK25_REF pin.
14	REXT	AVDD_3P3	External Bias Reference Resistor. Connect a 1% 3.01 kΩ resistor (1% tolerance, 100ppm/ºC temperature coefficient (TC)) to GND.
27	LINK_ST/PHY_CFG1[1]	VDDIO	General-Purpose Output Used to Output Link Status (LINK_ST). This indicates whether a valid link has been established.
			4-Level Hardware Configuration Pin for PHY Configuration (PHY_CFG1) (see Table 27).
45	GND		Connect this pin to GND.
46	MACIF_SEL2	VDDIO	MAC Interface Selection Hardware Configuration Pin (MACIF_SEL2). See Table 26.
Power and Ground Pins			
4, 13, 24	AVDD_3P3		3.3V Power Supply Input for the PHY Interface, Analog Circuitry, Crystal Oscillator, DLL, CLK25_REF Generation, LED Circuitry, and Serdes Subsystem. Connect 0.1µF and 0.01µF capacitors to GND as close as possible to these pins.
7, 28, 30, 41	DVDD_0P9		0.9V Digital Core Power Supply Input. Connect 0.1µF and 0.01µF capacitors to GND as close as possible to these pins
25, 36, 48	VDDIO		3.3V/2.5V/1.8V MDIO and MAC Interface Power Supply Input. Connect 0.1µF and 0.01µF capacitors to GND as close as possible to these pins. If using 3.3V, to minimize power supplies, VDDIO and AVDD_3P3 can be connected to the same supply.
	EP		Exposed Pad. This must be connected to GND on the board. The LFCSP package has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to GND. A 4 × 4 array of thermal vias beneath the exposed GND pad is also required.

[1] In cases where a pin is shared between a functional signal(s) and a hardware pin configuration signal(s), the hardware pin configuration signal(s) is the last name in the mnenomic and the pin is referred to using the functional signal(s) name throughout the data sheet.

Table 15. Pin Function Descriptions for Each MAC Interface Option

		MAC Interface Pin Function[2]			
Pin No.	Mnemonic[1]	RGMII	MII and EEE Advertisement Disabled[3]	MII and EEE Advertisement Enabled [3, 4]	RMII
3	INT_N[5]/CRS		CRS		
12	XTAL_I/CLK_IN/REF_CLK				REF_CLK[6, 8]
23	LED_1[5]/COL/TX_ER/LSFLD_CFG		COL	TX_ER[7]	
29	LED_2/GP_CLK[5]/RX_ER/ MDIX_MODE		RX_ER	RX_ER	RX_ER
31	RXD_3/PHYAD_3	RXD_3	RXD_3	RXD_3	
32	RXD_2/PHYAD_2	RXD_2	RXD_2	RXD_2	
33	RXD_1/PHYAD_1	RXD_1	RXD_1	RXD_1	RXD_1
34	RXD_0/PHYAD_0	RXD_0	RXD_0	RXD_0	RXD_0
35	RXC/RX_CLK/MACIF_SEL0	RXC	RX_CLK	RX_CLK	

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 15. Pin Function Descriptions for Each MAC Interface Option (Continued)

		MAC Interface Pin Function[2]			
Pin No.	Mnemonic[1]	RGMII	MII and EEE Advertisement Disabled[3]	MII and EEE Advertisement Enabled [3, 4]	RMII
37	RX_CTL/RX_DV/CRS_DV/ MACIF_SEL1	RX_CTL	RX_DV	RX_DV	CRS_DV
38	TX_CTL/TX_EN	TX_CTL	TX_EN	TX_EN	TX_EN
39	TXC/TX_CLK	TXC	TX_CLK	TX_CLK	REF_CLK[8] Output
40	TXD_0	TXD_0	TXD_0	TXD_0	TXD_0
42	TXD_1	TXD_1	TXD_1	TXD_1	TXD_1
43	TXD_2	TXD_2	TXD_2	TXD_2	
44	TXD_3	TXD_3	TXD_3	TXD_3	

1 Hardware pin configuration signal(s) have been omitted for clarity.

2 Wherever the field is left blank, the pin function is the first function listed in the Mnemonic column.

3 EEE advertisement enabled/disabled using the hardware pin configuration. See the Hardware Configuration Pins section.

4 EEE does not support half duplex. Therefore, no CRS pin or COL pin is required.

5 These pin functions can also be reconfigured via software.

6 A 50MHz reference clock must be supplied on the XTAL_I/CLK_IN/REF_CLK pin when using the RMII MAC interface option.

7 Because TX_ER shares a pin with COL, this pin is grouped with the PHY output pins, even though TX_ER is actually a PHY input pin.

8 ADIN1320 offers a mode to run RMII using 5MHz clock for 10Mbps speed. In this mode, TXC/TX_CLK will output 5MHz reference clock which should be connected to MAC Interface's REF_CLK pin. A 25MHz clock must be supplied to ADIN1320 CLK_IN pin when using 5MHz RMII.

TYPICAL PERFORMANCE CHARACTERISTICS

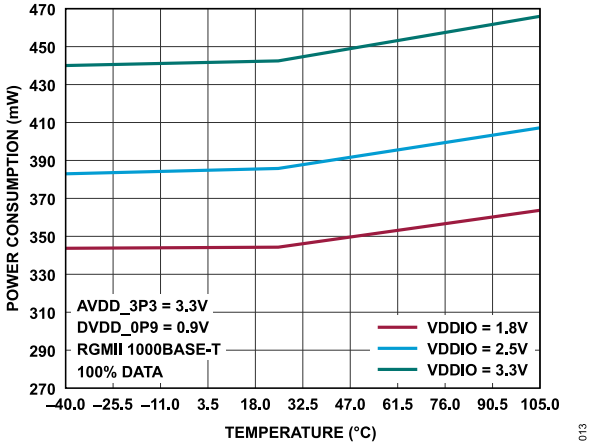


Figure 13. Power Consumption vs. Temperature, VDDIO Supply, RGMII 1000BASE-T, 100% Data

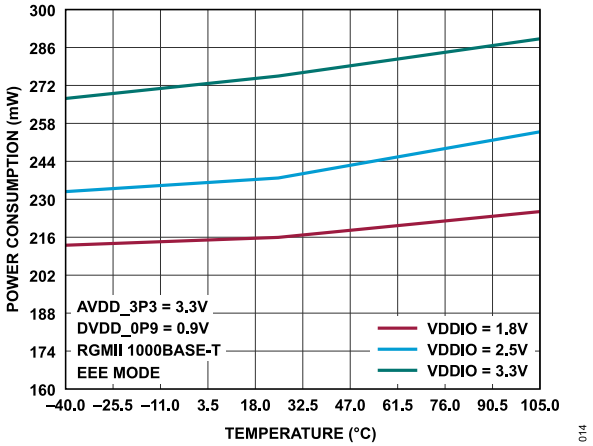


Figure 14. Power Consumption vs. Temperature, VDDIO Supply, RGMII 1000BASE-T, EEE Mode

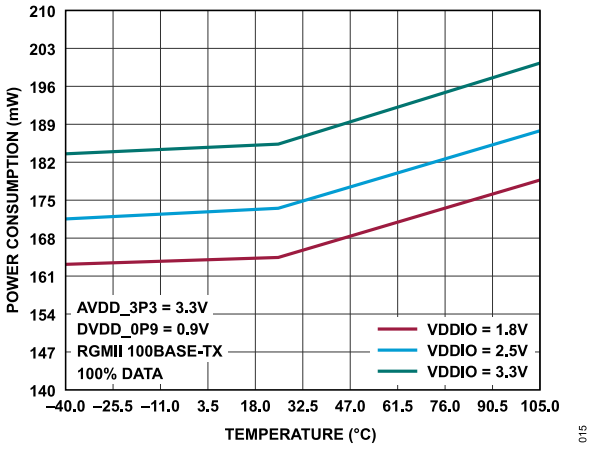


Figure 15. Power Consumption vs. Temperature, VDDIO Supply, RGMII 100BASE-TX, 100% Data

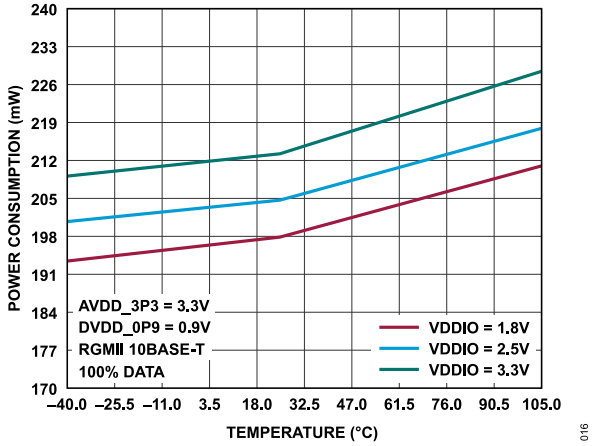


Figure 16. Power Consumption vs. Temperature, VDDIO Supply, RGMII 10BASE-T, 100% Data

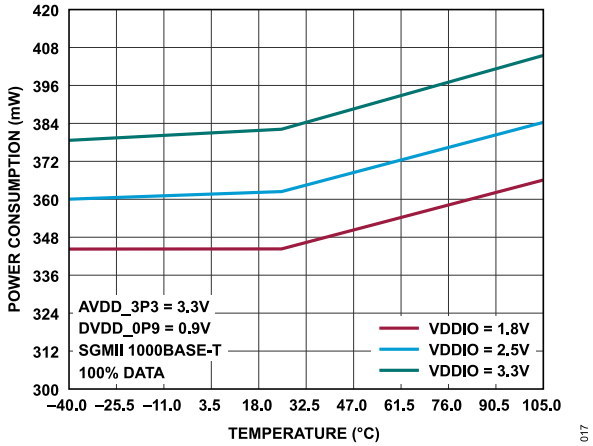


Figure 17. Power Consumption vs. Temperature, VDDIO Supply, SGMII 1000BASE-T, 100% Data

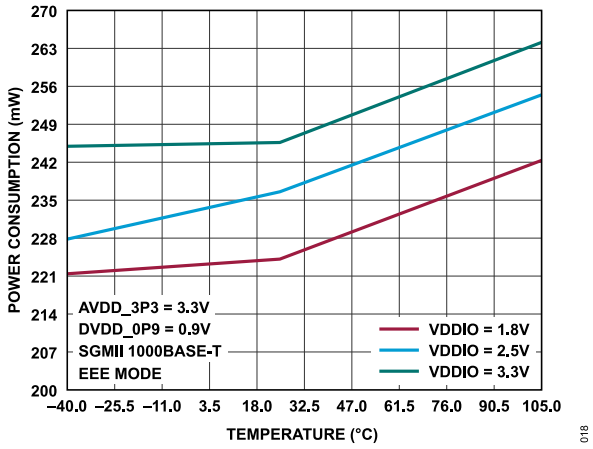


Figure 18. Power Consumption vs. Temperature, VDDIO Supply, SGMII 1000BASE-T, EEE Mode

TYPICAL PERFORMANCE CHARACTERISTICS

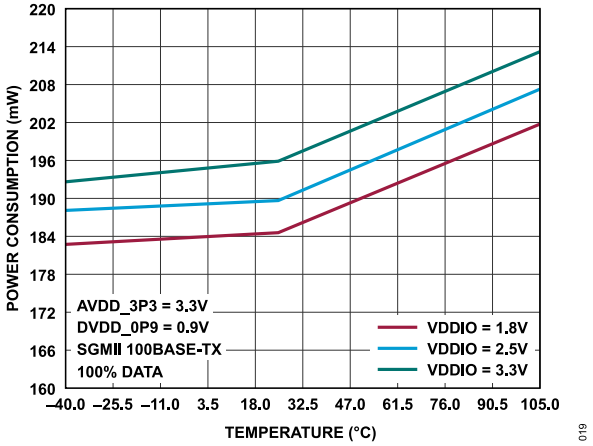


Figure 19. Power Consumption vs. Temperature, VDDIO Supply, SGMII 100BASE-TX, 100% Data

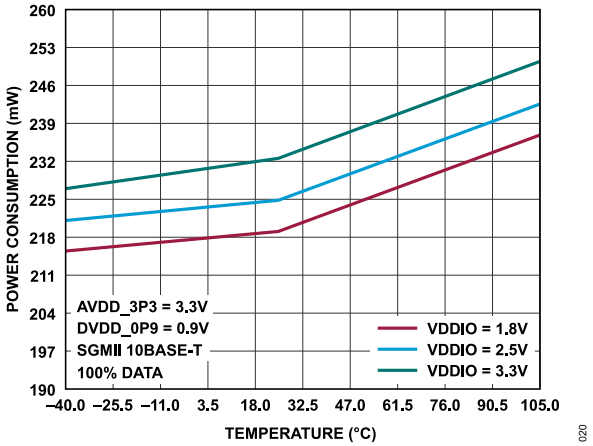


Figure 20. Power Consumption vs. Temperature, VDDIO Supply, SGMII 10BASE-T, 100% Data

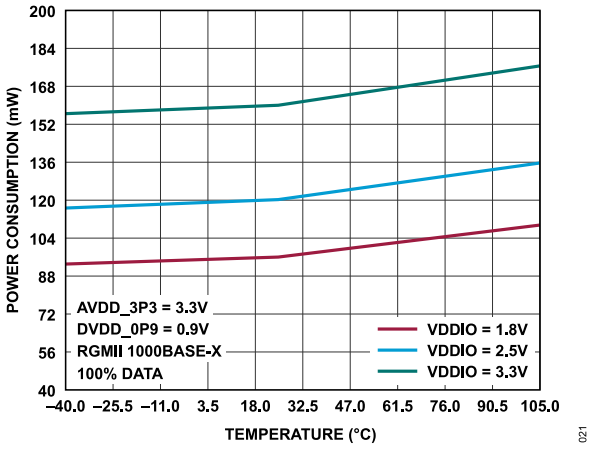


Figure 21. Power Consumption vs. Temperature, VDDIO Supply, RGMII 1000BASE-X, 100% Data

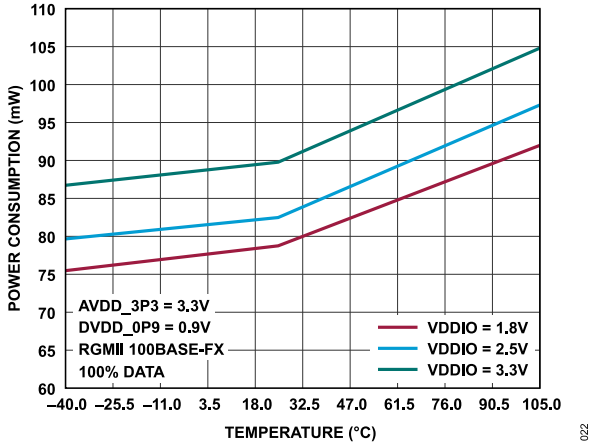


Figure 22. Power Consumption vs. Temperature, VDDIO Supply, RGMII 100BASE-FX, 100% Data

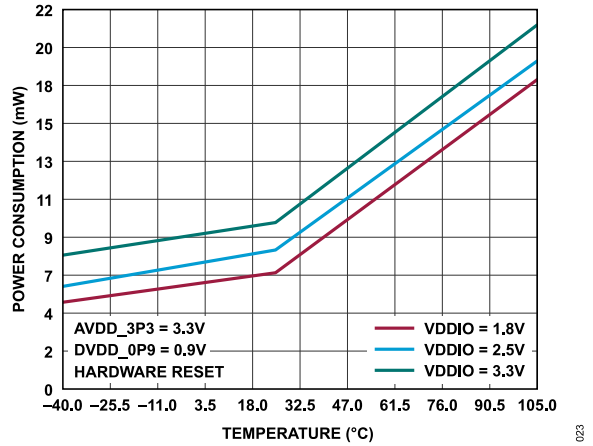


Figure 23. Power Consumption vs. Temperature, VDDIO Supply, Hardware Reset

THEORY OF OPERATION

OVERVIEW

The ADIN1320 is a low-power, single port Gigabit Ethernet transceiver, offering robust support for copper and fiber or backplane media. Primarily designed for industrial Ethernet applications, the ADIN1320 integrates an EEE Copper PHY core and a SerDes Subsystem for high performance data transmission. It also includes all necessary common analog circuitry, input/output clock buffering, management interfaces, subsystem registers, and Media Access Control (MAC) interface control logic to manage reset, clock control, and hardware pin configuration.

For copper connections, the ADIN1320 interfaces directly with twisted pair cables via an external transformer, and supports MAC-side connectivity through Serial Gigabit Media Independent Interface (SGMII), RGMII, RMII, or MII, depending on system requirements. MII, depending on system requirements.. It supports cable lengths of up to 150 meters at Gigabit speeds and extends to 180 meters when operating at 100Mbps or 10Mbps. When operating at 10Mbps, the device defaults to 10BASE-T mode, using 10BASE-T transmit levels. However, it can be configured via software (by setting the B_10_E_EN bit in the Base 10e Enable Register) to operate in 10BASE-Te mode with lower transmit levels. The only distinction between 10BASE-Te and 10BASE-T is the transmit level, and a PHY configured in 10BASE-Te mode is fully interoperable with a 10BASE-T PHY when using standard Cat-5 cables.

In addition to copper media support, the SerDes Subsystem allows the ADIN1320 to interface with fiber optic transceivers, connect to backplanes via the 1000BASE-KX standard, or interface with a MAC layer through the SGMII. The ADIN1320 also provides support for RGMII, RMII, and MII MAC interfaces, offering flexible connectivity options for a wide range of MAC and PHY configurations.

The ADIN1320 also supports automedia detect configurations in which the it can automatically monitor both media and select the active path based on link availability. The ADIN1320 can operate as a copper to fiber media converter, providing transparent layer-1 conversion between twisted pair cabling and optical modules. It also supports an SGMII to RGMII bridging mode, allowing the ADIN1320 to serve as a MAC interface translator when the physical layer is not in use.

The ADIN1320 further enhances usability with a suite of diagnostic features, enabling users to monitor link quality both during operation and when the link is down. Additionally, it includes a wake on LAN feature, allowing the controller or MAC to enter a low-power sleep state when no network activity is detected.

The Figure 24 shows a simplified overview of the main channel blocks.

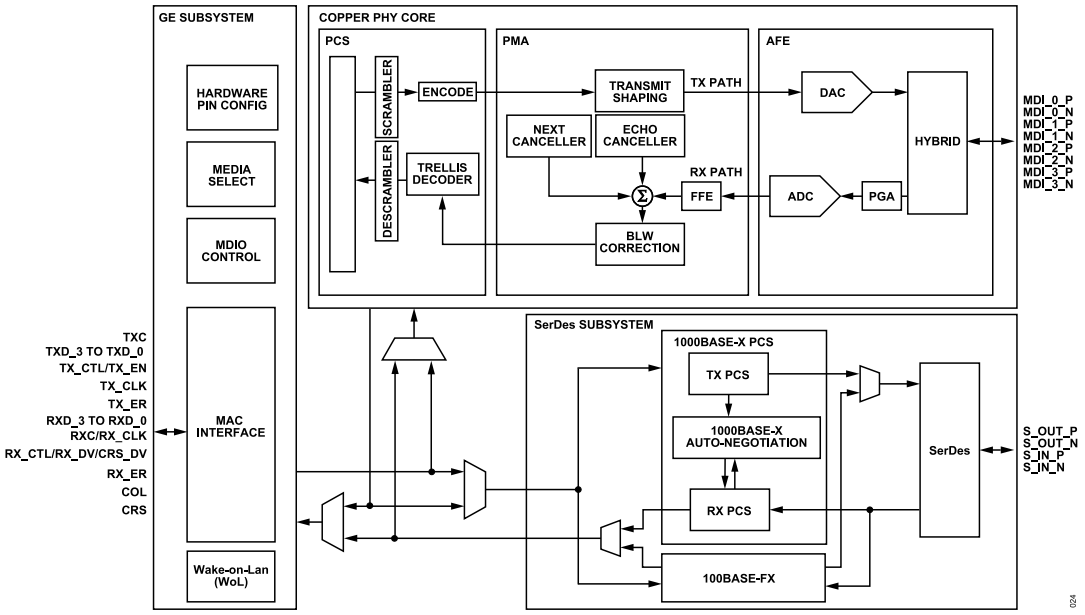


Figure 24. Simplified Channel Block Diagram

THEORY OF OPERATION

ANALOG FRONT END (AFE)

The AFE stage consists of a hybrid stage, a programmable gain amplifier (PGA), and an analog-to-digital convertor (ADC). The function of the hybrid stage is to remove the transmitted signal from the input signal, thereby allowing full duplex operation on the twisted pair. The PGA stage scales the incoming signal before it reaches the ADC. The gain stage is controlled and adjusted based on the output of the ADC to ensure the signal applied to the ADC is maximized but within range of the ADC.

Physical Media Attachment (PMA)

The PMA block consists of the feed forward equalizer (FFE) stage, which removes intersymbol interference (ISI).

The twisted pairs of Ethernet cables are not internally shielded from each other, so signals transmitted on one pair couple across to the other pairs. When a transmitter does not match to the line due to mismatches or cable connectors, reflections are observed as an echo. The echo and crosstalk estimates are subtracted from the equalizer output.

Baseline wander is an artifact of the external transformer that attenuates at low frequencies. When there are many symbols with the same sign transmitted consecutively, the signal at the receiver reduces. The baseline wander block monitors and corrects to ensure the likelihood of receiving a symbol error is reduced.

WAKE ON LAN (WOL)

The ADIN1320 features a WoL function capable of detecting a magic packet and generating a wake signal. If configured, this wake signal can be output on a dedicated pin and/or trigger an interrupt. The WoL interrupt can be enabled via the GE_WOL_WAKE_IRQ_EN bit in GE subsystem interrupt enable register (0xFF1D). The wake signal alerts station management software, typically running on an external processor. Upon receiving the wake signal, the station management software can wake up connected devices, such as the MAC, from a low-power mode.

The WoL functionality is enabled by setting the GE_WOL_EN bit in the GE subsystem WoL enable register (0xFF79). When WoL is enabled, a change in the link status in the PHY that is being monitored normally results in a wake event. This behavior can be modified using the GE_WOL_LS_CHG_WAKE_EN bit in GE subsystem WoL wake control register (0xFF7A).

By default, when both copper (Cu) and fiber PHYs are active, WoL monitors packets on the Cu PHY. However, the detection of magic packets from the fiber PHY can be enabled by setting the GE_WOL_2_PHY_SD_SEL bit in the GE subsystem WoL system sontrol register (0xFF78). Note that WoL can monitor only one PHY (either Cu or fiber) at a time.

A magic packet consists of six consecutive 0xFF bytes followed by 16 repetitions of the target MAC address. Optionally, it can also include a SecureOn password (refer to Figure 25). The WoL magic packet filter is configured via the GE subsystem magic packet control register (0xFF80). The destination MAC address and SecureOn key can be programmed using the GE subsystem WoL station 0 address (0xFF7C, 0xFF7D, & 0xFF7E) and GE subsystem SecureOn key register (0xFF81, 0xFF82, & 0xFF83) registers, respectively.

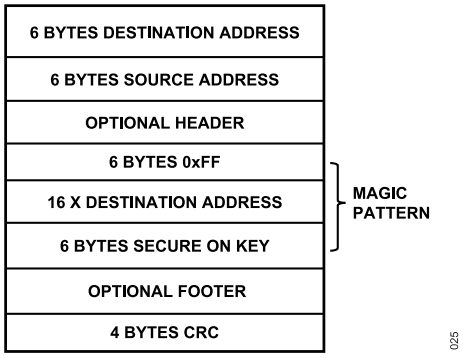


Figure 25. Magic Packet Structure

By default, the WoL wake signal is set to active high and level-sensitive. However, this can be modified to active low by enabling the GE_WOL_WAKE_INV_EN bit in the GE subsystem WoL system control register (0xFF78). Additionally, the GE subsystem WoL signal control register (0xFF7B) allows for configuring the WoL wake output as pulses instead of level-sensitive signals.

The WoL wake signal can be routed to various output pins, including INT_N, LED_0, LED_1, LED_2, or LINK_ST/LED_3, via their respective pin override control registers. The cause of the WoL wake event can be determined by reading the GE subsystem WoL status register (0xFF85).

The GE subsystem interrupt status register (0xFF1E) also contains a dedicated bit to indicate when a WoL wake event has occurred, regardless of whether interrupts are enabled. This allows for independent monitoring of WoL events through the interrupt system.

COPPER ETHERNET

The ADIN1320 supports operation as a copper Ethernet PHY, providing 10BASE-T, 100BASE-TX, and 1000BASE-T connectivity through an external transformer connected to twisted pair cabling. In this mode, the device offers full flexibility on the MAC-side interface, supporting SGMII, RGMII, RMII, or MII depending on system requirements. This allows the ADIN1320 to interface seamlessly with a wide range of host architectures while maintaining optimized copper mode performance. Figure 26 illustrates the primary functional blocks involved in copper Ethernet operation.

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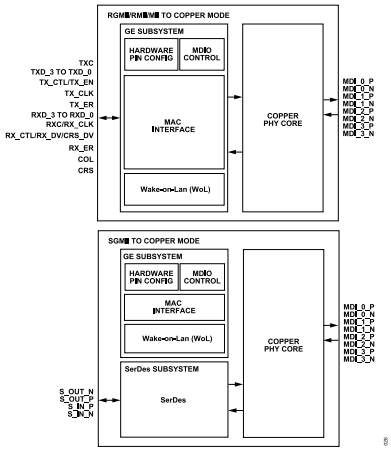


Figure 26. ADIN1320 in SGMII/RGMII/RMII/MII to Copper Mode

1000BASE-T Mode

In 1000BASE-T Transmit mode, the Copper PHY core encodes 8-bit data for transmission by the PMA as a 4D five-level pulse amplitude modulation (PAM) signal over the four pairs of cable.

In 1000BASE-T Receive mode, the PMA decodes the incoming 4D PAM signals into 8-bit data. After performing compensation and after additional cleanup, the PMA outputs the data to the receive pins of the MAC interface.

100BASE-TX Mode

For the 100BASE-TX transmit mode, the 4-bit data is first encoded into a 5-bit serial bit stream running at 125Mbps. This is then sent to the scrambler where it is encoded to a three-level multilevel transmit (MLT3) format for transmission by the PMA.

The PMA decodes the incoming 3-level MLT3 sequence into 4-bit data after descrambling and 5-bit to 4-bit decoding in 100BASE-TX receive mode.

10BASE-T Mode

For the 10BASE-T mode, the PHY transmits and receives Manchester-encoded data.

SERDES/FIBER ETHERNET

The ADIN1320 supports fiber and backplane Ethernet operation through its integrated SerDes subsystem, enabling 100BASE-FX, 1000BASE-X, and 1000BASE-KX modes depending on the attached media, with MAC-side connectivity provided through RGMII, RMII, or MII. In fiber mode, the device implements 100BASE-FX and 1000BASE-X using the SerDes S_OUT_x and S_IN_x pins, which interface directly with an external optical transceiver or SFP cage. In this data sheet, 1000BASE-X refers specifically to the 1000BASE-SX/LX fiber protocol. The same SerDes pins also support 1000BASE-KX backplane operation, offering a robust, low latency serialized interface optimized for controlled impedance PCB backplane channels.

When the SerDes data path is active, the ADIN1320 uses its high integrity serialization engine to provide reliable operation in electrically noisy environments, long reach optical applications, and embedded backplane systems. Figure 27 illustrates the primary functional blocks involved in SerDes and fiber/backplane Ethernet operation.

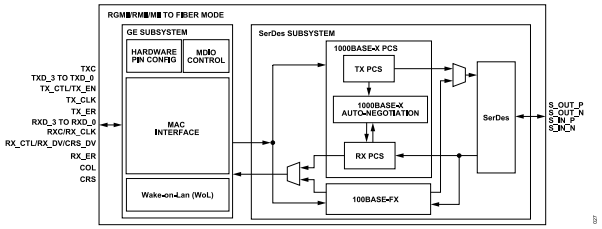


Figure 27. ADIN1320 in RGMII/RMII/MII to Fiber Mode

1000BASE-X Mode

In 1000BASE-X mode, the ADIN1320 uses two differential pair to interface with fiber via SFP. The 8-bit data is first encoded into a 10-bit serial bit stream running at 1.25Gbps. This is then encoded to nonreturn-to-zero (NRZ) format for transmission.

100BASE-FX Mode

In 100BASE-FX mode, the ADIN1320 uses two differential pair to interface with fiber via SFP. The 4-bit data is first encoded into a 5-bit serial bit stream running at 125Mbps. This is then encoded to nonreturn-to-zero inverted (NRZ-I) format for transmission.

1000BASE-KX, Backplane

When operating in backplane mode, the ADIN1320 uses two differential pairs to facilitate 1Gbps Ethernet over an electrical backplane with a maximum length of 1 meter. The Clause 37 auto negotiation feature can be enabled in backplane mode via hardware strapping by adjusting the LED_1 pin configuration (refer to Table 31 and Table 28). Alternatively, the auto negotiation feature can be enabled through software by setting the SD_AUTONEG_EN_CFG bit in the SerDes subsystem advertisement configuration register (0xFF53).

COPPER OR FIBER AUTOMEDIA DETECT

The ADIN1320 supports an automatic media detection mode that enables both the copper PHY and the SerDes-based Fiber/Backplane interface to operate concurrently. In this mode, the device continuously monitors each interface for valid link activity or autonegotiation signaling. When a link is detected on either copper or fiber first, the ADIN1320 automatically selects that interface as the active media path and begins forwarding data through the corresponding MAC interface. The nonselected media enters a low-power idle state to reduce power consumption.

If activity on the active media ceases, the device resumes monitoring both interfaces. Should the other media subsequently present valid signaling, the ADIN1320 switches to that interface and makes it the new active data path. This autonomous arbitration enables seamless copper or fiber operation and media flexibility in field

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environments. Figure 24 illustrates the functional blocks used in automatic media detection.

COPPER TO FIBER MEDIA CONVERTER

The ADIN1320 can operate as a transparent copper to fiber media converter, enabling Layer-1 translation between 100BASE-TX and 100BASE-FX, or between 1000BASE-T and 1000BASE-X, with the same link speed maintained on both sides. Figure 28 illustrates the blocks associated with copper to fiber media conversion.

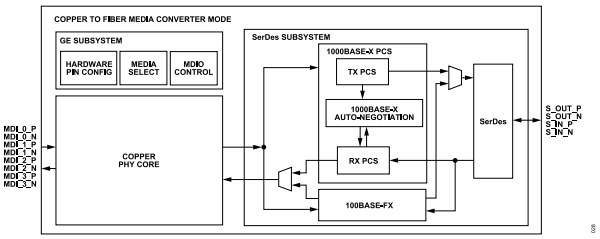


Figure 28. ADIN1320 in Copper-Fiber Media Converter Mode

AUTONEGOTIATION

The ADIN1320 includes autonegotiation capability in accordance with IEEE 802.3 Clause 28 (for copper) and 37 (for fiber and backplane), providing a mechanism for exchanging information between PHYs to allow link partners to agree to a common mode of operation at the highest supported speed. During the autonegotiation process, the PHYs advertise their capabilities and compare them to those received from the link partner. The concluded operating mode is the highest speed capability and duplex setting common across the two devices.

In the event of the link being dropped, the autonegotiation process restarts automatically.

Autonegotiation can be restarted by request through a write to the RESTART_ANEG bit in the MII Control register (0x0000) when using copper media, or through SD_RESTART_ANEG in SD_SerDes control register (0x0000) when using fiber or backplane media.

The autonegotiation process takes some time to complete, depending on the number of pages exchanged. Clauses 28 and 37 of the IEEE 802.3 standard details the timers related to autonegotiation.

Leader/Follower Resolution

For 1000BASE-T links, autonegotiation is also used to resolve leader or follower status. The PHY can be configured to prefer leader or follower through the hardware configuration or manually configured for fixed leader or follower through the leader follower control register (0x0009), Bit 11, and Bit 12 (MAN_MSTR_ADV bit and MAN_MSTR_SLV_EN_ADV bit, respectively). If the user chooses to manually fix this configuration, they must configure each side of the link differently.

Polarity Inversion Correction

The ADIN1320 is capable of detecting if the proper polarity is present on the copper media and adjust the polarity if not. If polarity inversion has been detected, it is identified in the PHY Status 1 register (0x001A).

Automatic MDI Crossover

The ADIN1320 is capable of distinguishing if a straight or crossover copper cable is connected between the link partners. The ADIN1320 automatically detects and sets the MDI configuration to match its receiver to that of the remote transmitter, thereby avoiding need for crossover copper cables or cross-wired copper cables. Details on the automatic MDI/MDIX process is included in Clause 40, Section 40.8.2. This feature is configured through the hardware strapping configuration (see Table 30) or, alternatively, can be changed through software access by writing to PHY Control 1 register (0x0012) via the MDIO interface.

AUTONEGOTIATION DISABLED

Autonegotiation is always used for a 1000BASE-T link, as required by the IEEE standards. 10BASE-T or 100BASE-TX can use or disable auto-negotiation. When autonegotiation is disabled, the PHY is configured for a single speed and the user must ensure that both sides of the link are configured properly. See Table 27 and Table 29 for details on hardware configuration with autonegotiation enabled or disabled.

The 1000BASE-X is always in full duplex with autonegotiation enabled when selected. Autonegotiation can be disabled in 1000BASE-X by clearing SD_AN_EN in SD_CONTROL Register (address 0x0000). Autonegotiation is not supported in 100BASE-FX.

When using the ADIN1320 in RGMII to 1000BASE-KX mode, the Clause 37 autonegotiation can be enabled or disabled via LED_1/LSFLD_CFG hardware configuration pin during reset operation according to Table 31 .

If the ADIN1320 has autonegotiation enabled and the other side of the link has autonegotiation disabled, the ADIN1320 detects this and parallel detects, as per the IEEE standard, and attempts to bring up a link at the speed the remote PHY is configured to.

MAC INTERFACE

The ADIN1320 provides the option of RGMII, MII, RMII, or SGMII MAC interface. The MAC interface is selected using hardware configuration pins (see Table 26).

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RGMII Interface Mode

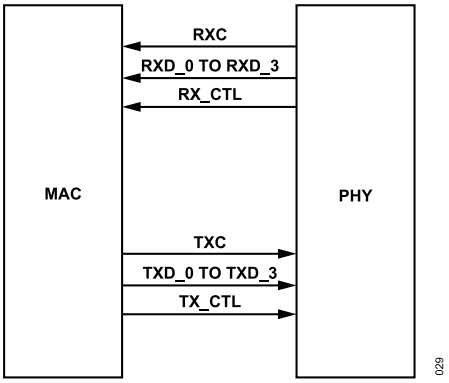


Figure 29. RGMII MAC-PHY Interface Signals

The RGMII interface is capable of supporting data rates of 1Gbps, 100Mbps, and 10Mbps. For the receive interface, the ADIN1320 generates a 125MHz, 25MHz, or 2.5MHz RXC signal to synchronize the RXD_x pin receive data in 1000BASE-T, 100BASE-TX, or 10BASE-T modes, respectively. The RX_CTL is a combination of the RX_DV and RX_ER signals (as described in the MII Interface Mode section) using both edges of the RXC signal. The ADIN1320 transmits the RX_DV signal on the positive edge of RXC and a combination (XOR function) of RX_DV and RX_ER on the negative edge of RXC.

For the transmit interface, when operating in 1000BASE-T mode, the MAC drives TXC with a 125MHz clock signal. The MAC transmits the TXD_x pin data, Bits[3:0] on the positive edge of TXC, and TXD_x pin data, Bits[7:4] on the negative edge of TXC. In 100BASE-TX and 10BASE-T modes, TXC is at 25MHz and 2.5MHz, respectively, and the MAC transmits the TXD_x pin data, Bits[3:0] on the rising edges of TXC (but in accordance with the RGMII standard, the data may be duplicated on the falling edge of the appropriate clock). TX_CTL is a combination of the TX_EN and TX_ER signals using both edges of TXC. TX_EN is transmitted on the positive edge of TXC, and TX_EN XOR TX_ER is transmitted on the negative edge of TXC.

Due to the fact that data is transmitted on both edges of the clock, an accurate delay requirement of 2ns is required on both clock edges (see Figure 30) to ensure that the delayed clock is at the center of the data window, ensuring accurate data capture.

It is possible to enable this 2ns delay on RXC only or on both RXC and TXC using hardware pin configuration settings (see Table 26). These delays can also be configured in software (see GE_RGMII_CFG register). In Figure 30, the 8ns period refers to 1000BASE-T operation, which is 40ns or 400ns in the case of 100BASE-TX and 10BASE-T, respectively. The 2ns delay is valid for 10BASE-T, 100BASE-TX, and 1000BASE-T. The RGMII interface operates at 10Mbps and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data may be duplicated on the falling edge of the appropriate clock. Figure 31 shows similar timing for 100BASE-TX.

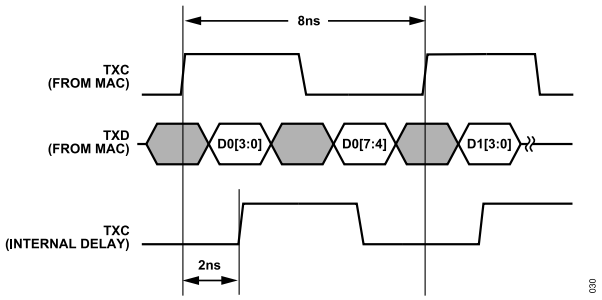


Figure 30. DLL Waveform (1000BASE-T)

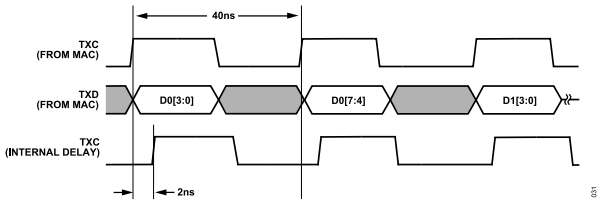


Figure 31. DLL Waveform (100BASE-TX)

MII Interface Mode

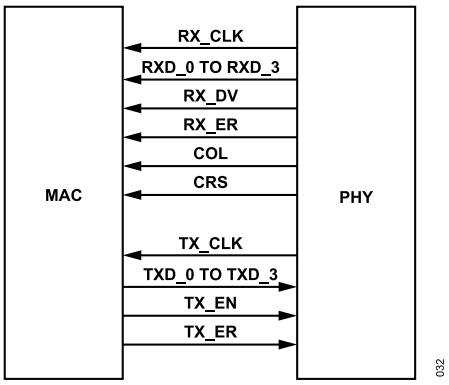


Figure 32. MII MAC to PHY Interface Signals

The MII interface is capable of supporting data rates of 100Mbps and 10Mbps. For the receive interface, the ADIN1320 generates a 25MHz or 2.5MHz RX_CLK signal to synchronize the RXD_x pin receive data in 100BASE-TX or 10BASE-T modes, respectively. RX_DV indicates to the MAC that there is valid data present on the RXD_x receive pin. RX_ER is driven high by the ADIN1320 if an error is detected in the frame that was received from the MDI interface and is being transmitted to the MAC, or during a false carrier event (in 100BASE-TX mode). The CRS pin indicates the presence of a carrier to the MAC, while the COL pin is asserted in a collision condition.

For the transmit interface, the PHY generates a 25MHz or 2.5MHz reference clock on TX_CLK. The MAC transmits data on the TXD_x transmit pin that is synchronized with TX_CLK. The MAC asserts the TX_EN pin to indicate to the ADIN1320 that transmission data is available on the TXD_x transmit data lines. Because the TX_ER pin is not used in 10BASE-T mode, and it is only used in 100BASE-TX mode for forward error propagation and for EEE low

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power idle (LPI) request, TX_ER is only supported when EEE is enabled via the hardware configuration pins (see Table 15).

RMII Interface Mode

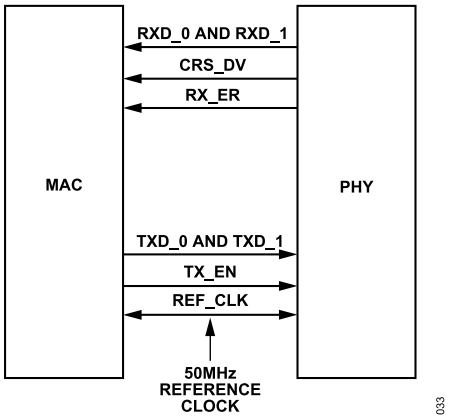


Figure 33. RMII MAC-PHY Interface Signals

This interface is capable of supporting 10Mbps and 100Mbps data rates. A single 50MHz reference clock (REF_CLK) is sourced from the MAC to PHY (or from an external source) to the XTAL_I/CLK_IN/REF_CLK pin for both the transmit and receive interfaces.

The receive data (RXD_0 pin and RXD_1 pin), transitions synchronously to the reference clock (REF_CLK). The carrier sense/received data valid signal (CRS_DV) is a combination of the CRS and RX_DV signals and is asserted while the receive medium is nonidle. The CRS_DV is asserted asynchronously to REF_CLK and deasserted synchronously. RX_ER is also synchronous to REF_CLK, and is asserted when an error is detected in the received frame or when a false carrier is detected in 100BASE-TX. RX_ER assertion on a false carrier can be disabled by software.

The MAC transmits the TXD_0 pin and TXD_1 pin synchronously to REF_CLK, and asserts TX_EN to indicate to the ADIN1320 that transmission data is available on the TXD_0 pin and TXD_1 pin lines.

The ADIN1320 can be configured to function in RMII to 10BASE-T mode using 5MHz reference clock. This mode does not require 50MHz reference clock, uses less pin compared to RGMII, and provides better isolation. In this mode, the ADIN1320 outputs 5MHz clock through TX_CLK pin which must be connected to REF_CLK pin of the MAC. Note that a 25MHz clock should be provided to CLK_IN pin of the ADIN1320.

SGMII Interface Mode

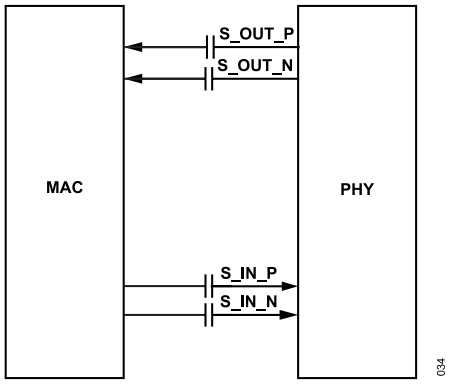


Figure 34. SGMII MAC-PHY Interface Signals

The serial Gigabit media independent interface (SGMII) is a serial interface using two differential pairs to transfer information between the ADIN1320 and a MAC, using less pins and requiring less routing and traces compared to RMII and RGMII interfaces. It transmits at 1.25Gbps and requires external AC coupling with 0.1µF capacitors. The interface is capable of 10Mbps, 100Mbps, 1Gbps full duplex communication with autonegotiation or forced modes.

SGMII-RGMII Bridge Mode

The ADIN1320 supports an interface bridge mode that enables low-latency data translation between SGMII and RGMII MAC interfaces. In this mode, the device operates solely as an interface bridge rather than as an active copper or fiber PHY, providing a compact and efficient means of interconnecting systems that use different MAC interface standards.

During SGMII–RGMII bridging, the ADIN1320 uses standard in band signaling to exchange link information such as speed and duplex between the two interfaces. This link information is used to align both sides of the bridge so that the active interface operates with the correct link parameters. The RGMII clocking automatically follows the negotiated link rate conveyed through the in band signaling mechanism, ensuring proper timing alignment between the serial and parallel domains.

This mode allows an Ethernet MAC using SGMII to interoperate seamlessly with a device using RGMII, or vice versa, without requiring additional external components. Figure 35 illustrates the principal functional blocks used in SGMII–RGMII bridging operation.

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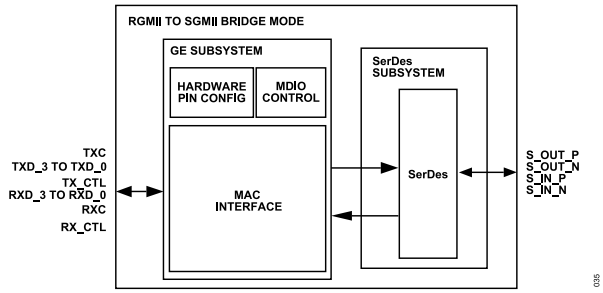


Figure 35. ADIN1320 in SGMII-RGMII Bridge Mode

MANAGEMENT INTERFACE

The MII management interface provides a two-wire serial interface between a host processor or MAC and the ADIN1320, allowing access to control and status information in the GE subsystem, copper PHY core, and SerDes subsystem management registers.

The MII management interface consists of the following:

- MDC, clock line.
- MDIO, bidirectional data line.
- PHYAD_0 pin to PHYAD_3 pin, which configures device addresses for each PHY.
- INT_N, management interrupt.

The interface is compatible with both IEEE Standard 802.3 Clause 22 and Clause 45 management frame structures, as shown in Table 16 and Table 17, respectively, and defined as the following:

- Preamble: establishes synchronization at beginning of frame.
- Start of frame.
- 01 indicates start of Clause 22 frame.
- 00 indicates start of Clause 45 frame.
- OP: the operation code indicates type of frame transaction.
- PHYAD/PRTAD: PHY address. MSB first, only the PHY with matching PHY address hardware configuration responds.
- REG ADDR/DEVAD: register address, MSB first.
- TA: used to avoid contention during a read transition, 2-bit time spacing between register address field and data field.
- DATA: 16-bit field, MSB first.
- ADDRESS/DATA: 16-bit field, MSB first.
- IDLE: high-Z state, the MDIO line is pulled high by the pull-up resistor.

The ADIN1320 adds a set of registers, referred to as extended management interface (EMI) registers, in addition to those specified in IEEE Standard 802.3. These EMI registers are accessed indirectly. Access to the EMI registers is primarily through the interface defined in Clause 45. For systems that do not support this interface, an alternative access mechanism is provided via the interface defined in Clause 22.

It is important to note that copper PHY registers are accessible only when the copper PHY is active, and similarly, SerDes subsystem registers are accessible only when the SerDes subsystem is active. In configurations where both subsystems are active simultaneously, the SerDes Subsystem's IEEE standard and vendor-specific registers are offset by 0xFC00 to ensure proper address mapping and avoid conflicts. Refer to Register Summary for more details.

Interrupt (INT_N)

The ADIN1320 can generate an interrupt to a host processor or MAC via the INT_N pin based on various user configurable conditions. Both the copper PHY and SerDes subsystem can be active simultaneously, and the relevant interrupt mask registers can be updated according to the interface requiring the interrupt. Specifically, the IRQ_MASK register (address 0x0018) must be updated to configure interrupts for the copper PHY, while the SD_IRQ_MASK register (address 0xFC18) must be updated for the SerDes subsystem. Additionally, the GE_IRQ_EN register (address 0xFF1D) must be updated to configure interrupts for the GE Subsystem.

The following conditions can be selected to trigger an interrupt:

- For both copper PHY and SerDes subsystem:
  - Link status change
  - MAC interface FIFO overflow/underflow
  - Autonegotiation page received
  - Autonegotiation status change
  - MDIO synchronization lost
  - Frame checker and generator
- Copper PHY only:
  - Speed change
  - Receive status change (1000BASE-T only)
  - Idle error counter saturated (1000BASE-T only)
  - Cable diagnostic change
- SerDes subsystem only:
  - SerDes subsystem PLLs lock lost interrupt
- GE subsystem:
  - Hardware reset
  - Auto media selection change
  - WoL

When an interrupt occurs, the system can poll the relevant status registers to determine the source of the interrupt: the IRQ_STATUS register (address 0x0019) for the copper PHY, the SD_IRQ_STATUS register (address 0xFC19) for the SerDes subsystem, and the GE_IRQ_LAT register (address 0xFF1E) for the GE subsystem.

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Table 16. Clause 22 Management Interface Frame Format

Operation	Preamble	Start of Frame	OP	PHYAD[4:0]	REG ADDR[4:0]	TA	DATA[15:0]	IDLE
Read	32 1s	01	10	AAAAA	RRRRR	Z0	d....d	Z
Write	32 1s	01	01	AAAAA	RRRRR	10	d....d	Z

Table 17. Clause 45 Management Interface Frame Format

Operation	Preamble	Start of Frame	OP	PRTAD[4:0]	DEVAD[4:0]	TA	ADDRESS/DATA[15:0]	IDLE
Address	32 1s	00	00	PPPPP	EEEEE	10	A.....A	Z
Write	32 1s	00	01	PPPPP	EEEEE	10	d....d	Z
Read	32 1s	00	11	PPPPP	EEEEE	Z0	d....d	Z
Post-read Increment Address	32 1s	00	10	PPPPP	EEEEE	Z0	d....d	Z

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MDI INTERFACE

The MDI connects the ADIN1320 to the Ethernet network via a transformer, as shown in Figure 36. In 1000BASE-T mode, transmit, and receive occur simultaneously on each of the MDI_x_x pairs. In 10BASE-T and 100BASE-TX modes, MDI_0_x are used to transmit when operating in MDI configuration and to receive when operating in MDIX configuration. The opposite is true of MDI_1_x in 10BASE-T mode and 100BASE-TX mode. For example, MDI_1_x are used to receive when operating in MDI configuration and to transmit when operating in MDIX configuration. If auto MDIX is enabled, the ADIN1320 automatically determines if the MDI or MDIX configuration must be used. Otherwise, it is forced to the chosen MDI or MDIX configuration. In 10BASE-T mode and 100BASE-TX mode, MDI_2_x and MDI_3_x are unused. The Flip MDI Dimensions section shows the mapping of the transmitter and receiver to the pins for the various modes across speeds.

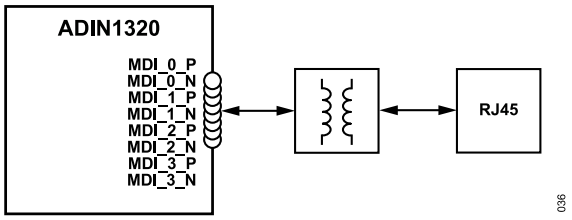


Figure 36. Media Dependent Interface

Flip MDI Dimensions

The ADIN1320 supports flipping the PHY dimensions to accommodate and simplify routing to different RJ-45 pinout orientations. The flip feature is user programmable over the MDIO interface. The default setting is normal MDI pin mapping as shown in Table 18 and Table 19.

Table 18. MDI/MDIX Pin Mapping

MDI Pins	MDI Pin Mapping[1]		MDIX Pin Mapping[1]	
	10BASE-T/ 100BASE-TX	1000BASE-T	10BASE-T/ 100BASE-TX	1000BASE-T
MDI_0_P/ MDI_0_N	Transmit ±	Transmit A± Receive B±	Receive ±	Transmit B± Receive A±
MDI_1_P/ MDI_1_N	Receive ±	Transmit B± Receive A±	Transmit ±	Transmit A± Receive B±
MDI_2_P/ MDI_2_N	Not applicable	Transmit C± Receive D±	Not applicable	Transmit D± Receive C±
MDI_3_P/ MDI_3_N	Not applicable	Transmit D± Receive C±	Not applicable	Transmit C± Receive D±

[1] Refer to IEEE802.3 Clause 40.8 for MDI/MDIX connector pinout.

Table 19. MDI Pair Flip Pin Mapping

MDI Pins	MDI Normal Mode, GE_MAN_MDI_FLIP_CFG = 0[1]		MDI Pair Flip, GE_MAN_MDI_FLIP_CFG = 1[1]	
	10BASE-T/ 100BASE-TX	1000BASE-T	10BASE-T/ 100BASE-TX	1000BASE-T
MDI_0_P/ MDI_0_N	Transmit ±	Transmit A± Receive B±	Not applicable	Transmit D± Receive C±
MDI_1_P/ MDI_1_N	Receive ±	Transmit B± Receive A±	Not applicable	Transmit C± Receive D±
MDI_2_P/ MDI_2_N	Not applicable	Transmit C± Receive D±	Receive ±	Transmit B± Receive A±
MDI_3_P/ MDI_3_N	Not applicable	Transmit D± Receive C±	Transmit ±	Transmit A± Receive B±

[1] Refer to IEEE802.3 Clause 40.8 for MDI connector pinout.

RESET OPERATION

The ADIN1320 supports a number of resets that include power-on reset, hardware reset, and multiple software reset types. All of these put the ADIN1320, including the Copper PHY core and SerDes subsystem, in a known state. Whenever the ADIN1320 is reset, the MAC interface output pins (output pins with respect to the ADIN1320) are driven to a known idle state. All outputs except RXC/RX_CLK are driven low and RXC/RX_CLK is driven high.

Power-On Reset

The ADIN1320 includes power monitoring circuitry to monitor all of the supplies. At power-up, the ADIN1320 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value.

Brownout protection is provided by monitoring the supplies to detect if one or more of the supplies drops below a minimum falling threshold value and holding the device in hardware reset until the power is valid again.

Table 20. Brown-Out Protection Threshold Values

Supply	Minimum Falling Threshold Value (V)
AVDD_3P3	2.35
VDDIO	1.35
DVDD_0P9	0.7

Hardware Reset

A hardware reset is initiated by the POR circuitry or by asserting the RESET_N pin low. Bring the pin low for a minimum of 10µs. Deglitch circuitry is included on this pin to reject pulses shorter than ~1µs.

A pull-up or pull-down of 1kΩ is recommended on this pin. Depending on the requirements of the MAC interface, the host may need to ensure that the PHY is out of hardware reset and ready to establish a link on power up, or may need to control when the PHY is brought out of hardware reset.

When the RESET_N pin is deasserted, the crystal oscillator circuit is enabled and the clock is given time to stabilize. The state of

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the hardware configuration pins is read and latched, the digital and analog circuits are initialized, and the copper PHY core clock multiplier unit (CMU) is reset. After 5ms from the deassertion of RESET_N, the management interface registers are accessible and the device can be programmed. This time is significantly shorter if a single-ended clock rather than a crystal is used and the management interface registers are accessible 3ms after the deassertion of RESET_N. If the ADIN1320 is configured to enter software power-down after a reset (see Table 27), the ADIN1320 enters software power-down mode and an interrupt is generated to indicate that a hardware reset occurred.

The following events occur after a hardware reset:

- The crystal oscillator circuit is enabled and time is allowed for the clock to stabilize.
- The hardware configuration pins are read and the values latched. These set the default values of the pin-dependent registers in the GE subsystem, SerDes subsystem and copper PHY core registers.
- The MAC interface block is reset.
- The copper PHY core is reset.
- The copper PHY core CMU is reset.
- The SerDes subsystem is reset.
- An interrupt to indicate that a hardware reset occurred is generated depending on the pin configuration, if the ADIN1320 was configured to enter software power-down mode after reset. Clearing the interrupt on INT_N after this condition can be performed by reading the GE_IRQ_LAT register at address 0xFF1E, or reading the (SD_)IRQ_STATUS register at Address 0x0019.

Software Reset

The ADIN1320 supports the following different software resets that reset specific circuit blocks under software control:

- GE Subsystem software reset with pin configuration
- GE Subsystem software reset
- Copper PHY core software reset
- SerDes Subsystem software reset

GE Subsystem Software Reset with Pin Configuration

The ADIN1320 supports a software reset capability that behaves in a similar way to a hardware reset (see Table 21 and the Register Summary section). A GE subsystem reset with a pin configuration can be initiated by setting the GE_SFT_ RST_CFG_EN bit (Address 0xFF0D) to 1 before setting GE_SFT_RST bit (Address 0xFF0C) to 1. This subsystem software reset follows the same reset sequence as the POR and hardware reset, except the crystal oscillator is not disabled and the clock stabilization step is skipped. The state of the hardware configuration pins is read and latched. These configuration pins set the default values of the pin dependent registers in the GE subsystem, SerDes Subsystem, and Copper PHY core registers. The MAC interface block, SerDes Subsystem, and Copper PHY core are reset. If a 125 MHz clock is selected as the PHY output clock, the GP_CLK pin, the PHY core CMU is not reset. Otherwise, the CMU is reset. The main difference between this type of reset and a hardware reset is that the crystal oscillator is not disabled.

The following events occur after a subsystem software reset with pin configuration:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are read and the values latched. These set the default values of the pin dependent registers in the subsystem and PHY core registers.
- The MAC interface block is reset.
- The Copper PHY core is reset.
- The Copper PHY core CMU is reset.
- The Serdes Subsystem is reset.
- The output reference clock is not available on the CLK25_REF pin during this reset.
- If a 125 MHz clock is selected as the PHY output clock it is not available on the GP_CLK pin during this reset.

GE Subsystem Software Reset

The GE subsystem can be reset by setting the GE_SFT_RST bit, Address 0xFF0C to 1. This bit is self clearing. Setting this bit resets the GE subsystem, copper PHY core, and SerDes subsystem registers, the MAC interface block, SerDes subsytem, and the copper PHY core. The hardware configuration pins are not reread, and previously latched values of the hardware configuration pins are used to set the default values of the pin dependent ADIN1320 registers.

The following events occur after a subsystem software reset:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are not reread. The pin dependent ADIN1320 registers are reset to the default values defined by the previously latched values of the hardware configuration pins.
- The MAC interface block is reset.
- The copper PHY core is reset.
- The Serdes subsystem is reset.
- If a 125MHz clock is selected as the PHY output clock, the GP_CLK pin, the PHY core CMU is not reset. Otherwise, the CMU is reset.
- The output reference clock (if enabled) is available on the CLK25_REF pin during this reset.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin during this reset.

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SerDes Subsystem Software Reset

The SerDes subsystem registers can be reset by setting the SD_SFT_RST bit in the SD_CONTROL register, Address 0x0000 to 1. This bit is self-clearing. Setting this bit resets the SerDes subsystem and its registers. The hardware configuration pins are not reread, and previously latched values of the hardware configuration pins are used to set the default values of the pin dependent registers in the SerDes subsytem registers. The GE subsystem registers are not reset to default values. This is a useful way to reset the SerDes registers to a known configuration defined by software without resetting the rest of the ADIN1320 circuitry.

The following events occur after a SerDes subsystem software reset:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are not reread. The pin dependent registers in SerDes subsystem registers are reset to the default values defined by the previously latched values of the hardware configuration pins. The GE subsystem and copper PHY core registers are not reset to their default values.
- The MAC interface block is not reset.
- The SerDes subsystem is reset.
- If a 125MHz clock is selected as the PHY output clock, the GP_CLK pin, the Copper PHY core CMU is not reset. Otherwise, the CMU is reset.
- The reference clock (if enabled) is available on the CLK25_REF pin during this reset.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin during this reset.

Copper PHY Core Software Reset

The copper PHY core registers can be reset by setting the SFT_RST bit in the MII_CONTROL register, Address 0x0000 to 1. This bit is self-clearing. Setting this bit resets the copper PHY core registers, the MAC interface block, and the copper PHY core. The hardware configuration pins are not reread, and previously latched values of the hardware configuration pins are used to set the default values of the pin dependent registers in the copper PHY core registers. The GE subsystem and SerDes subsystem registers are not reset to default values. This is a useful way to reset the copper PHY core registers to a known configuration defined by software without resetting the rest of the ADIN1320 circuitry.

The following events occur after a copper PHY core software reset:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are not reread. The pin dependent registers in copper PHY core registers are reset to the default values defined by the previously latched values of the hardware configuration pins. The GE subsystem and SerDes subsystem registers are not reset to their default values.
- The MAC interface block is not reset.
- The copper PHY core is reset.
- If a 125MHz clock is selected as the PHY output clock, the GP_CLK pin, the copper PHY core CMU is not reset. Otherwise, the CMU is reset.
- The reference clock (if enabled) is available on the CLK25_REF pin during this reset.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin during this reset.

Table 21. ADIN1320 Reset Options Summary

	Reset Type	Hardware Pin Configuration Values Latched Following Reset	Subsystem Registers Reset	Copper PHY Core Registers Reset	SerDes Registers Reset	MAC Interface Block Reset	XTAL Oscillator Disabled During Reset	CLK25_REF (if Enabled) Available During Reset	GP_CLK Output (if Enabled) Available During Reset
1	Hardware Reset	Yes	Yes	Yes	Yes	Yes	Yes	No	No
2	Subsystem Software Reset with Pin Configuration	Yes	Yes	Yes	Yes	Yes	No	No	No
3	Subsystem Software Reset	No	Yes	Yes	Yes	Yes	No	Yes	Yes
4	SerDes Subsystem Software Reset	No	No	No	Yes	No			
5	Copper PHY Core Software Reset	No	No	Yes	No	No	No	Yes	Yes

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POWER-DOWN MODES

The ADIN1320 supports multiple power-down modes: hardware, software, energy-detect, and EEE LPI. The hardware power-down mode offers the lowest power consumption.

Hardware Power-Down Mode

Hardware power-down mode is useful when operation of the ADIN1320 is not required and power must be minimized. The ADIN1320 enters hardware power-down mode when the RESET_N pin is asserted and held low. In this mode, all analog and digital circuits are disabled, the CMU is disabled, the clocks are gated off, and the only power is the leakage power of the circuits. The management interface registers are not accessible in this mode.

The following events occur in hardware power-down mode:

- All analog and digital circuits are disabled.
- The MAC interface output pins (output pins with respect to the ADIN1320) are tristated. Internally, these pins have a weak pull-down resistor, so these outputs are pulled low. This assumes no external pull-up resistors connected to these pins.
- All internal clocks are gated off.
- The PHY output clock (available on the GP_CLK pin) is disabled.
- The output reference clock (available on the CLK25_REF pin) is disabled.
- The management interface registers are not accessible.

Software Power-Down Mode

The ADIN1320 allows individual software power-down of the copper PHY Core and SerDes subsystem. In this mode, the copper PHY Core and/or SerDes subsystem powers down while maintaining access to the management interface, allowing configuration without establishing links.

Software power-down mode is useful when the device is being configured by software before links are brought up. The ADIN1320 can be configured to enter software power-down mode after reset using the appropriate pull-up/pull-down resistors on the LINK_ST pin and LED_0 pin, which sets the default value of the SFT_PD bit and SD_SFT_PD bit, on address 0x0000, to 1. The copper PHY core and SerDes subsystem can be made to enter software power-down mode individually by setting the corresponding software power down bit to 1 (SFT_PD bit for Copper PHY or SD_SFT_PD bit for SerDes Subsystem).

In software power-down, both analog and digital circuits operate in a low-power state. The CMU is typically disabled, most clocks are gated off, and the remaining digital circuitry runs at 25MHz. Signals or energy on the MDI_x_x and S_OUT/IN_x pins are ignored, and no links are established. The management interface remains accessible for configuration. When configured to output a 125MHz clock on the GP_CLK pin, the CMU stays enabled, increasing power consumption in this mode.

The following events occur in software power-down mode when SFT_PD bit is set:

- Copper PHY core's analog transmit and receive circuits are disabled.
- The RGMII/RMII/MII MAC interface output pins (output pins with respect to the ADIN1320) are driven to a known idle state. All outputs except RXC/RX_CLK are driven low and RXC/RX_CLK is driven high if in a mode where the RGMII/RMII/MII MAC interface is expected to be driven by the Copper PHY Core.
- Most internal clocks are gated off.
- The output reference clock (if enabled) is available on the CLK25_REF pin.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.

The following events occur in software power-down mode when SD_SFT_PD bit is set:

- SerDes subsystem's analog transmit and receive circuits are disabled.
- The RGMII/RMII/MII MAC interface output pins (output pins with respect to the ADIN1320) are driven are driven low if in a mode where the RGMII/RMII/MII MAC interface is expected to be driven by the SerDes subsystem. The serial output lines would be put in Hi-Z state.
- Most internal clocks are gated off.
- The output reference clock (if enabled) is available on the CLK25_REF pin.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.

The ADIN1320 copper PHY Core or SerDes subsystem exits software power-down mode when the respective SFT_PD or SD_SFT_PD bit is cleared. Upon exit, the they initiate link establishment based on their current configuration.

Energy Detect Power-Down Mode

In energy detect power-down mode, the ADIN1320 is powered down but still monitors the line for signal energy. Typically, the ADIN1320 enters this mode when there is no copper cable plugged in and remains in this mode until a remote link partner is available. This functionality applies only to copper media.

Energy detect power-down mode can be enabled using the appropriate pull-up/pull-down resistors on the LINK_ST pin and LED_0 pin (see Table 27) or via software. When the PHY is in normal operation (not software power-down) and energy detect power-down mode is enabled, the PHY enters energy detect power-down mode after a number of seconds of silence on the line. This is a very low power mode in which the analog and digital circuits are in a low power state. Typically, the CMU is disabled and most clocks are gated off. If the ADIN1320 is configured to output a 125 MHz

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clock on the GP_CLK pin, the CMU is enabled and the power in this mode is higher. The PHY monitors the line for signal energy and sends a link pulse once every second. If signal energy is detected, the PHY exits energy detect power-down mode and starts sending link pulses.

The following events occur when in energy detect power-down mode:

- All analog and digital circuits are disabled.
- Most internal clocks are gated off.
- The output reference clock (if enabled) is available on the CLK25_REF pin.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.
- The PHY monitors the line for signal energy.

Typically, the PHY enters energy detect power-down mode when the cable is unplugged and exits this mode when a cable is plugged in and a remote link partner appears. In this mode, the PHY periodically wakes up and transmits a link pulse on the MDI_0 and MDI_1 pins to ensure that a lock out is avoided where both local and remote PHY are in an energy detect power-down mode.

EEE, Low Power Idle Mode

The ADIN1320 supports EEE when using copper interface and is compliant with the IEEE 802.3 standard. EEE can be used to reduce power consumption when no data is being transmitted by either the local or remote end. Both devices must have EEE enabled and advertised. If EEE is advertised by the local and remote PHYs, an EEE link is brought up. If there is no data to be sent, the MAC requests the ADIN1320 to enter EEE low power idle mode. When the MAC or remote PHY wishes to send data, the ADIN1320 PHY wakes up (within 16µs for 1000BASE-T and 20µs for 100BASE-TX) and can send or receive data.

The transition between lower power consumption and normal operation is handled such that all frames remain intact and transmitted as normal, and the upper layer protocols are unaware of any changes at the PHY level. When data is transmitted, it continues to transmit at the fastest link speed established. See the Typical Power Consumption section for more details on the power savings in this mode.

EEE mode can be enabled using the appropriate pull-up/pull-down resistors on the LINK_ST pin and LED_0 pin (see Table 27) or by setting the EEE_1000_ADV or EEE_100_ADV bits (EEE_ADV register, Address 0x8001) to 1. During link autonegotiation, the local and remote PHYs advertise the speeds supported, including if they are EEE capable and, the PHYs then attempt to bring up a link at the highest speed supported by both sides. If EEE is advertised by both the local and remote PHYs for the established link speed, the link is an EEE link. If there is an EEE link and if at some point in time there is no data to be sent, the MAC requests the ADIN1320 to enter EEE LPI mode, which is almost as low power as energy detect power-down mode. The ADIN1320 wakes up periodically to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits to maintain link integrity.

The following events occur when in EEE LPI mode:

- All analog and digital circuits are in a low power mode.
- Most internal clocks are gated off.
- The output reference clock (if enabled) is available on the CLK25_REF pin.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.
- The PHY monitors the line for an LPI wake signal.

When the local or remote PHY wishes to send data, the PHY initiates an LPI wake sequence and the PHYs can then start to send or receive data within 16µs for 1000BASE-T (20 µs for 100BASE-TX).

STATUS LED

The ADIN1320 provides three configurable status LEDs. The LEDs can be configured using LED Control registers (0x001B to 0x001D) for copper modes, or using fiber LED pattern and configuration registers (0xFC9B to 0xFCAD) to indicate speed of operation, link status, activity, or pattern. The LED pin can also be configured to be active high or active low via GE subsystem LED active low status register (0xFF29). The recommendation is to use the LEDs as active low. The ADIN1320 automatically senses the connection of the LEDs during power up and reset. For example, if it senses that the pin is pulled to a supply, it configures the LED for active low operation. By default, LED_0 illuminates when a link is established and blinks when there is activity. LED_1 and LED_2 illuminates when 1Gbps and 100Mbps link is established respectively. The default LED operation can be overwritten in software using the PHY LED control registers. LED_0 and LED_1 are referenced to AVDD_3P3. LED_2 is referenced to the VDDIO domain, a level shifter may be required when VDDIO is running at a lower voltage.

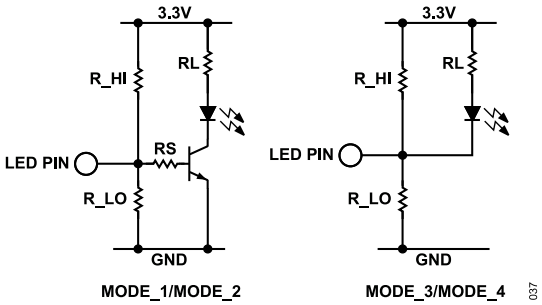


Figure 37. LED Hardware Configuration Pin Interaction

The LED pins are also shared with pin configuration functions and it can be necessary for the voltage level on the pin to be at a certain value on power-on and reset to configure the ADIN1320 as required (set by a pull-up resistor from the pin to the supply (R_HI) and a pull-down resistor from the pin to GND (R_LO) in Figure 37).

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The default operation of the LED is active low. So, if the default configuration setting is MODE_4, an external LED circuit using an active low LED results in a Logic 1 being read at the pin, and so the LED behaves as expected. For example, the LED does not turn on at power-on and reset.

An active low LED circuit is functional for a configuration setting of MODE_3 where the sense voltage is such that an active low LED is still off during power-on and reset, because there is insufficient forward voltage.

For configuration settings of MODE_1 or MODE_2, an external transistor must drive the LED as an active high LED, as shown in Figure 37. It is also be possible to drive an active high LED directly from the pin. However, this necessitates the use of an LED with a low forward voltage and, depending on the LED chosen, the LED may be quite dim.

LINK STATUS, LINK_ST

The LINK_ST pin is a general-purpose output used to indicate to the MAC whether a valid link has been established. LINK_ST polarity can be set using LED_1 hardware configuration pin according to Table 31 . For applications requiring a fourth LED (LED_3), the LINK_ST pin must be used. The default drive current for this pin is 4mA, and it can be increased via GE_CLK_DRV bit in GE subsystem clock I/O control register (0xFF3B), if the application requires the LINK_ST pin to drive an LED directly. LINK_ST is referenced to the VDDIO domain and is used for hardware strapping (PHY_CFG1). A level shifter may be required when VDDIO is running at a lower voltage.

PHY OUTPUT CLOCKS

The following internal PHY clock signals can be made available at the GP_CLK pin:

- 125MHz free running clock
- 125MHz recovered clock
- 25MHz clock
- 25MHz or 125MHz free running clock
- 25MHz or 125MHz recovered clock
- 125MHz Tx PLL from SerDes subsystem
- 125MHz Rx PLL recovered clock from SerDes subsystem

This is configured in through register writes via the GE_CLK_CFG register, Address 0xFF1F. By default, the PHY clock is off. Note that selecting the 125MHz free running clock has an impact on power consumption, as the CMU is always powered up except during reset and power up.

POWER SUPPLY DOMAINS

The ADIN1320 has the following three power supply domains and requires a minimum of two supply sources, 0.9V and 3.3V:

- 0.9V:
  - DVDD_0P9 is the digital core power supply input.
- 3.3V:
  - AVDD_3P3 is the analog power supply input for the PHY MDI interface, analog circuitry, XTAL oscillator, DLL, CLK25_REF generation, LED_0 and LED_1 circuitry, and SerDes subsystem.
- 3.3V, 2.5V, or 1.8V:
  - VDDIO enables MAC interface voltage supply to be configured independently of the other circuitry on the ADIN1320. In most cases, RMII/MII is operated at 3.3V and RGMII is operated at 2.5V, but the MAC interface can operate at 3.3V, 2.5V, or 1.8V to allow the MAC interface to run at a lower voltage and power if the MAC supports this. VDDIO also powers LED_2, and LINK_ST/LED_3 circuit. VDDIO also powers MDIO interface and RESET_N.

There are no power supply sequencing requirements around the order of power being applied to the device.

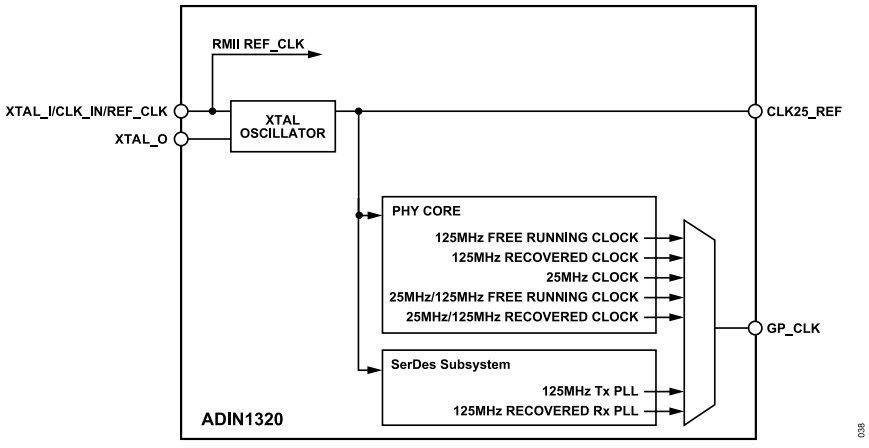


Figure 38. PHY Output Clocks Simplified Diagram

HARDWARE CONFIGURATION PINS

The ADIN1320 can operate in unmanaged or managed applications. In unmanaged applications, the desired operation of the PHY is configured from hardware configuration pins without any software intervention. For unmanaged applications, do not configure the PHY to enter software power-down after reset to ensure that the PHY immediately attempts to bring up links as configured by the PHY_CFG1 and PHY_CFG0 hardware configuration pins after power is applied to the device.

In managed applications, software is available to configure the PHY via the management interface (MDIO/MDC). In this case, it is possible to configure the PHY to enter software power-down mode after reset, such that the PHY can be configured before linking is attempted.

Hardware configuration pins are pins shared with functional pins and the voltage level on the pin is sensed and latched upon exiting from a reset. Some hardware configuration pins are multilevel sense, while others are two-level sense. Using two resistors, R_LO and R_HI (see Figure 39), four different voltage levels can be sensed, as shown in Table 22. Only MODE_1 (L) and MODE_4 (H) are relevant to the two-level sense pins and these are implemented with a 5.6kΩ pull-down resistor or a 5.6kΩ pull-up resistor, respectively. Note that LED_0 and LED_1 must be pulled up to the AVDD_3P3 rail rather than VDDIO.

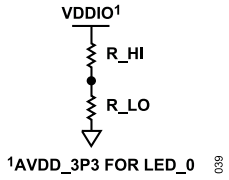


Figure 39. Hardware Configuration Pin Implementation

Note that the values listed in Table 22 assume no extra loading from circuitry external to the ADIN1320. It is likely that some configuration pins can be connected to a field-programmable gate array (FPGA) input that can have its own internal pull-up/pull-down resistor. This loads the resistor divider voltage.

Table 22. Configuration Modes

Mode	R_LO	R_HI	Voltage Threshold
MODE_1	5.6kΩ	Open	
MODE_2	5.6kΩ	39kΩ	>0.1 × VDDIO[1]
MODE_3	39kΩ	5.6kΩ	>0.5 × VDDIO[1]
MODE_4	Open	5.6kΩ	>0.9 × VDDIO[1]

[1] Note that the supply rail for the LED_0/1 pin is AVDD_3P3 rather than VDDIO. Therefore, pull up any pull-up on the LED_0/1 pin to AVDD_3P3.

Table 22 shows recommended resistor values for the multistrap pins with the corresponding voltage threshold range required for each mode. Table 23 shows the voltage ranges involved for each mode vs. VDDIO voltage. The voltage levels shown were chosen to steer clear of standard V_{IH}/V_{IL} voltage levels to avoid any shoot-through currents (and unknown voltage levels) in the input driver of disabled devices connected to the pins. VIH/VIL voltage levels do have voltage and device dependencies. Therefore, it may not always be possible to avoid such artifacts.

Table 23. Voltage Levels for Modes vs. VDDIO Voltage

VDDIO[1] Mode	1.8V (V)	2.5V (V)	3.3V (LED_0/1 = 3.3V) (V)
MODE_1	<0.18	<0.25	<0.33
MODE_2	>0.18	>0.25	>0.33
MODE_3	>0.9	>1.25	>1.65
MODE_4	>1.62	>2.25	>2.97

[1] Note that the supply rail for the LED_0/1 pin is AVDD_3P3 rather than VDDIO. Therefore, pull up any pull-up on the LED_0/1 pin to AVDD_3P3.

The large resistor values recommended in Table 22 were chosen to minimize power consumption from the resistor ladder. Smaller value resistors can also be used, but the user must maintain the same resistor ratios for the values used.

When arranging hardware strapping, review how the MAC interface pins default (whether internal pull-ups or pull-downs exist) on devices connected to the ADIN1320 to ensure they are not conflicting with desired strapping configuration.

HARDWARE CONFIGURATION PIN FUNCTIONS

The following functions can be configured via the ADIN1320 hardware pins (refer to the Table 24 section for pin details):

- PHY address selection
- MAC interface selection (RGMII, RMII, MII, or SGMII)
- Forced or advertised link speed for copper and/or fiber PHY
- Software power-down mode after reset
- Downspeed enable for copper PHY
- Energy detect power-down mode for copper PHY
- Energy efficient Ethernet (EEE) enable for copper PHY
- Auto-MDIX for copper PHY
- LINK_ST polarity configuration
- Enhanced link detection enable/disable
- Enable/disable Clause 37 autonegotiation for backplane

Table 24. Hardware Configuration Pins

Configuration Function	Functional Pin/Hardware Configuration Mnemonic[1]	Pin Levels	Internal Pull-Down[2]	Default Configuration
PHYAD_0 to PHYAD_3 Configuration	RXD_3/PHYAD_3	2	Yes	PHY Address 0x0
	RXD_2/PHYAD_2	2	Yes	
	RXD_1/PHYAD_1	2	Yes	

HARDWARE CONFIGURATION PINS

Table 24. Hardware Configuration Pins (Continued)

Configuration Function	Functional Pin/Hardware Configuration Mnemonic[1]	Pin Levels	Internal Pull-Down[2]	Default Configuration
	RXD_0/PHYAD_0	2	Yes	
PHY Forced or Advertised Link Speed (Copper/Fiber), Software Power-Down Mode After Reset, Downspeed Enable (Copper), Energy Detect Power-Down Mode (Copper), and EEE (Copper)	LINK_ST/PHY_CFG1 LED_0/PHY_CFG0	4 4	None[3] None	Unknown (external resistors are required)
Auto MDIX (Copper)	LED_2/GP_CLK/MDIX_MODE	4	None[3]	Unknown (external resistors are required)
MAC Interface Selection	MACIF_SEL2 RX_CTL/RX_DV/MACIF_SEL1 RX_CLK/MACIF_SEL0	2 2 2	Yes Yes Yes	RGMII to copper with 2ns internal delay on RXC and TXC
LINK_ST Polarity Enhanced Link Detection Enable Enable/Disable Clause 37 Autonegotiation for Backplane	LED_1/LSFLD_CFG	4	None	Unknown (external resistors are required)

[1] Hardware configuration pin is the last pin name in the pin mnemonic.

[2] The internal pull-down has a typical value of 45kΩ.

[3] Internal pull-down resistor only enabled while RESET_N is asserted.

HARDWARE CONFIGURATION PINS

PHY Address Configuration

PHY address configuration is shared with the RXD_3 pin to RXD_0 pin and can be configured according to Table 25. Four of the ADIN1320 pins are available for configuring the PHY address. These are two-level configuration pins, which means that it is possible to configure the ADIN1320 to any of the 16 available PHY addresses. In many applications, the default address of 0x0 is used and, in that case, it may not be necessary to configure these pins externally because the RXD_3 pin to RXD_0 pin have weak internal pull-down resistors. This assumes that no other system level circuitry attached to these nodes, such as the MAC or Ethernet switch, has internal pull-up resistors on these pins.

Table 25. PHY Address Configuration

PHY Address	PHYAD_3 Pin	PHYAD_2 Pin	PHYAD_1 Pin	PHYAD_0 Pin
0	Low	Low	Low	Low
1	Low	Low	Low	High
2	Low	Low	High	Low
3	Low	Low	High	High
4	Low	High	Low	Low
5	Low	High	Low	High
6	Low	High	High	Low
7	Low	High	High	High
8	High	Low	Low	Low
9	High	Low	Low	High
10	High	Low	High	Low
11	High	Low	High	High
12	High	High	Low	Low
13	High	High	Low	High
14	High	High	High	Low
15	High	High	High	High

HARDWARE CONFIGURATION PINS

MAC Interface and Functional Mode Selection

The MACIF_SEL2, MACIF_SEL1, and MACIF_SEL0 pins are used for MAC interface selection and can be configured according to Table 26. MACIF_SEL1 and MACIF_SEL0 is shared with the RX_CTL/RX_DV/CRS_DV pin and RXC/RX_CLK pin respectively. In RGMII mode, it is possible to enable a 2ns internal delay on RXC only or on both RXC and TXC. The MACIF_SEL[2:0] pins have weak internal pull-down resistors. Therefore, by default, the ADIN1320 is configured in RGMII to copper mode with a 2ns delay on RXC and TXC. External resistors must be used to select any of the remaining MAC interface modes.

When configuring hardware strapping, ensure that the default states of the MAC interface pins (whether they have internal pull-ups or pull-downs) on devices connected to the ADIN1320 do not conflict with the intended strapping configuration.

The MAC interface can be selected via software by configuring GE_RGMII_CFG, GE_RMII_CFG, and GE_SD_CFG registers. However, because RMII mode requires 50MHz reference clock, it is impractical to select this mode via software.

Note that changing the MAC interface type via software is possible but not recommended. Always configure the device to enter software power-down mode using a specific MAC interface type defined by hardware.

Table 26. MAC Interface and Functional Mode Selection

MAC Interface Selection	MACIF_SEL2	MACIF_SEL1	MACIF_SEL0
RGMII to Copper, 2ns Internal Delay on RXC and TXC. Refer to Table 27	Low	Low	Low
RGMII to Copper, 2ns Internal Delay on RXC only. Refer to Table 27	Low	High	Low
SGMII to Copper. Refer to Table 27	Low	Low	High
RMII or MII to Copper. Refer to Table 29	Low	High	High
RGMII to Copper or Fiber Auto-media detect. 2ns Internal Delay on RXC and TXC. Refer to Table 27	High	Low	Low
RGMII to Copper or Fiber Auto-media detetec. 2ns Internal Delay on RXC only. Refer to Table 27	High	High	Low
RMII or MII to Copper or Fiber Auto-media detect. Refer to Table 29	High	High	High
RGMII, RMII, MII to Fiber, RGMII to Backplane, Media Converter, or SGMII-RGMII Bridge. Refer to Table 28	High	Low	High

HARDWARE CONFIGURATION PINS

PHY Configuration

The PHY_CFG1 and PHY_CFG0 hardware configuration pins are shared with the LINK_ST and LED_0 functional pins respectively. These pins must be configured according to the selected MAC interface mode, defined by the MACIF_SELx setting, and the intended PHY operating mode. These configuration modes support various features, including:

- PHY forced or advertised link speed (copper/fiber)
- Software power-down mode after reset
- Downspeed enable (copper)
- Energy detect power-down (EDPD) mode (copper)
- EEE enable (copper)
- Media converter
- SGMII-RGMII bridge mode

Refer to Table 28 for ADIN1320 configurations in fiber only, backplane, media converter, or SGMII-RGMII bridge modes. Refer to Table 27 when configuring ADIN1320 to use RGMII or SGMII as MAC interface, and Table 29 for RMII or MII as the MAC interface.

The PHY_CFG1 pin and PHY_CFG0 pin have no internal pull-up resistors, so external resistors must be used to configure these functions.

Table 27. PHY Configuration for RGMII to Copper/Fiber, and SGMII to Copper

Forced/Advertised	RGMII[1] to Copper and SGMII[2] to Copper.	RGMII to Copper/Fiber[3]	LINK_ST/ PHY_CFG1	LED_0/ PHY_CFG0	Row No.
Advertised Speeds (Autonegotiation[4] Enabled)	10BASE-T half duplex (HD)/full duplex (FD), 100BASE-TX HD/FD, and 1000BASE-T FD prefer follower[5]	1000BASE-X FD	MODE_4	MODE_4	1
	10BASE-T HD/FD, 100BASE-TX HD/FD, and 1000BASE-T FD prefer follower	1000BASE-X FD	MODE_1	MODE_4	2
	10BASE-T HD/FD, 100BASE-TX HD/FD, and 1000BASE-T FD prefer leader	1000BASE-X FD	MODE_2	MODE_4	3
	ADIN1320 in software power-down (SWPD) after reset. [6]	ADIN1320 in SWPD after reset	MODE_3	MODE_4	4
	10BASE-T FD	100BASE-FX FD	MODE_1	MODE_3	5
	100BASE-TX FD	100BASE-FX FD	MODE_2	MODE_3	6
	1000BASE-T FD prefer follower	1000BASE-X FD	MODE_4	MODE_3	7
	1000BASE-T FD prefer leader	1000BASE-X FD	MODE_3	MODE_3	8
	10BASE-T FD and 100BASE-TX FD	100BASE-FX FD	MODE_1	MODE_1	9
	10BASE-T FD, 100BASE-TX FD, and 1000BASE-T FD prefer follower	1000BASE-X FD	MODE_4	MODE_1	10
	10BASE-T FD, 100BASE-TX FD, and 1000BASE-T FD prefer leader	1000BASE-X FD	MODE_3	MODE_1	11
	1000BASE-T FD prefer follower with extended next page enabled	1000BASE-X FD	MODE_4	MODE_2	12
	1000BASE-T FD prefer leader with extended next page enabled	1000BASE-X FD	MODE_3	MODE_2	13
Forced Speed (Autonegotiation Disabled)	10BASE-T FD	100BASE-FX FD	MODE_2	MODE_1	14
	100BASE-TX HD	100BASE-FX FD	MODE_1	MODE_2	15
	100BASE-TX FD	100BASE-FX FD	MODE_2	MODE_2	16

1 For MACIF_SELx = 0b000, selects RGMII as MAC Interface with a 2ns internal delay in RXC and TXC. For MACIF_SELx = 0b010, RGMII has 2ns internal delay in RXC only.

2 MACIF_SELx = 0b001 selects SGMII as MAC Interface

3 Auto-media detect is supported in this mode. If the PHY links up over copper, copper mode functions apply—refer to the column to the left for applicable settings. If the PHY links up over fiber, the functions listed in this row apply. These fiber-specific functions are in addition to those defined for RGMII to Copper mode, as the PHY supports both copper and fiber operation under this configuration. For MACIF_SELx = 0b100, RGMII is selected as the MAC interface with a 2ns internal delay applied to both RXC and TXC. For MACIF_SELx = 0b110, the 2ns internal delay is applied to RXC only.

HARDWARE CONFIGURATION PINS

[4] Autonegotiation is specified in Clause 28 for copper and Clause 37 for 1000BASE-X. 100BASE-FX does not support autonegotiation. SGMII autonegotiation is always enabled.

[5] Downspeed, EDPD, and EEE are enabled.

[6] SerDes Subsystem is disabled in RGMII to Copper mode.

Table 28. PHY Configuration for RGMII/RMII/MII to Fiber, RGMII to Backplane, Media Converter, and SGMII-RGMII Bridge functions; MACIF_SELx = 0b101

PHY Speed Configuration/Functions	LINK_ST/ PHY_CFG1	LED_0/ PHY_CFG0	Row No.
RGMII[1] to 1000BASE-X FD	MODE_4	MODE_4	1
RGMII[2] to 1000BASE-X FD	MODE_1	MODE_4	2
1000BASE-T FD prefer follower to 1000BASE-X media converter	MODE_2	MODE_4	3
ADIN1320 in SWPD after reset. Copper PHY disabled.	MODE_3	MODE_4	4
RGMII[1] to 100BASE-FX FD	MODE_1	MODE_3	5
RGMII[2] to 100BASE-FX FD	MODE_2	MODE_3	6
100BASE-TX FD to 100BASE-FX FD media converter	MODE_4	MODE_3	7
100BASE-TX FD to 100BASE-FX FD media converter[3]	MODE_3	MODE_3	8
RGMII Back to Back Copper to External PHY media converter	MODE_1	MODE_1	9
MII to 100BASE-FX FD	MODE_4	MODE_1	10
RMII to 100BASE-FX FD	MODE_3	MODE_1	11
1000BASE-T FD, prefer Leader to 1000BASE-X FD Media Converter	MODE_3	MODE_2	12
SGMII-RGMII Bridge	MODE_2	MODE_1	13
RGMII[1] to 1000BASE-KX FD	MODE_1	MODE_2	14
RGMII[2] to 1000BASE-KX FD	MODE_2	MODE_2	15

[1] RGMII with 2ns internal delay in RXC and TXC.

[2] RGMII with 2ns internal delay in RXC only.

[3] Clause 28 Autonegotiation Disabled.

Table 29. PHY Configuration for RMII/MII to Copper/Fiber

Forced/Advertised	RMII/MII to Copper[1]	RMII/MII to Copper/Fiber[2]	LINK_ST/ PHY_CFG1	LED_0/ PHY_CFG0	Row No.
Advertised Speeds (Autonegotiation[3] Enabled)	RMII to 10 half duplex (HD)/full duplex (FD), 100 HD/FD[4]	RMII to 100BASE-FX FD	MODE_4	MODE_4	1
	RMII to 10 HD/FD and 100 HD/FD	RMII to 100BASE-FX FD	MODE_1	MODE_4	2
	MII to 10BASE-T HD/FD, 100BASE-TX HD/FD[4]	MII to 100BASE-FX FD	MODE_2	MODE_4	3
	ADIN1320 in SWPD after reset, default setting is an input clock of 50MHz. SerDes subsystem is disabled.	ADIN1320 in SWPD after reset, default setting is an input clock of 50MHz.	MODE_3	MODE_4	4
	RMII to 10BASE-T FD	RMII to 100BASE-FX FD	MODE_1	MODE_3	5
	RMII to 100BASE-TX FD	RMII to 100BASE-FX FD	MODE_2	MODE_3	6
	MII to 10BASE-T FD	MII to 100BASE-FX FD	MODE_4	MODE_3	7
	MII to 100BASE-TX FD	MII to 100BASE-FX FD	MODE_3	MODE_3	8
	RMII to 10BASE-T FD and 100BASE-TX FD	RMII to 100BASE-FX FD	MODE_1	MODE_1	9
	MII to 10BASE-T FD and 100BASE-TX FD	MII to 100BASE-FX FD	MODE_4	MODE_1	10
Forced Speed (Autonegotiation Disabled)	MII to 10BASE-T FD	MII to 100BASE-FX FD	MODE_3	MODE_1	11

HARDWARE CONFIGURATION PINS

Table 29. PHY Configuration for RMII/MII to Copper/Fiber (Continued)

Forced/Advertised	RMII/MII to Copper[1]	RMII/MII to Copper/Fiber[2]	LINK_ST/ PHY_CFG1	LED_0/ PHY_CFG0	Row No.
	MII to 100BASE-TX HD	SGMII Back-to-Back Copper to External PHY media converter[5, 6]	MODE_4	MODE_2	12
	MII to 100BASE-TX FD	RMII to 10BASE-T FD using 5MHz Clock[6]	MODE_3	MODE_2	13
	RMII to 10BASE-T FD	RMII to 100BASE-FX FD	MODE_2	MODE_1	14
	RMII to 100BASE-TX HD	MII to 100BASE-FX FD	MODE_1	MODE_2	15
	RMII to 100BASE-TX FD	RMII to 100BASE-FX FD	MODE_2	MODE_2	16

1 MACIF_SELx = 0b011.

2 MACIF_SELx = 0b111, Auto-media detect is supported in this mode. If the PHY links up over copper, copper mode functions apply—refer to the column to the left for applicable settings. If the PHY links up over fiber, the functions listed in this row apply. These fiber-specific functions are in addition to those defined for RGMII to Copper mode, as the PHY supports both copper and fiber operation under this configuration.

3 Autonegotiation is specified in Clause 28 for copper and Clause 37 for 1000BASE-X. 100BASE-FX does not support autonegotiation.

4 Downspeed, EDPD, and EEE are enabled.

5 SGMII autonegotion is enabled

6 Clause 28 autonegotion is enabled

Forced/Advertised PHY Speed

As outlined in Table 27, it is possible to advertise all or a subset of PHY speed capabilities, select preferred follower or leader, set half duplex or full duplex mode, and enable or disable autonegotiation.

Autonegotiation is enabled for the first 13 rows in Table 27, such as in the case of advertised speeds modes. It is also possible to configure forced speed modes where autonegotiation is disabled and the speed is forced as shown in row 14 to row 16. For faster linkup for 1Gb links, extended next page is enabled in row 12 and row 13.

Referring to Table 27, three of the PHY_CFG1 and PHY_CFG0 hardware configuration pin settings result in the same link speed configuration (Row 1, Row 2, and Row 4). However, Row 1 also enables three other functions, Row 2 does not enable any extra functions, and in Row 4, the ADIN1320 is configured to enter software power-down mode after reset. Refer to Table 29 when using RMII or MII.

The enabling or disabling of autonegotiation and advertised speed settings can also be set using the standard IEEE registers, MII_CONTROL (Address 0x0000), AUTONEG_ADV (Address 0x0004), and MSTR_SLV_CONTROL (Address 0x0009).

When using the ADIN1320 in RGMII to 1000BASE-KX Mode, the Clause 37 autonegotion can be enabled via hardware configuration by setting LED_1/LSFLD hardware configuration pin to MODE_3 or MODE_4, see Table 31.

Software Power-Down After Reset

If the ADIN1320 is configured so that it does not enter software power-down mode after reset, the ADIN1320 attempts to bring up links at the configured speeds and MDI/MDIX configuration after it exits reset. If the ADIN1320 is configured so that it enters software power-down mode after reset (Row 4), the ADIN1320 waits in software power-down until it is configured over the MDIO interface, at which point the PHY configuration can be set to exit software power-down by software. The copper PHY core and SerDes subsystem can also be put into software power-down mode by setting the SFT_PD bit and SD_SFT_PD bit.

Downspeed Configuration

If downspeed is enabled, the PHY down speeds to a lower speed after a number of attempts if it cannot link at the highest speed advertised. The use of downspeed requires autonegotiation to be enabled with multiple speeds advertised. The default operation of downspeed can be overwritten in software by writing to DN_SPEED_TO_100_EN (PHY_CTRL_2 register, Address 0x0016, Bit 11), DN_SPEED_TO_10_EN (PHY_CTRL_2 register, Address 0x0016, Bit 10), and NUM_SPEED_RETRY (PHY_CTRL_3 register, Address 0x0017, Bits[12:10]).

Energy Detect Power-Down Configuration

If energy detect power-down is enabled and no energy is detected at the MDI pins, the ADIN1320 enters a low power mode. Therefore, this mode saves power where there is no cable connected or the remote PHY is powered down.

Energy Efficient Ethernet

If EEE is enabled and also advertised by the remote PHY, the ADIN1320 can enter a low power mode (low power idle) when no data is being transmitted by either end. See the EEE, Low Power Idle Mode section for more details.

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Auto MDIX Configuration

Auto MDIX configuration mode is shared with the LED_2/GP_CLK pin and can be configured according to Table 30. This pin does not have an internal pull-up resistor, so external resistors must be used to set the MDI/MDIX mode.

If auto MDIX is enabled (MODE_3 or MODE_4), the ADIN1320 automatically determines if the MDI or MDIX configuration must be used. Otherwise, the ADIN1320 is forced to the chosen MDI or MDIX configuration.

If enabling auto MDIX, the ADIN1320 supports auto MDIX with a preference for MDI or MDIX. This determines which MDI/ MDIX setting is first in the autocrossover algorithm. To achieve a faster MDI/MDIX resolution in some cases, set both PHYs to the same preferred configuration (MDI or MDIX) when a crossover cable is used, and to opposite preferred configurations if a straight-through cable is used, which has the advantage of still being able to work with a mismatch of wiring and optimize the time to resolve auto MDIX.

The default operation of auto MDIX can be overwritten in software.

Table 30. LED_2/MDIX_MODE Hardware Configuration

LED_2/ MDIX_MODE HW CFG	MDIX_MODE	SGMII/RGMII Bridge Mode
MODE_1	Manual MDI	RGMII-Tx MAC to SGMII PHY
MODE_2	Manual MDIX	RGMII MAC to SGMII PHY
MODE_3	Auto MDIX, Prefer MDIX	Reserved
MODE_4	Auto MDIX, Prefer MDI	SGMII MAC to RGMII PHY

LED_1 Hardware Configuration Pin

The LED_1 pin is a multifunctional signal that supports both hardware configuration and MAC interface signaling. It is sampled during power-up or reset to determine the configuration of link status polarity, fast link down operation, and Clause 37 autonegotiation, based on external resistor combinations as defined in Table 31.

When the MII interface is selected, the LED_1 pin may operate as either TX_ER or COL, depending on whether EEE advertisement is enabled:

- If EEE is enabled, the pin functions as TX_ER, an input from the MAC used to indicate transmit errors.
- If EEE is disabled, the pin functions as COL, an output from the PHY used in half-duplex mode to signal collision detection.

In all other interface modes, the pin functions exclusively as LED_1, providing link and activity indication.

If the MAC does not actively drive TX_ER and EEE is enabled, the voltage level on the LED_1 pin is determined by the external hardware configuration resistors. This level is used during reset to latch the desired configuration mode and persists into normal operation, directly influencing the MII TX_ER input.

MODE_1 and MODE_2 result in a low voltage level, while MODE_3 and MODE_4 result in a high level. However, MODE_2 and MODE_3 correspond to intermediate voltage levels that are more susceptible to noise, which may cause the signal level to shift. When the pin is pulled high (MODE_3/4), TX_ER will be asserted, potentially disrupting normal MII transmit behavior. Therefore, when EEE is enabled, careful consideration must be given to the selection of LED_1 configuration modes to ensure compatibility with MII functional requirements.

Table 31. LED_1 Hardware Configuration Pin

LED_1	LINK_ST Polarity	Fast Link Down	Clause 37 Auto-Negotiation
MODE_1	Active High	Disabled	Disabled
MODE_2	Active Low	Disabled	Disabled
MODE_3	Active High	Enabled	Enabled
MODE_4	Active Low	Enabled	Enabled

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LOOPBACK MODES

The ADIN1320 provides multiple loopback modes for the copper PHY and SerDes subsystems (see Figure 40), enabling comprehensive in circuit testing of digital and analog data paths when used with frame generators and checkers. The copper PHY supports remote loopback, digital loopback, line driver loopback, and external cable loopback, while the SerDes subsystem offers remote loopback, digital loopback, near end SerDes loopback, and external cable loopback.

Copper PHY All Digital Loopback

When using copper PHY, the default loopback mode is copper PHY all digital loopback mode. This loops the data within the PHY at the analog/digital boundary to check for proper operation of the PHY, but does not require the external analog components, connections, or analog supplies to be accurate. In all digital loopback mode, it is possible to also transmit to the MDI pins, which can be useful for transmit testing. By default, the LB_ALL_DIG_SEL bit (PHY_CTRL_ STATUS_1 register, Address 0x0013) is set, which selects copper PHY all digital loopback mode and the LB_TX_SUP bit (Bit 6 within the PHY_CTRL_STATUS_1 register) is also set, which suppresses the transmission of the signal to the MDI pins. Setting the PHY_CTRL_STATUS_1 register to a value of 0x1001 selects digital loopback with transmission to the MDI pins. The loopback bit (MII_CONTROL register, Address 0x0000, Bit 14) also needs to be set to enable copper PHY all digital loopback mode.

Copper PHY Line Driver Loopback

For copper PHY line driver loopback, leave the MDI pins open circuit, thereby transmitting into an unterminated connector/cable. The PHY can then operate by receiving the reflection from its own transmission. This provides similar capabilities to the external cable loopback without the need to create any wire shorts by unplugging the cable. Setting the LB_LD_SEL bit (PHY_CTRL_STATUS_1 register, Address 0x0013) selects copper PHY line driver loopback. The loopback bit (MII_CONTROL register, Address 0x0000, Bit 14) also needs to be set to enable line driver loopback.

SerDes All Digital Loopback

When operating the SerDes subsystem, the default loopback mode is the SerDes all digital loopback mode. In this mode, transmit data is internally looped back within the SerDes subsystem at the analog-to-digital boundary, enabling verification of proper PHY operation without requiring external analog components, or board level connections.

By default, the SD_PCS_TBI_LPBK_EN bit in the SD_PHY_CTRL_1 register (address 0x0013) selects the all digital loopback path. Loopback operation is controlled through the SD_LOOPBACK bit in the SD_CONTROL register (address 0x0000).

The SD_SFT_PD bit is asserted prior to any modification of loopback related registers. To enable loopback mode, set SD_SFT_PD = 1, then configure RFD_ENABLE = 0 and SD_LOOPBACK = 1. After completing the configuration, clear SD_SFT_PD = 0 to resume operation. To exit loopback mode, set SD_SFT_PD = 1, restore RFD_ENABLE = 1, and clear SD_LOOPBACK = 0, then clear SD_SFT_PD = 0. All loopback related register changes must be performed while SD_SFT_PD = 1.

SerDes Near End Loopback

The SerDes near end loopback mode validates the internal digital signal path, including the serializer, TX PLL, deserializer, and RX CDR circuitry. This mode provides internal datapath verification without requiring external loopback connections.

To ensure correct loopback operation, the SD_SFT_PD bit shall be asserted prior to enabling or modifying near end loopback controls. Specifically, SD_SFT_PD = 1 must be set before enabling near end loopback.

With soft power-down asserted, near end loopback is enabled by setting the HS_LPBK_EN bit in the SD_HS_LPBK_CFG register (Address 0xFCC9) to select SerDes near end loopback mode. In addition, the SD_LOOPBACK bit in the SD_CONTROL register (Address 0x0000) must be set. After the loopback configuration is complete, the SerDes is brought out of soft power-down by clearing SD_SFT_PD = 0. Normal near end loopback operation begins once the SerDes exits soft power-down.

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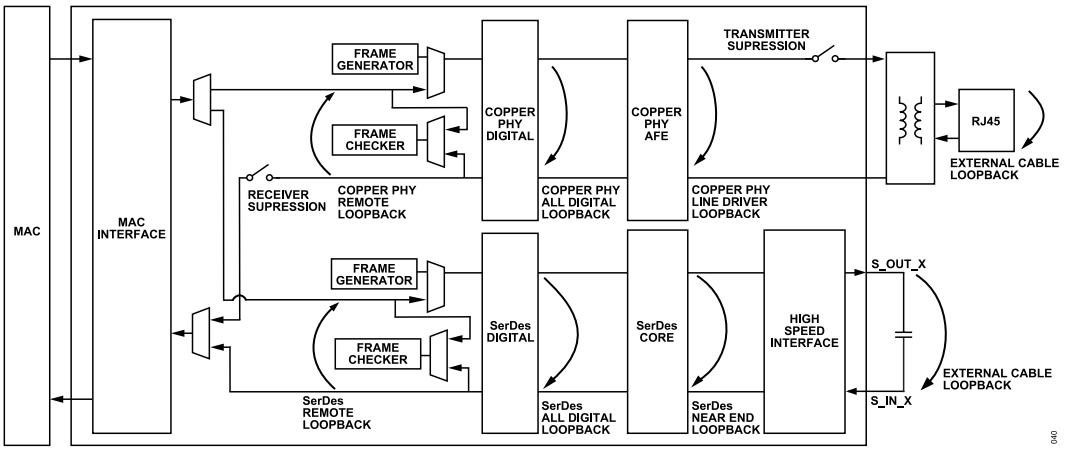


Figure 40. ADIN1320 Loopback Modes

External Cable Loopback

External cable loopback verifies the analog and digital path, including the external components and cable. For copper PHY, this requires that Pair 0 and Pair 1, and Pair 2, and Pair 3 are shorted together to provide an analog loopback at the end of the cable. The signal processing is adjusted so that the transmitted signal is not canceled. Setting the LB_EXT_EN bit (PHY_CTRL_STATUS_1 register, Address 0x0013) enables external cable loopback for copper PHY.

For the SerDes subsystem, connect the S_OUT_x pins to the corresponding S_IN_x pins through a 0.1µF AC coupling capacitor ensuring signal integrity and isolation for external loopback.

Remote Loopback

Remote loopback requires an active link with a remote PHY and is available separately for both copper and SerDes PHY subsystems, with identical configurations for each.

For copper PHY, enable remote loopback by setting the PHY_CTRL_STATUS_1 register to 0x0241. The ISOLATE_RX in the PHY_CTRL_STATUS_1 register can be enabled to prevent the packets from being forwarded to the MAC. Additionally, ensure that the loopback bit in the MII_CONTROL register (Address 0x0000, bit 14) remains cleared.

For SerDes subsytem or fiber PHY, enable remote loopback by setting the SD_PHY_CTRL_1 register to 0x01. Also, ensure that the SD_LOOPBACK bit in the SD_CONTROL register (Address 0x0000) is set to 1.

This configuration allows each subsystem to independently loop data back to the remote PHY for link integrity verification.

FRAME GENERATOR AND CHECKER

The ADIN1320 can be configured to generate frames and to check received frames in copper PHY and SerDes subsystem (see Figure 40). The frame generator and checker can be used independently to just generate frames or just check frames or can be used together to simultaneously generate frames and check frames. If frames are looped back at the remote end, the frame checker can be used to check frames generated by the ADIN1320.

When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator, the diagnostic clock must also be enabled.

The frame generator control registers configure the type of frames to be sent (random data, all 1s), the frame length, and the number of frames to be generated. The copper PHY and SerDes subsystem each have independent frame generators and checkers. The generation of the requested frames starts by enabling the frame generator by setting the FG_EN bit at address 0x9422 for copper PHY or the SD_FG_EN bit at address 0xFC4D in SerDes subsystem. When the generation of the frames is completed, the frame generator done bit is set which can be monitored at FG_DONE bit at Address 0x942B for copper PHY, or SD_FG_DONE bit at Address 0xFC56 in SerDes subsystem.

The frame checker is enabled using the frame checker enable bit (FC_EN bit at Address 0x9403 for copper PHY, or SD_FC_EN bit at Address 0xFC2D for SerDes subsystem). The frame checker can be configured to check and analyze received frames from either the MAC interface or the PHY, which is configured using the frame checker transmit select bit (FC_TX_SEL bit at Address 0x9406 for copper PHY, or SD_FC_TX_SEL bit at Address 0xFC30 for SerDes subsystem). The frame checker reports the number of frames received, cyclic redundancy check (CRC) errors, and various other frame errors. The frame checker frame counter register and frame checker error counter register count these events.

The frame checker counts the number of CRC errors and these are reported in the receive error counter register. To ensure synchronization between the frame checker error counter and frame checker frame counters, all of the counters are latched when the receive error counter register is read. Therefore, when using the frame checker, read the receive error counter first, and then read all other frame counters and error counters. A latched

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copy of the receive frame counter register is available in the FC_FRM_CNT_H and FC_FRM_CNT_L registers for copper PHY or SD_FC_FRM_CNT_H and SD_FC_FRM_CNT_L registers for SerDes subsystem.

In addition to CRC errors, the frame checker counts frame length errors, frame alignment errors, symbol errors, oversized frame errors, and undersized frame errors. In addition to the received frames, the frame checker counts frames with an odd number of nibbles in the frame in 100BASE-TX mode or 10BASE-T mode, and counts frames with an odd number of nibbles in the preamble in 100BASE-TX mode. The frame checker also counts frames with a noninteger number of nibbles in 10BASE-T mode and the number of false carrier events, which is a count of the number of times the bad start of stream delimiter (SSD) state is entered.

Frame Generator and Checker Used with Remote Loopback with Two PHYs

Using two PHY devices, the user can configure a convenient self contained validation of the PHY to PHY connection. Figure 41 shows an overview of how each PHY is configured. An external Ethernet cable is connected between both devices, and PHY1 is generating frames using the frame generator. PHY2 has remote loopback enabled on the MAC side. The frames issued by PHY1 are sent through the cable, through the PHY2 signal chain returned by PHY2 remote loopback, back again through the Ethernet cable, and checked by the PHY1 frame checker. Note that an equivalent connection and configuration is also applicable in the SerDes subsystem.

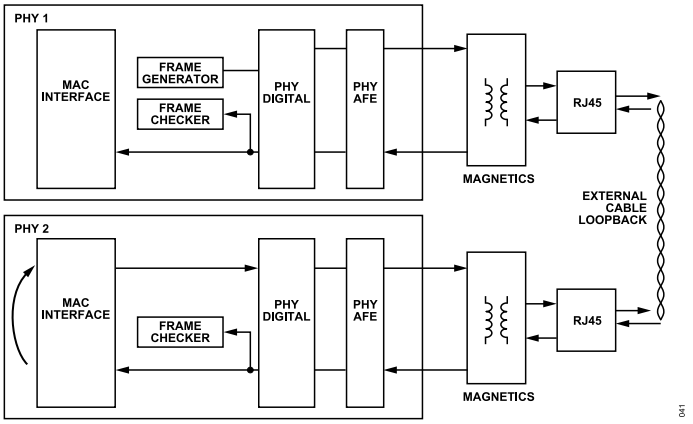


Figure 41. Remote Loopback Used Across Two PHYs for Self Check Purposes

ON-CHIP DIAGNOSTICS

CABLE DIAGNOSTICS

The ADIN1320 has on-chip copper cable diagnostics capabilities. This cable analysis can be used to detect cable impairments that may be preventing the establishment of a Gigabit link or degrading performance and can be performed both when the link is up or when the link is down.

Cable Length Estimate

Each time a 100BASE-TX or 1000BASE-T link is brought up, the ADIN1320 reports an estimate (typically ±15m) of the cable length based on the signal processing. This can be read in the cable diagnostics cable length estimate register. This estimate is not available for a 10BASE-T link.

Cable Analysis with TDR

When the link is down, the ADIN1320 can run cable fault detection using time domain reflectometry (TDR). By transmitting pulses and analyzing the reflections, the PHY can detect cable faults like opens, shorts, cross pair shorts, and the distance to the nearest fault. The PHY can also determine that the pair is well terminated and does not have any faults.

Put the remote PHY in a power-down state or disconnect the PHY to run cable fault detection because remote PHY link pulses can interfere with the analysis of the reflected pulses and can return a pair busy result. TDR measurements provide a more accurate cable length (typically ±2m) than the signal analysis method used in the cable length estimate described in the Cable Length Estimate section.

The cable fault detection is automatically run on all four pairs looking at all combinations of pair faults by first putting the PHY in standby (clear the LINK_EN bit, PHY_CTRL_3 register, Address 0x0017) and then enabling the diagnostic clock (set the DIAG_CLK_EN bit, PHY_CTRL_1 register, Address 0x0012). Cable diagnostics can then be run (set the CDIAG_RUN bit in the CDIAG_RUN register, Address 0xBA1B).

The results are reported for each pair in the cable diagnostics results registers, CDIAG_DTLD_RSLTS_0, CDIAG_DTLD_RSLTS_1, CDIAG_DTLD_RSLTS_2, and CDIAG_DTLD_RSLTS_3, Address 0xBA1D to Address 0xBA20. The distance to the first fault for each pair is reported in the cable fault distance registers, CDIAG_FLT_DIST_0, CDIAG_FLT_DIST_1, CDIAG_FLT_DIST_2, and CDIAG_FLT_DIST_3, Address 0xBA21 to Address 0xBA24.

Cable Polarity Inversion, Pair Swaps

A polarity inversion on each pair is reported in the polarity inversion register bits (PHY_2_STATUS register, Address 0x001F, Bits[13:10]) and the B_10_POL_INV bit (PHY_STATUS_1 register, Address 0x001A). Pair swaps are reported in the pair swap register bits (PAIR_23_SWAP bit, Address 0x001F and PAIR_01_SWAP bit, Address 0x001A).

Cable Signal Quality, MSE

The ADIN1320 provides a measure of the signal quality of the established link. This measurement relates directly to the signal-to-noise ratio (SNR) seen by the PHY receiver.

When the link is up, the signal quality on each pair is indicated in the mean square error register for each pair (MSE_A, MSE_B, MSE_C, and MSE_D registers, Address 0x8402 to Address 0x8405, Bits[7:0]). MSE register values in the range of 3 to 5 are expected for a cable length of up to 100 meters. As the cable length becomes longer and external noise increases, the mean square error (MSE) reported increases.

To calculate the associated signal-to-noise ratio during idle mode, apply the following formula to the MSE value read:

$$SNR\ (\text{dB}) = 10 \times \log10(MSE/1024) \quad (1)$$

An SNR value > 21dB (MSE of 8 or 9) indicates essentially error free performance. At 18dB or 19dB (MSE of 13 or 14), occasional errors may be observed over a 24-hour period.

ENHANCED LINK DETECTION

The ADIN1320 supports enhanced link detection, which is early detection and indication of link loss. This is a feature where the received signal is monitored, and if a significant number of consecutive samples of the signal are not as expected, early indication of link down is indicated. The ADIN1320 can simultaneously monitor for a significant number of consecutive 0s, a significant number of consecutive 1s, or a significant number of consecutive invalid levels.

The enhanced link detection can be enabled via hardware configuration (refer to Table 31) or via software. To change the configuration for 100BASE-TX via the enhanced link detection 100BASE-TX enable register bits and for 1000BASE-T via the 1000BASE-T enhanced link detection enable register bits in FLD_EN register, Address 0x8E27. Do not enable 1000BASE-T retrain (clear the B_1000_RTRN_EN bit, Address 0xA001) if enhanced link detection is enabled for 1000BASE-T.

If enhanced link detection is enabled, the ADIN1320 typically reacts to a break in the cable within 10µs and indicates link down via the LINK_ST pin. If enhanced link detection is not enabled, the ADIN1320 follows the IEEE standard, and in 100BASE-TX, it can take more than either 350ms or 750ms in 1000BASE-T, depending if the PHY is 1000BASE-T leader or 1000BASE-T follower.

The latched status of the enhanced link detection function can be read via the enhanced link detection status bit, FAST_LINK_DOWN_LAT (Address 0x8E38).

Having enhanced link detection enabled is not suitable for all applications because it causes the PHY to react quickly to high levels of disturbance on the MDI lines. This configuration needs to be considered when performing conformance testing and EMC testing where the media-dependent interface can be exposed to fast transients. These transients may trigger enhanced link detection to

bring the link down during such tests. In this case, it is preferred to configure all bits in the FLD_EN register to 0.

START OF PACKET INDICATION

The ADIN1320 is equipped with a feature that detects and indicates the start of packets (SOP) on both the transmit and receive sides. This feature supports IEEE 1588 time stamp controls, providing the MAC with more accurate timing information.

The SOP indication for both transmit and receive can be configured to be available at any of the following pins: LINK_ST, INT_N, LED_0, LED_1, and LED_2. This configuration is done using the respective registers: GE_IO_LINK_ST_OR_CNTRL, GE_IO_INT_N_OR_CNTRL, GE_IO_LED_A_OR_CNTRL, GE_IO_LED_B_OR_CNTRL, and GE_IO_LED_C_OR_CNTRL.

The detection of the transmit SOP occurs after the internal PHY FIFO, resulting in a fixed delay between the SOP indication at the pin and the actual SOP at the MDI pins or SerDes Interface pins.

The SOP indication is enabled via the SOP transmit and receive enables. To enable SOP in copper PHY, set the SOP_TX_EN bit and the SOP_RX_EN bit in the SOP_CTRL register (Address 0x944C). For fiber mode, set the SD_TX_SOP_DET_EN and the SD_RX_SOP_DET_EN in the SD_SOP_CTRL register (Address 0xFCE7).

By default, the SOP is asserted on the first byte or nibble of the frame. However, it can be configured to be asserted when the start frame delimitator (SFD) is detected in the frame. This is done by setting the SFD enable bit (SOP_SFD_EN for Copper PHY or SD_SFD_EN for Fiber).

The SOP indication is asserted for the duration of the frame by default. However, it can be configured to be asserted for a programmable number of cycles. This is done by setting the SOP N-cycle enable bit (SOP_NCYC_EN for Copper PHY or SD_SOP_NCYC_EN for Fiber), and the number of cycles is configured via the SOP N by 8 minus 1 cycles register (SOP_N_8_CYC_M_1 for Copper PHY or SD_SOP_N_8_CYC_M_1 for Fiber).

The ADIN1320includes a circuit that can delay each of the SOP transmit and receive indications by a programmable number of clock cycles. This feature is useful on the receive side to support MAC interfaces with long latency, ensuring that the received frame SOP indication is not asserted before the MAC receives the frame. On the transmit side, it helps align the transmit SOP indication assertion close to the reference point set on either MDI pins or S_IN_x pins. This eliminates the need for adjusting the time stamping point at the MAC/switch side. Programmable registers are available for the delays for various modes (1000BASE-X, 100BASE-FX, 1000BASE-T, 100BASE-TX, and 10BASE-T) for both transmit and receive. These registers are programmed via the SOP_RX_DEL register, SOP_TX_DEL register, SD_SOP_RX_DEL, and SD_SOP_TX_DEL.

TYPICAL POWER CONSUMPTION

Table 1 and the Typical Performance Characteristics section capture high level detail of the power consumption of the ADIN1320 under nominal conditions and across the device temperature range. Power consumption of a PHY depends heavily on power supply, speed established, operating condition, and capacitive loading on digital pins.

The tables in this section focus on RGMII to copper modes, as copper operation includes additional states such as cable unplug scenario that affect power consumption. Fiber modes do not include such operating conditions; therefore, all required electrical and power information for fiber operation is provided in Table 1.

POWER SUPPLIES

The most significant contributor to power consumption is the supply voltage choice and speed of operation.

The ADIN1320 can operate from a minimum of two power supply rails, where AVDD_3P3 = VDDIO = 3.3V and DVDD_0P9 = 0.9V. The VDDIO voltage requirements are dictated by the MAC interface. While two power supply rails result in a more simplified power strategy, the higher digital supply voltage translates directly to higher power consumption needs. This can be seen in Table 32, Table 33, and Table 34, which describe the various VDDIO voltages with ADIN1320 configured in copper mode. Using the lowest VDDIO supply rail can achieve a savings close to 100mW at Gigabit speeds with full throughput.

Speed of Link Established

The next biggest contributor to power consumption is the speed of the link. The ADIN1320 PHY has leading edge power consumption figures for Gigabit data. Lower data links run at lower power consumption numbers. This PHY was designed for low power consumption when operating at Gigabit speeds. As a result, 10 Mbps power consumption may not be as low as comparable offerings in the industry.

Lower Power Modes

The ADIN1320 has a number of means to lower power consumption under conditions where the PHY is not active or when it is linked and there is no data transmitting. Full details on these modes are captured in the Power-Down Modes section. Two key modes of operation to minimize power are energy detect power-down mode, when no link is present, and EEE low power idle mode, where a link is established but the line is idle. The power consumption under this state is significantly reduced compared to other idle states. Configuration of these modes is available through the hardware configuration pins or directly through the MDI interface. Typical power consumption for hardware reset, EEE, and EDPD are captured in Table 32, Table 33, and Table 34 as EEE.

Data Utilization

Table 32, Table 33, and Table 34 also capture the variation for data utilization for the various speeds in copper modes. Data is shown for 100% data to 0% or idle state. In the idle state, the PHY is linked, but no data transfer is taking place. The power consumption in this state is lower than full utilization.

Table 32. Typical Current and Power Consumption in RGMII to Copper Mode for VDDIO = 1.8V (T_A = 25°C, Cable Length = 100 meters)

Mode	DVDD_0P9 Core Supply, 0.9V (mA)	VDDIO Digital I/O Supply, 1.8V (mA)	AVDD_3P3 PHY AFE, LED Circuit, 3.3V (mA)	Total Power (mW)
1000BASE-T, 100% Data	43.6	36.6	70.5	336.7
1000BASE-T, Idle	40	28	70.5	319
100BASE-TX, 100% Data	13.6	8.9	39.3	157.1
100BASE-TX, Idle	12.5	7.8	39.3	155
10BASE-T, 100% Data	8.1	7.5	51.7	191
10BASE-T, Idle	7.7	7.4	35	135.4
Software Power-Down	3.7	1.1	3.2	15.7
Copper Cable Unplug	4.1	0.7	3	15
Hardware Power-Down	3.5	0.4	0.4	5

Table 33. Typical Current and Power Consumption in RGMII to Copper Mode for VDDIO = 2.5V (T_A = 25°C, cable length = 100 meters)

Mode	DVDD_0P9 Core Supply, 0.9V (mA)	VDDIO Digital I/O Supply, 2.5V (mA)	AVDD_3P3 PHY AFE, LED Circuit, 3.3V (mA)	Total Power (mW)
1000BASE-T, 100% Data	43.6	42	70.5	375.7
1000BASE-T, Idle	39.7	30	70.5	343.3
100BASE-TX, 100% Data	13.6	9.7	39.3	166
100BASE-TX, Idle	12.5	8.3	39.3	162
10BASE-T, 100% Data	8.2	7.8	51.6	197

TYPICAL POWER CONSUMPTION

Table 33. Typical Current and Power Consumption in RGMII to Copper Mode for VDDIO = 2.5V (T_A = 25°C, cable length = 100 meters) (Continued)

Mode	DVDD_0P9 Core Supply, 0.9V (mA)	VDDIO Digital I/O Supply, 2.5V (mA)	AVDD_3P3 PHY AFE, LED Circuit, 3.3V (mA)	Total Power (mW)
10BASE-T, Idle	7.6	7.4	35	140.7
Software Power-Down	4.3	1.2	3.3	17.7
Copper Cable Unplug	4	0.8	3.2	18
Hardware Power-Down	3.7	0.4	0.5	6

Table 34. Typical Current and Power Consumption in RGMII to Copper Mode for VDDIO = 3.3V (TA = 25°C, cable length = 100 meters)

Mode	DVDD_0P9 Core Supply, 0.9V (mA)	VDDIO Digital I/O Supply, 3.3V (mA)	AVDD_3P3 PHY AFE, LED Circuit, 3.3V (mA)	Total Power (mW)
1000BASE-T, 100% Data	43.6	48.7	70.5	431.2
1000BASE-T, Idle	39.6	32.5	70.5	375
100BASE-TX, 100% Data	13.6	11.1	39.3	177
100BASE-TX, Idle	12.5	9.4	39.3	172
10BASE-T, 100% Data	8.2	8.2	51.5	204.5
10BASE-T, Idle	7.5	7.9	34.8	147.6
Software Power-Down	4.3	1.6	3.3	20.3
Copper Cable Unplug	4.1	1.3	3	18
Hardware Power-Down	3.7	0.5	0.5	6.7

APPLICATIONS INFORMATION

SYSTEM OVERVIEW

The ADIN1320 is a low power, single port Gigabit Ethernet transceiver with support for copper and fiber interface, and backplane. It has low latency specifications primarily designed for industrial Ethernet applications. Figure 42 shows a basic system block diagram when using the ADIN1320 to interface with either copper or fiber. Other components in the block diagram may not be required when interfacing with copper only or fiber only, when configured in RGMII to 1000BASE-KX mode, media converter mode, or SGMII-RGMII bridge mode.

Consult the Hardware Configuration Pins section for PHY configuration options and MAC interface selection, and the MAC Interface section for specific information on each MAC interface configuration mode.

The Component Recommendations section captures some of the key requirements for external component selection for use with the ADIN1320.

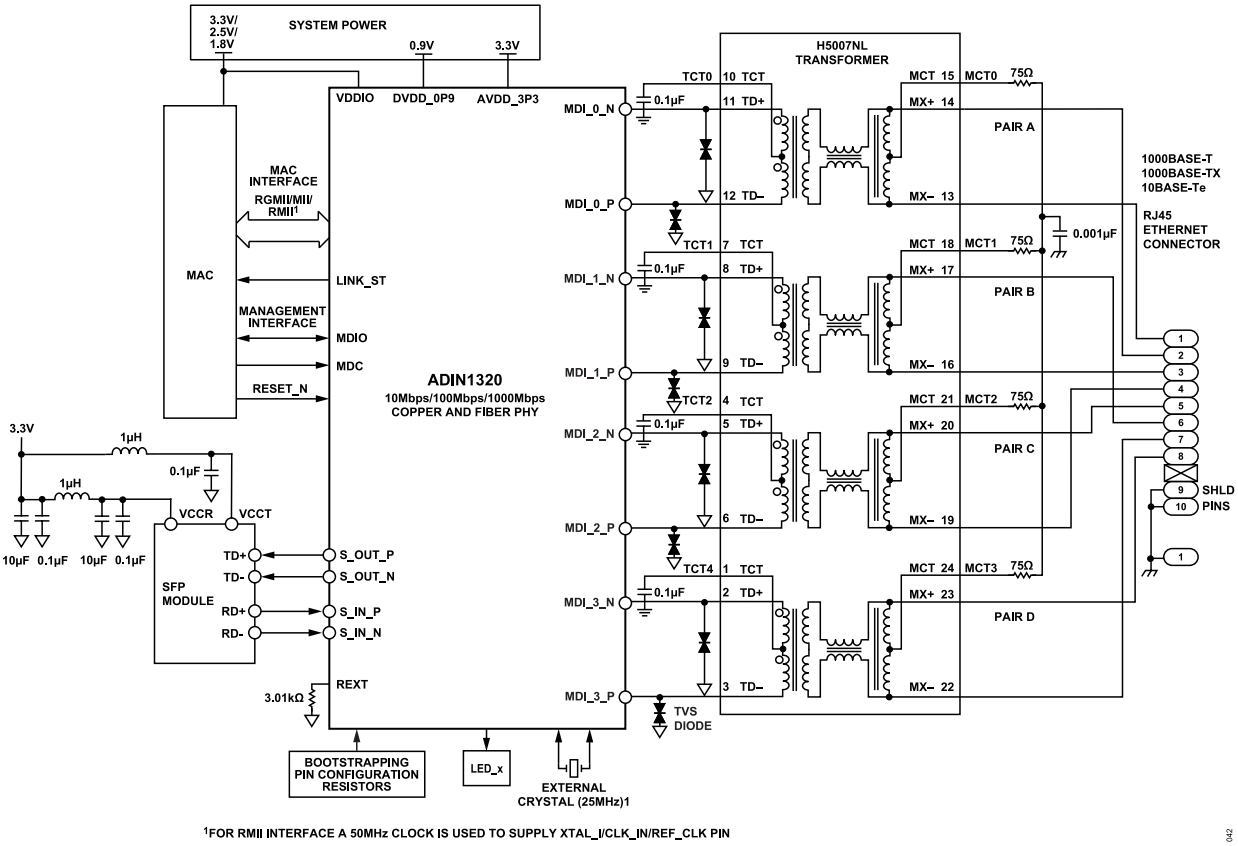


Figure 42. Simplified Typical Application Block Diagram Using Magnetics and SFP

APPLICATIONS INFORMATION

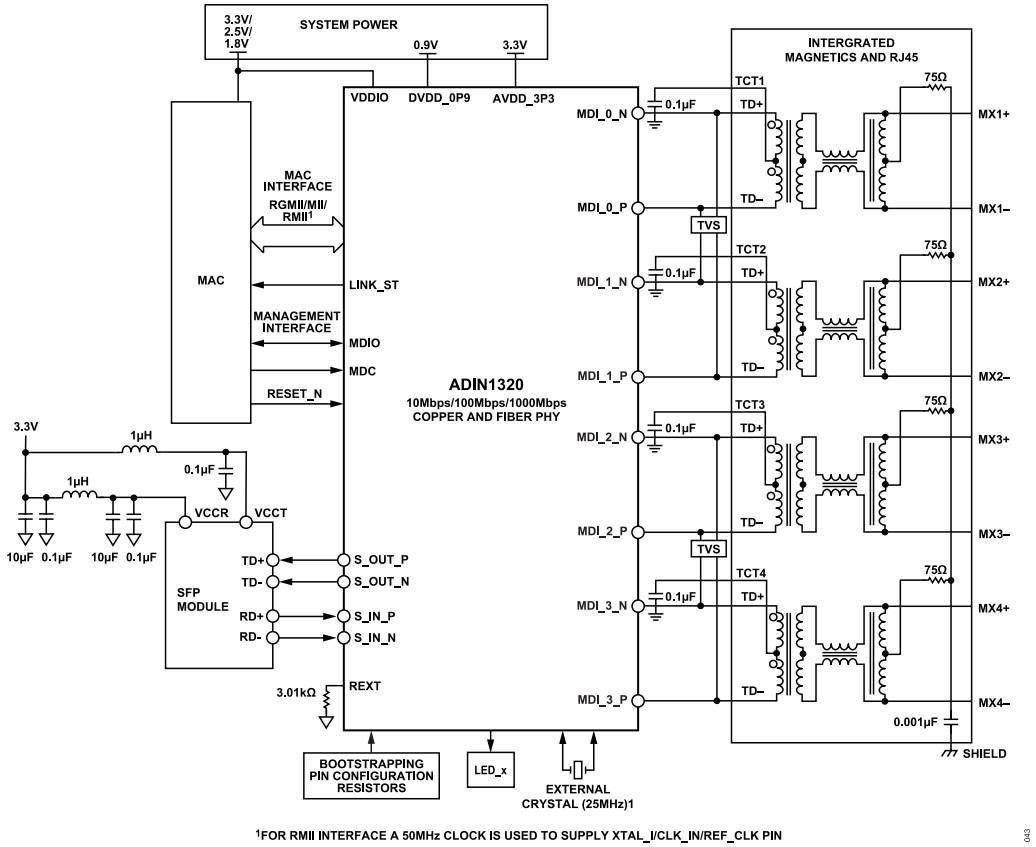


Figure 43. Simplified Typical Application Block Diagram Using an RJ45 with Integrated Magnetics

AUTO-MEDIA DETECT FOR RGMII/RMII/MII TO COPPER OR FIBER

When the MACIF_SEL[2:0] is configured to 0b100, 0b110, or 0b111, the ADIN1320 can interface with either copper or fiber. For detailed information on MACIF_SEL[2:0] pins, refer to the MAC Interface and Functional Mode Selectionsection.

In these operational modes, the ADIN1320 awaits valid link or autonegotiation signaling from both the copper PHY and fiber PHY. The selection of RGMII (or RMII/MII) to copper or fiber is based on which interface first provides valid signaling. The selected media remains active until no activity is detected, at which point the other media PHY enters power-down mode. If activity in the selected media ceases and the other media PHY detects activity first, it becomes the new active media. For example, if copper is initially selected and becomes active, the fiber PHY enters power-down mode. However, if copper activity ceases and the fiber interface detects activity before copper, fiber then becomes the active interface. This feature ensures efficient power management and optimal performance.

LOW POWER TERMINATION IN 100BASE-TX

In 100BASE-TX, the PHY transmits on one pair and receives on the other, and the default setting for 100BASE-TX operation is for normal termination on the receive dimension, which consumes the lowest power. The PHY can be configured for lowest common-mode impedance on the receive pair by clearing the B_100_ZPTM_EN_DIMRX bit. There is a trade-off of 12 mW increased power consumption with lowest common-mode impedance setting. In all cases, the differential impedance is 100 Ω. Use the lowest common-mode impedance setting for capacitive coupled applications and other applications where there may be a path for high common-mode noise to reach the PHY.

RGMII TO 1000BASE-KX (BACKPLANE)

The ADIN1320 can be set up for RGMII to 1000BASE-KX or backplane over a one meter trace. For detailed instructions on how to configure the ADIN1320, refer to the PHY Configuration section, which provides comprehensive guidance on the configuration process.

MEDIA CONVERTER MODE

The ADIN1320 can be configured in a copper/fiber media converter mode. This mode enables the translation of data between the copper and fiber interfaces. The device can be set to operate in either 1000BASE-T to 1000BASE-X or 100BASE-TX to 100BASE-FX mode. This configuration is achieved by setting the MAC_SEL[2:0] pins to 0b101.

APPLICATIONS INFORMATION

The PHY_CFG[1:0] pins must be set according to Table 28. Table 28 provides detailed instructions on how to configure the PHY_CFG[1:0] pins for the desired mode of operation.

SGMII-RGMII BRIDGE MODES

The ADIN1320 supports an SGMII-RGMII bridge mode for data translation between SGMII and RGMII MAC interfaces. This bridge mode is enabled by configuring the MACIF_SEL[2:0] and PHY_CFG[1:0] pins as specified in Table 28. When bridge mode is active, the LED_2/GP_CLK/MDIX_MODE pin sets the SGMII-RGMII bridge type according to Table 30.

In RGMII-to-SGMII bridge mode, the ADIN1320 RGMII interface automatically adjusts to the link configuration of the SGMII interface, synchronizing the MAC and PHY. Link parameters are received from the PHY over the SGMII interface and conveyed to the MAC via RGMII in-band signaling. When the PHY link is active, the RGMII receive clock (RXC) matches the PHY link speed; if the PHY link is down, the RGMII clock frequency defaults to 2.5MHz. In this mode, the ADIN1320 RGMII pins connect to an Ethernet MAC, while the SGMII pins connect to a PHY.

In SGMII-to-RGMII mode, the SGMII side adjusts the link configuration based on information received from the RGMII side. An Ethernet MAC connects to the SGMII pins of the ADIN1320, while an external PHY connects to the ADIN1320 RGMII pins in a back to back configuration. The PHY link configuration, received over the RGMII interface via in-band signaling, is conveyed to the MAC through the SGMII interface to enable adaptive link speed alignment between interfaces.

PHY BACK TO BACK CONNECTION

Some applications require extending cable reach beyond standard Ethernet lengths. This can be achieved by configuring an ADIN1320 PHY for back to back connection with an external PHY, connecting the TX pins of the MAC interface on each PHY to the RX pins on the other. Note that a back to back PHY connection does not function as a repeater and lacks collision handling; therefore, both PHYs must operate in full duplex mode.

RGMII Back to Back

The ADIN1320 RGMII interface supports back to back configuration without any modification required. Connect the receive outputs from one PHY across to the transmit inputs of the other PHY to achieve this. Configure the RGMII interface with internal delay on just one side, typically the receive side only for each PHY. The internal delay can be configured using hardware strapping, or alternatively by writing over the MDIO interface to Register GE_RGMII_CFG, Bit GE_RGMII_TX_ID_EN = 0 and Bit GE_RGMII_RX_ID_EN = 1.

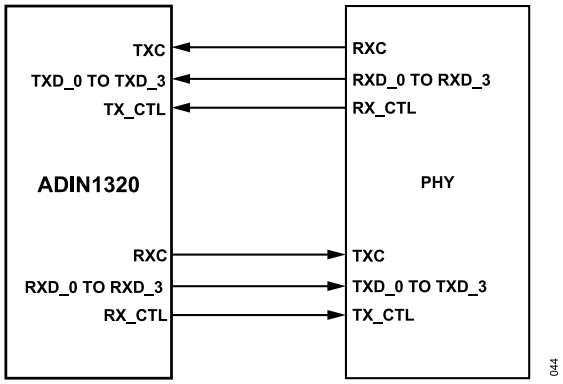


Figure 44. RGMII Configuration for Repeater/Back to Back Mode

RMII Back to Back

The RMII receive and transmit interfaces are not functionally compatible for direct RMII back to back connections per the RMII specification. This is due to the CRS_DV signal outputting both CRS and RX_DV, which prevents a direct connection to TX_EN . To enable a back to back RMII connection between PHYs, the CRS_DV must be configured to output only RX_DV and/or the TX_EN must be configured to ignore the CRS signal and decode only RX_DV.

The ADIN1320 supports both configuration options. To connect the CRS_DV of the ADIN1320 to the TX_EN of an external PHY, set GE_RMII_CRS_EN to 0 in the GE_RMII_CFG register. This disables CRS encoding, allowing CRS_DV to function as RX_DV, which now can be connected directly to TX_EN of an external PHY.

If the external PHY does not support the same CRS_DV configuration, setting the GE_RMII_TXD_CHK_EN to 1 enables the TX_EN of the ADIN1320 to decode the CRS_DV signal from the external PHY and only extract the RX_DV signal while ignoring the CRS signal.

These configurations ensure compatibility for back to back RMII connections using the ADIN1320.

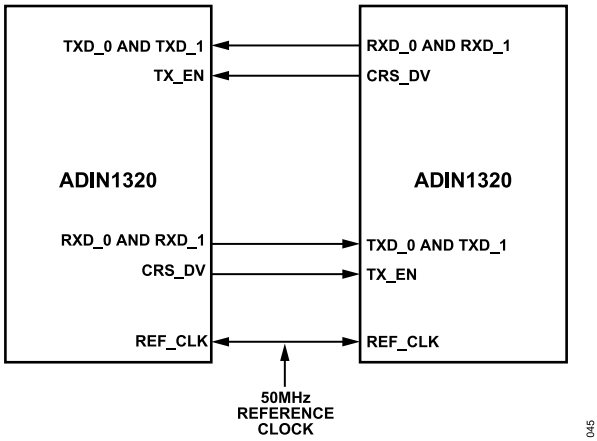


Figure 45. Back to Back with RMII Interface

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Back to Back Connection in 10BASE-T

In 10BASE-T mode and with any of the MAC interfaces, the 10BASE-T receiver can remove several preamble bits so that the receiver data can have <7 preamble bytes. This removal can cause problems for the remote end receiving the frame. To avoid any issues, the 10BASE-T receive preamble regeneration must be enabled by setting the GE_B10_REGEN_PRE register (Address 0xFF38) to 0x1. The GE_B10_REGEN_PRE is set to 0x1 by default when the ADIN1320 is configured via hardware configuration pins for 10BASE-T full-duplex mode, enabling 10BASE-T back to back operation in fully unmanaged modes.

BACK TO BACK MODE WITH EXTERNAL PHY

The ADIN1320 supports a back to back mode for connections from the copper PHY to an external PHY device. This external PHY can be any 10, 100, or 1000 Mbit/s PHY, including multi speed SGMII PHYs or SFP modules. The ADIN1320 can be configured for back-to-back connection with the external PHY via RGMII or SGMII interface using hardware configuration pins; refer to PHY Configuration section for details.

This mode facilitates the integration of newer PHY technologies with existing 10BASE-T, 100BASE-TX, and 1000BASE-T ports in legacy switches. The ADIN1320 operates as a media converter, bridging the PHY technology of the external device with supported copper PHY technologies while automatically following the link configuration of the external PHY.

In SGMII interface mode, connect the S_IN and S_OUT differential pins of the ADIN1320 to the serial differential output and input pins of the external PHY's SGMII interface. The ADIN1320 automatically adjusts to the link configuration of the external PHY via SGMII autonegotiation. When the external PHY establishes a link, the ADIN1320 restarts Clause 22 autonegotiation, advertising the same link configuration to establish a link (10BASE-T, 100BASE-TX, or 1000BASE-T) with matching speed, full duplex, and EEE configuration. If the external PHY does not have a link, the copper PHY in the ADIN1320 enters power-down mode to conserve energy.

In RGMII mode, connect the ADIN1320 in a standard RGMII back to back configuration. The ADIN1320 automatically adjusts to the link configuration of the external PHY through RGMII in band signaling. Upon link establishment by the external PHY, the ADIN1320 restarts Clause 22 autonegotiation, advertising the same link configuration to establish a link (10BASE-T, 100BASE-TX, or 1000BASE-T) with matching speed and full duplex. Note that EEE configuration is not communicated through RGMII in band signaling. If the external PHY does not establish a link, the copper PHY in the ADIN1320 enters power-down mode to save power.

RGMII TIMING EXAMPLES

The ADIN1320 RGMII timing parameters comply with the RGMII v2.0 standard, supporting both internal delay mode and legacy configurations that use external trace delays, although external delays are now less common.

In internal delay mode, each interface (MAC or PHY) applies a delay to the clock it sources. When operating as a PHY, the ADIN1320 delays its internally generated RXC, while the MAC delays TXC. The ADIN1320 can also be configured to delay both RXC and TXC. This feature is particularly useful when interfacing with MACs or microcontrollers that lack an internal DLL, allowing the PHY to handle both RXC and TXC delays internally to ensure accurate timing.

When the ADIN1320 is configured as a MAC, it can delay RXC (the ADIN1320 output) alone or both RXC and TXC, depending on the requirements.

Delay values for RXC and TXC are adjustable from 1.6ns to 2.4ns via the GE_RGMII_CFG register, ensuring compatibility across a wide range of configurations Figure 46 to Figure 48 show examples of RGMII timing for different modes of operation and speeds.

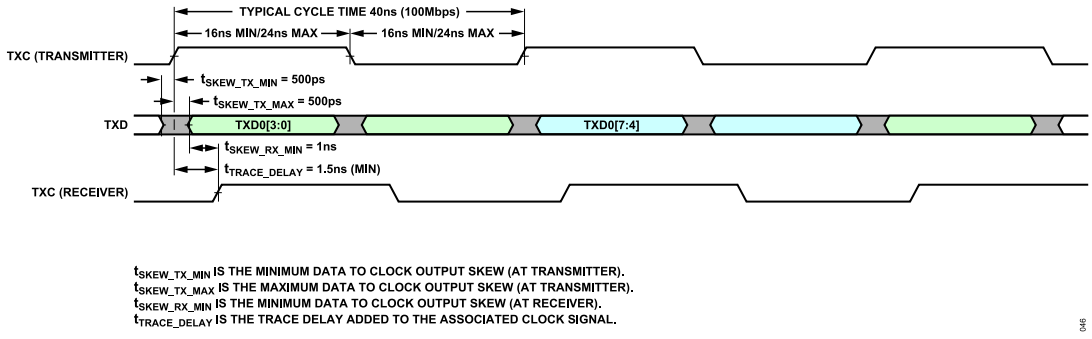


Figure 46. RGMII Timing Example for 100Mbps Data Rate (Using PCB Trace Delay)

APPLICATIONS INFORMATION

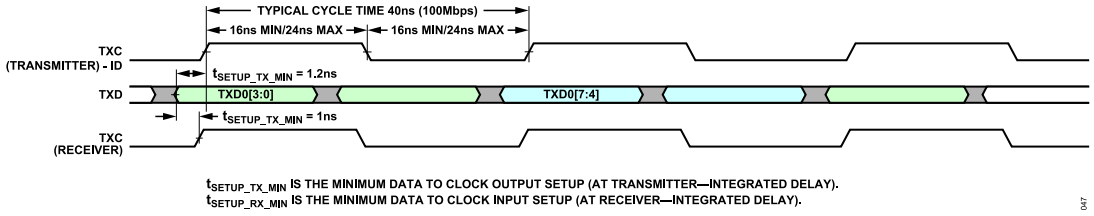


Figure 47. RGMII Timing Example for 100Mbps Data Rate, with Internal Delay Enabled

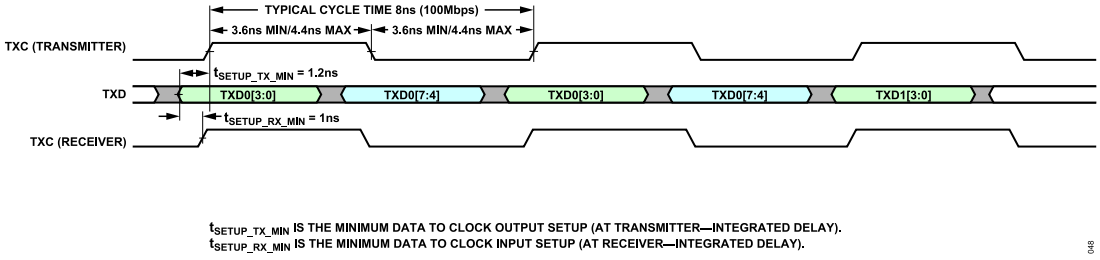


Figure 48. RGMII Timing Example for 1000Mbps Data Rate, with Internal Delay Enabled

APPLICATIONS INFORMATION

COMPONENT RECOMMENDATIONS

Crystal

The typical connection for an external crystal (XTAL) is shown in Figure 49. To ensure minimum current consumption and to minimize stray capacitances, make connections between the crystal, capacitors, and ground as close to the ADIN1320 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

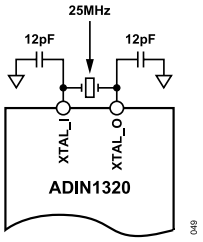


Figure 49. Crystal Oscillator Connection

External Clock Input

If using a single-ended reference clock on XTAL_I/CLK_IN/REF_CLK, leave XTAL_O open-circuit. The clock can be a unipolar 1.8V/ 2.5V/3.3V, 25MHz sine wave, or square wave signal. When using the RMII MAC interface, a single, 50MHz reference clock (REF_CLK) is required, which can be sourced from the MAC or from an external source.

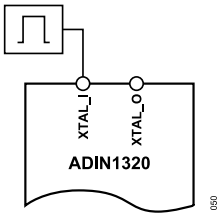


Figure 50. External Clock Connection

Magnetics

Galvanic isolation is necessary between any two point-to-point communication nodes in applications using the Ethernet protocol to transmit/receive data to protect against faults and transients, and achieve the best electromagnetic compatibility performance. Magnetic coupling between the PHY and the RJ45 is the most common way of achieving this isolation.

The magnetics can be discrete or integrated and there are strengths and weaknesses to both. Choosing the discrete option typically occupies more board space, but gives more freedom in terms of layout, tends to be cheaper than integrated magnetics, and offers better performance overall.

The integrated approach is a combined RJ45 connector jack with the magnetics built in, which provides a more compact solution due to fewer components and, in applications where space is at a premium, condenses the required footprint, but tends to cost more. Magnetics cores tend to be smaller and closer to each other, which can compromise EMC performance, increase the likelihood of crosstalk, and have impacts on performance by increasing losses and introducing nonlinear distortion.

For optimum performance, a discrete transformer with integrated common-mode choke is recommended for use with the ADIN1320 PHY. The common-mode choke is important because it attenuates any common-mode signals picked up by the twisted pair cable from the environment, improving the signal-to-noise ratio of the system. Transformers with an autotransformer stage following the common-mode choke provide additional attenuation of common-mode noise. Not all transformers include an autotransformer stage, integrated RJ45s that have the magnetics included tend to have fewer cores and therefore no autotransformer.

The ADIN1320 transmit drivers are voltage mode with on-chip terminations. Therefore, connect each of the center tap pins on the transformer on the ADIN1320 side separately to ground through a 0.1 µF capacitor.

The key considerations for the magnetics are outlined in Table 35.

Table 35. Magnetics Selection

Parameter	Value	Conditions
Turns Ratio	1CT:1CT	
Open-Circuit Inductance	350 µH	Min: 100 mV, 100 kHz, 8 mA
Insertion loss	−1 dB	Max: 0 MHz to 100 MHz

MDI ESD Protection

As shown in Figure 42, a transient voltage suppressor (TVS) diode is recommended in the MDI path.

MDI Capacitive Coupling

Typically, Ethernet applications use galvanic isolation in the form of magnetics between link partners as shown in Figure 42 and Figure 43. Some applications may need to provide isolation through capacitive coupling instead of using magnetics. The ADIN1320 can support capacitive coupling for short cable distances or backplane applications. Include a TVS diode on the MDI pairs for protection against ESD, transients, and surges. If cable length is longer than 1 meter, a common-mode choke is also recommended to minimize induced common-mode noise. Set the B_100_ZPTM_EN_DIMRX bit to zero to disable zero-power termination mode and enable active termination.

APPLICATIONS INFORMATION

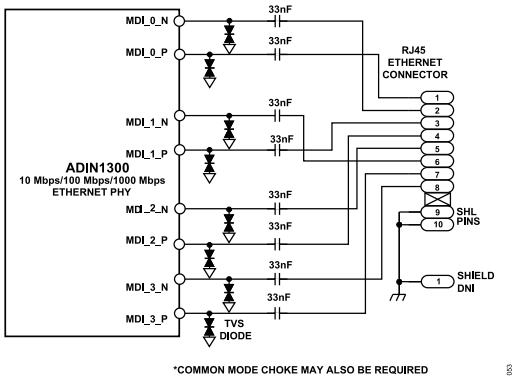


Figure 51. Media Dependent Interface Using Capacitive Coupling

Small Form Factor Pluggable (SFP)

The integration of the SFP module with SGMII pins is a critical component in the architecture of contemporary network devices, facilitating rapid data transfer and diverse connectivity options. The ADIN1320 is capable of supporting Gigabit Ethernet with this interface, offering data rates of 1.25Gbps. It is designed to work with a variety of SFP transceivers, including both optical and copper modules, and adheres to the standard SFP MSA (Multi Source Agreement) compliant modules. The SGMII interface employs differential signaling with AC coupling and is compatible with 1000BASE-X and 100BASE-FX for Ethernet communication, including the ability to auto-negotiate speed and duplex modes. The electrical specifications include an operating voltage of 3.3V ± 5% and a typical power consumption of less than 1W, which can vary depending on the SFP module. The connectors used include LC connectors for fiber optic modules and RJ-45 connectors for copper modules.

The SGMII pins interact with the SFP module to send and receive high-speed serial data, transforming it into the suitable format for transmission over optical fiber or copper cables. When choosing SFP modules, it's crucial to take into account factors such as data rate, signal travel distance, environmental conditions like temperature and humidity, and compatibility with network devices. It is also important to verify that the power consumption is within the host system's power budget.

In terms of board design, it's important to maintain signal integrity by adhering to high-speed design practices, using differential pairs for SGMII signals, and positioning the SFP module near the associated PHY to reduce trace lengths and signal degradation. Proper power supply decoupling with low ESR capacitors and sufficient thermal management, such as the use of heatsinks and thermal vias, are also vital. Mechanical considerations include ensuring the SFP cage is properly aligned and securely mounted on the PCB, and that it has enough support to withstand insertion and removal cycles. Testing and validation through simulation and practical testing are required to ensure signal integrity and reliable operation with different SFP modules.

SUPPLY DECOUPLING

It is recommended to decouple each of the AVDD_3P3, VDDIO, and DVDD_0P9 supply pins with 0.1µF in parallel with 0.01µF capacitors to ground. Place decoupling capacitors as close to the relevant pins as possible and ensure that the capacitor ground is routed directly into the plane.

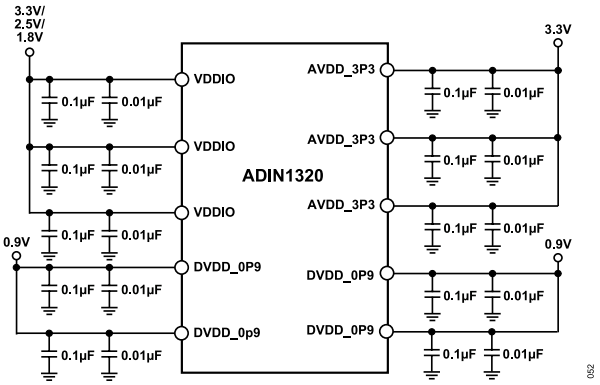


Figure 52. Supply Decoupling Overview

REGISTER SUMMARY

The MII management interface provides a 2-wire serial interface between a host processor or MAC and the ADIN1320 allowing access to control and status information in the Copper PHY core, SerDes Subsystem, and GE Subsystem management registers. The interface is compatible with both IEEE Standard 802.3 Clause 22 and Clause 45 management frame structures.

The device supplements the registers specified in IEEE Standard 802.3 with an additional set of registers that are accessed indirectly. These registers are referred to as extended management interface (EMI) registers. The EMI registers can be accessed using the interface specified under Clause 45. However, for systems that do not support this interface, an alternative access mechanism is provided using the interface specified under Clause 22.

The Copper PHY registers are accessible only when the Copper PHY is active, and similarly, SerDes Subsystem registers are accessible only when the SerDes Subsystem is active. In configurations where both subsystems are active simultaneously, the SerDes Subsystem's IEEE standard and vendor-specific registers are offset by 0xFC00 to ensure proper address mapping and avoid conflicts. The Copper PHY Core Register Summary, SerDes Subsystem Register Summary, and the GE Subsystem Register Summary sections list the ADIN1320 registers.

The access permissions of the registers are as follows:

- R/W: read/write
- R: read only
- R LL: read only, latch low
- R LH: read only, latch high
- R/W SC: read/write, self clear
- R SC: read only, self clear
- R LH SC: read only, latch high, self clear

COPPER PHY CORE REGISTER SUMMARY

The PHY core registers are made up of the following three register groupings:

- 0x0000 to 0x000F, IEEE standard registers
- 0x0010 to 0x001F, vendor specific registers
- Copper PHY core EMI registers at Device Address 0x1E

The IEEE standard registers and vendor specific registers are accessed using Clause 22 access, and the EMI registers are accessed using Clause 45 access. The ADIN1320 supports the IEEE Clause 45 MDIO manageable device (MMD) registers associated with EEE. These registers are all remapped to the Device Address 0x1E, so they are available at the same device address as the rest of the PHY extended management registers. For systems that do not support the interface specified under Clause 45, the EMI registers can be accessed using Clause 22 access via Register 0x0010 and Register 0x0011. Note that copper PHY core registers are only accessible in SGMII to Copper, RGMII/RMII/MII to Copper, and Media Converter modes.

The default value of some of the registers are determined by the value of the hardware configuration pins, which are read just after the RESET_N pin is deasserted (see the Hardware Configuration Pins section). This allows the default operation of the ADIN1320 to be configured in unmanaged applications. The default values in Table 36 assume the ADIN1320 is configured as follows:

- RGMII to Copper Mode
- All speeds advertised (prefer follower at 1000BASE-T)
- Autonegotiation enabled
- Auto MDIX, prefer MDI
- EEE, energy detect power-down, and downspeed disabled
- ADIN1320 is not configured to enter software power-down after reset

Table 36. MDIOMAP_GEPHY Register Summary

Register Address	Name	Description	Reset	Access
0x0000	MII_CONTROL	MII Control Register.	0x1040	R/W
0x0001	MII_STATUS	MII Status Register.	0x7949	R
0x0002	PHY_ID_1	PHY Identifier 1 Register.	0x0283	R
0x0003	PHY_ID_2	PHY Identifier 2 Register.	0xBC60	R
0x0004	AUTONEG_ADV	Autonegotiation Advertisement Register.	0x01E1	R/W
0x0005	LP_ABILITY	Autonegotiation Link Partner Base Page Ability Register.	0x0000	R
0x0006	AUTONEG_EXP	Autonegotiation Expansion Register.	0x0064	R
0x0007	TX_NEXT_PAGE	Autonegotiation Next Page Transmit Register.	0x2001	R/W
0x0008	LP_RX_NEXT_PAGE	Autonegotiation Link Partner Received Next Page Register.	0x0000	R
0x0009	MSTR_SLV_CONTROL	Leader Follower Control Register.	0x2000	R/W
0x000A	MSTR_SLV_STATUS	Leader Follower Status Register.	0x0000	R
0x000F	EXT_STATUS	Extended Status Register.	0x3000	R
0x0010	EXT_REG_PTR	Extended Register Pointer Register.	0x0000	R/W

REGISTER SUMMARY

Table 36. MDIOMAP_GEPHY Register Summary (Continued)

Register Address	Name	Description	Reset	Access
0x0011	EXT_REG_DATA	Extended Register Data Register.	0x0000	R/W
0x0012	PHY_CTRL_1	PHY Control 1 Register.	0x0002	R/W
0x0013	PHY_CTRL_STATUS_1	PHY Control Status 1 Register.	0x1041	R/W
0x0014	RX_ERR_CNT	Receive Error Count Register.	0x0000	R
0x0015	PHY_CTRL_STATUS_2	PHY Control Status 2 Register.	0x0000	R/W
0x0016	PHY_CTRL_2	PHY Control 2 Register.	0x0308	R/W
0x0017	PHY_CTRL_3	PHY Control 3 Register.	0x3048	R/W
0x0018	IRQ_MASK	Interrupt Mask Register.	0x0000	R/W
0x0019	IRQ_STATUS	Interrupt Status Register.	0x0000	R
0x001A	PHY_STATUS_1	PHY Status 1 Register.	0x0300	R
0x001B	LED_CTRL_1	LED Control 1 Register.	0x0001	R/W
0x001C	LED_CTRL_2	LED Control 2 Register.	0x210A	R/W
0x001D	LED_CTRL_3	LED Control 3 Register.	0x1855	R/W
0x001F	PHY_STATUS_2	PHY Status 2 Register.	0x03FC	R
0x8000	EEE_CAPABILITY	Energy Efficient Ethernet Capability Register.	0x0006	R
0x8001	EEE_ADV	Energy Efficient Ethernet Advertisement Register.	0x0000	R/W
0x8002	EEE_LP_ABILITY	Energy Efficient Ethernet Link Partner Ability Register.	0x0000	R
0x8008	EEE_RSLVD	Energy Efficient Ethernet Resolved Register.	0x0000	R
0x8402	MSE_A	Mean Square Error A Register.	0x0000	R
0x8403	MSE_B	Mean Square Error B Register.	0x0000	R
0x8404	MSE_C	Mean Square Error C Register.	0x0000	R
0x8405	MSE_D	Mean Square Error D Register.	0x0000	R
0x8E27	FLD_EN	Enhanced Link Detection Enable Register.	0x003D	R/W
0x8E38	FLD_STAT_LAT	Enhanced Link Detection Latched Status Register.	0x0000	R
0x9400	RX_MII_CLK_STOP_EN	Receive MII Clock Stop Enable Register.	0x0400	R/W
0x9401	PCS_STATUS_1	Physical Coding Sublayer (PCS) Status 1 Register.	0x0040	R
0x9403	FC_EN	Frame Checker Enable Register.	0x0001	R/W
0x9405	FC_IRQ_EN	Frame Checker Interrupt Enable Register.	0x0001	R/W
0x9406	FC_TX_SEL	Frame Checker Transmit Select Register.	0x0000	R/W
0x940D	FC_MAX_FRM_SIZE	Frame Checker Max Frame Size Register.	0x05F2	R/W
0x9410	FC_FRM_CNT_H	Frame Checker Count High Register.	0x0000	R
0x9411	FC_FRM_CNT_L	Frame Checker Count Low Register.	0x0000	R
0x9412	FC_ALGN_ERR_CNT	Frame Checker Alignment Error Count Register.	0x0000	R
0x9414	FC_SYMB_ERR_CNT	Frame Checker Symbol Error Counter Register.	0x0000	R
0x9415	FC_LEN_ERR_CNT	Frame Checker Length Error Count Register.	0x0000	R
0x9416	FC_USZ_CNT	Frame Checker Undersized Frame Count Register.	0x0000	R
0x9417	FC_OSZ_CNT	Frame Checker Oversized Frame Count Register.	0x0000	R
0x9418	FC_ODD_PRE_CNT	Frame Checker Odd Preamble Packet Count Register.	0x0000	R
0x941A	FC_DRIBBLE_BITS_CNT	Frame Checker Dribble Bits Frame Count Register.	0x0000	R
0x941B	FC_FALSE_CARRIER_CNT	Frame Checker False Carrier Count Register.	0x0000	R
0x9422	FG_EN	Frame Generator Enable Register.	0x0000	R/W
0x9423	FG_CNTRL_RSTRT	Frame Generator Control and Restart Register.	0x0001	R/W
0x9424	FG_CONT_MODE_EN	Frame Generator Continuous Mode Enable Register.	0x0000	R/W
0x9425	FG_IRQ_EN	Frame Generator Interrupt Enable Register.	0x0000	R/W
0x9427	FG_FRM_LEN	Frame Generator Frame Length Register.	0x006B	R/W
0x9428	FG_IFG_LEN	Frame Generator Interframe Gap Register.	0x000C	R/W
0x9429	FG_NFRM_H	Frame Generator Number of Frames High Register.	0x0000	R/W

REGISTER SUMMARY

Table 36. MDIOMAP_GEPHY Register Summary (Continued)

Register Address	Name	Description	Reset	Access
0x942A	FG_NFRM_L	Frame Generator Number of Frames Low Register.	0x0100	R/W
0x942B	FG_DONE	Frame Generator Done Register.	0x0000	R
0x944B	FIFO_SYNC	FIFO_SYNC Register.	0x0000	R/W
0x944C	SOP_CTRL	Start of Packet Control Register.	0x0034	R/W
0x944D	SOP_RX_DEL	Start of Packet Receive Detection Delay Register.	0x0000	R/W
0x944E	SOP_TX_DEL	Start of Packet Transmit Detection Delay Register.	0x0000	R/W
0x9602	DPTH_MII_BYTE	Control of FIFO Depth for MII Modes Register.	0x0001	R/W
0xA000	LPI_WAKE_ERR_CNT	LPI Wake Error Count Register.	0x0000	R
0xA001	B_1000_RTRN_EN	Base 1000 Retrain Enable Register.	0x0000	R/W
0xB403	B_10_E_EN	Base 10e Enable Register.	0x0001	R/W
0xB412	B_10_TX_TST_MODE	10BASE-T Transmit Test Mode Register.	0x0000	R/W
0xB413	B_100_TX_TST_MODE	100BASE-TX Transmit Test Mode Register.	0x0000	R/W
0xB685	B_100_ZPTM_EN_DIMRX	Low power termination for receive dimension 100BASE-TX Register	0x0001	R/W
0xBA1B	CDIAG_RUN	Run Automated Cable Diagnostics Register.	0x0000	R/W
0xBA1C	CDIAG_XPAIR_DIS	Cable Diagnostics Cross Pair Fault Checking Disable Register.	0x0000	R/W
0xBA1D	CDIAG_DTLD_RSLTS_0	Cable Diagnostics Results 0 Register.	0x0000	R
0xBA1E	CDIAG_DTLD_RSLTS_1	Cable Diagnostics Results 1 Register.	0x0000	R
0xBA1F	CDIAG_DTLD_RSLTS_2	Cable Diagnostics Results 2 Register.	0x0000	R
0xBA20	CDIAG_DTLD_RSLTS_3	Cable Diagnostics Results 3 Register.	0x0000	R
0xBA21	CDIAG_FLT_DIST_0	Cable Diagnostics Fault Distance Pair 0 Register.	0x00FF	R
0xBA22	CDIAG_FLT_DIST_1	Cable Diagnostics Fault Distance Pair 1 Register.	0x00FF	R
0xBA23	CDIAG_FLT_DIST_2	Cable Diagnostics Fault Distance Pair 2 Register.	0x00FF	R
0xBA24	CDIAG_FLT_DIST_3	Cable Diagnostics Fault Distance Pair 3 Register.	0x00FF	R
0xBA25	CDIAG_CBL_LEN_EST	Cable Diagnostics Cable Length Estimate Register.	0x00FF	R
0xBC00	LED_PUL_STR_DUR	LED Pulse Stretching Duration Register.	0x0011	R/W

COPPER PHY CORE REGISTER DETAILS

MII Control Register

Register Address: 0x0000, Reset: 0x1040, Name: MII_CONTROL

This address corresponds to the MII control register specified in clause 22.2.4.1 of Std 802.3. Note that the default reset value of this register is dependent on hardware configuration pins settings.

Table 37. Bit Descriptions for MII_CONTROL

Bits	Bit Name	Description	Reset	Access
15	SFT_RST	Software Reset Bit. Note that this bit is self-clearing. When the reset operation is complete, this bit returns to 1'b0. 1: PHY reset. 0: normal operation.	0x0	R/W
14	LOOPBACK	Enable/Disable Loopback Mode. 1: enable loopback mode. 0: disable loopback mode.	0x0	R/W
13	SPEED_SEL_LSB	The speed selection MSB and LSB register bits are used to configure the link speed. Note that the default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 11: reserved. 10: 1000Mb/s 01: 100Mb/s 00: 10Mb/s	0x0	R/W

REGISTER SUMMARY

Table 37. Bit Descriptions for MII_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
12	AUTONEG_EN	The autonegotiation enable bit is used to enable/disable autonegotiation. Note that the default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable autonegotiation process. 0: disable autonegotiation process.	0x1	R/W
11	SFT_PD	Software Power-Down Bit. Note that the default value of this register bit is configurable via the hardware configuration pins. The PHY can be held in reset until initialized by the software. 1: software power-down. 0: normal operation.	0x0	R/W
10	ISOLATE	Isolate Bit. 1: electrically isolate PHY from MAC interface by setting MAC interface pins to tristate (even if active). 0: normal operation	0x0	R/W
9	RESTART_ANEG	Restart Autonegotiation Bit. Note that this bit is self-clearing. When the autonegotiation process is restarted, this bit returns to 1'b0. 1: restart the autonegotiation process. 0: normal operation.	0x0	R/W SC
8	DPLX_MODE	Duplex Mode Bit. 1: full duplex. 0: half duplex.	0x0	R/W
7	COLTEST	Collision Test Bit. 1: enable collision signal test. 0: disable collision signal test.	0x0	R/W
6	SPEED_SEL_MSB	See SPEED_SEL_LSB Bit Description. 11: reserved. 10: 1000Mb/s 01: 100Mb/s 00: 10Mb/s	0x1	R/W
5	UNIDIR_EN	The unidirectional enable bit cannot be written and always reads as 1'b0 since the PHY does not have the ability to transmit data from the MII regardless of whether or not it has determined that a valid link has been established.	0x0	R
[4:0]	RESERVED	Reserved.	0x0	R

MII Status Register

Register Address: 0x0001, Reset: 0x7949, Name: MII_STATUS

This address corresponds to the MII status register specified in clause 22.2.4.2 of Std 802.3.

Table 38. Bit Descriptions for MII_STATUS

Bits	Bit Name	Description	Reset	Access
15	T_4_SPRT	The 100BASE-T4 ability bit always reads as 1'b0 because the PHY does not support 100BASE-T4.	0x0	R
14	FD_100_SPRT	The 100BASE-TX full duplex ability bit always reads as 1'b1 because the PHY supports 100BASE-TX full duplex.	0x1	R
13	HD_100_SPRT	The 100BASE-TX half duplex ability bit always reads as 1'b1 because the PHY supports 100BASE-TX half duplex.	0x1	R
12	FD_10_SPRT	The 10BASE-T full duplex ability bit always reads as 1'b1 because the PHY supports 10BASE-T full duplex.	0x1	R
11	HD_10_SPRT	The 10BASE-T half duplex ability bit always reads as 1'b1 because the PHY supports 10BASE-T half duplex.	0x1	R
10	FD_T_2_SPRT	The 100BASE-T2 full duplex ability bit always reads as 1'b0 because the PHY does not support 100BASE-T2.	0x0	R
9	HD_T_2_SPRT	The 100BASE-T2 half-duplex ability bit always reads as 1'b0 because the PHY does not support 100BASE-T2.	0x0	R

REGISTER SUMMARY

Table 38. Bit Descriptions for MII_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
8	EXT_STAT_SPRT	The extended status support bit always reads as 1'b1, indicating that the PHY provides extended status information in Register 0x000F.	0x1	R
7	UNIDIR_ABLE	When zero, the unidirectional ability register bit indicates that the PHY can only transmit data from the media independent interface when it has determined that a valid link has been established. This bit always reads as 1'b0.	0x0	R
6	MF_PREAM_SUP_ABLE	Management Frame Preamble Suppression Ability Bit. This always reads as 1'b1 because the PHY accepts management frames with preamble suppressed.	0x1	R
5	AUTONEG_DONE	Autonegotiation Complete Bit. 1: autonegotiation process completed. 0: autonegotiation process not completed.	0x0	R
4	REM_FLT_LAT	Remote Fault Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: remote fault condition detected.0: no remote fault condition detected.	0x0	R LH
3	AUTONEG_ABLE	Autonegotiation Ability Bit. This bit always reads as 1'b1. 1: PHY is able to perform autonegotiation. 0: PHY is not able to perform autonegotiation.	0x1	R
2	LINK_STAT_LAT	Link Status Bit. If the link subsequently drops, this bit latches low until it is unlatched by reading. 1: link is up 0: link is down.	0x0	R LL
1	JABBER_DET_LAT	Jabber Detect Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: jabber condition detected 0: no jabber condition detected.	0x0	R LH
0	EXT_CAPABLE	The extended capability bit always reads as 1'b1 because the PHY provides an extended set of capabilities	0x1	R

PHY Identifier 1 Register

Register Address: 0x0002, Reset: 0x0283, Name: PHY_ID_1

This address corresponds to the MII status register specified in Clause 22.2.4.3.1 of IEEE Standard 802.3 and allows 16 bits of the organizationally unique identifier (OUI) to be observed.

Table 39. Bit Descriptions for PHY_ID_1

Bits	Bit Name	Description	Reset	Access
[15:0]	PHY_ID_1	PHY Identifier 1. Organizationally Unique Identifier Bits [3:18].	0x283	R

PHY Identifier 2 Register

Register Address: 0x0003, Reset: 0xBC60, Name: PHY_ID_2

This address corresponds to the MII status register specified in Clause 22.2.4.3.1 of IEEE Standard 802.3 and allows 6 bits of the OUI along with the model number and revision number to be observed.

Table 40. Bit Descriptions for PHY_ID_2

Bits	Bit Name	Description	Reset	Access
[15:10]	PHY_ID_2OUI	PHY Identifier 2. Organizationally Unique Identifier Bits [19:24].	0x2F	R
[9:4]	MODEL_NUM	Manufacturer's Model Number.	0x6	R
[3:0]	REV_NUM	Manufacturer's Revision Number.	0x0	R

Autonegotiation Advertisement Register

Register Address: 0x0004, Reset: 0x01E1, Name: AUTONEG_ADV

This address corresponds to the autonegotiation advertisement register specified in Clause 28.2.4.1.3 of IEEE Standard 802.3. Note that the default reset value of this register is dependent on the hardware configuration pins settings.

REGISTER SUMMARY

Table 41. Bit Descriptions for AUTONEG_ADV

Bits	Bit Name	Description	Reset	Access
15	NEXT_PAGE_ADV	Next Page Exchange Bit. Next page exchange occurs after the base link codewords have been exchanged. Next page exchange consists of using the normal autonegotiation arbitration process to send next page messages. Next page transmission ends when both ends of a link segment set their next page bits to Logic 0, indicating that neither has anything additional to transmit.	0x0	R/W
14	RESERVED	Reserved.	0x0	R
13	REM_FLT_ADV	Remote Fault Bit. The remote fault bit provides a standard transport mechanism for the transmission of simple fault information.	0x0	R/W
12	EXT_NEXT_PAGE_ADV	Extended Next Page Bit. The extended next page bit indicates that the local device supports transmission of extended next pages. The use of extended next page is orthogonal to the negotiated data rate, medium, or link technology.	0x0	R/W
11	APAUSE_ADV	Asymmetric Pause Advertise Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise asymmetric pause operation for full duplex links.	0x0	R/W
10	PAUSE_ADV	Pause Advertise Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise pause operation for full duplex links.	0x0	R/W
9	T_4_ADV	100BASE-T4 Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-T4 and always reads as 1'b0 because this technology is not supported.	0x0	R
8	FD_100_ADV	100BASE-TX FD Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-TX full duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
7	HD_100_ADV	100BASE-TX HD Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-TX half duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
6	FD_10_ADV	10BASE-T FD Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 10BASE-T full duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
5	HD_10_ADV	10BASE-T HD Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 10BASE-T half duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
[4:0]	SELECTOR_ADV	Selector Field. Selector field is a 5-bit wide field, encoding 32 possible messages. This field always reads as 1'b1, indicating that the PHY only supports IEEE Standard 802.3.	0x1	R/W

Autonegotiation Link Partner Base Page Ability Register

Register Address: 0x0005, Reset: 0x0000, Name: LP_ABILITY

This address corresponds to the link partner ability register specified in Clause 28.2.4.1.4 of IEEE Standard 802.3.

Table 42. Bit Descriptions for LP_ABILITY

Bits	Bit Name	Description	Reset	Access
15	LP_NEXT_PAGE	Link Partner Next Page Bit. Link Partner Next Page Bit. Next page exchange occurs after the base link code words have been exchanged. Next page exchange consists of using the normal autonegotiation arbitration process to send next page messages. Next page	0x0	R

REGISTER SUMMARY

Table 42. Bit Descriptions for LP_ABILITY (Continued)

Bits	Bit Name	Description	Reset	Access
		transmission ends when both ends of a link segment set their next page bits to Logic 0, indicating that neither has anything additional to transmit.		
14	RESERVED	Reserved.	0x0	R
13	LP_REM_FLT	Link Partner Remote Fault Bit. The link partner remote fault bit provides a standard transport mechanism for the transmission of simple fault information.	0x0	R
12	LP_EXT_NEXT_PAGE_ABLE	Link Partner Extended Next Page Bit. The link partner extended next page bit indicates that the link partner supports transmission of extended next page. The use of extended next page is orthogonal to the negotiated data rate, medium, or link technology.	0x0	R
11	LP_APAUSE_ABLE	Link Partner Asymmetric Pause Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises asymmetric pause operation for full duplex links.	0x0	R
10	LP_PAUSE_ABLE	Link Partner Pause Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises pause operation for full duplex links.	0x0	R
9	LP_T_4_ABLE	Link Partner 100BASE-T4 Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 100BASE-T4.	0x0	R
8	LP_FD_100_ABLE	Link Partner 100BASE-TX FD Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 100BASE-TX full duplex.	0x0	R
7	LP_HD_100_ABLE	Link Partner 100BASE-TX HD Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 100BASE-TX half duplex.	0x0	R
6	LP_FD_10_ABLE	Link Partner 10BASE-T FD Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 10BASE-T full duplex.	0x0	R
5	LP_HD_10_ABLE	Link Partner 10BASE-T HD Advertisement Bit. The technology ability field is a 7-bit wide field (Bits [11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 100BASE-TX half duplex.	0x0	R
[4:0]	LP_SELECTOR	Link Partner Selector Field. Link Partner Selector Field. This is a 5-bit wide field, encoding 32 possible messages. The value 0x1 indicates IEEE Standard 802.3.	0x0	R

Autonegotiation Expansion Register

Register Address: 0x0006, Reset: 0x0064, Name: AUTONEG_EXP

This address corresponds to the autonegotiation expansion register specified in Clause 28.2.4.1.5 of IEEE Standard 802.3.

Table 43. Bit Descriptions for AUTONEG_EXP

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	RX_NP_LOC_ABLE	Received Next Page Location Ability Bit. The received next page location ability bit always reads as 1'b1 because received next pages are stored in Register 0x0008. 1: received next page storage location is specified by Bit 5 (RX_NP_LOC). 0: received next page storage location is not specified by Bit 5 (RX_NP_LOC).	0x1	R
5	RX_NP_LOC	Received Next Page Location. The received next page location bit always reads as 1'b1. 1: link partner next pages are stored in Register 0x0008.	0x1	R

REGISTER SUMMARY

Table 43. Bit Descriptions for AUTONEG_EXP (Continued)

Bits	Bit Name	Description	Reset	Access
		0: link partner next pages are stored in Register 0x0005.		
4	PAR_DET_FLT	Parallel Detection Fault Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: a fault has been detected via the parallel detection function. 0: a fault has not been detected via the parallel detection function.	0x0	R LH
3	LP_NP_ABLE	LP_NP_ABLELink Partner Next Page Ability Bit. 1: link partner is next page capable. 0: link partner is not next page capable.	0x0	R
2	NP_ABLE	Next Page Ability Bit. The next page ability bit always reads as 1'b1, indicating that the PHY supports next pages. 1: local device is next page capable. 0: local device is not next page capable.	0x1	R
1	PAGE_RX_LAT	Page Received Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: a new page has been received. 0: a new page has not been received.	0x0	R LH
0	LP_AUTONEG_ABLE	Link Partner Autonegotiation Ability Bit. 1: link partner is autonegotiation capable. 0: link partner is not autonegotiation capable.	0x0	R

Autonegotiation Next Page Transmit Register

Register Address: 0x0007, Reset: 0x2001, Name: TX_NEXT_PAGE

This address corresponds to the autonegotiation next page transmit register specified in Clause 28.2.4.1.6 of IEEE Standard 802.3.

Table 44. Bit Descriptions for TX_NEXT_PAGE

Bits	Bit Name	Description	Reset	Access
15	NP_NEXT_PAGE	Next page (NP) is used by the next page function to indicate that additional next page(s) follow. Otherwise, this is the last next page to be transmitted.	0x0	R/W
14	RESERVED	Reserved.	0x0	R
13	NP_MSG_PAGE	Message page (MP) is used by the next page function to indicate that this is a message page. Otherwise, this is an unformatted page.	0x1	R/W
12	NP_ACK_2	Acknowledge 2 (Ack2) is used by the next page function to indicate that a device has the ability to comply with the message.	0x0	R/W
11	NP_TOGGLE	Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit always takes the opposite value of the toggle bit in the previously exchanged link code word.	0x0	R
[10:0]	NP_CODE	Message code field is an 11-bit wide field, encoding 2048 possible messages. If the message page bit is set to Logic 0, the bit encoding of the link code word is interpreted as an unformatted page.	0x1	R/W

Autonegotiation Link Partner Received Next Page Register

Register Address: 0x0008, Reset: 0x0000, Name: LP_RX_NEXT_PAGE

This address corresponds to the autonegotiation link partner received next page register specified in Clause 28.2.4.1.7 of IEEE Standard 802.3.

Table 45. Bit Descriptions for LP_RX_NEXT_PAGE

Bits	Bit Name	Description	Reset	Access
15	LP_NP_NEXT_PAGE	Link Partner Next Page (NP). Link partner next page (NP) is used by the next page function to indicate that the link partner sends additional next page(s). Otherwise, this is the last next page to be transmitted.	0x0	R
14	RESERVED	Reserved.	0x0	R
13	LP_NP_MSG_PAGE	Link Partner Message Page (MP). Link partner message page (MP) is used by the next page function to indicate that this is a message page. Otherwise, this is an unformatted page.	0x0	R

REGISTER SUMMARY

Table 45. Bit Descriptions for LP_RX_NEXT_PAGE (Continued)

Bits	Bit Name	Description	Reset	Access
12	LP_NP_ACK_2	Link Partner Acknowledge 2 (Ack2). Acknowledge 2 (Ack2) is used by the next page function to indicate that the link partner has the ability to comply with the message.	0x0	R
11	LP_NP_TOGGLE	Link Partner Toggle (T). Link partner toggle (T) is used by the arbitration function to ensure synchronization with the link partner during the next page exchange. This bit always takes the opposite value of the toggle bit in the previously exchanged link code word.	0x0	R
[10:0]	LP_NP_CODE	Link Partner Message Code Field. Link partner message code field is an 11-bit wide field, encoding 2048 possible messages. If the message page bit is set to Logic 0, the bit encoding of the link code word is interpreted as an unformatted page.	0x0	R

Leader Follower Control Register

Register Address: 0x0009, Reset: 0x0200, Name: MSTR_SLV_CONTROL

This address corresponds to the leader follower control register specified in Clause 40.5.1.1 of IEEE Standard 802.3. Note that the default reset value of this register is dependent on the hardware configuration pins settings.

Table 46. Bit Descriptions for MSTR_SLV_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:13]	TST_MODE	Transmitter test mode operations are defined by the test mode bits as specified in Clause 40.6.1.1.2 of IEEE Standard 802.3. 111: reserved. 110: reserved. 101: reserved. 100: Test Mode 4—transmitter distortion test. 011: Test Mode 3—transmit jitter test in follower mode. 010: Test Mode 2—transmit jitter test in leader mode. 001: Test Mode 1—transmit waveform test. 000: normal operation.	0x0	R/W
12	MAN_MSTR_SLV_EN_ADV	Manual Leader/Follower Enable Advertisement Bit. 1: enable leader follower manual configuration value. 0: disable leader follower manual configuration value.	0x0	R/W
11	MAN_MSTR_ADV	Manual Leader/Follower Advertisement Bit. 1: configure PHY as leader during leader follower negotiation only when MAN_MSTR_SLV_EN_ADV is set to Logical 1. 0: configure PHY as follower during leader follower negotiation only when MAN_MSTR_SLV_EN_ADV is set to Logical 1.	0x0	R/W
10	PREF_MSTR_ADV	Prefer Leader (or Port Type) Advertisement Bit. This bit is used to indicate the preference to operate as leader (multiport device) or as follower (single port device) if the MAN_MSTR_SLV_EN_ADV bit (Bit 9), is not set. Usage of this bit is described in Clause 40.5.2 of IEEE Standard 802.3. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications. 1: multiport device. 0: single port device.	0x0	R/W
9	FD_1000_ADV	1000BASE-T Full Duplex Advertisement Bit. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications. 1: advertise PHY is 1000BASE-T full duplex capable. 0: advertise PHY is not 1000BASE-T full duplex capable.	0x1	R/W
8	HD_1000_ADV	1000BASE-T Half Duplex Advertisement Bit. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications. 1: advertise PHY is 1000BASE-T half duplex capable. 0: advertise PHY is not 1000BASE-T half duplex capable.	0x0	R/W
[7:0]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Leader Follower Status Register

Register Address: 0x000A, Reset: 0x0000, Name: MSTR_SLV_STATUS

This address corresponds to the leader follower status register specified in Clause 40.5.1.1 of IEEE Standard 802.3.

Table 47. Bit Descriptions for MSTR_SLV_STATUS

Bits	Bit Name	Description	Reset	Access
15	MSTR_SLV_FLT	Leader/Follower Configuration Fault Bit. When this bit goes high, it latches high until it is unlatched by reading. This bit self clears on autonegotiation enable or autonegotiation complete. See Clause 40.5.1.1 of IEEE Standard 802.3 for more details. 1: leader follower configuration fault detected. 0: no leader follower configuration fault detected.	0x0	R LH SC
14	MSTR_RSLVD	Leader/Follower Configuration Resolution Bit. 1: local PHY configuration resolved to leader. 0: local PHY configuration resolved to follower.	0x0	R
13	LOC_RCVR_STATUS	Local Receiver Status Bit. Defined by the value of LOC_RCVR_STATUS, as described in Clause 40.4.5.1 of IEEE Standard 802.3. 1: local receiver okay (LOC_RCVR_STATUS = okay). 0: local receiver not okay (LOC_RCVR_STATUS = not okay).	0x0	R
12	REM_RCVR_STATUS	Remote Receiver Status Bit. Defined by the value of REM_RCVR_STATUS as, described in Clause 40.4.5.1 of IEEE Standard 802.3. 1: remote receiver okay (REM_RCVR_STATUS = okay). 0: remote receiver not okay (REM_RCVR_STATUS = not okay).	0x0	R
11	LP_FD_1000ABLE	Link Partner 1000BASE-T Full Duplex Ability Bit. This bit is guaranteed to be valid only when the PAGE_RX_LAT bit (Register 0x0006, Bit 1) has been set to 1. 1: link partner is capable of 1000BASE-T full duplex. 0: link partner is not capable of 1000BASE-T full duplex.	0x0	R
10	LP_HD_1000ABLE	Link Partner 1000BASE-T Half Duplex Ability Bit. This bit is guaranteed to be valid only when the PAGE_RX_LAT bit (6.1) has been set to 1. 1: link partner is capable of 1000BASE-T half duplex. 0: link partner is not capable of 1000BASE-T half duplex.	0x0	R
[9:8]	RESERVED	Reserved.	0x0	R
[7:0]	IDLE_ERR_CNT	Idle Error Count. These idle error count bits contain a cumulative count of the errors detected when the receiver is receiving idles. See Clause 40.5.1.1 of IEEE Standard 802.3 for more details.	0x0	R SC

Extended Status Register

Register Address: 0x000F, Reset: 0x3000, Name: EXT_STATUS

This address corresponds to the extended status register specified in Clause 22.2.4.4 of IEEE Standard 802.3.

Table 48. Bit Descriptions for EXT_STATUS

Bits	Bit Name	Description	Reset	Access
15	FD_1000_X_SPRT	This bit is always zero because the PHY does not support full duplex 1000BASE-X.	0x0	R
14	HD_1000_X_SPRT	This bit is always zero because the PHY does not support half duplex 1000BASE-X.	0x0	R
13	FD_1000_SPRT	This bit is always one because the PHY supports full duplex 1000BASE-T.	0x1	R
12	HD_1000_SPRT	This bit is always one because the PHY supports half duplex 1000BASE-T.	0x1	R
[11:0]	RESERVED	Reserved.	0x0	R

Extended Register Pointer Register

Register Address: 0x0010, Reset: 0x0000, Name: EXT_REG_PTR

The extended register pointer and extended register data registers provide a mechanism to access the indirect access address map via directly accessible registers for cases where the station management does not support Clause 45.

REGISTER SUMMARY

Table 49. Bit Descriptions for EXT_REG_PTR

Bits	Bit Name	Description	Reset	Access
[15:0]	EXT_REG_PTR	Extended Register Pointer. The extended register pointer and extended register data registers provide an indirect mechanism to access EMI registers using normal Clause 22 access for cases where the station management does not support Clause 45. Write the 16-bit register address into the EXT_REG_PTR register. The EMI register can be read or written by reading or writing the EXT_REG_DATA register. An EMI register can be directly accessed using Clause 45 access.	0x0	R/W

Extended Register Data Register

Register Address: 0x0011, Reset: 0x0000, Name: EXT_REG_DATA

The extended register pointer and extended register data registers provide a mechanism to access the indirect access address map via directly accessible registers for cases where the station management does not support Clause 45.

Table 50. Bit Descriptions for EXT_REG_DATA

Bits	Bit Name	Description	Reset	Access
[15:0]	EXT_REG_DATA	Extended Register Data. The extended register pointer and extended register data registers provide an indirect mechanism to access EMI registers using normal Clause 22 access for cases where the station management does not support Clause 45. See Table 57 for further details.	0x0	R/W

PHY Control 1 Register

Register Address: 0x0012, Reset: 0x0002, Name: PHY_CTRL_1

This register provides access to various PHY control register bits, in particular for diagnostic clocking control and MDI crossover.

Table 51. Bit Descriptions for PHY_CTRL_1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	AUTO_MDI_EN	Automatic MDI/MDI-X Resolution Enable. The automatic MDI/MDIX resolution enable register bit allows the automatic cable crossover feature of the PHY to be controlled. Note that the default value of this register bit is configurable via a hardware configuration pin, which allows the default operation of the PHY to be configured in unmanaged applications. 1: enable auto MDI/MDIX. Prefer MDI if MAN_MDIX is 1'b0 and prefer MDIX if MAN_MDIX is 1'b1. 0: disable auto MDI/MDIX.	0x0	R/W
9	MAN_MDIX	Manual MDIX. When this bit is set and the AUTO_MDI_EN bit is clear, the PHY operates in the MDIX configuration. In this configuration, no crossover is implemented, and the logical pairs of the PCS correspond to the physical pairs of the AFE. When this bit is clear and the AUTO_MDI_EN bit is clear, the PHY operates in the MDI configuration and crossovers the pairs. If the AUTO_MDI_EN bit is set, the MAN_MDIX bit determines the MDI or MDIX preference option. 1: operate in MDIX configuration. 0: operate in MDI configuration.	0x0	R/W
[8:3]	RESERVED	Reserved.	0x0	R
2	DIAG_CLK_EN	Enable PHY Diagnostics Clock. Enable PHY Diagnostics Clock. This clock is required for certain diagnostic functions within the PHY, for example, the frame generator/checker. 1: enable PHY diagnostics clock. 0: disable PHY diagnostics clock.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x2	R/W

PHY Control Status 1 Register

Register Address: 0x0013, Reset: 0x1041, Name: PHY_CTRL_STATUS_1

This register provides access to PHY loopback control bits.

REGISTER SUMMARY

Table 52. Bit Descriptions for PHY_CTRL_STATUS_1

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R/W
12	LB_ALL_DIG_SEL	All Digital Loopback Select. Setting this bit selects all digital loopback. This loops the data within the PHY at the analog/digital boundary so that data received on the MAC interface TXD_x pins is looped back to the RXD_x pins. This requires the IEEE loopback bit (Register 0x0000, Bit 14) to be set.	0x1	R/W
11	RESERVED	Reserved.	0x0	R
10	LB_LD_SEL	Line Driver Loopback Select. Setting this bit selects line driver loopback. If this register bit is set, every time the loopback bit is set the PHY enters line driver loopback mode. In line driver loopback mode, leave the MDI pins open to create a large impedance mismatch. The PHY can then operate by receiving the reflection from its own transmission.	0x0	R/W
9	LB_REMOTE_EN	Remote Loopback Enable. Setting this bit enables remote loopback. This requires a link up with a remote PHY and it loops the data received from the remote PHY back to the remote PHY using all of the digital and analog circuitry of the PHY.	0x0	R/W
8	ISOLATE_RX	Isolate Rx Bit. Setting this bit suppresses data being sent to the MAC during loopback.	0x0	R/W
7	LB_EXT_EN	External Cable Loopback Enable. Setting this bit enables external cable loopback. This requires an external cable with Pair 0 and Pair 1 and Pair 2 and Pair 3 shorted together to provide an analog loopback at the end of the cable. All the digital and analog circuitry of the PHY and the signal processing is adjusted so that the transmitted signal is not cancelled. The IEEE loopback bit (Register 0x0000, Bit 14) must not be set.	0x0	R/W
6	LB_TX_SUP	Loopback Tx Suppress. Setting this bit suppresses the transmit signal at the MDI pins in all digital loopback.	0x1	R/W
[5:1]	RESERVED	Reserved.	0x0	R LH
0	LB_MII_LS_OK	MII Loopback Link Status. Setting this bit sets the link status signal to okay during MII loopback.	0x1	R/W

Receive Error Count Register

Register Address: 0x0014, Reset: 0x0000, Name: RX_ERR_CNT

The receive error counter register is used to access the receive error counter associated with the frame checker in the PHY.

Table 53. Bit Descriptions for RX_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	RX_ERR_CNT	Receive Error Counter. This is the receive error counter associated with the frame checker in the PHY. Note that this bit is self-clearing upon reading.	0x0	R SC

PHY Control Status 2 Register

Register Address: 0x0015, Reset: 0x0000, Name: PHY_CTRL_STATUS_2

This register provides access to various PHY control and status registers, in particular autonegotiation controls and energy detect power-down control and status bits.

Table 54. Bit Descriptions for PHY_CTRL_STATUS_2

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	NRG_PD_EN	Energy Detect Power Down Enable. Setting this bit enables energy to detect power-down. If there is no signal energy detected for a number of seconds, the PHY enters energy detect power-down mode. Note that the default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable energy to detect power-down mode. 0: disable energy detect power-down mode.	0x0	R/W
2	NRG_PD_TX_EN	Energy Detect Power Down Tx Enable. When this bit is set, the PHY periodically wakes up when in energy detect power-down and transmits a number of pulses. This is to avoid a lock up situation where the PHYs on both ends of the line are in energy detect power-down mode. Note that the	0x0	R/W

REGISTER SUMMARY

Table 54. Bit Descriptions for PHY_CTRL_STATUS_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable periodic transmission of the pulse while in energy detect power-down mode. 0: disable periodic transmission of the pulse while in energy detect power-down mode.		
1	PHY_IN_NRG_PD	Energy-detect Power Down Status Bit. This status bit indicates that the PHY is in energy detect power-down mode. 1: PHY is in energy detect power-down mode. 0: PHY is not in energy detect power-down mode.	0x0	R
0	RESERVED	Reserved.	0X0	R/W

PHY Control 2 Register

Register Address: 0x0016, Reset: 0x0308, Name: PHY_CTRL_2

This register provides access to various PHY control registers, for control of clocking, group MDIO access, and autonegotiation.

Table 55. Bit Descriptions for PHY_CTRL_2

Bits	Bit Name	Description	Reset	Access
15	HD_TX_CRS_EN	HD_TX_CRS_EN. When set this register indicates that the PHY should assert CRS on transmit in half duplex mode.	0x0	R/W
[14:12]	RESERVED	Reserved.	0x0	R
11	DN_SPEED_TO_100EN	Downspeed to 100BASE-TX En. Setting this bit enables downspeed to 100BASE-TX. Note that autonegotiation must also be enabled. If the PHY is unable to bring a link up at 1000BASE-T, it automatically drops down to 100BASE-TX (assuming this speed has been advertised). Note that the default value of this register bit is configurable via the hardware configuration pins performing the PHY_CFG1 and PHY_CFG0 functions, which allows the default operation of the PHY to be configured in unmanaged applications. 1: enable downspeed to 100BASE-TX. 0: disable downspeed to 100BASE-TX.	0x0	R/W
10	DN_SPEED_TO_10EN	Downspeed to 10BASE-T En. Setting this bit enables downspeed to 10BASE-T. Note that autonegotiation must also be enabled. If the PHY is unable to bring a link up at a high speed, it automatically drops down to 10BASE-T (assuming this speed has been advertised) if necessary. 1: enable downspeed to 10BASE-T. 0: disable downspeed to 10BASE-T.	0x0	R/W
[9:7]	RESERVED	Reserved.	0x6	R/W
6	GROUP_MDIO_EN	Group MDIO Enable. The group MDIO enable register bit may be used to place the PHY in group MDIO mode. In this mode, the PHY responds to any write or address operation to PHY address 5'd31 as if it was an access to its own PHY address. It is recommended that this bit be set only when performing specific sequences and then be cleared again.	0x0	R/W
5	RESERVED	Reserved.	0x0	R/W
4	RESERVED	Reserved.	0x0	R/W
[3:1]	CLK_CNTRL	The clock control register allows the desired speed of the TX_CLK and RX_CLK signals to be specified when the link is down and allows the desired speed of the TX_CLK signal to be specified when a 1000BASE-T link is active. In each case the choices of speed are off, 2.5MHz and 25MHz. The default value of 3b100 specifies 2.5MHz in all cases.	0x4	R/W
0	RESERVED	Reserved.	0x0	R

PHY Control 3 Register

Register Address: 0x0017, Reset: 0x3048, Name: PHY_CTRL_3

This register provides access to PHY control register bits for link enable and autonegotiation controls.

REGISTER SUMMARY

Table 56. Bit Descriptions for PHY_CTRL_3

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	LINK_EN	Link Enable. Setting this bit enables linking. If linking is disabled, the PHY enters the standby state and does not attempt to bring up links. The standby state can be used to run diagnostics, including cable diagnostics. 1: enable linking. 0: disable linking.	0x1	R/W
[12:10]	NUM_SPEED_RETRY	If downspeed is enabled, this register bit specifies the number of retries the PHY must attempt to bring up a link at the advertised speed before advertising a lower speed. By default, the PHY attempts to bring up a link 5 times (4 retries) before downspeeding.	0x4	R/W
[9:0]	RESERVED	Reserved.	0x48	R/W

Interrupt Mask Register

Register Address: 0x0018, Reset: 0x0000, Name: IRQ_MASK

The interrupt mask register allows interrupts to be masked or unmasked.

Table 57. Bit Descriptions for IRQ_MASK

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R/W
10	CBL_DIAG_IRQ_EN	Cable Diagnostics IRQ Enable. 1: enable cable diagnostics interrupt. 0: disable cable diagnostics interrupt.	0x0	R/W
9	MDIO_SYNC_IRQ_EN	MDIO Synchronization Lost IRQ Enable. 1: enable MDIO synchronization lost interrupt. 0: disable MDIO synchronization lost interrupt.	0x0	R/W
8	AN_STAT_CHNG_IRQ_EN	Auto-negotiation Status Changed IRQ Enable. 1: enable autonegotiation status changed interrupt. 0: disable autonegotiation status changed interrupt.	0x0	R/W
7	FC_FG_IRQ_EN	Frame Checker/Generator Interrupt Enable Bit. 1: enabled interrupt. 0: disable changed interrupt.	0x0	R/W
6	PAGE_RX_IRQ_EN	Auto-negotiation Page Received IRQ Enable. 1: enable autonegotiation page received interrupt. 0: disable autonegotiation page received interrupt.	0x0	R/W
5	IDLE_ERR_CNT_IRQ_EN	Idle Error Counter Saturated IRQ Enable. 1: enable idle error counter saturated interrupt. 0: disable idle error counter saturated interrupt.	0x0	R/W
4	FIFO_OU_IRQ_EN	FIFO Overflow/Underflow IRQ Enable. 1: enable MAC interface FIFO overflow/underflow interrupt. 0: disable MAC interface FIFO overflow/underflow interrupt.	0x0	R/W
3	RX_STAT_CHNG_IRQ_EN	Receive Status IRQ Enable. FIFO Overflow/Underflow IRQ Enable. 1: enable receive status changed interrupt. 0: disable receive status changed interrupt.	0x0	R/W
2	LNK_STAT_CHNG_IRQ_EN	Link Status Changed IRQ Enable. 1: enable link status changed interrupt. 0: disable link status changed interrupt.	0x0	R/W
1	SPEED_CHNG_IRQ_EN	Speed Changed IRQ Enable. 1: enable speed changed interrupt. 0: disable speed changed interrupt.	0x0	R/W
0	HW_IRQ_EN	Hardware IRQ Enable. When set, this enables the hardware interrupt pin, INT_N, and INT_N is asserted when an interrupt is generated. 1: enable the hardware interrupt pin, INT_N. 0: disable the hardware interrupt pin, INT_N.	0x0	R/W

REGISTER SUMMARY

Interrupt Status Register

Register Address: 0x0019, Reset: 0x0000, Name: IRQ_STATUS

The interrupt status register is used to check which interrupts have triggered since the last time it was read. Each bit goes high when the associated interrupt triggers and then latches high until it is unlatched by reading (note that reading any of the bits in this register unlatches all of the bits in the register). The bits of IRQ_STATUS go high even when the associated interrupts are not enabled. However, only bits associated with enabled interrupts are considered when generating the IRQ_PENDING indication.

Table 58. Bit Descriptions for IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R LH
10	CBL_DIAG_IRQ_STAT	Cable Diagnostics IRQ. If the cable diagnostics interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
9	MDIO_SYNC_IRQ_STAT	MDIO Synchronization IRQ. If the MDIO synchronization lost interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
8	AN_STAT_CHNG_IRQ_STAT	Auto-negotiation Status Changed IRQ. If the autonegotiation status changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
7	FC_FG_IRQ_STAT	Frame Checker/Generator IRQ. If the frame checker/generator interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
6	PAGE_RX_IRQ_STAT	Page Rx IRQ. If the autonegotiation page received interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
5	IDLE_ERR_CNT_IRQ_STAT	Idle Error Count IRQ. If the idle error counter saturated interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
4	FIFO_OU_IRQ_STAT	FIFO Overflow/Underflow IRQ. If the MAC interface RGMII transmit FIFO overflow/ underflow interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
3	RX_STAT_CHNG_IRQ_STAT	Rx Status Change IRQ. If the receive status changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
2	LNK_STAT_CHNG_IRQ_STAT	Link Status Changed IRQ. If the link status changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
1	SPEED_CHNG_IRQ_STAT	Speed Change IRQ. If the speed changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH
0	IRQ_PENDING	IRQ Pending. If the interrupt pending status bit is 1, this indicates that an interrupt has occurred and is pending. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R LH

PHY Status 1 Register

Register Address: 0x001A, Reset: 0x0300, Name: PHY_STATUS_1

This register provides access to various PHY status registers.

REGISTER SUMMARY

Table 59. Bit Descriptions for PHY_STATUS_1

Bits	Bit Name	Description	Reset	Access
15	PHY_IN_STNDBY	A 1 indicates that the PHY is in standby state and does not attempt to bring up links. The standby state can be used to run diagnostics, including cable diagnostics.	0x0	R
14	MSTR_SLV_FLT_STAT	LEADER-FOLLOWER Configuration Fault Status Bit. The leader/follower configuration fault status bit is a copy of MSTR_SLV_FLT. Reading this copy does not unlatch the original.	0x0	R
13	PAR_DET_FLT_STAT	Parallel Detection Fault Status Bit. Parallel Detection Fault Status Bit. A 1 indicates that a fault has occurred in the parallel detection process. This bit is a copy of PAR_DET_FLT, (AUTONEG_EXP register, Address 0x0006). Reading the PAR_DET_FLT_STAT bit does not clear PAR_DET_FLT.	0x0	R
12	AUTONEG_STAT	Auto-negotiation Status. A 1 indicates that autonegotiation has completed. This bit is a copy of AUTONEG_DONE (MII_STATUS register, Address 0x0001). Reading the AUTONEG_STAT bit does not clear AUTONEG_DONE.	0x0	R
11	PAIR_01_SWAP	A 1 indicates that Pair 0 and Pair 1 have been swapped.	0x0	R
10	B_10_POL_INV	A 1 indicates that the polarity of the 10BASE-T signal has been inverted.	0x0	R
[9:7]	HCD_TECH	Highest Common Denominator Technology Field. This field indicates the resolved technology after the link is established. 111: reserved. 110: reserved. 101: speed resolved to 1000BASE-T full duplex. 100: speed resolved to 1000BASE-T half duplex. 011: speed resolved to 100BASE-TX full duplex. 010: speed resolved to 100BASE-TX half duplex. 001: speed resolved to 10BASE-T full duplex. 000: speed resolved to 10BASE-T half duplex.	0x6	R
6	LINK_STAT	Link Status. A 1 indicates that a link is up.	0x0	R
5	TX_EN_STAT	Transmit Enable Status. A 1 indicates that transmit enable (TX_EN) is asserted.	0x0	R
4	RX_DV_STAT	Receive Data Valid. A 1 indicates that receive data valid (RX_DV) is asserted.	0x0	R
3	COL_STAT	Collision Status. A 1 indicates that collision is asserted.	0x0	R
2	AUTONEG_SUP	Auto-negotiation Support Bit. A 1 indicates that both the local and remote PHYs support autonegotiation.	0x0	R
1	LP_PAUSE_ADV	Link Partner Pause Advertisement Bit. A 1 indicates that the link partner has advertised pause. The link partner pause advertisement bit indicates that the link partner advertised support for pause operation on full duplex links. This bit provides the same information as LP_PAUSE_ABLE.	0x0	R
0	LP_APAUSE_ADV	Link Partner Asymmetric Pause Advertisement Bit. A 1 indicates that the link partner has advertised asymmetric pause. The link partner asymmetric pause advertisement bit indicates that the link partner advertised support for asymmetric pause operation on full duplex links. This bit provides the same information as LP_APAUSE_ABLE.	0x0	R

LED Control 1 Register

Register Address: 0x001B, Reset: 0x0001, Name: LED_CTRL_1

This register provides access to various PHY LED control register bits.

Table 60. Bit Descriptions for LED_CTRL_1

Bits	Bit Name	Description	Reset	Access
15	LED_23_2_CLR_EN	The LED 2/3 2-color mode enable register allows LED 2 and 3 to be configured for 2-color operation. In this case LED 2 is forced off when LED 3 is on.	0x0	R/W
14	LED_01_2_CLR_EN	The LED 0/1 2-color mode enable register allows LED 0 and 1 to be configured for 2-color operation. In this case LED 0 is forced off when LED 1 is on.	0x0	R/W
13	LED_3_EXT_CFG_EN	Enable Extended Configuration Set for LED_3 Pin. Also see LED_CTRL_2 register, Address 0x001C, Bits [15:12].	0x0	R/W
12	LED_2_EXT_CFG_EN	Enable Extended Configuration Set for LED_2 Pin. Also see LED_CTRL_2 register, Address 0x001C, Bits [11:8].	0x0	R/W

REGISTER SUMMARY

Table 60. Bit Descriptions for LED_CTRL_1 (Continued)

Bits	Bit Name	Description	Reset	Access
11	LED_1_EXT_CFG_EN	Enable Extended Configuration Set for LED_1 Pin. Also see LED_CTRL_2 register, Address 0x001C, Bits [7:4].	0x0	R/W
10	LED_0_EXT_CFG_EN	Enable Extended Configuration Set for LED_0 Pin. Also see LED_CTRL_2 register, Address 0x001C, Bits [3:0].1: enable extended configuration set for LED_0 pin.0: disable extended configuration set for LED_0 pin.	0x0	R/W
[9:8]	RESERVED	Reserved.	0x0	R
[7:4]	LED_PAT_PAUSE_DUR	Internal LED Pattern Pause Duration. Internal LED Pattern Pause Duration for LED_0. After the blink pattern is driven out to the LED pin, the last bit is held for a duration specified by the LED pattern pause duration register field. This duration is the value of LED tick duration (for example, the time for each bit) multiplied by the value of the LED pattern pause duration register field. Also see the LED_PAT register field (LED_CTRL_3 register, Address 0x001D, Bits [7:0]) and the LED_PAT_TICK_DUR register field (LED_CTRL_3 register, Address 0x001D, Bits [13:8]). The default blink is a 0.5 sec on and 0.5 sec off pattern.	0x0	R/W
[3:2]	LED_PUL_STR_DUR_SEL	LED Pulse Stretching Duration. This bit field selects the duration of the pulse stretching.11: user programmable. In this case, the duration of the pulse stretching is programmable by the LED_PUL_STR_DUR register (Address 0xBC00, Bits [5:0]).10: 102ms.01: 64ms.00: 32ms.	0x0	R/W
1	LED_OE_N	LED Active Low Output Enable Register Bit. 1: disable LED outputs. 0: enable LED outputs.	0x0	R/W
0	LED_PUL_STR_EN	LED Pulse Stretching Enable. Setting this bit enables pulse stretching for transmit, receive, or collision LED events so that very short duration events are visible. The LED pulse stretching enable register indicates that the PHY must stretch any pulses indicating transmit, receive, or collision. Without stretching, these pulses may be too short to cause an LED to light.	0x1	R/W

LED Control 2 Register

Register Address: 0x001C, Reset: 0x210A, Name: LED_CTRL_2

This address provides access to various PHY LEDs control registers.

Table 61. Bit Descriptions for LED_CTRL_2

Bits	Bit Name	Description	Reset	Access
[15:12]	LED_3_CFG	LED_3 Configuration. This register selects the configuration for LED_3. See LED_0_CFG for more information.	0x2	R/W
[11:8]	LED_2_CFG	LED_2 Configuration. This register selects the configuration for LED_2. See LED_0_CFG for more information.	0x1	R/W
[7:4]	LED_1_CFG	LED_1 Configuration. This register selects the configuration for LED_1. See LED_0_CFG for more information.	0x0	R/W
[3:0]	LED_0_CFG	LED_0 Configuration. LED_0 configuration is made up of five bits. These four bits, Bits [3:0], are the LSBs and Bit 4 is from LED_0_EXT_CFG_EN (LED_CTRL_1 register, Address 0x001B). The combination of the five bits configures LED_0, selecting one of 32 possible configuration functions according to the following settings. The default setting is 01010 (on if link up and blink on activity). 11111: on if 10BASE-T link, blink if 100BASE-TX link. 11110: on if 10BASE-T link, blink if 1000BASE-T link. 11101: on if 100BASE-TX link, blink if 10BASE-T link. 11100: on if 100BASE-TX link, blink if 1000BASE-T link. 11011: on if 1000BASE-T link, blink if 10BASE-T link. 11010: blink if transmit. 11001: blink on activity. 11000: on if 10BASE-T or 1000BASE-T link, blink on activity. 10111: on if 10BASE-T or 1000BASE-T link. 10110: on if 100BASE-TX or 1000BASE-T link, blink on activity. 10101: on if 10BASE-T or 100BASE-TX link, blink on activity. 10100: on if 1000BASE-T link, blink on activity.	0xA	R/W

REGISTER SUMMARY

Table 61. Bit Descriptions for LED_CTRL_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		10011: on if 100BASE-TX link, blink on activity. 10010: on if 10BASE-T link, blink on activity. 10001: on if 100BASE-TX or 1000BASE-T link. 10000: on if 10BASE-T or 100BASE-TX link. 01111: off. 01110: on. 01101: blink. 01100: on if full duplex link, blink on collision. 01011: on if link, blink if receiving. 01010: on if link, blink on activity. 01001: on if collision. 01000: on if full duplex link. 00111: on if activity (transmitting or receiving). 00110: on if receiving. 00101: on if transmitting. 00100: on if link up. 00011: on if 1000BASE-T link, blink if 100BASE-TX. 00010: on if 10BASE-T link. 00001: on if 100BASE-TX link. 00000: on if 1000BASE-T link.		

LED Control 3 Register

Register Address: 0x001D, Reset: 0x1855, Name: LED_CTRL_3

This register provides access to various PHY LED control register bits.

Table 62. Bit Descriptions for LED_CTRL_3

Bits	Bit Name	Description	Reset	Access
[15:14]	LED_PAT_SEL	LED Pattern Select. The LED blink pattern select register allows management to specify which of the LED blink patterns it wishes to program in accordance with the following encoding: 11: LED 3 blink pattern 10: LED 2 blink pattern 01: LED 1 blink pattern 00: LED 0 blink pattern The LED_PAT_PAUSE_DUR, LED_PAT and LED_PAT_TICK_DUR fields indirectly access the corresponding registers for selected blink pattern.	0x0	R/W
[13:8]	LED_PAT_TICK_DUR	Each bit in the blink pattern bit field (LED_PAT) is driven to the corresponding LED pin and held for the duration specified in this 6-bit LED pattern duration bit field. The duration is the value of this register plus 1 multiplied by 8, for example, 8ms, 16ms, … 504ms. The value 63 has a special meaning of 1ms tick duration. Also see the LED_PAT_PAUSE_DUR bit field (LED_CTRL_1 register, Address 0x001B). The default blink is a 0.5 sec on and 0.5 sec off pattern.	0x18	R/W
[7:0]	LED_PAT	The internal LED pattern register for LED_3, LED_2, LED_1 or LED_0 can be read or written via this field. The LED_PAT_SEL field selects which set of internal blink pattern registers (e.g. for LED_3, LED_2, LED_1 or LED_0) is accessed. The default value of the LED pattern register is 0x55 and is thus an alternating 0/1 pattern. (LED_CTRL_1 register, address 0x001B). The default blink is a 0.5s ON and 0.5s OFF pattern.	0x55	R/W

PHY Status 2 Register

Register Address: 0x001F, Reset: 0x03FC, Name: PHY_STATUS_2

This register provides access to various PHY status register bits.

REGISTER SUMMARY

Table 63. Bit Descriptions for PHY_STATUS_2

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	PAIR_23_SWAP	Pair 2 and 3 Swapped. A 1 indicates that Pair 2 and Pair 3 have been swapped.	0x0	R
13	PAIR_3_POL_INV	Pair 3 Polarity Inverted. A 1 indicates that the polarity on Pair 3 has been inverted.	0x0	R
12	PAIR_2_POL_INV	Pair 2 Polarity Inverted. A 1 indicates that the polarity on Pair 2 has been inverted.	0x0	R
11	PAIR_1_POL_INV	Pair 1 Polarity Inverted. A 1 indicates that the polarity on Pair 1 has been inverted.	0x0	R
10	PAIR_0_POL_INV	Pair 0 Polarity Inverted. A 1 indicates that the polarity on Pair 0 has been inverted.	0x0	R
[9:1]	RESERVED	Reserved.	0x1FE	R
0	B_1000_DSCR_ACQ_ERR	1000BASE-T Descrambler Acquisition Error Bit. A 1 indicates an error has occurred during the acquisition of the scrambler during 1000BASE-T start-up. This error can occur because the pair skew is too large.	0x0	R LH

Energy Efficient Ethernet Capability Register

Register Address: 0x8000, Reset: 0x0006, Name: EEE_CAPABILITY

This address corresponds to the EEE capability register specified in Clause 45.2.3.9 of IEEE Standard 802.3, which, in the IEEE standard, is at MMD Register Address 3.20. This register is used to indicate the capability of the PCS to support EEE functions for each PHY type.

Table 64. Bit Descriptions for EEE_CAPABILITY

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	EEE_10_G_KR_SPRT	The 10GBASE-KR EEE capability bit always reads as 1'b0 indicating that the PHY does not support this technology.	0x0	R
5	EEE_10G_KX_4_SPRT	The 10GBASE-KX4 EEE capability bit always reads as 1'b0 indicating that the PHY does not support this technology.	0x0	R
4	EEE_1000_KX_SPRT	The 1000BASE-KX EEE capability bit always reads as 1'b1. 1: EEE is supported for 1000BASE-KX. 0: EEE is not supported for 1000BASE-KX.	0x0	R
3	EEE_10_G_SPRT	The 10GBASE-T EEE capability bit always reads as 1'b0 indicating that the PHY does not support this technology.	0x0	R
2	EEE_1000_SPRT	The 1000BASE-T EEE capability bit always reads as 1'b1. 1: EEE is supported for 1000BASE-T. 0: EEE is not supported for 1000BASE-T.	0x1	R
1	EEE_100_SPRT	The 100BASE-TX EEE capability bit always reads as 1'b1. 1: EEE is supported for 100BASE-TX. 0: EEE is not supported for 100BASE-TX.	0x1	R
0	RESERVED	Reserved.	0x0	R

Energy Efficient Ethernet Advertisement Register

Register Address: 0x8001, Reset: 0x0000, Name: EEE_ADV

This address corresponds to the EEE advertisement register specified in Clause 45.2.7.13 of Standard 802.3, which, in the IEEE standard, is at MMD Register Address 7.60. This register is used to define the EEE advertisement during autonegotiation. The reset value of this register is 0x0000 except where the hardware configuration pins are set to enable EEE. In this case, the reset value is 0x0006.

Table 65. Bit Descriptions for EEE_ADV

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	EEE_10G_KR_ADV	The 10GBASE-KR EEE advertisement bit always reads as 1'b0. 1: advertise that the 10GBASE-KR has EEE capability. 0: do not advertise that the 10GBASE-KR has EEE capability	0x0	R

REGISTER SUMMARY

Table 65. Bit Descriptions for EEE_ADV (Continued)

Bits	Bit Name	Description	Reset	Access
5	EEE_10G_KX_4_ADV	The 10GBASE-KX4 EEE advertisement bit always reads as 1'b0. 1: advertise that the 10GBASE-KX4 has EEE capability. 0: do not advertise that the 10GBASE-KX4 has EEE capability.	0x0	R
4	EEE_1000_KX_ADV	1000BASE-KX EEE Advertisement. The default value of the 1000BASE-KX EEE advertisement register bit is dependent on the hardware configuration pins settings. When EEE is enabled by these pins, the default value is 1'b1 and when disabled, the default value is 1'b0. 1: advertise that the 1000BASE-KX has EEE capability. 0: do not advertise that the 1000BASE-KX has EEE capability.	0x0	R
3	EEE_10_G_ADV	The 10GBASE-T EEE advertisement bit always reads as 1'b0. 1: advertise that the 10GBASE-T has EEE capability. 0: do not advertise that the 10GBASE-T has EEE capability	0x0	R
2	EEE_1000_ADV	The default value of the 1000BASE-T EEE advertisement register bit is dependent on the hardware configuration pins settings. When EEE is enabled by these pins, the default value is 1'b1 and when disabled, the default value is 1'b0. 1: advertise that the 1000BASE-T has EEE capability. 0: do not advertise that the 1000BASE-T has EEE capability.	0x0	R/W
1	EEE_100_ADV	The default value of the 100BASE-TX EEE advertisement register bit is dependent on the hardware configuration pins settings. When EEE is enabled by these pins, the default value is 1'b1 and when disabled, the default value is 1'b0. 1: advertise that the 100BASE-TX has EEE capability. 0: do not advertise that the 100BASE-TX has EEE capability.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Energy Efficient Ethernet Link Partner Ability Register

Register Address: 0x8002, Reset: 0x0000, Name: EEE_LP_ABILITY

This address corresponds to the EEE link partner ability register specified in Clause 45.2.7.14 of Standard 802.3, which, in the IEEE standard, is at MMD Register Address 7.61. This register reflects the EEE advertisement of the link partner during autonegotiation.

Table 66. Bit Descriptions for EEE_LP_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	LP_EEE_10_G_KR_ABLE	Link Partner 10GBASE-KR EEE Ability Bit. 1: link partner is advertising EEE capability for 10GBASE-KR. 0: link partner is not advertising EEE capability for 10GBASE-KR.	0x0	R
5	LP_EEE_10_G_KX_4_ABLE	Link Partner 10GBASE-KX4 EEE Ability Bit. 1: link partner is advertising EEE capability for 10GBASE-KX4. 0: link partner is not advertising EEE capability for 10GBASE-KX4.	0x0	R
4	LP_EEE_1000_KX_ABLE	Link Partner 1000BASE-KX EEE Ability Bit. 1: link partner is advertising EEE capability for 1000BASE-KX. 0: link partner is not advertising EEE capability for 1000BASE-KX.	0x0	R
3	LP_EEE_10_G_ABLE	Link Partner 10GBASE-T EEE Ability Bit. 1: link partner is advertising EEE capability for 10GBASE-T. 0: link partner is not advertising EEE capability for 10GBASE-T.	0x0	R
2	LP_EEE_1000_ABLE	Link Partner 1000BASE-T EEE Ability Bit. 1: link partner is advertising EEE capability for 1000BASE-T. 0: link partner is not advertising EEE capability for 1000BASE-T.	0x0	R
1	LP_EEE_100_ABLE	Link Partner 100BASE-TX EEE Ability Bit. 1: link partner is advertising EEE capability for 100BASE-TX. 0: link partner is not advertising EEE capability for 100BASE-TX.	0x0	R
0	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Energy Efficient Ethernet Resolved Register

Register Address: 0x8008, Reset: 0x0000, Name: EEE_RSLVD

The EEE resolved bit indicates that auto-negotiation resolved to a technology with EEE enabled.

Table 67. Bit Descriptions for EEE_RSLVD

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	EEE_RSLVD	This bit indicates that the resolved technology after the link has been established is EEE capable. This is a vendor specific register bit. 1: resolved technology is EEE capable. 0: resolved technology is not EEE capable.	0x0	R

Mean Square Error A Register

Register Address: 0x8402, Reset: 0x0000, Name: MSE_A

This register is an indication of signal quality and is a measure of the mean square error on Dimension A.

Table 68. Bit Descriptions for MSE_A

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MSE_A	This register is an indication of signal quality when a 100BASE-TX or 1000BASE-T link is up and is a measure of the mean square error on Dimension A.	0x0	R

Mean Square Error B Register

Register Address: 0x8403, Reset: 0x0000, Name: MSE_B

This register is an indication of signal quality and is a measure of the mean square error on dimension B.

Table 69. Bit Descriptions for MSE_B

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MSE_B	This register is an indication of signal quality when a 1000BASE-T link is up and is a measure of the mean square error on Dimension B.	0x0	R

Mean Square Error C Register

Register Address: 0x8404, Reset: 0x0000, Name: MSE_C

This register is an indication of signal quality and is a measure of the mean square error on dimension C.

Table 70. Bit Descriptions for MSE_C

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MSE_C	This register is an indication of signal quality when a 1000BASE-T link is up and is a measure of the mean square error on Dimension C.	0x0	R

Mean Square Error D Register

Register Address: 0x8405, Reset: 0x0000, Name: MSE_D

This register is an indication of signal quality and is a measure of the mean square error on dimension D.

REGISTER SUMMARY

Table 71. Bit Descriptions for MSE_D

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MSE_D	This register is an indication of signal quality when a 1000BASE-T link is up and is a measure of the mean square error on Dimension D.	0x0	R

Enhanced Link Detection Enable Register

Register Address: 0x8E27, Reset: 0x003D, Name: FLD_EN

This register controls the enables for the enhanced link detection function. This is early detection and indication of link loss.

Table 72. Bit Descriptions for FLD_EN

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	FLD_PCS_ERR_B_100_EN	Enhanced link detection PCS receive error detection enable for 100BASE-TX.	0x0	R/W
6	FLD_PCS_ERR_B_1000_EN	Enhanced link detection PCS receive error detection enable for 1000BASE-T.	0x0	R/W
5	FLD_SLCR_OUT_STUCK_B_100_EN	Enhanced link detection PMA slicer output stuck at detection enable for 100BASE-TX.	0x1	R/W
4	FLD_SLCR_OUT_STUCK_B_1000_EN	Enhanced link detection PMA slicer output stuck at detection enable for 1000BASE-T	0x1	R/W
3	FLD_SLCR_IN_ZDET_B_100_EN	Enhanced link detection PMA slicer input zero detection enable for 100BASE-TX.	0x1	R/W
2	FLD_SLCR_IN_ZDET_B_1000_EN	Enhanced link detection PMA slicer input zero detection enable for 1000BASE-T.	0x1	R/W
1	FLD_SLCR_IN_INVLD_B_100_EN	Enhanced link detection PMA slicer input invalid level detection enable for 100BASE-TX.Enabled when set high.	0x0	R/W
0	FLD_SLCR_IN_INVLD_B_1000_EN	Enhanced link detection PMA slicer input invalid level detection enable for 1000BASE-T.Enabled when set high.	0x1	R/W

Enhanced Link Detection Latched Status Register

Register Address: 0x8E38, Reset: 0x0000, Name: FLD_STAT_LAT

This register is the latched status for the enhanced link detection function. This bit is latched until the start of the next link-up when it is cleared.

Table 73. Bit Descriptions for FLD_STAT_LAT

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	FAST_LINK_DOWN_LAT	Main Enhanced Link Detection Latched Indication.	0x0	R LH
[12:0]	RESERVED	Reserved.	0x0	R LH

Receive MII Clock Stop Enable Register

Register Address: 0x9400, Reset: 0x0400, Name: RX_MII_CLK_STOP_EN

This register contains the clock stop enable bit specified in Clause 45.2.3.1.4 of IEEE Standard 802.3, which, in the IEEE standard, is at MMD Register Address 3.0, Bit 10.

Table 74. Bit Descriptions for RX_MII_CLK_STOP_EN

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 74. Bit Descriptions for RX_MII_CLK_STOP_EN (Continued)

Bits	Bit Name	Description	Reset	Access
10	RX_MII_CLK_STOP_EN	If this bit is set, the PHY may stop the receive MII clock while it is signaling low power enable (LPI). Otherwise, it keeps the clock active. 1: the PHY may stop the clock during LPI. 0: clock not stoppable	0x1	R/W
[9:0]	RESERVED	Reserved.	0x0	R

Physical Coding Sublayer (PCS) Status 1 Register

Register Address: 0x9401, Reset: 0x0040, Name: PCS_STATUS_1

The bits contained in this register correspond to the bits in the PCS Status 1 register specified in Clause 45.2.3.2 of IEEE Standard 802.3, which, in the IEEE standard, is at MMD Register Address 3.1, Bits [11:8] and Bit 6.

Table 75. Bit Descriptions for PCS_STATUS_1

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	TX_LPI_RCVD	The transmit LPI received bit is a latched version of TX_LPI. When this bit goes high, it latches high until it is unlatched by reading. 1: transmit PCS has received LPI. 0: LPI not received.	0x0	R LH
10	RX_LPI_RCVD	The receive LPI received bit is a latched version of RX_LPI. When this bit goes high, it latches high until it is unlatched by reading. 1: receive PCS has received LPI. 0: LPI not receive	0x0	R LH
9	TX_LPI	Transmit LPI Bit. 1: transmit PCS is currently receiving LPI. 0: PCS is not currently receiving LPI.	0x0	R
8	RX_LPI	Receive LPI Bit. 1: transmit PCS is currently receiving LPI. 0: PCS is not currently receiving LPI.	0x0	R
7	RESERVED	Reserved.	0x0	R
6	TX_MII_CLK_STOP_CPBL	The transmit MII clock stop capable bit always reads as 1'b1. 1: the MAC may stop the clock during LPI. 0: clock not stoppable.	0x1	R
[5:0]	RESERVED	Reserved.	0x0	R

Frame Checker Enable Register

Register Address: 0x9403, Reset: 0x0001, Name: FC_EN

This register is used to enable the frame checker. The frame checker analyzes the received frames from either the MAC interface or the PHY (see the FC_TX_SEL register, Address 0x9407, Bit 0) to report the number of frames received, CRC errors, and various other frame errors. The frame checker frame and error counter registers count these events.

Table 76. Bit Descriptions for FC_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_EN	When set, this bit enables the frame checker	0x1	R/W

Frame Checker Interrupt Enable Register

Register Address: 0x9405, Reset: 0x0001, Name: FC_IRQ_EN

REGISTER SUMMARY

This register is used to enable the frame checker interrupt. An interrupt is generated when a receive error occurs. Enable the frame checker/generator interrupt in the interrupt mask register. Set the FC_FG_IRQ_EN bit (IRQ_MASK register, Address 0x0018). The interrupt status can be read via the FC_FG_IRQ_STAT bit (IRQ_STATUS register, Address 0x0019)

Table 77. Bit Descriptions for FC_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_IRQ_EN	When set, this bit enables the frame checker interrupt	0x1	R/W

Frame Checker Transmit Select Register

Register Address: 0x9406, Reset: 0x0000, Name: FC_TX_SEL

This register is used to select the transmit side or receive side for frames to be checked. If set, frames received on the MAC interface to be transmitted are checked. The frame checker can be used to verify that correct data is received over the MAC interface and is also useful if remote loopback is enabled (set the LB_REMOTE_EN bit the in PHY_CTRL_STATUS_1 register, Address 0x0013, Bit 9) because it can be used to check the received data after it is looped back at the MAC interface.

Table 78. Bit Descriptions for FC_TX_SEL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_TX_SEL	When set, this bit indicates that the frame checker must check frames received to be transmitted by the PHY. 1: check frames from the MAC interface to be transmitted by the PHY. 0: check frames received by the PHY from the remote end.	0x0	R/W

Frame Checker Max Frame Size Register

Register Address: 0x940D, Reset: 0x05F2, Name: FC_MAX_FRM_SIZE

This register specifies the maximum frame size. Frames longer than this size are counted as oversized frames.

Table 79. Bit Descriptions for FC_MAX_FRM_SIZE

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_MAX_FRM_SIZE	This bit field specifies the max frame size. Received frames that are longer than this are counted as oversized frames. Note, this frame length excludes the preamble and start frame delimiter	0x5F2	R/W

Frame Checker Count High Register

Register Address: 0x9410, Reset: 0x0000, Name: FC_FRM_CNT_H

This register is a latched copy of Bits [31:16] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the receive frame counter register is latched. A copy of the receive frame counter register is latched when RX_ERR_CNT register is read so that the error count and receive frame count are synchronized.

Table 80. Bit Descriptions for FC_FRM_CNT_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_H	Bits [31:16] of Latched Copy of the Number of Received Frames	0x0	R

Frame Checker Count Low Register

Register Address: 0x9411, Reset: 0x0000, Name: FC_FRM_CNT_L

This register is a latched copy of Bits [15:0] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the receive frame counter register is latched. A copy of the receive frame counter register is latched when RX_ERR_CNT is read so that the error count and receive frame count are synchronized.

REGISTER SUMMARY

Table 81. Bit Descriptions for FC_FRM_CNT_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_L	Bits [15:0] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Alignment Error Count Register

Register Address: 0x9412, Reset: 0x0000, Name: FC_ALGN_ERR_CNT

This register is a latched copy of the frame alignment error counter register. This register is a count of received frames with an alignment error status. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the alignment error counter register is latched, which ensures that the frame alignment error count and receive frame count are synchronized.

Table 82. Bit Descriptions for FC_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ALGN_ERR_CNT	Latched Copy of the Frame Alignment Error Counter.	0x0	R

Frame Checker Symbol Error Counter Register

Register Address: 0x9414, Reset: 0x0000, Name: FC_SYMB_ERR_CNT

This register is a latched copy of the symbol error counter register. This register is a count of received frames with both RX_ER and RX_DV set. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the symbol error counter register is latched, which ensures that the symbol error count and receive frame count are synchronized.

Table 83. Bit Descriptions for FC_SYMB_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_SYM_ERR_CNT	Latched Copy of the Symbol Error Counter.	0x0	R

Frame Checker Length Error Count Register

Register Address: 0x9415, Reset: 0x0000, Name: FC_LEN_ERR_CNT

This register is a latched copy of the frame length error counter register. This register is a count of received frames with a length error status. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the frame length error counter register is latched, which ensures that the frame length error count and receive frame count are synchronized.

Table 84. Bit Descriptions for FC_LEN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_LEN_ERR_CNT	Latched Copy of the Frame Length Error Counter.	0x0	R

Frame Checker Undersized Frame Count Register

Register Address: 0x9416, Reset: 0x0000, Name: FC_USZ_CNT

This register is a latched copy of the undersized frame error counter register. This register is a count of received frames with a length less than 64 bytes. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the undersized frame error counter register is latched, which ensures that the undersized frame error count and receive frame count are synchronized.

Table 85. Bit Descriptions for FC_USZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_USZ_CNT	Latched Copy of the Undersized Frame Error Counter	0x0	R

Frame Checker Oversized Frame Count Register

Register Address: 0x9417, Reset: 0x0000, Name: FC_OSZ_CNT

REGISTER SUMMARY

This register is a latched copy of the oversized frame error counter register. This register is a count of received frames with a length greater than specified in frame checker maximum frame size (FC_MAX_FRM_SIZE register, Address 0x9407). When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the oversized frame error counter register is latched, which ensures that the oversized frame error count and receive frame count are synchronized.

Table 86. Bit Descriptions for FC_OSZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_OSZ_CNT	Latched Copy of the Oversized Frame Error Counter.	0x0	R

Frame Checker Odd Preamble Packet Count Register

Register Address: 0x9418, Reset: 0x0000, Name: FC_ODD_PRE_CNT

This register is a latched copy of the odd preamble packet counter register. This register is a count of received frames with an odd number of nibbles in the preamble in 100BASE-TX mode. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the odd preamble packet counter register is latched, which ensures that the odd preamble packet count and receive frame count are synchronized.

Table 87. Bit Descriptions for FC_ODD_PRE_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_PRE_ODD_CNT	Latched Copy of the Odd Preamble Packet Counter	0x0	R

Frame Checker Dribble Bits Frame Count Register

Register Address: 0x941A, Reset: 0x0000, Name: FC_DRIBBLE_BITS_CNT

This register is a latched copy of the dribble bits frame counter register. This register is a count of received frames with a noninteger number of nibbles in 10BASE-T mode. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the dribble bits frame counter register is latched, which ensures that the dribble bits frame count and receive frame count are synchronized.

Table 88. Bit Descriptions for FC_DRIBBLE_BITS_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_DRIBBLE_BITS_CNT	Latched Copy of the Dribble Bits Frame Counter.	0x0	R

Frame Checker False Carrier Count Register

Register Address: 0x941B, Reset: 0x0000, Name: FC_FALSE_CARRIER_CNT

This register is a latched copy of the false carrier events counter register. This is a count of the number of times the BAD SSD state is entered. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the false carrier events counter register is latched, which ensures that the false carrier events count and receive frame count are synchronized.

Table 89. Bit Descriptions for FC_FALSE_CARRIER_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FALSE_CARRIER_CNT	Latched Copy of the False Carrier Events Counter.	0x0	R

Frame Generator Enable Register

Register Address: 0x9422, Reset: 0x0000, Name: FG_EN

This register is used to enable the frame generator. When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator, the diagnostic clock must also be enabled. Set the DIAG_CLK_EN bit (PHY_CTRL_1 register, Address 0x0012, Bit 2).

Table 90. Bit Descriptions for FG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 90. Bit Descriptions for FG_EN (Continued)

Bits	Bit Name	Description	Reset	Access
0	FG_EN	When set, this bit enables the built-in frame generator.	0x0	R/W

Frame Generator Control and Restart Register

Register Address: 0x9423, Reset: 0x0001, Name: FG_CNTRL_RSTRT

This register provides frame generator control and restart functions.

Table 91. Bit Descriptions for FG_CNTRL_RSTRT

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	FG_RSTRT	When set, this bit restarts the frame generator. This bit is self-clearing.	0x0	R/W SC
[2:0]	FG_CNTRL	This bit field controls the frame generator in accordance with the following encoding: 111: reserved. 110: reserved. 101: data field decrementing from 255 (decimal) to 0. 100: alternative 0x55 in the MAC client data frame field. 011: all ones in the MAC client data frame field. 010: all zeros in the MAC client data frame field. 001: random number in the MAC client data frame field. 000: no frames after completion of current frame	0x1	R/W

Frame Generator Continuous Mode Enable Register

Register Address: 0x9424, Reset: 0x0000, Name: FG_CONT_MODE_EN

This register is used to put the frame generator into continuous mode. The default mode of operation is burst mode, where the number of frames generated is specified by the FG_NFRM_H register and FG_NFRM_L register (Address 0x941C and Address 0x941D).

Table 92. Bit Descriptions for FG_CONT_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_CONT_MODE_EN	This bit is used to put the frame generator into continuous mode or burst mode. 1: frame generator operates in continuous mode. In this mode, the frame generator keeps generating frames indefinitely. 0: frame generator operates in burst mode. In this mode, the frame generator generates a single burst of frames and then stops. The number of frames in the burst is determined by the FG_NFRM_H register and FG_NFRM_L register.	0x0	R/W

Frame Generator Interrupt Enable Register

Register Address: 0x9425, Reset: 0x0000, Name: FG_IRQ_EN

This register is used to enable the frame generator interrupt. An interrupt is generated when the requested number of frames has been generated. Enable the frame checker/generator interrupt in the IRQ_MASK register. Set the FC_FG_IRQ_EN bit (Address 0x0018, Bit 7). The interrupt status can be read via the IRQ_STATUS register, FC_FG_IRQ_STAT bit (Address 0x0019, Bit 7)

Table 93. Bit Descriptions for FG_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_IRQ_EN	When set, this bit indicates that the frame generator must generate an interrupt when it has transmitted the programmed number of frames. 1: enable the frame generator interrupt. 0: disable the frame generator interrupt.	0x0	R/W

REGISTER SUMMARY

Frame Generator Frame Length Register

Register Address: 0x9427, Reset: 0x006B, Name: FG_FRM_LEN

This register specifies the MAC client data field frame length in bytes. In addition to the data field, 6 bytes are added for the source address, 6 bytes for the destination address, 2 bytes for the length field, and 4 bytes for the frame check sequence (FCS). The total frame length is the data field length plus 18

Table 94. Bit Descriptions for FG_FRM_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_FRM_LEN	The Data Field Frame Length in Bytes.	0x6B	R/W

Frame Generator Interframe Gap Register

Register Address: 0x9428, Reset: 0x000C, Name: FG_IFG_LEN

This register specifies the length in bytes of the interframe gap to be inserted between frames by the frame generator.

Table 95. Bit Descriptions for FG_IFG_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_IFG_LEN	Interframe gap length in bytes.	0xC	R/W

Frame Generator Number of Frames High Register

Register Address: 0x9429, Reset: 0x0000, Name: FG_NFRM_H

This register is Bits [31:16] of a 32-bit register that specifics the number of frames to be generated each time the frame generator is enabled or restarted.

Table 96. Bit Descriptions for FG_NFRM_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_H	Bits [31:16] of the Number of Frames to be Generated.	0x0	R/W

Frame Generator Number of Frames Low Register

Register Address: 0x942A, Reset: 0x0100, Name: FG_NFRM_L

This register is Bits [15:0] of a 32-bit register that specifics the number of frames to be generated each time the frame generator is enabled or restarted.

Table 97. Bit Descriptions for FG_NFRM_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_L	Bits [15:0] of the Number of Frames to be Generated.	0x100	R/W

Frame Generator Done Register

Register Address: 0x942B, Reset: 0x0000, Name: FG_DONE

This register is used to indicate that the frame generator has completed the generation of the number of frames requested in the FG_NFRM_H register and FG_NFRM_L register (Address 0x941C and Address 0x941D, respectively).

Table 98. Bit Descriptions for FG_DONE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_DONE	This bit reads as 1'b1 to indicate that the generation of frames has completed. When set, this bit goes high, and it latches high until it is unlatched by reading.	0x0	R LH

REGISTER SUMMARY

FIFO_SYNC Register

Register Address: 0x944B, Reset: 0x0000, Name: FIFO_SYNC

When set, the transmit FIFO is configured for synchronous operation (except in 1000BASE-T follower mode) to minimize latency.

Table 99. Bit Descriptions for FIFO_SYNC

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FIFO_SYNC	When set, the transmit FIFO is configured for synchronous operation (except in 1000BASE-T follower mode) to minimize latency.	0x0	R/W

Start of Packet Control Register

Register Address: 0x944C, Reset: 0x0E64, Name: SOP_CTRL

This register controls the start of packet (SOP) detection for IEEE 1588-time stamp controls.

Table 100. Bit Descriptions for SOP_CTRL

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0xE	R
[7:5]	SOP_N_8_CYCM_1	When the SOP_NCYC_EN register is set, this register specifies the number of cycles of the GMII/MII RX_CLK clock that the transmit and receive SOP indications remain asserted. Add 1 to the value specified and then multiply by 8 to get the number of cycles. Note that the SOP indications will always be de-asserted at the end of the frame.	0x3	R/W
4	SOP_NCYC_EN	When this register is set, the duration of the transmit and receive SOP indications are defined by the SOP_N_8_CYCM_1 register. Otherwise, the SOP indications are set for the duration of the frame	0x0	R/W
3	RESERVED	Reserved.	0x0	R/W
2	SOP_SFD_EN	When this bit is set, SFD detection is enabled, so that the SOP signals are asserted when the SFD in the frame is detected. If this register bit is cleared, the SOP signals are asserted on the first byte or nibble of the frame. Note that if this signal is changed while packets are being transmitted or received, the SOP signals may be wrongly asserted. Therefore, only change the signal while the link is down or when SOP_TX_EN and SOP_RX_EN are cleared.	0x1	R/W
1	SOP_RX_EN	When set this register enables the generation of SOP detection for received frames.	0x0	R/W
0	SOP_TX_EN	When set this register enables the generation of SOP detection for transmitted frames. To minimize the SOP indication variation, the detection is done after the transmit FIFO for modes in which the transmit FIFO is used.	0x0	R/W

Start of Packet Receive Detection Delay Register

Register Address: 0x944D, Reset: 0x0000, Name: SOP_RX_DEL

This register controls the receive side SOP detection delay.

Table 101. Bit Descriptions for SOP_RX_DEL

Bits	Bit Name	Description	Reset	Access
[15:11]	SOP_RX_10_DEL_NCYC	This register specifies the number of cycles of the GMII/MII RX_CLK clock to delay the received frames SOP indication for 10BASE-T links.	0x0	R/W
[10:6]	SOP_RX_100_DEL_NCYC	This register specifies the number of cycles of the GMII/MII RX_CLK clock to delay the received frames SOP indication for 100BASE-TX links.	0x0	R/W
[5:0]	SOP_RX_1000_DEL_NCYC	This register specifies the number of cycles of the GMII/MII RX_CLK clock to delay the received frames SOP indication for 1000BASE-T links. It is mainly intended to support MAC interfaces with long latency in Gigabit mode (like SGMII) so that the received frame SOP indication is not asserted before the MAC receives the frame.	0x0	R/W

REGISTER SUMMARY

Start of Packet Transmit Detection Delay Register

Register Address: 0x944E, Reset: 0x0000, Name: SOP_TX_DEL

This register controls the transmit side SOP detection delay.

Table 102. Bit Descriptions for SOP_TX_DEL

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	SOP_TX_10_DEL_N_8_NS	This register specifies the number of 8ns periods to delay the transmitted frames SOP indication for 10BASE-T links. To align the TX SOP indication assertion close to the reference point set on the MDI pins this register should be set to 5'd20	0x0	R/W
[7:4]	SOP_TX_100_DEL_N_8_NS	This register specifies the number of 8ns periods to delay the transmitted frames SOP indication for 100BASE-TX links. To align the TX SOP indication assertion close to the reference point set on the MDI pins this register should be set to 4'd0.	0x0	R/W
[3:0]	SOP_TX_1000DEL_N_8_NS	This register specifies the number of 8ns periods to delay the transmitted frames SOP indication for 1000BASE-T links. To align the TX SOP indication assertion close to the reference point set on the MDI pins (so that the timestamping point does not have to be adjusted at the MAC/Switch side) this register should be set to 4'd6.	0x0	R/W

Control of FIFO Depth for MII Modes Register

Register Address: 0x9602, Reset: 0x0001, Name: DPTH_MII_BYTE

FIFO depth in bytes in MII modes.

Table 103. Bit Descriptions for DPTH_MII_BYTE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	DPTH_MII_BYTE	Applies to MII modes for 10Mbps and 100Mbps. When set, the FIFO depth is in bytes. When zero, the FIFO depth is in nibbles. The default value of this bit is 1. Therefore, the FIFO prefill is set in bytes. In MII mode, because the interface is nibble based, the internal prefill in the transmit FIFO is larger and, therefore, the latency is longer.	0x1	R/W

LPI Wake Error Count Register

Register Address: 0xA000, Reset: 0x0000, Name: LPI_WAKE_ERR_CNT

This address corresponds to the EEE wake error counter register specified in Clause 45.2.3.10 of IEEE Standard 802.3, which in the IEEE standard is at MMD Register Address 3.22.

Table 104. Bit Descriptions for LPI_WAKE_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	LPI_WAKE_ERR_CNT	This bit field counts wake time faults where the PHY fails to complete its normal wake sequence within the time required. This field self clears upon reading	0x0	R SC

Base 1000 Retrain Enable Register

Register Address: 0xA001, Reset: 0x0000, Name: B_1000_RTRN_EN

This register allows 1000BASE-T retrain to be enabled. When 1000BASE-T retrain is enabled and the receiver status becomes not okay, the PHY retrains. During this time, the link remains up but it is not possible to transmit or receive data. When 1000BASE-T retrain is disabled and the receiver status becomes not okay, the PHY drops the link.

Table 105. Bit Descriptions for B_1000_RTRN_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 105. Bit Descriptions for B_1000_RTRN_EN (Continued)

Bits	Bit Name	Description	Reset	Access
0	B1000_RTRN_EN	When set, this bit enables 1000BASE-T retrain.	0x0	R/W

Base 10e Enable Register

Register Address: 0xB403, Reset: 0x0000, Name: B_10_E_EN

When set, this register enables 10BASE-Te operation. 10BASE-Te is a variant of 10BASE-T that transmits at a lower voltage level.

Table 106. Bit Descriptions for B_10_E_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	B_10_E_EN	10BASE-Te. When set, this bit enables 10BASE-Te operation. 10BASE-Te is a variant of 10BASE-T that transmits at a lower voltage level.	0x0	R/W

10BASE-T Transmit Test Mode Register

Register Address: 0xB412, Reset: 0x0000, Name: B_10_TX_TST_MODE

This register provides the ability to transmit a 10BASE-T test signal.

Table 107. Bit Descriptions for B_10_TX_TST_MODE

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	B_10_TX_TST_MODE	The PHY provides the ability to transmit a 10BASE-T test signal consisting of either a 5MHz or a 10MHz square wave. The B10_TX_TST_MODE register controls the 10BASE-T test signal in accordance with the following encoding: 011: Transmit 5MHz square wave on dimension 1010: Transmit 5MHz square wave on dimension 0010: Transmit 10MHz square wave on dimension 1001: Transmit 10MHz square wave on dimension 0000: 10BASE-T test mode disabled These test signals are intended to be used for making various measurements as specified in IEEE Std 1802.3d.	0x0	R/W

100BASE-TX Transmit Test Mode Register

Register Address: 0xB413, Reset: 0x0000, Name: B_100_TX_TST_MODE

This register provides the ability to transmit a 100BASE-TX test signal.

Table 108. Bit Descriptions for B_100_TX_TST_MODE

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	B_100_TX_TST_MODE	The PHY provides the ability to transmit a 100BASE-TX test signal that cycles continuously through the valid MLT3 signal levels: zero, positive, zero, and negative. Each transmit level can be held for either 16ns (short dwell time) or 112ns (long dwell time). The MLT3 transmit test waveform with a 16ns dwell time measures duty cycle distortion, as specified in Clause 9.1.8 of ANSI Standard X3.263. The MLT3 transmit test waveform with a 112ns dwell time measures waveform overshoot, amplitude symmetry, and rise/fall times, as specified in Clauses 9.1.3, 9.1.4, and 9.1.6 of ANSI Standard X3.263. 111: reserved. 110: reserved. 101: reserved. 100: transmit MLT3 test waveform, 112 ns dwell time on Dimension 1. 011: transmit MLT3 test waveform, 112ns dwell time on Dimension 0. 010: transmit MLT3 test waveform, 16ns dwell time on Dimension 1.	0x0	R/W

REGISTER SUMMARY

Table 108. Bit Descriptions for B_100_TX_TST_MODE (Continued)

Bits	Bit Name	Description	Reset	Access
		001: transmit MLT3 test waveform, 16ns dwell time on Dimension 0. 000: 100BASE-TX test mode disabled		

Low Power Termination Register

Register Address: 0xB685, Reset: 0x0001, Name: B_100_ZPTM_EN_DIMRX

Low power termination for receive dimension 100BASE-TX Register. This register provides the ability to configure for the lowest common-mode impedance on the receive pair for 100BASE-TX.

Table 109. Bit Descriptions for B_100_ZPTM_EN_DIMRX

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	B_100_ZPTM_EN_DIMRX	Applies to 100BASE-TX.Set to 1 to configure for normal termination on the receive dimension, lowest power (default).Set to 0 to configure for lowest common mode impedance.	0x1	R/W

Run Automated Cable Diagnostics Register

Register Address: 0xBA1B, Reset: 0x0000, Name: CDIAG_RUN

This register is used to start the automated running of cable diagnostics and to return results in the cable diagnostic results registers.

Table 110. Bit Descriptions for CDIAG_RUN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CDIAG_RUN	When set, this bit starts an automatic cable diagnostic run. Run this bit with the PHY in standby. Clear the LINK_EN bit (PHY_CTRL_3 register, Address 0x0017, Bit 13). This bit self clears when the cable diagnostics are completed	0x0	R/W SC

Cable Diagnostics Cross Pair Fault Checking Disable Register

Register Address: 0xBA1C, Reset: 0x0000, Name: CDIAG_XPAIR_DIS

Cable Diagnostics Cross Pair Fault Checking Disable Register. This register allows the checking of cross pair faults in the cable diagnostics to be disabled.

Table 111. Bit Descriptions for CDIAG_XPAIR_DIS

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CDIAG_XPAIR_DIS	When set, this bit disables cross pair fault checking. 1: disable cross pair fault checking. 0: enable cross pair fault checking.	0x0	R/W

Cable Diagnostics Results 0 Register

Register Address: 0xBA1D, Reset: 0x0000, Name: CDIAG_DTLD_RSLTS_0

This register provides cable diagnostics results for Pair 0.

Table 112. Bit Descriptions for CDIAG_DTLD_RSLTS_0

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CDIAG_RSLT_0_BSY	When set, this bit indicates that Pair 0 is busy. This bit indicates that there was unknown activity on Pair 0 during cable diagnostics.	0x0	R

REGISTER SUMMARY

Table 112. Bit Descriptions for CDIAG_DTLD_RSLTS_0 (Continued)

Bits	Bit Name	Description	Reset	Access
9	CDIAG_RSLT_0_XSIM_3	When set, this bit indicates that there is a significant impedance cross pair short between Pair 0 and Pair 3	0x0	R
8	CDIAG_RSLT_0_XSIM_2	When set, this bit indicates that there is a significant impedance cross pair short between Pair 0 and Pair 2.	0x0	R
7	CDIAG_RSLT_0_XSIM_1	When set, this bit indicates that there is a significant impedance cross pair short between Pair 0 and Pair 1	0x0	R
6	CDIAG_RSLT_0_SIM	When set, this bit indicates that there is a significant impedance mismatch on Pair 0.	0x0	R
5	CDIAG_RSLT_0_XSHRT_3	When set, this bit indicates that there is a cross pair short between Pair 0 and Pair 3.	0x0	R
4	CDIAG_RSLT_0_XSHRT_2	When set, this bit indicates that there is a cross pair short between Pair 0 and Pair 2	0x0	R
3	CDIAG_RSLT_0_XSHRT_1	When set, this bit indicates that there is a cross pair short between Pair 0 and Pair 1.	0x0	R
2	CDIAG_RSLT_0_SHRT	When set, this bit indicates that there is a short on Pair 0	0x0	R
1	CDIAG_RSLT_0_OPN	When set, this bit indicates that there is an open on Pair 0	0x0	R
0	CDIAG_RSLT_0_GD	When set, this bit indicates that Pair 0 is well terminated.	0x0	R

Cable Diagnostics Results 1 Register

Register Address: 0xBA1E, Reset: 0x0000, Name: CDIAG_DTLD_RSLTS_1

This register provides cable diagnostics results for Pair 1.

Table 113. Bit Descriptions for CDIAG_DTLD_RSLTS_1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CDIAG_RSLT_1_BSY	When set, this bit indicates Pair 1 is busy. This bit indicates that there was unknown activity on Pair 1 during cable diagnostics.	0x0	R
9	CDIAG_RSLT_1_XSIM_3	When set, this bit indicates that there is a significant impedance cross pair short between Pair 1 and Pair 3.	0x0	R
8	CDIAG_RSLT_1_XSIM_2	When set, this bit indicates that there is a significant impedance cross pair short between Pair 1 and Pair 2.	0x0	R
7	CDIAG_RSLT_1_XSIM_0	When set, this bit indicates that there is a significant impedance cross pair short between Pair 1 and Pair 0.	0x0	R
6	CDIAG_RSLT_1_SIM	When set, this bit indicates that there is a significant impedance mismatch on Pair 1.	0x0	R
5	CDIAG_RSLT_1_XSHRT_3	When set, this bit indicates that there is a cross pair short between Pair 1 and Pair 3.	0x0	R
4	CDIAG_RSLT_1_XSHRT_2	When set, this bit indicates that there is a cross pair short between Pair 1 and Pair 2.	0x0	R
3	CDIAG_RSLT_1_XSHRT_0	When set, this bit indicates that there is a cross pair short between Pair 1 and Pair 0.	0x0	R
2	CDIAG_RSLT_1_SHRT	When set, this bit indicates that there is a short on Pair 1	0x0	R
1	CDIAG_RSLT_1_OPN	When set, this bit indicates that there is an open on Pair 1.	0x0	R
0	CDIAG_RSLT_1_GD	When set, this bit indicates that Pair 1 is well terminated.	0x0	R

Cable Diagnostics Results 2 Register

Register Address: 0xBA1F, Reset: 0x0000, Name: CDIAG_DTLD_RSLTS_2

This register provides cable diagnostics results for Pair 2.

Table 114. Bit Descriptions for CDIAG_DTLD_RSLTS_2

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CDIAG_RSLT_2_BSY	When set, this bit indicates that Pair 2 is busy. This bit indicates that there was unknown activity on Pair 2 during cable diagnostics	0x0	R
9	CDIAG_RSLT_2_XSIM_3	When set, this bit indicates that there is a significant impedance cross pair short between Pair 2 and Pair 3.	0x0	R

REGISTER SUMMARY

Table 114. Bit Descriptions for CDIAG_DTLD_RSLTS_2 (Continued)

Bits	Bit Name	Description	Reset	Access
8	CDIAG_RSLT_2_XSIM_1	When set, this bit indicates that there is a significant impedance cross pair short between Pair 2 and Pair 1.	0x0	R
7	CDIAG_RSLT_2_XSIM_0	When set, this bit indicates that there is a significant impedance cross pair short between Pair 2 and Pair 0.	0x0	R
6	CDIAG_RSLT_2_SIM	When set, this bit indicates that there is a significant impedance mismatch on Pair 2.	0x0	R
5	CDIAG_RSLT_2_XSHRT_3	When set, this bit indicates that there is a cross pair short between Pair 2 and Pair 3.	0x0	R
4	CDIAG_RSLT_2_XSHRT_1	When set, this bit indicates that there is a cross pair short between Pair 2 and Pair 1.	0x0	R
3	CDIAG_RSLT_2_XSHRT_0	When set, this bit indicates that there is a cross pair short between Pair 2 and Pair 0.	0x0	R
2	CDIAG_RSLT_2_SHRT	When set, this bit indicates that there is a short on Pair 2.	0x0	R
1	CDIAG_RSLT_2_OPN	When set, this bit indicates that there is an open on Pair 2.	0x0	R
0	CDIAG_RSLT_2_GD	When set, this bit indicates that Pair 2 is well terminated.	0x0	R

Cable Diagnostics Results 3 Register

Register Address: 0xBA20, Reset: 0x0000, Name: CDIAG_DTLD_RSLTS_3

This register provides cable diagnostics results for Pair 3.

Table 115. Bit Descriptions for CDIAG_DTLD_RSLTS_3

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CDIAG_RSLT_3_BSY	When set, this bit indicates that Pair 3 is busy. This bit indicates that there was unknown activity on Pair 3 during cable diagnostics.	0x0	R
9	CDIAG_RSLT_3_XSIM_2	When set, this bit indicates that there is a significant impedance cross pair short between Pair 3 and Pair 2.	0x0	R
8	CDIAG_RSLT_3_XSIM_1	When set, this bit indicates that there is a significant impedance cross pair short between Pair 3 and Pair 1.	0x0	R
7	CDIAG_RSLT_3_XSIM_0	When set, this bit indicates that there is a significant impedance cross pair short between Pair 3 and Pair 0.	0x0	R
6	CDIAG_RSLT_3_SIM	When set, this bit indicates that there is a significant impedance mismatch on Pair 3	0x0	R
5	CDIAG_RSLT_3_XSHRT_2	When set, this bit indicates that there is a cross pair short between Pair 3 and Pair 2.	0x0	R
4	CDIAG_RSLT_3_XSHRT_1	When set, this bit indicates that there is a cross pair short between Pair 3 and Pair 1.	0x0	R
3	CDIAG_RSLT_3_XSHRT_0	When set, this bit indicates that there is a cross pair short between Pair 3 and Pair 0.	0x0	R
2	CDIAG_RSLT_3_SHRT	When set, this bit indicates that there is a short on Pair 3.	0x0	R
1	CDIAG_RSLT_3_OPN	When set, this bit indicates that there is an open on Pair 3.	0x0	R
0	CDIAG_RSLT_3_GD	When set, this bit indicates that Pair 3 is well terminated.	0x0	R

Cable Diagnostics Fault Distance Pair 0 Register

Register Address: 0xBA21, Reset: 0x00FF, Name: CDIAG_FLT_DIST_0

This register provides the distance to the first fault on Pair 0.

Table 116. Bit Descriptions for CDIAG_FLT_DIST_0

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_FLT_DIST_0	This bit field provides the distance to the first fault on Pair 0 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Fault Distance Pair 1 Register

Register Address: 0xBA22, Reset: 0x00FF, Name: CDIAG_FLT_DIST_1

REGISTER SUMMARY

This register provides the distance to the first fault on Pair 1.

Table 117. Bit Descriptions for CDIAG_FLT_DIST_1

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_FLT_DIST_1	This bit field provides the distance to the first fault on Pair 1 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Fault Distance Pair 2 Register

Register Address: 0xBA23, Reset: 0x00FF, Name: CDIAG_FLT_DIST_2

This register provides the distance to the first fault on Pair 2.

Table 118. Bit Descriptions for CDIAG_FLT_DIST_2

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_FLT_DIST_2	This bit field provides the distance to the first fault on Pair 2 in meters. A value of 0xFF indicates an unknown result	0xFF	R

Cable Diagnostics Fault Distance Pair 3 Register

Register Address: 0xBA24, Reset: 0x00FF, Name: CDIAG_FLT_DIST_3

This register provides the distance to the first fault on Pair 3.

Table 119. Bit Descriptions for CDIAG_FLT_DIST_3

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_FLT_DIST_3	This bit field provides the distance to the first fault on Pair 3 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Cable Length Estimate Register

Register Address: 0xBA25, Reset: 0x00FF, Name: CDIAG_CBL_LEN_EST

This register provides an estimate of the cable length in meters based on the signal processing and is estimated during link establishment for 100BASE-TX and 1000BASE-T.

Table 120. Bit Descriptions for CDIAG_CBL_LEN_EST

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_CBL_LEN_EST	This bit field provides a cable length estimate in meters. A value of 0xFF indicates an unknown result.	0xFF	R

LED Pulse Stretching Duration Register

Register Address: 0xBC00, Reset: 0x0011, Name: LED_PUL_STR_DUR

When the LED_PUL_STR_DUR_SEL bit field in the LED_CTRL_1 register (Address 0x001B, Bits[3:2]) is set to 2'b11, the LED_PUL_STR_DUR register determines the LED pulse stretching duration

Table 121. Bit Descriptions for LED_PUL_STR_DUR

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 121. Bit Descriptions for LED_PUL_STR_DUR (Continued)

Bits	Bit Name	Description	Reset	Access
[5:0]	LED_PUL_STR_DUR	When the LED_PUL_STR_DUR_SEL bit field in the LED_CTRL_1 register (Address 0x001B, Bits [3:2]) is set to 2'b11, the LED_PUL_STR_DUR bit field determines the LED pulse stretching duration. Multiply the value specified by 8 to determine the duration in milliseconds.	0x11	R/W

SERDES SUBSYSTEM REGISTER SUMMARY

The SerDes Subsystem registers are made up of the following three register groupings:

- 0x0000 to 0x000F, IEEE standard registers
- 0x0010 to 0x0019, vendor specific registers
- SerDes Subsystem EMI registers at Device Address 0x1E

The IEEE standard registers and vendor-specific registers are duplicated in the SerDes subsystem EMI registers at device address 0x1E, with an offset address of 0xFC00. For simplicity, the duplicate addresses from 0xFC00 to 0xFC19 are not shown in Table 122. The Fiber IEEE standard registers and vendor specific registers are only accessible RGMII/RMII/MII to Fiber, and RGMII to Backplane modes.

The IEEE standard registers and vendor specific registers are accessed using Clause 22 access, and the EMI registers are accessed using Clause 45 access. The ADIN1320 supports the IEEE Clause 45 MDIO manageable device (MMD) registers associated with EEE. These registers are all remapped to the Device Address 0x1E, so they are available at the same device address as the rest of the PHY extended management registers. For systems that do not support the interface specified under Clause 45, the EMI registers can be accessed using Clause 22 access via Register 0x0010 and Register 0x0011.The SerDes Subsystem EMI registers are only accessible in SGMII to Copper, RGMII/RMII/MII to Fiber, RGMII to Backplane, Media Converter, and SGMII-RGMII Bridge Modes.

The default value of some of the registers are determined by the hardware configuration settings, which are read just after the RESET_N pin is deasserted (see the Hardware Configuration Pins section). This allows the default operation of the ADIN1320 to be configured in unmanaged applications. The default values in Table 122 assume the ADIN1320 is configured in RGMII to 1000BASE-X Full Duplex (FD) mode.

Table 122. SerDes Subsystem Register Summary

Register Address	Name	Description	Reset	Access
0x0000	SD_CONTROL	SerDes Subsystem Control Register.	0x2100	R/W
0x0001	SD_STATUS	SerDes Subsystem Status Register.	0x0141	R
0x0004	SD_AUTONEG_ADV	SerDes Subsystem Autonegotiation Advertisement Register.	0x00020	R/W
0x0005	SD_LP_ABILITY	SerDes Subsystem Autonegotiation Link Partner Base Page Ability Register.	0x0000	R
0x0006	SD_AUTONEG_EXP	SerDes Subsystem Autonegotiation Expansion Register.	0x0004	R
0x0007	SD_TX_NEXT_PAGE	SerDes Subsystem Autonegotiation Next Page Transmit Register.	0x2001	R/W
0x0008	SD_LP_RX_NEXT_PAGE	SerDes Subsystem Autonegotiation Link Partner Received Next Page Register.	0x0000	R
0x000F	SD_EXT_STATUS	SerDes Subsystem Extended Status Register.	0x0000	R
0x0013	SD_PHY_CTRL_1	SerDes Subsystem PHY Control 1 Register.	0x0002	R/W
0x0015	SD_PHY_CTRL_STATUS_2	SerDes Subsystem PHY Control Status 1 Register.	0x0020	R/W
0x0016	SD_PHY_CTRL_2	SerDes Subsystem PHY Control 2 Register.	0x0000	R/W
0x0018	SD_IRQ_MASK	SerDes Subsystem Interrupt Mask Register.	0x0000	R/W
0x0019	SD_IRQ_STATUS	SerDes Subsystem Interrupt Status Register.	0x0000	R
0xFC21	SD_ONS_CTRL	SerDes Subsystem Odd Nibble Suppression Control Registers.	0x0000	R/W
0xFC22	SD_SGMII_CONTROL_0	SGMII Control Register 0.	0x0140	R/W
0xFC23	SD_SGMII_CONTROL_1	SGMII Control Register 1.	0x0000	R/W
0xFC24	SD_RA_CNTRL	SerDes Subsystem Rate Adaptation Control.	0x0000	R/W
0xFC26	SD_HBX_CNTRL_0	HBX Wrap Control Register 0.	0xA961	R/W
0xFC27	SD_HBX_CNTRL_1	HBX Wrap Control Register 1.	0x1907	R/W
0xFC28	SD_SGMII_AN_LNK_TMR_N_100US	SGMII Autonegotiation Timer.	0x0010	R/W

REGISTER SUMMARY

Table 122. SerDes Subsystem Register Summary (Continued)

Register Address	Name	Description	Reset	Access
0xFC29	SD_1000X_AN_LNK_TMR_N_100US	1000BASE-X Autonegotiation Timer.	0x0064	R/W
0xFC2A	SD_1000X_PCS_TMRS	PCS 1000BASE-X Timer Register.	0x0F0F	R/W
0xFC2B	SD_1000X_PCS_TEST_CTRL_1	Test Control Register for 1000BASE-X PMDs.	0x0000	R/W
0xFC2C	SD_1000X_PCS_CTRL	1000BASE-X PCS Control Register.	0x0000	R/W
0xFC2D	SD_FC_EN	SerDes Subsystem Frame Checker Enable Register.	0x0001	R/W
0xFC2F	SD_FC_IRQ_EN	SerDes Subsystem Frame Checker Interrupt Enable Register.	0x0001	R/W
0xFC30	SD_FC_TX_SEL	SerDes Subsystem Frame Checker Transmit Select Register.	0x0000	R/W
0xFC37	SD_FC_MAX_FRM_SIZE	SerDes Subsystem Frame Checker Max Frame Size Register.	0x05F2	R/W
0xFC3A	SD_FC_ERR_CNT	SerDes Frame Checker Error Counter Register	0x0000	R
0xFC3B	SD_FC_FRM_CNT_H	SerDes Subsystem Frame Checker Count High Register.	0x0000	R
0xFC3C	SD_FC_FRM_CNT_L	SerDes Subsystem Frame Checker Count Low Register.	0x0000	R
0xFC3D	SD_FC_ALGN_ERR_CNT	SerDes Subsystem Frame Checker Alignment Error Count Register.	0x0000	R
0xFC3F	SD_FC_SYMB_ERR_CNT	SerDes Subsystem Frame Checker Symbol Error Counter Register.	0x0000	R
0xFC40	SD_FC_LEN_ERR_CNT	SerDes Subsystem Frame Checker Length Error Count Register.	0x0000	R
0xFC41	SD_FC_USZ_CNT	SerDes Subsystem Frame Checker Undersized Frame Count Register.	0x0000	R
0xFC42	SD_FC_OSZ_CNT	SerDes Subsystem Frame Checker Oversized Frame Count.	0x0000	R
0xFC43	SD_FC_PRE_ODD_CNT	SerDes Subsystem Frame Checker Odd Preamble Packet Count Register.	0x0000	R
0xFC45	SD_FC_DRIBBLE_BITS_CNT	SerDes Subsystem Frame Checker Dribble Bits Count Register.	0x0000	R
0xFC46	SD_FC_FALSE_CARRIER_CNT	SerDes Subsystem Frame Checker False Carrier Count Register.	0x0000	R
0xFC4D	SD_FG_EN	SerDes Subsystem Frame Generator Enable Register.	0x0000	R/W
0xFC4E	SD_FG_CNTRL_RSTRT	SerDes Subsystem Frame Generator Control and Restart Register.	0x0001	R/W
0xFC4F	SD_FG_CONT_MODE_EN	SerDes Subsystem Frame Generator Continuous Mode Enable Register.	0x0000	R/W
0xFC50	SD_FG_IRQ_EN	SerDes Subsystem Frame Generator Interrupt Enable Register.	0x0000	R/W
0xFC52	SD_FG_FRM_LEN	SerDes Subsystem Frame Generator Frame Length Register.	0x006B	R/W
0xFC54	SD_FG_NFRM_H	SerDes Subsystem Frame Generator Number of Frames High Register.	0x0000	R/W
0xFC55	SD_FG_NFRM_L	SerDes Subsystem Frame Generator Number of Frames Low Register.	0x0100	R/W
0xFC56	SD_FG_DONE	SerDes Subsystem Frame Generator Done Register.	0x0000	R
0xFC78	SDTXEBUFCTRL	SerDes Subsystem TX FIFO Control Register.	0x0000	R/W
0xFC79	SD_TX_E_BUF_TH_1G	SerDes Subsystem FIFO Latency Threshold Register.	0x0550	R/W
0xFC7A	SD_TX_E_BUF_TH_MII	SerDes Subsystem FIFO Latency Threshold Register.	0x0761	R/W
0xFC80	SD_HB_X_CNTRL_2	SerDes Subsystem HBX Wrap Control Register 2.	0x1A46	R/W
0xFC81	SD_HB_X_CNTRL_3	SerDes Subsystem HBX Wrap Control Register 3.	0x0032	R/W
0xFC88	SD_SOP_CTRL	SerDes Subsystem Start of Packet Control.	0x0CE7	R/W
0xFC89	SD_SOP_RX_DEL	SerDes Subsystem Start of Packet Receive Detection Delay Register.	0x0000	R/W
0xFC8A	SD_SOP_TX_DEL	SerDes Subsystem Start of Packet Transmit Detection Delay Register.	0x0000	R/W
0xFC9B	SD_FIB_LED_PAT_0	Fiber LED Pattern 0.	0x0055	R/W
0xFC9C	SD_FIBER_LED_PAT_TICK_DUR_0	Fiber LED Pattern Tick Duration Register 0.	0x0018	R/W
0xFC9D	SD_FIB_LED_PAT_PAUSE_DUR_0	Fiber LED Pattern Pause Duration Register 0.	0x0000	R/W
0xFC9E	SD_FIB_LED_PAT_1	Fiber LED Pattern 1.	0x0055	R/W
0xFC9F	SD_FIBER_LED_PAT_TICK_DUR_1	Fiber LED Pattern Tick Duration Register 1.	0x0018	R/W
0xFCA0	SD_FIB_LED_PAT_PAUSE_DUR_1	Fiber LED Patter Pause Duration Register 1.	0x0000	R/W
0xFCA1	SD_FIB_LED_PAT_2	Fiber LED Pattern 2.	0x0055	R/W

REGISTER SUMMARY

Table 122. SerDes Subsystem Register Summary (Continued)

Register Address	Name	Description	Reset	Access
0xFCA2	SD_FIBER_LED_PAT_TICK_DUR_2	Fiber LED Pattern Tick Duration Register 2.	0x0018	R/W
0xFCA3	SD_FIB_LED_PAT_PAUSE_DUR_2	Fiber LED Pattern Pause Duration Register 2.	0x0000	R/W
0xFCA4	SD_FIB_LED_PAT_3	Fiber LED Pattern 3.	0x0055	R/W
0xFCA5	SD_FIBER_LED_PAT_TICK_DUR_3	Fiber LED Pattern Pause Duration Register 3.	0x0018	R/W
0xFCA6	SD_FIB_LED_PAT_PAUSE_DUR_3	Fiber LED Patter Tick Duration Register 3.	0x0000	R/W
0xFCA7	SD_FIB_LED_PUL_STR_EN	Fiber LED Pulse Stretching Register.	0x0001	R/W
0xFCA8	SD_FIB_LED_PUL_STR_DUR_SEL	Fiber LED Pulse Stretching Duration Register.	0x0000	R/W
0xFCA9	SD_FIB_LED_PUL_STR_DUR	Fiber LED Pulse Stretching Duration Register.	0x0011	R/W
0xFCAA	SD_FIB_LED_CFG_0	Fiber LED_0 Configuration Register.	0x0008	R/W
0xFCAB	SD_FIB_LED_CFG_1	Fiber LED_1 Configuration Register.	0x0000	R/W
0xFCAC	SD_FIB_LED_CFG_2	Fiber LED_2 Configuration Register.	0x0001	R/W
0xFCAD	SD_FIB_LED_CFG_3	Fiber LED_3 Configuration Register.	0x0002	R/W
0xFCB6	SD_TBI_LPBK_TX_INH	SerDes Subsystem TX Differential Output Control Register	0x0001	R/W
0xFCC9	SD_HS_LPBK_CFG	SerDes Subsystem High Speed Internal Loopback Control Register	0x0000	R/W
0xFCD0	SD_RFD_CFG	Rotational Frequency Detector Configuration Register	0x0052	R/W

SERDES SUBSYSTEM REGISTER DETAILS

SerDes Control Register

Register Address: 0x0000, Reset: 0x2100, Name: SD_CONTROL

This address corresponds to the SD control register specified in clause 22.2.4.1 of Std 802.3. Note that the default reset value of this register is dependent on hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC00.

Table 123. Bit Descriptions for SD_CONTROL

Bits	Bit Name	Description	Reset	Access
15	SD_SFT_RST	SD Software Reset Bit. 1: SerDes Subsystem reset. 0: normal operation.	0x0	R/W SC
14	SD_LOOPBACK	SD Enable/Disable Loopback Mode. 1: enable loopback mode. 0: disable loopback mode.	0x0	R/W
13	SD_SPEED_SEL_LSB	The speed selection MSB and LSB register bits are used to configure the link speed. The default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. Note that the configuration is only effective if the SD_AN_EN is disabled. 11: reserved. 10: 1 Gbps. 01: 100 Mbps. 00: 10 Mbps.	0x0	R/W
12	SD_AN_EN	The autonegotiation enable bit is used to enable/disable autonegotiation. Note that the default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable autonegotiation process. 0: disable autonegotiation process.	0x0	R/W
11	SD_SFT_PD	SD Software Power-Down Bit. Note that the default value of this register bit is configurable via the hardware configuration pins. The SerDes Subsystem can be held in reset until initialized by the software. 1: SerDes subsystem software power-down. 0: normal operation.	0x0	R/W
10	SD_ISOLATE	Isolate Bit	0x0	R/W

REGISTER SUMMARY

Table 123. Bit Descriptions for SD_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
		1: electrically isolate PHY from MAC interface by setting MAC interface pins to tristate (even if active). 0: normal operation.		
9	SD_RESTART_ANEG	Restart Autonegotiation Bit. Note that this bit is self-clearing. When the autonegotiation process is restarted, this bit returns to 0. 1: restart the autonegotiation process. 0: normal operation.	0x0	R/W SC
8	SD_DPLX_MODE	Duplex Mode Bit. 1: full duplex. 0: half duplex.	0x1	R/W
7	SD_COLTEST	Collision Test Bit. 1: enable collision signal test. 0: disable collision signal test.	0x0	R/W
6	SD_SPEED_SEL_MSB	See SD_SPEED_SEL_LSB Bit Description.	0x0	R/W
5	SD_UNIDIR_EN	The unidirectional enable register bit is read only and always reads as 0. Transmission from the media independent interface is only enabled when the PHY has determined that a valid link has been established.	0x0	R
[4:0]	RESERVED	Reserved.	0x0	R

SerDes Subsystem Status Register

Register Address: 0x0001, Reset: 0x0141, Name: SD_STATUS

This address corresponds to the SerDes Subsystem status register specified in Clause 22.2.4.2 of IEEE Standard 802.3. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC01.

Table 124. Bit Descriptions for SD_STATUS

Bits	Bit Name	Description	Reset	Access
15	SD_T_4_SPRT	The 100BASE-T4 ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
14	SD_FD_100_SPRT	The 100BASE-FX full duplex capability bit in the status register reflects whether the PHY supports 100BASE-FX full duplex technology. This bit will be set to 1 only if the ADIN1320 is configured in 100BASE-FX half duplex or full duplex mode.	0x0	R
13	SD_HD_100_SPRT	The 100BASE-FX half duplex capability bit in the status register reflects whether the PHY supports 100BASE-FX half duplex technology. This bit will be set to 1 only if the ADIN1320 is configured in 100BASE-FX half duplex or full duplex mode.	0x0	R
12	SD_FD_10_SPRT	The 10 Mb/s full duplex ability bit indicates that the PHY supports this technology.	0x0	R
11	SD_HD_10_SPRT	The 10 Mb/s half duplex ability bit indicates that the PHY supports this technology.	0x0	R
10	SD_FD_T_2_SPRT	The 100BASE-T2 full-duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
9	SD_HD_T_2_SPRT	The 100BASE-T2 half-duplex ability bit always reads as 0 to indicate that the PHY does not support this technology.	0x0	R
8	SD_EXT_STAT_SPRT	The extended status support bit indicates that the PHY provides extended status information. This bit always reads as 1, confirming the availability of extended status data in register 0x000F.	0x1	R
7	SD_UNIDIR_ABLE	The unidirectional ability register always reads as 0, indicating that the PHY can only transmit data from the MII once a valid link has been established.	0x0	R
6	SD_MF_PREAM_SUP_ABLE	Management Frame Preamble Suppression Ability Bit. This always reads as 1 because the PHY accepts management frames with preamble suppressed.	0x1	R
5	SD_AN_DONE	Autonegotiation Complete Bit. 1: autonegotiation process completed. 0: autonegotiation process not completed.	0x0	R

REGISTER SUMMARY

Table 124. Bit Descriptions for SD_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
4	SD_REM_FLT_LH	Remote Fault Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: remote fault condition detected. 0: no remote fault condition detected.	0x0	R LH
3	SD_AN_ABLE	Autonegotiation Ability Bit. This bit always reads as 0 for 100BASE-FX, indicating that auto-negotiation is not supported for 100BASE-FX. This bit is only applicable for 1000BASE-X modes. 1: PHY is able to perform autonegotiation. 0: PHY is not able to perform autonegotiation.	0x0	R
2	SD_LINK_STAT_OK_LL	Link Status Bit. If the link subsequently drops, this bit latches low until it is unlatched by reading. 1: link is up. 0: link is down.	0x0	R LL
1	SD_JABBER_DET_LH	When this bit goes high, it latches high until it is unlatched by reading. 1: jabber condition detected. 0: no jabber condition detected.	0x0	R LH
0	SD_EXT_CAPABLE	The extended capability bit always reads as 1, indicating that the PHY provides an extended set of capabilities.	0x1	R

SerDes Subsystem Autonegotiation Advertisement Register

Register Address: 0x0004, Reset: 0x0020, Name: SD_AUTONEG_ADV

This address corresponds to the Autonegotiation Advertisement Register specified in 802.3 clause 22.2.4.3.2 and Clause 37.2.5.1. The default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC04.

Table 125. Bit Descriptions for SD_AUTONEG_ADV

Bits	Bit Name	Description	Reset	Access
15	SD_NEXT_PAGE_ADV	Next page exchange occurs after the base link codewords have been exchanged. Next page exchange consists of using the normal autonegotiation arbitration process to send next page messages. Next page transmission ends when both ends of a link segment set their next page bits to Logic 0, indicating that neither has anything additional to transmit.	0x0	R/W
14	RESERVED	Reserved.	0x0	R
13	SD_REM_FLT_2_ADV	See bit 12 SD_REM_FLT_1_ADV.	0x0	R/W
12	SD_REM_FLT_1_ADV	The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. [RF1:RF2] 11: AN error 10: link failure 01: offline 00: No error, link OK (default)	0x0	R/W
[11:9]	RESERVED	Reserved.	0x0	R
8	SD_APAUSE_ADV	This bit indicates that asymmetric PAUSE operation is supported.	0x0	R/W
7	SD_PAUSE_ADV	This bit indicates that PAUSE operation is supported.	0x0	R/W
6	SD_HD_1000ADV	This bit is to advertise 1000BASE-X half duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications. Note that half duplex is not supported for 1000BASE-KX. This bit is only available when the ADIN1320 is set in 1000BASE-X Half Duplex mode.	0x0	R/W
5	SD_FD_1000ADV	This bit is to advertise 1000BASE-X full duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default	0x1	R/W

REGISTER SUMMARY

Table 125. Bit Descriptions for SD_AUTONEG_ADV (Continued)

Bits	Bit Name	Description	Reset	Access
		operation of the PHY to be configured in unmanaged applications. This bit is only available when the ADIN1320 is set in either 1000BASE-X Full Duplex or 1000BASE-KX mode.		
[4:0]	RESERVED	Reserved.	0x0	R

SerDes Subsystem Autonegotiation Link Partner Base Page Ability Register

Register Address: 0x0005, Reset: 0x0000, Name: SD_LP_ABILITY

This address corresponds to the Autonegotiation Link Partner Base Page Ability Register specified in 802.3 clause 22.2.4.3.3. The default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC05.

Table 126. Bit Descriptions for SD_LP_ABILITY

Bits	Bit Name	Description	Reset	Access
15	SD_LP_NEXT_PAGE	Link Partner Next Page Bit. Next page exchange occurs after the base link code words have been exchanged. Next page exchange consists of using the normal autonegotiation arbitration process to send next page messages. Next page transmission ends when both ends of a link segment set their next page bits to Logic 0, indicating that neither has anything additional to transmit. Note that when SD_SGMII_EN is set to 1 this bit will indicate the Link Partner Link Status. 1: Link Up 0: Link Down	0x0	R
14	SD_LP_ACK	This bit is used by the internal handshaking in autonegotiation and must be ignored. 1: link partner has successfully received its link code word. 0: link partner has not received its link code word.	0x0	R
13	SD_LP_REM_FLT_2	See bit 12 Description. Note that this bit is Reserved when SD_SGMII_EN is set to 1.	0x0	R
12	SD_LP_REM_FLT_1	The link partner remote fault bit provides a standard transport mechanism for the transmission of fault information. [RF1:RF2] 11: AN Error. 10: Link Failure. 01: Offline. 00: No Error, Link OK (Default). Note that when SD_SGMII_EN is set to 1, this bit will indicate Duplex Mode. 01: Full Duplex 10: Half Duplex	0x0	R
[11:9]	RESERVED	Reserved.	0x0	R
8	SD_LP_APAUSE_ABLE	This bit indicates that the link partner advertises asymmetric pause operation for full duplex links.	0x0	R
7	SD_LP_PAUSE_ABLE	This bit indicates that the link partner advertises symmetric pause operation for full duplex links.	0x0	R
6	SD_LP_HD_1000ABLE	This bit indicates that the link partner advertises 1000BASE-X Half Duplex (HD) Capability	0x0	R
5	SD_LP_FD_1000ABLE	This bit indicates that the link partner advertises 1000BASE-X Full Duplex (FD) Capability	0x0	R
[4:0]	RESERVED	Reserved.	0x0	R

SerDes Subsystem Autonegotiation Expansion Register

Register Address: 0x0006, Reset: 0x0004, Name: SD_AUTONEG_EXP

Autonegotiation Expansion Register specified in 802.3 clause 22.2.4.3.4. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC06.

REGISTER SUMMARY

Table 127. Bit Descriptions for SD_AUTONEG_EXP

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	SD_NP_ABLE	The next page ability bit always reads as 1, indicating that the 1000BASE-X supports next pages.	0x1	R
1	SD_PAGE_RX_LH	Page Received Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: a new page has been received. 0: a new page has not been received.	0x0	R LH
0	RESERVED	Reserved.	0x0	R

SerDes SUBSYSTEM AUTONEGOTIATION Next Page Transmit Register

Register Address: 0x0007, Reset: 0x2001, Name: SD_TX_NEXT_PAGE

This address corresponds to the autonegotiation next page transmit register specified in Clause 28.2.4.1.6 and Clause 37.3.5.1 of IEEE Standard 802.3. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC07.

Table 128. Bit Descriptions for SD_TX_NEXT_PAGE

Bits	Bit Name	Description	Reset	Access
15	SD_NP_NEXT_PAGE	Next page (NP) is used by the next page function to indicate that additional next page(s) follow. Otherwise, this is the last next page to be transmitted.	0x0	R/W
14	RESERVED	Reserved.	0x0	R
13	SD_NP_MSG_PAGE	Message page (MP) is used by the next page function to indicate that this is a message page. Otherwise, this is an unformatted page	0x1	R/W
12	SD_NP_ACK_2	Acknowledge 2 (Ack2) is used by the next page function to indicate that a device has the ability to comply with the message.	0x0	R/W
11	SD_NP_TOGGLE	Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit always takes the opposite value of the toggle bit in the previously exchanged link code word.	0x0	R
[10:0]	SD_NP_CODE	Message code field is an 11-bit wide field, encoding 2048 possible messages. If the message page bit is set to Logic 0, the bit encoding of the link code word is interpreted as an unformatted page.	0x1	R/W

SerDes Subsystem Autonegotiation Link Partner Received Next Page Register

Register Address: 0x0008, Reset: 0x0000, Name: SD_LP_RX_NEXT_PAGE

This address corresponds to the autonegotiation link partner received next page register specified in Clause 28.2.4.1.7 of IEEE Standard 802.3. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC08.

Table 129. Bit Descriptions for SD_LP_RX_NEXT_PAGE

Bits	Bit Name	Description	Reset	Access
15	SD_LP_NP_NEXT_PAGE	Link partner next page (NP) is used by the next page function to indicate that the link partner sends additional next page(s). Otherwise, this is the last next page to be transmitted.	0x0	R
14	RESERVED	Reserved.	0x0	R
13	SD_LP_NP_MSG_PAGE	Link partner message page (MP) is used by the next page function to indicate that this is a message page. Otherwise, this is an unformatted page.	0x0	R
12	SD_LP_NP_ACK_2	Acknowledge 2 (Ack2) is used by the next page function to indicate that the link partner has the ability to comply with the message.	0x0	R
11	SD_LP_NP_TOGGLE	Link partner toggle (T) is used by the arbitration function to ensure synchronization with the link partner during the next page exchange. This bit always takes the opposite value of the toggle bit in the previously exchanged link code word.	0x0	R

REGISTER SUMMARY

Table 129. Bit Descriptions for SD_LP_RX_NEXT_PAGE (Continued)

Bits	Bit Name	Description	Reset	Access
[10:0]	SD_LP_NP_CODE	Link partner message code field is an 11-bit wide field, encoding 2048 possible messages. If the message page bit is set to Logic 0, the bit encoding of the link code word is interpreted as an unformatted page.	0x0	R

SerDes Subsystem Extended Status Register

Register Address: 0x000F, Reset: 0x0000, Name: SD_EXT_STATUS

This address corresponds to the extended status register specified in Clause 22.2.4.4 of IEEE Standard 802.3. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC0F.

Table 130. Bit Descriptions for SD_EXT_STATUS

Bits	Bit Name	Description	Reset	Access
15	SD_FD_1000X_SPRT	This bit indicates that the PHY support 1000BASE-X full duplex ability. This bit is set to 1 when the ADIN1320 is configured in 1000BASE-KX, or 1000BASE-X HD or FD.	0x1	R
14	SD_HD_1000X_SPRT	This bit indicates that the PHY support 1000BASE-X half duplex ability. This bit is set to 1 when the ADIN1320 is configured in 1000BASE-X HD or FD mode. Note that Half Duplex not supported for 1000BASE-KX.	0x1	R
13	SD_FD_1000_SPRT	This bit is always zero because the PHY does not support full duplex 1000BASE-T full duplex.	0x0	R
12	SD_HD_1000_SPRT	This bit is always zero because the PHY does not support full duplex 1000BASE-T half duplex.	0x0	R
[11:0]	RESERVED	Reserved.	0x0	R

SerDes Subsystem PHY Control 1 Register

Register Address: 0x0013, Reset: 0x0002, Name: SD_PHY_CTRL_1

This register provides access to Fiber PHY loopback control bits. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC13.

Table 131. Bit Descriptions for SD_PHY_CTRL_1

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	SD_PCS_TBI_LPBK_EN	Ten-bit interface loopback together with loopback enable bit will configure the SerDes Subsystem to loopback the 10-bit data from TX to RX 10-bit interface.	0x1	R/W
0	SD_MII_LPBK_EN	MII loopback together with loopback enable bit will configure the SerDes Subsystem to loop the data it receives back to the transmitter side.	0x0	R/W

SerDes Subsystem PHY Control Status 1 Register

Register Address: 0x0015, Reset: 0x0020, Name: SD_PHY_CTRL_STATUS_2

This register provides access to various Fiber PHY control and status register bits, in particular for auto-negotiation control. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC15.

Table 132. Bit Descriptions for SD_PHY_CTRL_STATUS_2

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	SD_1000X_AN_ERR_RESTART	Enable autonegotiation restart for autonegotiation error scenario. 1: autonegotiation restarts if autonegotiation error occurs.	0x1	R/W

REGISTER SUMMARY

Table 132. Bit Descriptions for SD_PHY_CTRL_STATUS_2 (Continued)

Bits	Bit Name	Description	Reset	Access
		0: autonegotiation does not restarts if autonegotiation error occurs.		
4	SD_1000X_AN_ST_TOST	Asserted when autonegotiation FSM state is either ACKNOWLEDGE_DETECT, COMPLETE_ACKNOWLEDGE, NEXT_PAGE_WAIT, or IDLE_DETECT timed-out	0x0	R
3	SD_1000X_AN_ST_TO_EN	This status signal indicates that the autonegotiation state time-out is enabled.	0x0	R/W
2	RESERVED	Reserved.	0x0	R
1	SD_1000X_AN_AUTO_DIS_STAT	This status signal indicates that the AN process has been automatically disabled.	0x0	R
0	SD_1000X_AN_AUTO_DIS	SerDes autonegotiation automatic disabling function	0x0	R/W

SerDes Subsystem PHY Control 2 Register

Register Address: 0x0016, Reset: 0x0000, Name: SD_PHY_CTRL_2

This register provides access to various Fiber PHY control register bits, in particular for the GROUP_MDIO_EN. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC16.

Table 133. Bit Descriptions for SD_PHY_CTRL_2

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	SD_GROUP_MDIO_EN	The group MDIO enable register bit may be used to place the PHY in group MDIO mode. In this mode, the PHY responds to any write or address operation to PHY address 5'd31 as if it was an access to its own PHY address. It is recommended that this bit be set only when performing specific sequences and then be cleared again.	0x0	R/W
[5:0]	RESERVED	Reserved.	0x0	R

SerDes Subsystem Interrupt Mask Register

Register Address: 0x0018, Reset: 0x0000, Name: SD_IRQ_MASK

The interrupt mask register allows interrupts to be masked or unmasked. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC18.

Table 134. Bit Descriptions for SD_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	SD_OS_RX_PLL_LCK_LOST_IRQ_EN	SerDes IP Rx PLL lock lost Interrupt Enable Bit. 1: enable SerDes IP OS Rx PLL lock lost interrupt. 0: disable SerDes IP OS Rx PLL lock lost interrupt.	0x0	R/W
9	SD_RX_PLL_LCK_LOST_IRQ_EN	SerDes IP Rx PLL lock lost Interrupt Enable Bit. 1: enable SerDes IP Rx PLL lock lost interrupt. 0: disable SerDes IP Rx PLL lock lost interrupt.	0x0	R/W
8	SD_TX_PLL_LCK_LOST_IRQ_EN	SerDes IP Tx PLL lock lost Interrupt Enable Bit. 1: enable SerDes IP Tx PLL lock lost interrupt. 0: disable SerDes IP Tx PLL lock lost interrupt.	0x0	R/W
7	SD_AN_STAT_CHG_IRQ_EN	SerDes Autonegotiation Status Changed Interrupt Enable Bit. 1: enable SerDes autonegotiation status changed interrupt. 0: disable SerDes autonegotiation status changed interrupt.	0x0	R/W
6	SD_FC_FG_IRQ_EN	When set, this bit enables the frame checker interrupt.	0x0	R/W
5	SD_PAGE_RX_IRQ_EN	SerDes Autonegotiation Page Received Interrupt Enable Bit.	0x0	R/W

REGISTER SUMMARY

Table 134. Bit Descriptions for SD_IRQ_MASK (Continued)

Bits	Bit Name	Description	Reset	Access
		1: enable SerDes Autonegotiation Page Received interrupt. 0: disable SerDes Autonegotiation Page Received interrupt.		
4	SD_FIFO_OU_IRQ_EN	SerDes GMII/MII FIFO Overflow/Underflow Interrupt Enable Bit. 1: enable SerDes GMII/MII FIFO Overflow/Underflow interrupt. 0: disable SerDes GMII/MII FIFO Overflow/Underflow interrupt.	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R
1	SD_LINK_STAT_CHG_IRQ_EN	Enable SerDes link status change interrupt. 1: enable SerDes link status change interrupt. 0: disable SerDes link status change interrupt.	0x0	R/W
0	SD_MDIO_ERR_IRQ_EN	Enable SerDes MDIO framing error interrupt bit. 1: enable SerDes MDIO framing error interrupt. 0: disable SerDes MDIO framing error interrupt.	0x0	R/W

SerDes Subsystem Interrupt Status Register

Register Address: 0x0019, Reset: 0x0000, Name: SD_IRQ_STATUS

The interrupt status register is used to check which interrupts have triggered since the last time it was read. Each bit goes high when the associated interrupt triggers and then latches high until it is unlatched by reading (note that reading any of the bits in this register unlatches all of the bits in the register). The bits of SD_IRQ_STATUS go high even when the associated interrupts are not enabled. However, only bits associated with enabled interrupts are considered when generating the interrupt pending indication. Note: Default reset value of this register is dependent on the hardware configuration pins settings. This Clause 22 address is accessible only when either Fiber or Backplane mode is selected. For other SerDes modes, this register can be accessed through the equivalent Clause 45 address at 0xFC19.

Table 135. Bit Descriptions for SD_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	SD_OS_RX_PLL_LCK_LOST_IIRQ_LH	The OS Rx PLL Lock Lost interrupt status bit is set to 1 when the corresponding interrupt has been triggered since the last read. The bit remains latched high until cleared by reading the status register and is applicable only in 100BASE-FX operation.	0x0	R LH
9	SD_RX_PLL_LCK_LOST_IRQ_LH	The Rx PLL Lock Lost interrupt status bit is set to 1 when the associated interrupt has been triggered since the last read. The bit remains latched high until cleared by reading the status register. This is applicable for all modes except 100BASE-FX.	0x0	R LH
8	SD_TX_PLL_LCK_LOST_IRQ_IRQ_LH	The Tx PLL Lock Lost interrupt status bit is set to 1 when the associated inerrupt has been triggered since the last read. The bit remains latched high until cleared by reading the status register.	0x0	R LH
7	SD_AN_CHG_IRQ_LH	The SD autonegotiation status changed interrupt status bit is set to 1 when the associated interrupt has been triggered since the last read. The bit remains latched high until cleared by reading the status register.	0x0	R LH
6	SD_FC_FG_IRQ_LH	The SD frame checker/generator interrupt status bit is set to 1 when the associated interrupt has been triggered since the last read of SD_IRQ_STATUS. The bit remains latched high until cleared by reading the status register.	0x0	R LH
5	SD_PAGE_RX_IRQ_LH	The autonegotiation page received interrupt status bit is set to 1 when the associated interrupt has been triggered since the last read of SD_IRQ_STATUS. The bit remains latched high until cleared by reading the status register.	0x0	R LH
4	SD_FIFO_OU_IRQ_LH	The FIFO overflow/underflow interrupt status bit is set to 1 when the associated interrupt has been triggered since the last read of SD_IRQ_STATUS. The bit remains latched high until cleared by reading the status register.	0x0	R LH

REGISTER SUMMARY

Table 135. Bit Descriptions for SD_IRQ_STATUS (Continued)

Bits	Bit Name	Description	Reset	Access
[3:2]	RESERVED	Reserved.	0x0	R
1	SD_LINK_STAT_CHG_LH	If the link status changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading	0x0	R LH
0	SD_MDIO_ERR_LH	The SD MDIO framing error interrupt status bit is set to 1 when the associated interrupt has been triggered since the last read of SD_IRQ_STATUS. The bit remains latched high until cleared by reading the status register.	0x0	R LH

SerDes Subsystem Odd Nibble Suppression Control Registers

Register Address: 0xFC21, Reset: 0x0000, Name: SD_ONS_CTRL

The SerDes Subsystem Odd Nibble Suppression Control Register configures how the SerDes subsystem handles odd nibbles in data streams. By adjusting this register, users can enable or disable the suppression of odd nibbles, affecting data encoding, transmission, and error handling to optimize performance and data integrity. Detailed bit fields within the register offer specific control options to tailor the subsystem's behavior to the needs of the application.

Table 136. Bit Descriptions for SD_ONS_CTRL

Bits	Bit Name	Description	Reset	Access
[15:5]	RESERVED	Reserved.	0x0	R
[4:3]	ONS_TX_RA_CLK_SEL	Configures the clock enable shift setting when the ONS is bypassed. 11: SGMII to 100BASE-T 10: RGMII/RMII to 100BASE-FX 01: MII to 100BASE-FX 00: SGMII to 10BASE-T	0x0	R/W
2	ONS_PKT_SUP_DIS	Disables packet suppression. Odd nibbles are not suppressed in the payload of the frame when this bit is set.	0x0	R/W
1	ONS_BYPASS_OV_EN	Controls the override for ONS bypass. 1: ONS bypass override is enabled. 0: ONS bypass override is disabled.	0x0	R/W
0	ONS_BYPASS_EN	Enables the register to bypass odd nibble suppression. 1: Bypass ONS odd nibble suppression. 0: Do not bypass ONS (On-Chip Network Switch) odd nibble suppression.	0x0	R/W

SGMII Control Register 0

Register Address: 0xFC22, Reset: 0x0140, Name: SD_SGMII_CONTROL_0

The SGMII Control Register 0 configures the SGMII settings.

Table 137. Bit Descriptions for SD_SGMII_CONTROL_0

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	SD_SGMII_SPEED_SEL_LSB	Refer to SD_SGMII_SPEED_SEL_MSB (bit6)	0x0	R/W
12	SD_SGMII_AN_EN	The SD_SGMII_AN_EN bit controls the SGMII autonegotiation process. This bit is cleared, or autonegotiation is disabled, when both SD_SGMII_EN and SD_SGMII_MAC_EN are set to 1. In this scenario, speed and duplex mode are controlled through SD_SGMII_SPEED_SEL bits. The default value of this bit can be configured through hardware configuration pins. 1: enables autonegotiation 0: disables autonegotiation.	0x0	R/W
[11:9]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 137. Bit Descriptions for SD_SGMII_CONTROL_0 (Continued)

Bits	Bit Name	Description	Reset	Access
8	SD_SGMII_DPLX_MODE	The SD_SGMII_DPLX_MODE bit is used for manual configuration of the SGMII duplex mode. This bit is effective only when both SD_SGMII_EN and SD_SGMII_MAC_EN are set, and autonegotiation is disabled. 1: full duplex 0: half duplex.	0x1	R/W
7	RESERVED	Reserved.	0x0	R
6	SD_SGMII_SPEED_SEL_MSB	SD_SGMII_SPEED_SEL_MSB. The SD_SGMII_SPEED_SEL bitfields are used for manual configuration of the SGMII link speed. These settings take effect only when both SD_SGMII_EN and SD_SGMII_MAC_EN are set, and autonegotiation is disabled. 11: reserved. 10: 1000Mb/s 01:100 Mb/s 00: 10Mb/s	0x1	R/W
[5:0]	RESERVED	Reserved.	0x0	R

SGMII Control Register 1

Register Address: 0xFC23, Reset: 0x0000, Name: SD_SGMII_CONTROL_1

The SGMII Control Register 1 provides the ability to manually configure the SGMII link partner's advertised link status, speed, duplex mode, and Energy Efficient Ethernet (EEE) capabilities. The settings only take effect when both SD_SGMII_EN and SD_SGMII_MAC_EN are enabled.

Table 138. Bit Descriptions for SD_SGMII_CONTROL_1

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	SD_SGMII_EEEVAL	The SD_SGMII_EEEVAL bitfield allows the SGMII link partner's EEE (Energy Efficient Ethernet) advertised ability to be set when SD_SGMII_FRC_STAT_EN is enabled.	0x0	R/W
4	SD_SGMII_FRC_DUPLEX_VAL	The SD_SGMII_FRC_DUPLEX_VAL allows the SGMII link partner's advertised duplex ability to be set when SD_SGMII_FRC_STAT_EN is enabled.	0x0	R/W
[3:2]	SD_SGMII_FRC_SPEED_VAL	The SD_SGMII_FRC_SPEED_VAL bit allows manual setting of the SGMII link partner's advertised speed ability when enabled.	0x0	R/W
1	SD_SGMII_FRC_LINK_UP_VAL	The SD_SGMII_FRC_STAT_EN bit allows manual setting of the SGMII link partner's Link_up advertised ability.	0x0	R/W
0	SD_SGMII_FRC_STAT_EN	The SD_SGMII_FRC_STAT_EN bit forces the SGMII status of the Link Partner advertisement register when SGMII_MAC_EN is set to 1 and the system is in loopback mode.	0x0	R/W

SerDes Subsystem Rate Adaptation Control Register

Register Address: 0xFC24, Reset: 0x0000, Name: SD_RA_CNTRL

The SerDes Rate Adaptation Control register manages the rate adaptation settings for the SerDes interface, specifically focusing on the Low Power Idle (LPI) feature. It controls whether LPI can pass through the rate adaptation process, enabling optimization of power and performance.

Table 139. Bit Descriptions for SD_RA_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
[1:0]	SD_STP_LPI_OV	The SGMII RX Rate Adaptation LPI Override bitfield manages the Low Power Idle (LPI) feature for SGMII operations. Bit 0 controls LPI handling for SGMII to Copper (Cu) and SGMII Bridge PHY modes, while Bit 1 affects LPI handling for SGMII Bridge MAC mode. 0: Allow LPI to pass through Receive Rate Adaptation. 1: Stop LPI to pass through	0x0	R/W

REGISTER SUMMARY

SerDes Subsystem HBX Wrap Control Register 0

Register Address: 0xFC26, Reset: 0xA961, Name: SD_HBX_CNTRL_0

The HBX Control Register manages essential HBX interface functions, including Carrier Sense (CRS) signaling, clock phase adjustments, and Far-End Fault (FEF) settings. It allows for the configuration of CRS behavior, synchronization of clock phases, and control over fault detection and generation.

Table 140. Bit Descriptions for SD_HBX_CNTRL_0

Bits	Bit Name	Description	Reset	Access
[15:9]	HBX_FEF_ONES	The HBX_FEF_ONES bitfield sets the threshold for Far-End Fault (FEF) detection and generation based on consecutive ones per cycle. By default, this value conforms to IEEE Std 802.3, and changes should be made only for evaluation or debugging purposes. It is typically adjusted only when both FEF detection and generation are disabled.	0x54	R/W
8	HBX_FEF_GEN_EN	Enables or disables the generation of HBX Far-End Fault (FEF).	0x1	R/W
[7:5]	HBX_RX_CLK_PH	The HBX_RX_CLK_PH bitfield adjusts the phase of the HBX RX_CLK relative to the RX data output changes, similar to the HBX_TX_CLK phase control but applied to RX_CLK. For the SD subsystem, the only valid value for this bitfield is 0.	0x3	R/W
[4:2]	HBX_TX_CLK_PH	The HBX_TX_CLK_PH bitfield controls the phase of the TX_CLK rising edge relative to the TX data sampling cycle inside the PHY, measured in 125 MHz clock cycles. For the SD subsystem, this bitfield must be set to a value between 0 and 4, with values greater than 4 disabling TX_CLK. Only values 0 and 1 are valid for the SD subsystem.	0x0	R/W
1	HBX_TX_CRS_EN	The HBX_TX_CRS_EN bitfield controls whether the Carrier Sense (CRS) signal is active in full-duplex mode, in accordance with the simplified full-duplex operation and carrier sense deferral specified in Annex 4A of IEEE Std 802.3. When enabled, this bit ensures proper CRS signaling during full-duplex communication.	0x0	R/W
0	HBX_FD_CRS_EN	The HBX_FD_CRS_EN bitfield controls the assertion of the Carrier Sense (CRS) signal during transmission. When enabled, this bit ensures that the CRS signal is asserted whenever the transmit medium is non-idle, providing accurate carrier sense information to reflect active transmission conditions.	0x1	R/W

SerDes Subsystem HBX Wrap Control Register 1

Register Address: 0xFC27, Reset: 0x1907, Name: SD_HBX_CNTRL_1

The SERDES Subsystem HBX Wrap Control Register 1 is used to configure various parameters related to error detection and handling in the high-speed serial interface.

Table 141. Bit Descriptions for SD_HBX_CNTRL_1

Bits	Bit Name	Description	Reset	Access
[15:6]	HBX_NBAD_CAR_RST_TMR_N1MS	The HBX_NBAD_CAR_RST_TMR_N1MS bitfield sets the time window for monitoring the increment of bad carrier events. After the specified time window elapses, measured in milliseconds, the bad event counter is reinitialized.	0x64	R/W
5	HBX_FAR_END_FAULT_LH	The HBX_FAR_END_FAULT_LH bitfield indicates the presence of a Far-End Fault, as detected by the Far-End Fault Detection process. This signal is set when a Far-End Fault Indication is sensed and is self-cleared upon reading.	0x0	R LH
4	RESERVED	Reserved.	0x0	R
[3:1]	HBXF_FEF_CYCLES	The HBXF_FEF_CYCLES bitfield sets the number of cycles for Far-End Fault (FEF) detection. The default value conforms to IEEE Std 802.3 and should typically be adjusted only for evaluation or debugging purposes. Changes are expected only when FEF detection is disabled (MMR_FE_DET_EN set to 0).	0x3	R/W
0	HBX_FEF_DET_EN	HBX Far-End Fault (FEF) Detection Enable	0x1	R/W

REGISTER SUMMARY

SGMII Auto-Negotiation Timer Register

Register Address: 0xFC28, Reset: 0x0010, Name: SD_SGMII_AN_LNK_TMR_N_100US

Timer used for SGMII to ensure Auto-Negotiation protocol stability. The value is specified in units of 100µs.

Table 142. Bit Descriptions for SD_SGMII_AN_LNK_TMR_N_100US

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	SD_SGMII_AN_LNK_TMR_N100US	The SD_SGMII_AN_LNK_TMR_N100US bitfield sets the timer value in increments of 100 microseconds.	0x10	R/W

1000BASE-X Auto-Negotiation Timer Register

Register Address: 0xFC29, Reset: 0x0064, Name: SD_1000X_AN_LNK_TMR_N_100US

Timer used for 1000BASE-X to ensure Auto-Negotiation protocol stability. The value is specified in units of 100µs.

Table 143. Bit Descriptions for SD_1000X_AN_LNK_TMR_N_100US

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	SD_1000X_AN_LNK_TMR_N100US	The SD_1000X_AN_LNK_TMR_N100US bitfield sets the timer value in increments of 100 microseconds.	0x64	R/W

PCS 1000BASE-X Timer Register

Register Address: 0xFC2A, Reset: 0x0F0F, Name: SD_1000X_PCS_TMRS

The PCS 1000BASE-X Timer Register configures timing parameters essential for the operation of the 1000BASE-X Physical Coding Sublayer. It includes settings for the Auto-Negotiation Disable Timer and a Time-Out Function Timer for various PCS Auto-Negotiation states. The timer values are specified in units of 100 milliseconds, with a range from 100 milliseconds to 1.5 seconds, providing precise control over timing for effective Auto-Negotiation and state management.

Table 144. Bit Descriptions for SD_1000X_PCS_TMRS

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:8]	SD_AN_ST_TON100MS	SD_AN_ST_TON100MS. Configures the time-out duration for the PCS autonegotiation Finite State Machine (FSM) states, including ACK_DETECT, CMPL_ACK, IDLE_DETECT, and NEXT_PG_WAIT. The value is specified in units of 100 milliseconds, with a range from 100 milliseconds to 1.5 seconds. This bitfield sets the maximum time each state can remain active before a time-out occurs, ensuring proper management of the autonegotiation process.	0xF	R/W
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_AN_DIS_TMR_N100MS	SD_AN_DIS_TMR_N100MS. Configures the Auto-Negotiation disable timer. The value is specified in units of 100 milliseconds, with a range from 100 milliseconds to 1.5 seconds. This bitfield sets the duration for disabling autonegotiation, ensuring precise control over the timing for disabling the autonegotiation process.	0xF	R/W

Test Control Register for 1000BASE-X PMDs

Register Address: 0xFC2B, Reset: 0x0000, Name: SD_1000X_PCS_TEST_CTRL_1

Test Control Register for 1000BASE-X PMDs stated in 802.3 Annex 36A.

Table 145. Bit Descriptions for SD_1000X_PCS_TEST_CTRL_1

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 145. Bit Descriptions for SD_1000X_PCS_TEST_CTRL_1 (Continued)

Bits	Bit Name	Description	Reset	Access
[2:1]	SD_1000X_TEST_SEL	SD_1000X_TEST_SEL. Configures the test pattern selection for diagnostics and evaluation purposes. The bitfield settings are as follows: 11: 36A.3 Mixed frequency test pattern 10: 36A.2 Low-frequency test pattern 01: 36A.1 High-frequency test pattern 00: NONE	0x0	R/W
0	SD_1000X_PCS_TEST_EN	SD_1000X_PCS_TEST_EN. Enables or disables test pattern generation for the 1000BASE-X PCS. When this bitfield is set, test patterns configured via the SD_1000X_TEST_SEL bitfield are activated, allowing for diagnostics and evaluation of the PCS functionality.	0x0	R/W

1000BASE-X PCS Control Register

Register Address: 0xFC2C, Reset: 0x0000, Name: SD_1000X_PCS_CTRL

1000BASE-X PCS various input control settings

Table 146. Bit Descriptions for SD_1000X_PCS_CTRL

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	SD_1000X_PCS_CRS_DEF_SEL	SD_1000X_PCS_CRS_DEF_SEL. Determines the definition of the Carrier Sense (CRS) signal detection. The bitfield settings are as follows: 1: Receiving only definition 0: IEEE Standards definition	0x0	R/W
0	SD_1000X_PCS_LPI_EN	SD_1000X_PCS_LPI_EN. LPI mode for both TX and RX paths. The default setting is determined by strap pins and varies by mode: 1: LPI mode enabled for SGMII mode 0: LPI mode disabled for 100BASE-FX HD/FD, 1000BASE-SX/LX FD, or 1000BASE-KX mode	0x0	R/W

SerDes Subsystem Frame Checker Enable Register

Register Address: 0xFC2D, Reset: 0x0001, Name: SD_FC_EN

This register is used to enable the frame checker. The frame checker analyzes the received frames from either the MAC interface or the PHY (see the SD_FC_TX_SEL register, Address 0xFC30, Bit 0) to report the number of frames received, CRC errors, and various other frame errors. The frame checker frame and error counter registers count these events.

Table 147. Bit Descriptions for SD_FC_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	SD_FC_EN	When set, this bit enables the frame checker.	0x1	R/W

SerDes Subsystem Subsystem Frame Checker Interrupt Enable Register

Register Address: 0xFC2F, Reset: 0x0001, Name: SD_FC_IRQ_EN

This register is used to enable the frame checker interrupt. An interrupt is generated when a receive error occurs. Enable the frame checker/generator interrupt in the interrupt mask register. Set the SD_FC_FG_IRQ_EN bit (SD_IRQ_MASK register, Address 0xFC18). The interrupt status can be read via the FC_FG_IRQ_STAT bit (SD_FC_FG_IRQ_LH register, Address 0xFC19).

Table 148. Bit Descriptions for SD_FC_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	SD_FC_IRQ_EN	When set, this bit enables the frame checker interrupt.	0x1	R/W

REGISTER SUMMARY

SerDes Subsystem Frame Checker Transmit Select Register

Register Address: 0xFC30, Reset: 0x0000, Name: SD_FC_TX_SEL

When this register is set, it indicates that the frame checker should analyze frames received from the ASIC core before transmission at the Media Dependent Interface (MDI).

Table 149. Bit Descriptions for SD_FC_TX_SEL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	SD_FC_TX_SEL	When set, this bit indicates that the frame checker must check frames received to be transmitted by the PHY. 1: check frames from the MAC interface to be transmitted by the PHY. 0: check frames received by the PHY from the remote end.	0x0	R/W

SerDes Subsystem Frame Checker Max Frame Size Register

Register Address: 0xFC37, Reset: 0x05F2, Name: SD_FC_MAX_FRM_SIZE

This register specifies the maximum frame size. Frames longer than this size are counted as oversized frames.

Table 150. Bit Descriptions for SD_FC_MAX_FRM_SIZE

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_MAX_FRM_SIZE	This bit field specifies the max frame size. Received frames that are longer than this are counted as oversized frames. Note, this frame length excludes the preamble and start frame delimiter	0x5F2	R/W

SerDes Frame Checker Error Counter Register

Register Address: 0xFC3A, Reset: 0x0000, Name: SD_FC_ERR_CNT

This address allows the frame checker receive error counter to be observed.

Table 151. Bit Descriptions for SD_FC_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_ERR_CNT	This address allows the frame checker receive error counter to be observed.	0x0	R

SerDes Subsystem Frame Checker Count High Register

Register Address: 0xFC3B, Reset: 0x0000, Name: SD_FC_FRM_CNT_H

Provides access to bits 31:16 of a latched copy of the frame checker receives frame counter. This latched counter value is updated when the SD_FC_ERR_CNT register is read, allowing for observation of the number of CRC errors and corresponding frames. The receive frame counter tracks frames with the receiveOK status when SD_FC_RX_DATA_DECAP_EN is set to 1, or the total number of received frames when SD_FC_RX_DATA_DECAP_EN is set to 0.

Table 152. Bit Descriptions for SD_FC_FRM_CNT_H

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_FRM_CNT_H	Bits [31:16] of Latched Copy of the Number of Received Frames.	0x0	R

SerDes Subsystem Frame Checker Count Low Register

Register Address: 0xFC3C, Reset: 0x0000, Name: SD_FC_FRM_CNT_L

Provides access to bits 15:0 of a latched copy of the frame checker receives frame counter. This latched counter value is observed in conjunction with the SD_FC_FRM_CNT_H bitfield for a complete view of the receive frame count.

REGISTER SUMMARY

Table 153. Bit Descriptions for SD_FC_FRM_CNT_L

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_FRM_CNT_L	SD_FC_FRM_CNT_L. Bits [15:0] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Alignment Error Count Register

Register Address: 0xFC3D, Reset: 0x0000, Name: SD_FC_ALGN_ERR_CNT

Provides access to a latched copy of the frame checker alignment error counter. This counter is updated and latched when the SD_FC_ERR_CNT register is read. It counts the number of received frames that have the alignmentError status when SD_FC_RX_DATA_DECAP_EN is set to 1.

Table 154. Bit Descriptions for SD_FC_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_ALGN_ERR_CNT	Latched Copy of the Frame Alignment Error Counter.	0x0	R

Frame Checker Symbol Error Counter Register

Register Address: 0xFC3F, Reset: 0x0000, Name: SD_FC_SYMB_ERR_CNT

Provides access to a latched copy of the frame checker symbol error counter. This counter is latched when the SD_FC_ERR_CNT register is read. It counts the number of received frames where the RX_ER signal is asserted while RX_DV is also asserted. Note that when SD_FC_RX_DATA_DECAP_EN is set to 1, these frames are also included in the count recorded by SD_FC_ERR_CNT.

Table 155. Bit Descriptions for SD_FC_SYMB_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_SYM_ERR_CNT	Latched Copy of the Symbol Error Counter	0x0	R

SerDes Subsystem Frame Checker Length Error Count Register

Register Address: 0xFC40, Reset: 0x0000, Name: SD_FC_LEN_ERR_CNT

Provides access to a latched copy of the frame checker length error counter. This counter value is latched when the SD_FC_ERR_CNT register is read. It counts the number of received frames that have the length error status when SD_FC_RX_DATA_DECAP_EN is set to 1.

Table 156. Bit Descriptions for SD_FC_LEN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_LEN_ERR_CNT	Latched Copy of the Frame Length Error Counter	0x0	R

SerDes Subsystem Frame Checker Undersized Frame Count Register

Register Address: 0xFC41, Reset: 0x0000, Name: SD_FC_USZ_CNT

This register is a latched copy of the undersized frame error counter register. This register is a count of received frames with a length less than 64 bytes. When the receive error counter (SD_FC_ERR_CNT register, Address 0x0014) is read, the undersized frame error counter register is latched, which ensures that the undersized frame error count and receive frame count are synchronized.

Table 157. Bit Descriptions for SD_FC_USZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_USZ_CNT	Latched Copy of the Undersized Frame Error Counter.	0x0	R

SerDes Subsystem Frame Checker Oversized Frame Count Register.SdFcOszCnt

Register Address: 0xFC42, Reset: 0x0000, Name: SD_FC_OSZ_CNT

This register is a latched copy of the oversized frame error counter register. This register is a count of received frames with a length greater than specified in frame checker maximum frame size (SD_FC_MAX_FRM_SIZE register, Address 0xFC37). When the receive error counter

REGISTER SUMMARY

(SD_FC_ERR_CNT register) is read, the oversized frame error counter register is latched, which ensures that the oversized frame error count and receive frame count are synchronized.

Table 158. Bit Descriptions for SD_FC_OSZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_OSZ_CNT	Latched Copy of the Oversized Frame Error Counter	0x0	R

SerDes Subsystem Frame Checker Odd Preamble Packet Count Register

Register Address: 0xFC43, Reset: 0x0000, Name: SD_FC_PRE_ODD_CNT

This address allows a latched copy of the frame checker odd preamble frame counter to be observed. This copy of the counter is latched when SD_FC_ERR_CNT is read. The odd preamble frame counter counts the number of frames with an odd number of nibbles in the preamble and is applicable only to some technologies.

Table 159. Bit Descriptions for SD_FC_PRE_ODD_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_PRE_ODD_CNT	SD_FC_PRE_ODD_CNT. Latched Copy of the Odd Preamble Frame Counter	0x0	R

SerDes Subsystem Frame Checker Dribble Bits Frame Count Register

Register Address: 0xFC45, Reset: 0x0000, Name: SD_FC_DRIBBLE_BITS_CNT

This address allows a latched copy of the frame checker dribble bits frame counter to be observed. This copy of the counter is latched when SD_FC_ERR_CNT is read. The dribble bits frame counter counts the number of frames with dribble bits at the end of the frame and is applicable only to some technologies.

Table 160. Bit Descriptions for SD_FC_DRIBBLE_BITS_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_DRBBL_CNT	Latched Copy of the Dribble Bits Frame Counter.	0x0	R

SerDes Subsystem Frame Checker False Carrier Count Register

Register Address: 0xFC46, Reset: 0x0000, Name: SD_FC_FALSE_CARRIER_CNT

This address allows a latched copy of the frame checker false carrier event counter to be observed. This copy of the counter is latched when SD_FC_ERR_CNT is read. The false carrier event counter counts the number of times the BAD SSD state of the relevant PCS receive sequencer is entered and is applicable only to some technologies.

Table 161. Bit Descriptions for SD_FC_FALSE_CARRIER_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FC_FALSE_CARRIER_CNT	Latched Copy of the False Carrier Events Counter.	0x0	R

SerDes Subsystem Frame Generator Enable Register

Register Address: 0xFC4D, Reset: 0x0000, Name: SD_FG_EN

This register is used to enable the frame generator. When the frame generator is enabled, the source of data for the SerDes PHY comes from the frame generator and not the MAC interface.

Table 162. Bit Descriptions for SD_FG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	SD_FG_EN	When set, this bit enables the built-in frame generator.	0x0	R/W

REGISTER SUMMARY

SerDes Subsystem Frame Generator Control and Restart Register

Register Address: 0xFC4E, Reset: 0x0001, Name: SD_FG_CNTRL_RSTRT

This register provides frame generator control and restart functions.

Table 163. Bit Descriptions for SD_FG_CNTRL_RSTRT

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	SD_FG_RSTRT	When set, this bit restarts the frame generator. This bit is self-clearing	0x0	R/W SC
[2:0]	SD_FG_CNTRL	This register controls the frame generator in accordance with the following encoding: 111: Reserved 110: Reserved 101: Generate frames with payload of decrementing bytes 100: Generate frames with payload of 0x55 repeated 011: Generate frames with payload of 0xFF repeated 010: Generate frames with payload of 0x00 repeated 001: Generate frames with random payload 000: Generate no frames after completion of any current frame	0x1	R/W

SerDes Subsystem Frame Generator Continuous Mode Enable Register

Register Address: 0xFC4F, Reset: 0x0000, Name: SD_FG_CONT_MODE_EN

This register is used to put the frame generator into continuous mode. The default mode of operation is burst mode, where the number of frames generated is specified by the SD_FG_NFRM_H register and SD_FG_NFRM_L register.

Table 164. Bit Descriptions for SD_FG_CONT_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	SD_FG_CONT_MODE_EN	SD_FG_CONT_MODE_EN. This bit is used to put the frame generator into continuous mode or burst mode. 1: frame generator operates in continuous mode. In this mode, the frame generator keeps generating frames indefinitely. 0: frame generator operates in burst mode. In this mode, the frame generator generates a single burst of frames and then stops. The number of frames in the burst is determined by the SD_FG_NFRM_H register and SD_FG_NFRM_L register	0x0	R/W

SerDes Subsystem Frame Generator Interrupt Enable Register

Register Address: 0xFC50, Reset: 0x0000, Name: SD_FG_IRQ_EN

This register is used to enable the frame generator interrupt. An interrupt is generated when the requested number of frames has been generated. Enable the frame checker/generator interrupt in the IRQ_MASK register. Set the SD_FC_FG_IRQ_EN bit. The interrupt status can be read via the IRQ_STATUS register, SD_FC_FG_IRQ_STAT bit.

Table 165. Bit Descriptions for SD_FG_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	SD_FG_IRQ_EN	SD_FG_IRQ_EN. When set, this bit indicates that the frame generator must generate an interrupt when it has transmitted the programmed number of frames. 1: enable the frame generator interrupt. 0: disable the frame generator interrupt.	0x0	R/W

SerDes Subsystem Frame Generator Frame Length Register

Register Address: 0xFC52, Reset: 0x006B, Name: SD_FG_FRM_LEN

REGISTER SUMMARY

This register specifies the MAC client data field frame length in bytes. In addition to the data field, 6 bytes are added for the source address, 6 bytes for the destination address, 2 bytes for the length field, and 4 bytes for the frame check sequence (FCS). The total frame length is the data field length plus 18.

Table 166. Bit Descriptions for SD_FG_FRM_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FG_FRM_LEN	The Data Field Frame Length in Bytes.	0x6B	R/W

SerDes Subsystem Frame Generator Number of Frames High Register

Register Address: 0xFC54, Reset: 0x0000, Name: SD_FG_NFRM_H

This register is Bits [31:16] of a 32-bit register that specifics the number of frames to be generated each time the frame generator is enabled or restarted.

Table 167. Bit Descriptions for SD_FG_NFRM_H

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FG_NFRM_H	SD_FG_NFRM_H. Bits [31:16] of the Number of Frames to be Generated.	0x0	R/W

SerDes Subsystem Frame Generator Number of Frames Low Register

Register Address: 0xFC55, Reset: 0x0100, Name: SD_FG_NFRM_L

This register is Bits [15:0] of a 32-bit register that specifics the number of frames to be generated each time the frame generator is enabled or restarted

Table 168. Bit Descriptions for SD_FG_NFRM_L

Bits	Bit Name	Description	Reset	Access
[15:0]	SD_FG_NFRM_L	Bits [15:0] of the Number of Frames to be Generated.	0x100	R/W

SerDes Subsystem Frame Generator Done Register

Register Address: 0xFC56, Reset: 0x0000, Name: SD_FG_DONE

This register is used to indicate that the frame generator has completed the generation of the number of frames requested in the SD_FG_NFRM_H register and SD_FG_NFRM_L register.

Table 169. Bit Descriptions for SD_FG_DONE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	SD_FG_DONE	This bit reads as 1 to indicate that the generation of frames has completed. When set, this bit goes high, and it latches high until it is unlatched by reading.	0x0	R LH

SerDes Subsystem TX FIFO Control Register

Register Address: 0xFC78, Reset: 0x0000, Name: SDTXEBUFCTRL

TX FIFO Control Register for Serdes Subsystem.

Table 170. Bit Descriptions for SDTXEBUFCTRL

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	SD_TX_EBUF_RST	SD_TX_EBUF_RST. TX FIFO software reset bit.	0x0	R/W
0	SD_TX_EBUF_SYNC_EN	When set, the transmit FIFO is configured for synchronous operation to minimize latency	0x0	R/W

REGISTER SUMMARY

SerDes Subsystem FIFO Latency Threshold Register

Register Address: 0xFC79, Reset: 0x0550, Name: SD_TX_E_BUF_TH_1G

Enable Synchronous FIFO operation to minimize latency.

Table 171. Bit Descriptions for SD_TX_E_BUF_TH_1G

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:8]	SD_TX_EBUF_WR_OV_TH_1G	SerDes Subsystem TX buffer write overflow threshold. For a symmetric buffer it should be set to 2 x SD_TX_EBUF_WR_TH_1G + 5	0x5	R/W
[7:4]	SD_TX_EBUF_WR_TH_1G	SerDes Subsystem TX buffer write threshold. For a symmetric buffer it should be set to SD_TX_EBUF_RD_TH_1G + 5	0x5	R/W
[3:0]	SD_TX_EBUF_RD_TH_1G	SD_TX_EBUF_RD_TH_1G. SerDes Subsystem TX buffer read threshold. The settings, assuming the write thresholds are set for a symmetric elastic buffer configuration, are as follows: 0101: +/- 48 bits 0100: +/- 40 bits 0011: +/- 32 bits 0010: +/- 24 bits 0001: +/- 16 bits 0000: +/- 8 bits	0x0	R/W

SerDes Subsystem FIFO Latency Threshold Register

Register Address: 0xFC7A, Reset: 0x0761, Name: SD_TX_E_BUF_TH_MII

Enable Synchronous FIFO operation to minimize latency.

Table 172. Bit Descriptions for SD_TX_E_BUF_TH_MII

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:8]	SD_TX_EBUF_WR_OV_TH_MII	SerDes Subsystem TX buffer write overflow threshold. For a symmetric buffer it should be set to 2xSdTxEbufRdThMii + 5	0x7	R/W
[7:4]	SD_TX_EBUF_WR_TH_MII	SerDes Subsystem TX buffer write threshold. For a symmetric buffer it should be set to SD_TX_EBUF_RD_TH_MII + 5	0x6	R/W
[3:0]	SD_TX_EBUF_RD_TH_MII	SerDes Subsystem TX buffer read threshold. The settings, assuming the write thresholds are set for a symmetric elastic buffer configuration, are as follows: 0101: +/- 24 bits 0100: +/- 20 bits 0011: +/- 16 bits 0010: +/- 12 bits 0001: +/- 8 bits 0000: +/- 4 bits	0x1	R/W

SerDes Subsystem WBX Wrap Control Register 2

Register Address: 0xFC80, Reset: 0x1A46, Name: SD_HB_X_CNTRL_2

SD HBX wrap control registers 2.

Table 173. Bit Descriptions for SD_HB_X_CNTRL_2

Bits	Bit Name	Description	Reset	Access
15	HBX_MAX_CAR_DUR_DIS	Disable HBX_MAX_CAR_DUR	0x0	R/W
[14:4]	HBX_MAX_CAR_DUR	The maximum possible carrier duration for 100BASE-FX	0x1A4	R/W
[3:0]	HBX_NUM_IDLES_SIG_DET	100BASE-FX Number of IDLEs to be received before asserting 'signal detection' indication	0x6	R/W

REGISTER SUMMARY

SerDes Subsystem WBX Wrap Control Register 3

Register Address: 0xFC81, Reset: 0x0032, Name: SD_HB_X_CNTRL_3

SD HBX wrap control registers 3.

Table 174. Bit Descriptions for SD_HB_X_CNTRL_3

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
8	HBX_MAX_BAD_CAR_SIGDET_DIS	Disable HBX_MAX_BAD_CAR_SIGDET	0x0	R/W
[7:0]	HBX_MAX_BAD_CAR_SIGDET	Number of bad carrier events that needs to be detected before moving to 'Loss of Signal (Reset)' state to re-start the 'signal detection' operation.	0x32	R/W

SerDes Subsystem Start of Packet Control Register

Register Address: 0xFC88, Reset: 0x0CE7, Name: SD_SOP_CTRL

This register controls the start of packet (SOP) detection.

Table 175. Bit Descriptions for SD_SOP_CTRL

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:10]	SD_SOP_N8CYCM_1	When the SD_SOP_NCYC_EN bit is set, the SD_SOP_N_8_CYCM_1 bit field specifies the number of cycles of the MII RX_CLK clock that the transmit and receive SOP indications remain asserted. Add 1 to the value specified and then multiply by 8 to get the number of cycles. Note that the SOP indications are always deasserted at the end of the frame.	0x3	R/W
9	SD_SOP_NCYC_EN	When this bit is set, the duration of the transmit and receive SOP indications are defined by the SD_SOP_N_8_CYCM_1 bit field. Otherwise, the SOP indications are set for the duration of the frame	0x0	R/W
[8:5]	SD_SOP_LEN_MAX	When the SD_SOP_LEN_CHK_EN register is set, this register specifies the maximum length of the preamble in bytes for SFD/SMD detection.	0x7	R/W
4	SD_SOP_LEN_CHK_EN	When this register is set, and SD_SMD_EN or SD_SFD_EN are also set, the maximum preamble length of the packet, defined by SD_SOP_LEN_MAX, is checked, and if no SFD/SMD is detected within SD_SOP_LEN_MAX + 1 bytes, the packet is ignored so that the Start Of Packet signals are not set.	0x0	R/W
3	SD_SMD_EN	Enable SOP signal indication on SMD reception.	0x0	R/W
2	SD_SFD_EN	Enable RX SOP signal indication on SFD reception.	0x1	R/W
1	SD_TX_SOP_DET_EN	SD_TX_SOP_DET_EN. When set, this bit enables the generation of SOP detection for transmitted frames.	0x1	R/W
0	SD_RX_SOP_DET_EN	SD_RX_SOP_DET_EN. When set, this bit enables the generation of SOP detection for received frames	0x1	R/W

SerDes Subsystem Start of Packet Receive Detection Delay Register

Register Address: 0xFC89, Reset: 0x0000, Name: SD_SOP_RX_DEL

This register controls the receive side SOP detection delay in SerDes Subsystem.

Table 176. Bit Descriptions for SD_SOP_RX_DEL

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
[10:6]	SOP_RX_100DEL_NCYC	SOP_RX_100DEL_NCYC. This bit field specifies the number of cycles of the MII RX_CLK clock to delay the received frames SOP indication for 100BASE-FX links.	0x0	R/W
[5:0]	SOP_RX_1000DEL_NCYC	SOP_RX_1000DEL_NCYC. This register field specifies the number of cycles of the receive clock (for example, 8ns cycles) to delay the received frames SOP indication for 1000BASE-X links.	0x0	R/W

REGISTER SUMMARY

SerDes Subsystem Start of Packet Transmit Detection Delay Register

Register Address: 0xFC8A, Reset: 0x0000, Name: SD_SOP_TX_DEL

This register controls the transmit side SOP detection delay for SerDes Subsystem.

Table 177. Bit Descriptions for SD_SOP_TX_DEL

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:4]	SOP_TX_100DEL_8NS	SOP_TX_100DEL_8NS. This bit field specifies the number of 8ns periods to delay the transmitted frames SOP indication for 100BASE-FX links.	0x0	R/W
[3:0]	SOP_TX_1000DEL_8NS	This bit field specifies the number of 8ns periods to delay the transmitted frames SOP indication for 1000BASE-X links.	0x0	R/W

Fiber LED Pattern 0 Register

Register Address: 0xFC9B, Reset: 0x0055, Name: SD_FIB_LED_PAT_0

This register allows the LED pattern for Fiber LED_0 to be read or written. The default value is 0x55, representing an alternating 0/1-bit pattern. The LED blinks with a default cycle of 0.2 seconds on and 0.2 seconds off. This register provides configurable control over the LED pattern, enabling customization of the blink sequence as required.

Table 178. Bit Descriptions for SD_FIB_LED_PAT_0

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	SD_FIB_LED_PAT_0	The internal LED pattern for LED_0 can be read or written via this field.	0x55	R/W

FIBER LED Pattern Tick Duration Register 0

Register Address: 0xFC9C, Reset: 0x0018, Name: SD_FIBER_LED_PAT_TICK_DUR_0

This register controls the bit duration for the blink pattern of Fiber LED_0. Each bit in the blink pattern field (SD_FIB_LED_PAT_0) is driven to the corresponding LED pin and held for a duration determined by this register. The duration in milliseconds is calculated as the register value plus 1, multiplied by 8 (e.g., 8 ms, 16 ms, up to 504 ms). A register value of 63 signifies a special case where the bit duration is 1ms. Refer to the FIBERLED_PAT_PAUSE_DUR_0 register for additional configurations. The default LED blink pattern is 0.2 seconds on and 0.2 seconds off.

Table 179. Bit Descriptions for SD_FIBER_LED_PAT_TICK_DUR_0

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	SD_FIB_LED_PAT_TICK_DUR_0	The tick duration for Fiber LED_0 can be written to this field, with the value determining the duration as (register value + 1) × 8ms.	0x18	R/W

Fiber LED Pattern Pause Duration Register 0

Register Address: 0xFC9D, Reset: 0x0000, Name: SD_FIB_LED_PAT_PAUSE_DUR_0

This register specifies the pause duration for Fiber LED_0 after the blink pattern is driven to the LED_0 pin. The last bit is held for a duration calculated as the LED tick duration (defined in the SD_Fiber_LED_PAT_TICK_DUR_0 register) multiplied by the value in this register. The default blink pattern is 0.2 seconds on and 0.2 seconds off.

Table 180. Bit Descriptions for SD_FIB_LED_PAT_PAUSE_DUR_0

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_FIB_LED_PAT_PAUSE_DUR_0	The pause duration for Fiber LED_0 can be written to this field, with the value determining the duration as (register value + 1) × 8ms.	0x0	R/W

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FIBER LED Pattern 1 Register

Register Address: 0xFC9E, Reset: 0x0055, Name: SD_FIB_LED_PAT_1

This register allows the LED pattern for Fiber LED_1 to be read or written. The default value is 0x55, representing an alternating 0/1-bit pattern. The LED blinks with a default cycle of 0.2 seconds on and 0.2 seconds off. This register provides configurable control over the LED pattern, enabling customization of the blink sequence as required.

Table 181. Bit Descriptions for SD_FIB_LED_PAT_1

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	SD_FIB_LED_PAT_1	SD_FIB_LED_PAT_1. The internal LED pattern for LED_1 can be read or written via this field.	0x55	R/W

FIBER Pattern Tick Duration Register 1

Register Address: 0xFC9F, Reset: 0x0018, Name: SD_FIBER_LED_PAT_TICK_DUR_1

This register controls the bit duration for the blink pattern of Fiber LED_1. Each bit in the blink pattern field (FIBERLED_PAT) is driven to the corresponding LED pin and held for a duration determined by this register. The duration in milliseconds is calculated as the register value plus 1, multiplied by 8 (e.g., 8 ms, 16 ms, up to 504 ms). A register value of 63 signifies a special case where the bit duration is 1ms. Refer to the FIBERLED_PAT_PAUSE_DUR_1 register for additional configurations. The default LED blink pattern is 0.2 seconds on and 0.2 seconds off.

Table 182. Bit Descriptions for SD_FIBER_LED_PAT_TICK_DUR_1

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	SD_FIB_LED_PAT_TICK_DUR_1	LED pattern bit duration for Fiber LED_1. Each bit in the blink pattern bit field (FIBERLED_PAT) is driven to the corresponding LED pin and held for the duration specified in this register. The duration in milliseconds is the value of this register plus 1 multiplied by 8, for example, 8ms, 16ms, … 504ms. The value 63 has a special meaning of 1ms tick duration. Also see the FIBERLED_PAT_PAUSE_DUR_0 register. The default blink is a 0.2 sec on and 0.2 sec off pattern.	0x18	R/W

FIBER LED Patter Pause Duration Register 1

Register Address: 0xFCA0, Reset: 0x0000, Name: SD_FIB_LED_PAT_PAUSE_DUR_1

This register specifies the pause duration for Fiber LED_1 after the blink pattern is driven to the LED_1 pin. The last bit is held for a duration calculated as the LED tick duration (defined in the SD_Fiber_LED_PAT_TICK_DUR_1 register) multiplied by the value in this register. The default blink pattern is 0.2 seconds on and 0.2 seconds off.

Table 183. Bit Descriptions for SD_FIB_LED_PAT_PAUSE_DUR_1

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_FIB_LED_PAT_PAUSE_DUR_1	The pause duration for Fiber LED_0 can be written to this field, with the value determining the duration as (register value + 1) × 8ms.	0x0	R/W

Fiber LED Pattern 2 Register

Register Address: 0xFCA1, Reset: 0x0055, Name: SD_FIB_LED_PAT_2

This register allows the LED pattern for Fiber LED_2 to be read or written. The default value is 0x55, representing an alternating 0/1-bit pattern. The LED blinks with a default cycle of 0.2 seconds on and 0.2 seconds off. This register provides configurable control over the LED pattern, enabling customization of the blink sequence as required.

Table 184. Bit Descriptions for SD_FIB_LED_PAT_2

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 184. Bit Descriptions for SD_FIB_LED_PAT_2 (Continued)

Bits	Bit Name	Description	Reset	Access
[7:0]	SD_FIB_LED_PAT_2	SD_FIB_LED_PAT_2. The internal LED pattern for LED_2 can be read or written via this field.	0x55	R/W

Fiber LED Pattern Tick Duration Register 2

Register Address: 0xFCA2, Reset: 0x0018, Name: SD_FIBER_LED_PAT_TICK_DUR_2

This register controls the bit duration for the blink pattern of Fiber LED_2. Each bit in the blink pattern field (FIBERLED_PAT) is driven to the corresponding LED pin and held for a duration determined by this register. The duration in milliseconds is calculated as the register value plus 1, multiplied by 8 (e.g., 8ms, 16ms, up to 504ms). A register value of 63 signifies a special case where the bit duration is 1ms. Refer to the FIBERLED_PAT_PAUSE_DUR_2 register for additional configurations. The default LED blink pattern is 0.2 seconds on and 0.2 seconds off.

Table 185. Bit Descriptions for SD_FIBER_LED_PAT_TICK_DUR_2

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	SD_FIB_LED_PAT_TICK_DUR_2	SD_FIB_LED_PAT_TICK_DUR_2. LED pattern bit duration for Fiber LED_2. Each bit in the blink pattern bit field (FIBERLED_PAT) is driven to the corresponding LED pin and held for the duration specified in this register. The duration in milliseconds is the value of this register plus 1 multiplied by 8, for example, 8ms, 16ms, … 504ms. The value 63 has a special meaning of 1 ms tick duration. Also see the FIBERLED_PAT_PAUSE_DUR_0 register. The default blink is a 0.2 sec on and 0.2 sec off pattern.	0x18	R/W

Fiber LED Pattern Pause Duration Register 2

Register Address: 0xFCA3, Reset: 0x0000, Name: SD_FIB_LED_PAT_PAUSE_DUR_2

This register specifies the pause duration for Fiber LED_2 after the blink pattern is driven to the LED_2 pin. The last bit is held for a duration calculated as the LED tick duration (defined in the SD_Fiber_LED_PAT_TICK_DUR_2 register) multiplied by the value in this register. The default blink pattern is 0.2 seconds on and 0.2 seconds off.

Table 186. Bit Descriptions for SD_FIB_LED_PAT_PAUSE_DUR_2

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_FIB_LED_PAT_PAUSE_DUR_2	The pause duration for Fiber LED_2 can be written to this field, with the value determining the duration as (register value + 1) × 8ms.	0x0	R/W

Fiber LED Pattern 3 Register

Register Address: 0xFCA4, Reset: 0x0055, Name: SD_FIB_LED_PAT_3

This register allows the LED pattern for Fiber LED_3 to be read or written. The default value is 0x55, representing an alternating 0/1-bit pattern. The LED blinks with a default cycle of 0.2 seconds on and 0.2 seconds off. This register provides configurable control over the LED pattern, enabling customization of the blink sequence as required.

Table 187. Bit Descriptions for SD_FIB_LED_PAT_3

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	SD_FIB_LED_PAT_3	SD_FIB_LED_PAT_3. The internal LED pattern for LED_3 can be read or written via this field.	0x55	R/W

Fiber LED Pattern Pause Duration Register 3

Register Address: 0xFCA5, Reset: 0x0018, Name: SD_FIBER_LED_PAT_TICK_DUR_3

This register controls the bit duration for the blink pattern of Fiber LED_3. Each bit in the blink pattern field (FIBERLED_PAT) is driven to the corresponding LED pin and held for a duration determined by this register. The duration in milliseconds is calculated as the register value plus

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1, multiplied by 8 (e.g., 8ms, 16ms, up to 504ms). A register value of 63 signifies a special case where the bit duration is 1ms. Refer to the FIBERLED_PAT_PAUSE_DUR_3 register for additional configurations. The default LED blink pattern is 0.2 seconds on and 0.2 seconds off.

Table 188. Bit Descriptions for SD_FIBER_LED_PAT_TICK_DUR_3

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	SD_FIB_LED_PAT_TICK_DUR_3	SD_FIB_LED_PAT_TICK_DUR_3. LED pattern bit duration for Fiber LED_3. Each bit in the blink pattern bit field (FIBERLED_PAT) is driven to the corresponding LED pin and held for the duration specified in this register. The duration in milliseconds is the value of this register plus 1 multiplied by 8, for example, 8ms, 16ms, … 504ms. The value 63 has a special meaning of 1 ms tick duration. Also see the FIBERLED_PAT_PAUSE_DUR_0 register. The default blink is a 0.2 sec on and 0.2 sec off pattern.	0x18	R/W

Fiber Pattern Tick Duration Register 3

Register Address: 0xFCA6, Reset: 0x0000, Name: SD_FIB_LED_PAT_PAUSE_DUR_3

This register specifies the pause duration for Fiber LED_3 after the blink pattern is driven to the LED_3 pin. The last bit is held for a duration calculated as the LED tick duration (defined in the SD_Fiber_LED_PAT_TICK_DUR_3 register) multiplied by the value in this register. The default blink pattern is 0.2 seconds on and 0.2 seconds off.

Table 189. Bit Descriptions for SD_FIB_LED_PAT_PAUSE_DUR_3

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_FIB_LED_PAT_PAUSE_DUR_3	The pause duration for Fiber LED_3 can be written to this field, with the value determining the duration as (register value + 1) × 8ms.	0x0	R/W

Fiber LED Pulse Stretching Register

Register Address: 0xFCA7, Reset: 0x0001, Name: SD_FIB_LED_PUL_STR_EN

The SerDes Subsystem Fiber LED Pulse Stretching Register enables pulse stretching for transmit, receive, or activity events, ensuring that short-duration events are extended for better visibility. When this bit is set, the LED logic stretches the pulses, preventing them from being too brief to light the LED.

Table 190. Bit Descriptions for SD_FIB_LED_PUL_STR_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	SD_FIB_LED_PUL_STR_EN	SD_FIB_LED_PUL_STR_EN. Setting this bit enables pulse stretching for transmit, receive, or activity events to ensure short-duration events are visible.	0x1	R/W

Fiber LED Pulse Stretching Duration Register

Register Address: 0xFCA8, Reset: 0x0000, Name: SD_FIB_LED_PUL_STR_DUR_SEL

This register selects the pulse stretching duration.

Table 191. Bit Descriptions for SD_FIB_LED_PUL_STR_DUR_SEL

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
[1:0]	SD_FIB_LED_PUL_STR_DUR_SEL	This bit field selects the duration of the pulse stretching. 11: user programmable. In this case, the duration of the pulse stretching is programmable by the SD_FIB_LED_PUL_STR_DUR register (Address 0xFCA9, Bits [5:0]). 10: 102ms. 01: 64ms.	0x0	R/W

REGISTER SUMMARY

Table 191. Bit Descriptions for SD_FIB_LED_PUL_STR_DUR_SEL (Continued)

Bits	Bit Name	Description	Reset	Access
		00: 32ms.		

Fiber LED Pulse Stretching Duration Register

Register Address: 0xFCA9, Reset: 0x0011, Name: SD_FIB_LED_PUL_STR_DUR

This register sets the LED pulse stretch duration for Fiber LEDs in user-programmable mode.

Table 192. Bit Descriptions for SD_FIB_LED_PUL_STR_DUR

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	SD_FIB_LED_PUL_STR_DUR	This bit field sets the LED pulse stretch duration for Fiber LEDs when the user-programmable mode is selected. The duration is calculated as the value of this register multiplied by 8ms, with a default value corresponding to 136ms.	0x11	R/W

Fiber LED_0 Configuration Register

Register Address: 0xFCAA, Reset: 0x0008, Name: SD_FIB_LED_CFG_0

This register provides access to various Fiber LED_0 control register bits.

Table 193. Bit Descriptions for SD_FIB_LED_CFG_0

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_FIB_LED_CFG_0	SD_FIB_LED_CFG_0. The Fiber LED_0 function is selected via this register. The default Fiber LED_0 function is Link / Blink on Activity. 11xx: Reserved 1011: OFF 1010: ON 1001: Blink 1000: Link / Blink on Activity 0111: Link / Blink on Receiving 0110: Link / Blink on Transmitting 0101: Blink on Activity 0100: Blink on Receiving 0011: Blink on Transmitting 0010: Link Up 0001: On if 100BASE-FX link 0000: On if 1000BASE-X link	0x8	R/W

Fiber LED_1 Configuration Register

Register Address: 0xFCAB, Reset: 0x0000, Name: SD_FIB_LED_CFG_1

This register provides access to various Fiber LED_1 control register bits.

Table 194. Bit Descriptions for SD_FIB_LED_CFG_1

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_FIB_LED_CFG_1	SD_FIB_LED_CFG_1. The Fiber LED_1 function is selected via this register. The default Fiber LED_1 function is 1000BASE-X link. 11xx: Reserved 1011: OFF 1010: ON 1001: Blink 1000: Link / Blink on Activity	0x0	R/W

REGISTER SUMMARY

Table 194. Bit Descriptions for SD_FIB_LED_CFG_1 (Continued)

Bits	Bit Name	Description	Reset	Access
		0111: Link / Blink on Receiving 0110: Link / Blink on Transmitting 0101: Blink on Activity 0100: Blink on Receiving 0011: Blink on Transmitting 0010: Link Up 0001: On if 100BASE-FX link 0000: On if 1000BASE-X link		

Fiber LED_2 Configuration Register

Register Address: 0xFCAC, Reset: 0x0001, Name: SD_FIB_LED_CFG_2

This register provides access to various Fiber LED_2 control register bits.

Table 195. Bit Descriptions for SD_FIB_LED_CFG_2

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_FIB_LED_CFG_2	SD_FIB_LED_CFG_2. The Fiber LED_2 function is selected via this register. The default Fiber LED_2 function is 100BASE-FX link. 11xx: Reserved 1011: OFF 1010: ON 1001: Blink 1000: Link / Blink on Activity 0111: Link / Blink on Receiving 0110: Link / Blink on Transmitting 0101: Blink on Activity 0100: Blink on Receiving 0011: Blink on Transmitting 0010: Link Up 0001: On if 100BASE-FX link 0000: On if 1000BASE-X link	0x1	R/W

Fiber LED_3 Configuration Register

Register Address: 0xFCAD, Reset: 0x0002, Name: SD_FIB_LED_CFG_3

This register provides access to various Fiber LED_3 control register bits.

Table 196. Bit Descriptions for SD_FIB_LED_CFG_3

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	SD_FIB_LED_CFG_3	SD_FIB_LED_CFG_3. The Fiber LED_3 function is selected via this register. The default Fiber LED_3 function is Link Up. 11xx: Reserved 1011: OFF 1010: ON 1001: Blink 1000: Link / Blink on Activity 0111: Link / Blink on Receiving 0110: Link / Blink on Transmitting 0101: Blink on Activity 0100: Blink on Receiving 0011: Blink on Transmitting 0010: Link Up	0x2	R/W

REGISTER SUMMARY

Table 196. Bit Descriptions for SD_FIB_LED_CFG_3 (Continued)

Bits	Bit Name	Description	Reset	Access
		0001: On if 100BASE-FX link 0000: On if 1000BASE-X link		

SerDes Subsystem TX Differential Output Control Register

Register Address: 0xFCB6, Reset: 0x0001, Name: SD_TBI_LPBK_TX_INH

Control register to suppress data transmission on the TX differential lines.

Table 197. Bit Descriptions for RESERVEASYNCMM0

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVE	RESERVE	0x0	R/W
0	SD_ISOLATE_S_OUT	Control register to suppress the data on TX differential lines when SD_PCS_TBI_LPBK_EN = 1 and SD_LOOPBACK = 1.	0x1	R/W

SerDes Subsystem High Speed Internal Loopback Control Register

Register Address: 0xFCC9, Reset: 0x0000, Name: SD_HS_LPBK_CFG

Configuration settings for the SerDes IP to control high-speed internal loopback functionality.

Table 198. Bit Descriptions for SDPHYIPCFG9

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	HS_LPBK_EN	High-Speed Internal Loopback Enable. This bit activates serial near-end internal loopback.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Rotational Frequency Detector Configuration Register

Register Address: 0xFCD0, Reset: 0x0052, Name: SD_RFD_CFG

This register only applies to SGMII, 1000BASE-SX/LX, and 1000BASE-KX. RFD function does not apply to 100Base-FX.

Table 199. Bit Descriptions for SD_RFD_CFG

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x14	R/W
1	RFD_ENABLE	RFD_ENABLE. Active high control to allow rotational frequency detector to reset the lock detector. Note: This setting is applicable only for SGMII, 1000BASE-SX/LX/KX. RFD function is not used for 100BaseFX.	0x1	R/W
0	RESERVED	Reserved.	0x0	R

GE SUBSYSTEM REGISTER SUMMARY

The subsystem registers are accessible at Device Address 0x1E using Clause 45 access. For systems that do not support the interface specified under Clause 45, these registers can be accessed using Clause 22 access via Register 0x0010 and Register 0x0011.

The default value of some of the registers are determined by the value of the hardware configuration pins, which are read just after the RESET_N pin is deasserted (see the Hardware Configuration Pins section) so that the default operation of the ADIN1320 can be configured in unmanaged applications. The default values in the registers listed in Table 200 assume that the ADIN1320 is configured with autonegotiation enabled, all speeds advertised, and the ADIN1320 is not configured to enter software power-down after reset.

Table 200. MDIOMAP_GESUBSYS Register Summary

Register Address	Name	Description	Reset	Access
0xFF0C	GE_SFT_RST	GE Subsystem Software Reset Register.	0x0000	R/W
0xFF0D	GE_SFT_RST_CFG_EN	GE Subsystem Software Reset Enable Register.	0x0000	R/W

REGISTER SUMMARY

Table 200. MDIOMAP_GESUBSYS Register Summary (Continued)

Register Address	Name	Description	Reset	Access
0xFF1D	GE_IRQ_EN	GE Subsystem Interrupt Enable Register.	0x000E	R/W
0xFF1E	GE_IRQ_LAT	GE Subsystem Interrupt Status Register.	0x0010	R
0xFF1F	GE_CLK_CFG	GE Subsystem Clock Configuration Register.	0x0008	R/W
0xFF23	GE_RGMII_CFG	GE Subsystem RGMII Configuration Register.	0x7E04	R/W
0xFF24	GE_RMII_CFG	GE Subsystem RMII Configuration Register.	0x1116	R/W
0xFF26	GE_PHY_BASE_CFG	GE Subsystem Copper PHY Base Configuration Register.	0x0086	R/W
0xFF27	GE_PHY_IF_CFG	GE Subsystem Gigabit Ethernet PHY Configuration Register.	0x0000	R/W
0xFF29	GE_PHY_LED_CFG	GE Subsystem LED Active Low Status Register	0x0004	R/W
0xFF38	GE_B10_REGEN_PRE	GE Subsystem 10BASE-T Preamble Generation Register.	0x0000	R/W
0xFF3A	GE_RGMII_IO_CNTRL	GE Subsystem RGMII I/O Control Register.	0x0005	R/W
0xFF3B	GE_CLK_IO_CNTRL	GE Subsystem Clock I/O Control Register.	0x0002	R/W
0xFF3C	GE_LNK_STAT_INV_EN	GE Subsystem Link Status Invert Enable Register.	0x0000	R/W
0xFF3D	GE_IO_LINK_ST_OR_CNTRL	GE Subsystem Link Status Pin Override Control Register.	0x0000	R/W
0xFF3E	GE_IO_INT_N_OR_CNTRL	GE Subsystem INT_N Pin Override Control Register.	0x0000	R/W
0xFF3F	GE_IO_GTX_CLK_OR_CNTRL	GE Subsystem GTX_CLK Pin Override Control Register.	0x0000	R/W
0xFF40	GE_IO_LED_A_OR_CNTRL	GE Subsystem LED 0 Pin Override Control Register.	0x0000	R/W
0xFF41	GE_IO_LED_B_OR_CNTRL	GE Subsystem LED 1 Pin Override Control Register.	0x0000	R/W
0xFF42	GE_IO_LED_C_OR_CNTRL	GE Subsystem LED 2 Pin Override Control Register.	0x0000	R/W
0xFF53	GE_SD_CFG	SerDes Subsystem Advertisement Configuration Register.	0x0100	R/W
0xFF57	GE_MSEL_AUTO_STAT	GE Auto Media Select Status Register.	0x0000	R
0xFF78	GE_WOL_SYS_CNTRL	GE Subsystem Wake on Lan System Control Register.	0x0000	R/W
0xFF79	GE_WOL_EN	GE Subsystem Wake on Lan Enable Register.	0x0000	R/W
0xFF7A	GE_WOL_WAKE_CNTRL	GE Subsystem Wake on Lan Wake Control Register.	0x0001	R/W
0xFF7B	GE_WOL_SIG_CNTRL	GE Subsystem Wake on Lan Signal Control Register.	0x0100	R/W
0xFF7C	GE_WOL_STA_0_AD_01	GE Subsystem Wake on Lan Station 0 Address Register.	0x0000	R/W
0xFF7D	GE_WOL_STA_0_AD_23	GE Subsystem Wake on Lan Station 0 Address Register.	0x0000	R/W
0xFF7E	GE_WOL_STA_0_AD_45	GE Subsystem Wake on Lan Station 0 Address Register.	0x0000	R/W
0xFF80	GE_MGC_0_CNTRL	GE Subsystem Magic Packet Control Register.	0x0073	R/W
0xFF81	GE_MGC_0_KEY_01	GE Subsystem SecureOn Key Register.	0x0000	R/W
0xFF82	GE_MGC_0_KEY_23	GE Subsystem SecureOn Key Register.	0x0000	R/W
0xFF83	GE_MGC_0_KEY_45	GE Subsystem SecureOn Key Register.	0x0000	R/W
0xFF85	GE_WOL_STAT	GE Subsystem Wake on Lan Status Register.	0x0000	R

GE SUBSYSTEM REGISTER DETAILS

GE Subsystem Software Reset Register

Register Address: 0xFF0C, Reset: 0x0000, Name: GE_SFT_RST

The soft reset register is used to reset the subsystem.

Table 201. Bit Descriptions for GE_SFT_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GE_SFT_RST	The GE subsystem can be reset by setting GE_SFT_RST to 1. The subsystem behavior depends on the setting of the GE_SFT_RST_CFG_EN register. When the GE_SFT_RST_CFG_EN bit is set, the subsystem requests a new set of hardware configuration pin settings from the chip during the software reset sequence. When GE_SFT_RST_CFG_EN is clear, the previously stored hardware configuration pin settings are reloaded into the corresponding management registers.	0x0	R/W SC

REGISTER SUMMARY

GE Subsystem Software Reset Enable Register

Register Address: 0xFF0D, Reset: 0x0000, Name: GE_SFT_RST_CFG_EN

In the event of a software reset using the GE_SFT_RST bit, the subsystem behavior depends on the setting of this register bit.

Table 202. Bit Descriptions for GE_SFT_RST_CFG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GE_SFT_RST_CFG_EN	In the event of a subsystem software reset using the GE_SFT_RST bit, the subsystem behavior depends on the setting of the GE_SFT_RST_CFG_EN bit. 1: when the GE_SFT_RST_CFG_EN bit is set, the subsystem requests a new set of hardware configuration pin settings from the chip during the software reset sequence. 0: when GE_SFT_RST_CFG_EN is clear, the previously stored hardware configuration pin settings are reloaded into the corresponding management registers.	0x0	R/W

GE Subsystem Interrupt Enable Register

Register Address: 0xFF1D, Reset: 0x000E, Name: GE_IRQ_EN

This register is used to control whether or not the interrupt on INT_N hardware pin is asserted in response to various events.

Table 203. Bit Descriptions for GE_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R/W SC
7	GE_WOL_WAKE_IRQ_EN	This bit enables an interrupt in response to a Wake-on-LAN (WoL) wake event.	0x0	R/W
6	GE_MSEL_AUTO_CHNG_IRQ_EN	This bit enables an interrupt in response to an auto-media selection change	0x0	R/W
5	RESERVED	Reserved.	0x0	R/W
4	GE_HRD_RST_IRQ_EN	This bit enables an interrupt in response to a hardware reset. Note that this bit will be initialized to its pin dependent default value on reset. Therefore, the interrupt is only generated when the PHY is configured to enter software power-down on exit from reset either through hardware strapping or alternatively through software configuration (see Bit GE_PHY_SFT_PD_CFG in the GE_PHY_BASE_CFG register).	0x0	R/W
[3:0]	RESERVED	Reserved.	0xE	R/W

GE Subsystem Interrupt Status Register

Register Address: 0xFF1E, Reset: 0x0010, Name: GE_IRQ_LAT

This register is used to check and clear the interrupt on INT_N hardware pin after a hardware reset.

Table 204. Bit Descriptions for GE_IRQ_LAT

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R LH
7	GE_WOL_WAKE_IRQ_LH	This bit indicates that a WoL wake event occurred since the last time GE_IRQ_LAT was read.	0x0	R LH
6	GE_MSEL_AUTO_CHNG_IRQ_LH	This bit indicates that the auto-media selection has change since the last time GE_IRQ_LAT was read.	0x0	R LH
5	RESERVED	Reserved.	0x0	R LH
4	GE_HRD_RST_IRQ_LH	This bit indicates that a Hardware reset occurred since the last time GE_IRQ_LAT was read.	0x1	R LH
[3:0]	RESERVED	Reserved.	0x0	R LH

GE Subsystem Clock Configuration Register

Register Address: 0xFF1F, Reset: 0x0008, Name: GE_CLK_CFG

REGISTER SUMMARY

This register allows the subsystem output clock configuration to be controlled.

Table 205. Bit Descriptions for GE_CLK_CFG

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	SD_RX_CLK_125_EN	When this bit is set, the 125MHz SerDes RX recovered clock is driven at GP_CLK pin.	0x0	R/W
9	SD_TX_CLK_125_EN	When this bit is set, the 125MHz SerDes TX free running clock is driven at GP_CLK pin.	0x0	R/W
8	SD_RX_CLK_HRT_EN	The SerDes subsystem provides a digital recovered RX clock. This clock is sourced either from the reference clock or from the SerDes RX PLL recovered 125MHz clock depending on the mode that the PHY is in and on the settings of certain registers. Setting SD_RX_CLK_HRT_EN causes the GE sub-system to request the chip to drive the SerDes subsystem digital RX heartbeat clock at GP_CLK pin.	0x0	R/W
7	SD_TX_CLK_HRT_EN	The SerDes subsystem provides a digital TX heartbeat clock. This clock is sourced either from the reference clock or from the SerDes TX PLL free-running 125MHz clock depending on the mode and on the settings of certain registers. Setting SD_TX_CLK_HRT_EN causes the GE sub-system to request the chip to drive the SerDes subsystem digital TX heartbeat clock at the GP_CLK pin.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	GE_CLK_RCVR_125_EN	When this bit is set, the 125MHz GE PHY recovered clock (or PLL clock) is driven at the GP_CLK pin.	0x0	R/W
4	GE_CLK_FREE_125_EN	When this bit is set, the 125MHz GE PHY free running clock is driven at the GP_CLK pin.	0x0	R/W
3	GE_REF_CLK_EN	When this bit is set, the 25MHz reference clock from the crystal oscillator is driven at the CLK25_REF pin. Note that when an external 50MHz clock is driven at XTAL_I (for RMII), it is divided by 2, and the divided 25MHz reference clock is driven at the CLK25_REF pin.	0x1	R/W
2	GE_CLK_HRT_RCVR_EN	The GE PHY provides a digital recovered heartbeat clock. This clock is sourced from either the 25MHz reference clock or the 125MHz recovered clock depending on the mode that the PHY is in and on the settings of certain registers. Setting GE_CLK_HRT_RCVR_EN causes the subsystem to request the chip to drive the digital recovered heartbeat clock at the GP_CLK pin.	0x0	R/W
1	GE_CLK_HRT_FREE_EN	The GE PHY provides a digital free running heartbeat clock. This clock is sourced either from the 25MHz reference clock or the 125MHz free running clock depending on the mode that the PHY is in and on the settings of certain registers. Setting GE_CLK_HRT_FREE_EN causes the subsystem to request the chip to drive the digital free running heartbeat clock at the GP_CLK pin	0x0	R/W
0	GE_CLK_25_EN	When this bit is set, the 25MHz reference clock from the crystal oscillator is driven at the GP_CLK pin (having been processed through the digital block and is not as clean as the equivalent clock available at the CLK25_REF pin).	0x0	R/W

GE Subsystem RGMII Configuration Register

Register Address: 0xFF23, Reset: 0x7E07, Name: GE_RGMII_CFG

This register allows the MAC interface RGMII configuration to be controlled.

Table 206. Bit Descriptions for GE_RGMII_CFG

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0xF	R/W
10	GE_RGMII_100LOW_LTNCY_EN	Enable/Disable Low RGMII Latency for 100BASE-TX. 1: enable low RGMII latency for 100BASE-TX. 0: disable low RGMII latency for 100BASE-TX	0x1	R/W
9	GE_RGMII_10LOW_LTNCY_EN	Enable/Disable Low RGMII Latency for 10BASE-T. 1: enable low RGMII latency for 10BASE-T. 0: disable low RGMII latency for 10BASE-T.	0x1	R/W
[8:6]	GE_RGMII_RX_SEL	This field allows the RGMII receive clock delay to be specified in terms of the delay locked loop (DLL) unit delay (tu = 200ps). 111: 10 × tu + 400ps	0x0	R/W

REGISTER SUMMARY

Table 206. Bit Descriptions for GE_RGMII_CFG (Continued)

Bits	Bit Name	Description	Reset	Access
		110: 9 × tu + 400ps 101: reserved. 100: reserved. 011: reserved. 010: 7 × tu + 400ps 001: 6 × tu + 400ps 000: 8 × tu + 400ps		
[5:3]	GE_RGMII_GTX_SEL	This field allows the RGMII transmit clock delay to be specified in terms of the DLL unit delay (tu = 200ps). 111: 10 × tu + 400ps 110: 9 × tu + 400ps 101: reserved. 100: reserved. 011: reserved. 010: 7 × tu + 400ps 001: 6 × tu + 400ps 000: 8 × tu + 400ps	0x0	R/W
2	GE_RGMII_RX_ID_EN	Enable/disable receive clock internal 2ns delay in RGMII mode. Note that the default value of this bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable receive clock internal 2ns delay in RGMII mode. 0: disable receive clock internal 2ns delay in RGMII mode	0x1	R/W
1	GE_RGMII_TX_ID_EN	Enable/disable transmit clock internal 2ns delay in RGMII mode. Note that the default value of this bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable transmit clock internal 2ns delay in RGMII mode. 0: disable transmit clock internal 2ns delay in RGMII mode.	0x1	R/W
0	GE_RGMII_EN	This bit selects the RGMII MAC interface mode. Note that the default value of this bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W

GE Subsystem RMII Configuration Register

Register Address: 0xFF24, Reset: 0x1116, Name: GE_RMII_CFG

This register allows the MAC interface RMII configuration to be controlled.

Table 207. Bit Descriptions for GE_RMII_CFG

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x1	R
11	GE_RMII_CLK_5M	This bit sets the RMII REF_CLK frequency to 5MHz, valid only for 10Mbit/s operation. When enabled, the XTAL_I input must be 25MHz, and a 5MHz RMII REF_CLK is output on TX_CLK. This register is intended for evaluation and debugging purposes only. It is recommended to retain the default pin configuration. If modification is required, it should only be performed while the MAC interface is disabled.	0x0	R/W
[10:8]	RESERVED	Reserved.	0x1	R/W
7	GE_RMII_FIFO_RST	This field allows the RMII FIFO to be reset	0x0	R/W
[6:4]	GE_RMII_FIFO_DPTH	This field allows the RMII receive FIFO depth to be selected. 000: ± 4 bits 001: ± 8 bits 010: ± 12 bits 011: ± 16 bits	0x1	R/W

REGISTER SUMMARY

Table 207. Bit Descriptions for GE_RMII_CFG (Continued)

Bits	Bit Name	Description	Reset	Access
		100: ± 20 bits 101: ± 24 bits 110: Reserved. 111: Reserved.		
3	GE_RMII_TXD_CHK_EN	This bit determines whether or not the TXD_0 pin and TXD_1 pin is monitored to detect the start of a frame. This bit allows connecting the RMII receive CRS_DV to the RMII TX_EN signal. This allows a receiver to transmit RMII pin loopback for media converter applications. This is something that it is not supported in the RMII specification.	0x0	R/W
2	GE_RMII_CRS_EN	This bit determines whether or not CRS is encoded in the CRS_DV output signal. This allows a receiver to transmit RMII pin loopback for media converter applications. This is something that it is not supported in the RMII specification	0x1	R/W
1	GE_RMII_BAD_SSD_RX_ER_EN	This bit determines whether or not the RX_ER output signal is asserted when a False Carrier (Bad SSD) is detected. When cleared RX_ER will only be asserted in case of a symbol error during a frame.	0x1	R/W
0	GE_RMII_EN	This bit selects the RMII MAC interface mode. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. As RMII mode requires a 50MHz reference clock, the RMII interface must be configured from the hardware configuration pins and not from software.	0x0	R/W

GE Subsystem Copper PHY Base Configuration Register

Register Address: 0xFF26, Reset: 0x0086, Name: GE_PHY_BASE_CFG

This subsystem register allows the enhanced link detection function of the PHY to be configured for 100BASE-TX and for 1000BASE-T and allows 1000BASE-T retrain to be configured. Each time a Copper PHY core software reset is issued, the PHY resets its registers, including the 1000BASE-T retrain enable register bit (B_1000_RTRN_EN bit, Address 0xA001, Bit 0) and the enhanced link detection 1000BASE-T and 100BASE-TX enable register bits (within the FLD_EN register, Address 0x8E27). The default value of the B_1000_RTRN_EN bit is set via the 1000BASE-T retrain enable configuration bit (GE_RTRN_EN_CFG, within this register). The default value of the enhanced link detection 1000BASE-T enables register bits (within the FLD_EN register) are set via the GE_FLD_1000_EN_CFG bit and GE_FLD_100_EN_CFG bit within this register. If the value of any of these enable configuration bits are changed, the corresponding 1000BASE-T retrain enable register bit and the enhanced link detection 1000BASE-T and 100BASE-TX enable register bits in the PHY only change after a PHY software reset.

Table 208. Bit Descriptions for GE_PHY_BASE_CFG

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	GE_RTRN_EN_CFG	When this bit is set, the IEEE Standard 802.3 1000BASE-T retrain functionality is enabled in the PHY	0x0	R/W
11	GE_FLD_1000EN_CFG	When this bit is set, the enhanced link detection functionality is enabled when the PHY establishes a 1000BASE-T link.	0x1	R/W
10	GE_FLD_100EN_CFG	When this bit is set, the enhanced link detection functionality is enabled when the PHY establishes a 100BASE-TX link.	0x1	R/W
[9:5]	RESERVED	Reserved.	0x4	R/W
4	GE_MAN_MDI_FLIP_CFG	This bit allows the order of the PHY dimensions to be reversed to accommodate alternative board layouts and simplify the routing with a different RJ-45 orientation. 1: Inverts the mapping of the MDI pins. The analog physical pair 0 is mapped to digital logical pair 3, analog physical pair 1 to digital logical pair 2, analog physical pair 2 to digital logical pair 1 and analog physical pair 3 to digital logical pair 0. 0: Default MDI mapping.	0x0	R/W
3	GE_PHY_SFT_PD_CFG	When this bit is set, the PHY enters software power-down on exit from reset.	0x0	R/W
[2:0]	RESERVED	Reserved.	0x6	R/W

REGISTER SUMMARY

GE Subsystem Gigabit Ethernet PHY Configuration Register

Register Address: 0xFF27, Reset: 0x0002, Name: GE_PHY_IF_CFG

This register is used to configure the PHY Interface.

Table 209. Bit Descriptions for GE_PHY_IF_CFG

Bits	Bit Name	Description	Reset	Access
[15:5]	RESERVED	Reserved.	0x0	R
[4:2]	GE_FIFO_DPTH	This field allows the PHY FIFO depth to be configured. Setting a larger value allows longer (jumbo) packets to be handled but increases latency. In latency sensitive applications, this field must always be left at the default value of 0x0 because this value provides the lowest latency.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x2	R/W

GE Subsystem LED Active Low Status Register

Register Address: 0xFF29, Reset: 0x0004, Name: GE_PHY_LED_CFG

This register allows the PHY LED O/Ps to be configured. The individual fields are broken out in the following rows.

Table 210. Bit Descriptions for GE_PHY_LED_CFG

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R/W
6	LED_D_INV_EN	When this bit is set, it specifies that the LED signal is active low. Note that the default value of this register bit is configurable via the hardware configuration pins.	0x0	R/W
5	LED_C_INV_EN	When this bit is set, it specifies that the LED signal is active low. Note that the default value of this register bit is configurable via the hardware configuration pins.	0x0	R/W
4	LED_B_INV_EN	When this bit is set, it specifies that the LED signal is active low. Note that the default value of this register bit is configurable via the hardware configuration pins.	0x0	R/W
3	LED_A_INV_EN	When this bit is set, it specifies that the LED signal is active low. Note that the default value of this register bit is configurable via the hardware configuration pins.	0x0	R/W
[2:0]	RESERVED	Reserved.	0x4	R/W

GE Subsystem 10BASE-T Preamble Generation Register

Register Address: 0xFF38, Reset: 0x0000, Name: GE_B10_REGEN_PRE

In normal operation, the 10BASE-T preamble is consumed while synchronizing 10BASE-T receive timing and only 1 byte or 2 bytes of preamble are sent to the MAC. Setting this bit causes the GE subsystem to regenerate a full 10BASE-T preamble.

Table 211. Bit Descriptions for GE_B10_REGEN_PRE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GE_B10_REGEN_PRE	Setting this bit causes the GE subsystem to regenerate a full 10BASE-T preamble. This field must always be left at the default value of 0x0 for general use and set to 0x1 for media converter applications.	0x0	R/W

GE Subsystem RGMII I/O Control Register

Register Address: 0xFF3A, Reset: 0x0005, Name: GE_RGMII_IO_CNTRL

This register allows the characteristics of the RGMII I/O pins to be controlled.

Table 212. Bit Descriptions for GE_RGMII_IO_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R

REGISTER SUMMARY

Table 212. Bit Descriptions for GE_RGMII_IO_CNTRL (Continued)

Bits	Bit Name	Description	Reset	Access
[3:2]	GE_RGMII_RX_DRV	This bit field allows the drive strength of the RGMII receive buffers to be modified. Lower values correspond to higher drive current.	0x1	R/W
[1:0]	RESERVED	Reserved.	0x1	R/W

GE Subsystem Clock I/O Control Register

Register Address: 0xFF3B, Reset: 0x0002, Name: GE_CLK_IO_CNTRL

This register allows the characteristics of the clock I/O pins to be controlled.

Table 213. Bit Descriptions for GE_CLK_IO_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:1]	GE_CLK_DRV	This bit field allows the drive strength of the clock buffers (and LINK_ST) to be modified. Lower values correspond to higher drive current.	0x1	R/W
0	RESERVED	Reserved.	0x0	R/W

GE Subsystem Link Status Invert Enable Register

Register Address: 0xFF3C, Reset: 0x0000, Name: GE_LNK_STAT_INV_EN

This register allows the link status output signal on the LINK_ST pin to be inverted, meaning that link up is indicated by setting LINK_ST low.

Table 214. Bit Descriptions for GE_LNK_STAT_INV_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GE_LINK_ST_INV_EN_CFG	When set to 1, this bit enables the link status output signal on the LINK_ST pin to be inverted, meaning that link up is indicated by setting LINK_ST low.	0x0	R/W

GE Subsystem Link Status Pin Override Control Register

Register Address: 0xFF3D, Reset: 0x0000, Name: GE_IO_LINK_ST_OR_CNTRL

This register allows the default function of the LINK_ST pin to be overridden.

Table 215. Bit Descriptions for GE_IO_LINK_ST_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	GE_IO_LINK_ST_OR_CNTRL	This field allows the default function of the LINK_ST pin to be overridden. 1010: Wake on LAN indication 1001: LED_3 1000: LED_2 0110: RESERVED 0101: COL 0100: CRS 0011: receive start of packet indication 0010: transmit start of packet indication 0001: Link Status 0000: Default function. The default function, and for the settings not listed, is Link Status.	0x0	R/W

GE Subsystem INT_N Pin Override Control Register

Register Address: 0xFF3E, Reset: 0x0000, Name: GE_IO_INT_N_OR_CNTRL

REGISTER SUMMARY

This register allows the default function of the INT_N pin to be overridden.

Table 216. Bit Descriptions for GE_IO_INT_N_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	GE_IO_INT_N_OR_CNTRL	This field allows the default function of the INT_N pin to be overridden. 1010: Wake-on-LAN indication 1001: LED_3 1000: LED_2 0110: TX_ER 0101: COL 0100: CRS 0011: receive start of packet indication 0010: transmit start of packet indication 0001: link Status 0000: default function. The default function is CRS when configured for MII MAC interface and EEE advertisement is disabled from pin configuration. In all other cases, the default function is INT_N.	0x0	R/W

GE Subsystem GTX_CLK Pin Override Control Register

Register Address: 0xFF3F, Reset: 0x0000, Name: GE_IO_GTX_CLK_OR_CNTRL

This register allows the default function of the GTX_CLK pin to be overridden.

Table 217. Bit Descriptions for GE_IO_GTX_CLK_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
[1:0]	GE_IO_GTX_CLK_OR_CNTRL	This field allows the default function of the TX_CLK pin to be overridden. The settings are as follows: 10: MII transmit output clock (TX_CLK) 00: Default function. The default function is TX_CLK when configured for MII MAC interface. In all other cases, and for the settings not listed, the function of the pin is the RGMII input transmit clock (TXC). This pin is an unused input when the RMII MAC interface is selected.	0x0	R/W

GE Subsystem LED 0 Pin Override Control Register

Register Address: 0xFF40, Reset: 0x0000, Name: GE_IO_LED_A_OR_CNTRL

This register allows the default function of the LED_0 chip pin to be overridden.

Table 218. Bit Descriptions for GE_IO_LED_A_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	GE_IO_LED_A_OR_CNTRL	This field allows the default function of the LED_0 pin to be overridden. The settings are as follows: 1000: Wake-on-LAN wake indication 0111: GE PHY Test Clock Enable 0110: reserved 0101: COL 0100: CRS 0011: receive start of packet indication 0010: transmit start of packet indication 0001: link status 0000: default function. The default function, and for all the settings not listed, is LED_0.	0x0	R/W

REGISTER SUMMARY

GE Subsystem LED 1 Pin Override Control Register

Register Address: 0xFF41, Reset: 0x0000, Name: GE_IO_LED_B_OR_CNTRL

This register allows the default function of the LED_1 chip pin to be overridden.

Table 219. Bit Descriptions for GE_IO_LED_B_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	GE_IO_LED_B_OR_CNTRL	This field allows the default function of the LED_1 pin to be overridden. The settings are as follows: 111: Wake-on-LAN wake indication 110: TX_ER 101: COL 100: CRS 0011: receive start of packet indication 0010: transmit start of packet indication 001: link status 000: default function. The default function is COL when configured for MII MAC interface and EEE advertisement is disabled from pin configuration, and TX_ER when EEE advertisement is configured from pins. In all other cases, and for the settings not listed, is LED_1.	0x0	R/W

GE Subsystem LED 2 Pin Override Control Register

Register Address: 0xFF42, Reset: 0x0000, Name: GE_IO_LED_C_OR_CNTRL

This register allows the default function of the LED_2/GP_CLK pin to be overridden.

Table 220. Bit Descriptions for GE_IO_LED_C_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	GE_IO_LED_C_OR_CNTRL	This register allows the default function of the LED_2/GP_CLK pin to be overridden. The settings are as follows: 1000: Wake on LAN wake indication 0111: PHY clock selected in GE_CLK_CFG address (except GE_REF_CLK_EN) 0110: RX_ER 0101: COL 0100: CRS 0011: receive start of packet indication 0010: transmit start of packet indication 0001: link status 0000: default function. The default function is RX_ER when configured for MII or RMII MAC interface. In all other cases, and for the settings not listed, is LED_2.	0x0	R/W

SerDes Subsystem Advertisement Configuration Register

Device Address: 0x1E; Register Address: 0xFF53, Reset: 0x0100, Name: GE_SD_CFG

This register allows the SerDes subsystem advertisement configuration to be controlled.

Note that any register whose label ends with _CFG will not take effect until after the GE subsystem is reset.

Table 221. Bit Descriptions for GE_SD_CFG

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
8	SD_BASEX_MMR_EN	Enable direct registers access in RGMII/RMII/MII to fiber/backplane media mode.	0x1	R/W
[7:5]	SD_LINK_TYPE_CFG	SerDes Link Type Configuration: 111: 1000BASE-LX/SX half-duplex and full-duplex	0x0	R/W

REGISTER SUMMARY

Table 221. Bit Descriptions for GE_SD_CFG (Continued)

Bits	Bit Name	Description	Reset	Access
		110: 1000BASE-LX/SX half duplex 101: 1000BASE-LX/SX full duplex 100: 1000BASE-KX 011: 100BASE-FX full-duplex 010: 100BASE-FX half-duplex 001: reserved 000: No BASE-X		
[4:3]	SD_CTLE_CFG	These bits select the Continuous Time Linear Equalization configuration index.	0x0	R/W
2	SD_AUTONEG_EN_CFG	When this bit is set, Clause 37 autonegotiation will be enabled.	0x0	R/W
1	SD_SGMII_MAC_EN	When this bit is set SGMII, is configured in MAC mode.	0x0	R/W
0	SD_SGMII_EN	When this bit is set SGMII, is enabled.	0x0	R/W

GE Auto Media Select Status Register

Register Address: 0xFF57, Reset: 0x0000, Name: GE_MSEL_AUTO_STAT

The GE auto media selection status register allows various auto selection status to be observed.

Table 222. Bit Descriptions for GE_MSEL_AUTO_STAT

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	GE_MSEL_AUTO_SD	This bit indicates that the fiber/backplane media has been selected.	0x0	R
0	GE_MSEL_AUTO_GE	This bit indicates that the copper media has been selected. This bit is never set simultaneously with GE_MSEL_AUTO_SD.	0x0	R

GE Subsystem Wake on Lan System Control Register

Register Address: 0xFF78, Reset: 0x0000, Name: GE_WOL_SYS_CNTRL

This register allows the WoL configuration in the system to be controlled.

Table 223. Bit Descriptions for GE_WOL_SYS_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	GE_WOL_WAKE_INV_EN	When this bit is set, the WoL wake signal to the selected output pin is inverted. See also related GE I/O override control registers (GE_IO_LINK_ST_OR_CNTRL, GE_IO_INT_NOR_CNTRL, GE_IO_LED[A-C]_OR_CNTRL)	0x0	R/W
0	GE_WOL_2_PHY_SD_SEL	When set this bit enables monitoring of the SD PHY G/MII RX signals by WoL in applications where both PHYs are used.	0x0	R/W

GE Subsystem Wake on Lan Enable Register

Register Address: 0xFF79, Reset: 0x0000, Name: GE_WOL_EN

Enables the Wake-on-LAN (WoL) functionality.

Table 224. Bit Descriptions for GE_WOL_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GE_WOL_EN	GE_WOL_EN. When set this bit enables the Wake-on-LAN (WoL) functionality.Note that in general parts of the WoL logic may operate on a clock that is asynchronous with the clock that is used by the Management Interface. To avoid any unexpected behavior arising due to asynchronous clocks all relevant WoL configuration registers should be written before setting this bit. WoL configuration registers should not be changed on-the-fly while this bit is set.	0x0	R/W

REGISTER SUMMARY

GE Subsystem Wake on Lan Wake Control Register

Register Address: 0xFF7A, Reset: 0x0001, Name: GE_WOL_WAKE_CNTRL

This register allows the WoL wake behavior to be controlled.

Table 225. Bit Descriptions for GE_WOL_WAKE_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	GE_WOL_KEY_ERR_WAKE_EN	When set this bit enables WoL wake on key error.	0x0	R/W
0	GE_WOL_LS_CHG_WAKE_EN	When set this bit enables WoL wake on a change of link status.	0x1	R/W

GE Subsystem Wake on Lan Signal Control Register

Register Address: 0xFF7B, Reset: 0x0100, Name: GE_WOL_SIG_CNTRL

This registers allows the signaling of WoL events to be controlled.

Table 226. Bit Descriptions for GE_WOL_SIG_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:8]	GE_WOL_PUL_LENM_1	This registers specifies the length of the pulses that are used to signal WoL events when the GE_WOL_PUL_EN bit is set. The programmed value represents the number of cycles of the 25MHz system clock less 1 for which the pulsed signal is asserted.	0x1	R/W
[7:2]	RESERVED	Reserved.	0x0	R
1	GE_WOL_OS_EN	When GE_WOL_PUL_EN is set and this bit is set one-shot operation is enabled. In this case a WoL event is signaled by issuing a pulse after which WoL filter matching stops. When GE_WOL_PUL_EN is set and this bit is clear WoL filter matching operates continuously with each event being signaled by issuing a pulse.	0x0	R/W
0	GE_WOL_PUL_EN	When set this bit enables the signaling of WoL events using pulses rather than levels.	0x0	R/W

GE Subsystem Wake on Lan Station 0 Address Register

Register Address: 0xFF7C, Reset: 0x0000, Name: GE_WOL_STA_0_AD_01

This register specifies station 0 address bytes 0 and 1.

Table 227. Bit Descriptions for GE_WOL_STA_0_AD_01

Bits	Bit Name	Description	Reset	Access
[15:8]	GE_WOL_STA_0_AD_1	Station 0 address byte 1.	0x0	R/W
[7:0]	GE_WOL_STA_0_AD_0	Station 0 address byte 0. Magic Packet Filtering is disabled if this value is set to 8'hFF.	0x0	R/W

GE Subsystem Wake on Lan Station 0 Address Register

Register Address: 0xFF7D, Reset: 0x0000, Name: GE_WOL_STA_0_AD_23

This register specifies station 0 address bytes 2 and 3.

Table 228. Bit Descriptions for GE_WOL_STA_0_AD_23

Bits	Bit Name	Description	Reset	Access
[15:8]	GE_WOL_STA_0_AD_3	Station 0 address byte 3.	0x0	R/W
[7:0]	GE_WOL_STA_0_AD_2	Station 0 address byte 2.	0x0	R/W

GE Subsystem Wake on Lan Station 0 Address Register

Register Address: 0xFF7E, Reset: 0x0000, Name: GE_WOL_STA_0_AD_45

REGISTER SUMMARY

This register specifies station 0 address bytes 4 and 5.

Table 229. Bit Descriptions for GE_WOL_STA_0_AD_45

Bits	Bit Name	Description	Reset	Access
[15:8]	GE_WOL_STA_0_AD_5	Station 0 address byte 5.	0x0	R/W
[7:0]	GE_WOL_STA_0_AD_4	Station 0 address byte 4.	0x0	R/W

GE Subsystem Magic Packet Control Register

Register Address: 0xFF80, Reset: 0x0073, Name: GE_MGC_0_CNTRL

This registers allows Magic Packet Filter 0 to be controlled. The individual fields are broken out on the following rows.

This filter matches a magic pattern consisting of the value 8'hFF repeated 6 times followed by 6 repititions of the station 0 address. This pattern may be required to be immediately followed by a specified SecureOn key.

Table 230. Bit Descriptions for GE_MGC_0_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R
9	GE_MGC_0_MGC_CHK_DIS	When set this bit disables the magic pattern check. In this mode the filter matches any frame that satisfies the DA matching criteria and passes the CRC and length checks, if these are enabled. This bit is provided to simplify system testing as the response to a wake event can be evaluated by sending any type of packet.	0x0	R/W
8	GE_MGC_0_KEY_4BY_EN	When set this bit enables a 4-byte SecureOn key.	0x0	R/W
7	GE_MGC_0_KEY_CHK_EN	When set this bit enables the SecureOn key check.	0x0	R/W
6	GE_MGC_0_LEN_CHK_EN	When set this bit enables length checking on a received frame containing a magic packet. If the check fails, then the frame is ignored.	0x1	R/W
5	GE_MGC_0_CRC_CHK_EN	When set this bit enables CRC checking on a received frame containing a magic packet. If the check fails, then the frame is ignored.	0x1	R/W
4	GE_MGC_0_DA_BC_AD_EN	When set this bit enables matching of the broadcast address in the DA field of a received frame.	0x1	R/W
3	GE_MGC_0_DA_MC_AD_EN	When set this bit enables matching of any multicast address in the DA field of a received frame.	0x0	R/W
2	GE_MGC_0_DA_UC_AD_EN	When set this bit enables matching of any unicast address in the DA field of a received frame.	0x0	R/W
1	GE_MGC_0_DA_STA_0_AD_EN	When set this bit enables matching of the station 0 address in the DA field of a received frame.	0x1	R/W
0	GE_MGC_0_EN	When set this bit enables the filter.	0x1	R/W

GE Subsystem SecureOn Key Register

Register Address: 0xFF81, Reset: 0x0000, Name: GE_MGC_0_KEY_01

This register specifies bytes 0 and 1 of the SecureOn key for Magic Packet Filter 0.

Table 231. Bit Descriptions for GE_MGC_0_KEY_01

Bits	Bit Name	Description	Reset	Access
[15:8]	GE_MGC_0_KEY_1	Magic Packet Filter 0 SecureOn key byte 1.	0x0	R/W
[7:0]	GE_MGC_0_KEY_0	Magic Packet Filter 0 SecureOn key byte 0.	0x0	R/W

GE Subsystem SecureOn Key Register

Register Address: 0xFF82, Reset: 0x0000, Name: GE_MGC_0_KEY_23

This register specifies bytes 2 and 3 of the SecureOn key for Magic Packet Filter 0.

REGISTER SUMMARY

Table 232. Bit Descriptions for GE_MGC_0_KEY_23

Bits	Bit Name	Description	Reset	Access
[15:8]	GE_MGC_0_KEY_3	Magic Packet Filter 0 SecureOn key byte 3.	0x0	R/W
[7:0]	GE_MGC_0_KEY_2	Magic Packet Filter 0 SecureOn key byte 2.	0x0	R/W

GE Subsystem SecureOn Key Register

Register Address: 0xFF83, Reset: 0x0000, Name: GE_MGC_0_KEY_45

This register specifies bytes 4 and 5 of the SecureOn key for Magic Packet Filter 0.These bytes are not used when the GeMgc0Key4ByEn bit is set

Table 233. Bit Descriptions for GE_MGC_0_KEY_45

Bits	Bit Name	Description	Reset	Access
[15:8]	GE_MGC_0_KEY_5	Magic Packet Filter 0 SecureOn key byte 53.	0x0	R/W
[7:0]	GE_MGC_0_KEY_4	Magic Packet Filter 0 SecureOn key byte 4.	0x0	R/W

GE Subsystem Wake on Lan Status Register

Register Address: 0xFF85, Reset: 0x0000, Name: GE_WOL_STAT

This address allows the the WoL status to be observed.

Table 234. Bit Descriptions for GE_WOL_STAT

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	GE_MGC_0_KEY_ERR	When this bit is read as 1'b1 it indicates that Magic Packet Filter 0 has matched one or more frames with SecureOn key errors since the last time the WoL status was read.	0x0	R SC
1	GE_MGC_0_FRM_MATCH	When this bit is read as 1'b1 it indicates that Magic Packet Filter 0 has matched one or more frames since the last time the WoL status was read.	0x0	R SC
0	GE_WOL_LS_CHG	When this bit is read as 1'b1 it indicates that the link status has changed one or more times since the last time the WoL status was read.	0x0	R SC

PCB LAYOUT RECOMMENDATIONS

This is an overview of the key areas of interest during placement and layout of the PHY and corresponding support components. Take care when routing high speed interface signals to maximize signal performance and ensure optimum EMC performance, with a view to ensure critical signal traces are kept as short as possible to minimize noise coupling.

PHY PACKAGE LAYOUT

The LFCSP has an exposed pad underneath the package that must be soldered to the PCB ground for mechanical and thermal reasons. For thermal impedance performance and to maximize heat removal, use of a 4 × 4 array of thermal vias beneath the exposed ground pad is recommended.

There are also two bus bars on the side of the exposed pad. These bus bars are connected to internal voltage rails and are not intended to be, and must not be soldered to the board. The PCB land pattern must incorporate the exposed ground paddle with vias and these two keep out areas around the bus bars in the footprint. No PCB traces or vias can be used in either of the keep out areas.

COMPONENT PLACEMENT

Prioritization of the critical traces and components helps simplify the routing exercise. Place and orient the critical traces and components first to ensure an effective layout with minimal turns, vias, and crossing traces. For an Ethernet PHY layout, the important components are the crystal and load capacitors, the transformer on the MDI lines, and all bypass capacitors local to the device. Prioritize these components and the routing to them. Keep the PHY chip at least 1 in. away from the edge of the board. The following sections provide more detail for each of the areas.

Crystal Placement and Routing

To ensure minimum current consumption and to minimize stray capacitances, make connections between the crystal, capacitors, and ground as close to the ADIN1320 as possible and preferably on the same side as the device.

Magnetics Placement

Orient the magnetics and RJ45 in line with the MDI_x_x pins from the PHY chip.

MDI, DIFFERENTIAL PAIR ROUTING

The MDI interface runs from the ADIN1320 PHY to the transformer, and from there to the RJ45 connector. Traces running from the MDI_x_x pins of the ADIN1320 to the magnetics must be on the same side of the board, kept as short as possible (ideally less than 1 in. in length), and individual trace impedance of these tracks kept below 50 Ω, with differential impedance of 100 Ω for each pair. The same recommendations apply for traces running from the magnetics to the RJ45 connector. Keep impedances constant throughout because any discontinuities may affect signal integrity.

Each pair must be routed together, trace widths kept the same throughout, trace lengths kept equal where possible, and avoid any right angles on these traces (use curves in traces or 45° angles). Avoid stubs on all signal traces. Where possible, route traces on the same layer.

Route traces over a continuous reference plane with no interruptions to reduce inductance.

Where possible, ensure a solid return path underneath all signal traces. Avoid routing signal traces across plane splits.

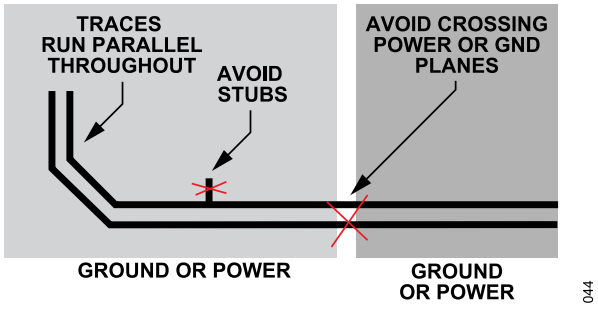


Figure 53. Things to Avoid when Routing Differential Pairs

SGMII, DIFFERENTIAL PAIR ROUTING

To ensure high signal integrity and reliable SGMII performance in high-speed PCB designs, it's crucial to adhere to certain practices. Optimal PCB trace routing of SGMII and differential pairs requires appropriate trace widths and spacing to achieve a differential impedance of 100Ω. It's important to maintain length matching within 5 mils (0.127mm) and route traces as directly and symmetrically as possible. Crosstalk can be minimized by isolating differential pairs and maintaining a continuous ground plane beneath them. Using AC coupling capacitors of 100nF near SGMII devices and ensuring any required termination resistors match the differential impedance is also recommended. To prevent signal degradation, minimize vias, avoid stubs, and use backdrilling for vias when needed. Lastly, employing signal integrity simulation tools to validate designs and performing prototyping with tests such as eye diagrams, TDR, and BER is essential to ensure performance.

MAC INTERFACE PINS

All signals within the transmit group must be length matched and similarly for all signals within the receive group. Where possible, route these interface pins on the same side as the component pins. Keep trace lengths as short as possible. Route traces with an impedance of 50 Ω to ground.

The user has the capability to program the drive current of the RGMII pins to help improve signal integrity and minimize ringing. Alternatively, series termination resistors can be placed in all RGMII output pins if further tuning is required.

PCB LAYOUT RECOMMENDATIONS

POWER AND GROUND PLANES

From a PCB layout point of view, it is important to place the decoupling capacitors as close as possible to the power and GND pins to minimize the inductance.

Magnetics Module Grounding

A split ground plane under the transformer minimizes noise coupling across the transformer and between adjacent coils within. Ensure a physical separation of the ground planes underneath the transformer. Make the width of this separation at least 100 mil.

RJ45 Module Grounding

For optimal EMC performance, it is recommended to use a metal shielded RJ45 connector with the shield connected to chassis ground. There must be an isolation gap between the chassis ground and the PHY IC ground with consistent isolation across all layers.

OUTLINE DIMENSIONS

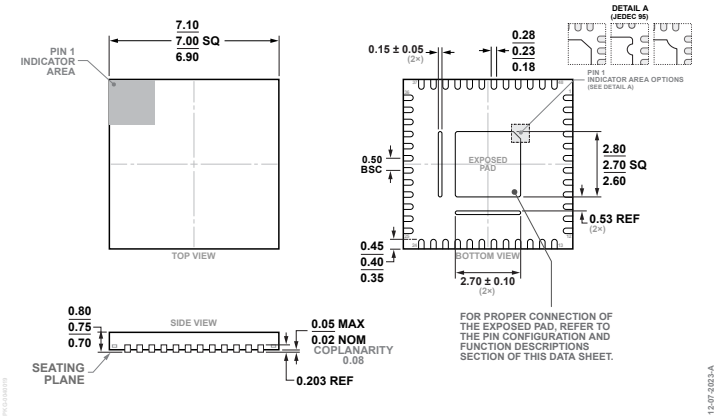


Figure 54. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-29)
Dimensions shown in millimeters

Updated: July 13, 2026

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADIN1320BCPZ	-40°C to +85°C	48-Lead LFCSP (7mm x 7mm x 0.75mm)	TRAY, 260	CP-48-26
ADIN1320BCPZ-R7	-40°C to +85°C	48-Lead LFCSP (7mm x 7mm x 0.75mm)	REEL, 750	CP-48-26
ADIN1320CCPZ	-40°C to +105°C	48-Lead LFCSP (7mm x 7mm x 0.75mm)	TRAY, 260	CP-48-26
ADIN1320CCPZ-R7	-40°C to +105°C	48-Lead LFCSP (7mm x 7mm x 0.75mm)	REEL, 750	CP-48-26

[1] Z = RoHS Compliant Part.

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