Data Sheet

ADHV4702-1

24 V to 220 V Precision Operational Amplifier

FEATURES

- Wide range of operating voltages
  - Dual-supply: ±12 V to ±110 V
  - Asymmetrical supply operation: 24 V to 220 V, VCC ≤ 175 V
- Wide input common-mode voltage range: 3 V from rails
- High common-mode rejection ratio: 160 dB typical
- High AOL: 170 dB typical
- High slew rate
  - 74 V/µs typical
  - 24 V/µs typical with external input clamping diodes
- Low input bias current: 2 pA maximum
- Low input offset voltage: 1 mV maximum
- Low input offset voltage drift: 2 µV/°C maximum
- Low input voltage noise: 8 nV/√Hz typical at 10 kHz
- Wide small signal bandwidth: 10 MHz typical
- Resistor adjustable quiescent current: 0.6 mA to 3 mA (VS = ±110 V)
- Unity-gain stable
- Thermal monitoring
- Small footprint: *12-lead, 7 mm × 7 mm LFCSP* compliant with IEC 61010-1 spacing
- Shutdown mode

APPLICATIONS

- High-side current sensing
- Automated test equipment
- High voltage drivers
- Piezotransducers
- Digital-to-analog converter (DAC) output buffers
- Light detecting and ranging (LiDAR), avalanche photodiode (APD), single photon avalanche diode (SPAD) biasing

GENERAL DESCRIPTION

The ADHV4702-1 is a high voltage (220 V), unity-gain stable precision operational amplifier. The ADHV4702-1 offers high input impedance with low input bias current, low input offset voltage, low drift, and low noise for precision demanding applications. The next generation of proprietary semiconductor processes and innovative architecture from Analog Devices, Inc., enable this precision operational amplifier to operate from symmetrical dual supplies of ±110 V, asymmetrical dual supplies up to 220 V span, or a single supply up to 175 V.

For precision performance, the ADHV4702-1 has a 170 dB typical open-loop gain (AOL) and a 160 dB typical common-mode rejection ratio (CMRR), as shown in *Figure 3*. The ADHV4702-1 also has a 2 µV/°C maximum input offset voltage (VOS) drift and an 8 nV/√Hz input voltage noise.

The exceptional DC precision of the ADHV4702-1 is complemented by excellent dynamic performance with a small signal bandwidth of 10 MHz and a slew rate of 74 V/µs. The ADHV4702-1 has an output current of 20 mA typical.

The ADHV4702-1 offers high voltage input common-mode swing as well as high voltage output swing, enabling precision high voltage use cases such as high-side current sensing.

The ADHV4702-1 is available in a *12-lead, 7 mm × 7 mm lead frame chip scale package (LFCSP)* with an exposed pad (EPAD) compliant to international electrotechnical commission (IEC) 61010-1 creepage and clearance standards. The copper EPAD provides a low thermal resistance path to improve heat dissipation and features high voltage isolation, allowing it to be safely connected to a 0 V ground plane regardless of VCC or VEE voltages. The ADHV4702-1 operates over the −40°C to +85°C industrial temperature range.

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TYPICAL APPLICATION CIRCUIT

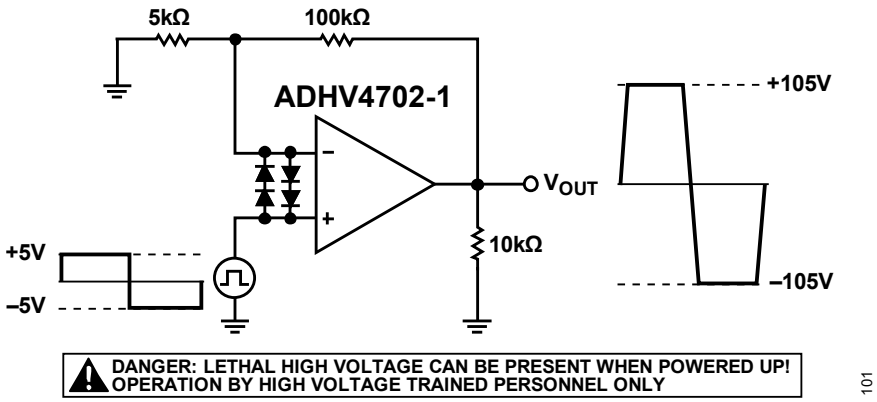

Figure 1. Typical Application Circuit

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		Changes to Figure	1
		Added Electrostatic Discharge (ESD) Ratings Section	5
		Added ESD Ratings for ADHV4702-1 Section and Table 4; Renumbered Sequentially	5
		Moved Figure 3	7
		Moved Figure 44	14
		Changes to Figure 44	14
		Changes to Figure 46	25
		Changes to Figure 63	20
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		Changes to Figure 65	20
Rev. D	4/2024	Changes to Features Section	1
		Changes to General Description Section	1
		Changes to ±12 V to ±110 V Supply Section and Table 1	3
		Changes to Table 2	5
		Changes to Power Supply and Decoupling Section	20
		Changes to Figure 63, Figure 64, and Figure 65	20
		Added Asymmetrical Power Supplies Operation Section	20
		Added Table 6, Figure 66, and Figure 67; Renumbered Sequentially	21
Rev. E	5/2025	Changes to Figure 1, Figure 42, and Figure 44	2, 17, 18
		Changes to Table of Contents	3
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		Added DGND Level Modification Section and Figure 68	30

Specifications

Table 1. Electrical Characteristics

(Supply voltage (V_S) = V_{CC} to V_{EE} = ±12 V to ±110 V , T_A = 25°C with an EPAD connected to a 0 V analog ground (AGND), DGND pin tied to 0 V AGND, R_{ADJ} = 0 Ω (R_{ADJ} is a resistor that connects the R_{ADJ} pin to DGND), gain (A_V) = 1, feedback resistor (R_F) = 100 kΩ and load resistance (R_{LOAD}) = 10 kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	f_{-3db}	A_V = 1, V_{OUT} = 200 mV p-p, R_F = 0 Ω		10		MHz
Slew Rate	SR	A_V = 20, V_{OUT} = 200 V p-p, 20% to 80%		74		V/µs
		A_V = 20, V_{OUT} = 200 V p-p, 20% to 80%, with external input clamping diodes [1]		24		V/µs
Settling Time to 0.1%	t_S	A_V = 1, V_{OUT} = 40 V p-p, R_F = 0 Ω		8.4		µs
		A_V = 20, V_{OUT} = 40 V p-p		6.2		µs
		A_V = 40, V_{OUT} = 40 V p-p		13		µs
NOISE PERFORMANCE						
Input Voltage Noise	e_n	Frequency = 10 kHz		8		nV/√Hz
Input Voltage Noise 1/f Corner				10		Hz
Input Current Noise	i_n	Frequency = 40 Hz		1		fA/√Hz
DC PERFORMANCE						
Input Offset Voltage	V_{OS}		-1	±0.15	+1	mV
Input Offset Voltage Drift	V_{OS_TC}	V_S = ±110 V, T_A = 25°C to 85°C	-2	±0.25	+2	µV/°C
		V_S = ±12 V, T_A = 25°C to 85°C	-3	±0.25	+3	µV/°C
Input Bias Current	I_B	T_A = 25°C	-2	±0.3	+2	pA
		T_A = 85°C	−100	±19	+100	pA
Input Bias Current Drift	I_{B_TC}	T_A = 25°C to 85°C		±0.3		pA/°C
Input Offset Current	I_{OS}	T_A = 25°C	-2	±0.15	+2	pA
		T_A = 85°C	−50	±8	+50	pA
Input Offset Current Drift	I_{OS_TC}	T_A = 25°C to 85°C		±0.13		pA/°C
Open-Loop Gain	A_{OL}	V_S = ±110 V	146	170		dB
		V_S = ±12 V	130	150		dB
INPUT CHARACTERISTICS						
Input Resistance Common-Mode	R_{INCM}	V_{CM} = −60 V to +60 V		45		TΩ
		V_{CM} = −90 V to +90 V		30		TΩ

(Supply voltage (V_S) = V_{CC} to V_{EE} = ±12 V to ±110 V , T_A = 25°C with an EPAD connected to a 0 V analog ground (AGND), DGND pin tied to 0 V AGND, R_{ADJ} = 0 Ω (R_{ADJ} is a resistor that connects the R_{ADJ} pin to DGND), gain (A_V) = 1, feedback resistor (R_F) = 100 kΩ and load resistance (R_{LOAD}) = 10 kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Resistance Differential	R_{IND}			4.2		TΩ
Input Capacitance Common-Mode	C_{INCM}			7.9		pF
Input Capacitance Differential	C_{IND}			17.9		pF
Input Common-Mode Voltage Range	V_{CM}			±107		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −70 V to +70 V	140	160		dB
SHUTDOWN PIN ($\overline{SD}$)						
Input Voltage Low	$VIL_{\overline{SD}}$	Disabled			0.8	V
Input Voltage High	$VIH_{\overline{SD}}$	Enabled	1.6			V
Input Current Low	$IIL_{\overline{SD}}$	$\overline{SD}$ = 0 V		-11		µA
Input Current High	$IIH_{\overline{SD}}$	$\overline{SD}$ = 5 V		-1		µA
OUTPUT CHARACTERISTICS						
Output Voltage Range	V_{OUT}	R_{LOAD} = 5 kΩ, T_A = −40°C to +85°C, V_S = ±110 V	108	108.5		V
				-108.5	-108	V
Output Current	I_{OUT}			20		mA
THERMAL MONITOR						
TMP Pin Voltage [2]	TMP	T_A = 25°C		1.9		V
TMP Pin Voltage Drift	$TMP_{\_TC}$	T_A = −40°C to +85°C		-4.5		mV/°C
POWER SUPPLY						
Operating Range	V_{CC} to V_{EE}		24		220	V
	V_{CC} to GND		12		175	V
	V_{EE} to GND		-175		0	V
Quiescent Current $\overline{SD}$ = 5 V (Enabled) [3]	I_Q	R_{ADJ} = 0 Ω, T_A = 25°C, V_S = ±110 V		3	3.3	mA
		R_{ADJ} = 0 Ω, T_A = 25°C, V_S = ±12 V		2.7	3.3	mA
		R_{ADJ} = 0 Ω, T_A = −40°C to +85°C			3.3	mA
		R_{ADJ} = 50 kΩ, T_A = 25°C, V_S = ±110 V		0.9	1	mA
		R_{ADJ} = 50 kΩ, T_A = 25°C, V_S = ±12 V		0.8	1	mA
		R_{ADJ} = 50 kΩ, T_A = −40°C to +85°C			1	mA

(Supply voltage (V_S) = V_{CC} to V_{EE} = ±12 V to ±110 V , T_A = 25°C with an EPAD connected to a 0 V analog ground (AGND), DGND pin tied to 0 V AGND, R_{ADJ} = 0 Ω (R_{ADJ} is a resistor that connects the R_{ADJ} pin to DGND), gain (A_V) = 1, feedback resistor (R_F) = 100 kΩ and load resistance (R_{LOAD}) = 10 kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Quiescent Current $\overline{SD}$ = 5 V (Enabled) [3]	I_Q	R_{ADJ} = 100 kΩ, T_A = 25°C, V_S = ±110 V		0.6		mA
Quiescent Current $\overline{SD}$ = 0 V (Disabled)	I_Q			0.18	0.2	mA
Power Supply Rejection Ratio	$PSRR_{VCC}$	V_{CC} = 107 V to 112.5 V, V_{EE} = 110 V	130	155		dB
		V_{CC} = 10 V to 14 V, V_{EE} = −12 V	110	130		dB
	$PSRR_{VEE}$	V_{CC} = 110 V, V_{EE} = −107 V to −112.5 V	130	155		dB
		V_{CC} = 12 V, V_{EE} = −10 V to −14 V	110	130		dB

1 This slew rate result is tested while the ADHV4702-1 inputs are clamped at the forward-biased voltage of two diodes using ON Semiconductor® SBAV199LT1G. For more information, see the *Slew Boost Circuit and Protection* section.

2 The TMP pin voltage may have device to device variation. For more information, see the *Temperature Monitor (TMP)* section.

3 This specification is for quiescent current only. For supply current or dynamic supply current information, see the *Theory of Operation* section.

Absolute Maximum Ratings

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{CC} to V_{EE}	225 V
V_{CC} to GND	180 V
V_{EE} to GND	-180 V
Output Voltage	$V_{CC\ to}\ V_{EE}$
Common-Mode Input Voltage	$V_{CC\ to}\ V_{EE}$
Differential Input Voltage	±2.0 V
Input Current	±5 mA
DGND Voltage	V_{CC} − 12 V to V_{EE}
RESERVED, $\overline{SD}$, and TMP Pins	DGND to DGND + 6 V
COMP Pin	V_{CC} − 5 V to V_{CC}
R_{ADJ} Pin	DGND to DGND + 0.6 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (Soldering 10 sec) [1]	260°C
Junction Temperature (T_J)	150°C

[1] See IPC/JEDEC J-STD-020 for more information.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Maximum Power Dissipation

The maximum safe power dissipation in the package is limited by the associated rise in T_J on the die. At approximately 150°C, which is the glass transition temperature, the plastic begins to change its properties. Exceeding a T_J of 150°C can result in changes in the silicon devices, potentially causing failure. *Table 3* shows the junction-to-case thermal resistance (θ_{JC}) for the LFCSP. For more detailed information on power dissipation and thermal management, see the *Applications Information* section.

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-12-8 [1]	37	1	°C/W

[1] The data is collected from a 2S2P board. A cold plate is attached to the bottom side of the PCB using 100 µm thermal interface material (TIM) for θ_{JC} simulation. See JEDEC standard for additional information.

Electrostatic Discharge (ESD) Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings for ADHV4702-1

Table 4. ADHV4702-1, 12-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
FICDM	±750	C3
HBM	±1000	1C
MM	±100	A

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin Configurations and Function Descriptions

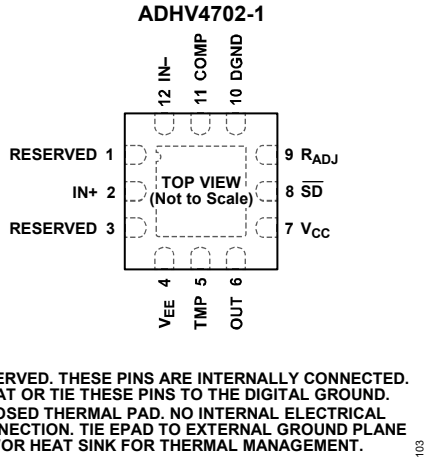

Figure 2. Pin Configuration

Pin Descriptions

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
1, 3	RESERVED	Reserved. These pins are internally connected. Float or connect these pins to the DGND.
2	IN+	Noninverting Input.
4	V_{EE}	Negative Power Supply Input.
5	TMP	Temperature Monitor Output.
6	OUT	Output.
7	V_{CC}	Positive Power Supply Input.
8	$\overline{SD}$	Shutdown (Active Low). $\overline{SD}$ is referenced to DGND
9	R_{ADJ}	Resistor Adjustable Quiescent Current. Connect R_{ADJ} to DGND to fully bias the amplifier.
10	DGND	Logic Reference for R_{ADJ} and $\overline{SD}$. Connect DGND to 0 V analog ground.
11	COMP	External Compensation.
12	IN-	Inverting Input.
	EPAD	Exposed Thermal Pad. No internal electrical connection. Tie EPAD to external ground plane and/or heat sink for thermal management.

Typical Performance Characteristics

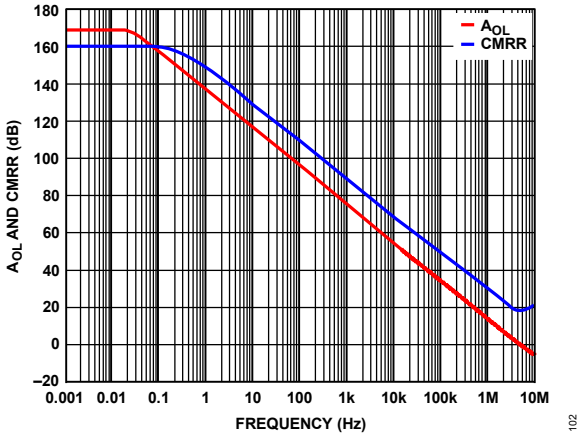

Figure 3. ADHV4702-1 Precision Performance

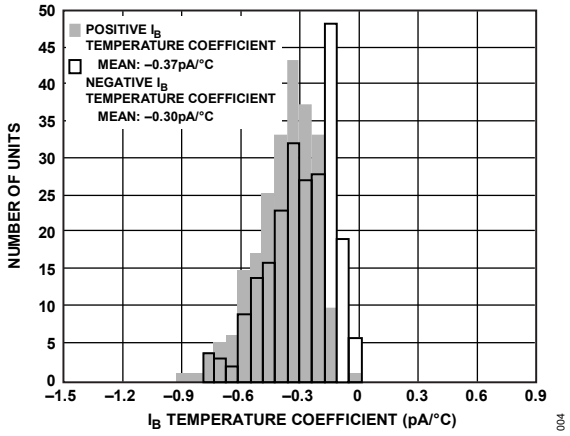

Figure 4. Positive and Negative Input Bias (I_B) Current Drift Distribution, T_A = 25°C, V_S = ±110 V, V_{CM} = 0 V, ΔT_A = 60°C, R_{ADJ} = 0 Ω

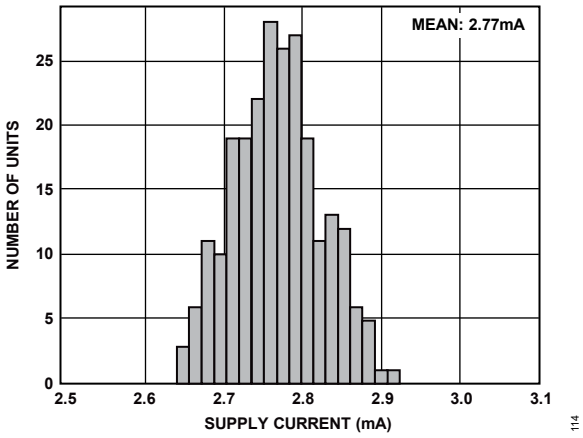

Figure 5. Supply Current Distribution, T_A = 25°C, V_S = ±110 V, R_{ADJ} = 0 Ω

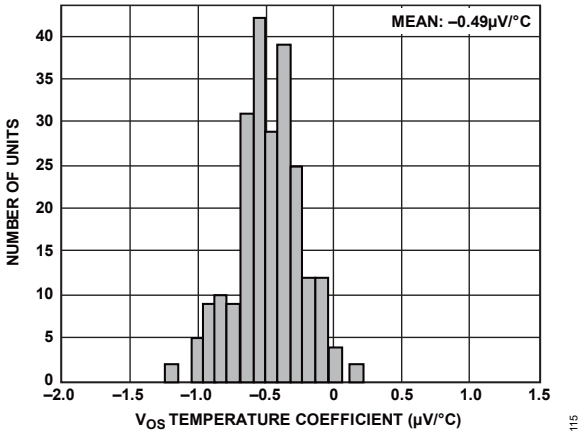

Figure 6. Input Offset Voltage Drift Distribution, T_A = 25°C, V_S = ±110 V, V_{CM} = 0 V, ΔT_J = 60°C, R_{ADJ} = 0 Ω

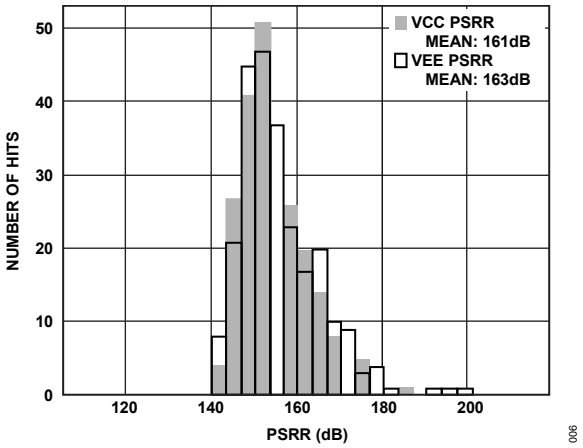

Figure 7. PSRR Distribution, T_A = 25°C, V_S = ±110 V, R_{ADJ} = 0 Ω

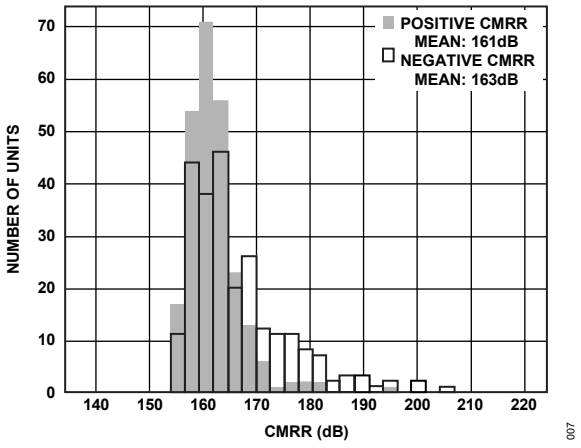

Figure 8. CMRR Distribution, T_A = 25°C, V_S = ±110 V, R_{ADJ} = 0 Ω

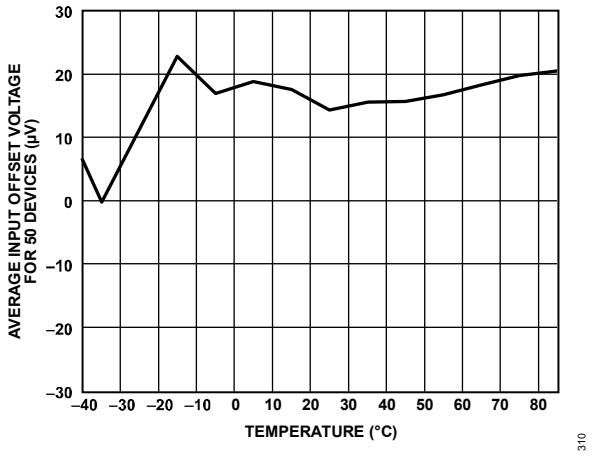

Figure 9. Average Input Offset Voltage for 50 Devices vs. Temperature, V_S = ±110 V

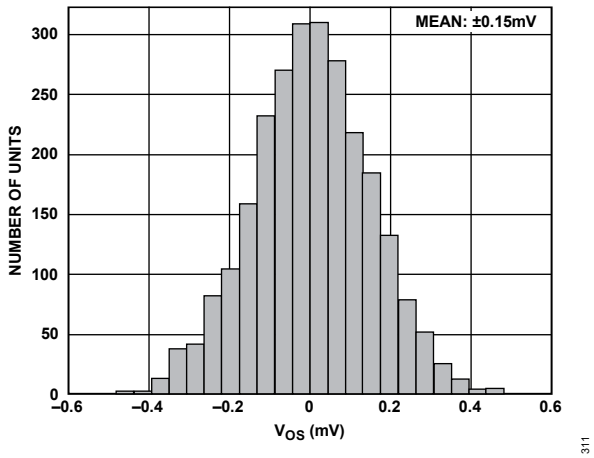

Figure 10. Input Offset Voltage Distribution, T_A = 25°C, V_S = ±110 V, V_{CM} = 0 V, R_{ADJ} = 0 Ω

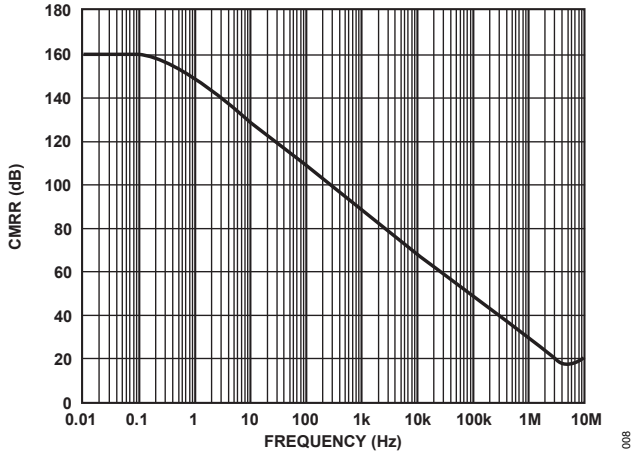

Figure 11. CMRR vs. Frequency, T_A = 25°C, V_S = ±110 V, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

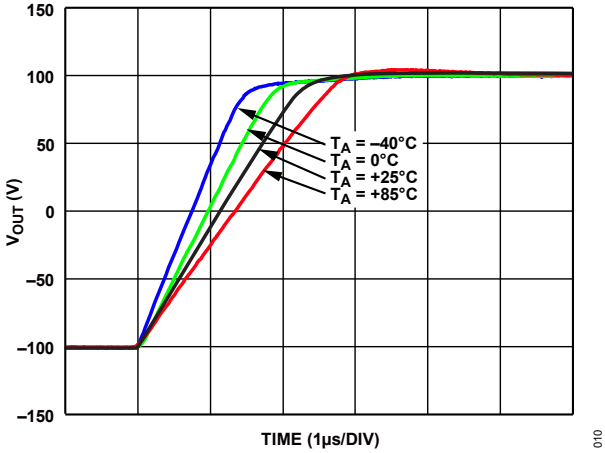

Figure 12. Large Signal Pulse Response at Various T_A, Rising Edge, A_V = 20, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

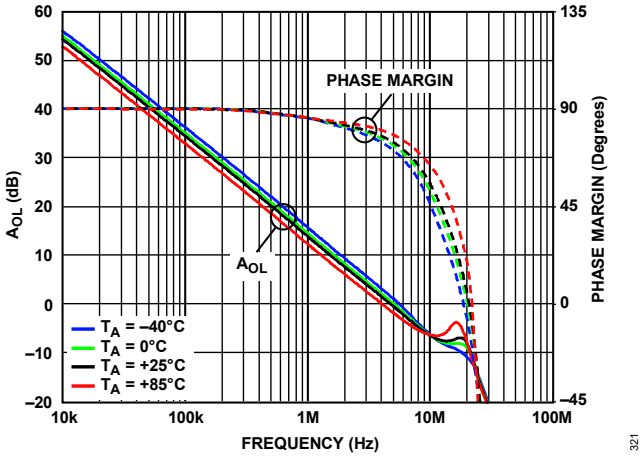

Figure 13. A_{OL} and Phase Margin vs. Frequency at Various T_A, V_S = ±110 V, R_{ADJ} = 0 Ω

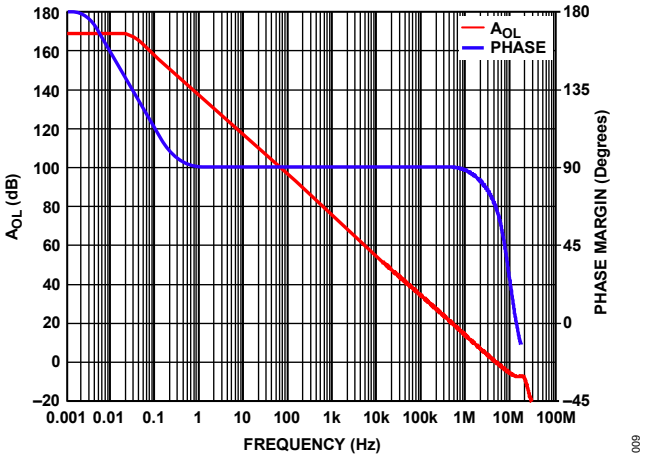

Figure 14. A_{OL} and Phase Margin vs. Frequency, T_A = 25°C, V_S = ±110 V, R_{ADJ} = 0 Ω

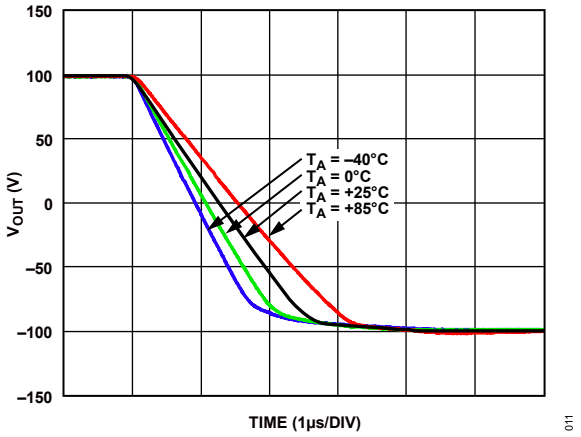

Figure 15. Large Signal Pulse Response at Various T_A, Falling Edge, A_V = 20, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

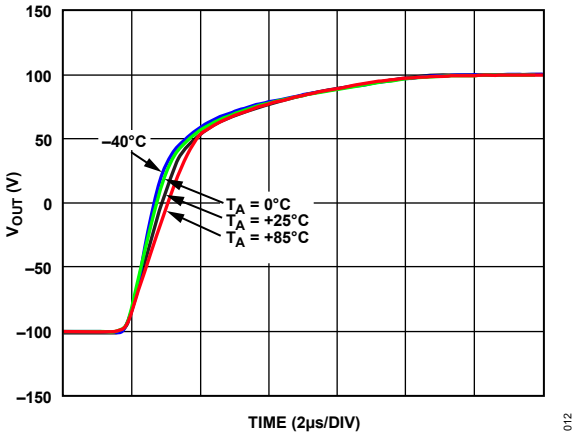

Figure 16. Large Signal Pulse Response at Various T_A, Rising Edge, A_V = 40, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

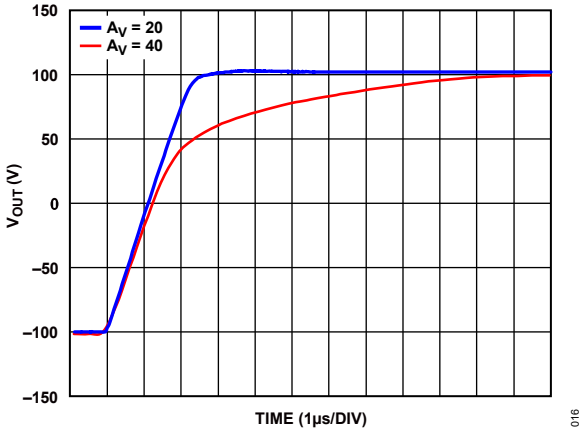

Figure 17. Large Signal Pulse Response at Various Gains, Rising Edge, T_A = 25°C, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

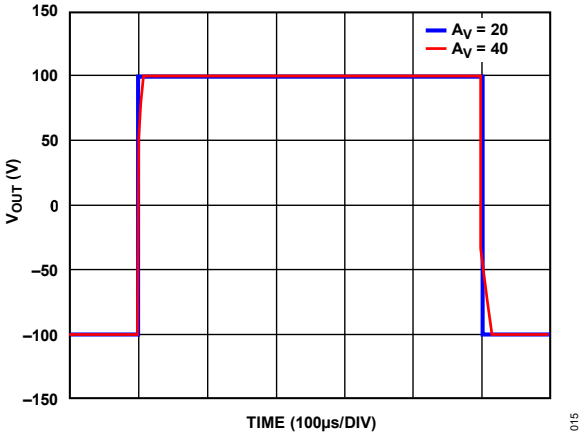

Figure 18. Large Signal Pulse Response at Various Gains, T_A = 25°C, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

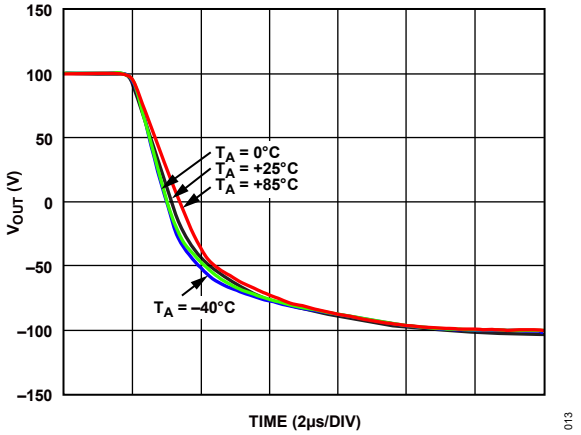

Figure 19. Large Signal Pulse Response at Various T_A, Falling Edge, A_V = 40, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

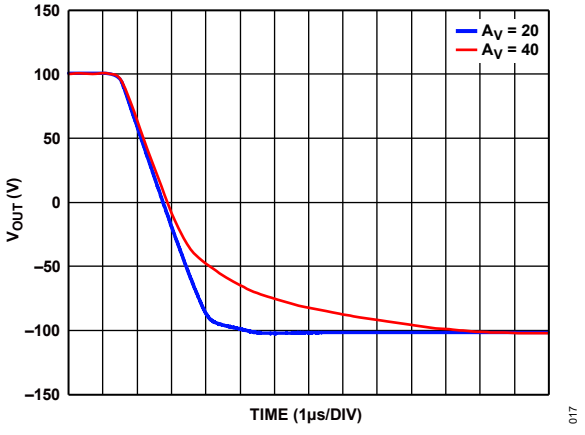

Figure 20. Large Signal Pulse Response at Various Gains, Falling Edge, T_A = 25°C, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

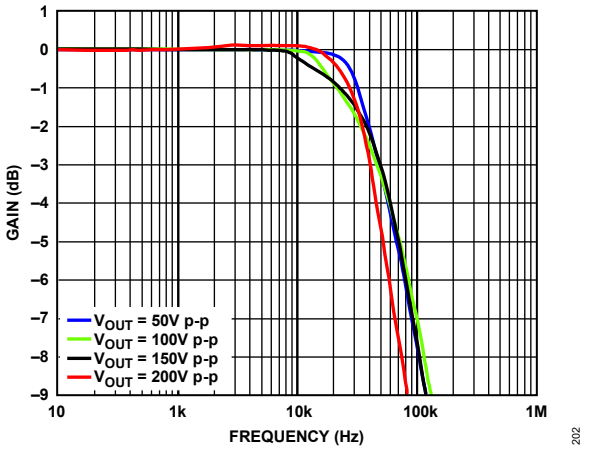

Figure 21. Large Signal Frequency Response at Various Output Swings with Input Clamping Diodes (See Slew Boost Circuit and Protection Section), T_A = 25°C, A_V = 40, V_S = ±110 V, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

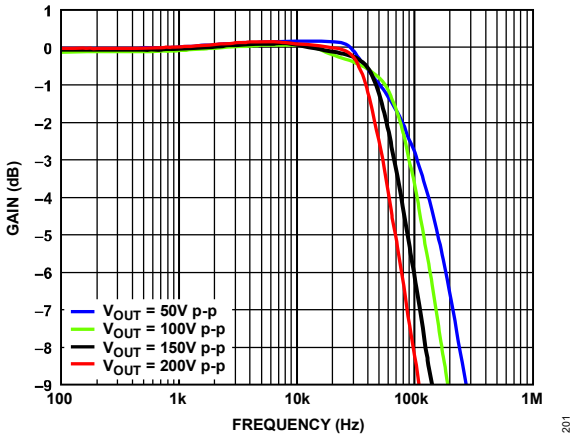

Figure 22. Large Signal Frequency Response at Various Output Swings with Input Clamping Diodes (See the Slew Boost Circuit and Protection Section), T_A = 25°C, A_V = 20, V_S = ±110 V, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

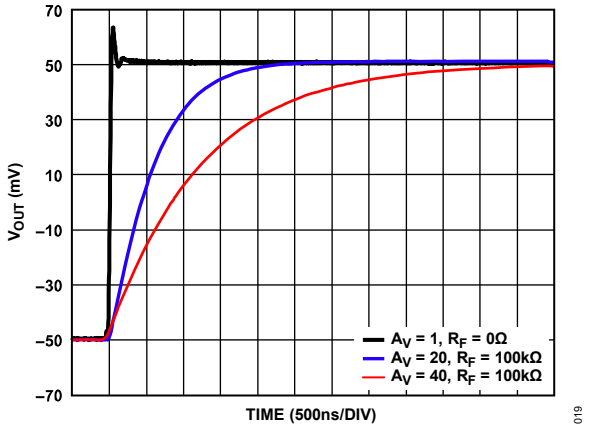

Figure 23. Small Signal Pulse Response at Various Gains, Rising Edge, T_A = 25°C, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

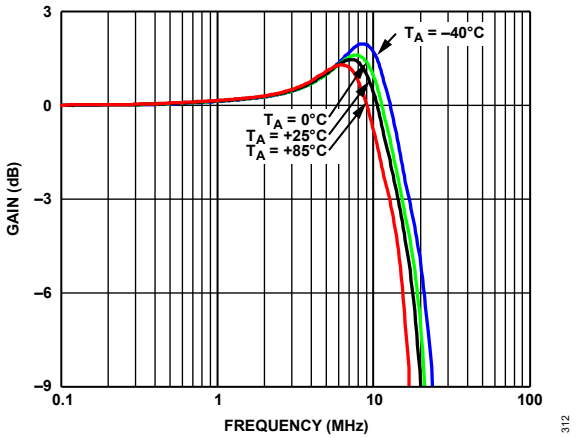

Figure 24. Small Signal Frequency Response at Various T_A, A_V = 1, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_{Load} = 10 kΩ, R_{ADJ} = 0 Ω

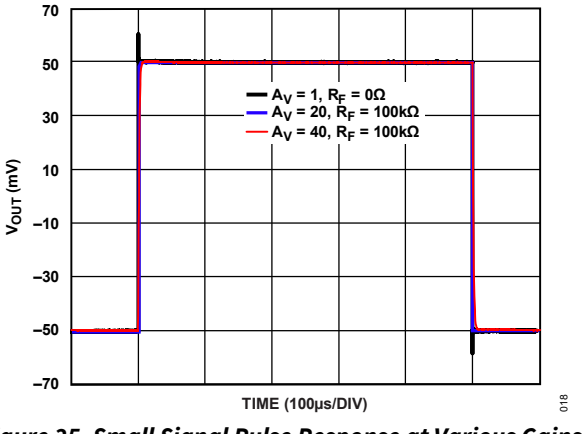

Figure 25. Small Signal Pulse Response at Various Gains, T_A = 25°C, V_S = 110 V, V_{OUT} = 100 mV p-p, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

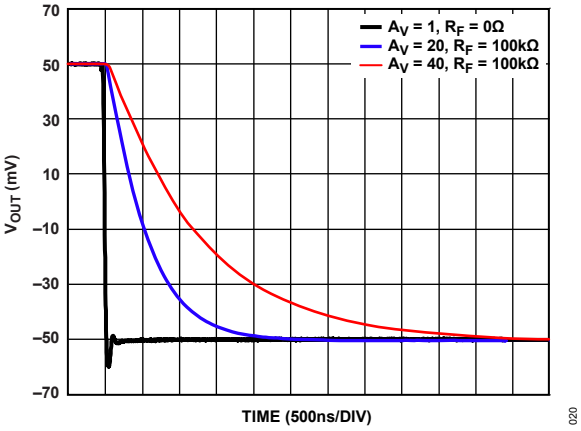

Figure 26. Small Signal Pulse Response at Various Gains, Falling Edge, T_A = 25°C, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

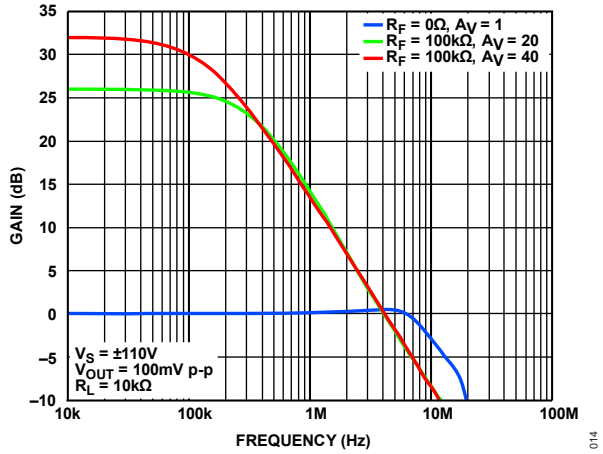

Figure 27. Small Signal Frequency Response at Various Gains, T_A = 25°C, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_L = 10 kΩ, R_{ADJ} = 0 Ω

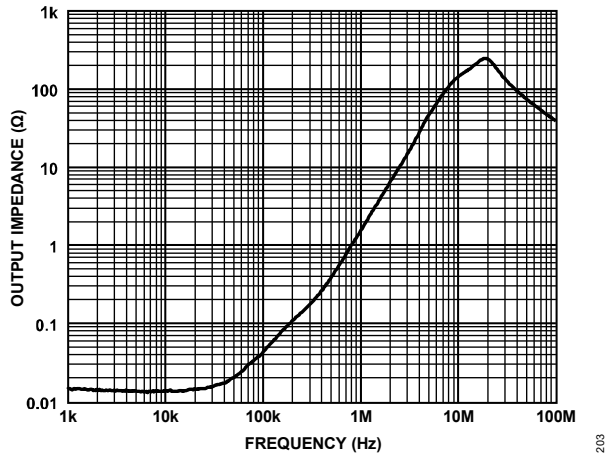

Figure 28. Output Impedance vs. Frequency, T_A = 25°C, A_V = 1, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_F = 0 Ω, R_{ADJ} = 0 Ω

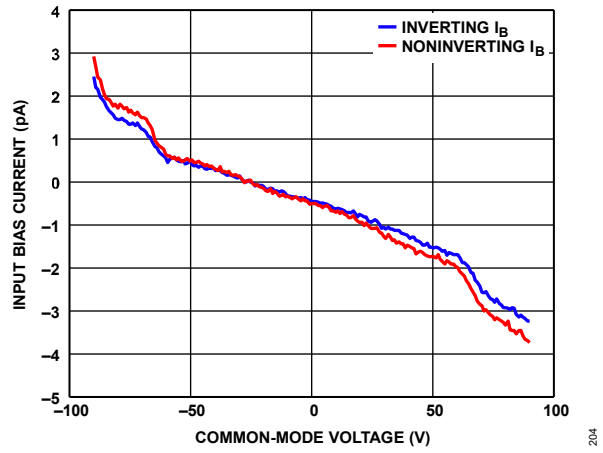

Figure 29. Input Bias Current vs. Common-Mode Voltage, T_A = 25°C, V_S = ±110 V, R_{ADJ} = 0 Ω

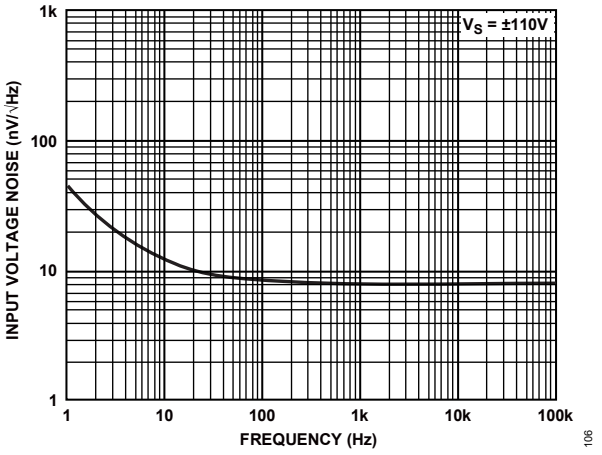

Figure 30. Input Voltage Noise vs. Frequency, T_A = 25°C, V_S = ±110, R_{ADJ} = 0 Ω

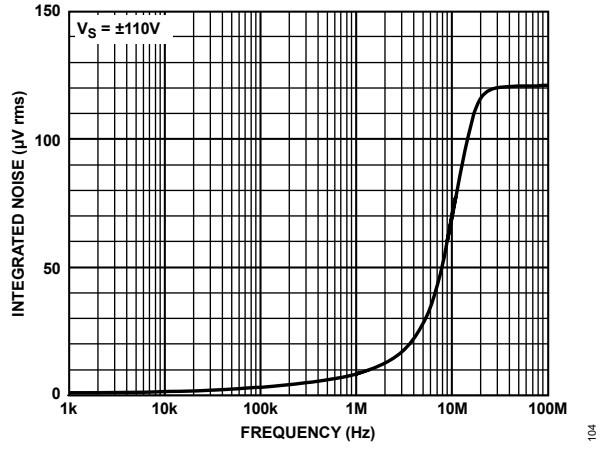

Figure 31. Integrated Noise vs. Frequency, T_A = 25°C, V_S = ±110 V, R_{ADJ} = 0 Ω

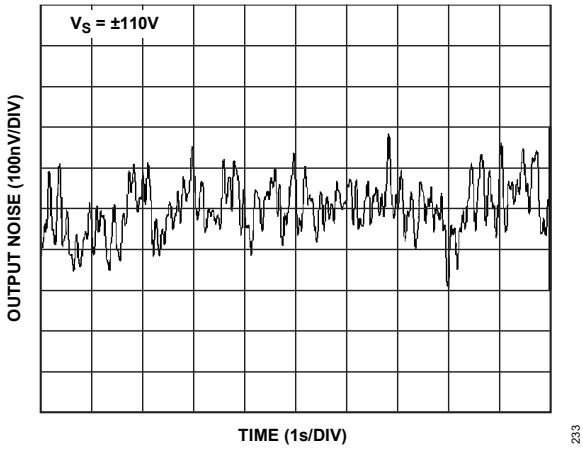

Figure 32. 0.1 Hz to 10 Hz Noise

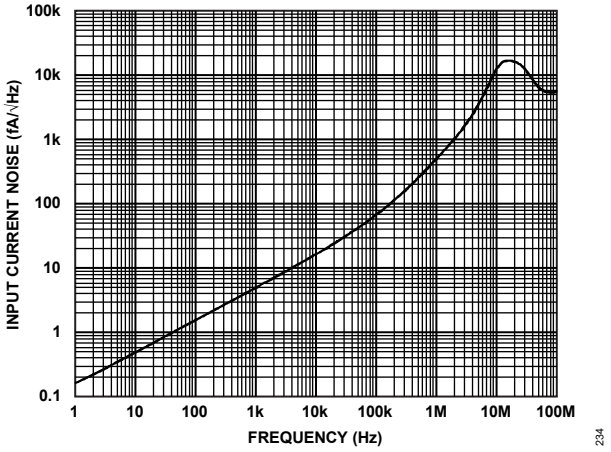

Figure 33. Input Current Noise vs. Frequency

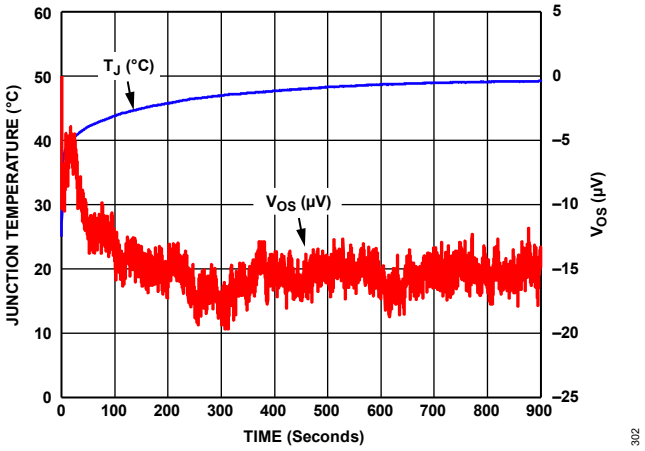

Figure 34. Offset Voltage Warmup Drift and T_J, V_S = ±110, R_{ADJ} = 0 Ω

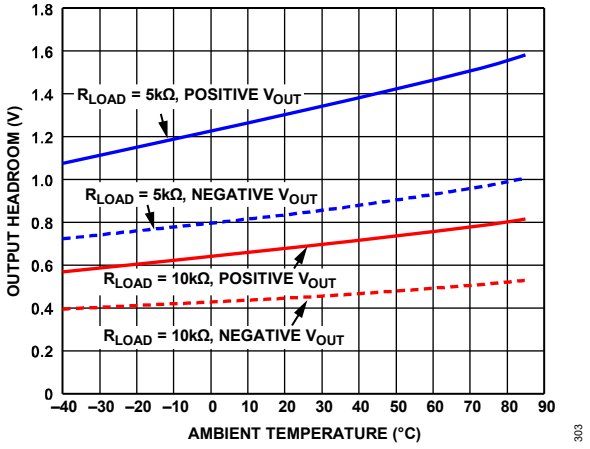

Figure 35. Output Headroom vs. Ambient Temperature at Various R_{LOAD}, V_S = ±110 V, R_{ADJ} = 0 Ω

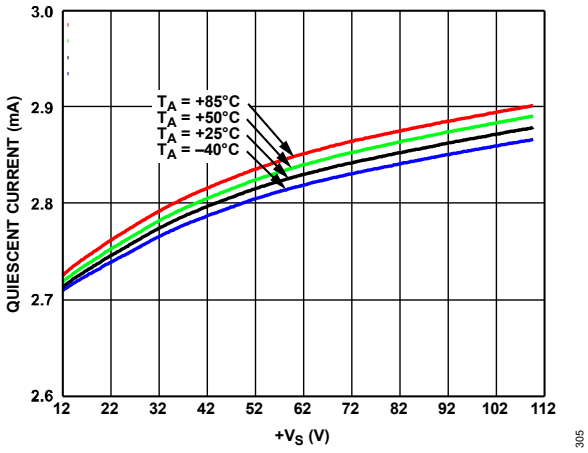

Figure 36. Quiescent Current vs. Positive Supply Voltage at Various T_A, R_{ADJ} = 0 Ω

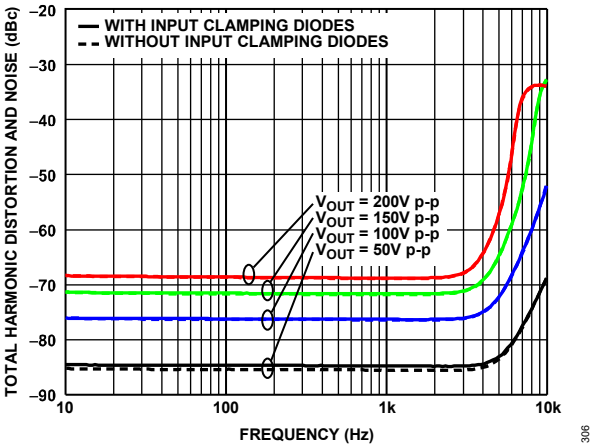

Figure 37. Total Harmonic Distortion and Noise vs. Frequency at Various Large Output Swings, T_A = 25°C, A_V = 20, V_S = ±110 V, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

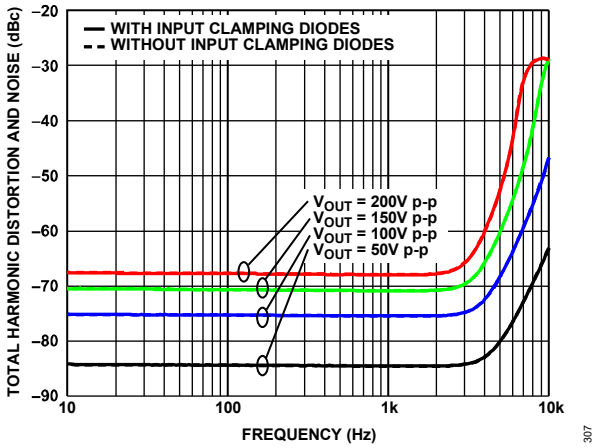

Figure 38. Total Harmonic Distortion and Noise vs. Frequency at Various Large Output Swings, T_A = 25°C, A_V = 40, V_S = ±110 V, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

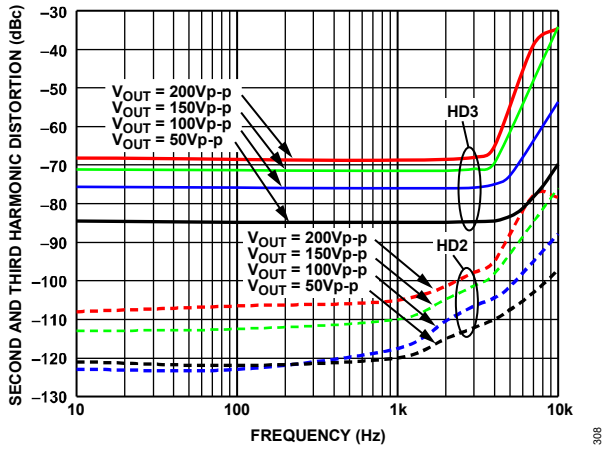

Figure 39. Second Harmonic Distortion (HD2) and Third Harmonic Distortion (HD3) vs. Frequency at Various Output Swings, T_A = 25°C, A_V = 20, V_S = ±110 V, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

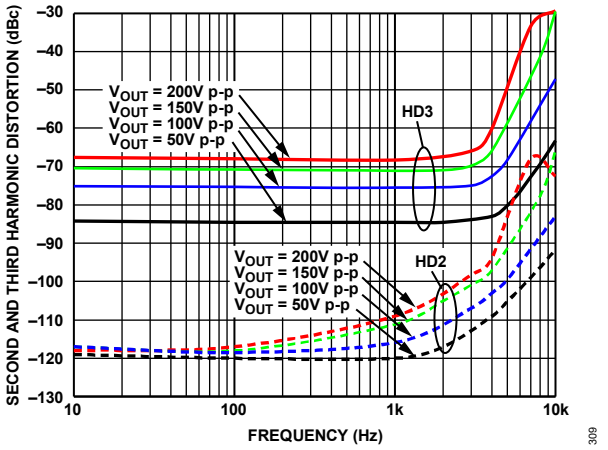

Figure 40. Second Harmonic Distortion (HD2) and Third Harmonic Distortion (HD3) vs. Frequency at Various Output Swings, T_A = 25°C, A_V = 40, V_S = ±110 V, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

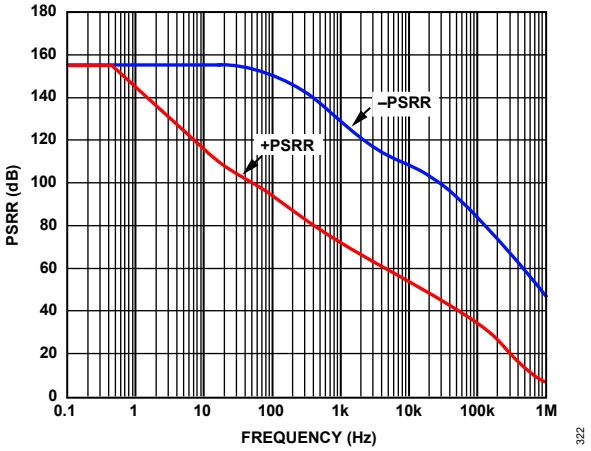

Figure 41. PSRR vs. Frequency, T_A = 25°C, V_S = ±110 V, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

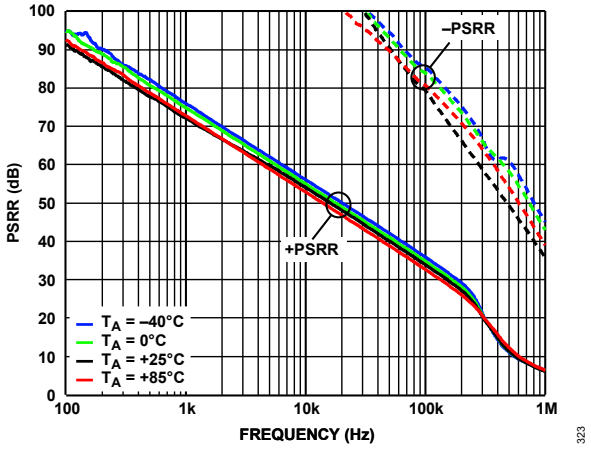

Figure 42. PSRR vs. Frequency at Various T_A, V_S = ±110 V, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

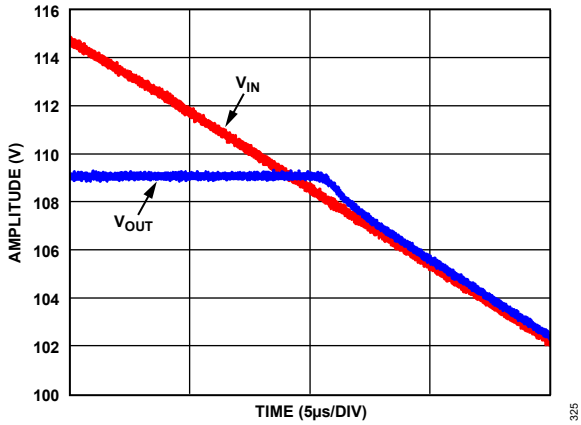

Figure 43. Output Overdrive Recovery, V_S = ±110 V, A_V = 40, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

Theory of Operation

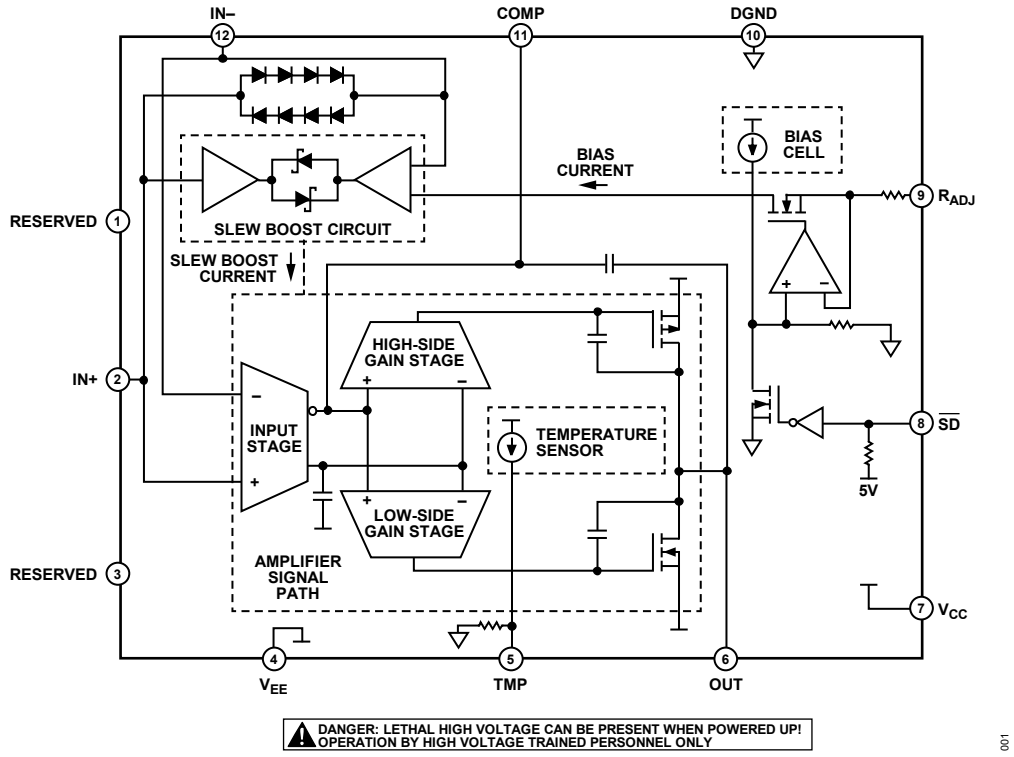

Figure 44. Functional Block Diagram

The ADHV4702-1 is a high voltage (220 V) precision amplifier designed using the next generation of proprietary bipolar/ complementary metal-oxide semiconductor (CMOS)/laterally diffused metal-oxide semiconductor (BCDMOS) process from Analog Devices. *Figure 44* shows the functional block diagram. The input stage architecture offers the advantages of high input impedance with low input bias current, low input offset voltage, low drift, and low noise for precision demanding applications, such as automated test equipment (ATE).

Internal Electrostatic Discharge (ESD) Protection

As shown in *Figure 45*, the ADHV4702-1 has an internal ESD configuration to prevent damage due to overvoltage. The ESD protection circuitry involves current steering diodes connected from the input and output pins to the power supply rails. The ADHV4702-1 also includes internal input clamping diodes across the inverting and noninverting inputs to prevent large differential input voltages from damaging the input stage transistors. This input clamping circuit greatly reduces the input impedance for differential input voltages greater than the forward-biased voltage (V_F) of four diodes.

The ESD protection circuitry remains inactive under normal operation. To avoid forward biasing the ESD diodes, do not overdrive the pin voltages above the absolute maximum ratings, and ensure that the input differential voltage does not exceed 4 V_F. Additional external input clamping diodes may be required to protect the slew boost circuit. See the *Slew Boost Circuit and Protection* section.

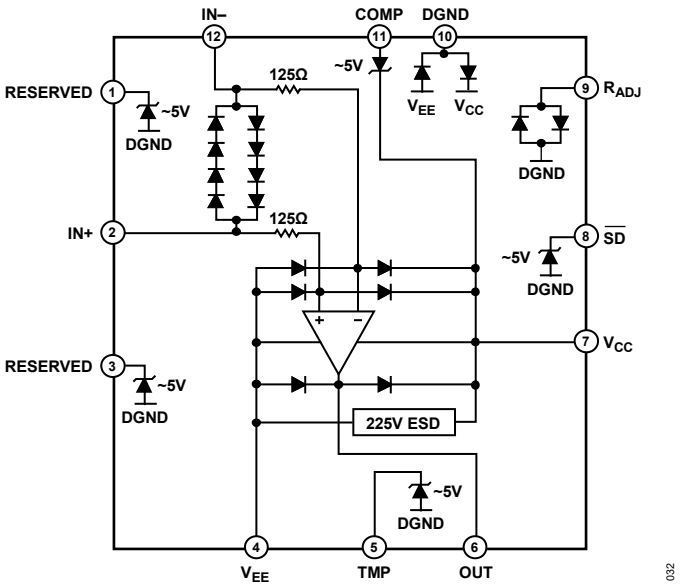

Figure 45. Simplified ESD Configuration

Slew Boost Circuit and Protection

The ADHV4702-1 uses a supplementary slew boosting circuit to achieve its typical slew rate of 74 V/µs across a 200 V p-p output range at unity gain. This slew boosting circuit works by sensing the differential input voltage of the amplifier and converting this voltage into a dynamic current to help drive capacitances within the signal path of the amplifier. With greater input voltage across the inputs, more dynamic current is produced, which enables the amplifier to slew faster. The current produced by the slew boosting circuit transmits to all stages of the amplifier during slewing.

Internally, the ADHV4702-1 contains differential input voltage clamps that limit transient differential signals to 4 V_F, placing an upper limit on the slew boost. Large differential input voltages (which can occur with signal frequencies approaching the full power bandwidth) trigger the slew boosting circuit, resulting in an increased dynamic supply current. The relationship between slew rate and full power bandwidth (f_M) is given in the following equation:

$$SR = V_O \times 2\pi f_M$$

where V_O is the peak output voltage.

When operating continuously at or near full power bandwidth, the increased supply current may cause an increase in T_J beyond the safe operating temperature, resulting in device damage. The dynamic safe operating area (SOA) for the *EVAL-ADHV4702-1CPZ* evaluation board is shown in *Figure 61* in the *Safe Operating Area* section. The dynamic SOA shows the connection between the output swing and the maximum input/output frequency for pulse response. To expand the SOA curve, use additional thermal management or limit the differential voltage across the inputs to 2 V_F with external diodes, which limits the current produced by the slew boosting circuit and reduces the internal power dissipation. Clamping the differential input voltage of the ADHV4702-1 in this way protects the amplifier in dynamic operation but limits slew rate and large signal bandwidth. *Figure 46* shows a simplified schematic with external input clamping diodes, and *Figure 47* to *Figure 50* show the large signal pulse response at various temperatures and gains while the ADHV4702-1 inputs are clamped by two ON Semiconductor SBAV199LT1G diode pairs at 2 V_F.

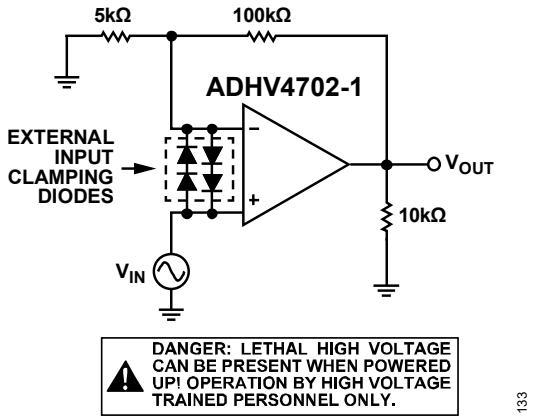

Figure 46. External Input Clamping Diodes Schematic

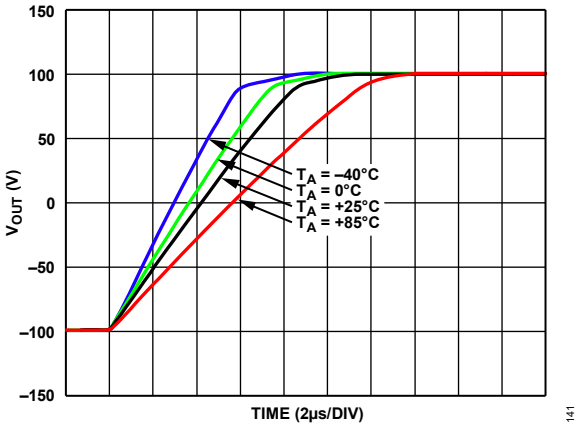

Figure 47. Large Signal Pulse Response at Various T_A with Two-Diode Forward Voltages, Rising Edge, A_V = 20, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

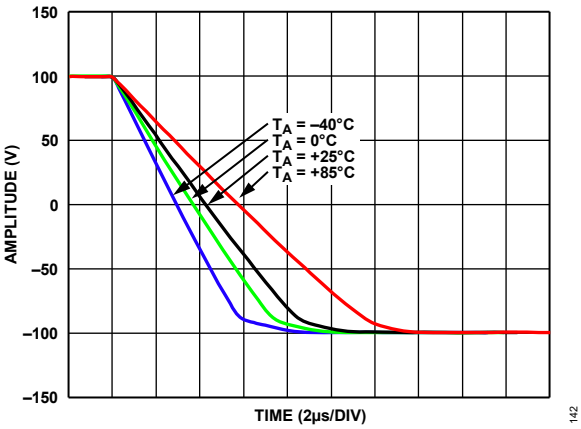

Figure 48. Large Signal Pulse Response at Various T_A with Two-Diode Forward Voltages, Falling Edge, A_V = 20, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

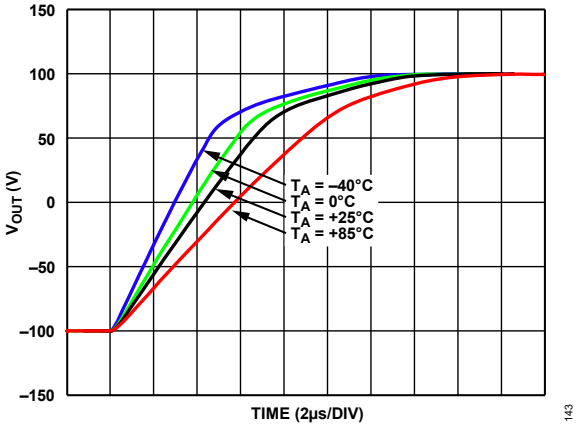

Figure 49. Large Signal Pulse Response at Various T_A with Two-Diode Forward Voltages, Rising Edge, A_V = 40, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

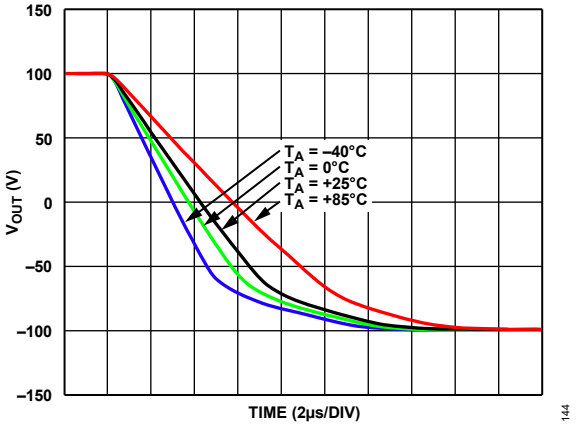

Figure 50. Large Signal Pulse Response at Various T_A with Two-Diode Forward Voltages, Falling Edge, A_V = 40, V_S = ±110 V, V_{OUT} = 200 V p-p, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

Digital Ground (DGND)

DGND is the reference for all low voltage pins of the amplifier (R_{ADJ}, TMP, and $\overline{SD}$) and serves as a signal ground for communication to a microprocessor or other low voltage logic circuit. Connect DGND to a 0 V digital ground or analog ground. Do not float DGND.

Resistor Adjustable Quiescent Current (RADJ)

To reduce further power consumption, the quiescent current of the ADHV4702-1 can be adjusted by placing a resistor (R_{ADJ}) between the R_{ADJ} pin and DGND.

To fully bias the amplifier, short the R_{ADJ} pin directly to DGND to allow maximum dynamic performance. To bias the amplifier with minimum quiescent power consumption, place a 100 kΩ resistor from R_{ADJ} to DGND. This resistor reduces quiescent supply current to approximately 0.6 mA. Operating the amplifier at a lower quiescent current has minimal effect on DC performance but can result in an associated reduction in dynamic performance, such as bandwidth and noise. *Figure 51* and *Figure 52* show the small signal frequency response and noise performance at various R_{ADJ} values.

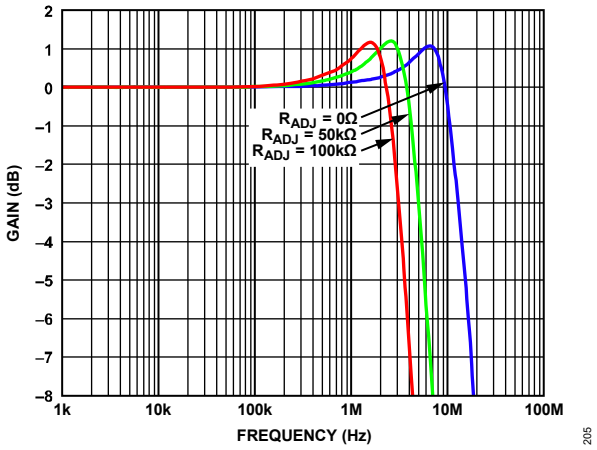

Figure 51. Small Signal Frequency Response at Various R_{ADJ}, T_A = 25°C, A_V = 1, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_F = 0 Ω, R_{LOAD} = 10 kΩ

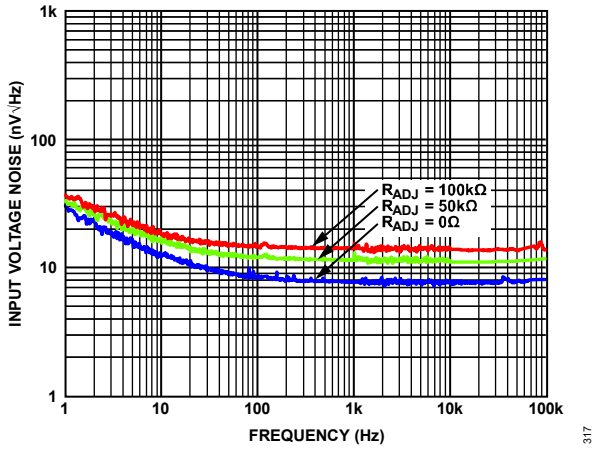

Figure 52. Input Voltage Noise at Various R_{ADJ}, T_A = 25°C, V_S = ±110 V

Shutdown Pin ($\overline{SD}$)

The ADHV4702-1 is equipped with a power saving shutdown feature. When the $\overline{SD}$ pin voltage is brought low to within 0.8 V of DGND, the amplifier is disabled and put in a low power state, reducing its quiescent current to approximately 0.18 mA. The $\overline{SD}$ pin has an internal approximately 400 kΩ pull-up resistor that enables the amplifier if SD is left floating. When turning the amplifier on from the shutdown state, pull the $\overline{SD}$ pin high to at least 1.6 V above the DGND pin. The $\overline{SD}$ pin response time for starting up and coming out of shutdown is shown in *Figure 53* and *Figure 54*. The $\overline{SD}$ pin can support digital logic levels down to 2.5 V. The $\overline{SD}$ pin can be used to implement thermal shutdown and short-circuit protection when used in conjunction with the temperature monitor feature of the ADHV4702-1.

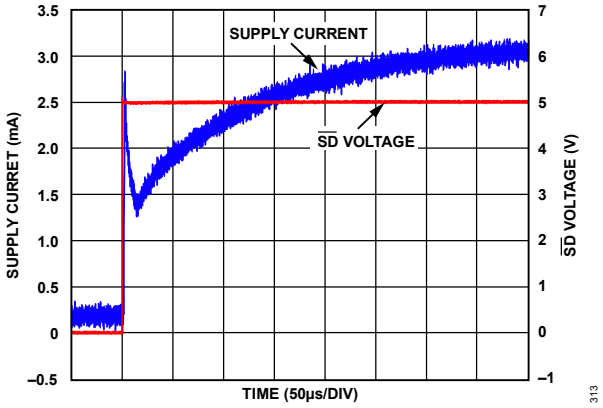

Figure 53. $\overline{SD}$ Pin Response Time, Turning On

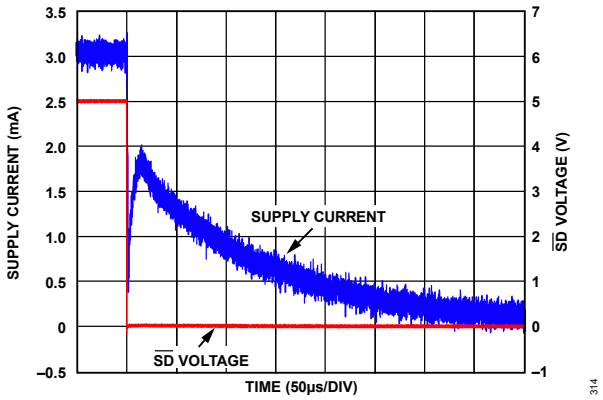

Figure 54. $\overline{SD}$ Pin Response Time, Turning Off

Temperature Monitor (TMP)

The ADHV4702-1 features an on-chip temperature sensor in close proximity to the output stage, where die temperature is the highest. The output voltage of the temperature sensor appears at the TMP pin. As an approximate indicator of die temperature, TMP voltage can be used to monitor power dissipation and implement thermal shutdown. The TMP voltage at room temperature is nominally 1.9 V, changing at approximately −4.5 mV/°C, as shown in *Figure 55*. More precise temperature readings can be achieved through a one-time room temperature calibration of the TMP pin.

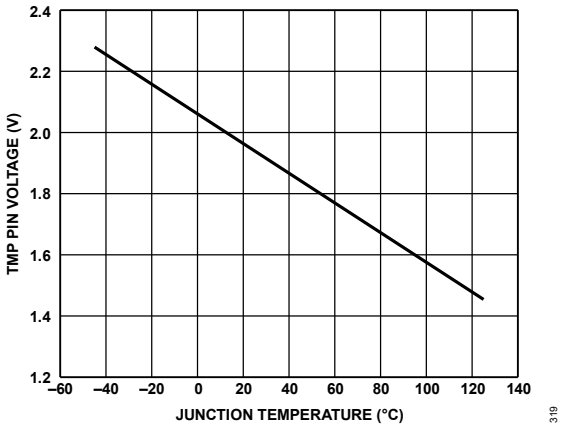

Figure 55. TMP Pin Voltage vs. Junction Temperature

Overtemperature Protection

Operation at or beyond the operating temperature specified in the *Absolute Maximum Ratings* section can affect product reliability. To minimize this risk, the ADHV4702-1 features an optional, resistor programmable thermal shutdown where the TMP pin voltage asserts the $\overline{SD}$ pin. In addition to proper heat sinking, thermal shutdown is recommended to protect the amplifier from an overtemperature condition. To implement the thermal shutdown function, tie TMP to $\overline{SD}$, as shown in *Figure 56*, and connect a 200 kΩ resistor (R_{TMP}) from TMP and $\overline{SD}$ to DGND in close proximity to the ADHV4702-1.

Device to device variation in the TMP pin voltage may result in different shutdown threshold temperatures or shutdown response times among various devices while implementing the 200 kΩ R_{TMP}. The shutdown threshold can be adjusted with a smaller R_{TMP} resistance, yielding a lower threshold temperature.

The R_{TMP} together with the internal resistors of TMP form a voltage divider that influences the TMP pin reading and TMP voltage drift. The TMP data in *Table 1* and the *Temperature Monitor (TMP)* section is only valid when R_{TMP} is uninstalled.

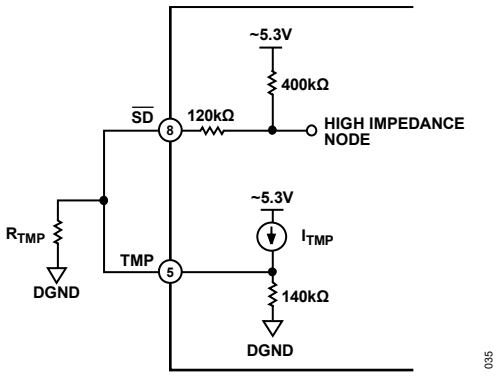

Figure 56. TMP and SD Pin Configuration for Short-Circuit Protection and Thermal Shutdown

Output Current Drive and Short Circuit Protection

The ADHV4702-1 uses an output stage constructed with cascaded, double diffused, metal-oxide-semiconductor (DMOS) high voltage transistors that provide wide output swing. The ADHV4702-1 can typically drive a 20 mA load current continuously. Though with proper thermal management, the ADHV4702-1 can deliver up to 50 mA. Short-circuit protection is provided by means of the thermal shutdown feature. To enable short-circuit protection, connect the $\overline{SD}$ and TMP pins, and tie both to DGND with a 200 kΩ R_{TMP}.

External Compensation and Capacitive Load (C_{LOAD}) Driving

When driving a C_{LOAD}, the amplifier output resistance and the load capacitance form a pole in the transfer function of the amplifier. This additional pole reduces phase margin at higher frequencies and, if left uncompensated, can result in excessive peaking and instability. Placing a series resistor (R_S) between the amplifier output and C_{LOAD} (as shown in *Figure 57*) allows the ADHV4702-1 to drive capacitive loads beyond 1 µF. *Figure 58* shows the series resistor value vs. load capacitance for a maximum of 2 dB peaking in the circuit of *Figure 57*.

In addition to the series resistor, the ADHV4702-1 includes an optional external compensation feature for driving capacitive loads. A capacitor (C_{COMP}) can be installed between COMP and OUT to reduce output stage peaking associated with capacitive loads. C_{COMP} must be rated for the full supply differential. *Figure 60* shows the effect of C_{COMP} on various capacitive loads.

The values shown in *Figure 58*, *Figure 59*, and *Figure 60* are for unity gain configuration with a purely C_{LOAD}. This is a worst case scenario because the amplifier is more stable at higher gains and with some resistive load in parallel with the load capacitance. Although the R_S or C_{COMP} significantly increases the stability while driving C_{LOAD}, they also reduce the headroom and bandwidth while driving a resistive load. For resistive loads, leave the COMP pin floating.

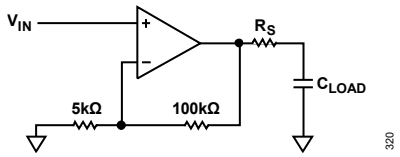

Figure 57. Circuit for C_{LOAD} Drive

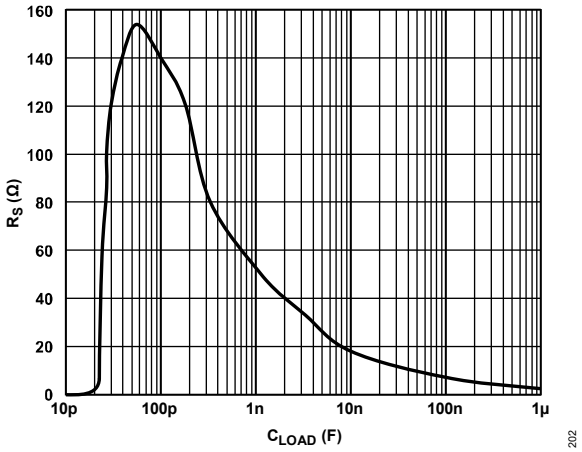

Figure 58. R_S vs. C_{LOAD} for Maximum 2 dB Peaking for Circuit from Figure 57, T_A = 25°C, A_V = 1, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_F = 0 Ω, R_{ADJ} = 0 Ω

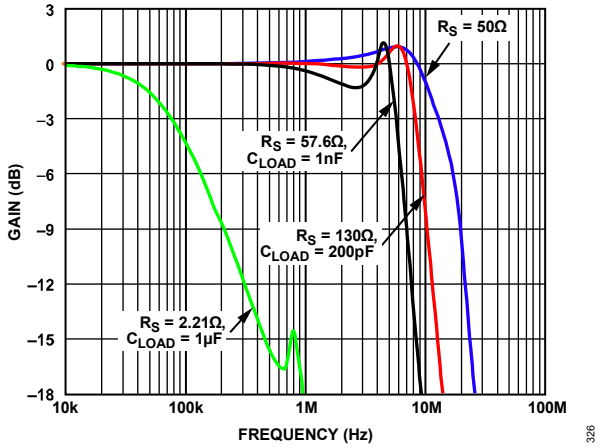

Figure 59. Small Signal Response for Various C_{LOAD} and R_S Values, T_A = 25°C, A_V = 1, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_F = 0 Ω, R_{ADJ} = 0 Ω

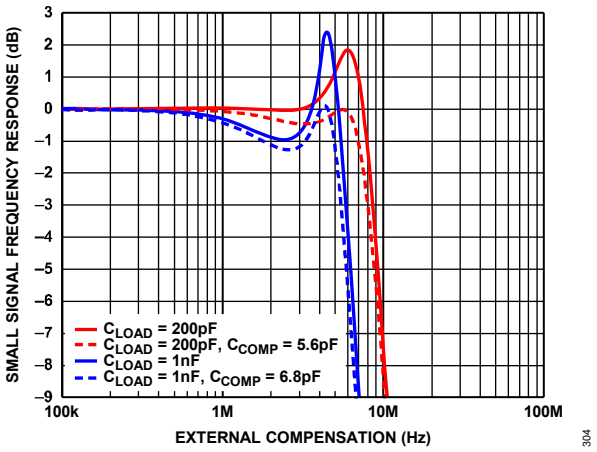

Figure 60. Small Signal Frequency Response vs. External Compensation, T_A = 25°C, A_V = 1, V_S = ±110 V, V_{OUT} = 100 mV p-p, R_F = 0 Ω, R_{ADJ} = 0 Ω

Safe Operating Area

The SOA represents the power handling capability of the device under various conditions.

The power dissipation of the ADHV4702-1 occurs primarily from the slew boosting circuit and output stage. The slew boosting circuit requires additional supply current. Operating the amplifier at its maximum slew rate at larger swing or at a high frequency increases the current consumption of the slew boosting circuit, increasing the T_J. *Figure 61* shows the dynamic SOA that maintains a T_J less than 150°C. The curve shows the maximum safe square wave frequency for a given amplitude. Operating the ADHV4702-1 outside of the boundaries can cause permanent damage. Using additional thermal management or input clamping diodes expands the dynamic SOA significantly. However, using input clamping diodes can compromise the slew rate and the large signal bandwidth.

The DC SOA is a curve of output current vs. the voltage across the output stage, which is the voltage difference between supply and output ($V_S - V_{OUT}$) under which the amplifier can operate at a safe T_J . The areas under the curves of *Figure 62* show the operational boundaries of the ADHV4702-1 that maintain a $T_J \leq 150°C$.

The SOA curves are unique to the conditions under which they were developed, such as PCB, heat sink, and T_A. All testing was performed in a still air environment. Forced air convection in any of the test cases effectively lowers θ_{JA} and expands the SOA.

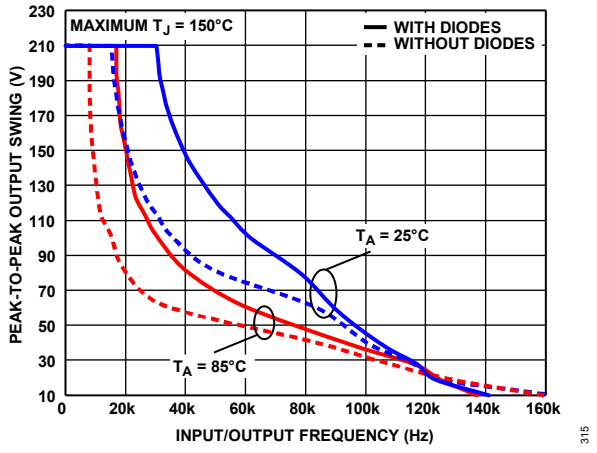

Figure 61. Dynamic SOA at T_A = 25°C and T_A = 85°C With and Without Input Clamping Diodes, A_V = 20, V_S = ±110 V, R_F = 100 kΩ, R_{LOAD} = 10 kΩ, R_{ADJ} = 0 Ω

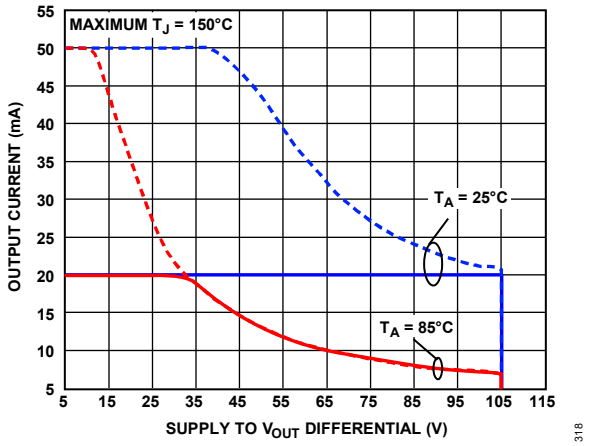

Figure 62. DC SOA at T_A = 25°C and T_A = 85°C, A_V = 20, V_S = ±110 V, R_F = 100 kΩ, R_{ADJ} = 0 Ω

LFCSP Package and High Voltage Pin Spacing

A 7 mm × 7 mm, 12-lead LFCSP with EPAD was selected for the ADHV4702-1 to provide high reliability and compliance to regional and global high voltage standards regarding dielectric withstanding (clearance) and carbonization of package surface (creepage). The package dimensions are shown in *Outline Dimensions*. The ADHV4702-1 meets the minimum 1.25 mm spacing requirement of IEC Standard 61010-1 for creepage distance to preclude failure due to carbon tracking at 250 V rms. To maintain these protections, it is essential to remove all flux and soldering residue around the package pins and exposed pad. Refer to the IEC 61010-1 standard for additional information.

Exposed Pad (EPAD)

The copper EPAD of the LFCSP provides a thermally conductive path to the PCB, which can be attached to a heat sink to improve heat dissipation. There is no internal electrical connection to the EPAD. High voltage isolation allows the EPAD to be safely biased to a 0 V ground plane, regardless of V_{CC} or V_{EE} voltages.

Applications Information

Power Supply and Decoupling

The ADHV4702-1 can operate from a single supply or dual supply. The ADHV4702-1 requires a minimum supply voltage (V_{CC} - V_{EE}) of 24 V. Single supply of ADHV4702-1 is V_{EE} = DGND, V_{CC} = 24 V and ±12 V for dual supplies. Decouple each supply pin to ground using high quality, low effective series resistance (ESR), 0.1 µF capacitors. Place decoupling capacitors as close to the supply pins as possible. Additionally, place 1.2 µF tantalum capacitors from each supply to ground to provide sufficient low frequency decoupling and supply the needed current to support large, fast slewing signals at the ADHV4702-1 output. To ensure reliable operation under high voltages, the voltage ratings for the bypass capacitors must be higher than the supply voltages of the ADHV4702-1.

High Voltage Guard Ring

The ADHV4702-1 features a pin placement that facilitates the use of a guard ring around the noninverting input of the amplifier. Guarding minimizes leakage from nearby pins and helps to achieve the benefit of low input bias current. The guard must be free of solder mask so that it remains exposed on the surface of the PCB. Drive the guard ring to a potential that tracks the input of the amplifier.

High Voltage DAC Voltage Subtractor

The ADHV4702-1 can be combined with a dual, 16-bit voltage output, DAC, such as the *AD5752R*, to produce a versatile high voltage DAC solution. For this configuration, set up the ADHV4702-1 as a voltage subtractor with a gain of 20, which is ideally suited for chemical analysis (mass spectrometry), piezodrive, scanning electron microscope (SEM), LiDAR APD/SPAD, and silicon photomultiplier bias control applications.

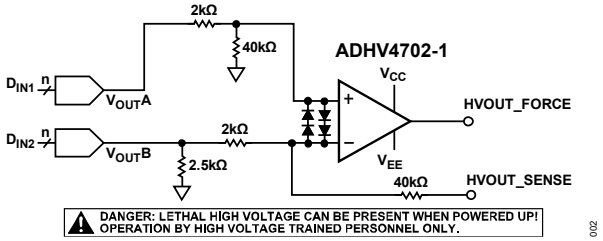

Figure 63. ADHV4702-1 Configured as a Voltage Subtractor Using DACs

High Current Output Driver

Figure 64 shows a system level application of the ADHV4702-1 that boosts the output current drive of the amplifier. By introducing a discrete unity-gain output stage, the ADHV4702-1 can be used as a high power output driver retaining the precision performance capabilities of the standalone amplifier, such as offset, drift, open-loop gain, and CMRR, while increasing the output current drive up to the current handling capabilities of the discrete devices.

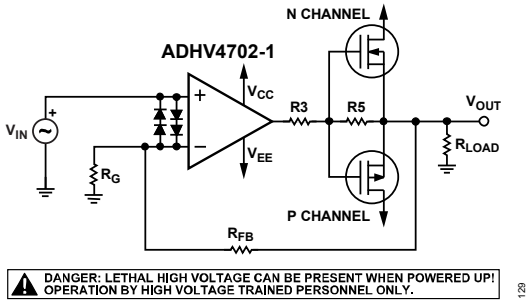

Figure 64. High Current Output Driver Schematic

Signal Range Extender

Figure 65 shows an example of a signal range extender configuration. By introducing two additional high power, discrete, metal-oxide semiconductor field effect transistors (MOSFETs), the range extender can deliver at least twice the signal range (depending on the MOSFET selection), while retaining the original performance characteristics of the amplifier.

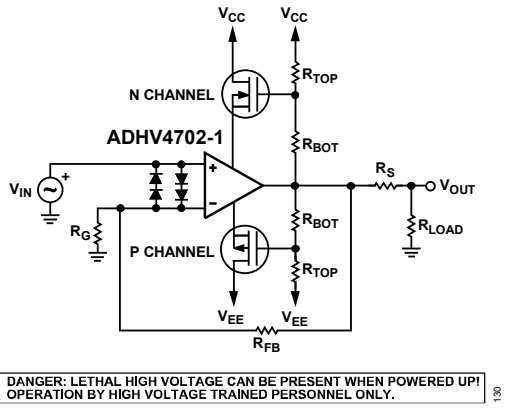

Figure 65. Voltage Extender Schematic

Asymmetrical Power Supplies Operation

If an application requires asymmetrical power supplies operation of the ADHV4702-1, certain boundary conditions, respective to each power supply, is observed for accurate and reliable operation. *Table 6* details some typical asymmetrical power supply cases. Input common-mode voltage range and output voltage swing limits are observed as shown in *Table 6*. Due to the higher gains needed for a high voltage use case, the input common-mode voltage range is usually not the limitation but always check the final application. The cases shown in *Table 6* use the 20 mA load current for the output voltage range given in *Table 1*. *Figure 66* shows a typical simulation schematic for an asymmetrical supplies operation with V_{CC} = 48 V and V_{EE} = −172 V. Note that in *Figure 67*, the performance aligns with that of *Table 6*. The schematic shown in *Figure 66* is simulated using *LTspice®*, which allows the user to easily check a circuit response through simulation

Table 6. Typical Asymmetrical Supplies Operation Cases

V_{CC} (V)	V_{EE} (V)	+ ICMV (V)	- ICMV(V)	Output High (V)	Output Low (V)	Boundary Comments
+12	-175	+9	-172	+10	-173	V_{CC} (min): +12 V V_{EE} (min): −175 V
+48	-172	+45	-169	+46	-170	V_{CC} to V_{EE}: 220 V
+175	-5	+172	-2	+173	-3	V_{CC} (max): 175 V
175	0	172	3	173	2	V_{CC} (max): 175 V

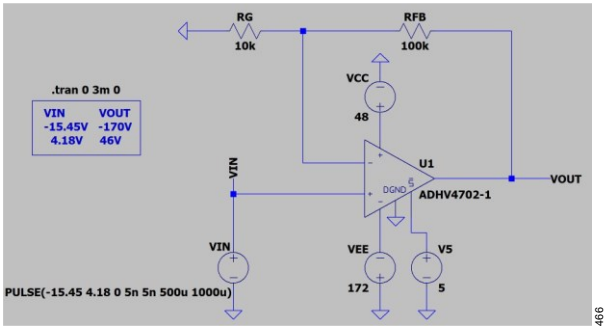

Figure 66. Typical Asymmetrical Supplies Operation Simulation

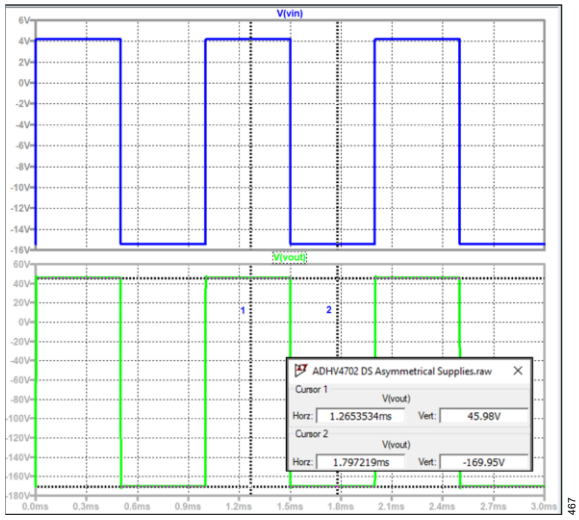

Figure 67. Typical Asymmetrical Supplies Operation Simulation Results

DGND Level Modification

For applications that require a positive asymmetrical supply for ADHV4702-1 but exceed the maximum allowable supply voltage, a workaround of shifting the level of DGND can be applied. The modification complies with the allowed range for positive asymmetric supply due to level shifting of the DGND. *Figure 68* shows the typical configuration for this setup, which requires a Zener diode, a resistor, and a capacitor. The Zener diode establishes a stable, level-shifted DGND voltage. Additionally, the modification includes an external circuit example for pins associated with the DGND level. In *Figure 68*, the SD pin is controlled by an external circuit composed of a switching element, a resistor, and an added Schottky diode for robustness and protection of the device. This circuit enables users to fully utilize the shutdown functionality of the ADHV4702-1.

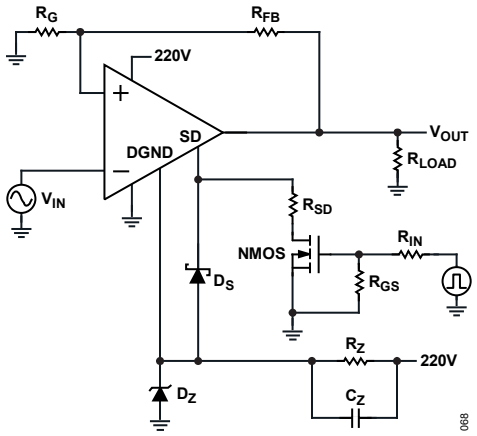

Figure 68. DGND Level Modification Circuit

Outline Dimensions

Package Drawing (Option)	Package Type	Package Description
CP-12-8	LFCSP	12-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to *Package Index*.

Ordering Guide

Table 7. Ordering Guide

Model	Temperature Range	Package Description	Packing Quantity	Package Option
ADHV4702-1BCPZ [1]	-40°C to +85°C	12-Lead LFCSP (7mm x 7mm x 0.75mm w/ EP)		CP-12-8
ADHV4702-1BCPZ-R7 [1]	-40°C to +85°C	12-Lead LFCSP (7mm x 7mm x 0.75mm w/ EP)	Reel, 750	CP-12-8

[1] Z = RoHS Compliant Part.

Evaluation Boards

Table 8. Evaluation Board

Model	Description
EVAL-ADHV4702-1CPZ [1]	Evaluation Board

[1] Z = RoHS Compliant Part.