Data Sheet

ADE9000

High Performance, Multiphase Energy, and Power Quality Monitoring IC

FEATURES

- 7 high performance ADCs
  - 101 dB SNR
  - Wide input voltage range: ±1 V, 707 mV rms FS at gain = 1
  - Differential inputs
- ±25 ppm/°C maximum channel drift (including ADC, internal VREF, PGA drift) enabling 10000:1 dynamic input range Class 0.2 metrology with standard external components
- Power quality measurements
  - Enables implementation of IEC 61000-4-30[1]
  - VRMS ½, IRMS ½ rms voltage refreshed each half cycle
  - 10 cycle rms/12 cycle rms
  - Dip and swell monitors
  - Line frequency—one per phase
  - Zero crossing, zero-crossing timeout
  - Phase angle measurements
- Supports CTs and Rogowski coil (di/dt) sensors
  - Multiple range phase/gain compensation for CTs
  - Digital integrator for Rogowski coils
- Flexible waveform buffer
  - Able to resample waveform to ensure 128 points per line cycle for ease of external harmonic analysis
  - Events, such as dip and swell, can trigger waveform storage
  - Simplifies data collection for IEC 61000-4-7 harmonic analysis
- Advanced metrology feature set
  - Total and fundamental active power, volt amperes reactive (VAR), volt amperes (VA), watthour, VAR hour, and VA hour
  - Total and fundamental IRMS, VRMS
  - Total harmonic distortion
  - Power factor
  - Supports active energy standards: IEC 62053-21 and IEC 62053-22; EN50470-3; OIML R46; and ANSI C12.20
  - Supports reactive energy standards: IEC 62053-23, IEC 62053-24
- High speed communication port: 20 MHz serial port interface (SPI)
- Integrated temperature sensor with 12-bit successive approximation register (SAR) ADC
  - ±3°C accuracy from −40°C to +85°C

APPLICATIONS

- Energy and power monitoring
- Power quality monitoring
- Protective devices
- Machine health
- Smart power distribution units
- Polyphase energy meters

[1] For IEC 61000-4-30 Class S implementation, refer to the ADE9430 IC data sheet.

Rev. B

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REVISION HISTORY

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1/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADE9000[2] is a highly accurate, fully integrated, multiphase energy and power quality monitoring device. Superior analog performance and a digital signal processing (DSP) core enable accurate energy monitoring over a wide dynamic range. An integrated high end reference ensures low drift over temperature with a combined drift of less than ±25 ppm/°C maximum for the entire channel including a programmable gain amplifier (PGA) and an analog-to-digital converter (ADC).

The ADE9000 offers complete power monitoring capability by providing total as well as fundamental measurements on rms, active, reactive, and apparent powers and energies. Advanced features such as dip and swell monitoring, frequency, phase angle, voltage total harmonic distortion (VTHD), current total harmonic distortion (ITHD), and power factor measurements enable implementation of power quality measurements. The ½ cycle rms and 10 cycle rms/12 cycle rms, calculated according to IEC 61000-4-30, provide instantaneous rms measurements for real-time monitoring.

The ADE9000 offers an integrated flexible waveform buffer that stores samples at a fixed data rate of 32 kSPS or 8 kSPS, or a sampling rate that varies based on line frequency to ensure 128 points per line cycle. Resampling simplifies fast Fourier transform (FFT) calculation of at least 50 harmonics in an external processor.

The ADE9000 simplifies the implementation of energy and power quality monitoring systems by providing tight integration of acquisition and calculation engines. The integrated ADCs and DSP engine calculate various parameters and provide data through user accessible registers or indicate events through interrupt pins. With seven dedicated ADC channels, the ADE9000 can be used on a 3-phase system or up to three single-phase systems. It supports current transformers (CTs) or Rogowski coils for current measurements. A digital integrator eliminates a discrete integrator required for Rogowski coils.

The ADE9000 absorbs most complexity in calculations for a power monitoring system. With a simple host microcontroller, the ADE9000 enables the design of standalone monitoring or protection systems, or low cost nodes uploading data into the cloud.

Note that throughout this data sheet, multifunction pins, such as CF4/$\overline{\text{EVENT}}$/DREADY, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{\text{EVENT}}$, when only that function is relevant.

[2] Protected by U.S. Patents 8,350,558; 8,010,304. Other patents are pending.

TYPICAL APPLICATIONS CIRCUIT

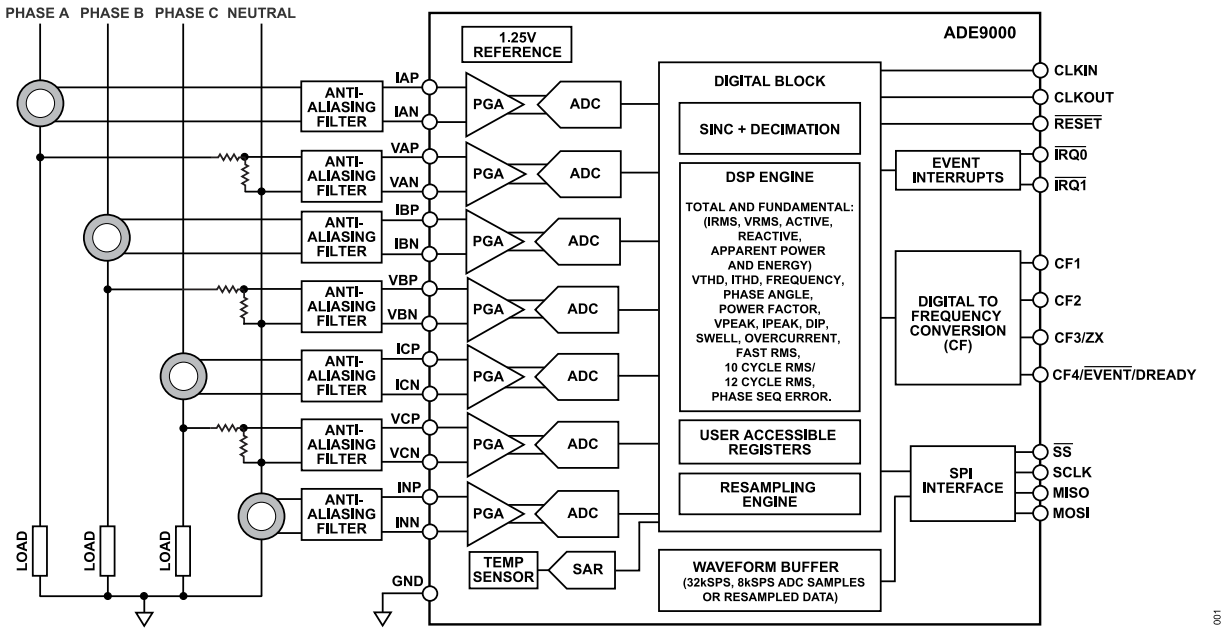

Figure 1. Typical Applications Circuit

SPECIFICATIONS

VDD = 2.97 V to 3.63 V, GND = AGND = DGND = 0 V, on-chip reference, CLKIN = 24.576 MHz crystal (XTAL), T_{MIN} to T_{MAX} = −40°C to +85°C, T_A = 25°C (typical), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY (MEASUREMENT ERROR PER PHASE)					
Total Active Energy		0.1		%	Over a dynamic range of 5000 to 1, 10 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, high-pass filter (HPF) corner = 4.98 Hz
		0.2		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Total Reactive Energy		0.1		%	Over a dynamic range of 5000 to 1, 10 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.2		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Total Apparent Energy		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation
		0.5		%	Over a dynamic range of 5000 to 1, 10 sec accumulation
		0.1		%	Over a dynamic range of 500 to 1, 1 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Fundamental Active Energy		0.1		%	Over a dynamic range of 5000 to 1, 2 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 10 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.2		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Fundamental Reactive Energy		0.1		%	Over a dynamic range of 5000 to 1, 2 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 10 sec accumulation

SPECIFICATIONS

Table 1. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.2		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Fundamental Apparent Energy		0.1		%	Over a dynamic range of 5000 to 1, 2 sec accumulation
		0.5		%	Over a dynamic range of 10,000 to 1, 10 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
IRMS, VRMS		0.1		%	Over a dynamic range of 1000 to 1
		0.5		%	Over a dynamic range of 5000 to 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 1000 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
Fundamental IRMS, VRMS		0.1		%	Over a dynamic range of 1000 to 1
		0.5		%	Over a dynamic range of 5000 to 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 2000 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
Active Power, VAR, VA		0.2		%	Over a dynamic range of 1000 to 1
		0.4		%	Over a dynamic range of, 3000 to 1
		0.2		%	Over a dynamic range of 500 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 1000 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
Power Factor (PF) Error		±0.001		%	Over a dynamic range of 5000 to 1
128-Point per Line Cycle Resampled Data		0.1		%	An FFT is performed to receive the magnitude response; this error is the worst case error in the magnitude caused by resampling algorithm distortion; input signal is 50 Hz fundamental and ninth harmonic both at half of full scale (FS)
		−72		dB	Amplitude of highest spur; input signal is 50 Hz fundamental and ninth harmonic both at half of FS
		1.25		%	An FFT is performed to receive the magnitude response; this error is the worst case error in the magnitude caused by resampling algorithm distortion; input signal is 50 Hz fundamental and 31st harmonic, both at half of FS
		−38		dB	Amplitude of highest spur; input signal is

SPECIFICATIONS

Table 1. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
					50 Hz fundamental and 31st harmonic, both at half of FS
VRMS½, IRMS½ RMS Voltage Refreshed Each Half-Cycle[1]		0.25		%	Data sourced before HPF, no dc offset at inputs, over a dynamic range of 100 to 1
10 Cycle/12 Cycle IRMS, VRMS[1]		0.2		%	Data sourced before HPF, no dc offset at inputs, over a dynamic range of 100 to 1
Line Period Measurement		0.001		Hz	Resolution at 50 Hz
Current to Current, Voltage to Voltage, and Voltage to Current Angle Measurement		0.018		Degrees	Resolution at 50 Hz
ADC					
PGA Gain Settings (PGA_GAIN)		1, 2, or 4		V/V	PGA gain setting is referred to as PGA_GAIN
Differential Input Voltage Range (VxP to VxN, IxP to IxN)	−1/Gain		+1/Gain	V	707 mV rms, when V_{REF} = 1.25 V, this voltage corresponds to 53 million codes
Maximum Operating Voltage on Analog Input Pins (VxP, VxN, IxP, and IxN)	−0.6		+0.6	V	Voltage on the pin with respect to ground (GND = AGND = DGND = REFGND)
Signal-to-Noise Ratio (SNR)[2]					
PGA = 1		96		dB	32 kSPS, sinc4 output, V_{IN} = −0.5 dB from FS
		101		dB	8 kSPS, sinc4 + infinite impulse response (IIR), low-pass filter (LPF) output, V_{IN} = −0.5 dB from FS
PGA = 4		93		dB	32 kSPS, sinc4 output
		96		dB	8 kSPS, sinc4 + IIR LPF output
Total Harmonic Distortion (THD)[2]					
PGA = 1		−101	−95	dB	32 kSPS, sinc4 output, V_{IN} = −0.5 dB from FS
		−101	−95	dB	8 kSPS, sinc4 + IIR LPF output, V_{IN} = −0.5 dB from FS
PGA = 4		−107	−99	dB	32 kSPS, sinc4 output
		−107	−99	dB	8 kSPS, sinc4 + IIR LPF output
Signal-to-Noise and Distortion Ratio (SINAD)[2]					
PGA = 1		95		dB	32 kSPS, sinc4 output, V_{IN} = −0.5 dB from FS
		98		dB	8 kSPS, sinc4 + IIR LPF output, V_{IN} = −0.5 dB from FS
PGA = 4		93		dB	32 kSPS, sinc4 output
		96		dB	8 kSPS, sinc4 + IIR LPF output
Spurious-Free Dynamic Range (SFDR)[2]					
PGA = 1		100		dB	32 kSPS, sinc4 output, V_{IN} = −0.5 dB from FS
		100		dB	8 kSPS, sinc4 + IIR LPF output, V_{IN} = −0.5 dB from FS
Output Pass Band (0.1dB)					
Sinc4 Outputs		1.344		kHz	32 kSPS, sinc4 output
Sinc4 + IIR LPF Outputs		1.344		kHz	8 kSPS output
Output Bandwidth (−3 dB)[2]					
Sinc4 Outputs		7.2		kHz	32 kSPS, sinc4 output
Sinc4 + IIR LPF Outputs		3.2		kHz	8 kSPS output
Crosstalk[2]		−120		dB	At 50 Hz or 60 Hz, see the Terminology section
AC Power Supply Rejection Ratio (AC PSRR)[2]		−120		dB	At 50 Hz, see the Terminology section

SPECIFICATIONS

Table 1. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Common-Mode Rejection Ratio (AC CMRR)[2]		115		dB	At 100 Hz and 120 Hz
Gain Error		±0.3	±1	%typ	See the Terminology section
Gain Drift[2]		±3		ppm/°C	See the Terminology section
Offset		±0.040	±3.8	mV	See the Terminology section
Offset Drift[2]		0	±2	µV/°C	See the Terminology section
Channel Drift (PGA, ADC, Internal Voltage Reference)		±7	±25	ppm/°C	PGA = 1, internal V_{REF}
		±7	±25	ppm/°C	PGA = 2, internal V_{REF}
		±7	±25	ppm/°C	PGA = 4, internal V_{REF}
Differential Input Impedance (DC)	165	185		kΩ	PGA = 1, see the Terminology section
	80	90		kΩ	PGA = 2
	40	45		kΩ	PGA = 4
INTERNAL VOLTAGE REFERENCE					Nominal = 1.25 V ± 1 mV
Voltage Reference		1.250		V	T_A = 25°C, REF pin
Temperature Coefficient[2]		±5	±20	ppm/°C	T_A = −40°C to +85°C, tested during device characterization
EXTERNAL VOLTAGE REFERENCE					
Input Voltage (REF)		1.2 or 1.25		V	REFGND must be tied to GND, AGND, and DGND, a 1.25 V external reference is preferred; the FS values mentioned in this data sheet are for a voltage reference of 1.25 V
Input Impedance		7.5		kΩ	
TEMPERATURE SENSOR					
Temperature Accuracy		±2		°C	−10°C to +40°C
		±3		°C	−40°C to +85°C
Temperature Readout Step Size			0.3	°C	
CRYSTAL OSCILLATOR					All specifications use CLKIN = 24.576 MHz ± 30 ppm
Input Clock Frequency	24.33	24.576	24.822	MHz	
Internal Capacitance on CLKIN, CLKOUT		4		pF	
Internal Feedback Resistance Between CLKIN and CLKOUT		2.45		MΩ	
Transconductance (g_m)	5	8		mA/V	
EXTERNAL CLOCK INPUT					
Input Clock Frequency	24.330	24.576	24.822	MHz	±1%
Duty Cycle[2]	45:55	50:50	55:45	%	
CLKIN Logic Input Voltage					3.3 V tolerant
High, V_{INH}	1.2			V	V_{DD} = 2.97 V to 3.63 V
Low, V_{INL}			0.5	V	V_{DD} = 2.97 V to 3.63 V
LOGIC INPUTS (PM0, PM1, $\overline{\text{RESET}}$, MOSI, SCLK, and $\overline{\text{SS}}$)					
Input Voltage					
V_{INH}	2.4			V	
V_{INL}			0.8	V	
Input Current, I_{IN}			15	µA	V_{IN} = 0 V
Internal Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					

SPECIFICATIONS

Table 1. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MISO, $\overline{IRQ0}$, and $\overline{IRQ1}$					
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 4 mA
Low, V_{OL}			0.8	V	I_{SINK} = 4 mA
Internal Capacitance, C_{IN}			10	pF	
C1, CF2, CF3, and CF4					
Output Voltage					
V_{OH}	2.4			V	I_{SOURCE} = 7 mA
V_{OL}			0.8	V	I_{SINK} = 8 mA
C_{IN}			10	pF	
LOW DROPOUT REGULATORS (LDOs)					
AVDD		1.9		V	
DVDD		1.7		V	
POWER SUPPLY					
V_{DD}	2.97	3.3	3.63	V	Power-on reset level is 2.4 V to 2.6 V
Supply Current (V_{DD})					
Power Save Mode 0 (PSM0)		15	17	mA	Normal mode
		14.5	16.5	mA	Normal mode, six ADCs enabled
Power Save Mode 3 (PSM3)		90	300	nA	Idle, V_{DD} = 3.3 V, AV_{DD} = 0 V, DV_{DD} = 0 V

[1] Enables implementation of IEC 61000-4-30.

[2] Tested during device characterization.

TIMING CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	10			ns
SCLK Frequency	f_{SCLK}			20	MHz
SCLK Low Pulse Width	t_{SL}	20			ns
SCLK High Pulse Width	t_{SH}	20			ns
Data Output Valid After SCLK Edge	t_{DAV}			20	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10			ns
Data Output Fall Time	t_{DF}			10	ns
Data Output Rise Time	t_{DR}			10	ns
SCLK Fall Time	t_{SF}			10	ns
SCLK Rise Time	t_{SR}			10	ns
MISO Disable Time After $\overline{SS}$ Rising Edge	t_{DIS}			100	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0			ns

SPECIFICATIONS

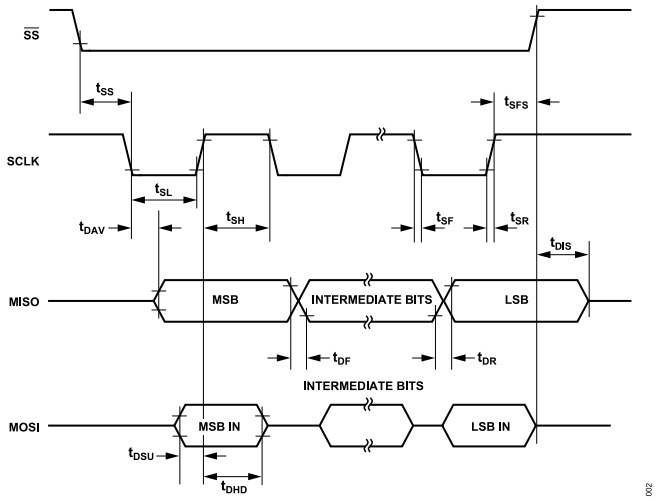

Figure 2. SPI Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to GND	−0.3 V to +3.96 V
Analog Input Voltage to GND, IAP, IAN, IBP, IBN, ICP, ICN, INP, INN, VAP, VAN, VBP, VBN, VCP, VCN	−2 V to +2 V
Reference Input Voltage to REFGND	−0.3 V to +2 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec)[1]	260°C
ESD	
Human Body Model[2]	4 kV
Machine Model[3]	300 V
Field Induced Charged Device Model (FICDM)[4]	1.25 kV

[1] Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

[2] Applicable standard: ANSI/ESDA/JEDEC JS-001-2014.

[3] Applicable standard: JESD22-A115-A (ESD machine model standard of JEDEC).

[4] Applicable standard: JESD22-C101F (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} and θ_{JC} are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-7[1]	27.14	3.13	°C/W

[1] The junction to air measurement uses a 2S2P JEDEC test board with 4 × 4 standard JEDEC vias. The junction to case measurement uses a 1S0P JEDEC test board with 4 × 4 standard JEDEC vias. See JEDEC standard JESD51-2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

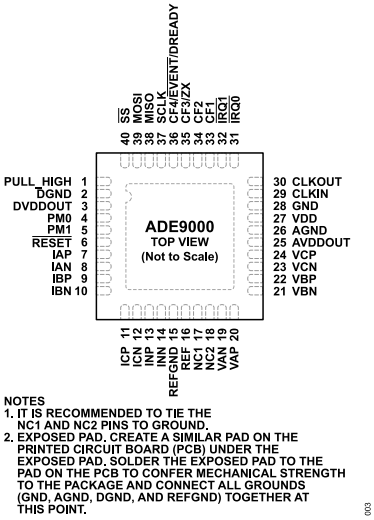

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PULL_HIGH	Pull High. Tie this pin to VDD.
2	DGND	Digital Ground. This pin provides the ground reference for the digital circuitry in the ADE9000. Because the digital return currents in the ADE9000 are small, it is acceptable to connect this pin to the analog ground plane of the whole system. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
3	DVDDOUT	1.8 V Output of the Digital Low Dropout Regulator (LDO). Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor.
4	PM0	Power Mode Pin 0. PM0, combined with PM1, defines the power mode. For normal operation, ground PM0 and PM1.
5	PM1	Power Mode Pin 1. PM1 combined with PM0, defines the power mode. For normal operation, ground PM0 and PM1.
6	$\overline{\text{RESET}}$	Reset Input, Active Low. This pin must stay low for at least 1 µs to trigger a hardware reset.
7, 8	IAP, IAN	Analog Inputs, Channel IA. The IAP (positive) and IAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
9, 10	IBP, IBN	Analog Inputs, Channel IB. The IBP (positive) and IBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
11, 12	ICP, ICN	Analog Inputs, Channel IC. The ICP (positive) and ICN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
13, 14	INP, INN	Analog Inputs, Channel IN. The INP (positive) and INN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
15	REFGND	Ground Reference, Internal Voltage Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
16	REF	Voltage Reference. The REF pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. An external reference source of 1.2 V to 1.25 V can also be connected at this pin. In either case, decouple REF to REFGND with 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor. After reset, the on-chip reference is enabled. To use the internal voltage reference with external circuits, a buffer is required.
17	NC1	No Connection. It is recommended to tie this pin to ground.
18	NC2	No Connection. It is recommended to tie this pin to ground.
19, 20	VAN, VAP	Analog Inputs, Channel VA. The VAP (positive) and VAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
21, 22	VBN, VBP	Analog Inputs, Channel VB. The VBP (positive) and VBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
23, 24	VCN, VCP	Analog Inputs, Channel VC. The VCP (positive) and VCN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
25	AVDDOUT	1.9 V Output of the Analog Low Dropout Regulator (LDO). Decouple AVDDOUT with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor. Do not connect external active circuitry to this pin.
26	AGND	Analog Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
27	VDD	Supply Voltage. The VDD pin provides the supply voltage. Decouple VDD to GND with a ceramic 0.1 µF capacitor in parallel with a 10 µF ceramic capacitor.
28	GND	Supply Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
29	CLKIN	Crystal/Clock Input. Connect a crystal across CLKIN and CLKOUT to provide a clock source. Alternatively, an external clock can be provided at this logic input.
30	CLKOUT	Crystal Output. Connect a crystal across CLKIN and CLKOUT to provide a clock source. When using CLKOUT to drive external circuits, connect an external buffer.
31	$\overline{\text{IRQ0}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
32	$\overline{\text{IRQ1}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
33	CF1	Calibration Frequency (CF) Logic Output 1. The CF1, CF2, CF3, and CF4 outputs provide power information based on the CFxSEL bits in the CFMODE register. Use these outputs for operational and calibration purposes. Scale the full-scale output frequency by writing to the CFxDEN registers (see the Digital to Frequency Conversion—CFx Output section).
34	CF2	CF Logic Output 2. This pin indicates CF2.
35	CF3/ZX	CF Logic Output 3/Zero Crossing. This pin indicates CF3 or zero crossing.
36	CF4/$\overline{\text{EVENT}}$/DREADY	CF Logic Output 4/Event Pin/Data Ready. This pin indicates CF4, events, or when new data is ready.
37	SCLK	Serial Clock Input for the SPI Port. All serial data transfers synchronize to this clock (see the Accessing On-Chip Data section). The SCLK pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time, for example, optoisolator outputs.
38	MISO	Data Output for the SPI Port.
39	MOSI	Data Input for the SPI Port.
40	$\overline{\text{SS}}$	Slave Select for the SPI Port.
	EPAD	Exposed Pad. Create a similar pad on the printed circuit board (PCB) under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package and connect all grounds (GND, AGND, DGND, and REFGND) together at this point.

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY LINEARITY OVER SUPPLY AND TEMPERATURE

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz, a sinusoidal current with variable amplitudes from 100% of full scale down to 0.01% or 0.02% of full scale, a frequency of 50 Hz, and the integrator off. Fundamental energies obtained with a fundamental voltage component, with an amplitude of 50% of full scale in phase with a fifth harmonic, a current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.01% of full scale, a fifth harmonic with a constant amplitude of 40% of fundamental, and the integrator off, unless otherwise noted.

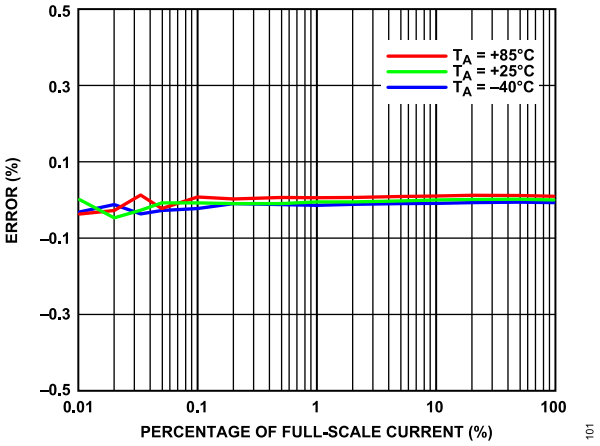

Figure 4. Total Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

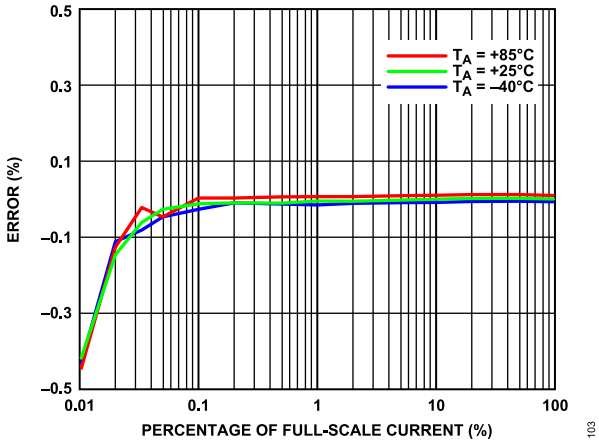

Figure 6. Total Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

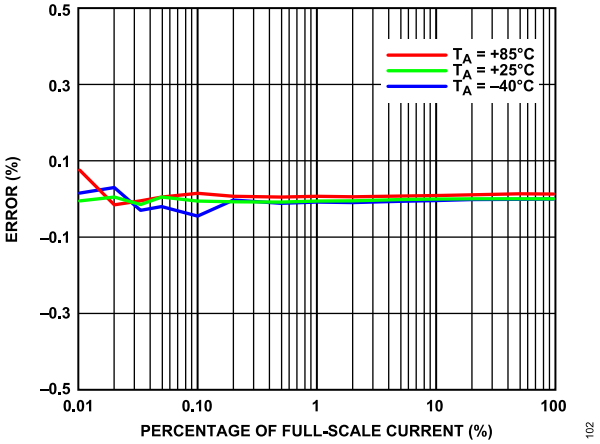

Figure 5. Total Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0

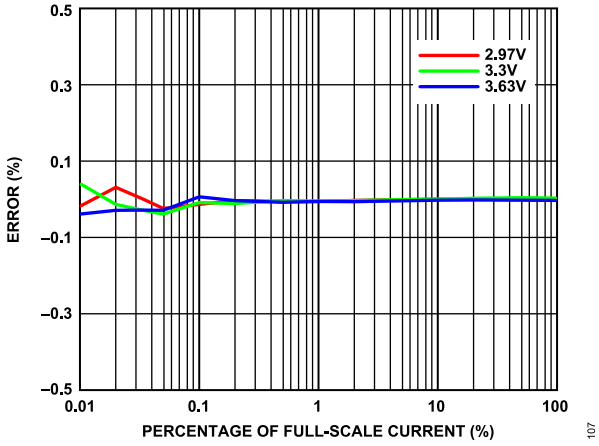

Figure 7. Total Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

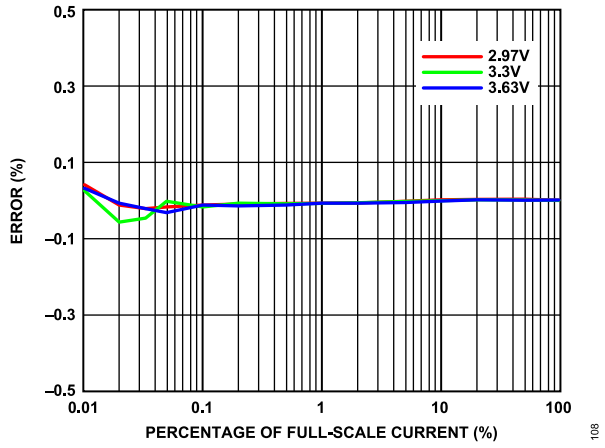

Figure 8. Total Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0, T_A = 25°C

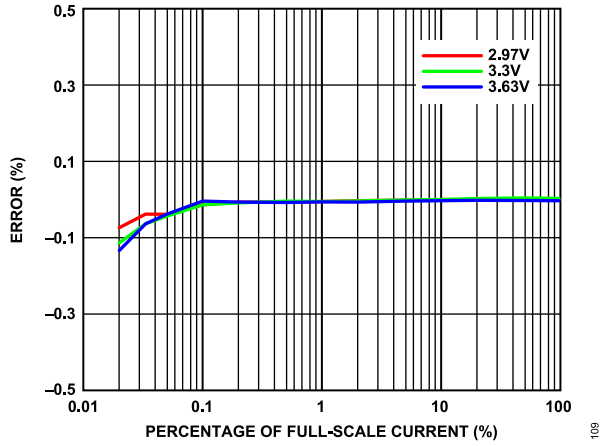

Figure 9. Total Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C

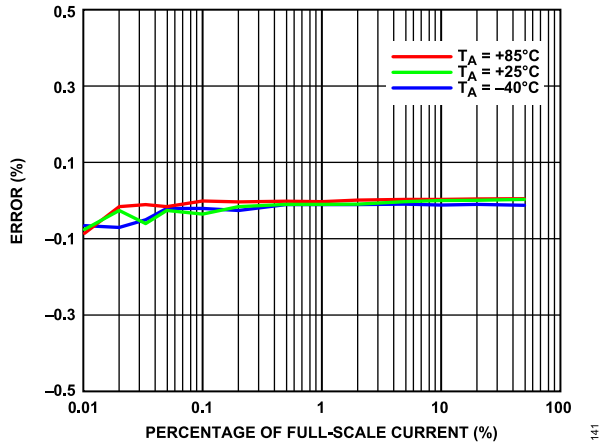

Figure 10. Fundamental Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

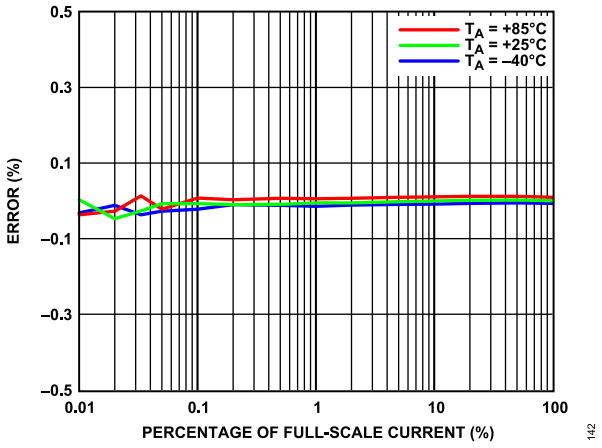

Figure 11. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0

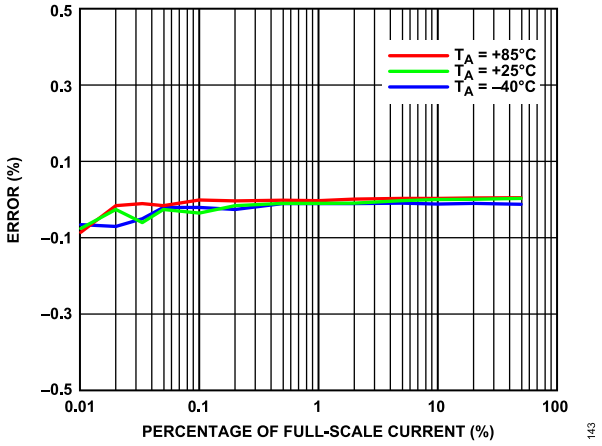

Figure 12. Fundamental Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

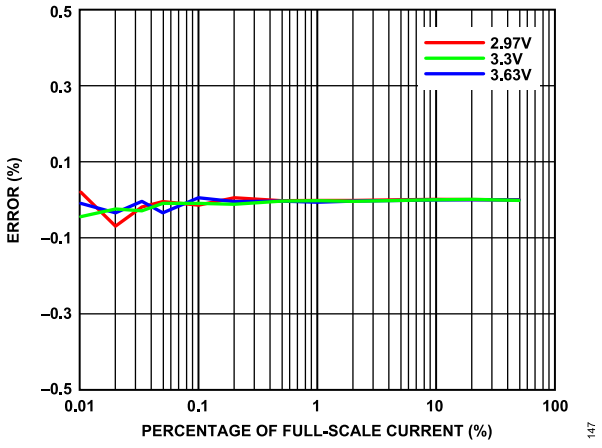

Figure 13. Fundamental Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

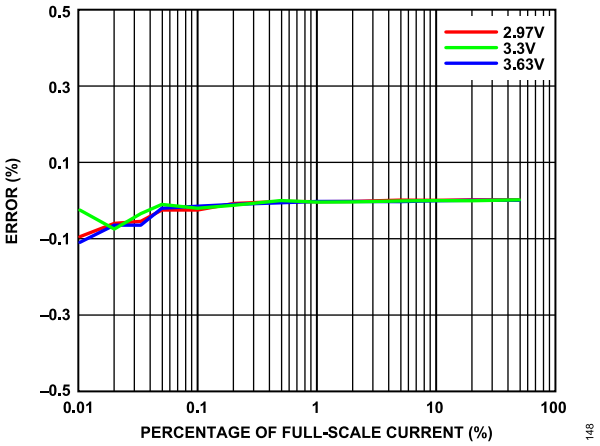

Figure 14. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0, T_A = 25°C

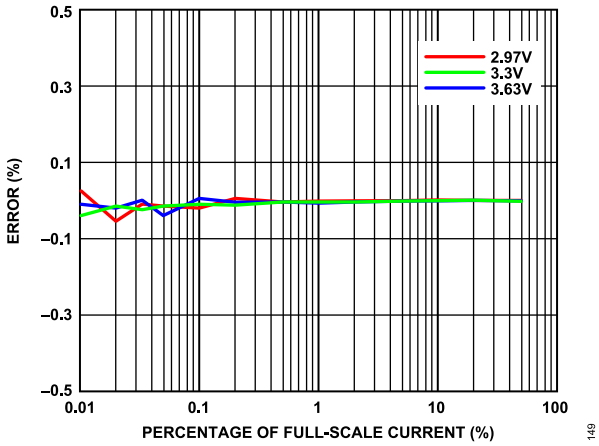

Figure 15. Fundamental Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY ERROR OVER FREQUENCY AND POWER FACTOR

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale, a sinusoidal current with a constant amplitude of 10% of full scale, a variable frequency between 45 Hz and 65 Hz, and the integrator off. Fundamental energies obtained with a fundamental voltage component, with an amplitude of 50% of full scale in phase with the fifth harmonic, a current with a 50 Hz component that has constant amplitude of 10% of full scale, a fifth harmonic with a constant amplitude of 40% of fundamental, and the integrator off, unless otherwise noted.

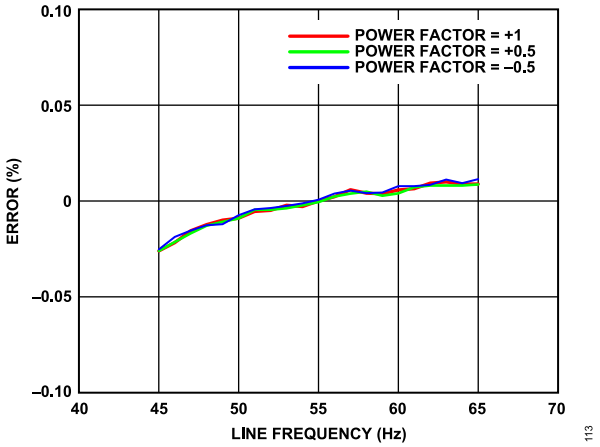

Figure 16. Total Active Energy Error vs. Line Frequency, Power Factor = −0.5, Power Factor = +0.5, and Power Factor = +1

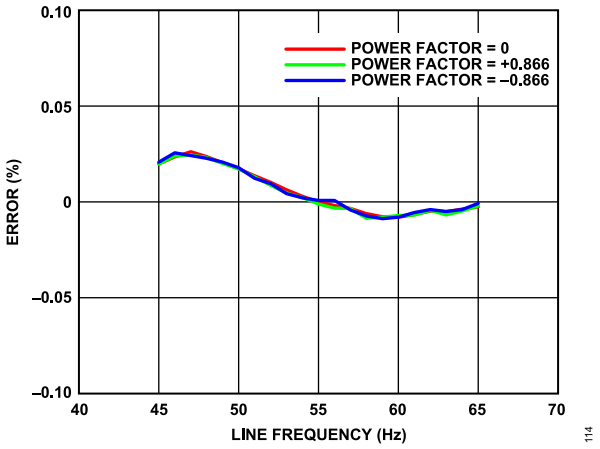

Figure 17. Total Reactive Energy Error vs. Line Frequency, Power Factor = −0.866, Power Factor = 0, and Power Factor = +0.866

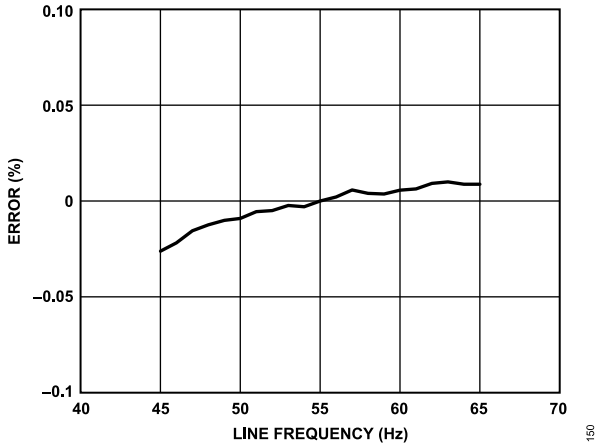

Figure 18. Total Apparent Energy Error vs. Line Frequency

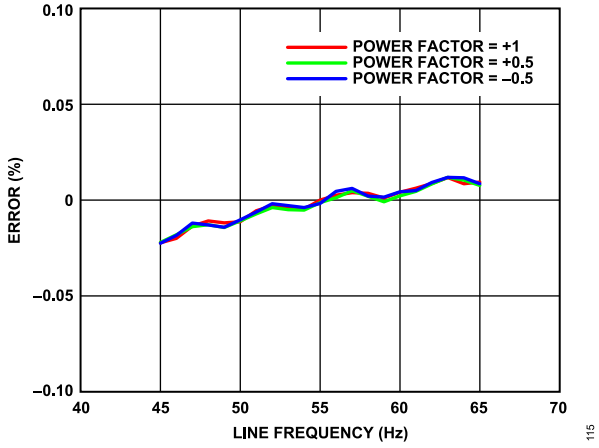

Figure 19. Fundamental Active Energy Error vs. Line Frequency, Power Factor = −0.5, Power Factor = +0.5, and Power Factor = +1

TYPICAL PERFORMANCE CHARACTERISTICS

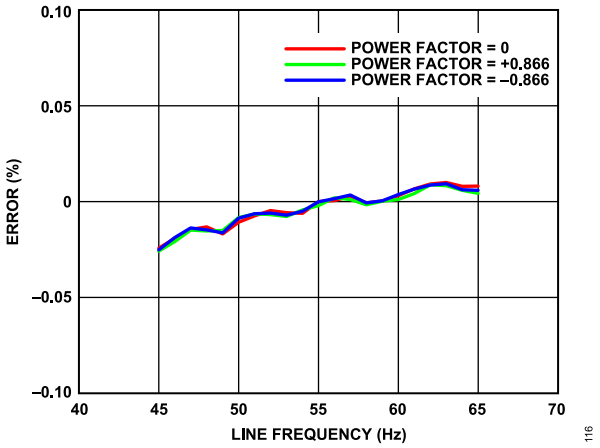

Figure 20. Fundamental Reactive Energy Error vs. Line Frequency, Power Factor = −0.866, Power Factor = 0, and Power Factor = +0.866

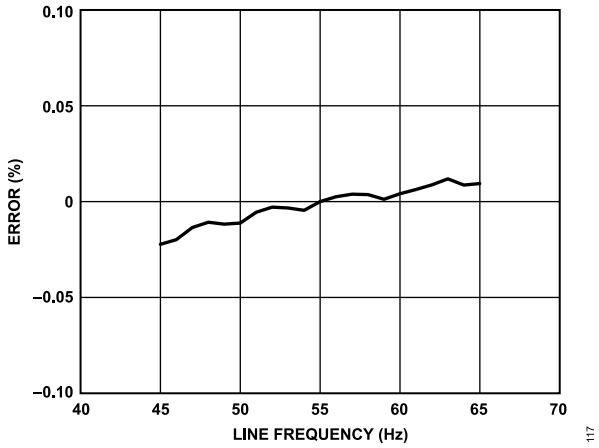

Figure 21. Fundamental Apparent Energy Error vs. Line Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY LINEARITY REPEATABILITY

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz, a sinusoidal current with variable amplitudes from 100% of full scale down to 0.01% of full scale, a frequency of 50 Hz, and the integrator off. Fundamental energies obtained with a fundamental voltage component, with an amplitude of 50% of full scale in phase with the fifth harmonic, a current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.01% of full scale, and a fifth harmonic with a constant amplitude of 40% of fundamental, and the integrator off. Measurements at 25°C repeated 30 times, unless otherwise noted.

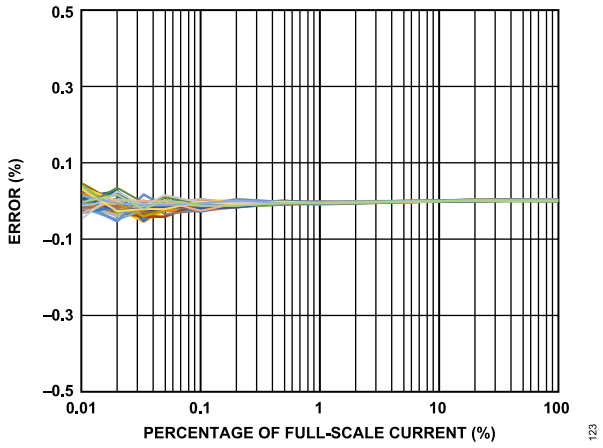

Figure 22. Total Active Energy Error as a Percentage of Full-Scale Current, Power Factor = 1 (Standard Deviation σ = 0.02% at 0.01% of Full-Scale Current)

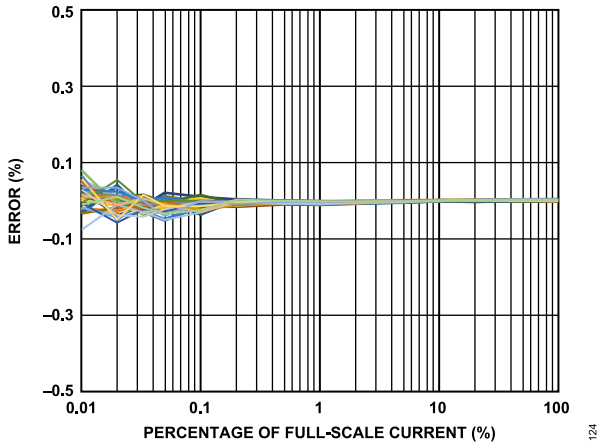

Figure 23. Total Reactive Energy Error as a Percentage of Full-Scale Current, Power Factor = 0 (Standard Deviation σ = 0.03% at 0.01% of Full-Scale Current)

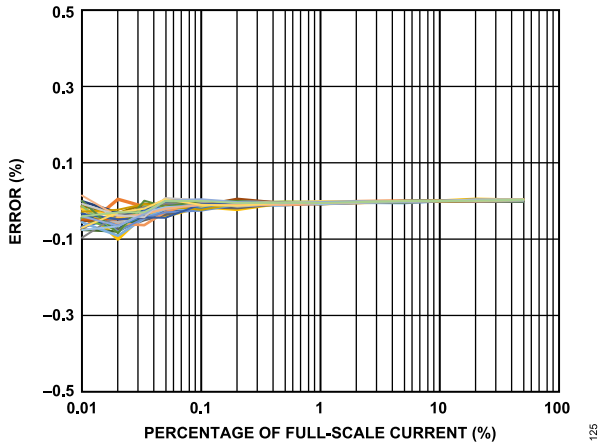

Figure 24. Fundamental Active Energy Error as a Percentage of Full-Scale Current, Power Factor = 1 (Standard Deviation σ = 0.03% at 0.01% of Full-Scale Current)

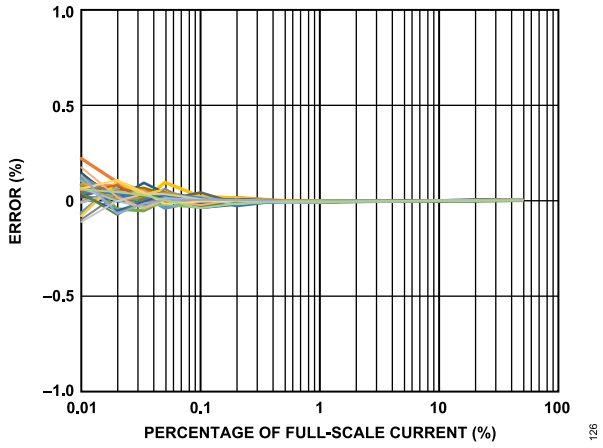

Figure 25. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current, Power Factor = 0 (Standard Deviation σ = 0.04% at 0.01% of Full-Scale Current)

TYPICAL PERFORMANCE CHARACTERISTICS

RMS LINEARITY OVER TEMPERATURE AND RMS ERROR OVER FREQUENCY

RMS linearity obtained with a sinusoidal current and voltage with variable amplitudes from 100% of full scale down to 0.01% of full scale using a frequency of 50 Hz, total rms error over frequency obtained with a sinusoidal current amplitude of 10% of full scale and voltage amplitude of 50% of full scale, and the integrator off. Fundamental rms error over frequency obtained with a sinusoidal current amplitude of 10% of full scale, a voltage amplitude of 50% of full scale, a fifth harmonic with a constant amplitude of 40% of fundamental, and the integrator off, unless otherwise noted.

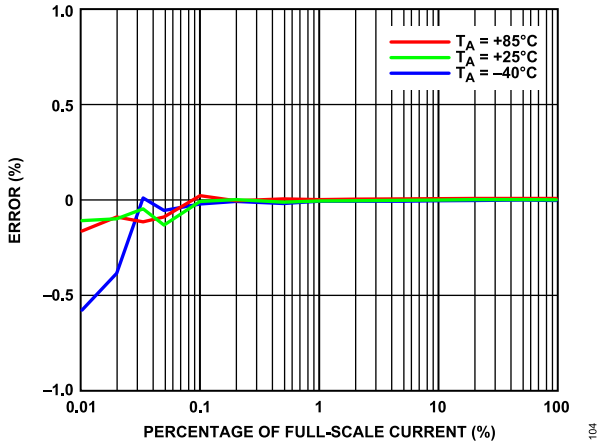

Figure 26. Current RMS Error as a Percentage of Full-Scale Current over Temperature

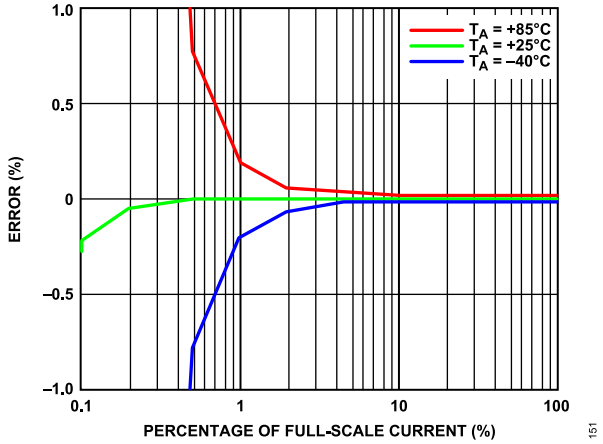

Figure 27. ½ Cycle Current RMS Error as a Percentage of Full-Scale Current over Temperature, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS_SRC_SEL = 1

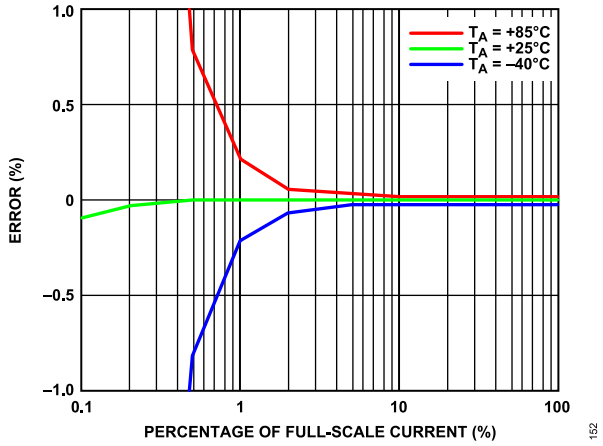

Figure 28. 10 Cycle Current RMS/12 Cycle Current Error as a Percentage of Full-Scale Current over Temperature, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS_SRC_SEL = 1

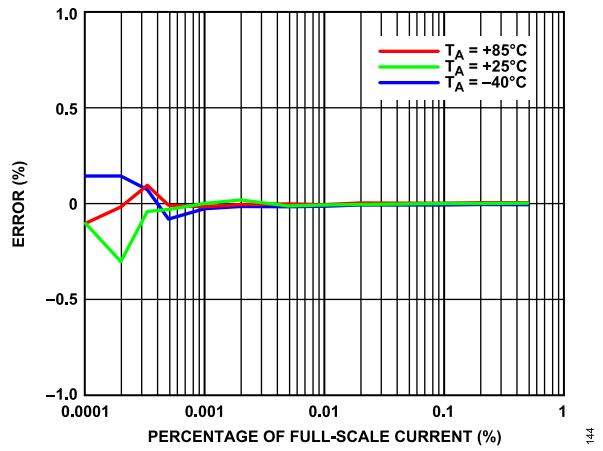

Figure 29. Fundamental Current RMS Error as a Percentage of Full-Scale Current over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

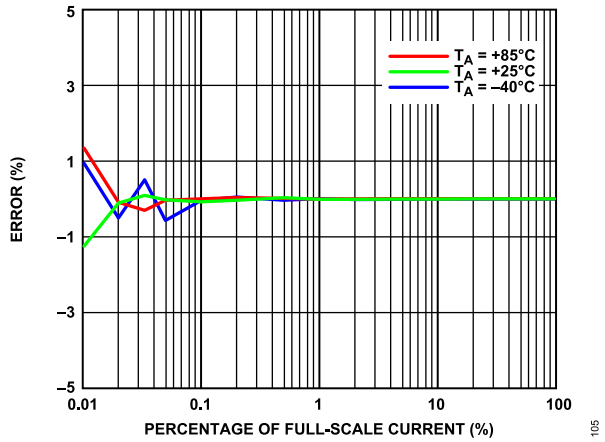

Figure 30. ½ Cycle Current RMS Error as a Percentage of Full-Scale Current over Temperature, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

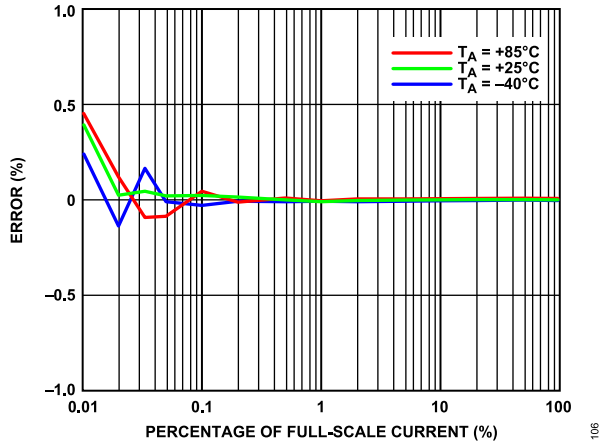

Figure 31. 10 Cycle Current RMS/12 Cycle Current Error as a Percentage of Full-Scale Current over Temperature, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

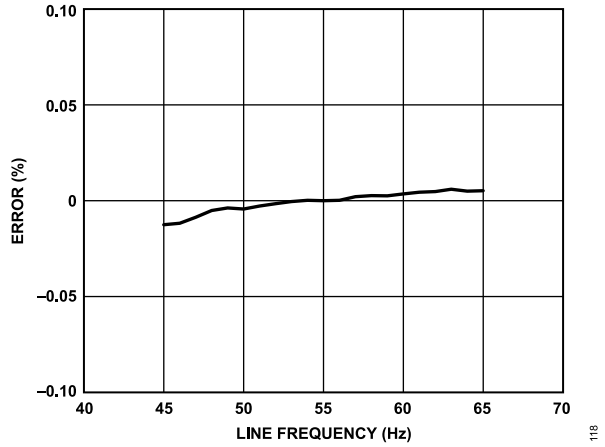

Figure 32. Current RMS Error vs. Line Frequency

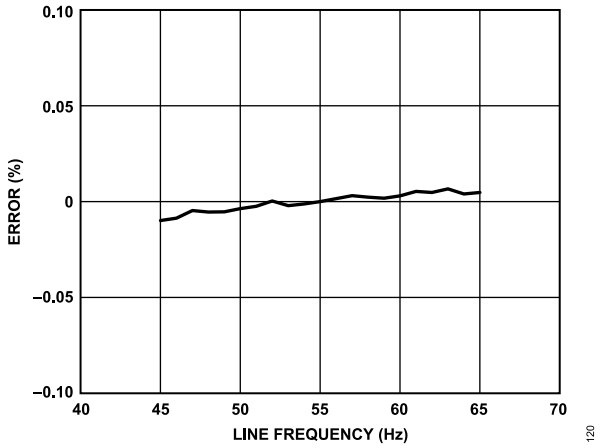

Figure 33. Fundamental Current RMS Error vs. Line Frequency

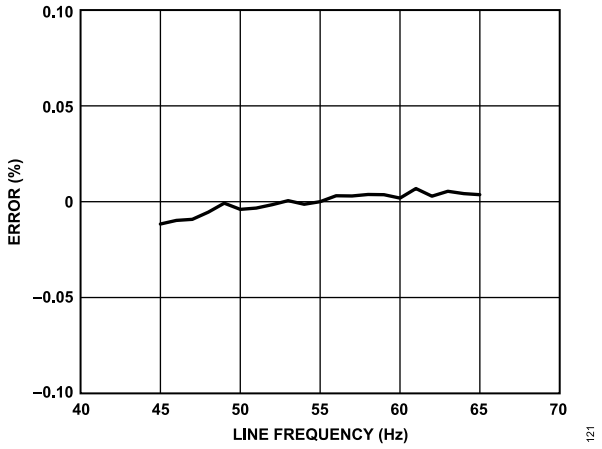

Figure 34. ½ Cycle Current RMS Error vs. Line Frequency, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

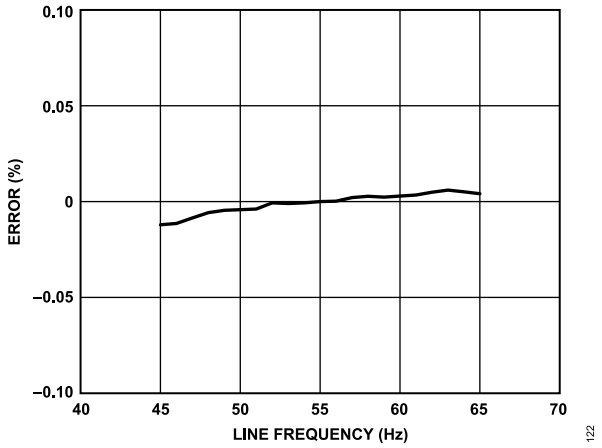

Figure 35. 10 Cycle Current RMS/12 Cycle Current Error vs. Line Frequency, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY AND RMS LINEARITY WITH INTEGRATOR ON

The sinusoidal voltage has an amplitude of 50% of full scale and a frequency of 50 Hz, PGA_GAIN is a gain set to 4, the sinusoidal current has variable amplitudes from 100% of full scale down to 0.01% or 0.1% of full scale and a frequency of 50 Hz, full scale at gain of 4 = (full scale at gain of 1)/4, a high-pass corner frequency of 4.97 Hz, and T_A = 25°C, unless otherwise noted.

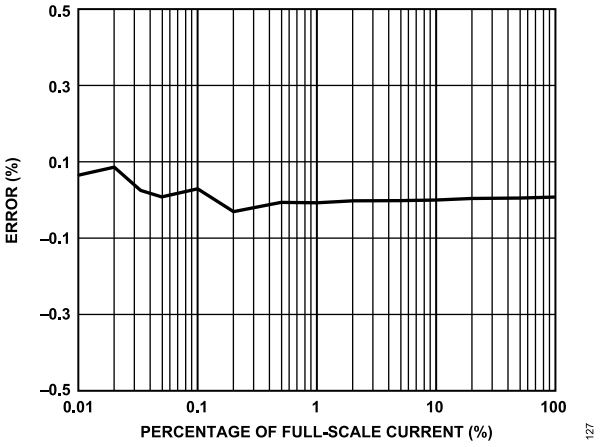

Figure 36. Total Active Energy Error, Gain = 4, Integrator On

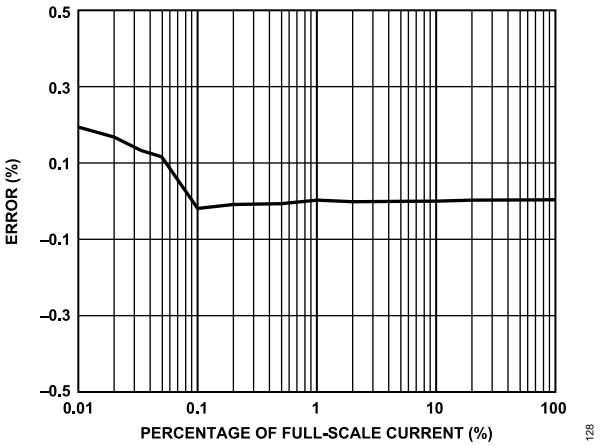

Figure 37. Total Reactive Energy Error, Gain = 4, Integrator On

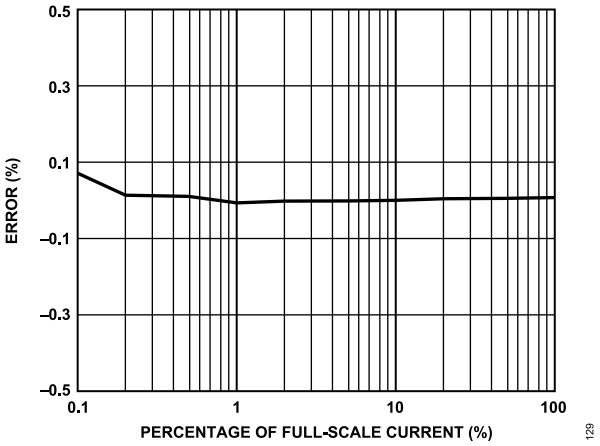

Figure 38. Total Apparent Energy Error, Gain = 4, Integrator On

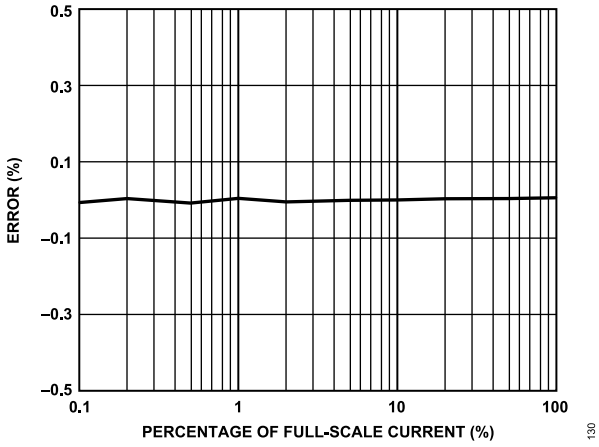

Figure 39. Total Current RMS Error, Gain = 4, Integrator On

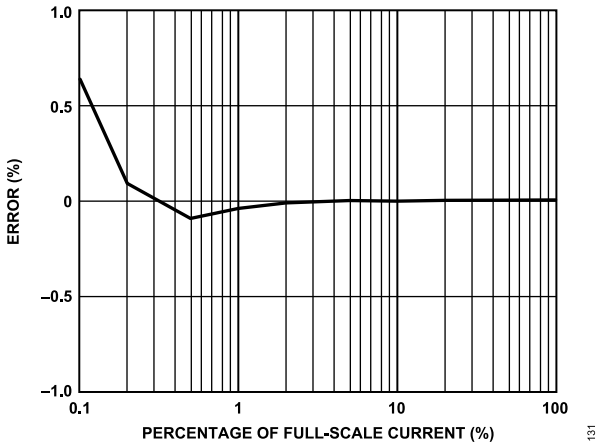

Figure 40. ½ Cycle Current RMS Error, Gain = 4, Integrator On, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

TYPICAL PERFORMANCE CHARACTERISTICS

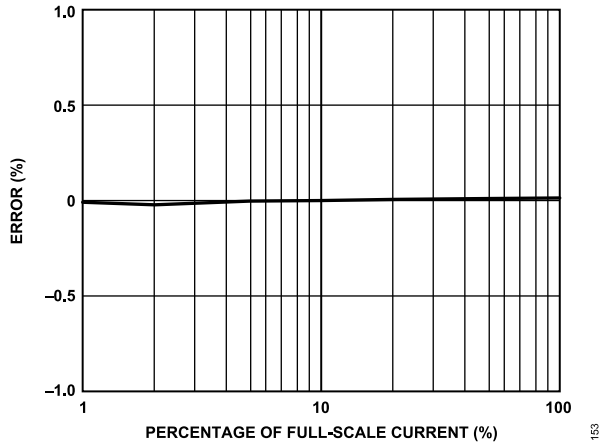

Figure 41. ½ Cycle Current RMS Error, Gain = 4, Integrator On, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS_SRC_SEL = 1

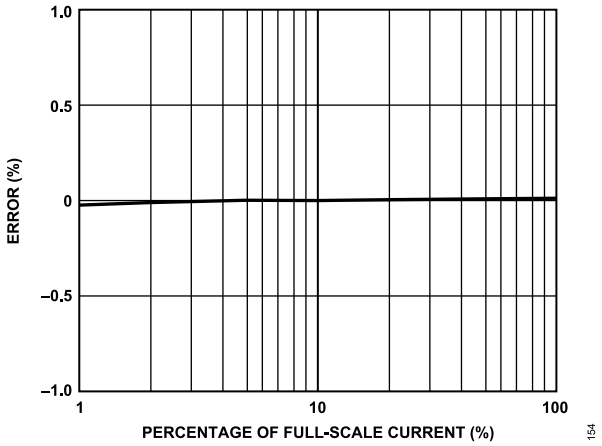

Figure 43. 10 Cycle Current RMS/12 Cycle Current RMS Error, Gain = 4, Integrator On, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS_SRC_SEL = 1

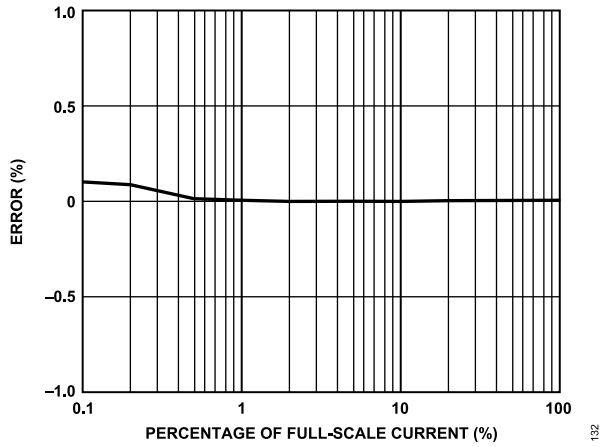

Figure 42. 10 Cycle Current RMS/12 Cycle Current Error, Gain = 4, Integrator On, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY AND RMS ERROR OVER FREQUENCY WITH INTEGRATOR ON

The sinusoidal voltage has a constant amplitude of 50% of full scale, PGA_GAIN is a gain set to 4, the sinusoidal current has a constant amplitude of 10% of full scale, and a variable frequency between 45 Hz and 65 Hz. Fundamental quantities obtained with a fundamental voltage component in phase with a fifth harmonic, a current with a fundamental component of 10% of full scale, a fifth harmonic with an amplitude of 40% of the fundamental, a full scale at gain of 4 = (full scale at gain of 1)/4, a high-pass corner frequency of 4.97 Hz, and T_A = 25°C, unless otherwise noted.

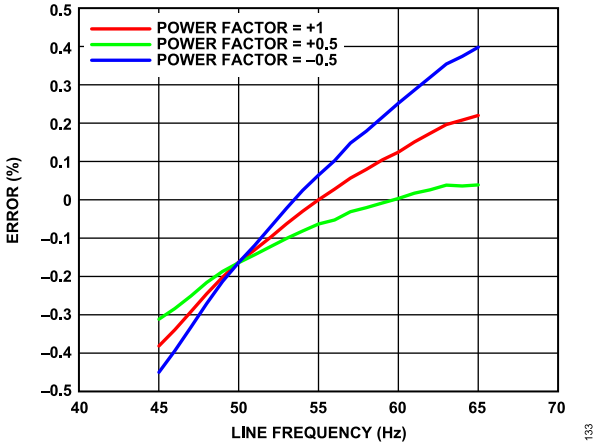

Figure 44. Total Active Energy Error vs. Line Frequency, Gain = 4, Integrator On, Power Factor = −0.5, Power Factor = +0.5, and Power Factor = +1

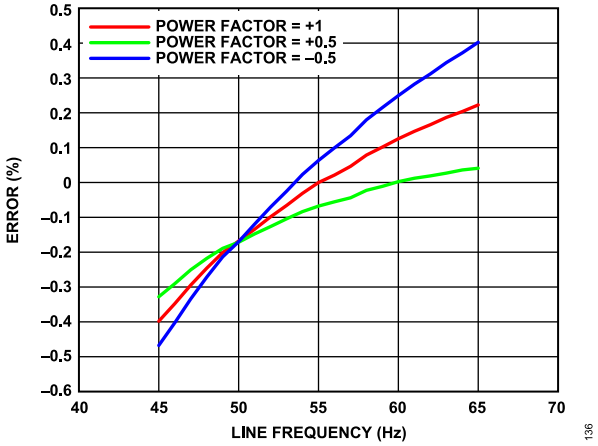

Figure 45. Fundamental Active Energy Error vs. Line Frequency, Gain = 4, Integrator On, Power Factor = −0.5, Power Factor = +0.5, and Power Factor = +1

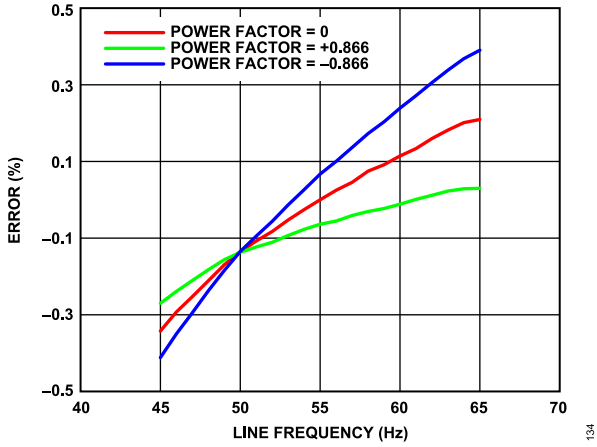

Figure 46. Total Reactive Energy Error vs. Line Frequency, Gain = 4, Integrator On, Power Factor = −0.866, Power Factor = +0.8665, and Power Factor = 0

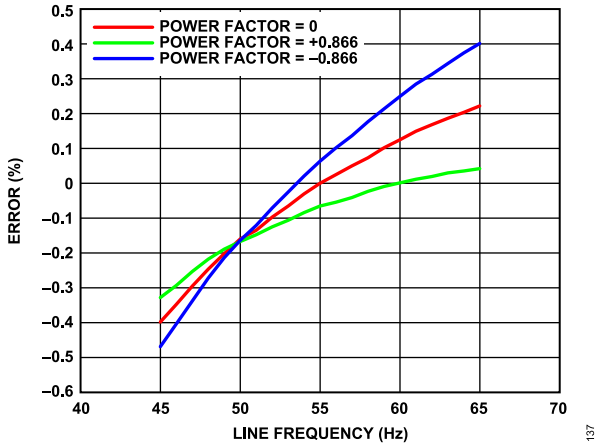

Figure 47. Fundamental Reactive Energy Error vs. Line Frequency, Gain = 4, Integrator On, Power Factor = −0.866, Power Factor = +0.8665, and Power Factor = 0

TYPICAL PERFORMANCE CHARACTERISTICS

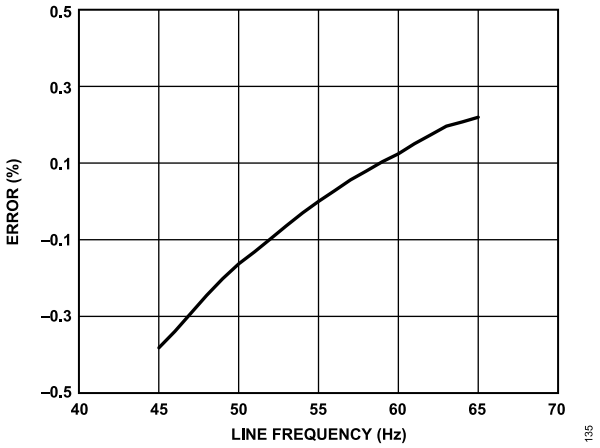

Figure 48. Total Apparent Energy Error vs. Line Frequency, Gain = 4, Integrator On

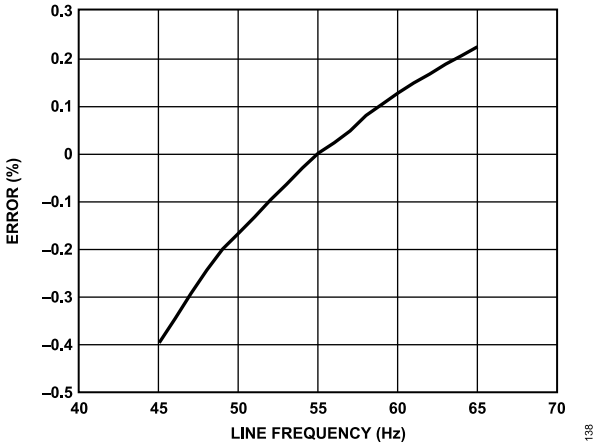

Figure 49. Fundamental Apparent Energy Error vs. Line Frequency, Gain = 4, Integrator On

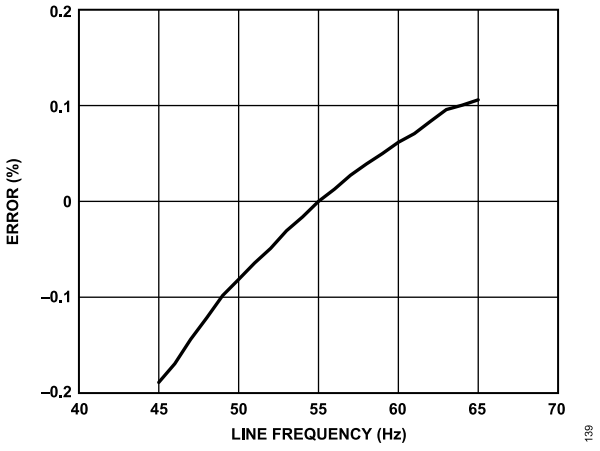

Figure 50. Current RMS Error vs. Line Frequency, Gain = 4, Integrator On

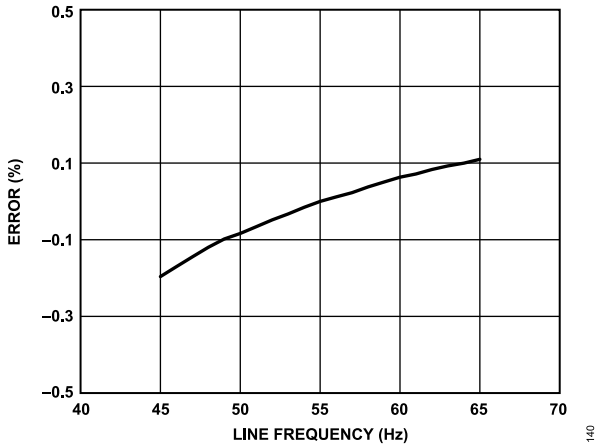

Figure 51. Fundamental Current RMS Error vs. Line Frequency, Gain = 4, Integrator On

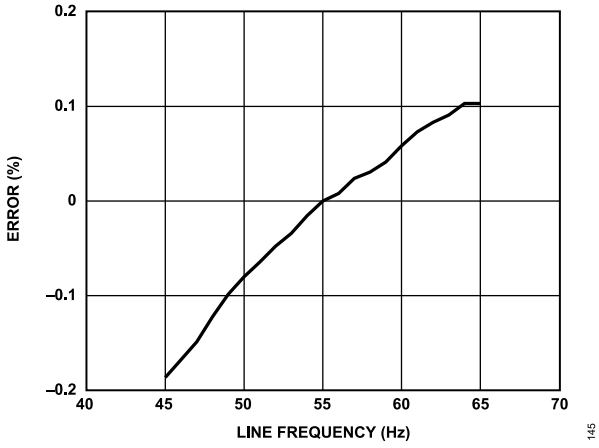

Figure 52. ½ Cycle Current RMS Error, Gain = 4, Integrator On, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

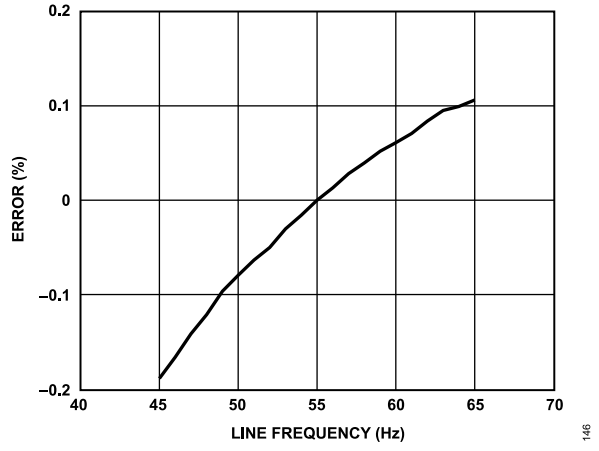

Figure 53. 10 Cycle Current RMS/12 Cycle Current Error, Gain = 4, Integrator On, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

TYPICAL PERFORMANCE CHARACTERISTICS

SIGNAL-TO-NOISE RATIO PERFORMANCE

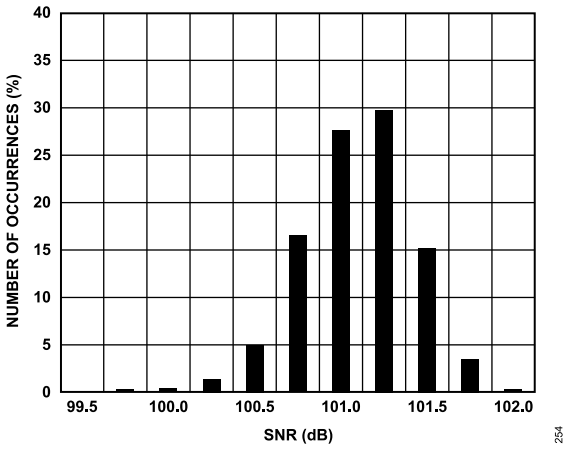

Figure 54. SNR Histogram of ADC SNR for 1000 Devices Tested at T_A = 25°C with PGA_GAIN = 1 and 8 kSPS Data Rate

TEST CIRCUIT

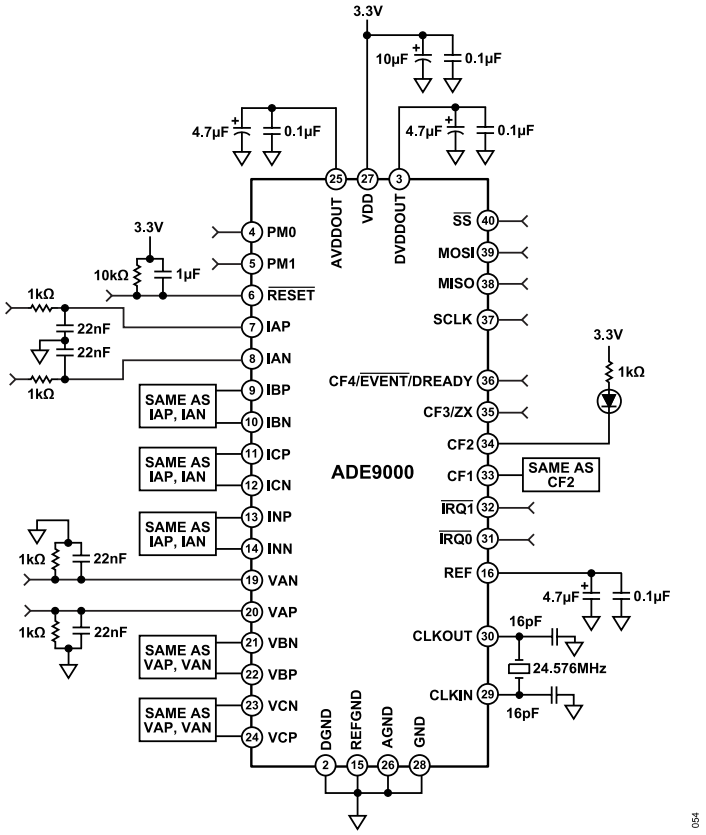

Figure 55. Test Circuit

TERMINOLOGY

Crosstalk

Crosstalk is measured by grounding one channel and applying a full-scale 50 Hz or 60 Hz signal on all the other channels. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 100 sec. Crosstalk is expressed in decibels.

Differential Input Impedance DC

The differential input impedance represents the impedance between the pair IxP and IxN or VxP and VxN. It varies with the PGA gain selection as indicated in .

ADC Offset

ADC offset is the difference between the average measured ADC output code with both inputs connected to GND and the ideal ADC output code of zero. ADC offset is expressed in mV.

ADC Offset Drift over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +85°C. Calculate the offset drift over temperature as follows:

$$Drift = \max\left(\left|\frac{Offset(-40°C) - Offset(+25°C)}{(-40°C - +25°C)}\right|, \left|\frac{Offset(+85°C) - Offset(+25°C)}{(+85°C - +25°C)}\right|\right) \quad (1)$$

Offset drift is expressed in µV/°C.

ADC Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when an external voltage reference of 1.2 V is used. The difference is expressed as a percentage of the ideal code. It represents the overall gain error of one channel.

ADC Gain Drift over Temperature

This temperature coefficient includes the temperature variation of the ADC gain while using an external voltage reference of 1.2 V. It represents the overall temperature coefficient of one current or voltage channel. With an external voltage reference of 1.2 V in use, the ADC gain is measured at −40°C, +25°C, and +85°C. Then the temperature coefficient is computed as follows:

$$Drift = \max\left(\left|\frac{Gain(-40°C) - Gain(+25°C)}{Gain(+25°C) \times (-40°C - +25°C)}\right|, \left|\frac{Gain(+85°C) - Gain(+25°C)}{Gain(+25°C) \times (+85°C - +25°C)}\right|\right) \quad (2)$$

Gain drift is measured in ppm/°C.

AC Power Supply Rejection (PSRR)

AC PSRR quantifies the measurement error as a percentage of reading when the dc power supply is nominal (V_{NOM}) and modulated with ac, and the inputs are grounded. For the ac PSRR measurement, 20 sec samples are captured with nominal supplies (3.3 V, which is V1) and a second set (V2) is captured with an additional ac signal (330 mV peak at 50 Hz) introduced onto the supplies. Then, the PSRR is expressed as PSRR = 20 $\log_{10}$(V2/V1).

Signal-to-Noise Ratio SNR

SNR is calculated by inputting a 50 Hz signal, and samples are acquired for 2 sec. The amplitudes for each frequency up to the bandwidth given in as the ADC output bandwidth (−3 dB) are calculated. To determine the SNR, the signal at 50 Hz is compared to the sum of the power from all the other frequencies, removing power from its harmonics. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio SINAD

SINAD is calculated by inputting a 50 Hz signal, and samples are acquired for 2 sec. The amplitudes for each frequency up to the bandwidth given in as the ADC output bandwidth (−3 dB) are calculated. To determine the SINAD, the signal at 50 Hz is compared to the sum of the power from all the other frequencies. The value for SINAD is expressed in decibels.

Total Harmonic Distortion THD

THD is calculated by inputting a 50 Hz signal, and samples are acquired for over 2 sec. The amplitudes for each frequency up to the bandwidth given in as the ADC output bandwidth (−3 dB) are calculated. To determine the THD, the amplitudes of the 50 Hz harmonics up to the bandwidth are root sum squared. The value for THD is expressed in decibels.

Spurious-Free Dynamic Range SFDR

SFDR is calculated by inputting a 50 Hz signal, and samples are acquired for over 2 sec. The amplitudes for each frequency up to the bandwidth given in as the ADC output bandwidth (−3 dB) are calculated. To determine the SFDR, the amplitude of the largest signal that is not a harmonic of 50 Hz is recorded. The value for SFDR is expressed in decibels.

ADC Output Pass Band

The ADC output pass band is the bandwidth within 0.1 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

ADC Output Bandwidth

The ADC output bandwidth is the bandwidth within −3 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

THEORY OF OPERATION

MEASUREMENTS

Current Channel

The ADE9000 has three phase current channels and one neutral current channel. The phase current channel datapath for IA, IB, and IC is shown in Figure 56 and datapath for the neutral channel is shown in Figure 57.

ADC_REDIRECT Multiplexer

The ADE9000 provides a multiplexer that allows any ADC output to be redirected to any digital processing datapath (see Figure 58).

By default, each modulator is mapped to its corresponding datapath.

Current Channel Gain, xIGAIN

The ADE9000 provides current gain calibration registers (AIGAIN, BIGAIN, CIGAIN and NIGAIN), one for each current channel.

The current channel gain varies with xIGAIN as shown in the following equation:

$$Current\ Channel\ Gain = \left(1 + \left(xIGAIN/2^{27}\right)\right) \quad (3)$$

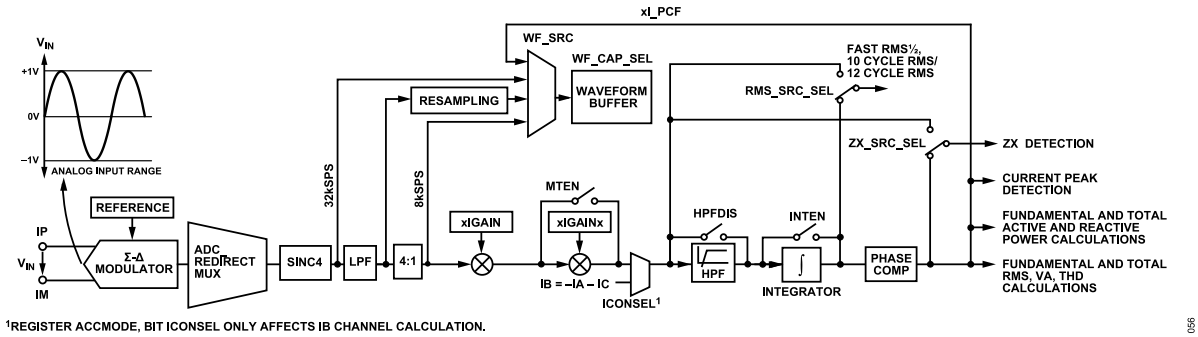

Figure 56. Current Channel (IA, IB, IC) Datapath

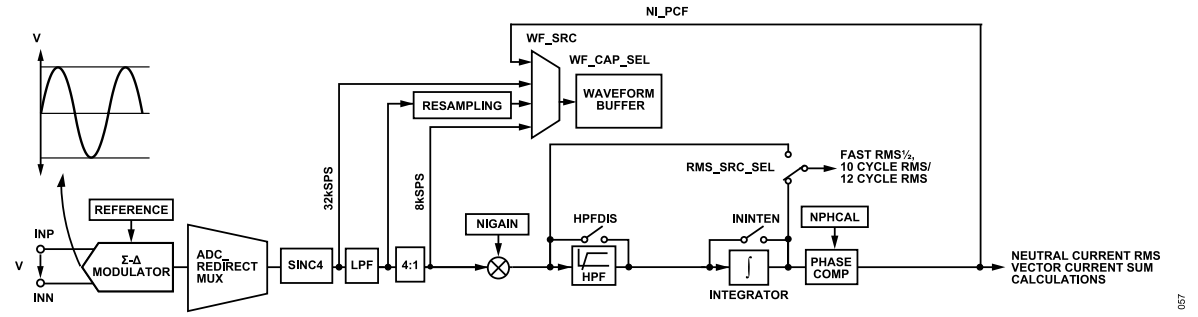

Figure 57. Neutral Current Channel (IN) Datapath

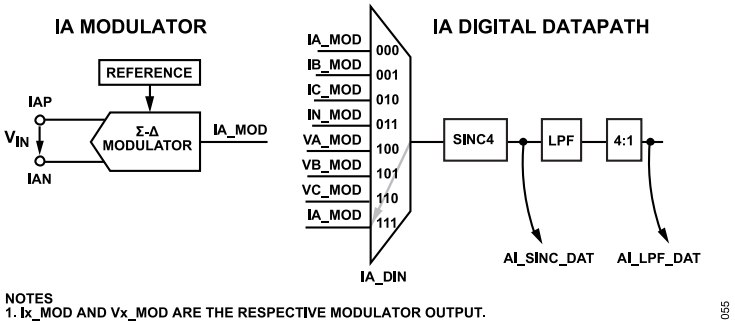

Figure 58. ADC_REDIRECT Modulator to Digital Datapath Multiplexing

THEORY OF OPERATION

IB Calculation Using ICONSEL

Write to the ICONSEL bit in the ACCMODE register to calculate $I_B = -I_A - I_C$. This setting can help save the cost of a current transformer in some 3-wire delta configurations.

High-Pass Filter

A high-pass filter removes dc offsets for accurate rms and energy measurements. It is enabled by default with a corner frequency is 1.25 Hz.

To disable the high-pass filter on all current and voltage channels set the HPFDIS bit in the CONFIG0 register. The corner frequency is configured with the HPF_CRN bits in the CONFIG2 register.

Digital Integrator

A digital integrator is included to allow easy interfacing to di/dt current sensors, also known as Rogowski coils. To configure the digital integrator use the INTEN and ININTEN bits in the CONFIG0 register. It is disabled by default. If the integrator is enabled, set the DICOEFF value to 0xFFFFE000.

Phase Compensation

The ADE9000 provides a phase compensation register for each current channel: APHCALx, BPHCALx, CPHCALx, and NPHCAL.

The phase calibration range is −15° to +2.25° at 50 Hz and −15° to +2.7° at 60 Hz.

Use the following equation to calculate the xPHCALx value for a given phase correction (φ)° angle. Phase correction (φ)° is positive to correct a current that lags the voltage, and negative to correct a current that leads the voltage, as seen in a current transformer.

$$xPHCALx = \left(\frac{\sin(\phi - \omega) + \sin\omega}{\sin(2\omega - \phi)}\right) \times 2^{27} \quad (4)$$

$\omega = 2\pi \times f_{LINE}/f_{DSP}$

where: f_{LINE} is the line frequency. f_{DSP} is 8 kHz.

Multipoint Phase and Gain Calibration

The ADE9000 allows multipoint gain and phase compensation with hysteresis on the IA, IB, and IC current channels. The current channel gain and phase compensation vary as a function of the calculated input current rms amplitude in xIRMS. There are five gain registers (xIGAIN0 to xIGAIN4) and five phase calibration registers (xPHCAL0 to xPHCAL4) for each channel. Set the MTEN bit in the CONFIG0 register to enable multipoint gain and phase calibration. MTEN = 0 by default.

The gain and phase calibration factor is applied based on the xIRMS current amplitude and the MTTHR_Lx and the MTTHR_Hx register values, as shown in Figure 59.

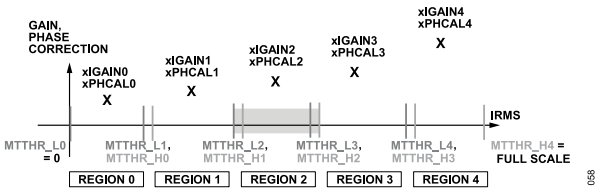

Figure 59. Multipoint Phase and Gain Calibration

Voltage Channel

The ADE9000 has three voltage channels. The datapaths for the VA, VB, and VC voltage channels is shown in Figure 60. The xVGAIN registers calibrate the voltage channel of each phase. The xVGAIN registers have the same scaling as the xIGAIN registers.

THEORY OF OPERATION

RMS and Power Measurements

The ADE9000 calculates total and fundamental values of rms current, rms voltage, active power, reactive power, and apparent power. The fundamental algorithm requires initialization of the network frequency using the SELFREQ bit in the ACCMODE register and the nominal voltage in the VLEVEL register. Calculate VLEVEL value according to the following equation:

VLEVEL = *x* × 1,144,084

where *x* is the dynamic range that the nominal input signal is at with respect to full scale.

For instance, if the signal is at ½ of full scale, x = 2.

VLEVEL = 2 × 1,144,084 = 2,288,168

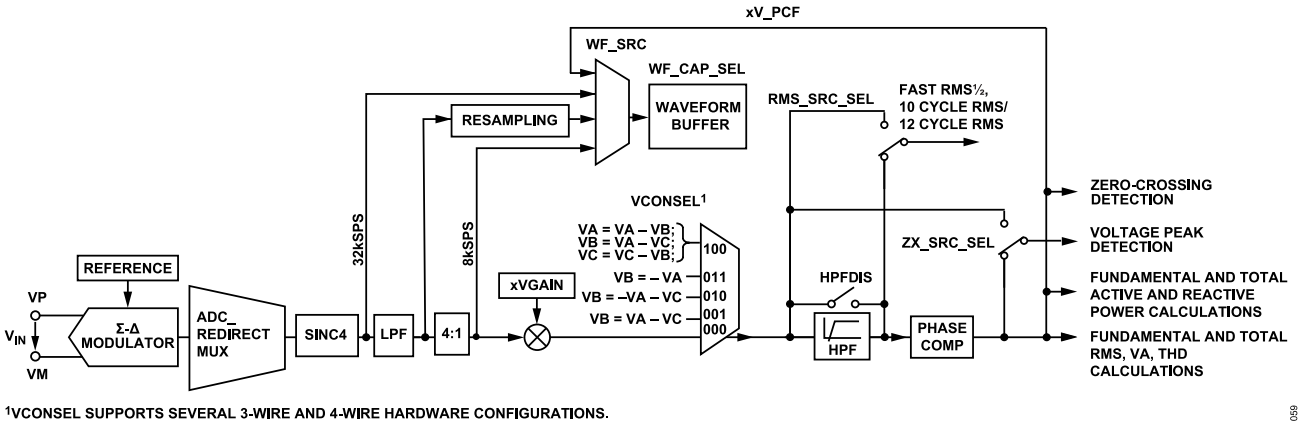

Figure 60. Voltage Channel Datapath

THEORY OF OPERATION

Total and Fundamental RMS

The ADE9000 offers total and fundamental current and voltage rms measurements on all phase channels. The datapath is shown in Figure 61.

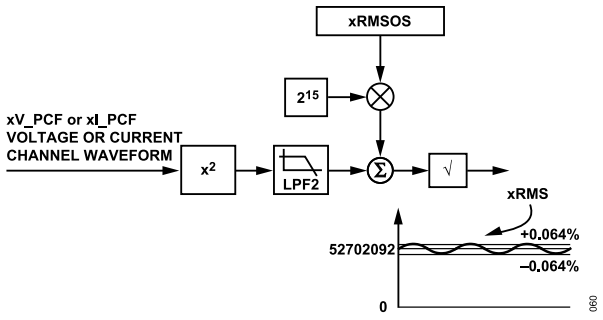

Figure 61. Filter-Based Total RMS

The total rms calculations, one for each channel (AIRMS, BIRMS, CIRMS, NIRMS, AVRMS, BVRMS, and CVRMS), are updated every 8 kSPS. The fundamental rms calculations available in the AIFRMS, BIFRMS, CIFRMS, AVFRMS, BVFRMS, and CVFRMS registers are also updated every 8 kSPS. The fundamental rms is not available for the neutral channel.

The xRMS and xFRMS value at full scale is 52,702,092 decimals.

The total and fundamental rms measurements can be calibrated for gain and offset. Perform gain calibration on the respective current and voltage channel datapath. The following equations indicate how the offset calibration registers modify the result in corresponding rms registers:

$$xRMS = \sqrt{xRMS_0{}^2 + 2^{15} \times xRMOSOS} \quad (5)$$

where $xRMS_0$ is the initial xRMS register value before offset calibration.

$$xFRMS = \sqrt{xFRMS_0{}^2 + 2^{15} \times xFRMOSOS} \quad (6)$$

The ADE9000 also calculates the rms of the sum of $I_A + I_B + I_C \pm I_N$ and stores the result in ISUMRMS. The ISUM_CFG bits in the CONFIG0 register configure the components included in summation.

Total and Fundamental Active Power

The ADE9000 offers total and fundamental active power measurements on all channels. To calculated the total active power for Phase A, see Figure 62.

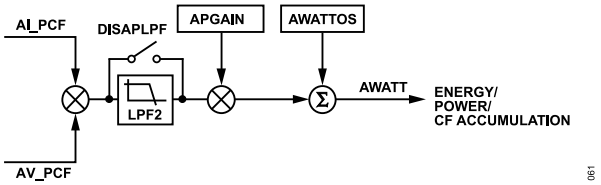

Figure 62. Total Active Power, AWATT, Calculation for Phase A

The active power calculations, one for each channel (AWATT, BWATT, and CWATT), are updated every 8 kSPS. The fundamental active power is also updated every 8 kSPS and is available in the AFWATT, BFWATT, and CFWATT registers. With full-scale inputs, the xWATT and xFWATT value is 20,694,066 decimals.

Enable the LPF2 (DISAPLPF = 0) for normal operation. Disable LFP2 by setting DISAPLPF in the CONFIG0 register to obtain instantaneous total active power. DISAPLPF is zero at reset.

The total and fundamental measurements can be calibrated for gain and offset. The following equations indicate how the gain and offset calibration registers modify the results in the corresponding power registers:

$$xWATT = \left(1 + \frac{xPGAIN}{2^{27}}\right) xWATT_0 + xWATTOS \quad (7)$$

$$xFWATT = \left(1 + \frac{xPGAIN}{2^{27}}\right) xFWATT_0 + xFWATTOS \quad (8)$$

xPGAIN is a common gain to total and fundamental components of active, reactive, and apparent powers.

Total and Fundamental Reactive Power

The ADE9000 offers total and fundamental reactive power measurements on all channels. Figure 63 shows how to perform the total reactive power calculation.

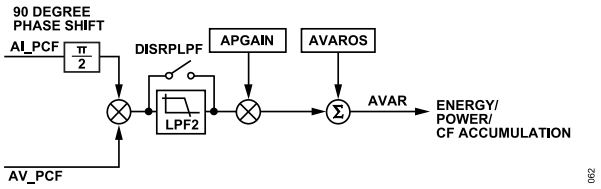

Figure 63. Total Reactive Power, AVAR, Calculation

The reactive power calculations, one for each channel (AVAR, BVAR, and CVAR) are updated every 8 kSPS. The fundamental reactive power is also updated every 8 kSPS and is available in the AFVAR, BFVAR, and CFVAR registers. With full-scale inputs, the xVAR and xFVAR value is 20,694,066.

Enable the LPF2 (DISRPLPF = 0) for normal operation. Disable LFP2 by setting DISRPLPF in the CONFIG0 register to obtain instantaneous total reactive power. DISRPLPF is 0 at reset.

THEORY OF OPERATION

The following equations indicate how the gain and offset calibration registers modify the result in the corresponding power registers:

$$xVAR = \left(1 + \frac{xPGAIN}{2^{27}}\right)xVAR_0 + xVAROS \quad (9)$$

$$xFVAR = \left(1 + \frac{xPGAIN}{2^{27}}\right)xFVAR_0 + xFVAROS \quad (10)$$

Total and Fundamental Apparent Power

The ADE9000 offers total and fundamental apparent power measurements on all channels. See Figure 64 for how to calculate the total apparent power for Phase A.

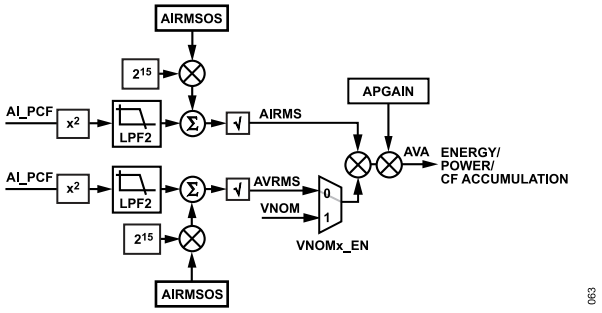

Figure 64. Total Apparent Power, AVA, Calculation for Phase A

The total apparent power calculations, one for each channel (AVA, BVA, and CVA) are updated every 8 kSPS. The fundamental apparent power is also updated every 8 kSPS and is available in the AFVA, BFVA and CFVA registers. With full-scale inputs, the xVA and xFVA value is 20,694,066 decimals.

The ADE9000 offers a register (VNOM) that can be set to a value to correspond to the desired voltage rms value. If the VNOMx_EN bits in the CONFIG0 register are set, VNOM multiplies by xIRMS when calculating xVA.

No Load Detection, Energy Accumulation, and Power Accumulation Features

The ADE9000 calculates the total and fundamental values of active, reactive, and apparent energy for all the three phases. The ADE9000 can have signed, absolute, positive, or negative only accumulation on active and reactive energies using the WATTACC and VARACC bits in the ACCMODE register. The default accumulation mode is signed.

No Load Detection Feature

The ADE9000 has a no load detection for each phase and energy to prevent energy accumulation due to noise. If the accumulated energy over the user defined time period is below the user defined threshold, zero energy is accumulated into the energy register. The NOLOAD_TMR bits in the EP_CFG register determine the no load time period and the ACT_NL_LVL, REACT_NL_LVL, and APP_NL_LVL registers contain the user defined no load threshold.

The no load status is available in the PHNOLOAD register, the $\overline{\text{IRQ1}}$ interrupt, and the $\overline{\text{EVENT}}$ pin.

Energy Accumulation

The energy is accumulated into a 42-bit signed internal energy register at 8 kSPS. The internal register can accumulate a user defined number of samples or half line cycles configured by EGY_TMR_MODE bit in the EP_CFG register. When half line cycle accumulation is enabled, configure the zero-crossing source using the ZX_SEL bits in the ZX_LP_SEL register. The number of samples or half line cycles is set in the EGY_TIME register. The maximum value of EGY_TIME is 8191d. With full-scale inputs, the internal register overflows in 13.3 sec. For a 50 Hz signal, EGY_TIME must be lower than 1329 decimals to prevent overflow during half line cycle accumulation.

After EGY_TIME + 1 samples or half line cycles, the EGYRDY bit is set in the STATUS0 register and the energy register is updated. The data from the internal energy register is added or latched to the user energy register depending on the EGY_LD_ACCUM bit setting in the EP_CFG register.

The energy register is signed and is 45 bits wide, split between two 32-bit registers, as shown in Figure 65. The user energy can reset on a read using the RD_RST_EN bit in the EP_CFG register. With full-scale inputs, the user energy register overflows in 106.3 sec.

THEORY OF OPERATION

Power Accumulation

The ADE9000 accumulates the total and fundamental values of active, reactive, and apparent power for all the three phases into respective xWATT_ACC and xFWATT_ACC, xVAR_ACC and xFVAR_ACC, and xVA_ACC, and xFVA_ACC 32-bit signed registers. The number of samples accumulated is set using the PWR_TIME register. The PWRRDY bit in the STATUS0 register is set after PWR_TIME + 1 samples accumulate at 8 kSPS. The maximum value of the PWR_TIME register is 8191 decimals, and the maximum power accumulation time is 1.024 sec.

The xSIGN bits in the PHSIGN register indicate the sign of accumulated powers over the PWR_TIME interval. The PWR_SIGN_SEL[1:0] bits allow the user to select whether the power sign change follows the total or fundamental energies. When sign of the accumulated power changes, the corresponding REVx bits in the STATUS0 register are set and $\overline{\text{IRQ0}}$ generates an interrupt.

The ADE9000 allows the user to accumulate total active power and VAR powers into separate positive and negative values into the PWATT_ACC and NWATT_ACC, and PVAR_ACC and NVAR_ACC registers. A new accumulation from zero begins when the power update interval set in PWR_TIMER elapses.

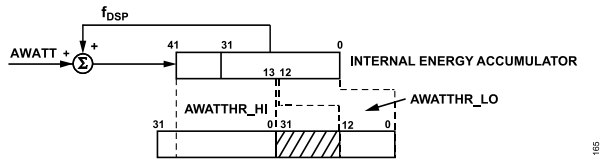

Figure 65. Internal Energy Register to AWATTHR_HI and AWATTHR_LO

Digital to Frequency Conversion—CFx Output

The ADE9000 includes four pulse outputs that are proportional to the energy accumulation in the CF1 through CF4 output pins. Figure 66 shows a block diagram of the CFx pulse generation. CF3 is multiplexed with ZX, and CF4 is multiplexed with $\overline{\text{EVENT}}$ and DREADY.

Energy and Phase Selection

The CFxSEL bits in the CFMODE register select which type of energy to output on the CFx pins. The TERMSELx bits in the COMPMODE register select which phase energies to include in the CFx output.

For example, with CF1SEL = 000 and TERMSEL1 = 111, CF1 indicates the total active power output of Phase A, Phase B, and Phase C.

Configuring the CFx Pulse Width

The value of the CFx_LT and the CF_LTMR bits in the CF_LCFG register determines the pulse width.

The maximum CFx with threshold (xTHR) = 0x00100000 and CFxDEN = 2 is 78.9 kHz. It is recommended to have xTHR = 0x00100000.

CFx Pulse Sign

The SUMxSIGN bits in the PHSIGN register indicate whether the sum of the energy that went into the last CFx pulse is positive or negative. The REVPSUMx bits in the STATUS0 register and the EVENT_STATUS register indicate if the CFx polarity changed sign. This feature generates an interrupt on $\overline{\text{IRQ0}}$.

Clearing the CFx Accumulator

To clear the accumulation in the digital to frequency converter and CFDEN counter, write 1 to the CF_ACC_CLR bit in the CONFIG1 register. The CF_ACC_CLR bit automatically clears itself.

THEORY OF OPERATION

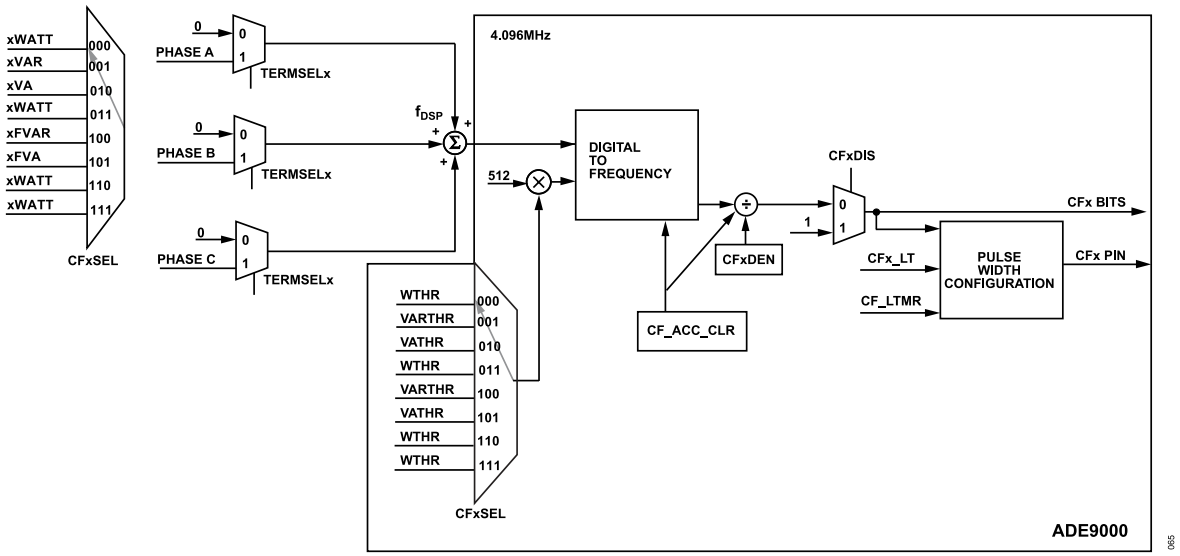

Figure 66. Digital to Frequency Conversion for CFx

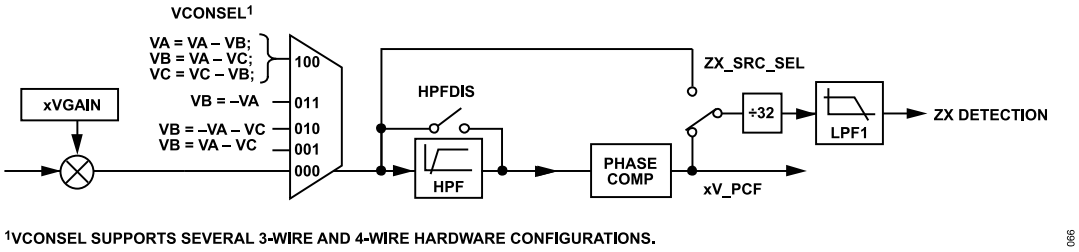

Figure 67. Voltage Channel Signal Chain Preceding Zero-Crossing Detection

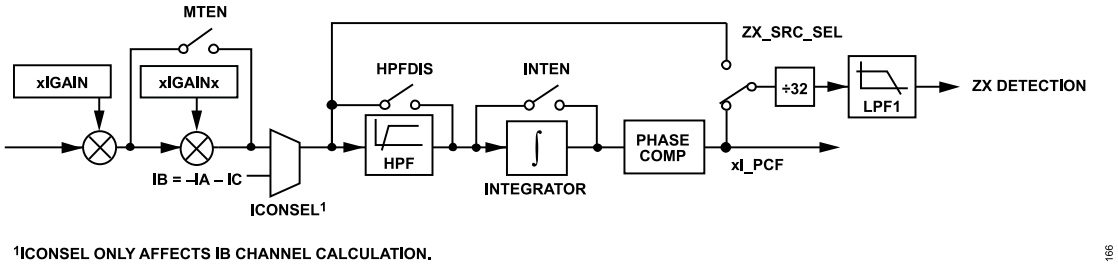

Figure 68. Current Channel Signal Chain Preceding Zero-Crossing Detection

THEORY OF OPERATION

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE9000 offers zero-crossing detection on the VA, VB, VC, IA, IB, and IC input signals. The neutral current channel, IN, does not contain a zero-crossing detection circuit. Figure 67 and Figure 68 show the current and voltage channel datapaths preceding zero-crossing detection.

Use the ZX_SRC_SEL bit in the CONFIG0 register to select data before the high-pass filter or after phase compensation to configure the inputs to zero-crossing detection. ZX_SRC_SEL is zero by default after reset.

To provide protection from noise, voltage channel zero-crossing events (ZXVA, ZXVB, and ZXVC) do not generate if the absolute value of the LPF1 output voltage is smaller than the threshold, ZXTHRSH. The current channel zero-crossing detection outputs (ZXIA, ZXIB, and ZXIC) are active for all input signals levels.

Calculate the zero-crossing threshold, ZXTHRSH, from the following equation:

ZXTHRSH =

$$\frac{(V\_PCF\ at\ Full\ Scale)\ \times\ (LPF1\ Attenuation)}{x\ \times\ 32\ \times\ 2^8} \quad (11)$$

where *V_PCF at Full Scale* is ±74,532,013 decimals. *LPF1 Attenuation* is 0.86 at 50 Hz, and 0.81 at 60 Hz. *x* is the dynamic range below which the voltage channel zero-crossing must be blocked.

The ADE9000 can calculate the combined zero crossings for all three phases as (V_A + V_B − V_C)/2 by configuring the ZX_SEL bits in the ZX_LP_SEL register. If VCONSEL is not equal to 0, the VB component in the combined zero-crossing circuit is set to zero.

The zero-crossing detection circuits have two different output rates: 8 kSPS and 1024 kSPS. The 8 kSPS zero-crossing signal calculates the line period, updates the ZXx bits in the STATUS1 register, and monitors the zero-crossing timeout, phase sequence error detection, resampling, and energy accumulation functions. The 1024 kSPS zero-crossing signal calculates the angle and updates the zero-crossing output on the CF3/ZX pin.

CF3/ZX

The CF3/ZX pin can output zero crossings using the CF3_CFG bit in the CONFIG1 register. To configure the source for zero crossing, use the ZX_SEL bits in ZX_LP_SEL register. The CF3/ZX output pin goes from low to high when a negative to positive transition is detected and from high to low when a positive to negative transition occurs.

Zero-Crossing Timeout

If a zero crossing is not received after (ZXTOUT + 1)/8000 sec, the corresponding ZXTOx bit in the STATUS1 register is set and generates an interrupt on the $\overline{IRQ1}$ pin.

Line Period Calculation

The ADE9000 calculates the line period for the Phase A, Phase B, and Phase C voltages, and the combined voltage signal, and the results are available in the APERIOD, BPERIOD, CPERIOD, and COM_PERIOD registers, respectively.

Calculate the line period, t_L, from the xPERIOD register, according to the following equation:

$$t_L = \frac{xPERIOD + 1}{8000 \times 2^{16}}\ (\text{sec}) \quad (12)$$

If the calculated period value is outside the range of 40 Hz to 70 Hz, or if zero crossings for that phase are not detected, the xPERIOD register is coerced to correspond to 50 Hz or 60 Hz, depending on SELFREQ bit in the ACCMODE register.

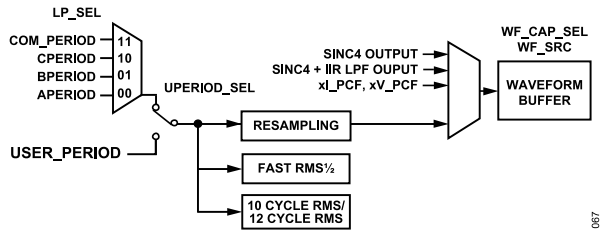

Figure 69. Line Period Selection for Resampling

Angle Measurement

The ADE9000 provides nine angle measurements. ANGL_IA_IB, ANGL_IB_IC, and ANGL_IA_IC provide phase angle between currents. ANGL_VA_VB, ANGL_VB_VC, and ANGL_VA_VC provide phase angle between voltages. ANGL_VA_IA, ANGL_VB_IB, and ANGL_VC_IC provide phase angle between voltage and currents. To convert angle register reading to degrees, use the following equations.

For a 50 Hz system,

$$Angle\ (Degrees) = ANGL_{\_x\_y} \times 0.017578125 \quad (13)$$

For a 60 Hz system,

$$Angle\ (Degrees) = ANGL_{\_x\_y} \times 0.02109375 \quad (14)$$

Phase Sequence Error Detection

The ADE9000 monitors phase sequences and sets the SEQERR bit in the STATUS1 register if a sequence error occurs or a phase drops below ZXTHRSH. SEQ_CYC determines the number of cycles to monitor to generate the sequence error. To generate an interrupt on $\overline{IRQ1}$, set the SEQERR bit in the MASK1 register.

THEORY OF OPERATION

Fast RMS½ Measurement

RMS½ is an rms measurement performed over one line cycle, updated every half cycle. This measurement is provided for voltage and current on all phases plus the neutral current. All the half cycle rms measurements are performed over the same time interval and update at the same time, as indicated by the RMSONERDY bit in the STATUS0 register. The results are stored in the AIRMSONE, BIRMSONE, CIRMSONE, NIRMSONE, AVRMSONE, BVRMSONE, and CVRMSONE registers. The xRMSONE register reading with full-scale inputs is 52,702,092d.

It is recommended to select the data before the high-pass filter for the fast rms measurement by setting the RMS_SRC_SEL bit in the CONFIG0 register.

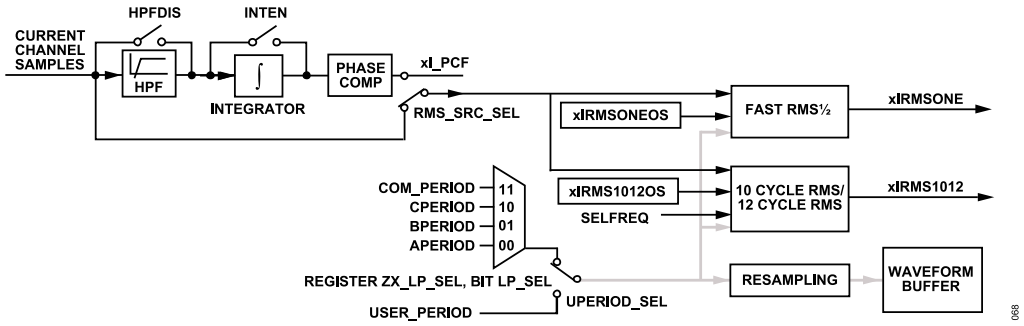

Figure 70. RMS½, 10 Cycle RMS, and 12 Cycle RMS Measurements

10 Cycle RMS/12 Cycle RMS

The 10 cycle rms/12 cycle rms measurement is performed over 10 cycles on a 50 Hz network or 12 cycles on a 60 Hz network. The SELFREQ bit in the ACCMODE register selects whether the network is 50 Hz or 60 Hz. Then, the UPERIOD_SEL bit in the CONFIG2 register selects whether to use a measured line period or a user configured value in the USER_PERIOD register to set the number of samples used in the calculation.

An offset correction register is available for improved performance with small input signal levels, xRMS1012OS. The xRMS1012 register reading with full-scale inputs is 52,702,092d.

The signal chain is shown in Figure 70.

Dip and Swell Indication

The ADE9000 monitors rms½ value on voltage channels to determine a dip and swell event. If the voltage goes below a threshold specified in the DIP_LVL register for a user configured number of half cycles in the DIP_CYC register, the corresponding DIPA, DIPB, and DIPC bits are set in the STATUS1 register. The minimum rms½ value measured during the dip is stored in the corresponding DIPA, DIPB, and DIPC registers.

Similarly, if the voltage goes above a threshold specified in the SWELL_LVL register for a user configured number of half cycles in the SWELL_CYC register, the corresponding SWELLA, SWELLB, and SWELLC bits are set in the STATUS1 register. The maximum rms½ value measured during the swell is stored in the corresponding SWELLA, SWELLB, and SWELLC registers.

The dip and swell event generates an interrupt on the $\overline{\text{IRQ1}}$ pin and also generates an event on the CF4/$\overline{\text{EVENT}}$/DREADY pin.

Overcurrent Indication

The ADE9000 monitors the rms½ value on current channels to determine overcurrent events. If a rms½ current is greater than the user configured threshold in the OILVL register, the OI bit in the STATUS1 register is set. The overcurrent event generates an interrupt on the $\overline{\text{IRQ1}}$ pin.

The OC_EN bits in the CONFIG3 register select which phases to monitor for overcurrent events. The OIPHASE bits in the OISTATUS register indicate which current channels exceeded the threshold. The overcurrent value is stored in the corresponding OIA, OIB, or OIC registers.

Peak Detection

The ADE9000 records the peak value measured on the current and voltage channels from the xI_PCF and xV_PCF waveforms. The PEAKSEL bits in the CONFIG3 register allow the user to select which phases to monitor.

The LP_SEL bits in the ZX_LP_SEL register select which line period measurement sets the number of samples used in the rms½ measurement. Alternatively, set the UPERIOD_SEL bit in the CONFIG2 register to set desired period in the USER_PERIOD register for line period measurement. An offset correction register is available for improved performance with small input signal levels, xRMSONEOS.

The signal chain is shown in Figure 70.

THEORY OF OPERATION

The IPEAK register stores the peak current value in the IPEAKVAL bits and indicates which phase currents reached the value in the IPPHASE bits. IPEAKVAL is equal to xI_PCF/2^5.

Similarly, VPEAK stores the peak voltage value in the VPEAKVAL bits. VPEAKVAL is equal to xV_PCF/2^5. After a read, the VPEAK and IPEAK registers reset.

Power Factor

The power factor calculation, one for each channel (APF, BPF, and CPF), is updated every 1.024 sec.

The sign of the APF calculation follows the sign of AWATT. To determine if power factor is leading or lagging, refer to the sign of the total or fundamental reactive energy and the sign of the xPF or xWATT value, as indicated in Figure 71.

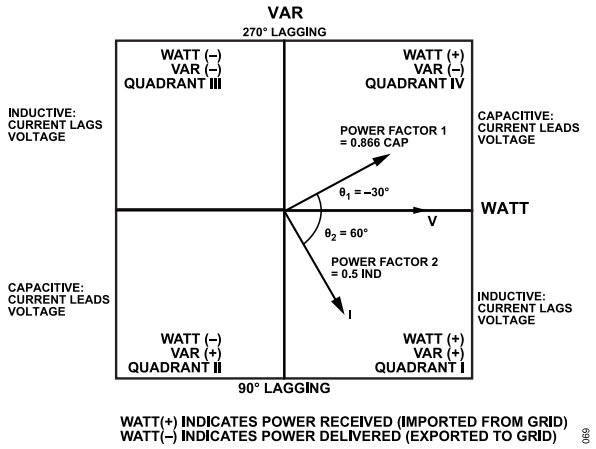

Figure 71. Active Power and VAR Sign for Capacitive and Inductive Loads

The power factor result is stored in 5.27 format. The highest power factor value is 0x0800 000, which corresponds to a power factor of 1. A power factor of −1 is stored as 0xF800 0000. To determine the power factor from the xPF register value, use the following equation:

$$Power\ Factor = xPF \times 2^{-27} \quad (15)$$

Total Harmonic Distortion (THD)

A THD calculation is available on the IA, IB, IC, VA, VB, and VC channels in the AITHD, BITHD, CITHD, AVTHD, BVTHD, and CVTHD registers, respectively. THD updates once every second.

The THD calculation is stored in signed 5.27 format. The highest THD value is 0x2000 0000, which corresponds to a THD of 400%. To calculate the THD value as a percentage, use the following equation:

$$\%THD\ on\ Current\ Channel\ A = AITHD \times 2^{-27} \times 100\ \% \quad (16)$$

Resampling 128 Points per Cycle

The ADE9000 resamples the input data to provide 128 points per line cycle, independent of the input line frequency. The resampled data is available for all current channels and voltage channels in the waveform buffer. Each resampled waveform sample is stored as a 16-bit signed integer in the waveform buffer.

The resampler supports line frequency of upto 62.5 Hz this is because the internal DSP that calculates the resample data runs at 8kHz.

$$Resampling\ rate_{max} = 8\,kHz/128 = 62.5\,Hz \quad (17)$$

Temperature

The temperature reading is available in the TEMP_RSLT register. To convert the temperature range into Celsius, use the following equation:

$$Temperature(℃) = TEMP\_RSLT \times (-TEMP\_GAIN/65536) + (TEMP\_OFFSET/32) \quad (18)$$

During manufacturing of each device, the TEMP_GAIN and TEMP_OFFSET bits of Register TEMP_TRIM are programed. To configure the temperature sensor, program the TEMP_CFG register.

WAVEFORM BUFFER

The ADE9000 has a waveform buffer comprised of 2048, 32-bit memory locations. To configure the data into the waveform buffer, use the WF_SRC and WF_CAP_SEL bits in the WFB_CFG register.

The data can come from the following four locations, as follows:

- Sinc4 outputs at 32 kSPS. The waveform buffer holds 8 ms of waveform data per channel.
- Sinc4 + IIR LPF output at 8 kSPS. The waveform buffer holds 32 ms of waveform data per channel.
- Current and voltage channel waveforms processed by the DSP at 8 kSPS. The waveform buffer holds 32 ms of waveform data per channel.
- Resampled waveforms with 128 points per line cycle processed by the DSP. The data rate varies with the line period. The waveform buffer holds 80 ms of waveform data per channel.

The waveform buffer offers the following different filling modes for use with fixed data rate samples:

- Stop when buffer is full
- Continuous filling

The ADE9000 allows a selection of events to trigger waveform buffer captures, and there is an option to store the current waveform buffer address during an event to allow the user to synchronize the event with the waveform samples. The following waveform buffer actions are associated with an event when the buffer is filling continuously:

- Stops filling on trigger
- Centers capture around trigger
- Saves the event address and keeps filling

Use the SPI burst read mode to read the waveform buffer contents. The default value bursts out all the channels in the waveform buffer.

The waveform buffer generates an interrupt on $\overline{\text{IRQ0}}$ after the last address is filled. The DSP must be on to use the waveform buffer.

INTERRUPTS/EVENTS

The ADE9000 has three pins ($\overline{IRQ0}$, $\overline{IRQ1}$, and CF4/$\overline{EVENT}$/ DREADY) that can be used as interrupts to the host processor. The $\overline{IRQ0}$ and $\overline{IRQ1}$ pins go low when an enabled interrupt occurs and stay low until the event is acknowledged by setting the corresponding status bit in the STATUS0 and STATUS1 registers, respectively. The bits in MASK0 and MASK1 configure respective interrupts. The $\overline{EVENT}$ function, which can multiplex with the CF4 and DREADY options, tracks the state of the enabled signals and goes low and high with these internal signals. The CF4_CFG bits in CONFIG1 register set the CF4/$\overline{EVENT}$/DREADY pin functionality. The CF4/$\overline{EVENT}$/ DREADY pin is useful for measuring the duration of events, such as dips or swells, externally.

ACCESSING ON-CHIP DATA

SPI PROTOCOL OVERVIEW

The ADE9000 has an SPI-compatible interface, consisting of four pins: SCLK, MOSI, MISO, and $\overline{SS}$. The ADE9000 is always an SPI slave; it never initiates SPI communication. The SPI interface is compatible with 16-bit and 32-bit read/write operations. The maximum serial clock frequency supported by this interface is 20 MHz.

The ADE9000 provides SPI burst read functionality on certain registers and the waveform buffer that allows multiple registers to be read after sending one CMD_HDR.

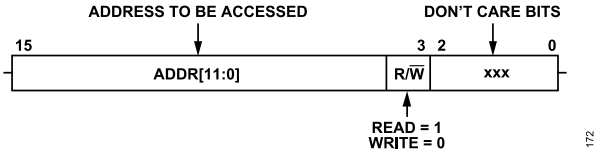

Figure 72. Command Header, CMD_HDR

The ADE9000 SPI port calculates a 16-bit cyclic redundancy check (CRC-16) of the data sent out on its MISO pin so that the integrity of the data received by the master can be checked. The CRC of the data sent out on the MISO pin during the last register read is offered in a 16-bit register, CRC_SPI, and can be appended to the SPI read data as part of the SPI transaction.

ADDITIONAL COMMUNICATION VERIFICATION REGISTERS

The ADE9000 includes three registers that allow SPI operation verification. The LAST_CMD (Address 0x4AE), LAST_DATA_16 (Address 0x4AC), and LAST_DATA_32 (Address 0x423) registers record the received CMD_HDR and the last read or transmitted data.

CRC OF CONFIGURATION REGISTERS

The configuration register CRC feature in the ADE9000 monitors certain external and internal register values. It also optionally includes 15 registers that are individually selectable in the CRC_OPTEN register. The result is stored in the CRC_RSLT register. The ADE9000 generates an interrupt on $\overline{IRQ1}$ if any of the monitored registers change the value of the CRC_RSLT register.

CONFIGURATION LOCK

The configuration lock feature prevents changes to the ADE9000 configuration. To enable this feature, write 0x3C64 to the WR_LOCK register. To disable the feature, write 0x4AD1.

To determine whether this feature is active, read the WR_LOCK register, which reads as 1 if the protection is enabled and 0 if it is disabled.

When this feature is enabled, it prevents writing to addresses from Address 0x000 to Address 0x073 and Address 0x400 to Address 0x4FE.

ERRATA

There is a bug in read with reset when using energy accumulation. Using linecyc or sample base accumulation is suggested. Register affected by this is RD_RST_EN, keep this register at the default value of 0.

REGISTER MAP

Table 6. Register Map

Address	Name	Description	Reset[1]	Access
0x000	AIGAIN	Phase A current gain adjust.	0x00000000	R/W
0x001	AIGAIN0	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x002	AIGAIN1	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x003	AIGAIN2	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x004	AIGAIN3	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x005	AIGAIN4	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x006	APHCAL0	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x007	APHCAL1	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x008	APHCAL2	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x009	APHCAL3	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x00A	APHCAL4	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x00B	AVGAIN	Phase A voltage gain adjust.	0x00000000	R/W
0x00C	AIRMSOS	Phase A current rms offset for the filter-based AIRMS calculation.	0x00000000	R/W
0x00D	AVRMSOS	Phase A voltage rms offset for the filter-based AVRMS calculation.	0x00000000	R/W
0x00E	APGAIN	Phase A power gain adjust for the AWATT, AVA, AVAR, AFWATT, AFVA, and AFVAR calculations.	0x00000000	R/W
0x00F	AWATTOS	Phase A total active power offset correction for the AWATT calculation.	0x00000000	R/W
0x010	AVAROS	Phase A total reactive power offset correction for the AVAR calculation.	0x00000000	R/W
0x011	AFWATTOS	Phase A fundamental active power offset correction for the AFWATT calculation.	0x00000000	R/W

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x012	AFVAROS	Phase A fundamental reactive power offset correction for the AFVAR calculation.	0x00000000	R/W
0x013	AIFRMSOS	Phase A current rms offset for the fundamental current rms, AIFRMS calculation.	0x00000000	R/W
0x014	AVFRMSOS	Phase A voltage rms offset for the fundamental voltage rms, AVFRMS calculation.	0x00000000	R/W
0x015	AVRMSONEOS	Phase A voltage rms offset for the fast rms½ AVRMSONE calculation.	0x00000000	R/W
0x016	AIRMSONEOS	Phase A current rms offset for the fast rms½ AIRMSONE calculation.	0x00000000	R/W
0x017	AVRMS1012OS	Phase A voltage rms offset for the 10 cycle rms/12 cycle rms AVRMS1012 calculation.	0x00000000	R/W
0x018	AIRMS1012OS	Phase A current rms offset for the 10 cycle rms/12 cycle rms AIRMS1012 calculation.	0x00000000	R/W
0x020	BIGAIN	Phase B current gain adjust.	0x00000000	R/W
0x021	BIGAIN0	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x022	BIGAIN1	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x023	BIGAIN2	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x024	BIGAIN3	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x025	BIGAIN4	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x026	BPHCAL0	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x027	BPHCAL1	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x028	BPHCAL2	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x029	BPHCAL3	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x02A	BPHCAL4	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x02B	BVGAIN	Phase B voltage gain adjust.	0x00000000	R/W
0x02C	BIRMSOS	Phase B current rms offset for the BIRMS calculation.	0x00000000	R/W
0x02D	BVRMSOS	Phase B voltage rms offset for the BVRMS calculation.	0x00000000	R/W
0x02E	BPGAIN	Phase B power gain adjust for the BWATT, BVA, BVAR, BFWATT, BFVA, and BFVAR calculations.	0x00000000	R/W
0x02F	BWATTOS	Phase B total active power offset correction for the BWATT calculation.	0x00000000	R/W
0x030	BVAROS	Phase B total reactive power offset correction for the BVAR calculation.	0x00000000	R/W
0x031	BFWATTOS	Phase B fundamental active power offset correction for the BFWATT calculation.	0x00000000	R/W
0x032	BFVAROS	Phase B fundamental reactive power offset correction for the BFVAR calculation.	0x00000000	R/W
0x033	BIFRMSOS	Phase B current rms offset for the fundamental current rms BIFRMS calculation.	0x00000000	R/W
0x034	BVFRMSOS	Phase B voltage rms offset for the fundamental voltage rms BVFRMS calculation.	0x00000000	R/W
0x035	BVRMSONEOS	Phase B voltage rms offset for the fast rms½ BVRMSONE calculation.	0x00000000	R/W
0x036	BIRMSONEOS	Phase B current rms offset for the fast rms½ BIRMSONE calculation.	0x00000000	R/W
0x037	BVRMS1012OS	Phase B voltage rms offset for the 10 cycle rms/12 cycle rms BVRMS1012 calculation.	0x00000000	R/W
0x038	BIRMS1012OS	Phase B current rms offset for the 10 cycle rms/12 cycle rms BVRMS1012 calculation.	0x00000000	R/W
0x040	CIGAIN	Phase C current gain adjust.	0x00000000	R/W
0x041	CIGAIN0	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x042	CIGAIN1	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x043	CIGAIN2	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x044	CIGAIN3	Phase C Multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x045	CIGAIN4	Phase C Multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x046	CPHCAL0	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x047	CPHCAL1	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x048	CPHCAL2	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x049	CPHCAL3	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint	0x00000000	R/W

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
		phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.		
0x04A	CPHCAL4	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x04B	CVGAIN	Phase C voltage gain adjust.	0x00000000	R/W
0x04C	CIRMSOS	Phase C current rms offset for the CIRMS calculation.	0x00000000	R/W
0x04D	CVRMSOS	Phase C voltage rms offset for the CVRMS calculation.	0x00000000	R/W
0x04E	CPGAIN	Phase C power gain adjust for the CWATT, CVA, CVAR, CFWATT, CFVA, and CFVAR calculations.	0x00000000	R/W
0x04F	CWATTOS	Phase C total active power offset correction for the CWATT calculation.	0x00000000	R/W
0x050	CVAROS	Phase C total reactive power offset correction for the CVAR calculation.	0x00000000	R/W
0x051	CFWATTOS	Phase C fundamental active power offset correction for the CFWATT calculation.	0x00000000	R/W
0x052	CFVAROS	Phase C fundamental reactive power offset correction for the CFVAR calculation.	0x00000000	R/W
0x053	CIFRMSOS	Phase C current rms offset for the fundamental current rms CIFRMS calculation.	0x00000000	R/W
0x054	CVFRMSOS	Phase C voltage rms offset for the fundamental voltage rms CVFRMS calculation.	0x00000000	R/W
0x055	CVRMSONEOS	Phase C voltage rms offset for the fast rms½ CVRMSONE calculation.	0x00000000	R/W
0x056	CIRMSONEOS	Phase C current rms offset for the fast rms½ CIRMSONE calculation.	0x00000000	R/W
0x057	CVRMS1012OS	Phase C voltage rms offset for the 10 cycle rms/12 cycle rms CVRMS1012 calculation.	0x00000000	R/W
0x058	CIRMS1012OS	Phase C current rms offset for the 10 cycle rms/12 cycle rms CIRMS1012 calculation.	0x00000000	R/W
0x060	CONFIG0	Configuration Register 0.	0x00000000	R/W
0x061	MTTHR_L0	Multipoint phase/gain threshold. If MTEN = 1 in the CONFIG0 register, the MTGNTHR_Lx and MTGNTHR_Hx registers set up the ranges in which to apply each set of corrections, allowing hysteresis. See the Multipoint Phase and Gain Calibration section for more information.	0x00000000	R/W
0x062	MTTHR_L1	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x063	MTTHR_L2	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x064	MTTHR_L3	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x065	MTTHR_L4	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x066	MTTHR_H0	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x067	MTTHR_H1	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x068	MTTHR_H2	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x069	MTTHR_H3	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x06A	MTTHR_H4	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x06B	NIRMSOS	Neutral current rms offset for the NIRMS calculation.	0x00000000	R/W
0x06C	ISUMRMSOS	Offset correction for the ISUMRMS calculation based on the sum of IA + IB + IC ± IN.	0x00000000	R/W
0x06D	NIGAIN	Neutral current gain adjust.	0x00000000	R/W
0x06E	NPHCAL	Neutral current phase compensation.	0x00000000	R/W
0x06F	NIRMSONEOS	Neutral current rms offset for the fast rms½ NIRMSONE calculation.	0x00000000	R/W
0x070	NIRMS1012OS	Neutral current rms offset for the 10 cycle rms/12 cycle rms NIRMS1012 calculation.	0x00000000	R/W
0x071	VNOM	Nominal phase voltage rms used in the computation of apparent power, xVA, when the VNOMx_EN bit is set in the CONFIG0 register.	0x00000000	R/W
0x072	DICOEFF	Value used in the digital integrator algorithm. If the integrator is turned on, with INTEN or ININTEN equal to one in the CONFIG0 register, it is recommended to set this value to 0xFFFFE000.	0x00000000	R/W
0x073	ISUMLVL	Threshold to compare ISUMRMS against. Configure this register to receive a MISMTCH indication in STATUS0 if ISUMRMS exceeds this threshold.	0x00000000	R/W
0x20A	AI_PCF	Instantaneous Phase A current channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x20B	AV_PCF	Instantaneous Phase A voltage channel waveform processed by the DSP at 8 kSPS.	0x00000000	R

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x20C	AIRMS	Phase A filter-based current rms value, updates at 8 kSPS.	0x00000000	R
0x20D	AVRMS	Phase A filter-based voltage rms value, updates at 8 kSPS.	0x00000000	R
0x20E	AIFRMS	Phase A current fundamental rms, updates at 8 kSPS.	0x00000000	R
0x20F	AVFRMS	Phase A voltage fundamental RMS, updates at 8 kSPS.	0x00000000	R
0x210	AWATT	Phase A low-pass filtered total active power, updated at 8 kSPS.	0x00000000	R
0x211	AVAR	Phase A low-pass filtered total reactive power, updated at 8 kSPS.	0x00000000	R
0x212	AVA	Phase A total apparent power, updated at 8 kSPS.	0x00000000	R
0x213	AFWATT	Phase A fundamental active power, updated at 8 kSPS.	0x00000000	R
0x214	AFVAR	Phase A fundamental reactive power, updated at 8 kSPS.	0x00000000	R
0x215	AFVA	Phase A fundamental apparent power, updated at 8 kSPS.	0x00000000	R
0x216	APF	Phase A power factor, updated every 1.024 sec.	0x00000000	R
0x217	AVTHD	Phase A voltage THD, updated every 1.024 sec.	0x00000000	R
0x218	AITHD	Phase A current THD, updated every 1.024 sec.	0x00000000	R
0x219	AIRMSONE	Phase A current fast rms½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x21A	AVRMSONE	Phase A voltage fast rms½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x21B	AIRMS1012	Phase A current fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x21C	AVRMS1012	Phase A voltage fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x21D	AMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, this register indicate which AIGAINx and APHCALx is currently being used.	0x0000000F	R
0x22A	BI_PCF	Instantaneous Phase B current channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x22B	BV_PCF	Instantaneous Phase B voltage channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x22C	BIRMS	Phase B filter-based current rms value, updates at 8 kSPS.	0x00000000	R
0x22D	BVRMS	Phase B filter-based voltage rms value, updates at 8 kSPS.	0x00000000	R
0x22E	BIFRMS	Phase B current fundamental rms, updates at 8 kSPS.	0x00000000	R
0x22F	BVFRMS	Phase B voltage fundamental rms, updates at 8 kSPS.	0x00000000	R
0x230	BWATT	Phase B low-pass filtered total active power, updated at 8 kSPS.	0x00000000	R
0x231	BVAR	Phase B low-pass filtered total reactive power, updated at 8 kSPS.	0x00000000	R
0x232	BVA	Phase B total apparent power, updated at 8 kSPS.	0x00000000	R
0x233	BFWATT	Phase B fundamental active power, updated at 8 kSPS.	0x00000000	R
0x234	BFVAR	Phase B fundamental reactive power, updated at 8 kSPS.	0x00000000	R
0x235	BFVA	Phase B fundamental apparent power, updated at 8 kSPS.	0x00000000	R
0x236	BPF	Phase B power factor, updated every 1.024 sec.	0x00000000	R
0x237	BVTHD	Phase B voltage THD, updated every 1.024 sec.	0x00000000	R
0x238	BITHD	Phase B current THD, updated every 1.024 sec.	0x00000000	R
0x239	BIRMSONE	Phase B current fast rms½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x23A	BVRMSONE	Phase B voltage fast rms½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x23B	BIRMS1012	Phase B current fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x23C	BVRMS1012	Phase B voltage fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x23D	BMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the COFIG0 register, this register indicate which BIGAINx and BPHCALx is currently being used.	0x0000000F	R
0x24A	CI_PCF	Instantaneous Phase C current channel waveform processed by the DSP at 8 kSPS.	0x00000000	R

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x24B	CV_PCF	Instantaneous Phase C voltage channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x24C	CIRMS	Phase C filter-based current rms value, updates at 8 kSPS.	0x00000000	R
0x24D	CVRMS	Phase C filter-based voltage rms value, updates at 8 kSPS.	0x00000000	R
0x24E	CIFRMS	Phase C current fundamental rms, updates at 8 kSPS.	0x00000000	R
0x24F	CVFRMS	Phase C voltage fundamental rms, updates at 8 kSPS.	0x00000000	R
0x250	CWATT	Phase C low-pass filtered total active power, updated at 8 kSPS.	0x00000000	R
0x251	CVAR	Phase C low-pass filtered total reactive power, updated at 8 kSPS.	0x00000000	R
0x252	CVA	Phase C total apparent power, updated at 8 kSPS.	0x00000000	R
0x253	CFWATT	Phase C fundamental active power, updated at 8 kSPS.	0x00000000	R
0x254	CFVAR	Phase C fundamental reactive power, updated at 8 kSPS.	0x00000000	R
0x255	CFVA	Phase C fundamental apparent power, updated at 8 kSPS.	0x00000000	R
0x256	CPF	Phase C power factor, updated every 1.024 sec.	0x00000000	R
0x257	CVTHD	Phase C voltage THD, updated every 1.024 sec.	0x00000000	R
0x258	CITHD	Phase C current total THD, updated every 1.024 sec.	0x00000000	R
0x259	CIRMSONE	Phase C current fast rms½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x25A	CVRMSONE	Phase C voltage fast rms½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x25B	CIRMS1012	Phase C current fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x25C	CVRMS1012	Phase C voltage fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x25D	CMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which CIGAINx and CPHCALx is currently being used.	0x0000000F	R
0x265	NI_PCF	Instantaneous neutral current channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x266	NIRMS	Neutral current filter-based rms value.	0x00000000	R
0x267	NIRMSONE	Neutral current fast rms½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x268	NIRMS1012	Neutral current fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x269	ISUMRMS	Filter-based rms based on the sum of IA + IB + IC ± IN.	0x00000000	R
0x26A	VERSION2	This register indicates the version of the metrology algorithms after the user writes run = 1 to start the measurements.	0x0000000C	R
0x2E4	AWATT_ACC_LO	Phase A accumulated total active power, LSB, Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2E5	AWATT_ACC_HI	Phase A accumulated total active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2E6	AWATTHR_LO	Phase A accumulated total active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x2E7	AWATTHR_HI	Phase A accumulated total active energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0X2EE	AVAR_ACC_LO	Phase A accumulated total reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2EF	AVAR_ACC_HI	Phase A accumulated total reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2F0	AVARHR_LO	Phase A accumulated total reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x2F1	AVARHR_HI	Phase A accumulated total reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x2F8	AVA_ACC_LO	Phase A accumulated total apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2F9	AVA_ACC_HI	Phase A accumulated total apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2FA	AVAHR_LO	Phase A accumulated total apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x2FB	AVAHR_HI	Phase A accumulated total apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x302	AFWATT_ACC_LO	Phase A accumulated fundamental active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x303	AFWATT_ACC_HI	Phase A accumulated fundamental active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x304	AFWATTHR_LO	Phase A accumulated fundamental active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x305	AFWATTHR_HI	Phase A accumulated fundamental active energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x30C	AFVAR_ACC_LO	Phase A accumulated fundamental reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x30D	AFVAR_ACC_HI	Phase A accumulated fundamental reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x30E	AFVARHR_LO	Phase A accumulated fundamental reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x30F	AFVARHR_HI	Phase A accumulated fundamental reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x316	AFVA_ACC_LO	Phase A accumulated fundamental apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x317	AFVA_ACC_HI	Phase A accumulated fundamental apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x318	AFVAHR_LO	Phase A accumulated fundamental apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x319	AFVAHR_HI	Phase A accumulated fundamental apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0X320	BWATT_ACC_LO	Phase B accumulated total active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x321	BWATT_ACC_HI	Phase B accumulated total active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x322	BWATTHR_LO	Phase B accumulated total active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x323	BWATTHR_HI	Phase B accumulated total active energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0X32A	BVAR_ACC_LO	Phase B accumulated total reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x0000000	R
0x32B	BVAR_ACC_HI	Phase B accumulated total reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x32C	BVARHR_LO	Phase B accumulated total reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x32D	BVARHR_HI	Phase B accumulated total reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0X334	BVA_ACC_LO	Phase B accumulated total apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x335	BVA_ACC_HI	Phase B accumulated total apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x336	BVAHR_LO	Phase B accumulated total apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x337	BVAHR_HI	Phase B accumulated total apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x33E	BFWATT_ACC_LO	Phase B accumulated fundamental active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x33F	BFWATT_ACC_HI	Phase B accumulated fundamental active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x340	BFWATTHR_LO	Phase B accumulated fundamental active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x341	BFWATTHR_HI	Phase B accumulated fundamental active energy, MSB. Updated according to the settings in EP_CFG and EGY_TIME registers.	0x00000000	R
0x348	BFVAR_ACC_LO	Phase B accumulated fundamental reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x349	BFVAR_ACC_HI	Phase B accumulated fundamental reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x34A	BFVARHR_LO	Phase B accumulated fundamental reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x34B	BFVARHR_HI	Phase B accumulated fundamental reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x352	BFVA_ACC_LO	Phase B accumulated fundamental apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x353	BFVA_ACC_HI	Phase B accumulated fundamental apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x354	BFVAHR_LO	Phase B accumulated fundamental apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x355	BFVAHR_HI	Phase B accumulated fundamental apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x35C	CWATT_ACC_LO	Phase C accumulated total active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x35D	CWATT_ACC_HI	Phase C accumulated total active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x35E	CWATTHR_LO	Phase C accumulated total active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x35F	CWATTHR_HI	Phase C accumulated total active energy, MSB. Updated according to the settings in the P_CFG and EGY_TIME registers.	0x00000000	R
0x366	CVAR_ACC_LO	Phase C accumulated total reactive power, LSB updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x367	CVAR_ACC_HI	Phase C accumulated total reactive power, MSB updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x368	CVARHR_LO	Phase C accumulated total reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x369	CVARHR_HI	Phase C accumulated total reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x370	CVA_ACC_LO	Phase C accumulated total apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x371	CVA_ACC_HI	Phase C accumulated total apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x372	CVAHR_LO	Phase C accumulated total apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x373	CVAHR_HI	Phase C accumulated total apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x37A	CFWATT_ACC_LO	Phase C accumulated fundamental active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x37B	CFWATT_ACC_HI	Phase C accumulated fundamental active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x37C	CFWATTHR_LO	Phase C accumulated fundamental active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x37D	CFWATTHR_HI	Phase C accumulated fundamental active energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x384	CFVAR_ACC_LO	Phase C accumulated fundamental reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x385	CFVAR_ACC_HI	Phase C accumulated fundamental reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x386	CFVARHR_LO	Phase C accumulated fundamental reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x387	CFVARHR_HI	Phase C accumulated fundamental reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x38E	CFVA_ACC_LO	Phase C accumulated fundamental apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x38F	CFVA_ACC_HI	Phase C accumulated fundamental apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x390	CFVAHR_LO	Phase C accumulated fundamental apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x391	CFVAHR_HI	Phase C accumulated fundamental apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x396	PWATT_ACC_LO	Accumulated positive total active power, LSB, from AWATT, BWATT, and CWATT registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x397	PWATT_ACC_HI	Accumulated positive total active power, MSB, from AWATT, BWATT, and CWATT registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x39A	NWATT_ACC_LO	Accumulated Negative total active power, LSB, from AWATT, BWATT, and CWATT registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x39B	NWATT_ACC_HI	Accumulated Negative total active power, MSB, from AWATT, BWATT, and CWATT registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x39E	PVAR_ACC_LO	Accumulated positive total reactive power, LSB, from AVAR, BVAR, and CVAR registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x39F	PVAR_ACC_HI	Accumulated positive total reactive power, MSB, from AVAR, BVAR, and CVAR registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x3A2	NVAR_ACC_LO	Accumulated Negative total reactive power, LSB, from AVAR, BVAR, and CVAR registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x3A3	NVAR_ACC_HI	Accumulated Negative total reactive power, MSB, from AVAR, BVAR, and CVAR registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x400	IPEAK	Current peak register.	0x00000000	R
0x401	VPEAK	Voltage peak register.	0x00000000	R
0x402	STATUS0	Status Register 0.	0x00000000	R/W
0x403	STATUS1	Status Register 1.	0x00000000	R/W
0x404	EVENT_STATUS	Event status register.	0x00000000	R
0x405	MASK0	Interrupt Enable Register 0.	0x00000000	R/W
0x406	MASK1	Interrupt Enable Register 1.	0x00000000	R/W
0x407	EVENT_MASK	Event enable register.	0x00000000	R/W
0x409	OILVL	Over current detection threshold level.	0x00FFFFFF	R/W
0x40A	OIA	Phase A overcurrent rms½ value. If a phase is enabled, with the OC_ENA bit set in the CONFIG3 register and AIRMSONE greater than the OILVL threshold, this value is updated.	0x00000000	R
0x40B	OIB	Phase B overcurrent rms½ value. If a phase is enabled, with the OC_ENB bit set in the CONFIG3 register and BIRMSONE greater than the OILVL threshold, this value is updated.	0x00000000	R
0x40C	OIC	Phase C overcurrent rms½ value. If a phase is enabled, with the OC_ENC bit set in the CONFIG3 register and CIRMSONE greater than the OILVL threshold, this value is updated.	0x00000000	R
0x40D	OIN	Neutral current overcurrent rms½ value. If enabled, with the OC_ENN bit set in the CONFIG3 register and NIRMSONE greater than the OILVL threshold, this value is updated.	0x00000000	R
0x40E	USER_PERIOD	User configured line period value used for resampling, fast rms½ and 10 cycle rms/ 12 cycle rms when the UPERIOD_SEL bit in the CONFIG2 register is set.	0x00500000	R/W
0x40F	VLEVEL	Register used in the algorithm that computes the fundamental active, reactive, and apparent powers as well as the fundamental IRMS and VRMS values.	0x00045D45	R/W
0x410	DIP_LVL	Voltage RMS½ dip detection threshold level.	0x00000000	R/W
0x411	DIPA	Phase A voltage rms½ value during a dip condition.	0x007FFFFF	R
0x412	DIPB	Phase B voltage rms½ value during a dip condition.	0x007FFFFF	R
0x413	DIPC	Phase C voltage rms½ value during a dip condition.	0x007FFFFF	R
0x414	SWELL_LVL	Voltage rms½ swell detection threshold level.	0x00FFFFFF	R/W
0x415	SWELLA	Phase A voltage rms½ value during a swell condition.	0x00000000	R
0x416	SWELLB	Phase B voltage rms½ value during a swell condition.	0x00000000	R
0x417	SWELLC	Phase C voltage rms½ value during a swell condition.	0x00000000	R
0x418	APERIOD	Line period on Phase A voltage.	0x00A00000	R

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x419	BPERIOD	Line period on Phase B voltage.	0x00A00000	R
0x41A	CPERIOD	Line period on Phase C voltage.	0x00A00000	R
0x41B	COM_PERIOD	Line period measurement on combined signal from Phase A, Phase B, and Phase C voltages.	0x00A00000	R
0x41C	ACT_NL_LVL	No load threshold in the total and fundamental active power datapath.	0x0000FFFF	R/W
0x41D	REACT_NL_LVL	No load threshold in the total and fundamental reactive power datapath.	0x0000FFFF	R/W
0x41E	APP_NL_LVL	No load threshold in the total and fundamental apparent power datapath.	0x0000FFFF	R/W
0x41F	PHNOLOAD	Phase no load register.	0x00000000	R
0x420	WTHR	Sets the maximum output rate from the digital to frequency converter for the total and fundamental active power for the CFx calibration pulse output. It is recommended to write WTHR = 0x0010_0000.	0x0000FFFF	R/W
0x421	VARTHR	Sets the maximum output rate from the digital to frequency converter for the total and fundamental reactive power for the CFx calibration pulse output. It is recommended to write VARTHR = 0x0010_0000.	0x0000FFFF	R/W
0x422	VATHR	Sets the maximum output rate from the digital to frequency converter for the total and fundamental apparent power for the CFx calibration pulse output. It is recommended to write VATHR = 0x0010_0000.	0x0000FFFF	R/W
0x423	LAST_DATA_32	This register holds the data read or written during the last 32-bit transaction on the SPI port.	0x00000000	R
0x424	ADC_REDIRECT	This register allows any ADC output to be redirected to any digital datapath.	0x001FFFFF	R/W
0x425	CF_LCFG	CFx calibration pulse width configuration register.	0x00000000	R/W
0x472	PART_ID	This register identifies the IC. If the ADE9000_ID bit = 1, the IC is the ADE9000.	0xXX1XXXXX[2]	R
0x474	TEMP_TRIM	Temperature sensor gain and offset, calculated during the manufacturing process.	0xXXXXXXXX	R
0x480	RUN	Write this register to 1 to start the measurements.	0x0000	R/W
0x481	CONFIG1	Configuration Register 1.	0x0000	R/W
0x482	ANGL_VA_VB	Time between positive to negative zero crossings on Phase A and Phase B voltages.	0x0000	R
0x483	ANGL_VB_VC	Time between positive to negative zero crossings on Phase B and Phase C voltages.	0x0000	R
0x484	ANGL_VA_VC	Time between positive to negative zero crossings on Phase A and Phase C voltages.	0x0000	R
0x485	ANGL_VA_IA	Time between positive to negative zero crossings on Phase A voltage and current.	0x0000	R
0x486	ANGL_VB_IB	Time between positive to negative zero crossings on Phase B voltage and current.	0x0000	R
0x487	ANGL_VC_IC	Time between positive to negative zero crossings on Phase C voltage and current.	0x0000	R
0x488	ANGL_IA_IB	Time between positive to negative zero crossings on Phase A and Phase B current.	0x0000	R
0x489	ANGL_IB_IC	Time between positive to negative zero crossings on Phase B and Phase C current.	0x0000	R
0x48A	ANGL_IA_IC	Time between positive to negative zero crossings on Phase A and Phase C current.	0x0000	R
0x48B	DIP_CYC	Voltage rms½ dip detection cycle configuration.	0xFFFF	R/W
0x48C	SWELL_CYC	Voltage rms½ swell detection cycle configuration.	0xFFFF	R/W
0x48F	OISTATUS	Overcurrent status register.	0x0000	R
0x490	CFMODE	CFx configuration register.	0x0000	R/W
0x491	COMPMODE	Computation mode register.	0x0000	R/W
0x492	ACCMODE	Accumulation mode register.	0x0000	R/W
0x493	CONFIG3	Configuration Register 3.	0xF000	R/W
0x494	CF1DEN	CF1 denominator register.	0xFFFF	R/W
0x495	CF2DEN	CF2 denominator register.	0xFFFF	R/W
0x496	CF3DEN	CF3 denominator register.	0xFFFF	R/W
0x497	CF4DEN	CF4 denominator register.	0xFFFF	R/W
0x498	ZXTOUT	Zero-crossing timeout configuration register.	0xFFFF	R/W
0x499	ZXTHRSH	Voltage channel zero-crossing threshold register.	0x0009	R/W
0x49A	ZX_LP_SEL	This register selects which zero crossing and which line period measurement are used for other calculations.	0x001E	R/W

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x49C	SEQ_CYC	Number of line cycles used for phase sequence detection. It is recommended to set this register to 1.	0x00FF	R/W
0x49D	PHSIGN	Power sign register.	0x0000	R
0x4A0	WFB_CFG	Waveform buffer configuration register.	0x0000	R/W
0x4A1	WFB_PG_IRQEN	This register enables interrupts to occur after specific pages of the waveform buffer are filled.	0x0000	R/W
0x4A2	WFB_TRG_CFG	This register enables events to trigger a capture in the waveform buffer.	0x0000	R/W
0x4A3	WFB_TRG_STAT	This register indicates the last page that was filled in the waveform buffer and the location of trigger events.	0x0000	R/W
0x4A8	CRC_RSLT	This register holds the CRC of the configuration registers.	0x0000	R
0x4A9	CRC_SPI	This register holds the 16-bit CRC of the data sent out on the MOSI pin during the last SPI register read.	0x0000	R
0x4AC	LAST_DATA_16	This register holds the data read or written during the last 16-bit transaction on the SPI port.	0x0000	R
0x4AE	LAST_CMD	This register holds the address and read/write operation request (CMD_HDR) for the last transaction on the SPI port.	0x0000	R
0x4AF	CONFIG2	Configuration Register 2.	0x0C00	R/W
0x4B0	EP_CFG	Energy and power accumulation configuration.	0x0000	R/W
0x4B1	PWR_TIME	Power update time configuration.	0x00FF	R/W
0x4B2	EGY_TIME	Energy accumulation update time configuration.	0x00FF	R/W
0x4B4	CRC_FORCE	This register forces an update of the CRC of configuration registers.	0x0000	R/W
0x4B5	CRC_OPTEN	This register selects which registers are optionally included in the configuration register CRC feature.	0x0000	R/W
0x4B6	TEMP_CFG	Temperature sensor configuration register.	0x0000	R/W
0x4B7	TEMP_RSLT	Temperature measurement result.	0x0000	R
0x4B9	PGA_GAIN	This register configures the PGA gain for each ADC.	0x0000	R/W
0x4BA	CHNL_DIS	ADC channel enable/disable.	0x0000	R/W
0x4BF	WR_LOCK	This register enables the configuration lock feature.	0x0000	R/W
0x4E0	VAR_DIS	Enables/disables total reactive power calculation.	0x0000	R/W
0x4F0	RESERVED1	This register is reserved.	0x0000	R
0x4FE	Version	Version of ADE9000 IC. Use Logical AND 16-bit value with 0xFFC0 to obtain the current version. The current version is 0x00C0.	0x00FE	R
0x500	AI_SINC_DAT	Current channel A ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x501	AV_SINC_DAT	Voltage channel A ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x502	BI_SINC_DAT	Current channel B ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x503	BV_SINC_DAT	Voltage channel B ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x504	CI_SINC_DAT	Current channel C ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x505	CV_SINC_DAT	Voltage channel C ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x506	NI_SINC_DAT	Neutral current channel ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x510	AI_LPF_DAT	Current channel A ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x511	AV_LPF_DAT	Voltage channel A ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x512	BI_LPF_DAT	Current channel B ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x513	BV_LPF_DAT	Voltage channel B ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x514	CI_LPF_DAT	Current channel C ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x515	CV_LPF_DAT	Voltage channel C ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x516	NI_LPF_DAT	Neutral current channel ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x600	AV_PCF_1	SPI burst read accessible. Registers organized functionally. See AV_PCF.	0x00000000	R/W
0x601	BV_PCF_1	SPI burst read accessible. Registers organized functionally. See BV_PCF.	0x00000000	R/W
0x602	CV_PCF_1	SPI burst read accessible. Registers organized functionally. See CV_PCF.	0x00000000	R/W
0x603	NI_PCF_1	SPI burst read accessible. Registers organized functionally. See NI_PCF.	0x00000000	R/W

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x604	AI_PCF_1	SPI burst read accessible. Registers organized functionally. See AI_PCF.	0x00000000	R/W
0x605	BI_PCF_1	SPI burst read accessible. Registers organized functionally. See BI_PCF.	0x00000000	R/W
0x606	CI_PCF_1	SPI burst read accessible. Registers organized functionally. See CI_PCF.	0x00000000	R/W
0x607	AIRMS_1	SPI burst read accessible. Registers organized functionally. See AIRMS.	0x00000000	R/W
0x608	BIRMS_1	SPI burst read accessible. Registers organized functionally. See BIRMS.	0x00000000	R/W
0x609	CIRMS_1	SPI burst read accessible. Registers organized functionally. See CIRMS.	0x00000000	R/W
0x60A	AVRMS_1	SPI burst read accessible. Registers organized functionally. See AVRMS.	0x00000000	R/W
0x60B	BVRMS_1	SPI burst read accessible. Registers organized functionally. See BVRMS.	0x00000000	R/W
0x60C	CVRMS_1	SPI burst read accessible. Registers organized functionally. See CVRMS.	0x00000000	R/W
0x60D	NIRMS_1	SPI burst read accessible. Registers organized functionally. See NIRMS.	0x00000000	R/W
0x60E	AWATT_1	SPI burst read accessible. Registers organized functionally. See AWATT.	0x00000000	R/W
0x60F	BWATT_1	SPI burst read accessible. Registers organized functionally. See BWATT.	0x00000000	R/W
0x610	CWATT_1	SPI burst read accessible. Registers organized functionally. See CWATT.	0x00000000	R/W
0x611	AVA_1	SPI burst read accessible. Registers organized functionally. See AVA.	0x00000000	R/W
0x612	BVA_1	SPI burst read accessible. Registers organized functionally. See BVA.	0x00000000	R/W
0x613	CVA_1	SPI burst read accessible. Registers organized functionally. See CVA.	0x00000000	R/W
0x614	AVAR_1	SPI burst read accessible. Registers organized functionally. See AVAR.	0x00000000	R/W
0x615	BVAR_1	SPI burst read accessible. Registers organized functionally. See BVAR.	0x00000000	R/W
0x616	CVAR_1	SPI burst read accessible. Registers organized functionally. See CVAR.	0x00000000	R/W
0x617	AFVAR_1	SPI burst read accessible. Registers organized functionally. See AFVAR.	0x00000000	R/W
0x618	BFVAR_1	SPI burst read accessible. Registers organized functionally. See BFVAR.	0x00000000	R/W
0x619	CFVAR_1	SPI burst read accessible. Registers organized functionally. See CFVAR.	0x00000000	R/W
0x61A	APF_1	SPI burst read accessible. Registers organized functionally. See APF.	0x00000000	R/W
0x61B	BPF_1	SPI burst read accessible. Registers organized functionally. See BPF.	0x00000000	R/W
0x61C	CPF_1	SPI burst read accessible. Registers organized functionally. See CPF.	0x00000000	R/W
0x61D	AVTHD_1	SPI burst read accessible. Registers organized functionally. See AVTHD.	0x00000000	R/W
0x61E	BVTHD_1	SPI burst read accessible. Registers organized functionally. See BVTHD.	0x00000000	R/W
0x61F	CVTHD_1	SPI burst read accessible. Registers organized functionally. See CVTHD.	0x00000000	R/W
0x620	AITHD_1	SPI burst read accessible. Registers organized functionally. See AITHD.	0x00000000	R/W
0x621	BITHD_1	SPI burst read accessible. Registers organized functionally. See BITHD.	0x00000000	R/W
0x622	CITHD_1	SPI burst read accessible. Registers organized functionally. See CITHD.	0x00000000	R/W
0x623	AFWATT_1	SPI burst read accessible. Registers organized functionally. See AFWATT.	0x00000000	R/W
0x624	BFWATT_1	SPI burst read accessible. Registers organized functionally. See BFWATT.	0x00000000	R/W
0x625	CFWATT_1	SPI burst read accessible. Registers organized functionally. See CFWATT.	0x00000000	R/W
0x626	AFVA_1	SPI burst read accessible. Registers organized functionally. See AFVA.	0x00000000	R/W
0x627	BFVA_1	SPI burst read accessible. Registers organized functionally. See BFVA.	0x00000000	R/W
0x628	CFVA_1	SPI burst read accessible. Registers organized functionally. See CFVA.	0x00000000	R/W
0x629	AFIRMS_1	SPI burst read accessible. Registers organized functionally. See AFIRMS.	0x00000000	R/W
0x62A	BFIRMS_1	SPI burst read accessible. Registers organized functionally. See BFIRMS.	0x00000000	R/W
0x62B	CFIRMS_1	SPI burst read accessible. Registers organized functionally. See CFIRMS.	0x00000000	R/W
0x62C	AFVRMS_1	SPI burst read accessible. Registers organized functionally. See AFVRMS.	0x00000000	R/W
0x62D	BFVRMS_1	SPI burst read accessible. Registers organized functionally. See BFVRMS.	0x00000000	R/W
0x62E	CFVRMS_1	SPI burst read accessible. Registers organized functionally. See CFVRMS.	0x00000000	R/W
0x62F	AIRMSONE_1	SPI burst read accessible. Registers organized functionally. See AIRMSONE.	0x00000000	R/W
0x630	BIRMSONE_1	SPI burst read accessible. Registers organized functionally. See BIRMSONE.	0x00000000	R/W
0x631	CIRMSONE_1	SPI burst read accessible. Registers organized functionally. See CIRMSONE.	0x00000000	R/W
0x632	AVRMSONE_1	SPI burst read accessible. Registers organized functionally. See AVRMSONE.	0x00000000	R/W

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x633	BVRMSONE_1	SPI burst read accessible. Registers organized functionally. See BVRMSONE.	0x00000000	R/W
0x634	CVRMSONE_1	SPI burst read accessible. Registers organized functionally. See CVRMSONE.	0x00000000	R/W
0x635	NIRMSONE_1	SPI burst read accessible. Registers organized functionally. See NIRMSONE.	0x00000000	R/W
0x636	AIRMS1012_1	SPI burst read accessible. Registers organized functionally. See AIRMS1012.	0x00000000	R/W
0x637	BIRMS1012_1	SPI burst read accessible. Registers organized functionally. See BIRMS1012.	0x00000000	R/W
0x638	CIRMS1012_1	SPI burst read accessible. Registers organized functionally. See CIRMS1012.	0x00000000	R/W
0x639	AVRMS1012_1	SPI burst read accessible. Registers organized functionally. See AVRMS1012.	0x00000000	R/W
0x63A	BVRMS1012_1	SPI burst read accessible. Registers organized functionally. See BVRMS1012.	0x00000000	R/W
0x63B	CVRMS1012_1	SPI burst read accessible. Registers organized functionally. See CVRMS1012.	0x00000000	R/W
0x63C	NIRMS1012_1	SPI burst read accessible. Registers organized functionally. See NIRMS1012.	0x00000000	R/W
0x680	AV_PCF_2	SPI burst read accessible. Registers organized by phase. See AV_PCF.	0x00000000	R/W
0x681	AI_PCF_2	SPI burst read accessible. Registers organized by phase. See AI_PCF.	0x00000000	R/W
0x682	AIRMS_2	SPI burst read accessible. Registers organized by phase. See AIRMS.	0x00000000	R/W
0x683	AVRMS_2	SPI burst read accessible. Registers organized by phase. See AVRMS.	0x00000000	R/W
0x684	AWATT_2	SPI burst read accessible. Registers organized by phase. See AWATT.	0x00000000	R/W
0x685	AVA_2	SPI burst read accessible. Registers organized by phase. See AVA.	0x00000000	R/W
0x686	AVAR_2	SPI burst read accessible. Registers organized by phase. See AVAR.	0x00000000	R/W
0x687	AFVAR_2	SPI burst read accessible. Registers organized by phase. See AFVAR.	0x00000000	R/W
0x688	APF_2	SPI burst read accessible. Registers organized by phase. See APF.	0x00000000	R/W
0x689	AVTHD_2	SPI burst read accessible. Registers organized by phase. See AVTHD.	0x00000000	R/W
0x68A	AITHD_2	SPI burst read accessible. Registers organized by phase. See AITHD.	0x00000000	R/W
0x68B	AFWATT_2	SPI burst read accessible. Registers organized by phase. See AFWATT.	0x00000000	R/W
0x68C	AFVA_2	SPI burst read accessible. Registers organized by phase. See AFVA.	0x00000000	R/W
0x68D	AFIRMS_2	SPI burst read accessible. Registers organized by phase. See AFIRMS.	0x00000000	R/W
0x68E	AFVRMS_2	SPI burst read accessible. Registers organized by phase. See AFVRMS.	0x00000000	R/W
0x68F	AIRMSONE_2	SPI burst read accessible. Registers organized by phase. See AIRMSONE.	0x00000000	R/W
0x690	AVRMSONE_2	SPI burst read accessible. Registers organized by phase. See AVRMSONE.	0x00000000	R/W
0x691	AIRMS1012_2	SPI burst read accessible. Registers organized by phase. See AIRMS1012.	0x00000000	R/W
0x692	AVRMS1012_2	SPI burst read accessible. Registers organized by phase. See AVRMS1012.	0x00000000	R/W
0x693	BV_PCF_2	SPI burst read accessible. Registers organized by phase. See BV_PCF.	0x00000000	R/W
0x694	BI_PCF_2	SPI burst read accessible. Registers organized by phase. See BI_PCF.	0x00000000	R/W
0x695	BIRMS_2	SPI burst read accessible. Registers organized by phase. See BIRMS.	0x00000000	R/W
0x696	BVRMS_2	SPI burst read accessible. Registers organized by phase. See BVRMS.	0x00000000	R/W
0x697	BWATT_2	SPI burst read accessible. Registers organized by phase. See BWATT.	0x00000000	R/W
0x698	BVA_2	SPI burst read accessible. Registers organized by phase. See BVA.	0x00000000	R/W
0x699	BVAR_2	SPI burst read accessible. Registers organized by phase. See BVAR.	0x00000000	R/W
0x69A	BFVAR_2	SPI burst read accessible. Registers organized by phase. See BFVAR.	0x00000000	R/W
0x69B	BPF_2	SPI burst read accessible. Registers organized by phase. See BPF.	0x00000000	R/W
0x69C	BVTHD_2	SPI burst read accessible. Registers organized by phase. See BVTHD.	0x00000000	R/W
0x69D	BITHD_2	SPI burst read accessible. Registers organized by phase. See BITHD.	0x00000000	R/W
0x69E	BFWATT_2	SPI burst read accessible. Registers organized by phase. See BFWATT.	0x00000000	R/W
0x69F	BFVA_2	SPI burst read accessible. Registers organized by phase. See BFVA.	0x00000000	R/W
0x6A0	BFIRMS_2	SPI burst read accessible. Registers organized by phase. See BFIRMS.	0x00000000	R/W
0x6A1	BFVRMS_2	SPI burst read accessible. Registers organized by phase. See BFVRMS.	0x00000000	R/W
0x6A2	BIRMSONE_2	SPI burst read accessible. Registers organized by phase. See BIRMSONE.	0x00000000	R/W
0x6A3	BVRMSONE_2	SPI burst read accessible. Registers organized by phase. See BVRMSONE.	0x00000000	R/W
0x6A4	BIRMS1012_2	SPI burst read accessible. Registers organized by phase. See BIRMS1012.	0x00000000	R/W

REGISTER MAP

Table 6. Register Map (Continued)

Address	Name	Description	Reset[1]	Access
0x6A5	BVRMS1012_2	SPI burst read accessible. Registers organized by phase. See BVRMS1012.	0x00000000	R/W
0x6A6	CV_PCF_2	SPI burst read accessible. Registers organized by phase. See CV_PCF.	0x00000000	R/W
0x6A7	CI_PCF_2	SPI burst read accessible. Registers organized by phase. See CI_PCF.	0x00000000	R/W
0x6A8	CIRMS_2	SPI burst read accessible. Registers organized by phase. See CIRMS.	0x00000000	R/W
0x6A9	CVRMS_2	SPI burst read accessible. Registers organized by phase. See CVRMS.	0x00000000	R/W
0x6AA	CWATT_2	SPI burst read accessible. Registers organized by phase. See CWATT.	0x00000000	R/W
0x6AB	CVA_2	SPI burst read accessible. Registers organized by phase. See CVA.	0x00000000	R/W
0x6AC	CVAR_2	SPI burst read accessible. Registers organized by phase. See CVAR.	0x00000000	R/W
0x6AD	CFVAR_2	SPI burst read accessible. Registers organized by phase. See CFVAR.	0x00000000	R/W
0x6AE	CPF_2	SPI burst read accessible. Registers organized by phase. See CPF.	0x00000000	R/W
0x6AF	CVTHD_2	SPI burst read accessible. Registers organized by phase. See CVTHD.	0x00000000	R/W
0x6B0	CITHD_2	SPI burst read accessible. Registers organized by phase. See CITHD.	0x00000000	R/W
0x6B1	CFWATT_2	SPI burst read accessible. Registers organized by phase. See CFWATT.	0x00000000	R/W
0x6B2	CFVA_2	SPI burst read accessible. Registers organized by phase. See CFVA.	0x00000000	R/W
0x6B3	CFIRMS_2	SPI burst read accessible. Registers organized by phase. See CFIRMS.	0x00000000	R/W
0x6B4	CFVRMS_2	SPI burst read accessible. Registers organized by phase. See CFVRMS.	0x00000000	R/W
0x6B5	CIRMSONE_2	SPI burst read accessible. Registers organized by phase. See CIRMSONE.	0x00000000	R/W
0x6B6	CVRMSONE_2	SPI burst read accessible. Registers organized by phase. See CVRMSONE.	0x00000000	R/W
0x6B7	CIRMS1012_2	SPI burst read accessible. Registers organized by phase. See CIRMS1012.	0x00000000	R/W
0x6B8	CVRMS1012_2	SPI burst read accessible. Registers organized by phase. See CVRMS1012.	0x00000000	R/W
0x6B9	NI_PCF_2	SPI burst read accessible. Registers organized by phase. See NI_PCF.	0x00000000	R/W
0x6BA	NIRMS_2	SPI burst read accessible. Registers organized by phase. See NIRMS.	0x00000000	R/W
0x6BB	NIRMSONE_2	SPI burst read accessible. Registers organized by phase. See NIRMSONE.	0x00000000	R/W
0x6BC	NIRMS1012_2	SPI burst read accessible. Registers organized by phase. See NIRMS1012.	0x00000000	R/W

[1] Not valid until run bit is set.

[2] The default value is unique to every individual IC.

REGISTER DETAILS

Table 7 details the registers of the ADE9000 that have bit fields. Additional registers listed in Table 6 do not have bit fields.

Table 7. Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
0x060	CONFIG0	[31:14]	RESERVED		Reserved.	0x0	R
		13	DISRPLPF		Set this bit to disable the low-pass filter in the total reactive power datapath.	0x0	R/W
		12	DISAPLPF		Set this bit to disable the low-pass filter in the total active power datapath.	0x0	R/W
		11	ININTEN		Set this bit to enable the digital integrator in the neutral current channel.	0x0	R/W
		10	VNOMC_EN		Set this bit to use the nominal phase voltage rms, V_{NOM}, in the computation of Phase C total apparent power, CVA.	0x0	R/W
		9	VNOMB_EN		Set this bit to use the nominal phase voltage rms, V_{NOM}, in the computation of Phase B total apparent power, BVA.	0x0	R/W
		8	VNOMA_EN		Set this bit to use the nominal phase voltage rms, V_{NOM}, in the computation of Phase A total apparent power, AVA.	0x0	R/W
		7	RMS_SRC_SEL		This bit selects which samples are used for the rms½ and 10 cycle rms/12 cycle rms calculation.	0x0	R/W
				0	xI_PCF waveforms, after the high-pass filter and integrator.		
				1	ADC samples, before the high-pass filter and integrator.		
		6	ZX_SRC_SEL		This bit selects whether data going into the zero-crossing detection circuit comes before the high-pass filter, integrator, and phase compensation or afterwards.	0x0	R/W
				0	After the high-pass filter, integrator, and phase compensation.		
				1	Before the high-pass filter, integrator, and phase compensation.		
		5	INTEN		Set this bit to enable the integrators in the phase current channels. The neutral current channel integrator is managed by the ININTEN bit in the CONFIG0 register.	0x0	R/W
		4	MTEN		Set this bit to enable multipoint phase and gain compensation. If enabled, an additional gain factor, xIGAIN0 through xIGAIN5, is applied to the current channel based on the xIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x0	R/W
		3	HPFDIS		Set this bit to disable high-pass filters in all the voltage and current channels.	0x0	R/W
		2	RESERVED		Reserved.	0x0	R
		[1:0]	ISUM_CFG		ISUM calculation configuration.	0x0	R/W
				00	ISUM = AI_PCF + BI_PCF + CI_PCF (for approximated neutral current rms calculation).		
				01	ISUM = AI_PCF + BI_PCF + CI_PCF + NI_PCF (to determine mismatch between neutral and phase currents).		
				10	ISUM = AI_PCF + BI_PCF + CI_PCF − NI_PCF (to determine mismatch between neutral and phase currents).		
				11	ISUM = AI_PCF + BI_PCF + CI_PCF (for approximated neutral current rms calculation).		
0x21D	AMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	AREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits	0xF	R

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
					indicate which AIGAINx and APHCALx is currently being used		
				0000	AIGAIN0, APHCAL0.		
				0001	AIGAIN1, APHCAL1.		
				0010	AIGAIN2, APHCAL2.		
				0011	AIGAIN3, APHCAL3.		
				0100	AIGAIN4, APHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x23D	BMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	BREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which BIGAINx and BPHCALx is currently being used.	0xF	R
				0000	BIGAIN0, BPHCAL0.		
				0001	BIGAIN1, BPHCAL1.		
				0010	BIGAIN2, BPHCAL2.		
				0011	BIGAIN3, BPHCAL3.		
				0100	BIGAIN4, BPHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x25D	CMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which CIGAINx and CPHCALx is currently being used.	0xF	R
				0000	CIGAIN0, CPHCAL0.		
				0001	CIGAIN1, CPHCAL1.		
				0010	CIGAIN2, CPHCAL2.		
				0011	CIGAIN3, CPHCAL3.		
				0100	CIGAIN4, CPHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x400	IPEAK	[31:27]	RESERVED		Reserved.	0x0	R
		[26:24]	IPPHASE		These bits indicate which phases generate the IPEAKVAL value. Note that the PEAKSEL, Bits[4:2] in the CONFIG3 register determine which current channel to monitor the peak value on. When IPPHASE, Bit 0 is set to 1, Phase A current is generated by the IPEAKVAL, Bits[23:0] value. Similarly, IPPHASE, Bit 1 indicates that the Phase B and IPPHASE, Bit 2 indicates that the Phase C current generated the peak value.	0x0	R
		[23:0]	IPEAKVAL		The IPEAK register stores the signed value of the peak current. IPEAK is equal to xI_PCF/2^5.	0x0	R
0x401	VPEAK	[31:27]	RESERVED		Reserved.	0x0	R
		[26:24]	VPPHASE		These bits indicate which phase(s) generate the VPEAKVAL value. Note that the PEAKSEL, Bits[4:2] in the CONFIG3 register determine which voltage channels to monitor the peak value on. When VPPHASE, Bit 0 is 1, the Phase A voltage generated the VPEAKVAL, Bits[23:0] value. Similarly, VPPHASE, Bit 1 indicates Phase B and	0x0	R

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
					VPPHASE, Bit 2 indicates that the Phase C voltage generated the peak value.		
		[23:0]	VPEAKVAL		The VPEAK register stores the signed value of the peak voltage. VPEAK is equal to xV_PCF/2^5.	0x0	R
0x402	STATUS0	[31:26]	RESERVED		Reserved.	0x0	R
		25	TEMP_RDY		This bit goes high to indicate when a new temperature measurement is available.	0x0	R/W
		24	MISMTCH		This bit is set to indicate a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W
		23	COH_WFB_FULL		This bit is set when the waveform buffer is full with resampled data, which is selected when WF_CAP_SEL = 0 in the WFB_CFG register.	0x0	R/W
		22	WFB_TRIG		This bit is set when one of the events configured in WFB_TRG_CFG occurs.	0x0	R/W
		21	THD_PF_RDY		This bit goes high to indicate when the THD and power factor measurements update, every 1.024 sec.	0x0	R/W
		20	RMS1012RDY		This bit is set when the 10 cycle rms/12 cycle rms values update.	0x0	R/W
		19	RMSONERDY		This bit is set when the fast rms½ rms values update.	0x0	R/W
		18	PWRRDY		This bit is set when the power values in the xWATT_ACC, xVA_ACC, xVAR_ACC, xFWATT_ACC, xFVA_ACC, and xFVAR_ACC registers update, after PWR_TIME 8 kSPS samples.	0x0	R/W
		17	PAGE_FULL		This bit is set when a page enabled in the WFB_PG_IRQEN register is filled with fixed data rate samples, when WF_CAP_SEL bit in the WFB_CFG register is equal to zero.	0x0	R/W
		16	WFB_TRIG_IRQ		This bit is set when the waveform buffer stops filling after an event configured in WFB_TRG_CFG occurs. This happens with fixed data rate samples only, when WF_CAP_SEL bit in the WFB_CFG register is equal to zero.	0x0	R/W
		15	DREADY		This bit is set when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W
		14	CF4		This bit is set when a CF4 pulse is issued, when the CF4 pin goes from a high to low state.	0x0	R/W
		13	CF3		This bit is set when a CF3 pulse is issued, when the CF3 pin goes from a high to low state.	0x0	R/W
		12	CF2		This bit is set when a CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W
		11	CF1		This bit is set when a CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W
		10	REVPSUM4		This bit is set to indicate if the CF4 polarity changed sign. For example, if the last CF4 pulse was positive reactive energy and the next CF4 pulse is negative reactive energy, the REVPSUM4 bit is set. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R/W
		9	REVPSUM3		This bit is set to indicate if the CF3 polarity changed sign. See REVPSUM4.	0x0	R/W
		8	REVPSUM2		This bit is set to indicate if the CF2 polarity changed sign. See REVPSUM4.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		7	REVPSUM1		This bit is set to indicate if the CF1 polarity changed sign. See REVPSUM4.	0x0	R/W
		6	REVRPC		This bit indicates if the Phase C total or fundamental reactive power has changed sign. The PWR_SIGN_SEL bit in the EP_CFG register selects whether total or fundamental reactive power is monitored. This bit is updated when the power values in the xVAR_ACC and xFVAR_ACC registers update, after PWR_TIME 8 kSPS samples.	0x0	R/W
		5	REVRPB		This bit indicates if the Phase B total or fundamental reactive power has changed sign. See REVRPC.	0x0	R/W
		4	REVRPA		This bit indicates if the Phase A total or fundamental reactive power has changed sign. See REVRPC.	0x0	R/W
		3	REVAPC		This bit indicates if the Phase C total or fundamental active power has changed sign. The PWR_SIGN_SEL bit in the EP_CFG register selects whether total or fundamental active power is monitored. This bit is updated when the power values in the xWATT_ACC and xFWATT_ACC registers update, after PWR_TIME 8 kSPS samples.	0x0	R/W
		2	REVAPB		This bit indicates if the Phase B total or fundamental active power has changed sign. See REVAPC.	0x0	R/W
		1	REVAPA		This bit indicates if the Phase A total or fundamental active power has changed sign. See REVAPC.	0x0	R/W
		0	EGYRDY		This bit is set when the power values in the xWATTHR xVAHR, xVARHR, xFVARHR, xFWATTHR, xFVAHR registers update, after EGY_TIME 8 kSPS samples or line cycles, depending on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W
0x403	STATUS1	31	ERROR3		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R/W
		30	ERROR2		This bit indicates that an error was detected and corrected. No action is required.	0x0	R/W
		29	ERROR1		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R
		28	ERROR0		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R
		27	CRC_DONE		This bit is set to indicate when the configuration register CRC calculation is complete, after initiated by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register.	0x0	R/W
		26	CRC_CHG		This bit is set if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W
		25	DIPC		This bit is set to indicates Phase C voltage entered or exited a dip condition.	0x0	R/W
		24	DIPB		This bit is set to indicates Phase B voltage entered or exited a dip condition.	0x0	R/W
		23	DIPA		This bit is set to indicates Phase A voltage entered or exited a dip condition.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		22	SWELLC		This bit is set to indicates Phase C voltage entered or exited a swell condition.	0x0	R/W
		21	SWELLB		This bit is set to indicates Phase B voltage entered or exited a swell condition.	0x0	R/W
		20	SWELLA		This bit it set to indicates Phase A voltage entered or exited a swell condition.	0x0	R/W
		19	RESERVED		Reserved.	0x0	R
		18	SEQERR		This bit is set to indicate a phase sequence error on the Phase voltage zero crossings.	0x0	R/W
		17	OI		This bit is set to indicate that an overcurrent event occurred on one of the phases indicated in the OISTATUS register.	0x0	R/W
		16	RSTDONE		This bit is set to indicate that the IC finished its power-up sequence after a reset or after changing between PSM3 operating mode to PSM0, which indicates that the user can configure the IC via the SPI port.	0x0	R/W
		15	ZXIC		When this bit is set to 1, it indicates a zero crossing is detected on Phase C current.	0x0	R/W
		14	ZXIB		When this bit is set to 1, it indicates a zero crossing is detected on Phase B current.	0x0	R/W
		13	ZXIA		When this bit is set to 1, it indicates a zero crossing is detected on Phase A current.	0x0	R/W
		12	ZXCOMB		When this bit is set, it indicates a zero crossing is detected on the combined signal from VA, VB, and VC.	0x0	R/W
		11	ZXVC		When this bit is set, it indicates a zero crossing is detected on the Phase C voltage channel.	0x0	R/W
		10	ZXVB		When this bit is set, it indicates a zero crossing is detected on the Phase B voltage channel.	0x0	R/W
		9	ZXVA		When this bit is set, it indicates a zero crossing is detected on the Phase A voltage channel.	0x0	R/W
		8	ZXTOVC		This bit is set to indicate a zero-crossing timeout on Phase C. This means that a zero crossing on the Phase C voltage is missing.	0x0	R/W
		7	ZXTOVB		This bit is set to indicate a zero-crossing timeout on Phase B. This means that a zero crossing on the Phase B voltage is missing.	0x0	R/W
		6	ZXTOVA		This bit is set to indicate a zero-crossing timeout on Phase A. This means that a zero crossing on the Phase A voltage is missing.	0x0	R/W
		5	VAFNOLOAD		This bit is set when one or more phase fundamental apparent energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		4	RFNOLOAD		This bit is set when one or more phase fundamental reactive energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		3	AFNOLOAD		This bit is set when one or more phase fundamental active energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		2	VANLOAD		This bit is set when one or more phase total apparent energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		1	RNLOAD		This bit is set when one or more phase total reactive energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		0	ANLOAD		This bit is set when one or more phase total active energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
0x404	EVENT_STATUS	[31:17]	RESERVED		Reserved.	0x0	R
		16	DREADY		This bit changes from a zero to a one when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R
		15	VAFNOLOAD		This bit is set when the fundamental apparent energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total apparent energy accumulation goes into no load.	0x0	R
		14	RFNOLOAD		This bit is set when the fundamental reactive energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of fundamental reactive energy accumulation goes into no load.	0x0	R
		13	AFNOLOAD		This bit is set when the fundamental active energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of fundamental active energy accumulation goes into no load.	0x0	R
		12	VANLOAD		This bit is set when the total apparent energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total apparent energy accumulation goes into no load.	0x0	R
		11	RNLOAD		This bit is set when the total reactive energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total reactive energy accumulation goes into no load.	0x0	R
		10	ANLOAD		This bit is set when the total active energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total active energy accumulation goes into no load.	0x0	R
		9	REVPSUM4		This bit indicates the sign of the last CF4 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R
		8	REVPSUM3		This bit indicates the sign of the last CF3 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF3 pulse is output, when the CF3 pin goes from high to low.	0x0	R
		7	REVPSUM2		This bit indicates the sign of the last CF2 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF2 pulse is output, when the CF2 pin goes from high to low.	0x0	R
		6	REVPSUM1		This bit indicates the sign of the last CF1 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is	0x0	R

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
					updated when a CF1 pulse is output, when the CF1 pin goes from high to low.		
		5	SWELLC		This bit is equal to one when the Phase C voltage is in the swell condition and is zero when it is not in a swell condition.	0x0	R
		4	SWELLB		This bit is equal to one when the Phase B voltage is in the swell condition and is zero when it is not in a swell condition.	0x0	R
		3	SWELLA		This bit is equal to one when the Phase A voltage is in the swell condition and is zero when it is not in a swell condition.	0x0	R
		2	DIPC		This bit is equal to one when the Phase C voltage is in the dip condition and is zero when it is not in a dip condition.	0x0	R
		1	DIPB		This bit is equal to one when the Phase B voltage is in the dip condition and is zero when it is not in a dip condition	0x0	R
		0	DIPA		This bit is equal to one when the Phase A voltage is in the dip condition and is zero when it is not in a dip condition.	0x0	R
0x405	MASK0	[31:26]	RESERVED		Reserved.	0x0	R
		25	TEMP_RDY_MASK		Set this bit to enable an interrupt when a new temperature measurement is available.	0x0	R/W
		24	MISMTCH		Set this bit to enable an interrupt when there is a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W
		23	COH_WFB_FULL		Set this bit to enable an interrupt when the waveform buffer is full with resampled data, which is selected when WF_CAP_SEL = 0 in the WFB_CFG register.	0x0	R/W
		22	WFB_TRIG		Set this bit to enable an interrupt when one of the events configured in WFB_TRG_CFG occurs.	0x0	R/W
		21	THD_PF_RDY		Set this bit to enable an interrupt when the THD and power factor measurements are updated, every 1.024 sec.	0x0	R/W
		20	RMS1012RDY		Set this bit to enable an interrupt when the 10 cycle rms/12 cycle rms values are updated.	0x0	R/W
		19	RMSONERDY		Set this bit to enable an interrupt when the fast rms½ values are updated.	0x0	R/W
		18	PWRRDY		Set this bit to enable an interrupt when the power values in the xWATT_ACC, xVA_ACC, xVAR_ACC, xFWATT_ACC, xFVA_ACC, and xFVAR_ACC registers update, after PWR_TIME 8 kSPS samples.	0x0	R/W
		17	PAGE_FULL		Set this bit to enable an interrupt when a page enabled in the WFB_PG_IRQEN register is filled.	0x0	R/W
		16	WFB_TRIG_IRQ		Set this bit to enable an interrupt when the waveform buffer has stopped filling after an event configured in WFB_TRG_CFG occurs.	0x0	R/W
		15	DREADY		Set this bit to enable an interrupt when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W
		14	CF4		Set this bit to enable an interrupt when the CF4 pulse is issued, when the CF4 pin goes from a high to low state.	0x0	R/W
		13	CF3		Set this bit to enable an interrupt when the CF3 pulse is issued, when the CF3 pin goes from a high to low state.	0x0	R/W
		12	CF2		Set this bit to enable an interrupt when the CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		11	CF1		Set this bit to enable an interrupt when the CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W
		10	REVPSUM4		Set this bit to enable an interrupt when the CF4 polarity changed sign.	0x0	R/W
		9	REVPSUM3		Set this bit to enable an interrupt when the CF3 polarity changed sign.	0x0	R/W
		8	REVPSUM2		Set this bit to enable an interrupt when the CF2 polarity changed sign.	0x0	R/W
		7	REVPSUM1		Set this bit to enable an interrupt when the CF1 polarity changed sign.	0x0	R/W
		6	REVRPC		Set this bit to enable an interrupt when the Phase C total or fundamental reactive power has changed sign.	0x0	R/W
		5	REVRPB		Set this bit to enable an interrupt when the Phase C total or fundamental reactive power has changed sign.	0x0	R/W
		4	REVRPA		Set this bit to enable an interrupt when the Phase A total or fundamental reactive power has changed sign.	0x0	R/W
		3	REVAPC		Set this bit to enable an interrupt when the Phase C total or fundamental active power has changed sign.	0x0	R/W
		2	REVAPB		Set this bit to enable an interrupt when the Phase B total or fundamental active power has changed sign.	0x0	R/W
		1	REVAPA		Set this bit to enable an interrupt when the Phase A total or fundamental active power has changed sign.	0x0	R/W
		0	EGYRDY		Set this bit to enable an interrupt when the power values in the xWATTHR, xVAHR xVARHR xFWATTHR, xFVAHR, and xFVARHR registers update, after EGY_TIME 8 kSPS samples or line cycles, depending on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W
0x406	MASK1	31	ERROR3		Set this bit to enable an interrupt if ERROR3 occurs. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		30	ERROR2		Set this bit to enable an interrupt if ERROR2 occurs.	0x0	R/W
		29	ERROR1		This interrupt is not maskable. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		28	ERROR0		This interrupt is not maskable. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		27	CRC_DONE		Set this bit to enable an interrupt when the configuration register CRC calculation is complete, after initiated by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register.	0x0	R/W
		26	CRC_CHG		Set this bit to enable an interrupt if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W
		25	DIPC		Set this bit to enable an interrupt when the Phase C voltage enters a dip condition	0x0	R/W
		24	DIPB		Set this bit to enable an interrupt when the Phase B voltage enters a dip condition.	0x0	R/W
		23	DIPA		Set this bit to enable an interrupt when the Phase A voltage enters a dip condition.	0x0	R/W
		22	SWELLC		Set this bit to enable an interrupt when the Phase C voltage enters a swell condition.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		21	SWELLB		Set this bit to enable an interrupt when the Phase B voltage enters a swell condition.	0x0	R/W
		20	SWELLA		Set this bit to enable an interrupt when the Phase A voltage enters a swell condition.	0x0	R/W
		19	RESERVED		Reserved.	0x0	R
		18	SEQERR		Set this bit to enable an interrupt when on a phase sequence error on the phase voltage zero crossings.	0x0	R/W
		17	OI		Set this bit to enable an interrupt when one of the currents enabled in the OC_EN bits in the CONFIG3 register enters an overcurrent condition.	0x0	R/W
		16	RESERVED		Reserved.	0x0	R
		15	ZXIC		Set this bit to enable an interrupt when a zero crossing is detected on the Phase C current channel.	0x0	R/W
		14	ZXIB		Set this bit to enable an interrupt when a zero crossing is detected on the Phase B current channel.	0x0	R/W
		13	ZXIA		Set this bit to enable an interrupt when a zero crossing is detected on the Phase A current channel.	0x0	R/W
		12	ZXCOMB		Set this bit to enable an interrupt when a zero crossing is detected on the combined signal from VA, VB, and VC.	0x0	R/W
		11	ZXVC		Set this bit to enable an interrupt when a zero crossing is detected on the Phase C voltage channel.	0x0	R/W
		10	ZXVB		Set this bit to enable an interrupt when a zero crossing is detected on the Phase B voltage channel.	0x0	R/W
		9	ZXVA		Set this bit to enable an interrupt when a zero crossing is detected on the Phase A voltage channel.	0x0	R/W
		8	ZXTOVC		Set this bit to enable an interrupt when there is a zero-crossing timeout on Phase C. This means that a zero crossing on the Phase C voltage is missing.	0x0	R/W
		7	ZXTOVB		Set this bit to enable an interrupt when there is a zero-crossing timeout on Phase B. This means that a zero crossing on the Phase B voltage is missing.	0x0	R/W
		6	ZXTOVA		Set this bit to enable an interrupt when there is a zero-crossing timeout on Phase A. This means that a zero crossing on the Phase A voltage is missing.	0x0	R/W
		5	VAFNOLOAD		Set this bit to enable an interrupt when one or more phase fundamental apparent energy enters or exits the no load condition.	0x0	R/W
		4	RFNOLOAD		Set this bit to enable an interrupt when one or more phase total reactive energy enters or exits the no load condition.	0x0	R/W
		3	AFNOLOAD		Set this bit to enable an interrupt when one or more phase fundamental active energy enters or exits the no load condition.	0x0	R/W
		2	VANLOAD		Set this bit to enable an interrupt when one or more phase total apparent energy enters or exits the no load condition.	0x0	R/W
		1	RNLOAD		Set this bit to enable an interrupt when one or more phase total reactive energy enters or exits the no load condition.	0x0	R/W
		0	ANLOAD		Set this bit to enable an interrupt when one or more phase total active energy enters or exits the no load condition.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
0x407	EVENT_MASK	[31:17]	RESERVED		Reserved.	0x0	R
		16	DREADY		Set this bit to enable the EVENT pin to go low when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W
		15	VAFNOLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of fundamental apparent energy accumulation goes into no load.	0x0	R/W
		14	RFNOLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of fundamental reactive energy accumulation goes into no load.	0x0	R/W
		13	AFNOLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of fundamental active energy accumulation goes into no load.	0x0	R/W
		12	VANLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of total apparent energy accumulation goes into no load.	0x0	R/W
		11	RNLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of total reactive energy accumulation goes into no load.	0x0	R/W
		10	ANLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of total active energy accumulation goes into no load.	0x0	R/W
		9	REVPSUM4		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate if the last CF4 pulse was from negative energy. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R/W
		8	REVPSUM3		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate if the last CF3 pulse was from negative energy. This bit is updated when a CF3 pulse is output, when the CF3 pin goes from high to low.	0x0	R/W
		7	REVPSUM2		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate if the last CF2 pulse was from negative energy. This bit is updated when a CF2 pulse is output, when the CF2 pin goes from high to low.	0x0	R/W
		6	REVPSUM1		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate if the last CF1 pulse was from negative energy. This bit is updated when a CF1 pulse is output, when the CF1 pin goes from high to low.	0x0	R/W
		5	SWELLCEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase C voltage is in a swell condition.	0x0	R/W
		4	SWELLBEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase B voltage is in a swell condition.	0x0	R/W
		3	SWELLAEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase A voltage is in a swell condition.	0x0	R/W
		2	DIPCEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase C voltage is in a dip condition.	0x0	R/W
		1	DIPBEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase B voltage is in a dip condition.	0x0	R/W
		0	DIPAEN		Set this bit to enable the EVENT pin to go low to indicate that the Phase A voltage is in a dip condition.	0x0	R/W
0x409	OILVL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OILVL_VAL		Over current detection threshold level.	0xFFFFFF	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
0x40A	OIA	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OI_VAL		Phase A overcurrent rms½ value. If a phase is enabled, with the OC_ENA bit set in the CONFIG3 register and AIRMSONE greater than the OILVL threshold, this value is updated.	0x0	R
0x40B	OIB	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OIB_VAL		Phase B overcurrent rms½ value. If a phase is enabled, with the OC_ENB bit set in the CONFIG3 register and BIRMSONE greater than the OILVL threshold, this value is updated.	0x0	R
0x40C	OIC	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OIC_VAL		Phase C overcurrent rms½ value. If a phase is enabled, with the OC_ENC bit set in the CONFIG3 register and CIRMSONE greater than the OILVL threshold, this value is updated.	0x0	R
0x40D	OIN	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OIN_VAL		Neutral current overcurrent rms½ value. If enabled, with the OC_ENN bit set in the CONFIG3 register and NIRMSONE greater than the OILVL threshold, this value is updated.	0x0	R
0x40F	VLEVEL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	VLEVEL_VAL		Register used in the algorithm that computes the fundamental active, reactive, and apparent powers, as well as the fundamental IRMS and VRMS values.	0x45D45	R/W
0x410	DIP_LVL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	DIPLVL		Voltage rms½ dip detection threshold level.	0x0	R/W
0x411	DIPA	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	DIPA_VAL		Phase A voltage rms½ value during a dip condition.	0x7FFFFF	R
0x412	DIPB	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	DIPB_VAL		Phase B voltage rms½ value during a dip condition.	0x7FFFFF	R
0x413	DIPC	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	DIPC_VAL		Phase C voltage rms½ value during a dip condition.	0x7FFFFF	R
0x414	SWELL_LVL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	SWELLLVL		Voltage rms½ swell detection threshold level.	0xFFFFFF	R/W
0x415	SWELLA	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	SWELLA_VAL		Phase A voltage rms½ value during a swell condition.	0x0	R
0x416	SWELLB	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	SWELLB_VAL		Phase B voltage rms½ value during a swell condition.	0x0	R
0x417	SWELLC	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	SWELLC_VAL		Phase C voltage rms½ value during a swell condition.	0x0	R
0x41F	PHNOLOAD	[31:18]	RESERVED		Reserved.	0x0	R
		17	CFVANL		This bit is set if the Phase C fundamental apparent energy is in no load.	0x0	R
		16	CFVARNL		This bit is set if the Phase C fundamental reactive energy is in no load.	0x0	R
		15	CFWATTNL		This bit is set if the Phase C fundamental active energy is in no load.	0x0	R
		14	CVANL		This bit is set if the Phase C total apparent energy is in no load.	0x0	R

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		13	CVARNL		This bit is set if the Phase B total reactive energy is in no load.	0x0	R
		12	CWATTNL		This bit is set if the Phase C total active energy is in no load.	0x0	R
		11	BFVANL		This bit is set if the Phase B fundamental apparent energy is in no load.	0x0	R
		10	BFVARNL		This bit is set if the Phase B fundamental reactive energy is in no load.	0x0	R
		9	BFWATTNL		This bit is set if the Phase B fundamental active energy is in no load.	0x0	R
		8	BVANL		This bit is set if the Phase B total apparent energy is in no load.	0x0	R
		7	BVARNL		This bit is set if the Phase B total reactive energy is in no load.	0x0	R
		6	BWATTNL		This bit is set if the Phase B total active energy is in no load.	0x0	R
		5	AFVANL		This bit is set if the Phase A fundamental apparent energy is in no load.	0x0	R
		4	AFVARNL		This bit is set if the Phase A fundamental reactive energy is in no load.	0x0	R
		3	AFWATTNL		This bit is set if the Phase A fundamental active energy is in no load.	0x0	R
		2	AVANL		This bit is set if the Phase A total apparent energy is in no load.	0x0	R
		1	AVARNL		This bit is set if the Phase A total reactive energy is in no load.	0x0	R
		0	AWATTNL		This bit is set if the Phase A total active energy is in no load.	0x0	R
0x424	ADC_REDIRECT	[31:21]	RESERVED		Reserved.	0x0	R
		[20:18]	VC_DIN		VC channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				000	IA ADC data.		
				001	IB ADC data.		
				010	IC ADC data.		
				011	IN ADC data.		
				100	VA ADC data.		
				101	VB ADC data.		
				110	VC ADC data.		
				111	VC ADC data.		
		[17:15]	VB_DIN		VB channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	VB ADC data.		
		[14:12]	VA_DIN		VA channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	VA ADC data.		
		[11:9]	IN_DIN		IN channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				111	IN ADC data.		
		[8:6]	IC_DIN		IC channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	IC ADC data.		
		[5:3]	IB_DIN		IB channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	IB ADC data.		
		[2:0]	IA_DIN		IA channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	IA ADC data.		
0x425	CF_LCFG	[31:23]	RESERVED		Reserved.	0x0	R
		22	CF4_LT		If this bit is set, the CF4 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, then the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		21	CF3_LT		If this bit is set, the CF3 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		20	CF2_LT		If this bit is set, the CF2 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		19	CF1_LT		If this bit is set, the CF1 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		[18:0]	CF_LTMR		If the CFx_LT bit in the CF_LCFG register is set, this value determines the active low pulse width of the CFx pulse.	0x0	R/W
0x472	PART_ID	[31:21]	RESERVED		Reserved.	0xX[2]	R
		20	ADE9000_ID		This bit is set to identify an ADE9000 IC.	0x1	R
		[19:0]	RESERVED		Reserved.	0xX	R
0x474	TEMP_TRIM	[31:16]	TEMP_OFFSET		Offset of temperature sensor, calculated during the manufacturing process.	0xX	R
		[15:0]	TEMP_GAIN		Gain of temperature sensor, calculated during the manufacturing process.	0xX	R
0x481	CONFIG1	15	EXT_REF		Set this bit if using an external voltage reference.	0x0	R/W
		[14:13]	RESERVED		Reserved.	0x0	R
		12	IRQ0_ON_IRQ1		Set this bit to combine all the interrupts onto a single interrupt pin, IRQ1, instead of using two pins, IRQ0 and IRQ1. Note that the IRQ0 pin still indicates the enabled IRQ0 events while in this mode and the IRQ1pin indicates both IRQ1 and IRQ0 events.	0x0	R/W
		11	BURST_EN		Set this bit to enable burst read functionality on the registers from Address 0x500 to Address 0x63C or Address 0x680 to Address 0x6BC. Note that this bit disables the CRC being appended to SPI register reads.	0x0	R/W
		10	DIP_SWELL_IRQ_MODE		Set interrupt mode for dip/swell.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				0	Receive continuous interrupts after every DIP_CYC/ SWELL_CYC cycles.		
				1	Receive one interrupt when entering dip/swell mode and another interrupt when exiting dip/swell mode.		
		[9:8]	PWR_SETTLE		These bits configure the time for the power and filter-based rms measurements to settle before starting the power, energy, and CF accumulations. 0: 64 ms. 1: 128 ms. 2: 256 ms. 3: 0 ms.	0x0	R/W
		[7:6]	RESERVED		Reserved.	0x0	R
		5	CF_ACC_CLR		Set this bit to clear the accumulation in the digital to frequency converter and the CFDEN counter. Note that this bit automatically clears itself.	0x0	W
		4	RESERVED		Reserved.	0x0	R
		[3:2]	CF4_CFG		These bits select which function to output on the CF4 pin.	0x0	R/W
				00	CF4, from digital to frequency converter.		
				01	CF4, from digital to frequency converter.		
				10	$\overline{\text{EVENT}}$.		
				11	DREADY.		
		1	CF3_CFG		This bit selects which function to output on the CF3 pin.	0x0	R/W
				0	CF3, from digital to frequency converter.		
				1	Zero-crossing output selected by the ZX_SEL bits in the ZX_LP_SEL register.		
		0	SWRST		Set this bit to initiate a software reset. Note that this bit is self clearing.	0x0	W
0x48F	OISTATUS	[15:4]	RESERVED		Reserved.	0x0	R
		[3:0]	OIPHASE		OIPHASE, Bit 0 indicates Phase A is above OILVL. OIPHASE, Bit 1 indicates Phase B is above OILVL. OIPHASE, Bit 2 indicates Phase C is above OILVL. OIPHASE, Bit 3 indicates Phase N is above OILVL.	0x0	R
0x490	CFMODE	15	CF4DIS		CF4 output disable. Set this bit to disable the CF4 output and bring the pin high. Note that when this bit is set, the CFx bit in STATUS0 is not set when a CF pulse is accumulated in the digital to frequency converter.	0x0	R/W
		14	CF3DIS		CF3 output disable. See CF4DIS.	0x0	R/W
		13	CF2DIS		CF2 output disable. See CF4DIS.	0x0	R/W
		12	CF1DIS		CF1 output disable. See CF4DIS	0x0	R/W
		[11:9]	CF4SEL		Type of energy output on the CF4 pin. Configure TERMSEL4 in the COMPMODE register to select which phases are included.	0x0	R/W
				000	Total active power.		
				001	Total reactive power.		
				010	Total apparent power.		
				011	Fundamental active power.		
				100	Fundamental reactive power.		
				101	Fundamental apparent power.		
				110	Total active power.		
				111	Total active power.		

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		[8:6]	CF3SEL		Selects type of energy output on CF3 pin. See CF4SEL.	0x0	R/W
		[5:3]	CF2SEL		Selects type of energy output on CF2 pin. See CF4SEL.	0x0	R/W
		[2:0]	CF1SEL		Selects type of energy output on CF1 pin. See CF4SEL.	0x0	R/W
0x491	COMPMODE	[15:12]	RESERVED		Reserved.	0x0	R
		[11:9]	TERMSEL4		Phases to include in CF4 pulse output. Set TERMSEL4, Bit 2 to 1 to include Phase C in the CF4 pulse output. Similarly, set TERMSEL4, Bit 1 to include Phase B, and TERMSEL4, Bit 0 for Phase A.	0x0	R/W
		[8:6]	TERMSEL3		Phases to include in CF3 pulse output. See TERMSEL4.	0x0	R/W
		[5:3]	TERMSEL2		Phases to include in CF2 pulse output. See TERMSEL4.	0x0	R/W
		[2:0]	TERMSEL1		Phases to include in CF1 pulse output. See TERMSEL4.	0x0	R/W
0x492	ACCMODE	[15:9]	RESERVED		Reserved.	0x0	R
		8	SELFREQ		Use this bit to configure the IC for a 50 Hz or 60 Hz system. This setting is used in the fundamental power measurements and to set the default line period used for VRMS½, 10 cycle rms/ 12 cycle rms and resampling calculations if a zero crossing is not present.	0x0	R/W
				0	50 Hz.		
				1	60 Hz.		
		7	ICONSEL		Set this bit to calculate the current flowing through IB from the IA and IC measurements. If this bit is set, IB = −IA − IC.	0x0	R/W
		[6:4]	VCONSEL		3-wire and 4-wire hardware configuration selection.	0x0	R/W
				000	4-wire wye.		
				001	3-wire delta. VB' = VA − VC.		
				010	4-wire wye, nonBlondel compliant. VB' = −VA − VC.		
				011	4-wire delta, nonBlondel compliant. VB' = −VA.		
				100	3-wire delta. VA' = VA − VB; VB' = VA − VC; VC' = VC − VB.		
		[3:2]	VARACC		Total and fundamental reactive power accumulation mode for energy registers and CFx pulses.	0x0	R/W
				00	Signed accumulation mode.		
				01	Absolute value accumulation mode.		
				10	Positive accumulation mode.		
				11	Negative accumulation mode.		
		[1:0]	WATTACC		Total and fundamental active power accumulation mode for energy registers and CFx pulses. See VARACC.	0x0	R/W
0x493	CONFIG3	[15:12]	OC_EN		Overcurrent detection enable. OC_EN[3:0] bits can all be set to 1 simultaneously to allow overcurrent detection on all three phases and/or neutral simultaneously. Bit 12. When OC_EN[3] is set to 1, the neutral line is selected for the overcurrent detection. Bit 13. When OC_EN[2] is set to 1, Phase C is selected for the overcurrent detection. Bit 14. When OC_EN[1] is set to 1, Phase B is selected for the overcurrent detection. Bit 15. When OC_EN[0] is set to 1, Phase A is selected for the overcurrent detection.	0xF	R/W
		[11:5]	RESERVED		Reserved.	0x0	R
		[4:2]	PEAKSEL		Set this bit to select which phase(s) to monitor peak voltages and currents on. Write 1 to PEAKSEL, Bit 0 to	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
					enable Phase A peak detection. Similarly, PEAKSEL, Bit 1 enables Phase B peak detection, and PEAKSEL, Bit 2 enables Phase C peak detection.		
		[1:0]	RESERVED		Reserved.	0x0	R
0x49A	ZX_LP_SEL	[15:5]	RESERVED		Reserved.	0x0	R
		[4:3]	LP_SEL		Selects line period measurement used for VRMS½ cycle, 10 cycle rms/12 cycle rms, and resampling.	0x3	R/W
				00	APERIOD, line period measurement from Phase A voltage.		
				01	BPERIOD, line period measurement from Phase B voltage.		
				10	CPERIOD, line period measurement from Phase C voltage.		
				11	COM_PERIOD, line period measurement on combined signal from VA, VB, and VC.		
		[2:1]	ZX_SEL		Selects the zero-crossing signal, which can be routed to the CF3/ZX output pin and used for line cycle energy accumulation.	0x3	R/W
				00	ZXVA, Phase A voltage zero-crossing signal.		
				01	ZXVB, Phase B voltage zero-crossing signal.		
				10	ZXVC, Phase C voltage zero-crossing signal.		
				11	ZXCOMB, zero crossing on combined signal from VA, VB, and VC.		
		0	RESERVED		Reserved.	0x0	R
0x49D	PHSIGN	[15:10]	RESERVED		Reserved.	0x0	R
		9	SUM4SIGN		Sign of the sum of the powers included in the CF4 datapath. The CF4 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		8	SUM3SIGN		Sign of the sum of the powers included in the CF3 datapath. The CF3 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		7	SUM2SIGN		Sign of the sum of the powers included in the CF2 datapath. The CF2 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		6	SUM1SIGN		Sign of the sum of the powers included in the CF1 datapath. The CF1 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		5	CVARSIGN		Phase C reactive power sign bit. The PWR_SIGN_ SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R
		4	CWSIGN		Phase C active power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental active power.	0x0	R
		3	BVARSIGN		Phase B reactive power sign bit. The PWR_SIGN_ SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R
		2	BWSIGN		Phase B active power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental active power.	0x0	R
		1	AVARSIGN		Phase A reactive power sign bit. The PWR_SIGN_ SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		0	AWSIGN		Phase A active power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental active power.	0x0	R
0x4A0	WFB_CFG	[15:13]	RESERVED		Reserved.	0x0	R
		12	WF_IN_EN		This setting determines whether the IN waveform samples are read out of the waveform buffer through the SPI.	0x0	R/W
				0	IN waveform samples are not read out of waveform buffer through the SPI.		
				1	IN waveform samples are read out of waveform buffer through the SPI.		
		[11:10]	RESERVED		Reserved.	0x0	R
		[9:8]	WF_SRC		Waveform buffer source and DREADY (data ready update rate) selection.	0x0	R/W
				00	Sinc4 output at 32 kSPS.		
				01	Reserved.		
				10	Sinc4 + IIR LPF output at 8 kSPS.		
				11	Current and voltage channel waveform samples, processed by the DSP (xI_PCF, xV_PCF) at 8 kSPS.		
		[7:6]	WF_MODE		Fixed data rate waveforms filling and trigger based modes.	0x0	R/W
				00	Stop when waveform buffer is full.		
				01	Continuous fill—stop only on enabled trigger events.		
				10	Continuous filling—center capture around enabled trigger events.		
				11	Continuous fill—save event address of enabled trigger events.		
		5	WF_CAP_SEL		This bit selects whether the waveform buffer is filled with resampled data or fixed data rate data, selected in the WF_CAP_SEL bits.	0x0	R/W
				0	Resampled data.		
				1	Fixed data rate data.		
		4	WF_CAP_EN		When this bit is set, a waveform capture is started.	0x0	R/W
				0	The waveform capture is disabled. The waveform buffer contents are maintained.		
				1	The waveform capture is started, according to the type of capture in WF_CAP_SEL and the WF_SRC bits when this bit goes from a 0 to a 1.		
		[3:0]	BURST_CHAN		Selects which data to read out of the waveform buffer through SPI.	0x0	R/W
				0000	All channels.		
				0001	IA and VA.		
				0010	IB and VB.		
				0011	IC and VC.		
				1000	IA.		
				1001	VA.		
				1010	IB.		
				1011	VB.		
				1100	IC.		
				1101	VC.		
				1110	IN if WF_IN_EN = 1 in the WFB_CFG register.		

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				1111	Single address read (SPI burst read mode is disabled).		
0x4A2	WFB_TRG_CFG	[15:11]	RESERVED		Reserved.	0x0	R
		10	TRIG_FORCE		Set this bit to trigger an event to stop the waveform buffer filling.	0x0	R/W
		9	ZXCOMB		Zero crossing on combined signal from VA, VB, and VC.	0x0	R/W
		8	ZXVC		Phase C voltage zero crossing.	0x0	R/W
		7	ZXVB		Phase B voltage zero crossing.	0x0	R/W
		6	ZXVA		Phase A voltage zero crossing.	0x0	R/W
		5	ZXIC		Phase C current zero crossing.	0x0	R/W
		4	ZXIB		Phase B current zero crossing.	0x0	R/W
		3	ZXIA		Phase A current zero crossing.	0x0	R/W
		2	OI		Over current event in any phase.	0x0	R/W
		1	SWELL		Swell event in any phase.	0x0	R/W
		0	DIP		Dip event in any phase.	0x0	R/W
0x4A3	WFB_TRG_STAT	[15:12]	WFB_LAST_PAGE		These bits indicate which page of the waveform buffer was filled last, when filling with fixed rate data samples.	0x0	R/W
		11	RESERVED		Reserved.	0x0	R
		[10:0]	WFB_TRIG_ADDR		These bits hold the address of the last sample put into the waveform buffer after a trigger event occurred, which is within a sample or two of when the actual trigger event occurred.	0x0	R
0x4AF	CONFIG2	[15:13]	RESERVED		Reserved.	0x0	R
		12	UPERIOD_SEL		Set this bit to use a user configured line period, in USER_PERIOD, for the VRMS½, 10 cycle rms/ 12 cycle rms and resampling calculation. If this bit is clear, the phase voltage line period selected by the LP_SEL[1:0] bits in the ZX_LP_SEL register is used.	0x0	R/W
		[11:9]	HPF_CRN		High-pass filter corner (f_{3dB}) enabled when the HPFDIS bit in the CONFIG0 register is equal to zero.	0x6	R/W
				000	77.39 Hz.		
				001	39.275 Hz.		
				010	19.79 Hz.		
				011	9.935 Hz.		
				100	4.98 Hz.		
				101	2.495 Hz.		
				110	1.25 Hz.		
				111	0.625 Hz.		
		[8:0]	RESERVED		Reserved.	0x0	R
0x4B0	EP_CFG	[15:13]	NOLOAD_TMR		This register configures how many 8 kSPS samples to evaluate the no load condition over.	0x0	R/W
				000	64 samples.		
				001	128 samples.		
				010	256 samples.		
				011	512 samples.		
				100	1024 samples.		
				101	2048 samples.		
				110	4096 samples.		
				111	Disable no load threshold.		
		[12:8]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		7	PWR_SIGN_SEL[1]		Selects whether the REVRPx bit follows the sign of the total or fundamental reactive power.	0x0	R/W
				0	Total reactive power.		
				1	Fundamental reactive power.		
		6	PWR_SIGN_SEL[0]		Selects whether the REVAPx bit follows the sign of the total or fundamental active power.	0x0	R/W
				0	Total active power.		
				1	Fundamental active power.		
		5	RD_RST_EN[3]		Set this bit to enable the energy register read with reset feature. If this bit is set, when one of the xWATTHR, xVAHR, xVARH, xFWATTHR, xFVAHR, and xFVARHR register is read, it is reset and begins accumulating energy from zero.	0x0	R/W
		4	EGY_LD_ACCUM		If this bit is equal to zero, the internal energy register is added to the user accessible energy register. If the bit is set, the internal energy register overwrites the user accessible energy register when the EGYRDY event occurs.	0x0	R/W
		[3:2]	RESERVED		Reserved.	0x0	R
		1	EGY_TMR_MODE		This bit determines whether energy is accumulated based on the number of 8 kSPS samples or zero-crossing events configured in the EGY_TIME register.	0x0	R/W
				0	Accumulate energy based on 8 kSPS samples.		
				1	Accumulate energy based on the zero crossing selected by the ZX_SEL bits in the ZX_LP_SEL register.		
		0	EGY_PWR_EN		Set this bit to enable the energy and power accumulator, when the run bit is also set.	0x0	R/W
0x4B4	CRC_FORCE	[15:1]	RESERVED		Reserved.	0x0	R
		0	FORCE_CRC_UPDATE		Write this bit to force the configuration register CRC calculation to start. When the calculation is complete, the CRC_DONE bit is set in the STATUS1 register.	0x0	R/W
0x4B5	CRC_OPTEN	15	CRC_WFB_TRG_CFG_EN		Set this bit to include the WFB_TRG_CFG register in the configuration register CRC calculation.	0x0	R/W
		14	CRC_WFB_PG_IRQEN		Set this bit to include the WFB_PG_IRQEN register in the configuration register CRC calculation.	0x0	R/W
		13	CRC_WFB_CFG_EN		Set this bit to include the WFB_CFG register in the configuration register CRC calculation.	0x0	R/W
		12	CRC_SEQ_CYC_EN		Set this bit to include the SEQ_CYC register in the configuration register CRC calculation.	0x0	R/W
		11	CRC_ZXLPSEL_EN		Set this bit to include the ZX_LP_SEL register in the configuration register CRC calculation.	0x0	R/W
		10	CRC_ZXTOUT_EN		Set this bit to include the CRC_ZXTOUT_EN register in the configuration register CRC calculation.	0x0	R/W
		9	CRC_APP_NL_LVL_EN		Set this bit to include the APP_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		8	CRC_REACT_NL_LVL_EN		Set this bit to include the REACT_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		7	CRC_ACT_NL_LVL_EN		Set this bit to include the ACT_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		6	CRC_SWELL_CYC_EN		Set this bit to include the SWELL_CYC register in the configuration register CRC calculation.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		5	CRC_SWELL_LVL_EN		Set this bit to include the SWELL_LVL register in the configuration register CRC calculation.	0x0	R/W
		4	CRC_DIP_CYC_EN		Set this bit to include the DIP_CYC register in the configuration register CRC calculation.	0x0	R/W
		3	CRC_DIP_LVL_EN		Set this bit to include the DIP_LVL register in the configuration register CRC calculation.	0x0	R/W
		2	CRC_EVENT_MASK_EN		Set this bit to include the EVENT_MASK register in the configuration register CRC calculation.	0x0	R/W
		1	CRC_MASK1_EN		Set this bit to include the MASK1 register in the configuration register CRC calculation.	0x0	R/W
		0	CRC_MASK0_EN		Set this bit to include the MASK0 register in the configuration register CRC calculation.	0x0	R/W
0x4B6	TEMP_CFG	[15:4]	RESERVED		Reserved.	0x0	R
		3	TEMP_START		Set this bit to manually request a new temperature sensor reading. The new temperature reading is available in 1 ms, indicated by the TEMP_RDY bit in the STATUS0 register. Note that this bit is self clearing.	0x0	W
		2	TEMP_EN		Set this bit to enable the temperature sensor.	0x0	R/W
		[1:0]	TEMP_TIME		Select the number of temperature readings to average.	0x0	R/W
				0	1 sample. New temperature measurement every 1 ms.		
				1	256 samples. New temperature measurement every 256 ms.		
				10	512 samples. New temperature measurement every 512 ms.		
				11	1024 samples. New temperature measurement every 1 sec.		
0x4B7	TEMP_RSLT	[15:12]	RESERVED		Reserved.	0x0	R
		[11:0]	TEMP_RESULT		12-bit temperature sensor result.	0x0	R
0x4B9	PGA_GAIN	[15:14]	RESERVED		Reserved.	0x0	R
		[13:12]	VC_GAIN		PGA gain for voltage Channel C ADC.	0x0	R/W
				00	Gain = 1.		
				01	Gain = 2.		
				10	Gain = 4.		
				11	Gain = 4.		
		[11:10]	VB_GAIN		PGA gain for Voltage Channel B ADC. See VC_GAIN.	0x0	R/W
		[9:8]	VA_GAIN		PGA gain for Voltage Channel A ADC. See VC_GAIN.	0x0	R/W
		[7:6]	IN_GAIN		PGA gain for neutral current channel ADC. See VC_GAIN.	0x0	R/W
		[5:4]	IC_GAIN		PGA gain for Current Channel C ADC. See VC_GAIN.	0x0	R/W
		[3:2]	IB_GAIN		PGA gain for Voltage Channel B ADC. See VC_GAIN.	0x0	R/W
		[1:0]	IA_GAIN		PGA gain for Current Channel A ADC. See VC_GAIN.	0x0	R/W
0x4BA	CHNL_DIS	[15:7]	RESERVED		Reserved.	0x0	R
		6	VC_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		5	VB_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		4	VA_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		3	IN_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		2	IC_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		1	IB_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		0	IA_DISADC		Set this bit to one to disable the ADC.	0x0	R/W

REGISTER DETAILS

Table 7. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
0x4E0	VAR_DIS	[15:1]	RESERVED		Reserved.	0x0	R
		0	VARDIS		Set this bit to disable the total VAR calculation. This bit must be set before writing the run bit for proper operation.	0x0	R/W

[1] Not valid until run bit is set.

[2] The default value is unique to every individual IC.

[3] Do not use, for more details, see the Errata section.

OUTLINE DIMENSIONS

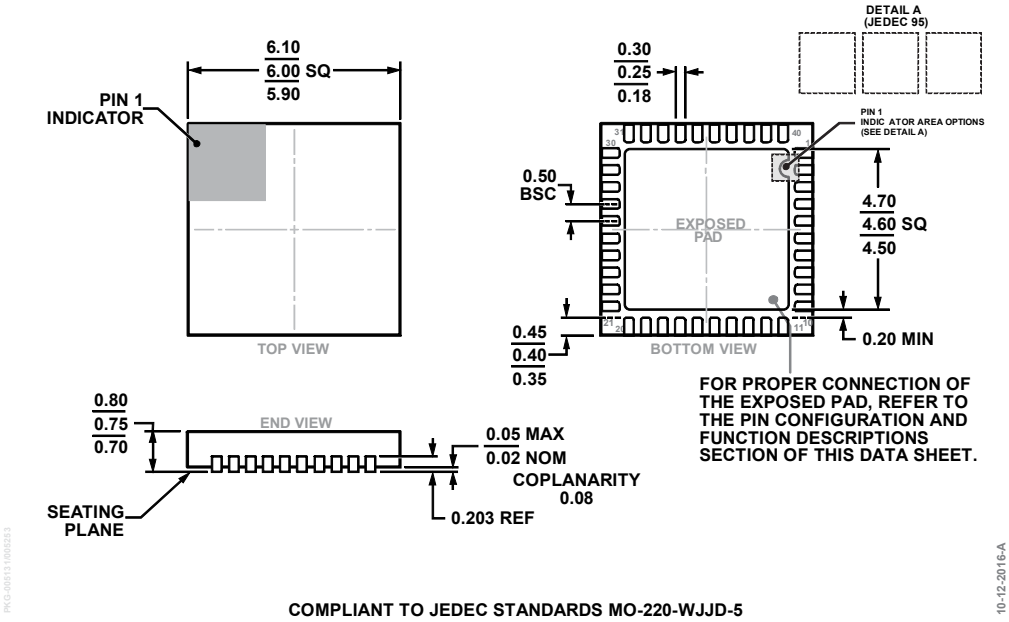

Figure 73. 40-Lead Lead Frame Chip Scale Package [LFCSP] 6 mm × 6 mm Body and 0.75 mm Package Height (CP-40-7) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADE9000ACPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
ADE9000ACPZ-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP], 13" Tape and Reel	CP-40-7
EVAL-ADE9000EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.