10 GHz to 40 GHz, 1:4 Channel, 4× Frequency Multiplier/Filter

FEATURES

- 4× input frequency multiplier with programmable harmonic filter
- Quad differential output PAs with independent enable control
- Input frequency range: 2.5 GHz to 10 GHz
- Output frequency range: 10 GHz to 40 GHz
- Input power: −20 dBm (50 Ω)
- Output power: 5 dBm differential (100 Ω)
- Harmonic rejection: −20 dBc to −40 dBc at all frequencies
- 3-wire or 4-wire SPI control of all functions
- On-chip programmable state machines for fast multiplier/filter and transmitter switching and control
- On-chip temperature sensor, output power detectors, and ADC
- DC power: 450 mW (2.5 V supply)
- 40-terminal, 6 mm × 6 mm LGA package

APPLICATIONS

- Millimeter wave imaging
  - Security
  - Medical
  - Industrial
- Wideband local oscillator (LO) multiplier/distributor

GENERAL DESCRIPTION

The ADAR2001 is a transmitter IC optimized for millimeter wave body scanning applications. Accepting a single-ended continuous wave (CW) input signal between 2.5 GHz and 10 GHz, the ADAR2001 provides gain, 4× frequency multiplication, harmonic filtering, 1:4 signal splitting, and four independently controllable power amplifiers (PAs) with differential outputs designed to directly drive dipole antennas with differential inputs.

All device functions and configuration options can be accessed by a 3-wire or 4-wire Analog Devices, Inc., serial peripheral interface (SPI).

Two state machines are also integrated into the ADAR2001, which facilitate easy configuration, control, and fast switching of the frequency multiplier, filter, and transmitter sections. These sequencers are programmed through the SPI and are then operated by pulsed inputs (reset and advance).

The output power and chip temperature can be monitored by four on-chip detectors and a temperature sensor whose outputs are multiplexed to an 8-bit ADC.

The ADAR2001 requires only a single 2.5 V supply with power consumption of 450 mW with one channel turned on.

The ADAR2001 is available in a compact, 40-terminal, 6 mm × 6 mm LGA package and is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

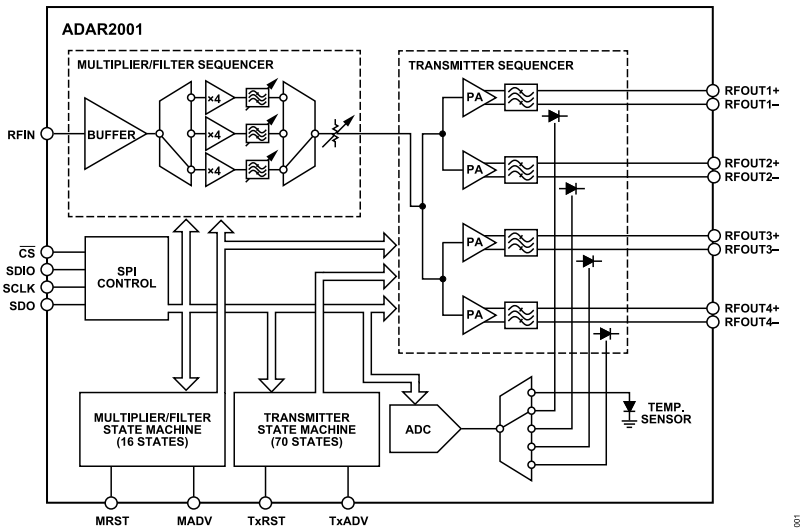

Figure 1.

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.935.5565 |

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REVISION HISTORY

1/2026—Rev. 0 to Rev. A

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Changes to Power Detectors and Temperature Sensor Section ... 13

8/2020—Revision 0: Initial Version

SPECIFICATIONS

V_{POS1}, V_{POS3}, V_{POS4}, V_{POS5} = 2.5 V, V_{POS2} = VREG, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT					
Frequency Range		2.5		10	GHz
Impedance			50		Ω
Return Loss			−15		dB
Power Range		−25	−20	−10	dBm
RF OUTPUT					
Frequency Range		10		40	GHz
Output Power	Input power (P_{IN}) = −20 dBm		5		dBm
	Multiplier enabled, PA disabled		−30		dBm
	Multiplier and PA disabled		−80		dBm
Channel Isolation	Disabled channel to active channel		−50		dBc
	Ready channel to active channel		−50		dBc
Channel to Channel Switching Frequency	Using ready mode			100	MHz
Phase Noise					
10 GHz Output					
	10 kHz offset		120		dBc/Hz
	100 kHz offset		123		dBc/Hz
	1 MHz offset		129		dBc/Hz
20 GHz Output					
	10 kHz offset		121		dBc/Hz
	100 kHz offset		119		dBc/Hz
	1 MHz offset		131		dBc/Hz
30 GHz Output					
	10 kHz offset		119		dBc/Hz
	100 kHz offset		117		dBc/Hz
	1 MHz offset		129		dBc/Hz
40 GHz Output					
	10 kHz offset		115		dBc/Hz
	100 kHz offset		116		dBc/Hz
	1 MHz offset		127		dBc/Hz
Differential Impedance			100		Ω
Differential Return Loss			8		dB
HARMONIC FILTERING					
Input Frequency					
Second Harmonic Rejection			−40		dBc
Third Harmonic Rejection			−40		dBc
Output Frequency					
Second Harmonic Rejection			−25		dBc
Third Harmonic Rejection			−20		dBc
STATE MACHINES AND TIMING					
Minimum Pulse Width					
MADV, MRST		3			ns
TxADV, TxRST		3			ns
Minimum Pulse Separation	Pulse start to pulse start				
MADV, MRST		10			ns
TxADV, TxRST		10			ns
Switching Frequency	Using ready mode			100	MHz

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Switching Time					
Multiplier Band Sleep to Active			50		ns
Multiplier Band Switch	Using ready mode		10		ns
PA Sleep to Active			50		ns
Channel to Channel Switch	Using ready mode, first channel off to second channel on		2		ns
DIGITAL INPUT LOGIC LEVELS					
Logic Low			0	0.3	V
Logic High		1	1.8		V
DIGITAL OUTPUT LOGIC LEVELS					
Logic Low			0	0.4	V
Logic High		1.4	1.8		V
VREG OUTPUT			1.8		V
POWER SUPPLY					
Analog					
Supply Voltage Range (V_{POS1}, V_{POS3}, V_{POS4}, V_{POS5})		2.25	2.5	2.75	V
Current Consumption	One channel active		180		mA
	Chip disabled		10		mA
Power Consumption	One channel active		450		mW
	Chip disabled		25		mW
Digital					
Supply Voltage Range (V_{POS2})		1.6	1.8	2	V
Current Consumption	Chip enabled		25		µA
Power Consumption	Chip enabled		45		µW

TIMING SPECIFICATIONS

V_{POS1}, V_{POS3}, V_{POS4}, V_{POS5} = 2.5 V, V_{POS2} = VREG, T_A = −40°C to +85°C, unless otherwise noted.

Table 2. SPI Timing

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
f_{SCLK}	Maximum clock rate	Write only			40	MHz
		Write and read			15	MHz
t_{PWH}	Minimum pulse width high			10		ns
t_{PWL}	Minimum pulse width low			10		ns
t_{DS}	Setup time, SDIO to SCLK			5		ns
t_{DH}	Hold time, SDIO to SCLK			5		ns
t_{DV}	Data valid, SDO to SCLK			5		ns
t_{DCS}	Setup time, $\overline{CS}$ to SCLK			10		ns
t_R	SDIO, SDO rise time	Outputs loaded with 10 pF, 10% to 90%		40		ns
t_F	SDIO, SDO fall time	Outputs loaded with 10 pF, 10% to 90%		40		ns

Timing Diagrams

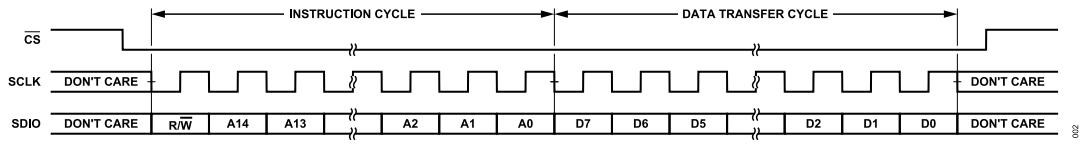

Figure 2. SPI Transaction Structure (MSB First)

SPECIFICATIONS

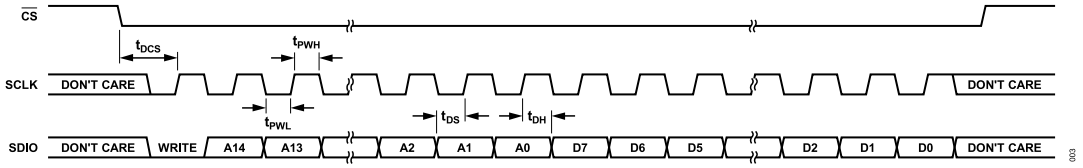

Figure 3. SPI Write Timing Diagram

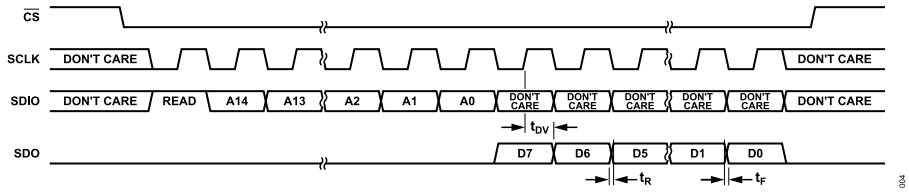

Figure 4. SPI 4-Wire Read Timing Diagram

SPI Block Write Mode

Data can be written to the SPI registers using the block write mode where the register address automatically increments and data for consecutive registers can be written without sending new address bits. Data writing can be continued indefinitely until $\overline{CS}$ is raised, ending the transaction. See Figure 5.

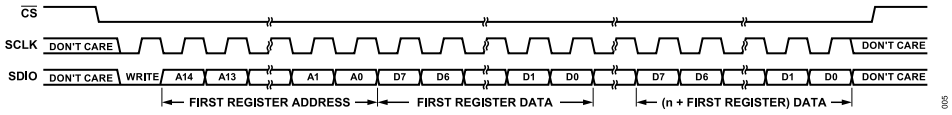

Figure 5. SPI Block Write

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{POS1}, V_{POS3}, V_{POS4}, V_{POS5} to GND[1]	+3 V, −0.3 V
V_{POS2} to GND[1]	+2.1 V, −0.3 V
Digital Input to GND[1]	+2.1 V, −0.3 V
RFIN to GND[1]	±0.3 V
RFIN Power	−5 dBm
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	135°C
Reflow Soldering	
Peak Temperature	260°C

[1] GND is the common ground to which all GNDx pins are connected.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CC-40-7[1]	33.8	12.2	°C/W

[1] Pad soldered.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAR2001

Table 5. ADAR2001, 40-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	1000 to 2000	1C
CDM	500 to 750	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

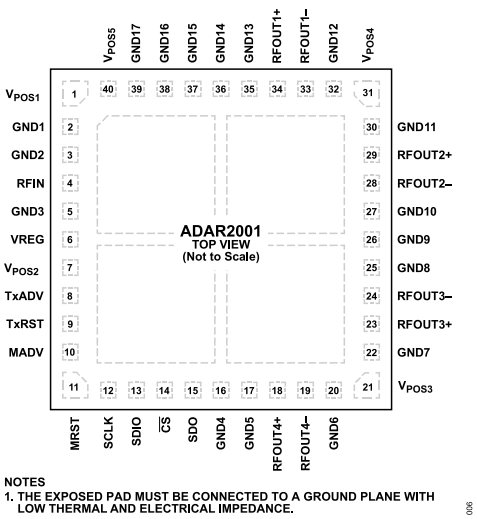

Figure 6. Pin Configuration (Top View, Not to Scale)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 21, 31, 40	V_{POS1}, V_{POS3}, V_{POS4}, V_{POS5}	2.5 V Power Supply for the Analog Section. Connect decoupling capacitors (one 10 nF and one 100 pF on each pin, and a 1 µF for the rail) to the ground plane as close as possible to these pins.
2, 3, 5, 16, 17, 20, 22, 25 to 27, 30, 32, 35 to 39	GND1 to GND17	Ground. Connect all ground pins to a ground plane with low thermal and electrical impedance.
4	RFIN	RF Input. RFIN is a single-ended, 50 Ω input operating from 2.5 GHz to 10 GHz, ac-coupled internally. The nominal input power level is −20 dBm.
6	VREG	1.8 V Low Dropout (LDO) Regulator Output. Directly connect VREG to Pin 7 (V_{POS2}).
7	V_{POS2}	1.8 V Power Supply for the Digital Section. Directly connect this supply to Pin 6 (VREG). Place a 1 µF capacitor to ground as close as possible to V_{POS2}.
8	TxADV	Transmitter State Machine Advance. If the state machine is enabled, pulsing TxADV advances the transmitter state machine to the next state in its cycle. If currently at the end of the cycle, pulsing TxADV returns the pointer to the mode defined in TX_STATE_1 (Register 0x019, Bits[7:4]).
9	TxRST	Transmitter State Machine Reset. If the state machine is enabled, TxRST immediately sets the transmit control state machine back to the configuration in the TX_EN1_MODE_0 and TX_EN2_MODE_0 registers (Register 0x050 and Register 0x051).
10	MADV	Multiplier/Filter State Machine Advance. If the state machine is enabled, pulsing MADV advances the multiplier/filter state machine to the next state in its cycle. If currently at the end of the cycle, pulsing MADV returns the pointer to the mode defined in MULT_STATE_1 (Register 0x03C, Bits[7:4]).
11	MRST	Multiplier/Filter State Machine Reset. If the state machine is enabled, MRST immediately sets the multiplier/filter state machine back to the configuration defined in the MULT_EN_MODE_0 and MULT_PASS_MODE_0 registers (Register 0x070 and Register 0x071).
12	SCLK	Serial Clock. The SCLK pin is used to clock data into and out of the SPI interface.
13	SDIO	Serial Data Input/Output. The SDIO pin is a high impedance data input for clocking in information. SDIO can also be used to read out data if Register 0x000, Bits[4:3] are set low (default).
14	$\overline{CS}$	Chip Select Bar. $\overline{CS}$ is used to activate the SPI port on the ADAR2001 and is active low. When $\overline{CS}$ goes high, the data previously clocked into the shift registers is latched to the chip. Connect a 200 kΩ pull-up resistor to 1.8 V from $\overline{CS}$ to ensure that the SPI interface is deactivated when not in use.
15	SDO	Serial Data Output. Register states can be read back on the SDO line if Register 0x000, Bits[4:3] are set high.
18, 19, 23, 24, 28, 29, 33, 34	RFOUT4+, RFOUT4−, RFOUT3+, RFOUT3−, RFOUT2−, RFOUT2+, RFOUT1−, RFOUT1+	Differential RF Outputs. RFOUTx± are 100 Ω differential pairs, ac-coupled internally. RFOUTx± operate from 10 GHz to 40 GHz. All eight lines must have equal electrical and mechanical lengths.
	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal and electrical impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

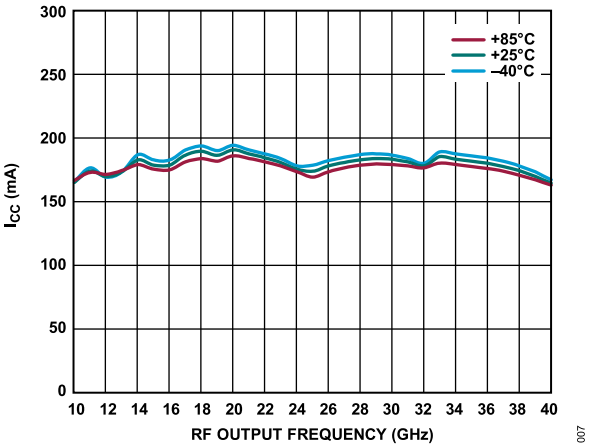

Figure 7. Supply Current (I_{CC}) vs. RF Output Frequency and Temperature, Supply Voltage = 2.5 V

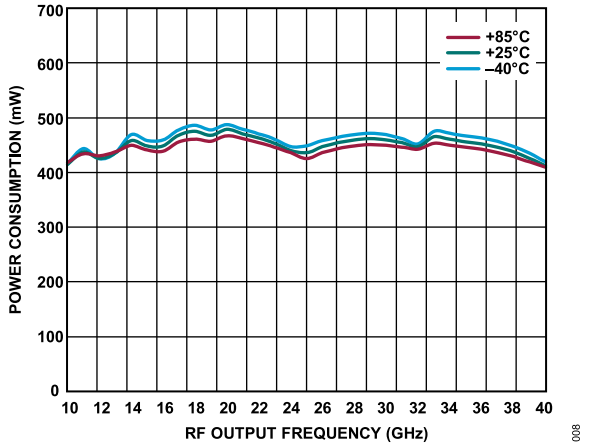

Figure 8. Power Consumption vs. RF Output Frequency and Temperature, Supply Voltage = 2.5 V

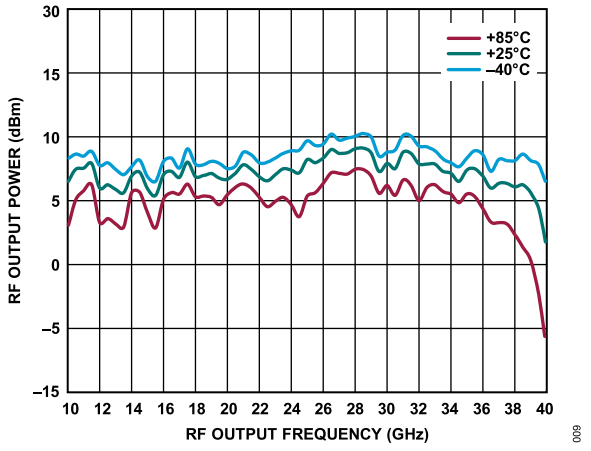

Figure 9. RF Output Power vs. RF Output Frequency and Temperature, RF Input Power = −20 dBm, Supply Voltage = 2.5 V

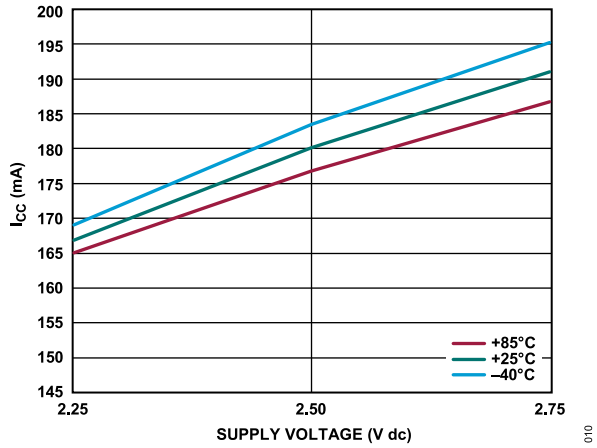

Figure 10. I_{CC} vs. Supply Voltage and Temperature

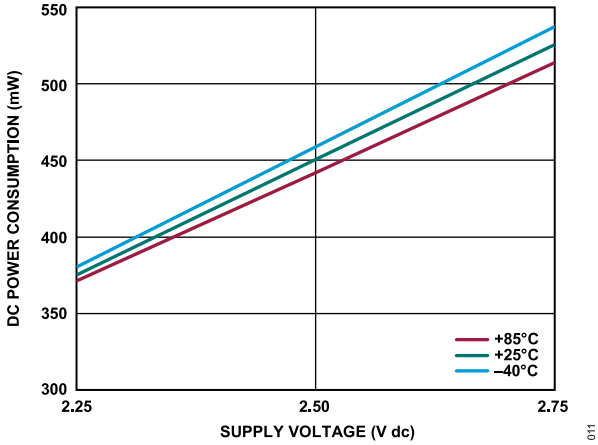

Figure 11. DC Power Consumption vs. Supply Voltage and Temperature

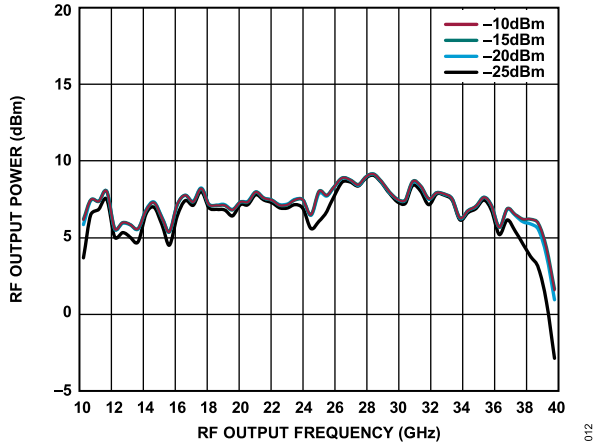

Figure 12. RF Output Power vs. RF Output Frequency and RF Input Power

TYPICAL PERFORMANCE CHARACTERISTICS

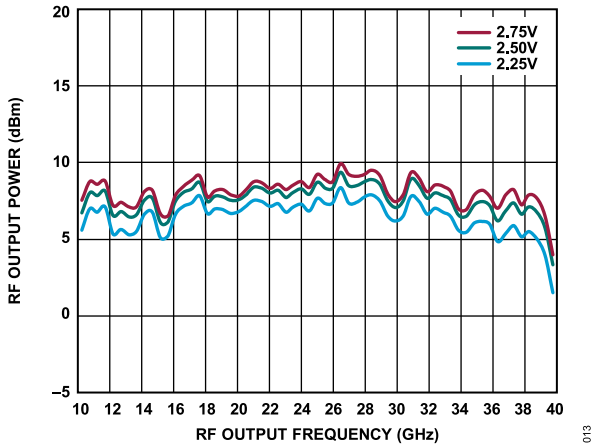

Figure 13. RF Output Power vs. RF Output Frequency and Supply Voltage, RF Input Power = −20 dBm

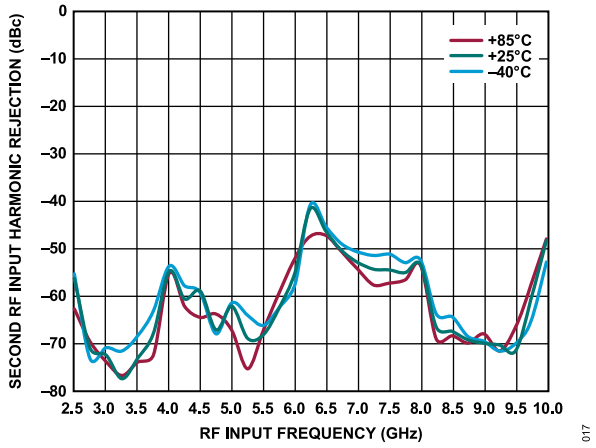

Figure 14. Second RF Input Harmonic Rejection vs. RF Input Frequency and Temperature

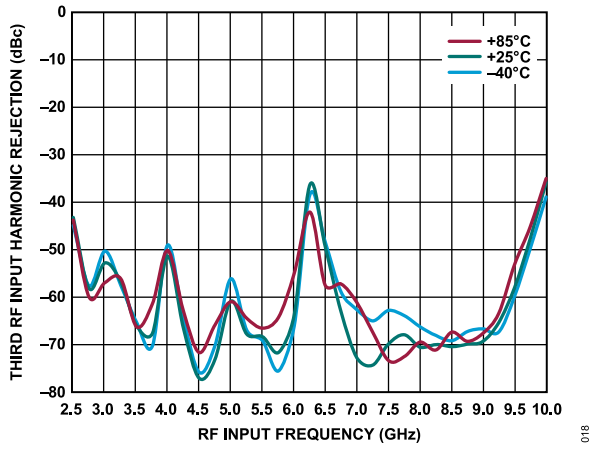

Figure 15. Third RF Input Harmonic Rejection vs. RF Input Frequency and Temperature

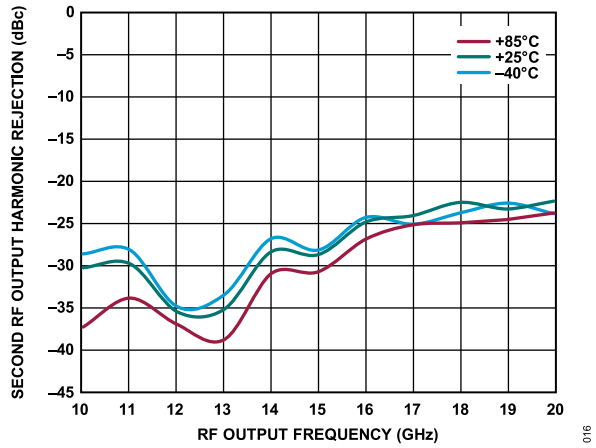

Figure 16. Second RF Output Harmonic Rejection vs. RF Output Frequency and Temperature

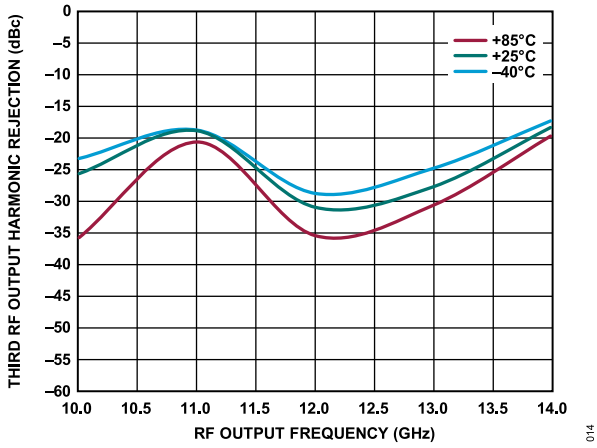

Figure 17. Third RF Output Harmonic Rejection vs. RF Output Frequency and Temperature

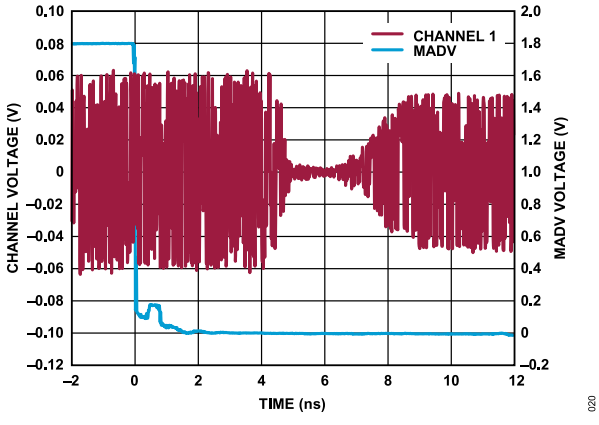

Figure 18. 25 GHz RF Frequency Band Switching with MADV

TYPICAL PERFORMANCE CHARACTERISTICS

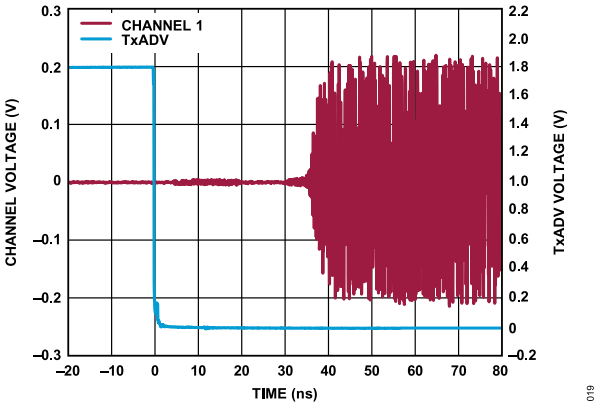

Figure 19. RF Output Sleep to Active Switching Time

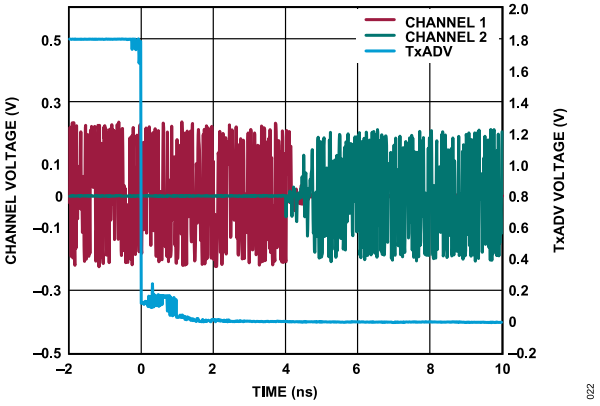

Figure 20. Channel to Channel Switching Time

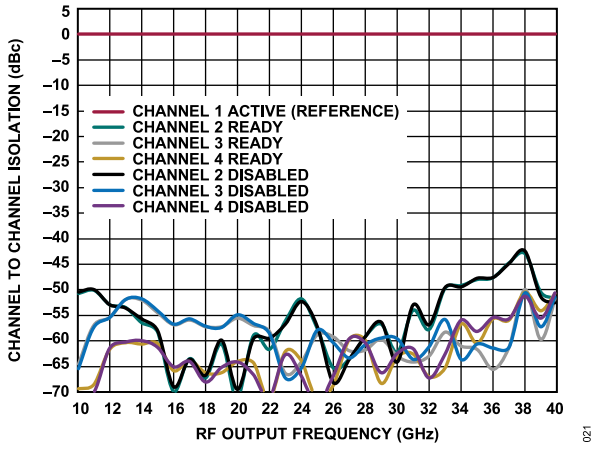

Figure 21. Channel to Channel Isolation vs. RF Output Frequency, RF Input = −20 dBm

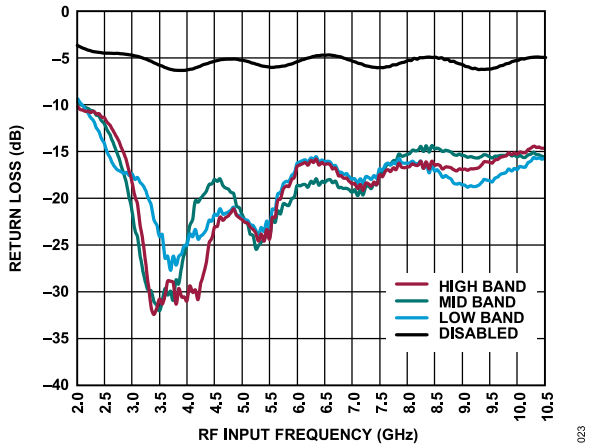

Figure 22. RF Input Return Loss

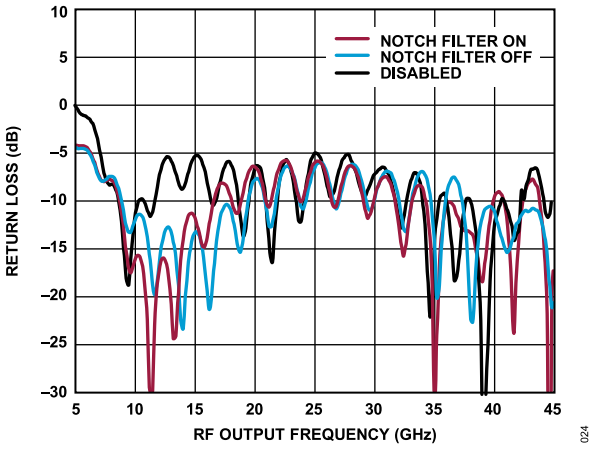

Figure 23. RF Output Return Loss

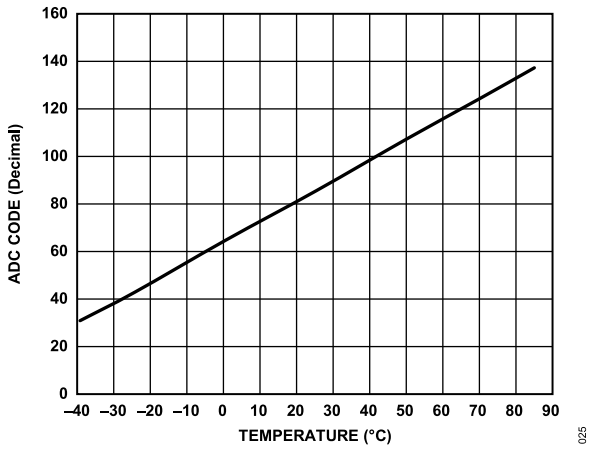

Figure 24. ADC Code vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

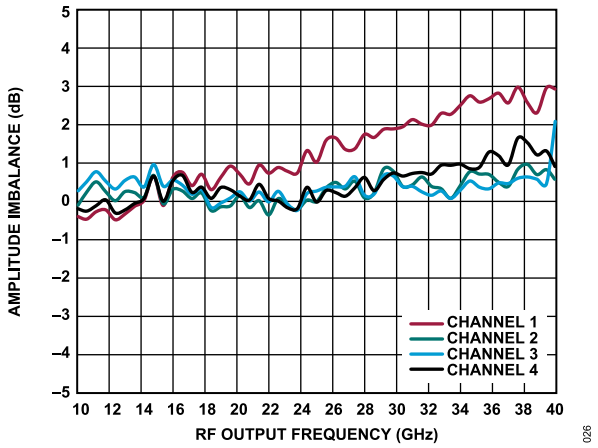

Figure 25. Amplitude Imbalance vs. RF Output Frequency

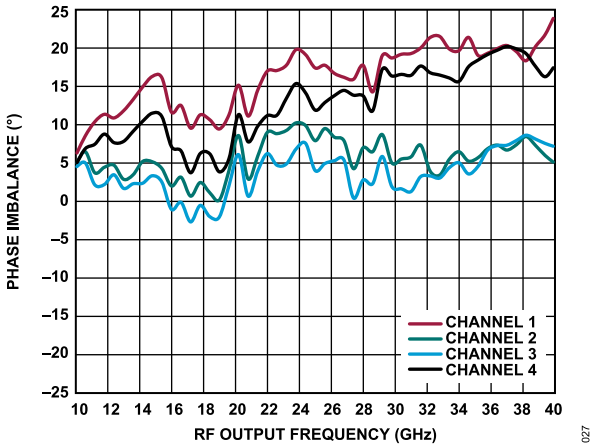

Figure 26. Phase Imbalance vs. RF Output Frequency

THEORY OF OPERATION

OVERVIEW

The main elements of the ADAR2001 are an RF input buffer, a 4× frequency multiplier with integrated switchable harmonic filter, a 1:4 signal splitter, and four differential output PAs that can drive dipole or similar antennas with differential inputs.

Apply a CW RF input signal between 2.5 GHz and 10 GHz with a power level of approximately −20 dBm to the RFIN port (Pin 4), which results in a nominal PA output power of 5 dBm on each of the differential PA outputs, RFOUTx± (Pin 18, Pin 19, Pin 23, Pin 24, Pin 28, Pin 29, Pin 33, and Pin 34).

The operation of these subcircuits can be controlled from the SPI port as well as two programmable state machines, one focused on multiplier/filter control and the other focused on transmit control.

RF output power on each channel can be monitored using individual, on-chip RF detectors. Temperature can also be observed with a temperature diode. These sensors feed into a 5:1 multiplexer that passes the desired signal to an on-chip, 8-bit ADC.

The ADAR2001 also includes an Analog Devices SPI port that is used for device configuration and readback. Although the state machines provide the fastest switching between states, all functions can also be controlled directly through the SPI port.

INPUT BUFFER, 4× MULTIPLIER, AND BAND-PASS FILTER

The RF input buffer provides approximately 17 dB of gain and provides an optimal driver for the 4× multiplier bands. The bias levels of the input and output stages of the buffer are independently adjustable through the SPI via Register 0x013. See the Bias Points section for more information.

The broadband frequency multiplier consists of three parallel subcircuits. Each subcircuit (low band, mid band, high band) is optimized to multiply and filter a segment of the total frequency range (2.5 GHz to 10 GHz input, 10 GHz to 40 GHz output). Recommended ranges and register settings for each band are shown in Table 7. Switches at the input and output of the multiplier block are used to select the subcircuit for the desired frequency of operation.

Each subcircuit consists of a 4× multiplier and a band-pass filter (BPF) with an adjustable corner frequency. The bias levels of the 4× multipliers are adjustable through the SPI using Register 0x011 and Register 0x012. See the Bias Points section for more information.

When the input frequency is in the low end of the band of the subcircuit, the BPF corner frequency must be set to its low state. Set the associated bit high to set the BPF corner frequency to its low state. See Table 7.

To complete a full 10 GHz to 40 GHz frequency sweep, the multiplier/filter block settings must be adjusted seven times to ensure optimum harmonic rejection and output power. These seven settings are shown in Table 7. By using the appropriate subcircuit and filter settings, harmonic distortion across the 10 GHz to 40 GHz range can be kept below −25 dBc. Within the 20 GHz to 40 GHz range, −30 dBc of harmonic rejection can be achieved.

In addition to having sleep and active modes, the 4× multipliers can be set to ready mode. Ready mode is a hybrid state between sleep and active mode, which does not pass a signal, but allows fast turn on. Current consumption in ready mode is higher than sleep mode but lower than in active mode. The switching time between ready mode and active mode is significantly faster than from sleep mode to active mode.

DIGITAL STEP ATTENUATOR

Although there is a digital step attenuator inside the multiplier/ filter block of the ADAR2001, it is not intended to be used as a level control for the output power of the ADAR2001. This attenuator is meant for reducing the level of harmonic content coming out of the multipliers before entering the splitter network.

Suggested values for the digital step attenuator vs. RF frequency are shown in Table 7 and represent a balance between harmonic performance and output power level. Therefore, altering these values is not recommended. Note that a value of 0x00 for ATTN_x (which refers to the ATTN_MDx and ATTN_SPI bits) corresponds to maximum attenuation.

LOW-PASS/NOTCH FILTER

A low-pass/notch filter is included after the PA outputs to help reduce any undesired harmonic content before transmission of the desired signal. RF output frequencies less than 16 GHz benefit from having this filter enabled. RF output frequencies more than 16 GHz must have this filter switched out to reduce any insertion loss due to the filter. Set the associated bit high to enable the filter. See Table 7.

Table 7. Multiplier/Filter Settings for Optimal Harmonic Rejection

Input Frequency (GHz)	Output Frequency (GHz)	Multiplier Band	BPF	ATTN_x[1]	Low-Pass/ Notch Filter	MULT_EN_x Register Value[2]	MULT_PASS_x Register Value[3]
2.50 to 3.00	10 to 12	Low band active (mid and high bands ready)	Low	0x13	On	0x7A	0xD3
3.00 to 3.50	12 to 14	Low band active (mid and high bands ready)	High	0x07	On	0x7A	0x47
3.50 to 4.00	14 to 16	Low band active (mid and high bands ready)	High	0x13	On	0x7A	0x53

THEORY OF OPERATION

Table 7. Multiplier/Filter Settings for Optimal Harmonic Rejection (Continued)

Input Frequency (GHz)	Output Frequency (GHz)	Multiplier Band	BPF	ATTN_x[1]	Low-Pass/ Notch Filter	MULT_EN_x Register Value[2]	MULT_PASS_x Register Value[3]
4.00 to 5.00	16 to 20	Mid band active (low and high bands ready)	Low	0x1F	Off	0x6E	0x9F
5.00 to 6.25	20 to 25	Mid band active (low and high bands ready)	High	0x1F	Off	0x6E	0x1F
6.25 to 8.00	25 to 32	High band active (low and mid bands ready)	Low	0x1F	Off	0x6B	0x9F
8.00 to 10.00	32 to 40	High band active (low and mid bands ready)	High	0x1F	Off	0x6B	0x1F

[1] ATTN_x refers to the ATTN_MDx and ATTN_SPI bit fields.

[2] MULT_EN_x refers to the MULT_EN_MODE_x and MULT_EN_SPI registers.

[3] MULT_PASS_x refers to the MULT_PASS_MODE_x and MULT_PASS_SPI registers.

1:4 SIGNAL SPLITTER NETWORK

The output of the multiplier/filter block is then applied to a 1:4 active power splitting network that is composed of two stages. The first stage is a 1:2 active splitter, which then feeds the second stage, two 1:2 active splitters. Each output path from the second stage drives a single PA, which results in a single input signal being split into four independently controlled output channels. The bias levels of each splitter stage are adjustable through the SPI via Register 0x014. See the Bias Points section for more information.

OUTPUT POWER AMPLIFIERS

There are four PAs, each with an ac-coupled, differential output operating from 10 GHz to 40 GHz. The differential output is intended to facilitate direct connection to an antenna with differential inputs. In applications where a single-ended output is required, the unused output can be terminated to ground using a 50 Ω resistor. Terminating the unused output results in 3 dB lower output power (that is, a single-ended output power of 2 dBm, nominal) along with some degradation in harmonic rejection. The bias level of the PAs is adjustable through the SPI. One setting, PA_BIAS in Register 0x015, controls all four PA bias points. See the Bias Points section for more information.

In normal operation, only one of the four PAs is active at a time, but the programmability allows all four (or any combination thereof) to be turned on simultaneously.

Like the 4× multipliers, each PA has three modes of operation: sleep, ready, and active. Ready mode is a hybrid state between sleep and active, which does not pass a signal, but allows fast turn on. Current consumption in ready mode is higher than sleep mode but lower than active mode. The switching time between ready mode and active mode is significantly faster than from sleep mode to active mode.

For the fastest switching times, use of the ready mode is critical. For example, while Power Amplifier 1 (PA1) is transmitting, Power Amplifier 2 (PA2) can be set to ready mode. The transmitter state machine can then be used to put PA1 to sleep and switch PA2 from ready to active.

POWER DETECTORS AND TEMPERATURE SENSOR

Each transmit channel on the ADAR2001 has a dedicated power detector with an enable bit in Register 0x049. All the detectors feed into a 5:1 multiplexer along with the local temperature sensor. This multiplexer allows the 8-bit on-chip ADC the flexibility to measure the current output power level of any channel, or the temperature of the chip itself. To calculate the approximate temperature in Celsius from the ADC output code, use the following equation:

$$T_A = (1.16 \times ADC\_OUTPUT) - 77$$

where *ADC_OUTPUT* is the ADC output word in Register 0x04B.

ADC INPUT MULTIPLEXER

The multiplexer position can be programmed using the MUX_SEL bits (Register 0x04A, Bits[3:1]). The multiplexer has five valid states, from 0 to 4. Figure 27 shows the multiplexer mapping.

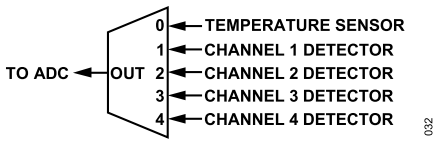

Figure 27. ADC Input Multiplexer Mapping

THEORY OF OPERATION

ADC AND ADC CLOCK

The ADAR2001 has an on-chip, 8-bit ADC and a variable clock input, each with their own enable control bits.

To take a measurement from the ADC, the user must first write to the ADC_CTRL register, Register 0x04A. This register contains the following bits:

- Bit 0: ADC_EOC (read only). This bit is a flag for when the ADC conversion is done.
- Bit 1 to Bit 3: MUX_SEL (read/write). These bits are used to select the ADC input, according to Figure 27.
- Bit 4: ST_CONV (read/write). This bit is set to start an ADC conversion cycle.
- Bit 5: CLK_EN (read/write). This bit enables the ADC clock.
- Bit 6: ADC_EN (read/write). This bit enables the ADC.
- Bit 7: ADC_CLKFREQ_SEL (read/write). This bit sets the clock frequency. A low sets the clock to 2 MHz, whereas a high sets the clock to 250 kHz.

After the ADC_CTRL register is written, it must be polled to wait for the ADC_EOC bit to go high. When this happens, the measured value can be read out from the ADC_OUTPUT register, Register 0x04B.

APPLICATIONS INFORMATION

SPI CONTROL

The ADAR2001 is designed to operate as part of a larger array. The built in state machines help to ease the control of multiple chips in parallel and to ensure that the fastest switching speeds are achieved. However, it is possible to operate every aspect of the ADAR2001 using the SPI port alone. When the state machines are disabled by setting MULT_SEQ_EN (Register 0x018, Bit 7) and TX_SEQ_EN (Register 0x016, Bit 7) low, the multiplier/filter and transmitter blocks respond to the SPI controlled registers (Register 0x045 to Register 0x048), rather than stepping through the programmed states.

Register 0x047 and Register 0x048 set up the multiplier/filter block when controlling the block with the SPI and have all the same controls as a typical multiplier/filter mode when controlling the block with the multiplier/filter sequencer.

Register 0x045 and Register 0x046 set up the transmitter block when controlling the block with the SPI and have all the same controls as a typical transmitter mode when controlling the block with the transmitter sequencer.

Operating the ADAR2001 in this manner can be thought of as a manual, rather than an automatic, approach. With the sequencers disabled, any changes to the configuration of the chip must occur through a SPI write.

STATE MACHINE MODES vs. STATES

Both the multiplier/filter state machine and the transmitter state machine have 16 modes available to set the configuration of their respective subcircuitry. The multiplier/filter state machine has 16 states available to cycle through, whereas the transmitter state machine has 70 available states.

Within each mode of the multiplier/filter state machine, the user can define the following:

- The enabled status of the RF input buffer (on or off, one bit)
- Sleep, ready, or active state of each 4× multiplier band (two bits for each band, six bits in total). The two bits control the ready and active status, and if neither is high, the multiplier band is set to sleep. Both bits must be high to be fully active.
- Digital step attenuator value (five bits)
- BPF corner frequency (low or high, one bit controls the filters in all bands)
- Low-pass/notch filter status (on or off, one bit controls all low-pass/notch filters)

Within each mode of the transmitter state machine, the user can define the following:

- Sleep, ready, or active state of each PA (two bits for each band, eight bits in total). The two bits control the ready and active status, and if neither is high, the PA is set to sleep. Both bits must be high to be fully active.
- The enabled status of the first 1:2 signal splitter feeding the second stage of splitters (on or off, one bit)
- The enabled status of the 1:2 signal splitter feeding PA Channel 1 and Channel 2 (on or off, one bit)
- The enabled status of the 1:2 signal splitter feeding PA Channel 3 and Channel 4 (on or off, one bit)

Each multiplier/filter state is used to select a previously configured operating mode. Each state bit field contains four bits, allowing selection of any mode between 0 and 15 (Register 0x070 to Register 0x08F). There are 16 multiplier/filter states available (Register 0x03C to Register 0x043). When the multiplier/filter state machine is enabled and the sequencer depth set in Register 0x018, Bits[3:0], the state machine cycles through the states in order, up to the defined state machine depth.

Similarly, each transmitter state is used to select a previously configured operating mode. Each state bit field has four bits, allowing selection of any mode between 0 and 15 (Register 0x050 to Register 0x06F). There are 70 transmit control states available (Register 0x019 to Register 0x03B). When the transmitter state machine is enabled, and the sequencer depth set in Register 0x017, the state machine cycles through the states in order, up to the defined state machine depth.

Figure 28 shows how the state machine pointer moves through a loop. In this diagram, n is the total number of states inside the loop. Because the sequencer depth bit field is 0 indexed, n is equal to one more than the value of the bits in the sequencer depth.

$n = MULT\_STATES + 1$

where:
n = 1 to 16.
MULT_STATES is the multiplier sequencer depth.

$n = TX\_STATES + 1$

where:
n = 1 to 16.
TX_STATES is the transmitter sequence depth.

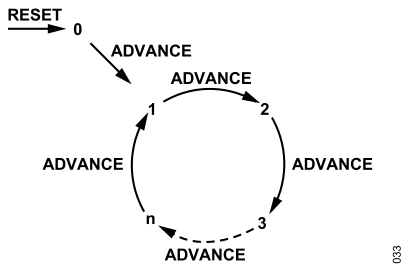

Figure 28. State Machine Position Loop

STATE MACHINE SETUP

Both state machines in the ADAR2001 have configuration registers that control various aspects of the state machine.

APPLICATIONS INFORMATION

For the multiplier/filter sequencer, this register is Register 0x018, and contains the following bits:

- Bit 0 to Bit 3: MULT_STATES. Sets the number of states in the loop (see Figure 28).
- Bit 4: MULT_CTL_LATCH_BYP. Bypasses the latch on the MADV and MRST pins. Setting this bit high bypasses the latch. Regardless of the value of this bit, the new state is preloaded on the rising edge of a MRST or MADV pulse. If the latch is enabled, the new settings are all latched to the appropriate section at the same time on the falling edge of the same pulse. If the latch is bypassed, the new settings are applied as soon as possible after the rising edge of the pulse, with no latching and no guaranteed order.
- Bit 5: MULT_SLP_HOLD. Prevents the multiplier/filter block from advancing when forced into a sleep state by the transmitter block. Used in conjunction with MULT_SLP_CTRL. See the Sequencer Sleep Control section for more information.
- Bit 6: MULT_SLP_CTRL. Forces the multiplier/filter block to sleep whenever the transmitter block is sleeping.
- Bit 7: MULT_SEQ_EN. Enables the multiplier/filter block. MULT_SEQ_EN must be set high for the block to operate with the external pins.

For the transmitter sequencer, the two control registers are Register 0x016 and Register 0x017.

Register 0x016 contains the following bits:

- Bit 4: TX_CTL_LATCH_BYP. Bypasses the latch on the TxADV and TxRST pins. Setting this bit high bypasses the latch. Regardless of the value of this bit, the new state is preloaded on the rising edge of a TxRST or TxADV pulse. If the latch is enabled, the new settings are all latched to the appropriate section at the same time on the falling edge of the same pulse. If the latch is bypassed, the new settings are applied as soon as possible after the rising edge of the pulse, with no latching and no guaranteed order.
- Bit 5: TX_SLP_HOLD. Prevents the transmitter block from advancing when forced into a sleep state by the multiplier/filter block. Used in conjunction with MULT_SLP_CTRL. See the Sequencer Sleep Control section for more information.
- Bit 6: TX_SLP_CTRL. Forces the transmitter block to sleep whenever the multiplier/filter block is sleeping.
- Bit 7: TX_SEQ_EN. Enables the transmitter block. Must be set high for the block to operate with the external pins.

Register 0x017 contains Bit 0 to Bit 6, TX_STATES, which sets the number of states in the loop (see Figure 28).

MULTIPLIER/FILTER STATE MACHINE

A programmable state machine provides a convenient and fast control mechanism for the multiplier/filter block and avoids the need for SPI writes each time the block must be reconfigured.

To enable the state machine, set the MULT_SEQ_EN bit (Register 0x018, Bit 7) high.

Although only seven multiplier/filter modes are required for a complete 10 GHz to 40 GHz sweep as described in Table 7, a maximum state machine depth of 16 is provided for optimum flexibility.

Nine preloaded modes can be assigned to any of the 16 states. These nine modes consist of a sleep mode, a ready mode, and the seven modes required to perform a 10 GHz to 40GHz sweep, as shown in Table 7. It is possible to overwrite any of the multiplier/filter modes with a custom set of operating conditions by changing the bits in Register 0x070 to Register 0x08F.

After the modes are defined, the order in which the sequencer moves through the desired modes must be set by filling the state bits in Register 0x03C to Register 0x043 in order, with the modes of interest. Any state can point to any mode, except State 0, which always points to Mode 0. Note that the sequencer moves through the states in order, up to the state machine depth.

Finally, the user must define how many states are used by setting the state machine depth (MULT_STATES, Register 0x018, Bits[3:0]). MULT_STATES is 0 indexed. Therefore, setting the depth to 0 leaves MULT_STATE_1 (Register 0x03C, Bits[7:4]) as the only state in the loop.

After the multiplier/filter state machine is programmed and enabled, operation is controlled by the MRST (multiplier reset, Pin 11) and MADV (multiplier advance, Pin 10) pins. Alternatively, operation can be controlled through the SPI using the MULT_RST_SPI and MULT_ADV_SPI bits (Register 0x044, Bit 3 and Bit 2, respectively). Note that using the SPI is slower than pulsing the sequencer pins directly.

MRST moves the pointer on the multiplier/filter state machine to State 0 regardless of the current position of the pointer and can be asserted at any time. State 0 always refers to Mode 0 and cannot be set to another mode. However, Mode 0 can be overwritten with any multiplier/filter configuration. Mode 0 is defined in Register 0x070 and Register 0x071.

MADV pulses advance the multiplier/filter state machine pointer one state at a time until the defined sequencer depth is cycled through. At that point, an additional MADV pulse moves the pointer back to State 1, which is normally set to a ready mode (however, State 1 can be set to any mode). State 1 applies the mode defined in the MULT_STATE_1 bits (Register 0x03C, Bits[7:4]).

TRANSMITTER STATE MACHINE

Like the multiplier/filter state machine, the transmitter state machine can be used to quickly cycle through transmit states without using the comparatively slower SPI interface.

To enable the state machine, set the TX_SEQ_EN bit (Register 0x016, Bit 7) high.

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The transmitter state machine controls the status of the four PAs (sleep, ready, or active) and the status of the 1:4 splitter network by defining the desired modes of operation in Register 0x050 to Register 0x06F. The PAs are in sleep mode when the ready and active bits are not enabled. Each mode outlines a custom set of operating conditions.

Although only four states are required to cycle through a transmit cycle by each of the PAs, a state machine depth of 70 is provided for optimum flexibility and to lower the total number of control lines required to operate multiple ADAR2001 chips in parallel. It is possible to control up to 16 ADAR2001 ICs using the same four sequencer lines (MADV, MRST, TxADV, TxRST). See the Sequencer Control Latch Bypass section for more information.

Following the mode definitions, the user must fill the state bits in Register 0x019 to Register 0x03B with the modes of interest. Any state can point to any mode, except State 0 which always points to Mode 0. Note that the sequencer moves through the states in order, up to the state machine depth.

After the states are defined, the user must set the number of states to be used by the sequencer by changing the TX_STATES bits (Register 0x017, Bits[6:0]). TX_STATES is 0 indexed. Therefore, setting the depth to 0 leaves TX_STATE_1 (Register 0x019, Bits[7:4]) as the only state in the loop.

After the transmit state machine is programmed, operation is controlled by the TxRST (transmit reset, Pin 9) and TxADV (transmit advance, Pin 8) pins. Alternatively, operation can be controlled through the SPI using the TX_RST_SPI and TX_ADV_SPI bits (Register 0x044, Bit 1 and Bit 0, respectively). TxRST moves the pointer on the transmit state machine to State 0 regardless of the current position of the pointer and can be asserted at any time. State 0 always refers to Mode 0 and cannot be set to another mode. However, Mode 0 can be overwritten with any transmitter configuration. Mode 0 is defined in Register 0x050 and Register 0x051.

TxADV pulses advance the transmitter state machine pointer one state at a time until the defined sequencer depth is cycled through. At that point, an additional TxADV pulse moves the pointer back to State 1. State 1 applies the mode defined in the TX_STATE_1 bits (Register 0x019, Bits[7:4]).

SINGLE-CHANNEL FREQUENCY SWEEP

Figure 29 shows a method of operation that can be used during a 20 GHz to 40 GHz frequency sweep of Channel 1. Based on Table 7, three multiplier/filter states are required during a 20 GHz to 40 GHz sweep. In this example, the defined state machine depth, MULT_STATES (Register 0x018, Bits[3:0]), is 3 because there are four states inside the loop, and MULT_STATES is 0 indexed.

As shown in Figure 29,

- Multiplier/Filter State 0 = sleep (outside the loop)
- Multiplier/Filter State 1 = mid band multiplier ready
- Multiplier/Filter State 2 = output 20 GHz to 25 GHz to PAs
- Multiplier/Filter State 3 = output 25 GHz to 30 GHz to PAs
- Multiplier/Filter State 4 = output 30 GHz to 40 GHz to PAs

The initial state is the sleep state where power consumption is at a minimum. This state is reached by pulsing the MRST pin. A pulse on MADV then advances the state machine to the first state inside the loop, which is defined as a ready state, where the mid band multiplier is partially powered but not active, and the BPF is disabled to pass the higher portion of the mid band. By using this ready state, an additional pulse on MADV makes this subcircuit path active in less than 10 ns. By making use of the ready mode for the upcoming state throughout the sweep, the multiplier/filter switching and settling time can be kept less than 10 ns between all states.

After the appropriate number of pulses is applied to MADV (5, in this case), the state machine automatically returns to the first state in the loop (ready).

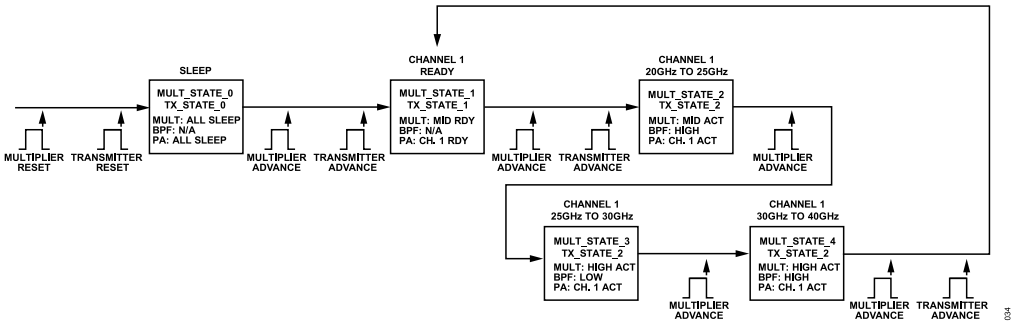

Figure 29. State Machine Loop Example for a Frequency Sweep from 20 GHz to 40 GHz on a Single Channel

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SINGLE FREQUENCY CHANNEL SWEEP

Figure 30 shows how the transmitter state machine can be used to cycle through the four PAs on a single ADAR2001 while at a fixed frequency. In this example, the defined state machine depth, TX_STATES (Register 0x017, Bits[6:0]), is 5 because there are 6 states inside the loop, and TX_STATES is 0 indexed.

As shown in Figure 30,

- Transmit State 0 = sleep (outside the loop)
- Transmit State 1 = Channel 1 PA ready
- Transmit State 2 = transmit on Channel 1, Channel 2 PA ready
- Transmit State 3 = transmit on Channel 2, Channel 3 PA ready
- Transmit State 4 = transmit on Channel 3, Channel 4 PA ready
- Transmit State 5 = transmit on Channel 4

The initial state is the sleep state, where power consumption is at a minimum. This state is reached by pulsing the TxRST pin.

A pulse on TxADV then advances the state machine to the first state inside the loop, which is defined as a ready state, where Channel 1 is partially powered but not active. The splitters feeding Channel 1 are active to speed up the switching speed of the next state. An additional pulse on TxADV then makes this subcircuit path fully active. Continuing to make use of the ready mode for the upcoming state throughout the sweep, the PA switching and settling time can be minimized for all states.

After the appropriate number of pulses are applied to TxADV (6, in this case), the state machine automatically returns to the first state in the loop (ready).

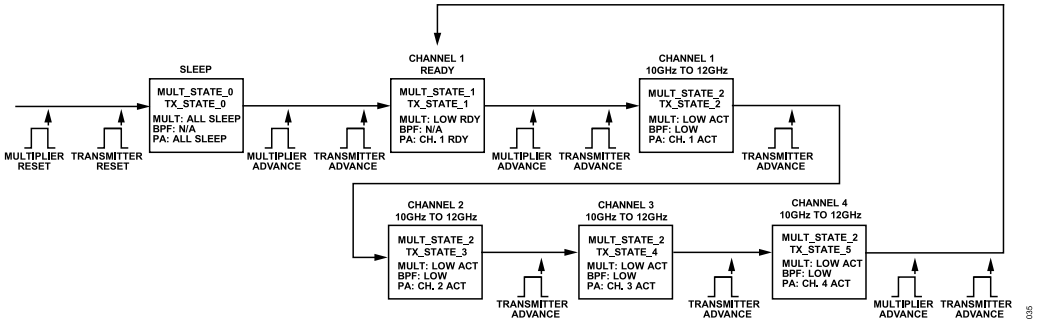

Figure 30. State Machine Loop Example for a Channel Sweep with a Fixed Frequency

APPLICATIONS INFORMATION

MULTICHANNEL FREQUENCY SWEEP

Figure 31 shows an example of how the two state machines can be used to perform a multichannel frequency sweep from 20 GHz to 40 GHz (that is, sweep through a frequency range while on one channel, move to the next channel, and repeat the sweep). In this example, because both MULT_STATES (Register 0x018, Bits[3:0]) and TX_STATES (Register 0x017 Bits[6:0]) are 0 indexed, MULT_STATES is defined as 2 because there are three states inside the multiplier/filter loop and TX_STATES as 3 because there are four states inside the transmitter loop.

As shown in Figure 31,

- Multiplier/Filter State 0 = sleep (outside the loop)
- Multiplier/Filter State 1 = output 20 GHz to 25 GHz to PAs
- Multiplier/Filter State 2 = output 25 GHz to 30 GHz to PAs
- Multiplier/Filter State 3 = output 30 GHz to 40 GHz to PAs
- Transmit State 0 = sleep (outside the loop)
- Transmit State 1 = transmit on Channel 1
- Transmit State 2 = transmit on Channel 2
- Transmit State 3 = transmit on Channel 3
- Transmit State 4 = transmit on Channel 4

Reset pulses on TxRST and MRST put both state machines in their initial states, which in this case are defined as sleep modes. Pulses on MADV and TxADV then advance both state machines to their first active state.

In this example, an initial ready state is skipped, and the circuit goes directly from sleep mode to active mode. Additional pulses on MADV are applied as the frequency is swept. Multiplier ready modes are used to ensure the fastest switching of the multiplier/filter circuitry.

After the frequency sweep is completed on Channel 1, both MADV and TxADV are pulsed to put the multiplier/filter back into its first state and the transmitter switches the active channel from 1 to 2. Then, the frequency sweep repeats itself using repeated pulses on the MADV pin.

In this example, after the four channels are frequency swept, both state machines loop back to their first active state. In a large array, it is recommended to loop them back to a sleep or ready state to wait for their turn to transmit again.

SEQUENCER SLEEP CONTROL

To further simplify the control of the ADAR2001, it is possible to link the sleep states of the two state machines so that one sequencer going to sleep forces the other to sleep as well. This link helps to limit the total number of required states to achieve a desired type of operation. To use this feature, one of the two sleep control bits must be set, but not both.

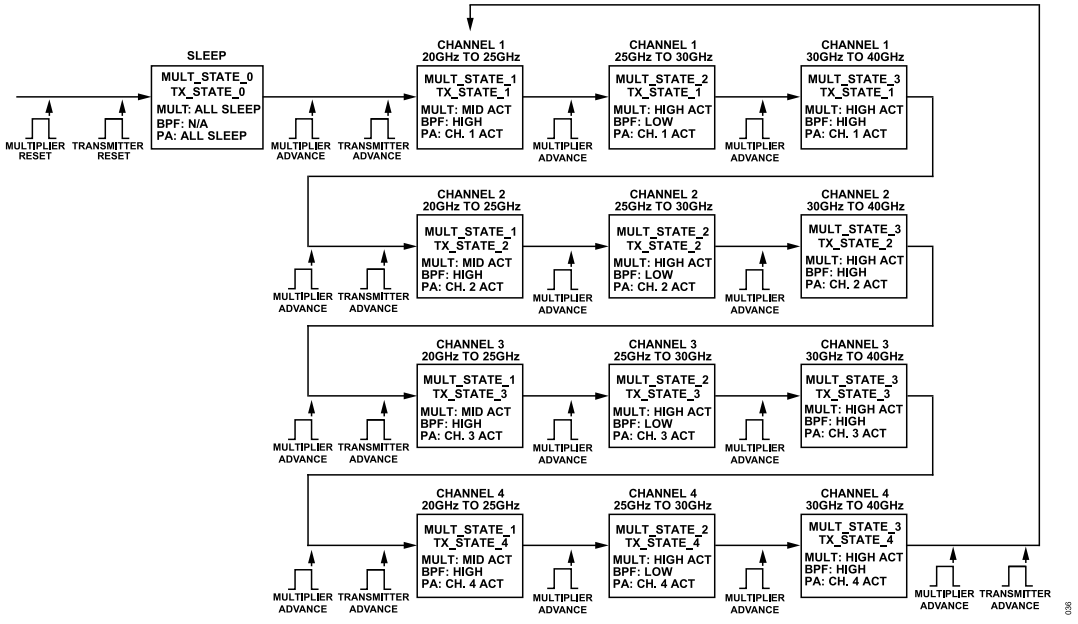

Figure 31. State Machine Loop Example for 4-Channel Frequency Sweep

For example, when the ADAR2001 is configured for a frequency sweep (as shown in Figure 29), if the TX_SLP_CTRL bit (Register 0x016, Bit 6) is set, when the multiplier/filter sequencer is reset, the transmitter state machine is forced to sleep as well. This means that the transmitter state machine does not need to have a state dedicated to sleep if it only needs to sleep when the multiplier/ filter sleeps. Furthermore, because the multiplier/ filter sleep state is controlling the sleep state of the transmitter, bringing the multiplier/filter out of sleep also brings the transmitter out of sleep, all of which is controlled with either the SPI or one external line (MADV).

APPLICATIONS INFORMATION

SEQUENCER SLEEP HOLD

By default, when one of the sequencers is forced asleep using one of the sleep control bits (MULT_SLP_CTRL or TX_SLP_CTRL), the counter for the sequencer being controlled can still be advanced. Because of this behavior, it is possible for a state machine to be put to sleep in one condition and brought out of sleep in another, depending on whether the sequencer advance or reset signals were exercised while the sequencer was sleeping.

If this behavior is undesired, the sleep hold bits (MULT_SLP_HOLD and TX_SLP_HOLD) can be asserted to force the associated state machine counter to ignore any inputs on the sequencer advance line. The counter also ignores advance signals coming from the SPI.

Note that the state machine counters always respond to a reset signal, even when the sleep hold bit is high.

When sleep hold is used, care must be taken when bringing the state machines out of sleep mode to ensure that the desired modes are reached. If the advance pins for both sequencers are pulsed too closely together under this condition, it is possible for the sequencer being controlled to not move into the expected state. To prevent this, the advance pulses must be staggered such that the rising edges are separated by a minimum of 3 ns with the pulse of the controlled sequencer coming second. See Figure 32 for an example of how to pulse the sequencers under this condition.

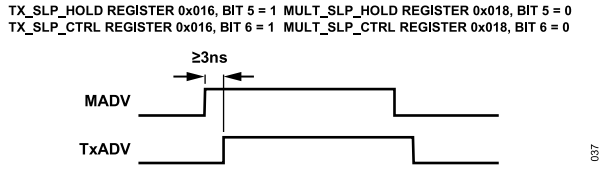

Figure 32. Example of How to Pulse the Sequencer Advance Pins to Ensure Advancement with Transmitter State Machine Sleep Hold Enabled

SEQUENCER CONTROL LATCH BYPASS

Typically, when a sequencer control line is pulsed, the upcoming state is loaded on the rising edge of the control pulse and latched to the various signal blocks on the falling edge of the same pulse. The latching helps to line up all the internal control signals so that the changes take place simultaneously.

It is possible to bypass the latching of the internal control signals by setting the bypass bits (TX_CTL_LATCH_BYP and MULT_CTL_LATCH_BYP) in the sequencer setup registers (Register 0x016, Bit 4 and Register 0x018, Bit 4).

Bypassing the latch results in the new state taking effect as soon as possible after the rising edge. Because the internal control signals are not aligned, the overall switching time between states can increase when compared to using the latch. Also, glitches are more likely to occur in the internal control signals, resulting in undesired transients in the RF blocks.

Note that this latch is the last check before any new data is sent to the various individual blocks. Therefore, when using the ADAR2001 in manual or SPI mode (sequencers disabled), the latching must be bypassed. If latching is not bypassed, the blocks never receive the new instructions unless the external sequencer pins are pulsed. However, this issue is uncommon because the sequencers are disabled in this mode of operation.

PARALLEL CHIP CONTROL

Up to 16 devices (a total of 64 channels) can be driven by a single set of four state machine control lines, three common SPI lines, and a $\overline{CS}$ line for each chip. Using this method, the total number of digital control lines is 7 + N, where N is the number of ADAR2001 ICs (see Figure 33 for a basic diagram). Parallel chip control can be used to minimize the total number of digital control lines. The SPI lines can be reduced to two common lines if 3-wire mode is selected by setting the SDOACTIVE and SDOACTIVE_ bits (Register 0x00, Bit 4 and Bit 3, respectively) to low. If 3-wire SPI mode is used, the total number of digital lines to 6 + N.

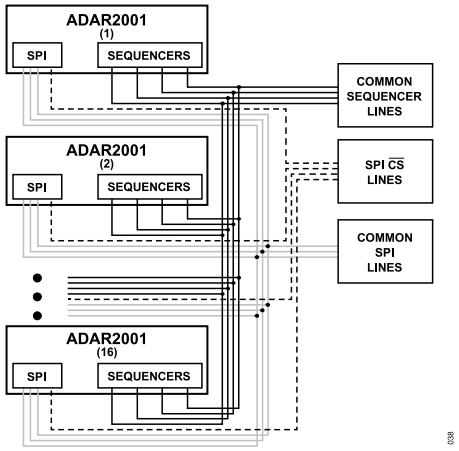

Figure 33. SPI and State Machine Digital Lines for Addressing and Controlling Up to 16 ADAR2001 Devices in Parallel

MULTICHIP FREQUENCY AND CHANNEL SWEEP

Figure 34 shows an example of how the two state machines can be used to perform a multichip frequency and channel sweep from 10 GHz to 16 GHz (that is, sweep through all four channels on a single chip while at a fixed frequency range, move to the next chip to repeat the channel sweep, then move to the next frequency to repeat the process). This example assumes that the state machine control lines are connected in parallel for up to 16 devices (64 channels, see Figure 33).

Initially, pulses on TxRST and MRST put both state machines in State 0, which in this case, is a sleep mode.

Next, pulses on MADV and TxADV advance both state machines to their first active state (transmitting on Channel 1 of ADAR2001 IC

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1). Additional pulses on the TxADV line are applied to successively switch through all the transmit channels of the first ADAR2001.

After all four channels are swept on the first device, an additional pulse on TxADV activates Channel 1 on ADAR2001 IC 2 while putting the Channel 4 PA on the first chip into a ready mode to prevent disrupting the multiplier/filter signal before the PA turns off. This sequence continues until all 64 channels on all 16 ADAR2001 ICs have transmitted at the first frequency or range.

At that point, a pulse is applied to both MADV and TxADV to advance the multiplier/filter sequencer to the next frequency range of interest and set the Channel 1 PA on ADAR2001 IC 1 back into an active mode. Another series of TxADV pulses follows until the last channel on ADAR2001 IC 16 is transmitting the new frequency or range.

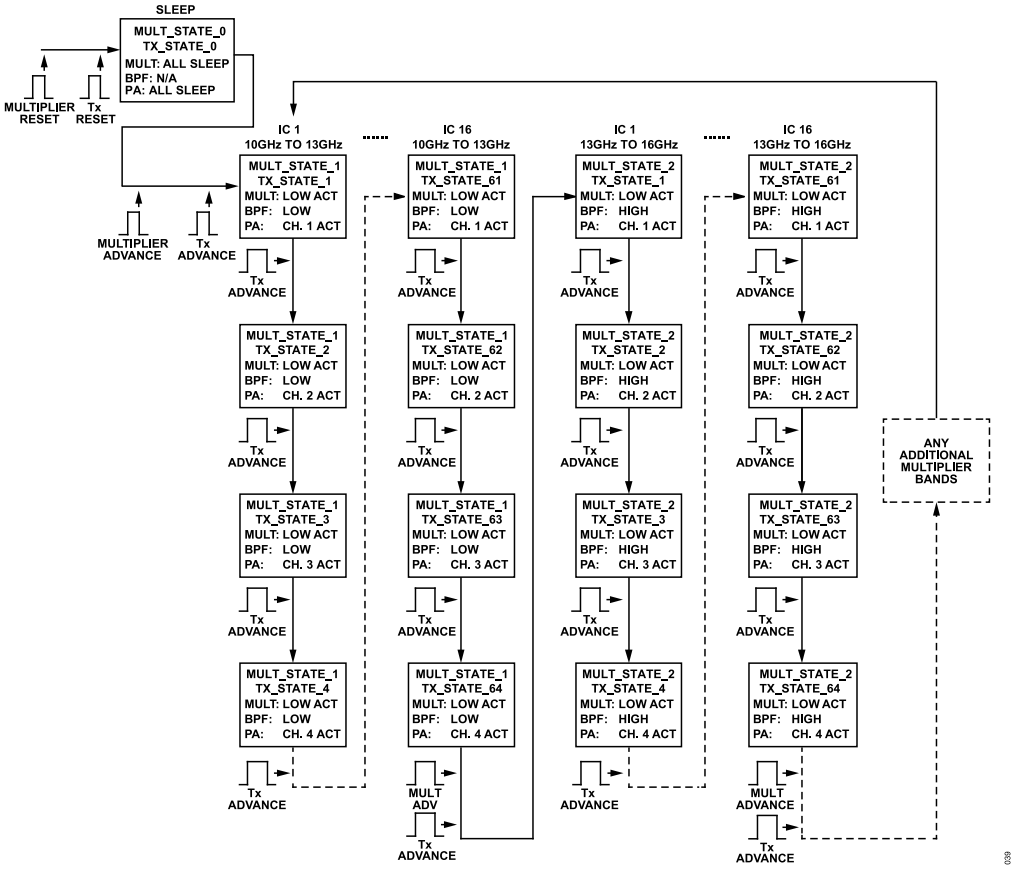

Figure 34. State Machine Loop Example for a 16-Chip Frequency and Channel Sweep

Table 8 shows how the transmitter state machine for each ADAR2001 can be set up to work in sequence, as described. Each device is turned fully on for only four states, but these four on states are all offset from each other. To run this sequence where up to 64 channels are swept with the state machines of all devices driven in parallel, 64 transmit states are used inside the loop, with the sleep state (State 0) used as a reset condition. In Table 8, SLP is the sleep state (State 0), CH1 to CH4 indicates the actively transmitting channel (Channel 1, Channel 2, Channel 3, or Channel 4), and RDY is ready mode.

If there are more tiles of 16 chips in the array that need to transmit after the tile shown in Table 8, this tile can have a reset pulse sent to put the sequencers into the initial sleep mode to wait for their turn to transmit again.

Table 8. Transmitter Sequencer Settings for 16 ADAR2001 Chips Using Shared Sequencer Lines for a Chip and Channel Sweep

	ADAR2001 Chip Number																
Tx State	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**Function**
(Reset) 0	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	All sleep
1	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	RDY	Chip 1 transmitting

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Table 8. Transmitter Sequencer Settings for 16 ADAR2001 Chips Using Shared Sequencer Lines for a Chip and Channel Sweep (Continued)

	ADAR2001 Chip Number																
Tx State	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Function
2	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
3	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
4	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
5	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 2 transmitting
6	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
7	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
8	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
9	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 3 transmitting
10	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
11	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
12	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
13	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 4 transmitting
14	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
15	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
16	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
17	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 5 transmitting
18	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
19	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
20	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
21	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 6 transmitting
22	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
23	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
24	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
25	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 7 transmitting
26	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
27	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
28	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
29	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 8 transmitting
30	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
31	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
32	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
33	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	Chip 9 transmitting
34	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
35	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	
36	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	
37	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	SLP	Chip 10 transmitting
38	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	SLP	
39	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	SLP	
40	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	SLP	
41	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	SLP	Chip 11 transmitting
42	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	SLP	
43	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	SLP	
44	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	SLP	
45	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	SLP	Chip 12 transmitting
46	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	SLP	
47	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	SLP	
48	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	SLP	

APPLICATIONS INFORMATION

Table 8. Transmitter Sequencer Settings for 16 ADAR2001 Chips Using Shared Sequencer Lines for a Chip and Channel Sweep (Continued)

	ADAR2001 Chip Number																
Tx State	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**Function**
49	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	SLP	Chip 13 transmitting
50	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	SLP	
51	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	SLP	
52	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	SLP	
53	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	SLP	Chip 14 transmitting
54	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	SLP	
55	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	SLP	
56	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	SLP	
57	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	SLP	Chip 15 transmitting
58	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	SLP	
59	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	SLP	
60	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	**RDY**	
61	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**RDY**	**CH1**	Chip 16 transmitting
62	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH2**	
63	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH3**	
64	**RDY**	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	SLP	**CH4**	

BIAS POINTS

Table 9. Default Bias Points

Register Address	Register Name	Bit Field Name(s)	Register Bit(s)	Default Value	Description
0x011	BIAS_CURRENT_MULT1			0xBB	Low and mid band multiplier bias current
		MULT_LOW_BIAS	[3:0]	0xB	Low band multiplier bias current
		MULT_MID_BIAS	[7:4]	0xB	Mid band multiplier bias current
0x012	BIAS_CURRENT_MULT2			0x0B	High band multiplier bias current
		MULT_HIGH_BIAS	[3:0]	0xB	High band multiplier bias current
0x013	BIAS_CURRENT_RFAMP			0x75	RF buffer amplifier bias current
		RF_AMP1_BIAS	[3:0]	0x05	RF buffer input stage bias current
		RF_AMP2_BIAS	[7:4]	0x07	RF buffer output stage bias current
0x014	BIAS_CURRENT_SPLT			0xB5	Active splitter bias current
		SPLT1_BIAS	[3:0]	0x5	First stage active splitter bias current
		SPLT2_BIAS	[7:4]	0xB	Second stage active splitter bias current
0x015	BIAS_CURRENT_PA			0x0C	Power amplifier bias current
		PA_BIAS	[3:0]	0xC	Power amplifier bias current

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x000	INTERFACE_CONFIG_A	7	SOFTRESET	Soft Reset	0x0	R/W
		6	LSB_FIRST	LSB First	0x0	R/W
		5	ADDR_ASCN	Address Ascension	0x0	R/W
		4	SDOACTIVE	SDO Active	0x1	R/W
		3	SDOACTIVE_	SDO Active	0x1	R/W
		2	ADDR_ASCN_	Address Ascension	0x0	R/W
		1	LSB_FIRST_	LSB First	0x0	R/W
		0	SOFTRESET_	Soft Reset	0x0	R/W
0x001	INTERFACE_CONFIG_B	7	SINGLE_INSTRUCTION	Single Instruction	0x0	R/W
		6	$\overline{CS}$_STALL	$\overline{CS}$ Stall	0x0	R/W
		5	MASTER_SLAVE_RB	Master Slave Readback	0x0	R/W
		4	SLOW_INTERFACE_CTRL	Slow Interface Control	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:1]	SOFT_RESET	Soft Reset	0x0	R/W
		0	RESERVED	Reserved	0x0	R
0x002	DEV_CONFIG	[7:4]	DEV_STATUS	Device Status	0x1	R/W
		[3:2]	CUST_OPERATING_MODE	Custom Operating Modes	0x0	R/W
		[1:0]	NORM_OPERATING_MODE	Normal Operating Modes	0x0	R/W
0x003	CHIP_TYPE	[7:0]	CHIP_TYPE	Chip Type	0x0	R
0x004	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]	Product ID High	0x0	R
0x005	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]	Product ID Low	0x0	R
0x00A	SCRATCH_PAD	[7:0]	SCRATCHPAD	Scratch Pad	0x0	R/W
0x00B	SPI_REV	[7:0]	SPI_REV	SPI Revision	0x0	R
0x00C	VENDOR_ID_H	[7:0]	VENDOR_ID[15:8]	Vendor ID High	0x0	R
0x00D	VENDOR_ID_L	[7:0]	VENDOR_ID[7:0]	Vendor ID Low	0x0	R
0x00F	TRANSFER_REG	[7:1]	RESERVED	Reserved	0x0	R
		0	MASTER_SLAVE_XFER	Master Slave Transfer	0x0	R/W
0x010	PWRON	[7:1]	RESERVED	Reserved	0x0	R
		0	PWRON	Chip Power-Up	0x1	R/W
0x011	BIAS_CURRENT_MULT1	[7:4]	MULT_MID_BIAS	Multiplier Mid Band 4× Bias Current Setting	0xB	R/W
		[3:0]	MULT_LOW_BIAS	Multiplier Low Band 4× Bias Current Setting	0xB	R/W
0x012	BIAS_CURRENT_MULT2	[7:4]	RESERVED	Reserved	0x0	R/W
		[3:0]	MULT_HIGH_BIAS	Multiplier High Band 4× Bias Current Setting	0xB	R/W
0x013	BIAS_CURRENT_RFAMP	[7:4]	RF_AMP2_BIAS	RF Amp Output Stage Bias Current Setting	0x7	R/W
		[3:0]	RF_AMP1_BIAS	RF Amp Input Stage Bias Current Setting	0x5	R/W
0x014	BIAS_CURRENT_SPLT	[7:4]	SPLT2_BIAS	Second Active Splitter Stages Bias Current Setting	0xB	R/W
		[3:0]	SPLT1_BIAS	First Active Splitter Stage Bias Current Setting	0x5	R/W
0x015	BIAS_CURRENT_PA	[7:4]	RESERVED	Reserved	0x0	R
		[3:0]	PA_BIAS	PA Bias Current Setting	0xC	R/W
0x016	TX_SEQUENCER_SETUP	7	TX_SEQ_EN	Enables Transmit Sequencer	0x0	R/W
		6	TX_SLP_CTRL	Sets Transmit Sleep Mode Control	0x0	R/W
		5	TX_SLP_HOLD	Holds the Transmit Sequencer State When Multiplier Is in Sleep Mode	0x0	R/W
		4	TX_CTL_LATCH_BYP	Bypasses the Control Latch for Transmit Controls	0x1	R/W
		[3:0]	RESERVED	Reserved	0x0	R
0x017	TX_SEQUENCER_SETUP2	7	RESERVED	Reserved	0x0	R
		[6:0]	TX_STATES	Sets Transmit Sequencer Depth	0x0	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x018	MULT_SEQUENCER_SETUP	7	MULT_SEQ_EN	Enables Multiplier Sequencer	0x0	R/W
		6	MULT_SLP_CTRL	Sets Multiplier Sleep Mode Control	0x0	R/W
		5	MULT_SLP_HOLD	Holds the Multiplier Sequencer State When Transmit Is in Sleep Mode	0x0	R/W
		4	MULT_CTL_LATCH_BYP	Bypasses the Control Latch for Multiplier Controls	0x1	R/W
		[3:0]	MULT_STATES	Sets Multiplier Sequencer Depth	0x0	R/W
0x019	TX_STATES_1_2	[7:4]	TX_STATE_1	Mode Select for Transmit Sequencer State 1	0x0	R/W
		[3:0]	TX_STATE_2	Mode Select for Transmit Sequencer State 2	0x0	R/W
0x01A	TX_STATES_3_4	[7:4]	TX_STATE_3	Mode Select for Transmit Sequencer State 3	0x0	R/W
		[3:0]	TX_STATE_4	Mode Select for Transmit Sequencer State 4	0x0	R/W
0x01B	TX_STATES_5_6	[7:4]	TX_STATE_5	Mode Select for Transmit Sequencer State 5	0x0	R/W
		[3:0]	TX_STATE_6	Mode Select for Transmit Sequencer State 6	0x0	R/W
0x01C	TX_STATES_7_8	[7:4]	TX_STATE_7	Mode Select for Transmit Sequencer State 7	0x0	R/W
		[3:0]	TX_STATE_8	Mode Select for Transmit Sequencer State 8	0x0	R/W
0x01D	TX_STATES_9_10	[7:4]	TX_STATE_9	Mode Select for Transmit Sequencer State 9	0x0	R/W
		[3:0]	TX_STATE_10	Mode Select for Transmit Sequencer State 10	0x0	R/W
0x01E	TX_STATES_11_12	[7:4]	TX_STATE_11	Mode Select for Transmit Sequencer State 11	0x0	R/W
		[3:0]	TX_STATE_12	Mode Select for Transmit Sequencer State 12	0x0	R/W
0x01F	TX_STATES_13_14	[7:4]	TX_STATE_13	Mode Select for Transmit Sequencer State 13	0x0	R/W
		[3:0]	TX_STATE_14	Mode Select for Transmit Sequencer State 14	0x0	R/W
0x020	TX_STATES_15_16	[7:4]	TX_STATE_15	Mode Select for Transmit Sequencer State 15	0x0	R/W
		[3:0]	TX_STATE_16	Mode Select for Transmit Sequencer State 16	0x0	R/W
0x021	TX_STATES_17_18	[7:4]	TX_STATE_17	Mode Select for Transmit Sequencer State 17	0x0	R/W
		[3:0]	TX_STATE_18	Mode Select for Transmit Sequencer State 18	0x0	R/W
0x022	TX_STATES_19_20	[7:4]	TX_STATE_19	Mode Select for Transmit Sequencer State 19	0x0	R/W
		[3:0]	TX_STATE_20	Mode Select for Transmit Sequencer State 20	0x0	R/W
0x023	TX_STATES_21_22	[7:4]	TX_STATE_21	Mode Select for Transmit Sequencer State 21	0x0	R/W
		[3:0]	TX_STATE_22	Mode Select for Transmit Sequencer State 22	0x0	R/W
0x024	TX_STATES_23_24	[7:4]	TX_STATE_23	Mode Select for Transmit Sequencer State 23	0x0	R/W
		[3:0]	TX_STATE_24	Mode Select for Transmit Sequencer State 24	0x0	R/W
0x025	TX_STATES_25_26	[7:4]	TX_STATE_25	Mode Select for Transmit Sequencer State 25	0x0	R/W
		[3:0]	TX_STATE_26	Mode Select for Transmit Sequencer State 26	0x0	R/W
0x026	TX_STATES_27_28	[7:4]	TX_STATE_27	Mode Select for Transmit Sequencer State 27	0x0	R/W
		[3:0]	TX_STATE_28	Mode Select for Transmit Sequencer State 28	0x0	R/W
0x027	TX_STATES_29_30	[7:4]	TX_STATE_29	Mode Select for Transmit Sequencer State 29	0x0	R/W
		[3:0]	TX_STATE_30	Mode Select for Transmit Sequencer State 30	0x0	R/W
0x028	TX_STATES_31_32	[7:4]	TX_STATE_31	Mode Select for Transmit Sequencer State 31	0x0	R/W
		[3:0]	TX_STATE_32	Mode Select for Transmit Sequencer State 32	0x0	R/W
0x029	TX_STATES_33_34	[7:4]	TX_STATE_33	Mode Select for Transmit Sequencer State 33	0x0	R/W
		[3:0]	TX_STATE_34	Mode Select for Transmit Sequencer State 34	0x0	R/W
0x02A	TX_STATES_35_36	[7:4]	TX_STATE_35	Mode Select for Transmit Sequencer State 35	0x0	R/W
		[3:0]	TX_STATE_36	Mode Select for Transmit Sequencer State 36	0x0	R/W
0x02B	TX_STATES_37_38	[7:4]	TX_STATE_37	Mode Select for Transmit Sequencer State 37	0x0	R/W
		[3:0]	TX_STATE_38	Mode Select for Transmit Sequencer State 38	0x0	R/W
0x02C	TX_STATES_39_40	[7:4]	TX_STATE_39	Mode Select for Transmit Sequencer State 39	0x0	R/W
		[3:0]	TX_STATE_40	Mode Select for Transmit Sequencer State 40	0x0	R/W
0x02D	TX_STATES_41_42	[7:4]	TX_STATE_41	Mode Select for Transmit Sequencer State 41	0x0	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		[3:0]	TX_STATE_42	Mode Select for Transmit Sequencer State 42	0x0	R/W
0x02E	TX_STATES_43_44	[7:4]	TX_STATE_43	Mode Select for Transmit Sequencer State 43	0x0	R/W
		[3:0]	TX_STATE_44	Mode Select for Transmit Sequencer State 44	0x0	R/W
0x02F	TX_STATES_45_46	[7:4]	TX_STATE_45	Mode Select for Transmit Sequencer State 45	0x0	R/W
		[3:0]	TX_STATE_46	Mode Select for Transmit Sequencer State 46	0x0	R/W
0x030	TX_STATES_47_48	[7:4]	TX_STATE_47	Mode Select for Transmit Sequencer State 47	0x0	R/W
		[3:0]	TX_STATE_48	Mode Select for Transmit Sequencer State 48	0x0	R/W
0x031	TX_STATES_49_50	[7:4]	TX_STATE_49	Mode Select for Transmit Sequencer State 49	0x0	R/W
		[3:0]	TX_STATE_50	Mode Select for Transmit Sequencer State 50	0x0	R/W
0x032	TX_STATES_51_52	[7:4]	TX_STATE_51	Mode Select for Transmit Sequencer State 51	0x0	R/W
		[3:0]	TX_STATE_52	Mode Select for Transmit Sequencer State 52	0x0	R/W
0x033	TX_STATES_53_54	[7:4]	TX_STATE_53	Mode Select for Transmit Sequencer State 53	0x0	R/W
		[3:0]	TX_STATE_54	Mode Select for Transmit Sequencer State 54	0x0	R/W
0x034	TX_STATES_55_56	[7:4]	TX_STATE_55	Mode Select for Transmit Sequencer State 55	0x0	R/W
		[3:0]	TX_STATE_56	Mode Select for Transmit Sequencer State 56	0x0	R/W
0x035	TX_STATES_57_58	[7:4]	TX_STATE_57	Mode Select for Transmit Sequencer State 57	0x0	R/W
		[3:0]	TX_STATE_58	Mode Select for Transmit Sequencer State 58	0x0	R/W
0x036	TX_STATES_59_60	[7:4]	TX_STATE_59	Mode Select for Transmit Sequencer State 59	0x0	R/W
		[3:0]	TX_STATE_60	Mode Select for Transmit Sequencer State 60	0x0	R/W
0x037	TX_STATES_61_62	[7:4]	TX_STATE_61	Mode Select for Transmit Sequencer State 61	0x0	R/W
		[3:0]	TX_STATE_62	Mode Select for Transmit Sequencer State 62	0x0	R/W
0x038	TX_STATES_63_64	[7:4]	TX_STATE_63	Mode Select for Transmit Sequencer State 63	0x0	R/W
		[3:0]	TX_STATE_64	Mode Select for Transmit Sequencer State 64	0x0	R/W
0x039	TX_STATES_65_66	[7:4]	TX_STATE_65	Mode Select for Transmit Sequencer State 65	0x0	R/W
		[3:0]	TX_STATE_66	Mode Select for Transmit Sequencer State 66	0x0	R/W
0x03A	TX_STATES_67_68	[7:4]	TX_STATE_67	Mode Select for Transmit Sequencer State 67	0x0	R/W
		[3:0]	TX_STATE_68	Mode Select for Transmit Sequencer State 68	0x0	R/W
0x03B	TX_STATES_69_70	[7:4]	TX_STATE_69	Mode Select for Transmit Sequencer State 69	0x0	R/W
		[3:0]	TX_STATE_70	Mode Select for Transmit Sequencer State 70	0x0	R/W
0x03C	MULT_STATES_1_2	[7:4]	MULT_STATE_1	Mode Select for Multiplier Sequencer State 1	0x0	R/W
		[3:0]	MULT_STATE_2	Mode Select for Multiplier Sequencer State 2	0x0	R/W
0x03D	MULT_STATES_3_4	[7:4]	MULT_STATE_3	Mode Select for Multiplier Sequencer State 3	0x0	R/W
		[3:0]	MULT_STATE_4	Mode Select for Multiplier Sequencer State 4	0x0	R/W
0x03E	MULT_STATES_5_6	[7:4]	MULT_STATE_5	Mode Select for Multiplier Sequencer State 5	0x0	R/W
		[3:0]	MULT_STATE_6	Mode Select for Multiplier Sequencer State 6	0x0	R/W
0x03F	MULT_STATES_7_8	[7:4]	MULT_STATE_7	Mode Select for Multiplier Sequencer State 7	0x0	R/W
		[3:0]	MULT_STATE_8	Mode Select for Multiplier Sequencer State 8	0x0	R/W
0x040	MULT_STATES_9_10	[7:4]	MULT_STATE_9	Mode Select for Multiplier Sequencer State 9	0x0	R/W
		[3:0]	MULT_STATE_10	Mode Select for Multiplier Sequencer State 10	0x0	R/W
0x041	MULT_STATES_11_12	[7:4]	MULT_STATE_11	Mode Select for Multiplier Sequencer State 11	0x0	R/W
		[3:0]	MULT_STATE_12	Mode Select for Multiplier Sequencer State 12	0x0	R/W
0x042	MULT_STATES_13_14	[7:4]	MULT_STATE_13	Mode Select for Multiplier Sequencer State 13	0x0	R/W
		[3:0]	MULT_STATE_14	Mode Select for Multiplier Sequencer State 14	0x0	R/W
0x043	MULT_STATES_15_16	[7:4]	MULT_STATE_15	Mode Select for Multiplier Sequencer State 15	0x0	R/W
		[3:0]	MULT_STATE_16	Mode Select for Multiplier Sequencer State 16	0x0	R/W
0x044	SEQUENCER_CTRL_SPI	[7:4]	RESERVED	Reserved	0x0	R
		3	MULT_RST_SPI	Resets Multiplier Sequencer	0x0	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		2	MULT_ADV_SPI	Advances Multiplier Sequencer State	0x0	R/W
		1	TX_RST_SPI	Resets Transmit Sequencer	0x0	R/W
		0	TX_ADV_SPI	Advances Transmit Sequencer State	0x0	R/W
0x045	TX_EN1_SPI	7	CH1_RDY_SPI	SPI Mode Channel 1 Ready Enable	0x0	R/W
		6	CH1_ACT_SPI	SPI Mode Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_SPI	SPI Mode Channel 2 Ready Enable	0x0	R/W
		4	CH2_ACT_SPI	SPI Mode Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_SPI	SPI Mode Channel 3 Ready Enable	0x0	R/W
		2	CH3_ACT_SPI	SPI Mode Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_SPI	SPI Mode Channel 4 Ready Enable	0x0	R/W
		0	CH4_ACT_SPI	SPI Mode Channel 4 Active Enable	0x0	R/W
0x046	TX_EN2_SPI	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_SPI	SPI Mode Active Splitter1 Enable	0x0	R/W
		1	SPLT12_EN_SPI	SPI Mode Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		0	SPLT34_EN_SPI	SPI Mode Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
0x047	MULT_EN_SPI	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_SPI	SPI Mode RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_SPI	SPI Mode Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_SPI	SPI Mode Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_SPI	SPI Mode Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_SPI	SPI Mode Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_SPI	SPI Mode High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_SPI	SPI Mode High Band Active Enable	0x0	R/W
0x048	MULT_PASS_SPI	7	BPF_SPI	SPI Mode BPF Select	0x0	R/W
		6	PA_NOTCH_SPI	SPI Mode Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_SPI	SPI Mode Attenuator Setting	0x0	R/W
0x049	DET_ENABLES	[7:4]	RESERVED	Reserved	0x0	R
		3	CH4_DET_EN	Enables Channel 4 Power Detector	0x0	R/W
		2	CH3_DET_EN	Enables Channel 3 Power Detector	0x0	R/W
		1	CH2_DET_EN	Enables Channel 2 Power Detector	0x0	R/W
		0	CH1_DET_EN	Enables Channel 1 Power Detector	0x0	R/W
0x04A	ADC_CTRL	7	ADC_CLKFREQ_SEL	ADC Clock Frequency Selection	0x0	R/W
		6	ADC_EN	Turns on Comparator and Resets State Machine	0x0	R/W
		5	CLK_EN	Turns on Clock Oscillator	0x0	R/W
		4	ST_CONV	Pulse Triggers Conversion Cycle	0x0	R/W
		[3:1]	MUX_SEL	ADC Input Signal Select	0x0	R/W
		0	ADC_EOC	ADC End of Conversion Signal	0x0	R
0x04B	ADC_OUTPUT	[7:0]	ADC	ADC Output Word	0x0	R
0x04C	TX_CURR_MODE	[7:4]	RESERVED	Reserved	0x0	R
		[3:0]	TX_CURR_MODE	Read Back Current Transmit Mode	0x0	R
0x04D	TX_CURR_STATE	7	RESERVED	Reserved	0x0	R
		[6:0]	TX_CURR_STATE	Read Back Current Transmit Sequencer Count	0x0	R
0x04E	MULT_STATUS	[7:4]	MULT_CURR_STATE	Read Back Current Multiplier Sequencer Count	0x0	R
		[3:0]	MULT_CURR_MODE	Read Back Current Multiplier Mode	0x0	R
0x04F	REV_ID	[7:0]	REV_ID	Chip Revision ID	0x0	R
0x050	TX_EN1_MODE_0	7	CH1_RDY_MD0	Transmit Mode 0 Channel 1 Ready Enable	0x0	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		6	CH1_ACT_MD0	Transmit Mode 0 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD0	Transmit Mode 0 Channel 2 Ready Enable	0x0	R/W
		4	CH2_ACT_MD0	Transmit Mode 0 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD0	Transmit Mode 0 Channel 3 Ready Enable	0x0	R/W
		2	CH3_ACT_MD0	Transmit Mode 0 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD0	Transmit Mode 0 Channel 4 Ready Enable	0x0	R/W
		0	CH4_ACT_MD0	Transmit Mode 0 Channel 4 Active Enable	0x0	R/W
0x051	TX_EN2_MODE_0	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD0	Transmit Mode 0 Active Splitter 1 Enable	0x0	R/W
		1	SPLT12_EN_MD0	Transmit Mode 0 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		0	SPLT34_EN_MD0	Transmit Mode 0 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
0x052	TX_EN1_MODE_1	7	CH1_RDY_MD1	Transmit Mode 1 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD1	Transmit Mode 1 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD1	Transmit Mode 1 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD1	Transmit Mode 1 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD1	Transmit Mode 1 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD1	Transmit Mode 1 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD1	Transmit Mode 1 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD1	Transmit Mode 1 Channel 4 Active Enable	0x0	R/W
0x053	TX_EN2_MODE_1	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD1	Transmit Mode 1 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD1	Transmit Mode 1 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD1	Transmit Mode 1 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x054	TX_EN1_MODE_2	7	CH1_RDY_MD2	Transmit Mode 2 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD2	Transmit Mode 2 Channel 1 Active Enable	0x1	R/W
		5	CH2_RDY_MD2	Transmit Mode 2 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD2	Transmit Mode 2 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD2	Transmit Mode 2 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD2	Transmit Mode 2 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD2	Transmit Mode 2 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD2	Transmit Mode 2 Channel 4 Active Enable	0x0	R/W
0x055	TX_EN2_MODE_2	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD2	Transmit Mode 2 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD2	Transmit Mode 2 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD2	Transmit Mode 2 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x056	TX_EN1_MODE_3	7	CH1_RDY_MD3	Transmit Mode 3 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD3	Transmit Mode 3 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD3	Transmit Mode 3 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD3	Transmit Mode 3 Channel 2 Active Enable	0x1	R/W
		3	CH3_RDY_MD3	Transmit Mode 3 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD3	Transmit Mode 3 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD3	Transmit Mode 3 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD3	Transmit Mode 3 Channel 4 Active Enable	0x0	R/W
0x057	TX_EN2_MODE_3	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD3	Transmit Mode 3 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD3	Transmit Mode 3 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD3	Transmit Mode 3 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x058	TX_EN1_MODE_4	7	CH1_RDY_MD4	Transmit Mode 4 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD4	Transmit Mode 4 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD4	Transmit Mode 4 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD4	Transmit Mode 4 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD4	Transmit Mode 4 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD4	Transmit Mode 4 Channel 3 Active Enable	0x1	R/W
		1	CH4_RDY_MD4	Transmit Mode 4 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD4	Transmit Mode 4 Channel 4 Active Enable	0x0	R/W
0x059	TX_EN2_MODE_4	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD4	Transmit Mode 4 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD4	Transmit Mode 4 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD4	Transmit Mode 4 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x05A	TX_EN1_MODE_5	7	CH1_RDY_MD5	Transmit Mode 5 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD5	Transmit Mode 5 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD5	Transmit Mode 5 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD5	Transmit Mode 5 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD5	Transmit Mode 5 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD5	Transmit Mode 5 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD5	Transmit Mode 5 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD5	Transmit Mode 5 Channel 4 Active Enable	0x1	R/W
0x05B	TX_EN2_MODE_5	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD5	Transmit Mode 5 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD5	Transmit Mode 5 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD5	Transmit Mode 5 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x05C	TX_EN1_MODE_6	7	CH1_RDY_MD6	Transmit Mode 6 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD6	Transmit Mode 6 Channel 1 Active Enable	0x1	R/W
		5	CH2_RDY_MD6	Transmit Mode 6 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD6	Transmit Mode 6 Channel 2 Active Enable	0x1	R/W
		3	CH3_RDY_MD6	Transmit Mode 6 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD6	Transmit Mode 6 Channel 3 Active Enable	0x1	R/W
		1	CH4_RDY_MD6	Transmit Mode 6 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD6	Transmit Mode 6 Channel 4 Active Enable	0x1	R/W
0x05D	TX_EN2_MODE_6	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD6	Transmit Mode 6 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD6	Transmit Mode 6 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD6	Transmit Mode 6 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x05E	TX_EN1_MODE_7	7	CH1_RDY_MD7	Transmit Mode 7 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD7	Transmit Mode 7 Channel 1 Active Enable	0x1	R/W
		5	CH2_RDY_MD7	Transmit Mode 7 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD7	Transmit Mode 7 Channel 2 Active Enable	0x1	R/W
		3	CH3_RDY_MD7	Transmit Mode 7 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD7	Transmit Mode 7 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD7	Transmit Mode 7 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD7	Transmit Mode 7 Channel 4 Active Enable	0x0	R/W
0x05F	TX_EN2_MODE_7	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD7	Transmit Mode 7 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD7	Transmit Mode 7 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		0	SPLT34_EN_MD7	Transmit Mode 7 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x060	TX_EN1_MODE_8	7	CH1_RDY_MD8	Transmit Mode 8 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD8	Transmit Mode 8 Channel 1 Active Enable	0x1	R/W
		5	CH2_RDY_MD8	Transmit Mode 8 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD8	Transmit Mode 8 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD8	Transmit Mode 8 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD8	Transmit Mode 8 Channel 3 Active Enable	0x1	R/W
		1	CH4_RDY_MD8	Transmit Mode 8 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD8	Transmit Mode 8 Channel 4 Active Enable	0x0	R/W
0x061	TX_EN2_MODE_8	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD8	Transmit Mode 8 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD8	Transmit Mode 8 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD8	Transmit Mode 8 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x062	TX_EN1_MODE_9	7	CH1_RDY_MD9	Transmit Mode 9 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD9	Transmit Mode 9 Channel 1 Active Enable	0x1	R/W
		5	CH2_RDY_MD9	Transmit Mode 9 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD9	Transmit Mode 9 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD9	Transmit Mode 9 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD9	Transmit Mode 9 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD9	Transmit Mode 9 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD9	Transmit Mode 9 Channel 4 Active Enable	0x1	R/W
0x063	TX_EN2_MODE_9	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD9	Transmit Mode 9 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD9	Transmit Mode 9 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD9	Transmit Mode 9 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x064	TX_EN1_MODE_10	7	CH1_RDY_MD10	Transmit Mode 10 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD10	Transmit Mode 10 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD10	Transmit Mode 10 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD10	Transmit Mode 10 Channel 2 Active Enable	0x1	R/W
		3	CH3_RDY_MD10	Transmit Mode 10 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD10	Transmit Mode 10 Channel 3 Active Enable	0x1	R/W
		1	CH4_RDY_MD10	Transmit Mode 10 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD10	Transmit Mode 10 Channel 4 Active Enable	0x0	R/W
0x065	TX_EN2_MODE_10	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD10	Transmit Mode 10 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD10	Transmit Mode 10 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD10	Transmit Mode 10 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x066	TX_EN1_MODE_11	7	CH1_RDY_MD11	Transmit Mode 11 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD11	Transmit Mode 11 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD11	Transmit Mode 11 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD11	Transmit Mode 11 Channel 2 Active Enable	0x1	R/W
		3	CH3_RDY_MD11	Transmit Mode 11 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD11	Transmit Mode 11 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD11	Transmit Mode 11 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD11	Transmit Mode 11 Channel 4 Active Enable	0x1	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x067	TX_EN2_MODE_11	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD11	Transmit Mode 11 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD11	Transmit Mode 11 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD11	Transmit Mode 11 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x068	TX_EN1_MODE_12	7	CH1_RDY_MD12	Transmit Mode 12 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD12	Transmit Mode 12 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD12	Transmit Mode 12 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD12	Transmit Mode 12 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD12	Transmit Mode 12 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD12	Transmit Mode 12 Channel 3 Active Enable	0x1	R/W
		1	CH4_RDY_MD12	Transmit Mode 12 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD12	Transmit Mode 12 Channel 4 Active Enable	0x1	R/W
0x069	TX_EN2_MODE_12	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD12	Transmit Mode 12 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD12	Transmit Mode 12 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD12	Transmit Mode 12 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x06A	TX_EN1_MODE_13	7	CH1_RDY_MD13	Transmit Mode 13 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD13	Transmit Mode 13 Channel 1 Active Enable	0x1	R/W
		5	CH2_RDY_MD13	Transmit Mode 13 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD13	Transmit Mode 13 Channel 2 Active Enable	0x1	R/W
		3	CH3_RDY_MD13	Transmit Mode 13 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD13	Transmit Mode 13 Channel 3 Active Enable	0x1	R/W
		1	CH4_RDY_MD13	Transmit Mode 13 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD13	Transmit Mode 13 Channel 4 Active Enable	0x0	R/W
0x06B	TX_EN2_MODE_13	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD13	Transmit Mode 13 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD13	Transmit Mode 13 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD13	Transmit Mode 13 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W
0x06C	TX_EN1_MODE_14	7	CH1_RDY_MD14	Transmit Mode 14 Channel 1 Ready Enable	0x1	R/W
		6	CH1_ACT_MD14	Transmit Mode 14 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD14	Transmit Mode 14 Channel 2 Ready Enable	0x1	R/W
		4	CH2_ACT_MD14	Transmit Mode 14 Channel 2 Active Enable	0x1	R/W
		3	CH3_RDY_MD14	Transmit Mode 14 Channel 3 Ready Enable	0x1	R/W
		2	CH3_ACT_MD14	Transmit Mode 14 Channel 3 Active Enable	0x1	R/W
		1	CH4_RDY_MD14	Transmit Mode 14 Channel 4 Ready Enable	0x1	R/W
		0	CH4_ACT_MD14	Transmit Mode 14 Channel 4 Active Enable	0x1	R/W
0x06D	TX_EN2_MODE_14	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD14	Transmit Mode 14 Active Splitter 1 Enable	0x1	R/W
		1	SPLT12_EN_MD14	Transmit Mode 14 Channel 1 to Channel 2 Active Splitter Enable	0x1	R/W
		0	SPLT34_EN_MD14	Transmit Mode 14 Channel 3 to Channel 4 Active Splitter Enable	0x1	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x06E	TX_EN1_MODE_15	7	CH1_RDY_MD15	Transmit Mode 15 Channel 1 Ready Enable	0x0	R/W
		6	CH1_ACT_MD15	Transmit Mode 15 Channel 1 Active Enable	0x0	R/W
		5	CH2_RDY_MD15	Transmit Mode 15 Channel 2 Ready Enable	0x0	R/W
		4	CH2_ACT_MD15	Transmit Mode 15 Channel 2 Active Enable	0x0	R/W
		3	CH3_RDY_MD15	Transmit Mode 15 Channel 3 Ready Enable	0x0	R/W
		2	CH3_ACT_MD15	Transmit Mode 15 Channel 3 Active Enable	0x0	R/W
		1	CH4_RDY_MD15	Transmit Mode 15 Channel 4 Ready Enable	0x0	R/W
		0	CH4_ACT_MD15	Transmit Mode 15 Channel 4 Active Enable	0x0	R/W
0x06F	TX_EN2_MODE_15	[7:3]	RESERVED	Reserved	0x0	R
		2	SPLT1_EN_MD15	Transmit Mode 15 Active Splitter 1 Enable	0x0	R/W
		1	SPLT12_EN_MD15	Transmit Mode 15 Channel 1 to Channel 2 Active Splitter Enable	0x0	R/W
		0	SPLT34_EN_MD15	Transmit Mode 15 Channel 3 to Channel 4 Active Splitter Enable	0x0	R/W
0x070	MULT_EN_MODE_0	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD0	Multiplier Mode 0 RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD0	Multiplier Mode 0 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD0	Multiplier Mode 0 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD0	Multiplier Mode 0 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD0	Multiplier Mode 0 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD0	Multiplier Mode 0 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD0	Multiplier Mode 0 High Band Active Enable	0x0	R/W
0x071	MULT_PASS_MODE_0	7	BPF_MD0	Multiplier Mode 0 BPF Select	0x0	R/W
		6	PA_NOTCH_MD0	Multiplier Mode 0 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD0	Multiplier Mode 0 Attenuator Setting	0x0	R/W
0x072	MULT_EN_MODE_1	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD1	Multiplier Mode 1 RF Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD1	Multiplier Mode 1 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD1	Multiplier Mode 1 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD1	Multiplier Mode 1 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD1	Multiplier Mode 1 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD1	Multiplier Mode 1 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD1	Multiplier Mode 1 High Band Active Enable	0x0	R/W
0x073	MULT_PASS_MODE_1	7	BPF_MD1	Multiplier Mode 1 BPF Select	0x0	R/W
		6	PA_NOTCH_MD1	Multiplier Mode 1 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD1	Multiplier Mode 1 Attenuator Setting	0x13	R/W
0x074	MULT_EN_MODE_2	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD2	Multiplier Mode 2 RF Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD2	Multiplier Mode 2 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD2	Multiplier Mode 2 Low Band Active Enable	0x1	R/W
		3	MULT_MID_RDY_MD2	Multiplier Mode 2 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD2	Multiplier Mode 2 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD2	Multiplier Mode 2 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD2	Multiplier Mode 2 High Band Active Enable	0x0	R/W
0x075	MULT_PASS_MODE_2	7	BPF_MD2	Multiplier Mode 2 BPF Select	0x1	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		6	PA_NOTCH_MD2	Multiplier Mode 2 Notch Filter Select	0x1	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD2	Multiplier Mode 2 Attenuator Setting	0x13	R/W
0x076	MULT_EN_MODE_3	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD3	Multiplier Mode 3 RF Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD3	Multiplier Mode 3 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD3	Multiplier Mode 3 Low Band Active Enable	0x1	R/W
		3	MULT_MID_RDY_MD3	Multiplier Mode 3 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD3	Multiplier Mode 3 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD3	Multiplier Mode 3 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD3	Multiplier Mode 3 High Band Active Enable	0x0	R/W
0x077	MULT_PASS_MODE_3	7	BPF_MD3	Multiplier Mode 3 BPF Select	0x0	R/W
		6	PA_NOTCH_MD3	Multiplier Mode 3 Notch Filter Select	0x1	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD3	Multiplier Mode 3 Attenuator Setting	0x7	R/W
0x078	MULT_EN_MODE_4	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD4	Multiplier Mode 4 RF Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD4	Multiplier Mode 4 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD4	Multiplier Mode 4 Low Band Active Enable	0x1	R/W
		3	MULT_MID_RDY_MD4	Multiplier Mode 4 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD4	Multiplier Mode 4 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD4	Multiplier Mode 4 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD4	Multiplier Mode 4 High Band Active Enable	0x0	R/W
0x079	MULT_PASS_MODE_4	7	BPF_MD4	Multiplier Mode 4 BPF Select	0x0	R/W
		6	PA_NOTCH_MD4	Multiplier Mode 4 Notch Filter Select	0x1	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD4	Multiplier Mode 4 Attenuator Setting	0x13	R/W
0x07A	MULT_EN_MODE_5	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD5	Multiplier Mode 5 RF Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD5	Multiplier Mode 5 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD5	Multiplier Mode 5 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD5	Multiplier Mode 5 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD5	Multiplier Mode 5 Mid Band Active Enable	0x1	R/W
		1	MULT_HIGH_RDY_MD5	Multiplier Mode 5 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD5	Multiplier Mode 5 High Band Active Enable	0x0	R/W
0x07B	MULT_PASS_MODE_5	7	BPF_MD5	Multiplier Mode 5 BPF Select	0x1	R/W
		6	PA_NOTCH_MD5	Multiplier Mode 5 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD5	Multiplier Mode 5 Attenuator Setting	0x1F	R/W
0x07C	MULT_EN_MODE_6	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD6	Multiplier Mode 6 RF Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD6	Multiplier Mode 6 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD6	Multiplier Mode 6 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD6	Multiplier Mode 6 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD6	Multiplier Mode 6 Mid Band Active Enable	0x1	R/W
		1	MULT_HIGH_RDY_MD6	Multiplier Mode 6 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD6	Multiplier Mode 6 High Band Active Enable	0x0	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x07D	MULT_PASS_MODE_6	7	BPF_MD6	Multiplier Mode 6 BPF Select	0x0	R/W
		6	PA_NOTCH_MD6	Multiplier Mode 6 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD6	Multiplier Mode 6 Attenuator Setting	0x1F	R/W
0x07E	MULT_EN_MODE_7	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD7	Multiplier Mode 7 RF Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD7	Multiplier Mode 7 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD7	Multiplier Mode 7 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD7	Multiplier Mode 7 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD7	Multiplier Mode 7 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD7	Multiplier Mode 7 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD7	Multiplier Mode 7 High Band Active Enable	0x1	R/W
0x07F	MULT_PASS_MODE_7	7	BPF_MD7	Multiplier Mode 7 BPF Select	0x1	R/W
		6	PA_NOTCH_MD7	Multiplier Mode 7 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD7	Multiplier Mode 7 Attenuator Setting	0x1F	R/W
0x080	MULT_EN_MODE_8	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD8	Multiplier Mode 8 RF Amplifier Enable	0x1	R/W
		5	MULT_LOW_RDY_MD8	Multiplier Mode 8 Low Band Ready Enable	0x1	R/W
		4	MULT_LOW_ACT_MD8	Multiplier Mode 8 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD8	Multiplier Mode 8 Mid Band Ready Enable	0x1	R/W
		2	MULT_MID_ACT_MD8	Multiplier Mode 8 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD8	Multiplier Mode 8 High Band Ready Enable	0x1	R/W
		0	MULT_HIGH_ACT_MD8	Multiplier Mode 8 High Band Active Enable	0x1	R/W
0x081	MULT_PASS_MODE_8	7	BPF_MD8	Multiplier Mode 8 BPF Select	0x0	R/W
		6	PA_NOTCH_MD8	Multiplier Mode 8 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD8	Multiplier Mode 8 Attenuator Setting	0x1F	R/W
0x082	MULT_EN_MODE_9	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD9	Multiplier Mode 9 RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD9	Multiplier Mode 9 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD9	Multiplier Mode 9 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD9	Multiplier Mode 9 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD9	Multiplier Mode 9 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD9	Multiplier Mode 9 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD9	Multiplier Mode 9 High Band Active Enable	0x0	R/W
0x083	MULT_PASS_MODE_9	7	BPF_MD9	Multiplier Mode 9 BPF Select	0x0	R/W
		6	PA_NOTCH_MD9	Multiplier Mode 9 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD9	Multiplier Mode 9 Attenuator Setting	0x0	R/W
0x084	MULT_EN_MODE_10	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD10	Multiplier Mode 10 RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD10	Multiplier Mode 10 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD10	Multiplier Mode 10 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD10	Multiplier Mode 10 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD10	Multiplier Mode 10 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD10	Multiplier Mode 10 High Band Ready Enable	0x0	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		0	MULT_HIGH_ACT_MD10	Multiplier Mode 10 High Band Active Enable	0x0	R/W
0x085	MULT_PASS_MODE_10	7	BPF_MD10	Multiplier Mode 10 BPF Select	0x0	R/W
		6	PA_NOTCH_MD10	Multiplier Mode 10 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD10	Multiplier Mode 10 Attenuator Setting	0x0	R/W
0x086	MULT_EN_MODE_11	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD11	Multiplier Mode 11 RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD11	Multiplier Mode 11 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD11	Multiplier Mode 11 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD11	Multiplier Mode 11 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD11	Multiplier Mode 11 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD11	Multiplier Mode 11 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD11	Multiplier Mode 11 High Band Active Enable	0x0	R/W
0x087	MULT_PASS_MODE_11	7	BPF_MD11	Multiplier Mode 11 BPF Select	0x0	R/W
		6	PA_NOTCH_MD11	Multiplier Mode 11 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD11	Multiplier Mode 11 Attenuator Setting	0x0	R/W
0x088	MULT_EN_MODE_12	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD12	Multiplier Mode 12 RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD12	Multiplier Mode 12 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD12	Multiplier Mode 12 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD12	Multiplier Mode 12 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD12	Multiplier Mode 12 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD12	Multiplier Mode 12 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD12	Multiplier Mode 12 High Band Active Enable	0x0	R/W
0x089	MULT_PASS_MODE_12	7	BPF_MD12	Multiplier Mode 12 BPF Select	0x0	R/W
		6	PA_NOTCH_MD12	Multiplier Mode 12 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD12	Multiplier Mode 12 Attenuator Setting	0x0	R/W
0x08A	MULT_EN_MODE_13	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD13	Multiplier Mode 13 RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD13	Multiplier Mode 13 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD13	Multiplier Mode 13 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD13	Multiplier Mode 13 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD13	Multiplier Mode 13 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD13	Multiplier Mode 13 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD13	Multiplier Mode 13 High Band Active Enable	0x0	R/W
0x08B	MULT_PASS_MODE_13	7	BPF_MD13	Multiplier Mode 13 BPF Select	0x0	R/W
		6	PA_NOTCH_MD13	Multiplier Mode 13 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD13	Multiplier Mode 13 Attenuator Setting	0x0	R/W
0x08C	MULT_EN_MODE_14	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD14	Multiplier Mode 14 RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD14	Multiplier Mode 14 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD14	Multiplier Mode 14 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD14	Multiplier Mode 14 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD14	Multiplier Mode 14 Mid Band Active Enable	0x0	R/W

REGISTER SUMMARY

Table 10. ADAR2001 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		1	MULT_HIGH_RDY_MD14	Multiplier Mode 14 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD14	Multiplier Mode 14 High Band Active Enable	0x0	R/W
0x08D	MULT_PASS_MODE_14	7	BPF_MD14	Multiplier Mode 14 BPF Select	0x0	R/W
		6	PA_NOTCH_MD14	Multiplier Mode 14 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD14	Multiplier Mode 14 Attenuator Setting	0x0	R/W
0x08E	MULT_EN_MODE_15	7	RESERVED	Reserved	0x0	R
		6	RFAMP_EN_MD15	Multiplier Mode 15 RF Amplifier Enable	0x0	R/W
		5	MULT_LOW_RDY_MD15	Multiplier Mode 15 Low Band Ready Enable	0x0	R/W
		4	MULT_LOW_ACT_MD15	Multiplier Mode 15 Low Band Active Enable	0x0	R/W
		3	MULT_MID_RDY_MD15	Multiplier Mode 15 Mid Band Ready Enable	0x0	R/W
		2	MULT_MID_ACT_MD15	Multiplier Mode 15 Mid Band Active Enable	0x0	R/W
		1	MULT_HIGH_RDY_MD15	Multiplier Mode 15 High Band Ready Enable	0x0	R/W
		0	MULT_HIGH_ACT_MD15	Multiplier Mode 15 High Band Active Enable	0x0	R/W
0x08F	MULT_PASS_MODE_15	7	BPF_MD15	Multiplier Mode 15 BPF Select	0x0	R/W
		6	PA_NOTCH_MD15	Multiplier Mode 15 Notch Filter Select	0x0	R/W
		5	RESERVED	Reserved	0x0	R
		[4:0]	ATTN_MD15	Multiplier Mode 15 Attenuator Setting	0x0	R/W
0x100	SCAN_MODE_EN	[7:1]	RESERVED	Reserved	0x0	R
		0	SCAN_MODE_EN	Scan Mode Enable	0x0	R/W

OUTLINE DIMENSIONS

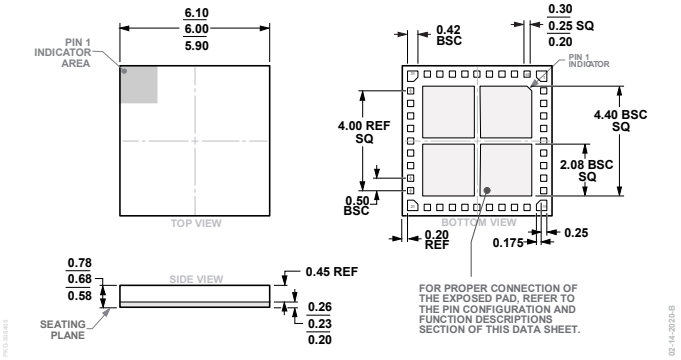

Figure 35. 40-Terminal Land Grid Array [LGA]
6 mm × 6 mm Body and 0.75 mm Package Height
(CC-40-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAR2001ACCZ	−40°C to +85°C	40-Terminal Land Grid Array [LGA], Tray	CC-40-7
ADAR2001ACCZ-R7	−40°C to +85°C	40-Terminal Land Grid Array [LGA], 7" Tape and Reel	CC-40-7

[1] Z = RoHS Compliant part.

EVALUATION BOARDS

Model[1]	Description
ADAR2001-EVALZ	Evaluation Board

[1] Z = RoHS Compliant part.