High Input Impedance, Programmable Gain, 24-Bit, 1MSPS, Alias-Free µModule® DAQ Solution

FEATURES

- Highly integrated data-acquisition solution
- Wide input common-mode range
  - Maximum unipolar input range of +24V or −24V
- 8 programmable binary gain options from 1V/V to 128V/V
- 3-pin selectable AAF gain options
  - G = 1V/V, 0.364V/V, 0.143V/V
- Fourth-order AAF with maximum flatness and linear phase
  - Full aliasing protection with 90dB typical rejection
- Excellent device-to-device phase matching and drift
- Combined precision AC and DC performance
  - Total system dynamic range up to 136dB
  - −113dB typical THD at 1kHz input tone, total gain = 1
  - 81dB typical DC CMRR at total gain = 1
  - 1pA typical input bias current at 25°C
  - ±3.3ppm typical INL
  - 5ppm/°C max gain error drift
  - ±0.5° maximum device-to-device phase mismatch at 20kHz
- Programmable output data rate, filter type, and latency
  - Linear phase digital filter options:
    - Wideband low-ripple FIR filter (256kSPS, 110kHz max input BW)
    - Sinc5 filter (1.024MSPS, 208.9kHz max input BW, 4µS max group delay)
    - Sinc3 filter (50Hz/60Hz rejection)
- Integrated LDO
- Built-in supply decoupling capacitors
- Configuration through pin strapping or SPI interface
- Digital interface optimized for isolated applications
- Suite of diagnostic check mechanisms
- Operating temperature range: −40°C to +105°C
- Available in a 12.00mm × 6.00mm 84-ball CSP_BGA with a 0.80mm ball pitch package
  - 11x footprint reduction vs. discrete solution

APPLICATIONS

- Universal input measurement platform
- Electrical test and measurement
- Sound and vibration, acoustic, and material science research and development
- Control and hardware in loop verification
- Condition monitoring for predictive maintenance
- Audio test

FUNCTIONAL BLOCK DIAGRAM

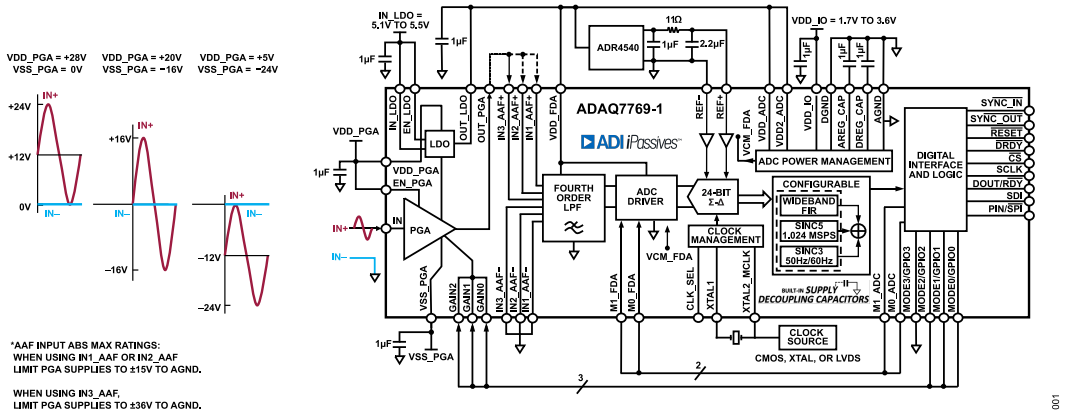

Figure 1. Functional Block Diagram

TABLE OF CONTENTS

TABLE OF CONTENTS

REVISION HISTORY

7/2025—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADAQ7769-1 is a 24-bit precision data-acquisition (DAQ) µModule® system that encapsulates signal conditioning, conversion, and processing blocks into one system in package (SiP) design that enables rapid development of highly compact, high performance precision DAQ systems.

The ADAQ7769-1 consists of:

- A low noise, low bias current, high-bandwidth programmable gain amplifier (PGA) that can be programmed to operate at binary gains of 1 to 128.
- A fourth-order, low noise, linear phase anti-aliasing filter (AAF).
- A low noise, low distortion, high bandwidth, gain-selectable ADC driver plus an optional linearity boost buffer
- A high-performance medium bandwidth 24-bit sigma delta ADC with programmable digital filter.
- A low noise, low dropout linear regulator.
- Reference buffer.
- Critical passive components required for the signal chain.

The ADAQ7769-1 supports a wide range of single-ended input amplitudes, with a maximum unipolar range of 0V to +24V or 0V to −24V, or a bipolar range of ±16V, basing its flexibility on the PGA supply voltages. With eight programmable binary PGA gain settings and three pin-selectable AAF gain settings, the ADAQ7769-1 offers additional system dynamic range and improved signal chain noise performance with input signals of lower amplitude. The input signal is fully buffered with very-low typical input bias current of 1pA. This allows easy input impedance matching and enables the ADAQ7769-1 to directly interface to sensors with high output impedance.

A fourth-order low-pass analog filter combined with the user programmable digital filter ensures the signal chain is fully protected against the high frequency noise and out of band tones presented at the input node from aliasing back into the band of interest. The analog low-pass filter is carefully designed to achieve high phase linearity and maximum in-band magnitude response flatness. Constructed with iPassives™ technology, the resistor network used within the analog low-pass filter possess superior resistance matching in both absolute values and over temperature. As a result, the signal chain performance is maintained with minimum drift over temperature and the ADAQ7769-1 has a tight phase mismatch across devices.

A high-performance ADC driver amplifier ensures the full settling of the ADC input at the maximum sampling rate. The driver circuit is designed to have minimum additive noise, error, and distortion while maintaining stability. The fully-differential architecture helps maximizing the signal chain dynamic range.

The analog-to-digital converter (ADC) inside the ADAQ7769-1 is a high performance, 24-bit precision, single channel sigma delta converter with excellent AC performance and DC precision and a throughput rate of 256kSPS from a 16.384MHz MCLK. It includes an optional linearity boost buffer that can further improve the signal chain linearity.

The ADAQ7769-1 is specified with the input reference voltage of 4.096V, but the device can support reference voltages ranging from VDD_ADC down to 1V.

The ADAQ7769-1 has two types of reference buffers. A precharge reference buffer to ease the reference input driving requirement or a full reference buffer to provide high-impedance reference input. Both buffers are optional and can be turned off through register configuration.

The ADAQ7769-1 supports three clock input types: crystal, CMOS or LVDS.

Three types of digital low-pass filters are available on the ADAQ7769-1. The wideband low-ripple FIR filter has a filter profile similar to an ideal brick wall filter, which makes it a great fit for doing frequency analysis. The Sinc5 filter has a low latency path with a smooth step response while maintaining a good level of aliasing rejection. It supports an output data rate up to 1.024MSPS from a 16.384MHz MCLK, which makes the Sinc5 filter ideal for low latency data capturing and time domain analysis. The Sinc3 filter supports a wide decimation ratio and can produce output data rate down to 50SPS from a 16.384MHz MCLK. This combined with the simultaneous 50Hz/60Hz rejection post filter makes Sinc3 filter especially useful for precision DC measurement. All the three digital filters on the ADAQ7769-1 are FIR filters with linear phase response. The bandwidth of the filters, which directly corresponds to the bandwidth of the DAQ signal chain are fully programmable through register configuration.

The ADAQ7769-1 supports two device configuration methods. The user has the option to choose to configure the device via register write through its SPI interface, or through a simple hardware pin strapping method to configure the device to operate under a number of predefined modes.

A single SPI interface supports both the register access and the sample data readback functions. The ADAQ7769-1 always acts as an SPI target. Multiple interface modes are supported with a minimum of three IO channels required to communicate with the device.

The ADAQ7769-1 features a suite of internal diagnostic functions that can detect a broad range of errors during operation to help improving the system reliability.

The ADAQ7769-1 supply connections can be greatly simplified by using its internal LDO. Note that, 0.1µF decoupling capacitors are also integrated to further reduce the number of discrete components.

On power standby, each functional block of the device can be put into standby mode. This enables the device to have a total power consumption less than 0.65mW.

GENERAL DESCRIPTION

The ADAQ7769-1 device has an operating temperature range of −40°C to +105°C and is available in a 12mm x 6mm, 84-ball BGA package with 0.8mm ball pitch package, which makes it suitable for multichannel applications. The footprint of the device is eleven times smaller compared to the footprint of the same solution using discrete components.

SPECIFICATIONS

AAF_GAIN = IN1_AAF

IN1_AAF+ = OUT_PGA, IN1_AAF− = AGND, VDD_PGA = 15V, VSS_PGA = −15V, AGND = DGND = 0V, IN_LDO = EN_LDO = 5.1V to 5.5V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2V to 5.5V, VDD_IO = 1.7V to 3.6V, REF+ = 4.096V, REF− = 0V, MCLK = SCLK = 16.384MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband low ripple, Decimation = 32, ODR = 256kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full-power mode, T_A = −40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1. Specifications using AAF_GAIN = IN1_AAF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS					
Programmable Gain Amplifier (PGA) Input	IN pin				
Input Bias Current	−40°C < T_A < 85°C		1	150	pA
	−40°C < T_A < 105°C			600	pA
PGA Common-Mode Input Range		VSS_PGA		VDD_PGA − 4	V
PGA Gain Range	PGA_GAIN = 1, 2, 4, 8, 16, 32, 64, 128	1		128	V/V
Linear Input Range	PGA_GAIN = 1		±4.096		V
Anti-Aliasing Filter (AAF) Input	IN1_AAF+/− pins				
AAF Gain	AAF_GAIN = 1		1		V/V
AAF Differential Input Range	±V_{REF}/AAF_GAIN		±4.096		V
AAF Common-Mode Input Range		−2.1		+4.5	V
AAF Common-Mode Rejection DC	DC to 60Hz, referred to IN1_AAF input		81.8		dB
AAF Common-Mode Rejection AC	f = 10kHz, referred to IN1_AAF input		71.0		dB
AAF Input Resistance, R_{IN}	Fully-differential configuration (IN1_AAF+ = positive input, IN1_AAF− = negative input)		4		kΩ
	Single-ended to differential configuration (IN1_AAF+ = input, IN1_AAF− = AGND)		2.67		kΩ
OVERALL SYSTEM DC ACCURACY					
Gain Error[1]	All PGA_GAIN, RTI	−0.16	−0.07	+0.06	%
Gain Error Drift[1, 2]	Endpoint Method				
	PGA_GAIN = 1 to 64	0.0	1.6	3.0	ppm/°C
	PGA_GAIN = 128	0.1	2.4	4.8	ppm/°C
Offset Error[1]	RTI, T_A = 25°C				
	PGA_GAIN = 1		±(10+390/PGA_GAIN)	±1100	µV
	PGA_GAIN = 2 to 128		±(10+390/PGA_GAIN)		µV
Offset Error Drift[1, 2]	RTI, Endpoint Method				
	PGA_GAIN = 1	−13.1	0.1−(3.1/PGA_GAIN)	4.2	µV/°C
	PGA_GAIN = 2 to 128		0.1−(3.1/PGA_GAIN)		µV/°C
Integral Nonlinearity (INL)[3]	Endpoint Method				
	PGA_GAIN = 1		±3.3		ppm of linear input range
	PGA_GAIN = 16		±7.6		ppm of linear input range
	PGA_GAIN = 128		±75.0		ppm of linear input range
Low-Frequency Noise	Sinc3 filter, ODR = 50SPS, BW = 15Hz, shorted input, RTI				
	PGA_GAIN = 1		0.37		µV rms
	PGA_GAIN = 2		0.22		µV rms

SPECIFICATIONS

Table 1. Specifications using AAF_GAIN = IN1_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 4		0.12		µV rms
	PGA_GAIN = 8		0.08		µV rms
	PGA_GAIN = 16		0.05		µV rms
	PGA_GAIN = 32		0.05		µV rms
	PGA_GAIN = 64		0.04		µV rms
	PGA_GAIN = 128		0.04		µV rms
Peak-to-Peak Resolution[4]	Sinc3 filter, ODR = 50SPS, BW = 15Hz, shorted input, RTI				
	PGA_GAIN = 1		20.7		Bits
	PGA_GAIN = 2		20.4		Bits
	PGA_GAIN = 4		20.3		Bits
	PGA_GAIN = 8		19.9		Bits
	PGA_GAIN = 16		19.6		Bits
	PGA_GAIN = 32		18.6		Bits
	PGA_GAIN = 64		17.8		Bits
	PGA_GAIN = 128		17.0		Bits
OVERALL SYSTEM AC PERFORMANCE	Wideband low-ripple FIR filter, ODR = 256kSPS, DEC_RATE = 32, BW = 110.8kHz				
Dynamic Range (DR)[5]	Shorted input				
	PGA_GAIN = 1	105.5	107.6		dB
	PGA_GAIN = 2		106.7		dB
	PGA_GAIN = 4		105.1		dB
	PGA_GAIN = 8		102.3		dB
	PGA_GAIN = 16		98.4		dB
	PGA_GAIN = 32		93.6		dB
	PGA_GAIN = 64		88.3		dB
	PGA_GAIN = 128		83.2		dB
	Total system DR		125.5		dB
Noise Spectral Density	RTI, shorted input, at 1kHz				
	PGA_GAIN = 1		36		nV/√Hz
	PGA_GAIN = 2		20		nV/√Hz
	PGA_GAIN = 4		12		nV/√Hz
	PGA_GAIN = 8		8.4		nV/√Hz
	PGA_GAIN = 16		6.6		nV/√Hz
	PGA_GAIN = 32		5.7		nV/√Hz
	PGA_GAIN = 64		5.1		nV/√Hz
	PGA_GAIN = 128		4.8		nV/√Hz
Total RMS Noise	RTI, shorted input				
	PGA_GAIN = 1		12.0		µV rms
	PGA_GAIN = 2		6.7		µV rms
	PGA_GAIN = 4		4.1		µV rms
	PGA_GAIN = 8		2.8		µV rms
	PGA_GAIN = 16		2.2		µV rms
	PGA_GAIN = 32		1.9		µV rms
	PGA_GAIN = 64		1.7		µV rms
	PGA_GAIN = 128		1.6		µV rms
Signal-to-Noise Ratio (SNR)	−0.5dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 3.87Vp		105.8		dB
	PGA_GAIN = 2, 1.93Vp		105.0		dB

SPECIFICATIONS

Table 1. Specifications using AAF_GAIN = IN1_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 4, 0.97Vp		103.4		dB
	PGA_GAIN = 8, 0.48Vp		100.8		dB
	PGA_GAIN = 16, 0.24Vp		97.0		dB
	PGA_GAIN = 32, 0.12Vp		92.0		dB
	PGA_GAIN = 64, 0.060Vp		86.9		dB
	PGA_GAIN = 128, 0.030Vp		81.9		dB
Total Harmonic Distortion (THD)	−0.5dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 3.87Vp		−113.4		dB
	PGA_GAIN = 2, 1.93Vp		−112.1		dB
	PGA_GAIN = 4, 0.97Vp		−113.8		dB
	PGA_GAIN = 8, 0.48Vp		−114.6		dB
	PGA_GAIN = 16, 0.24Vp		−116.1		dB
	PGA_GAIN = 32, 0.12Vp		−116.1		dB
	PGA_GAIN = 64, 0.060Vp		−111.6		dB
	PGA_GAIN = 128, 0.030Vp		−104.1		dB
Signal-to-Noise and Distortion Ratio (SINAD)	−0.5dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 3.87Vp		105.1		dB
	PGA_GAIN = 2, 1.93Vp		104.2		dB
	PGA_GAIN = 4, 0.97Vp		103.0		dB
	PGA_GAIN = 8, 0.48Vp		100.6		dB
	PGA_GAIN = 16, 0.24Vp		97.0		dB
	PGA_GAIN = 32, 0.12Vp		92.0		dB
	PGA_GAIN = 64, 0.060Vp		86.9		dB
	PGA_GAIN = 128, 0.030Vp		81.9		dB
Spurious-Free Dynamic Range (SFDR)	−0.5dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 3.87Vp		−114.6		dBc
	PGA_GAIN = 2, 1.93Vp		−112.6		dBc
	PGA_GAIN = 4, 0.97Vp		−115.1		dBc
	PGA_GAIN = 8, 0.48Vp		−116.9		dBc
	PGA_GAIN = 16, 0.24Vp		−118.9		dBc
	PGA_GAIN = 32, 0.12Vp		−121.8		dBc
	PGA_GAIN = 64, 0.060Vp		−113.7		dBc
	PGA_GAIN = 128, 0.030Vp		−105.6		dBc
Intermodulation Distortion (IMD)	f_{IN_A} = 9kHz, f_{IN_B} = 10kHz				
	Second-order				
	PGA_GAIN = 1		−115		dBc
	PGA_GAIN = 2		−106		dBc
	PGA_GAIN = 4		−115		dBc
	PGA_GAIN = 8		−117		dBc
	PGA_GAIN = 16		−113		dBc
	PGA_GAIN = 32		−109		dBc
	PGA_GAIN = 64		−104		dBc
	PGA_GAIN = 128		−98		dBc
	Third-order				
	PGA_GAIN = 1 to 16		−120		dBc
	PGA_GAIN = 32		−118		dBc
	PGA_GAIN = 64		−115		dBc
	PGA_GAIN = 128		−110		dBc

SPECIFICATIONS

Table 1. Specifications using AAF_GAIN = IN1_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG FRONT-END (AFE) MAGNITUDE AND PHASE PERFORMANCE[6]					
AFE Bandwidth	−3dB relative to signal amplitude at DC				
	PGA_GAIN = 1		358.2		kHz
	PGA_GAIN = 2		382.7		kHz
	PGA_GAIN = 4		375.1		kHz
	PGA_GAIN = 8		366.9		kHz
	PGA_GAIN = 16		351.3		kHz
	PGA_GAIN = 32		309.1		kHz
	PGA_GAIN = 64		224.8		kHz
	PGA_GAIN = 128		117.2		kHz
Analog Group Delay	f_{IN} = 20 kHz				
	PGA_GAIN = 1		0.81		µs
	PGA_GAIN = 2		0.69		µs
	PGA_GAIN = 4		0.73		µs
	PGA_GAIN = 8		0.81		µs
	PGA_GAIN = 16		0.92		µs
	PGA_GAIN = 32		1.11		µs
	PGA_GAIN = 64		1.44		µs
	PGA_GAIN = 128		2.10		µs
Phase Angle Mismatch over Gain[2, 3, 6]	Sine wave, f_{IN} = 20kHz, single device, normalized to PGA_GAIN = 1, T_A = 25°C				
	PGA_GAIN = 2	−0.936	−0.865	−0.793	Degrees
	PGA_GAIN = 4	−0.595	−0.531	−0.467	Degrees
	PGA_GAIN = 8	0.006	0.063	0.119	Degrees
	PGA_GAIN = 16	0.774	0.842	0.910	Degrees
	PGA_GAIN = 32	2.036	2.155	2.273	Degrees
	PGA_GAIN = 64	4.360	4.594	4.829	Degrees
	PGA_GAIN = 128	8.868	9.336	9.804	Degrees
Phase Angle Drift[2, 3, 6]	f_{IN} = 20kHz				
	PGA_GAIN = 1	0.13	0.20	0.26	m°/°C
	PGA_GAIN = 2	−0.01	0.05	0.12	m°/°C
	PGA_GAIN = 4	0.25	0.32	0.39	m°/°C
	PGA_GAIN = 8	0.61	0.82	1.03	m°/°C
	PGA_GAIN = 16	1.24	1.72	2.20	m°/°C
	PGA_GAIN = 32	2.46	3.47	4.47	m°/°C
	PGA_GAIN = 64	4.88	6.89	8.90	m°/°C
	PGA_GAIN = 128	9.52	13.47	17.42	m°/°C
Device-to-Device Phase Angle Mismatch[2, 3, 6]	f_{IN} = 20kHz, typical = ±1σ, T_A = 25°C				
	PGA_GAIN = 1	−0.038	±0.013	0.038	Degrees
	PGA_GAIN = 2	−0.079	±0.020	0.079	Degrees
	PGA_GAIN = 4	−0.073	±0.018	0.073	Degrees
	PGA_GAIN = 8	−0.067	±0.017	0.067	Degrees
	PGA_GAIN = 16	−0.078	±0.020	0.078	Degrees
	PGA_GAIN = 32	−0.126	±0.032	0.126	Degrees
	PGA_GAIN = 64	−0.240	±0.060	0.240	Degrees
	PGA_GAIN = 128	−0.471	±0.118	0.471	Degrees

SPECIFICATIONS

Table 1. Specifications using AAF_GAIN = IN1_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Device-to-Device Phase Angle Mismatch Drift[2, 3, 6]	f_{IN} = 20kHz, typical = |1σ| per °C				
	PGA_GAIN = 1		0.2	1.0	µ°/°C
	PGA_GAIN = 2		−2.7	−11.0	µ°/°C
	PGA_GAIN = 4		−2.6	−10.4	µ°/°C
	PGA_GAIN = 8		0.1	0.4	µ°/°C
	PGA_GAIN = 16		9.1	36.6	µ°/°C
	PGA_GAIN = 32		32.1	128.3	µ°/°C
	PGA_GAIN = 64		72.4	289.6	µ°/°C
	PGA_GAIN = 128		141.5	565.9	µ°/°C
Magnitude Flatness	f_{IN} = 20kHz				
	PGA_GAIN = 1 to 16		±0.005		dB
	PGA_GAIN = 32		−0.010		dB
	PGA_GAIN = 64		−0.030		dB
	PGA_GAIN = 128		−0.100		dB
	f_{IN} = 100kHz				
	PGA_GAIN = 1 to 16		±0.10		dB
	PGA_GAIN = 32		−0.10		dB
	PGA_GAIN = 64		−0.50		dB
	PGA_GAIN = 128		−2.00		dB
Alias Rejection	All PGA_GAIN, −6.0dBFS input signal at MCLK = 16.384MHz		90		dB
POWER SUPPLY CURRENT					
VDD_PGA	IN = AGND		1.3		mA
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		1.35		mA rms
	Full-scale DC input with common mode = AGND, any PGA_GAIN		2.4		mA
VSS_PGA	IN = AGND		−2.0		mA
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		−2.1		mA rms
	Full-scale DC input with common mode = AGND, any PGA_GAIN		−1.3		mA
VDD_FDA	IN1_AAF+ = IN1_AAF− = AGND		4.9		mA
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		5.0		mA rms
	Full-scale DC input with common mode = AGND, any PGA_GAIN		4.8		mA
	Standby		120		µA
VDD_ADC	Linearity boost buffer on, reference precharge buffer on		6.3		mA
	Linearity boost buffer off, reference precharge buffers off		2.4		mA
	Standby		205		µA
VDD2_ADC			4.7		mA
	Standby		30		µA
VDD_IO					
Sinc3 Filter			3.5		mA
Sinc5 Filter			3.7		mA
Wideband Low-Ripple FIR Filter			9.1		mA

SPECIFICATIONS

Table 1. Specifications using AAF_GAIN = IN1_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Standby			380		µA
POWER DISSIPATION	VDD_PGA = 15V, VSS_PGA = −15V, IN_LDO = EN_LDO = 5.3 V, OUT_LDO = VDD_FDA = VDD_ADC = VDD2_ADC, VDD_IO = 3.3 V, linearity boost buffer on, reference precharge buffer on, external CMOS MCLK				
Full Operating Mode					
Sinc3 Filter	IN = AGND, any PGA_GAIN		145		mW
Sinc5 Filter	IN = AGND, any PGA_GAIN		146		mW
Wideband Low-Ripple FIR Filter	IN = AGND, any PGA_GAIN		164		mW
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		167		mW
	Full-scale DC input with common mode = AGND, any PGA_GAIN		169		mW
Standby Mode	FDA in standby mode, and ADC in standby mode		3.14		mW
ADC Power-Down	FDA in standby mode, and ADC in power-down mode		0.65		mW

[1] Tester repeatability and reproducibility guard band is not included.

[2] Limits calculated based on the characterization data of 50 samples from one nominal wafer from −40°C to +105°C.

[3] Specification is not production tested but is supported by characterization data at initial product release.

[4] For peak-to-peak resolution, see the Terminology section. Noise used in calculation is listed under the Low-Frequency Noise specification.

[5] For more details on dynamic range and noise across different gain and filter configurations, see the Noise Performance section.

[6] For AFE performance, terminology, and calculation, see the Calculations on AFE Phase Performance section.

SPECIFICATIONS

AAF_GAIN = IN2_AAF

IN2_AAF+ = OUT_PGA, IN2_AAF− = AGND, VDD_PGA = 15V, VSS_PGA = −15V, AGND = DGND = 0V, IN_LDO = EN_LDO = 5.1V to 5.5V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2V to 5.5V, VDD_IO = 1.7V to 3.6V, REF+ = 4.096V, REF− = 0V, MCLK = SCLK = 16.384MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband low ripple, Decimation = 32, ODR = 256kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full-power mode, T_A = −40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 2. Specifications using AAF_GAIN = IN2_AAF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS					
PGA Input	IN pin				
Input Bias Current	−40°C < T_A < 85°C		1	150	pA
	−40°C < T_A < 105°C			600	pA
PGA Common-Mode Input Range		VSS_PGA		VDD_PGA − 4	V
PGA Gain Range	PGA_GAIN = 1, 2, 4, 8, 16, 32, 64, 128	1		128	V/V
Linear Input Range	PGA_GAIN = 1		±11.264		V
AAF Input	IN2_AAF+/− pins				
AAF Gain	AAF_GAIN = 0.364		4/11		V/V
AAF Differential Input Range	±V_{REF}/AAF_GAIN		±11.264		V
AAF Common-Mode Input Range		−6.1		+6.2	V
AAF Common-Mode Rejection DC	DC to 60Hz, referred to IN2_AAF input		81.9		dB
AAF Common-Mode Rejection AC	f = 10kHz, referred to IN2_AAF input		78.8		dB
AAF Input Resistance, R_{IN}	Fully-differential configuration (IN2_AAF+ = positive input, IN2_AAF− = negative input)		11		kΩ
	Single-ended to differential configuration (IN2_AAF+ = input, IN2_AAF− = AGND)		6.35		kΩ
OVERALL SYSTEM DC ACCURACY					
Gain Error[1]	All PGA_GAIN, RTI	−0.12	−0.02	+0.10	%
Gain Error Drift[1, 2]	Endpoint Method				
	PGA_GAIN = 1 to 64	−0.9	+0.9	+2.3	ppm/°C
	PGA_GAIN = 128	−0.6	+1.7	+4.0	ppm/°C
Offset Error[1]	RTI, T_A = 25°C				
	PGA_GAIN = 1		±(10+620/PGA_GAIN)	±1600	µV
	PGA_GAIN = 2 to 128		±(10+620/PGA_GAIN)		µV
Offset Error Drift[1, 2]	RTI, Endpoint Method				
	PGA_GAIN = 1	−23.4	0.1−(5.1/PGA_GAIN)	9.4	µV/°C
	PGA_GAIN = 2 to 128		0.1−(5.1/PGA_GAIN)		µV/°C
INL[3]	Endpoint Method				
	PGA_GAIN = 1		±2.0		ppm of linear input range
	PGA_GAIN = 16		±2.6		ppm of linear input range
	PGA_GAIN = 128		±19.9		ppm of linear input range
Low-Frequency Noise	Sinc3 filter, ODR = 50SPS, BW = 15Hz, shorted input, RTI				
	PGA_GAIN = 1		1.08		µV rms
	PGA_GAIN = 2		0.73		µV rms

SPECIFICATIONS

Table 2. Specifications using AAF_GAIN = IN2_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 4		0.25		µV rms
	PGA_GAIN = 8		0.12		µV rms
	PGA_GAIN = 16		0.08		µV rms
	PGA_GAIN = 32		0.08		µV rms
	PGA_GAIN = 64		0.06		µV rms
	PGA_GAIN = 128		0.07		µV rms
Peak-to-Peak Resolution[4]	Sinc3 filter, ODR = 50SPS, BW = 15Hz, shorted input, RTI				
	PGA_GAIN = 1		20.6		Bits
	PGA_GAIN = 2		20.2		Bits
	PGA_GAIN = 4		20.7		Bits
	PGA_GAIN = 8		20.7		Bits
	PGA_GAIN = 16		20.4		Bits
	PGA_GAIN = 32		19.3		Bits
	PGA_GAIN = 64		18.8		Bits
	PGA_GAIN = 128		17.6		Bits
OVERALL SYSTEM AC PERFORMANCE	Wideband low-ripple FIR filter, ODR = 256kSPS, DEC_RATE = 32, BW = 110.8kHz				
DR[5]	Shorted input				
	PGA_GAIN = 1	105.5	108.1		dB
	PGA_GAIN = 2		108.0		dB
	PGA_GAIN = 4		107.6		dB
	PGA_GAIN = 8		106.8		dB
	PGA_GAIN = 16		104.9		dB
	PGA_GAIN = 32		101.4		dB
	PGA_GAIN = 64		96.9		dB
	PGA_GAIN = 128		91.9		dB
	Total system DR		134.0		dB
Noise Spectral Density	RTI, shorted input, at 1kHz				
	PGA_GAIN = 1		95		nV/√Hz
	PGA_GAIN = 2		48		nV/√Hz
	PGA_GAIN = 4		25		nV/√Hz
	PGA_GAIN = 8		14		nV/√Hz
	PGA_GAIN = 16		8.4		nV/√Hz
	PGA_GAIN = 32		6.3		nV/√Hz
	PGA_GAIN = 64		5.4		nV/√Hz
	PGA_GAIN = 128		4.8		nV/√Hz
Total RMS Noise	RTI, shorted input				
	PGA_GAIN = 1		31.5		µV rms
	PGA_GAIN = 2		15.8		µV rms
	PGA_GAIN = 4		8.3		µV rms
	PGA_GAIN = 8		4.6		µV rms
	PGA_GAIN = 16		2.8		µV rms
	PGA_GAIN = 32		2.1		µV rms
	PGA_GAIN = 64		1.8		µV rms
	PGA_GAIN = 128		1.6		µV rms
SNR	−0.5dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 10.6Vp		106.0		dB
	PGA_GAIN = 2, 5.32Vp		105.8		dB

SPECIFICATIONS

Table 2. Specifications using AAF_GAIN = IN2_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 4, 2.66Vp		105.6		dB
	PGA_GAIN = 8, 1.33Vp		104.7		dB
	PGA_GAIN = 16, 0.67Vp		102.9		dB
	PGA_GAIN = 32, 0.33Vp		99.7		dB
	PGA_GAIN = 64, 0.16Vp		95.2		dB
	PGA_GAIN = 128, 0.083Vp		90.3		dB
THD	−0.5dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 10.6Vp		−111.6		dB
	PGA_GAIN = 2, 5.32Vp		−105.2		dB
	PGA_GAIN = 4, 2.66Vp		−114.8		dB
	PGA_GAIN = 8, 1.33Vp		−118.1		dB
	PGA_GAIN = 16, 0.67Vp		−117.8		dB
	PGA_GAIN = 32, 0.33Vp		−116.2		dB
	PGA_GAIN = 64, 0.16Vp		−112.5		dB
	PGA_GAIN = 128, 0.083Vp		−106.9		dB
SINAD	−0.5dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 10.6Vp		104.9		dB
	PGA_GAIN = 2, 5.32Vp		102.4		dB
	PGA_GAIN = 4, 2.66Vp		105.1		dB
	PGA_GAIN = 8, 1.33Vp		104.5		dB
	PGA_GAIN = 16, 0.67Vp		102.7		dB
	PGA_GAIN = 32, 0.33Vp		99.5		dB
	PGA_GAIN = 64, 0.16Vp		95.1		dB
	PGA_GAIN = 128, 0.083Vp		90.2		dB
SFDR	−0.5dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 10.6Vp		−116.6		dBc
	PGA_GAIN = 2, 5.32Vp		−104.3		dBc
	PGA_GAIN = 4, 2.66Vp		−115.4		dBc
	PGA_GAIN = 8, 1.33Vp		−124.1		dBc
	PGA_GAIN = 16, 0.67Vp		−129.4		dBc
	PGA_GAIN = 32, 0.33Vp		−126.0		dBc
	PGA_GAIN = 64, 0.16Vp		−115.3		dBc
	PGA_GAIN = 128, 0.083Vp		−109.3		dBc
IMD	f_{IN_A} = 9kHz, f_{IN_B} = 10kHz				
	Second-order				
	PGA_GAIN = 1		−105		dBc
	PGA_GAIN = 2		−93		dBc
	PGA_GAIN = 4		−107		dBc
	PGA_GAIN = 8		−116		dBc
	PGA_GAIN = 16		−110		dBc
	PGA_GAIN = 32		−107		dBc
	PGA_GAIN = 64		−104		dBc
	PGA_GAIN = 128		−100		dBc
	Third-order				
	PGA_GAIN = 1		−113		dBc
	PGA_GAIN = 2		−117		dBc
	PGA_GAIN = 4		−119		dBc
	PGA_GAIN = 8		−118		dBc
	PGA_GAIN = 16		−116		dBc

SPECIFICATIONS

Table 2. Specifications using AAF_GAIN = IN2_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 32		−115		dBc
	PGA_GAIN = 64		−112		dBc
	PGA_GAIN = 128		−108		dBc
AFE MAGNITUDE AND PHASE PERFORMANCE[6]					
AFE Bandwidth	−3dB relative to signal amplitude at DC				
	PGA_GAIN = 1		299.3		kHz
	PGA_GAIN = 2		312.6		kHz
	PGA_GAIN = 4		308.7		kHz
	PGA_GAIN = 8		303.1		kHz
	PGA_GAIN = 16		293.5		kHz
	PGA_GAIN = 32		265.4		kHz
	PGA_GAIN = 64		202.6		kHz
	PGA_GAIN = 128		116.1		kHz
Analog Group Delay	f_{IN} = 20kHz				
	PGA_GAIN = 1		1.05		µs
	PGA_GAIN = 2		0.93		µs
	PGA_GAIN = 4		0.98		µs
	PGA_GAIN = 8		1.06		µs
	PGA_GAIN = 16		1.17		µs
	PGA_GAIN = 32		1.35		µs
	PGA_GAIN = 64		1.68		µs
	PGA_GAIN = 128		2.34		µs
Phase Angle Mismatch over Gain[2, 3, 6]	Sine wave, f_{IN} = 20kHz, single device, normalized to PGA_GAIN = 1, T_A = 25°C				
	PGA_GAIN = 2	−0.936	−0.863	−0.791	Degrees
	PGA_GAIN = 4	−0.595	−0.531	−0.466	Degrees
	PGA_GAIN = 8	−0.003	0.054	0.122	Degrees
	PGA_GAIN = 16	0.779	0.847	0.914	Degrees
	PGA_GAIN = 32	2.036	2.155	2.273	Degrees
	PGA_GAIN = 64	4.335	4.570	4.805	Degrees
	PGA_GAIN = 128	8.807	9.275	9.743	Degrees
Phase Angle Drift[2, 3, 6]	f_{IN} = 20kHz				
	PGA_GAIN = 1	0.11	0.23	0.35	m°/°C
	PGA_GAIN = 2	−0.03	0.09	0.20	m°/°C
	PGA_GAIN = 4	0.24	0.35	0.47	m°/°C
	PGA_GAIN = 8	0.63	0.86	1.08	m°/°C
	PGA_GAIN = 16	1.25	1.76	2.27	m°/°C
	PGA_GAIN = 32	2.49	3.50	4.51	m°/°C
	PGA_GAIN = 64	4.90	6.92	8.94	m°/°C
	PGA_GAIN = 128	9.59	13.50	17.40	m°/°C
Device-to-Device Phase Angle Mismatch[2, 3, 6]	f_{IN} = 20kHz, typical = ±1σ, T_A = 25°C				
	PGA_GAIN = 1	−0.051	±0.015	0.051	Degrees
	PGA_GAIN = 2	−0.088	±0.022	0.088	Degrees
	PGA_GAIN = 4	−0.082	±0.021	0.082	Degrees
	PGA_GAIN = 8	−0.077	±0.019	0.077	Degrees
	PGA_GAIN = 16	−0.087	±0.022	0.087	Degrees
	PGA_GAIN = 32	−0.133	±0.033	0.133	Degrees
	PGA_GAIN = 64	−0.244	±0.061	0.244	Degrees

SPECIFICATIONS

Table 2. Specifications using AAF_GAIN = IN2_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 128	−0.475	±0.119	0.475	Degrees
Device-to-Device Phase Angle Mismatch Drift[2, 3, 6]	f_{IN} = 20kHz, typical = |1σ| per °C				
	PGA_GAIN = 1		−3.9	−15.8	µ°/°C
	PGA_GAIN = 2		−3.3	−13.1	µ°/°C
	PGA_GAIN = 4		−3.9	−15.7	µ°/°C
	PGA_GAIN = 8		0.9	3.5	µ°/°C
	PGA_GAIN = 16		12.7	50.7	µ°/°C
	PGA_GAIN = 32		37.2	148.8	µ°/°C
	PGA_GAIN = 64		87.7	350.9	µ°/°C
	PGA_GAIN = 128		165.5	661.8	µ°/°C
Magnitude Flatness	f_{IN} = 20kHz				
	PGA_GAIN = 1 to 16		±0.005		dB
	PGA_GAIN = 32		−0.010		dB
	PGA_GAIN = 64		−0.030		dB
	PGA_GAIN = 128		−0.100		dB
	f_{IN} = 100kHz				
	PGA_GAIN = 1 to 16		±0.10		dB
	PGA_GAIN = 32		−0.15		dB
	PGA_GAIN = 64		−0.60		dB
	PGA_GAIN = 128		−2.00		dB
Alias Rejection	All PGA_GAIN, −6.0dBFS input signal at MCLK = 16.384MHz		90		dB
POWER SUPPLY CURRENT					
VDD_PGA	IN = AGND		1.33		mA
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		1.6		mA rms
	Full-scale DC input with common mode = AGND, any PGA_GAIN		3.4		mA
VSS_PGA	IN = AGND		−1.7		mA
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		−2.0		mA rms
	Full-scale DC input with common mode = AGND, any PGA_GAIN		−1.25		mA
VDD_FDA	IN2_AAF+ = IN2_AAF− = AGND		4.4		mA
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		4.7		mA rms
	Full-scale DC input with common mode = AGND, any PGA_GAIN		4.3		mA
	Standby		120		µA
VDD_ADC	Linearity boost buffer on, reference precharge buffer on		6.3		mA
	Linearity boost buffer off, reference precharge buffers off		2.4		mA
	Standby		205		µA
VDD2_ADC			4.7		mA
	Standby		30		µA
VDD_IO					
Sinc3 Filter			3.5		mA
Sinc5 Filter			3.7		mA

SPECIFICATIONS

Table 2. Specifications using AAF_GAIN = IN2_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Wideband Low-Ripple FIR Filter			9.1		mA
Standby			380		µA
POWER DISSIPATION	VDD_PGA = 15V, VSS_PGA = −15V, IN_LDO = EN_LDO = 5.3 V, OUT_LDO = VDD_FDA = VDD_ADC = VDD2_ADC, VDD_IO = 3.3 V, linearity boost buffer on, reference precharge buffer on, external CMOS MCLK				
Full Operating Mode					
Sinc3 Filter	IN = AGND, any PGA_GAIN		139		mW
Sinc5 Filter	IN = AGND, any PGA_GAIN		139		mW
Wideband Low-Ripple FIR Filter	IN = AGND, any PGA_GAIN		157		mW
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		167		mW
	Full-scale DC input with common mode = AGND, any PGA_GAIN		181		mW
Standby Mode	FDA in standby mode, and ADC in standby mode		3.14		mW
ADC Power-Down	FDA in standby mode, and ADC in power-down mode		0.65		mW

[1] Tester repeatability and reproducibility guard band is not included.

[2] Limits calculated based on the characterization data of 50 samples from one nominal wafer from −40°C to +105°C.

[3] Specification is not production tested but is supported by characterization data at initial product release.

[4] For peak-to-peak resolution, see the Terminology section. Noise used in calculation is listed under the Low-Frequency Noise specification.

[5] For more details on dynamic range and noise across different gain and filter configurations, see the Noise Performance section.

[6] For AFE performance, terminology, and calculation, see the Calculations on AFE Phase Performance section.

SPECIFICATIONS

AAF_GAIN = IN3_AAF

IN3_AAF+ = OUT_PGA, IN3_AAF− = AGND, VDD_PGA = 20V, VSS_PGA = −16V, AGND = DGND = 0V, IN_LDO = EN_LDO = 5.1V to 5.5V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2V to 5.5V, VDD_IO = 1.7V to 3.6V, REF+ = 4.096V, REF− = 0V, MCLK = SCLK = 16.384MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband low ripple, Decimation = 32, ODR = 256kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full-power mode, T_A = −40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 3. Specifications using AAF_GAIN = IN3_AAF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS					
PGA Input	IN pin				
Input Bias Current	−40°C < T_A < 85°C		1	150	pA
	−40°C < T_A < 105°C			600	pA
PGA Common-Mode Input Range		VSS_PGA		VDD_PGA − 4	V
PGA Gain Range	PGA_GAIN = 1, 2, 4, 8, 16, 32, 64, 128	1		128	V/V
Linear Input Range[1]	PGA_GAIN = 1				
	VDD_PGA = +20V, VSS_PGA = −16V	−16		+16	V
	VDD_PGA = +28V, VSS_PGA = 0V	0		+24	V
	VDD_PGA = +5V, VSS_PGA = −24V	−24		0	V
AAF Input	IN3_AAF+/− pins				
AAF Gain	AAF_GAIN = 0.143		1/7		V/V
AAF Differential Input Range	$\pm V_{REF}$/AAF_GAIN		±28.672		V
AAF Common-Mode Input Range		−16		+12	V
AAF Common-Mode Rejection DC	DC to 60Hz, referred to IN3_AAF input		93.0		dB
AAF Common-Mode Rejection AC	f = 10kHz, referred to IN3_AAF input		89.5		dB
AAF Input Resistance, R_{IN}	Fully-differential configuration (IN3_AAF+ = positive input, IN3_AAF− = negative input)		28		kΩ
	Single-ended to differential configuration (IN3_AAF+ = input, IN3_AAF− = AGND)		14.93		kΩ
OVERALL SYSTEM DC ACCURACY					
Gain Error[2]	All PGA_GAIN, RTI	−0.08	+0.02	+0.13	%
Gain Error Drift[2, 3]	Endpoint Method				
	PGA_GAIN = 1 to 64	−0.4	+1.5	+3.0	ppm/°C
	PGA_GAIN = 128	−0.1	+2.3	+4.7	ppm/°C
Offset Error[2]	RTI, T_A = 25°C				
	PGA_GAIN = 1		±(10+710/PGA_GAIN)	±2200	µV
	PGA_GAIN = 2, 4, 8, 16, 32, 64, 128		±(10+710/PGA_GAIN)		µV
Offset Error Drift[2, 3]	RTI, Endpoint Method				
	PGA_GAIN = 1	−49.6	0.1−(9.0/PGA_GAIN)	22.0	µV/°C
	PGA_GAIN = 2 to 128		0.1−(9.0/PGA_GAIN)		µV/°C
INL[4]	Endpoint Method				
	PGA_GAIN = 1		±2.5		ppm of linear input range
	PGA_GAIN = 16		±1.6		ppm of linear input range
	PGA_GAIN = 128		±7.4		ppm of linear input range

SPECIFICATIONS

Table 3. Specifications using AAF_GAIN = IN3_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Low-Frequency Noise	Sinc3 filter, ODR = 50SPS, BW = 15Hz, shorted input, RTI				
	PGA_GAIN = 1		2.15		µV rms
	PGA_GAIN = 2		1.11		µV rms
	PGA_GAIN = 4		0.51		µV rms
	PGA_GAIN = 8		0.25		µV rms
	PGA_GAIN = 16		0.15		µV rms
	PGA_GAIN = 32		0.08		µV rms
	PGA_GAIN = 64		0.05		µV rms
	PGA_GAIN = 128		0.04		µV rms
Peak-to-Peak Resolution[5]	Sinc3 filter, ODR = 50SPS, BW = 15Hz, shorted input, RTI				
	PGA_GAIN = 1		20.1		Bits
	PGA_GAIN = 2		20.1		Bits
	PGA_GAIN = 4		20.2		Bits
	PGA_GAIN = 8		20.2		Bits
	PGA_GAIN = 16		20.2		Bits
	PGA_GAIN = 32		19.9		Bits
	PGA_GAIN = 64		19.4		Bits
	PGA_GAIN = 128		18.8		Bits
OVERALL SYSTEM AC PERFORMANCE	Wideband low-ripple FIR filter, ODR = 256kSPS, DEC_RATE = 32, BW = 110.8kHz				
DR[6]	Shorted input				
	PGA_GAIN = 1, input range = ±16V	101.7	102.9		dB
	PGA_GAIN = 2, input range = ±8V		103.0		dB
	PGA_GAIN = 4, input range = ±4V		102.9		dB
	PGA_GAIN = 8, input range = ±2V		102.8		dB
	PGA_GAIN = 16, input range = ±1V		102.6		dB
	PGA_GAIN = 32, input range = ±0.5V		101.0		dB
	PGA_GAIN = 64, input range = ±0.25V		98.5		dB
	PGA_GAIN = 128, input range = ±0.125V		94.4		dB
	Total system DR		136.5		dB
Noise Spectral Density	RTI, shorted input, at 1kHz				
	PGA_GAIN = 1		243		nV/√Hz
	PGA_GAIN = 2		119		nV/√Hz
	PGA_GAIN = 4		61		nV/√Hz
	PGA_GAIN = 8		31		nV/√Hz
	PGA_GAIN = 16		16		nV/√Hz
	PGA_GAIN = 32		9.6		nV/√Hz
	PGA_GAIN = 64		6.3		nV/√Hz
	PGA_GAIN = 128		5.1		nV/√Hz
Total RMS Noise	RTI, shorted input				
	PGA_GAIN = 1		80.8		µV rms
	PGA_GAIN = 2		39.7		µV rms
	PGA_GAIN = 4		20.3		µV rms
	PGA_GAIN = 8		10.2		µV rms
	PGA_GAIN = 16		5.2		µV rms
	PGA_GAIN = 32		3.2		µV rms
	PGA_GAIN = 64		2.1		µV rms

SPECIFICATIONS

Table 3. Specifications using AAF_GAIN = IN3_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 128		1.7		µV rms
SNR	−5.2dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 16Vp		102.2		dB
	PGA_GAIN = 2, 8Vp		102.1		dB
	PGA_GAIN = 4, 4Vp		102.2		dB
	PGA_GAIN = 8, 2Vp		102.0		dB
	PGA_GAIN = 16, 1Vp		101.5		dB
	PGA_GAIN = 32, 0.5Vp		100.1		dB
	PGA_GAIN = 64, 0.25Vp		97.4		dB
	PGA_GAIN = 128, 0.125Vp		93.4		dB
THD	−5.2dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 16Vp		−110.1		dB
	PGA_GAIN = 2, 8Vp		−113.5		dB
	PGA_GAIN = 4, 4Vp		−112.5		dB
	PGA_GAIN = 8, 2Vp		−110.6		dB
	PGA_GAIN = 16, 1Vp		−110.2		dB
	PGA_GAIN = 32, 0.5Vp		−110.0		dB
	PGA_GAIN = 64, 0.25Vp		−109.8		dB
	PGA_GAIN = 128, 0.125Vp		−108.7		dB
SINAD	−5.2dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 16Vp		101.5		dB
	PGA_GAIN = 2, 8Vp		101.8		dB
	PGA_GAIN = 4, 4Vp		101.8		dB
	PGA_GAIN = 8, 2Vp		101.4		dB
	PGA_GAIN = 16, 1Vp		100.9		dB
	PGA_GAIN = 32, 0.5Vp		99.7		dB
	PGA_GAIN = 64, 0.25Vp		97.1		dB
	PGA_GAIN = 128, 0.125Vp		93.3		dB
SFDR	−5.2dBFS, sine input, 1kHz tone				
	PGA_GAIN = 1, 16Vp		−113.6		dBc
	PGA_GAIN = 2, 8Vp		−122.9		dBc
	PGA_GAIN = 4, 4Vp		−112.5		dBc
	PGA_GAIN = 8, 2Vp		−111.6		dBc
	PGA_GAIN = 16, 1Vp		−111.5		dBc
	PGA_GAIN = 32, 0.5Vp		−111.8		dBc
	PGA_GAIN = 64, 0.25Vp		−112.5		dBc
	PGA_GAIN = 128, 0.125Vp		−112.4		dBc
IMD	All PGA_GAIN, f_{IN_A} = 9kHz, f_{IN_B} = 10kHz				
	Second-order				
	PGA_GAIN = 1		−105		dBc
	PGA_GAIN = 2		−118		dBc
	PGA_GAIN = 4		−103		dBc
	PGA_GAIN = 8		−103		dBc
	PGA_GAIN = 16 to 128		−102		dBc
	Third-order				
	PGA_GAIN = 1		−118		dBc
	PGA_GAIN = 2		−121		dBc
	PGA_GAIN = 4		−121		dBc
	PGA_GAIN = 8		−119		dBc

SPECIFICATIONS

Table 3. Specifications using AAF_GAIN = IN3_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 16		−118		dBc
	PGA_GAIN = 32		−116		dBc
	PGA_GAIN = 64		−112		dBc
	PGA_GAIN = 128		−108		dBc
AFE MAGNITUDE AND PHASE PERFORMANCE[7]					
AFE Bandwidth	−3dB relative to signal amplitude at DC				
	PGA_GAIN = 1		278.1		kHz
	PGA_GAIN = 2		290.1		kHz
	PGA_GAIN = 4		286.4		kHz
	PGA_GAIN = 8		282.1		kHz
	PGA_GAIN = 16		273.7		kHz
	PGA_GAIN = 32		249.5		kHz
	PGA_GAIN = 64		194.1		kHz
	PGA_GAIN = 128		114.1		kHz
Analog Group Delay	f_{IN} = 20kHz				
	PGA_GAIN = 1		1.25		µs
	PGA_GAIN = 2		1.13		µs
	PGA_GAIN = 4		1.18		µs
	PGA_GAIN = 8		1.26		µs
	PGA_GAIN = 16		1.37		µs
	PGA_GAIN = 32		1.55		µs
	PGA_GAIN = 64		1.88		µs
	PGA_GAIN = 128		2.54		µs
Phase Angle Mismatch over Gain[3, 4, 7]	Sine wave, f_{IN} = 20kHz, single device, normalized to PGA_GAIN = 1, T_A = 25°C				
	PGA_GAIN = 2	−0.934	−0.861	−0.788	Degrees
	PGA_GAIN = 4	−0.589	−0.525	−0.460	Degrees
	PGA_GAIN = 8	0.002	0.060	0.119	Degrees
	PGA_GAIN = 16	0.784	0.854	0.923	Degrees
	PGA_GAIN = 32	2.042	2.160	2.278	Degrees
	PGA_GAIN = 64	4.337	4.573	4.809	Degrees
	PGA_GAIN = 128	8.809	9.273	9.738	Degrees
Phase Angle Drift[3, 4, 7]	f_{IN} = 20kHz				
	PGA_GAIN = 1	0.27	0.54	0.82	m°/°C
	PGA_GAIN = 2	0.14	0.38	0.62	m°/°C
	PGA_GAIN = 4	0.35	0.65	0.94	m°/°C
	PGA_GAIN = 8	0.80	1.16	1.52	m°/°C
	PGA_GAIN = 16	1.43	2.05	2.68	m°/°C
	PGA_GAIN = 32	2.71	3.81	4.90	m°/°C
	PGA_GAIN = 64	5.10	7.22	9.34	m°/°C
	PGA_GAIN = 128	9.83	13.78	17.73	m°/°C
Device-to-Device Phase Angle Mismatch[3, 4, 7]	f_{IN} = 20kHz, typical = ±1σ, T_A = 25°C				
	PGA_GAIN = 1	−0.058	±0.016	0.058	Degrees
	PGA_GAIN = 2	−0.091	±0.023	0.091	Degrees
	PGA_GAIN = 4	−0.084	±0.021	0.084	Degrees
	PGA_GAIN = 8	−0.081	±0.020	0.081	Degrees
	PGA_GAIN = 16	−0.087	±0.022	0.087	Degrees
	PGA_GAIN = 32	−0.131	±0.033	0.131	Degrees

SPECIFICATIONS

Table 3. Specifications using AAF_GAIN = IN3_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	PGA_GAIN = 64	−0.243	±0.061	0.243	Degrees
	PGA_GAIN = 128	−0.469	±0.117	0.469	Degrees
Device-to-Device Phase Angle Mismatch Drift[3, 4, 7]	f_{IN} = 20kHz, typical = |1σ| per °C				
	PGA_GAIN = 1		−5.9	−23.5	µ°/°C
	PGA_GAIN = 2		−7.4	−29.7	µ°/°C
	PGA_GAIN = 4		−5.1	−20.4	µ°/°C
	PGA_GAIN = 8		−8.1	−32.5	µ°/°C
	PGA_GAIN = 16		−2.4	−9.7	µ°/°C
	PGA_GAIN = 32		28.6	114.3	µ°/°C
	PGA_GAIN = 64		70.7	282.7	µ°/°C
	PGA_GAIN = 128		155.6	622.5	µ°/°C
Magnitude Flatness	f_{IN} = 20kHz				
	PGA_GAIN = 1 to 16		±0.005		dB
	PGA_GAIN = 32		−0.010		dB
	PGA_GAIN = 64		−0.030		dB
	PGA_GAIN = 128		−0.100		dB
	f_{IN} = 100kHz				
	PGA_GAIN = 1 to 16		±0.10		dB
	PGA_GAIN = 32		−0.20		dB
	PGA_GAIN = 64		−0.70		dB
	PGA_GAIN = 128		−2.10		dB
Alias Rejection	All PGA_GAIN, −20dBFS input signal at MCLK = 16.384MHz		90		dB
POWER SUPPLY CURRENT					
VDD_PGA	IN = AGND		1.4		mA
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		1.6		mA rms
	Full-scale DC input with common mode = AGND, any PGA_GAIN		3.2		mA
VSS_PGA	IN = AGND		−1.6		mA
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		−1.9		mA rms
	Full-scale DC input with common mode = AGND, any PGA_GAIN		−1.3		mA
VDD_FDA	IN3_AAF+ = IN3_AAF− = AGND		4.2		mA
	IN3_AAF+ = 12.5Vp 1kHz sine input, IN3_AAF− = AGND		4.3		mA rms
	IN3_AAF+ = 12.5VDC, IN3_AAF− = AGND		4.0		mA
	Standby		120		µA
VDD_ADC	Linearity boost buffer on, reference precharge buffer on		6.3		mA
	Linearity boost buffer off, reference precharge buffers off		2.4		mA
	Standby		205		µA
VDD2_ADC			4.7		mA
	Standby		30		µA
VDD_IO					
Sinc3 Filter			3.5		mA
Sinc5 Filter			3.7		mA

SPECIFICATIONS

Table 3. Specifications using AAF_GAIN = IN3_AAF (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Wideband Low-Ripple FIR Filter			9.1		mA
Standby			380		µA
POWER DISSIPATION	VDD_PGA = 20V, VSS_PGA = −16V, IN_LDO = EN_LDO = 5.3 V, OUT_LDO = VDD_FDA = VDD_ADC = VDD2_ADC, VDD_IO = 3.3 V, linearity boost buffer on, reference precharge buffer on, external CMOS MCLK				
Full Operating Mode					
Sinc3 Filter	IN = AGND, any PGA_GAIN		137		mW
Sinc5 Filter	IN = AGND, any PGA_GAIN		138		mW
Wideband Low-Ripple FIR Filter	IN = AGND, any PGA_GAIN		157		mW
	Full-scale 1kHz sine input with common mode = AGND, any PGA_GAIN		164		mW
	Full-scale DC input with common mode = AGND, any PGA_GAIN		177		mW
Standby Mode	FDA in standby mode, and ADC in standby mode		3.14		mW
ADC Power-Down	FDA in standby mode, and ADC in power-down mode		0.65		mW

[1] The linear input range using IN3_AAF+/− is limited by the PGA's common-mode input range, and is dependent on the PGA supply voltages. For complete list of linear input ranges across various PGA gains and AAF gains, see the Input Range Selection section.

[2] Tester repeatability and reproducibility guard band is not included.

[3] Limits calculated based on the characterization data of 50 samples from one nominal wafer from −40°C to +105°C.

[4] Specification is not production tested but is supported by characterization data at initial product release.

[5] For peak-to-peak resolution, see the Terminology section. Noise used in calculation is listed under the Low-Frequency Noise specification.

[6] For more details on dynamic range and noise across different gain and filter configurations, see the Noise Performance section.

[7] For AFE performance, terminology, and calculation, see the Calculations on AFE Phase Performance section.

SPECIFICATIONS

GENERAL SPECIFICATIONS

VDD_PGA = 15V, VSS_PGA = −15V, AGND = DGND = 0V, IN_LDO = EN_LDO = 5.1V to 5.5V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2V to 5.5V, VDD_IO = 1.7V to 3.6V, REF+ = 4.096V, REF− = 0V, MCLK = SCLK = 16.384MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband low ripple, Decimation = 32, ODR = 256kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full-power mode, T_A = −40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 4. General Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR)[1]					
	Wideband low-ripple FIR	8		256	kSPS
	Sinc5	8		1024	kSPS
	Sinc3	0.05		256	kSPS
No Missing Codes	Wideband low-ripple FIR, Decimation ratio ≥ 32	24			Bits
	Sinc5 filter, decimation ratio ≥ 32	24			Bits
	Sinc3 Filter, decimation ratio ≥ 64	24			Bits
Data Output Coding		Twos complement, MSB first			
REFERENCE INPUT CHARACTERISTICS					
REFIN Voltage	REFIN = (REF+) − (REF−)	1		VDD_ADC− AGND	V
Absolute REFIN Voltage Limit	Reference unbuffered	AGND − 0.05		VDD_ADC+ 0.05	V
	Reference buffer on	AGND		VDD_ADC	V
	Reference precharge buffer on	AGND		VDD_ADC	V
Average REFIN Current	Reference unbuffered		±80		µA/V
	Reference precharge buffer on		±20		µA
	Reference buffer on		±300		nA
Average REFIN Current Drift	Reference unbuffered		±1.7		nA/V/°C
	Reference precharge buffer on		125		nA/°C
	Reference buffer on		4		nA/°C
Common-Mode Rejection	Up to 10MHz		100		dB
DIGITAL FILTER RESPONSE					
Wideband Low-Ripple FIR Filter					
Decimation Rate	Six selectable decimation rates	32		1024	
Output Data Rate				256	kSPS
Group Delay	Latency		34/ODR		Sec
Settling Time	Complete settling		68/ODR		Sec
Pass-Band Ripple				±0.005	dB
Pass Band	−0.005dB		0.4 × ODR		Hz
	−0.1dB pass band		0.409 × ODR		
	−3dB Bandwidth		0.433 × ODR		Hz
Stop-Band Frequency	Attenuation >105dB		0.499 × ODR		Hz
Stop-Band Attenuation		105			dB
Sinc5					
Decimation Rate	Eight selectable decimation rates	8		1024	
Output Data Rate				1.024	MSPS
Group Delay	Latency		< 3/ODR		Sec
Settling time	Complete settling		< 6/ODR		Sec
Pass Band	−0.1dB bandwidth		0.0376 × ODR		Hz
	−3dB bandwidth		0.204 × ODR		Hz

SPECIFICATIONS

Table 4. General Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Sinc3 Filter					
Decimation Rate	1024 decimation rates	32		185,280	
Output Data Rate				256	kSPS
Group Delay	Latency		2/ODR		Sec
Settling Time	Complete settling to reject 50Hz		60		ms
Pass Band	−0.1dB bandwidth		0.0483 × ODR		Hz
	−3dB bandwidth		0.2617 × ODR		Hz
CLOCK					
External Clock MCLK		0.6	16.384	17	MHz
Internal Clock MCLK			16.384		MHz
Input High Voltage	See the logic input parameter				
Duty Cycle	16.384MHz MCLK	25:75	50:50	25:75	%
MCLK Logic Low-Pulse Width		16			ns
MCLK Logic High-Pulse Width		16			ns
Crystal Frequency		8	16	17	MHz
Crystal Start-Up Time	Clock output valid		2		ms
ADC RESET					
ADC Start-Up Time after Reset	Reset rising edge to first $\overline{\text{DRDY}}$, $\overline{\text{PIN}}$ mode, Decimate by 8		100		µs
Minimum $\overline{\text{RESET}}$ Low-Pulse Width		0.0001		100	ms
LOGIC INPUTS	Applies to all logic inputs unless specified otherwise, voltage referenced to AGND				
Input High Voltage, V_{INH}	1.7V ≤ VDD_IO ≤ 1.9V	0.65 × VDD_IO			V
	2.22V ≤ VDD_IO ≤ 3.6V	0.65 × VDD_IO			V
Input Low Voltage, V_{INL}	1.7V ≤ VDD_IO ≤ 1.9V			0.35 × VDD_IO	V
	2.22V ≤ VDD_IO ≤ 3.6V			0.7	V
Hysteresis	2.22V ≤ VDD_IO ≤ 3.6V	0.08		0.25	V
	1.7V ≤ VDD_IO ≤ 1.9V	0.04		0.2	V
Leakage Current	Excluding $\overline{\text{RESET}}$ pin	−10	0.05	+10	µA
	$\overline{\text{RESET}}$ pin pull-up resistor		1		kΩ
GAIN0, GAIN1, GAIN2, EN_PGA	Voltage referenced to AGND				
Input High Voltage		2			V
Input Low Voltage				0.8	V
Input Current	GAIN0/GAIN1/GAIN2/EN_PGA = VDD_PGA or AGND		2	±100	nA
M0_FDA, M1_FDA	Voltage referenced to AGND				
Input High Voltage		1.4			V
Input Low Voltage				1	V
Input Current	M0_FDA or M1_FDA = 0V to 5V		−10		nA
EN_LDO	Voltage referenced to AGND				
Input High Voltage	5.1V ≤ IN_LDO ≤ 5.5V	1.2			V
Input Low Voltage	5.1V ≤ IN_LDO ≤ 5.5V			0.4	V
Input Current	EN_LDO = IN_LDO or AGND		0.1		µA
LOGIC OUTPUTS					
Output High Voltage	2.2V ≤ VDD_IO < 3.6V, I_{SOURCE} = 500µA, LV_BOOST_off	0.8 × VDD_IO			V
	1.7V ≤ VDD_IO ≤ 1.9V, I_{SOURCE} = 200µA, LV_BOOST_on	0.8 × VDD_IO			V

SPECIFICATIONS

Table 4. General Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Low Voltage	2.2V ≤ VDD_IO < 3.6V, I_{SINK} = 1mA, LV_BOOST_off			0.4	V
	1.7V ≤ VDD_IO ≤ 1.9V, I_{SINK} = 400µA, LV_BOOST_on			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
LDO CHARACTERISTIC					
Input Voltage Range		5.1		5.5	V
IN_LDO Supply Current	OUT_LDO load current = 20mA		80		µA
OUT_LDO Voltage		4.80	4.90	5.03	V
Load Regulation	I_{OUT} = 1mA to 20mA		0.0005		%/mA
Dropout Voltage[2]	I_{OUT} = 20mA		3		mV
Start-Up Time[3]			350		µs
Current Limit Threshold			500		mA
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C
POWER REQUIREMENTS					
VDD_PGA		5		30	V
VSS_PGA		−25		0	V
VDD_PGA − VSS_PGA		5		30	V
VDD_FDA	Referenced to AGND	4.75	5	5.5	V
VDD_ADC	Referenced to AGND	4.75	5	5.5	V
VDD2_ADC	Referenced to AGND	2	2.5	5.5	V
VDD_IO	Referenced to AGND	1.7	1.8	3.6	V
POWER SUPPLY REJECTION	Referred to input (RTI), DC to 100Hz				
VDD_PGA	PGA_GAIN = 1		113		dB
	PGA_GAIN = 128		116		dB
VSS_PGA	PGA_GAIN = 1		130		dB
	PGA_GAIN = 128		117		dB
VDD_FDA	V_{STEP} = 0.2Vp-p		105		dB
VDD_ADC	V_{STEP} = 0.2Vp-p		85		dB
VDD2_ADC	V_{STEP} = 0.2Vp-p		105		dB
VDD_IO	V_{STEP} = 0.2Vp-p		100		dB
LDO	V_{STEP} = 0.2Vp-p		124		dB

[1] ODR ranges refer to the programmable decimation rates available on the ADAQ7769-1 for a fixed MCLK of 16.384MHz across varying MCLK_DIV and decimation rates. For suggestion on the ODR speed to achieve optimum performance, see the ADC Speed and Performance section.

[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This voltage applies only for output voltages greater than 2.3V.

[3] Start-up time is defined as the time between the rising edge of EN_LDO to output voltage (OUT_LDO) being at 90% of its nominal value.

SPECIFICATIONS

TIMING SPECIFICATIONS

VDD_ADC = 4.5V to 5.5V, VDD2_ADC = 2.0V to 5.5V, VDD_IO = 2.2V to 3.6V, AGND = DGND = 0V, Input Logic 0 = 0V, Input Logic 1 = VDD_IO, and load capacitance (C_{LOAD}) = 20pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register, Register 0x14) disabled, unless otherwise noted.

These specifications are sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of VDD_IO and timed from a voltage level of VDD_IO/2). For the timing diagrams, see Figure 2 to Figure 8.

These specifications are not production tested, but are supported by characterization data at initial product release.

Table 5. Timing Specifications

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Controller clock frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	MCLK_DIV[1:0] = 11		MCLK/2		Hz
		MCLK_DIV[1:0] = 10		MCLK/4		Hz
		MCLK_DIV[1:0] = 01		MCLK/8		Hz
		MCLK_DIV[1:0] = 00		MCLK/16		Hz
$t_{\overline{DRDY}}$	Conversion period	Rising $\overline{DRDY}$ edge to next rising $\overline{DRDY}$ edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz
$t_{\overline{DRDY}\_HIGH}$	$\overline{DRDY}$ high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
$t_{MCLK\_\overline{DRDY}}$	MCLK to $\overline{DRDY}$	Rising MCLK edge to $\overline{DRDY}$ rising edge	10	13	18	ns
$t_{MCLK\_\overline{RDY}}$	MCLK to $\overline{RDY}$ indicator on the DOUT/$\overline{RDY}$ pin	Rising MCLK edge to $\overline{RDY}$ falling edge	10	13	18	ns
t_{UPDATE}	ADC data update	Time prior to $\overline{DRDY}$ rising edge where the ADC conversion register updates, single conversion read		1 × t_{MCLK}		ns
$t_{\overline{START}}$	$\overline{START}$ pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to $\overline{SYNC\_OUT}$	Falling MCLK to falling $\overline{SYNC\_OUT}$			t_{MCLK} + 16	ns
t_{SCLK}	SCLK period		50			ns
t_1	$\overline{CS}$ falling to SCLK falling		0			ns
t_2	$\overline{CS}$ falling to data output enable				6	ns
t_3	SCLK falling edge to data output valid			10	15	ns
t_4	Data output hold time after SCLK falling edge		4			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	$\overline{CS}$ high time	4-wire interface	10			ns
t_8	SCLK high time		20			ns
t_9	SCLK low time		20			ns
t_{10}	SCLK rising edge to $\overline{DRDY}$ high	Single conversion read only, time from last SCLK rising edge to $\overline{DRDY}$ high	1 × t_{MCLK}			ns
t_{11}	SCLK rising edge to $\overline{CS}$ rising edge		6			ns
t_{12}	$\overline{CS}$ rising edge to DOUT/$\overline{RDY}$ output disable		4		7	ns
t_{13}	DOUT/$\overline{RDY}$ indicator pulse width	In continuous read mode with $\overline{RDY}$ on, DOUT enabled, with SCLK idling high		1 × t_{MCLK}		ns
t_{14}	$\overline{CS}$ falling edge to SCLK rising edge		2			ns
t_{15}	$\overline{SYNC\_IN}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{SYNC\_IN}$ pulse width		1.5 × t_{MCLK}			ns

SPECIFICATIONS

Table 5. Timing Specifications (Continued)

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{17}	SCLK rising edge to $\overline{RDY}$ indicator rising edge	In continuous read mode with $\overline{RDY}$ enabled on DOUT	1			ns
t_{18}	$\overline{DRDY}$ rising edge to SCLK falling edge	In continuous read mode with $\overline{RDY}$ enabled on DOUT	8			ns

1.8V TIMING SPECIFICATIONS

VDD_ADC = 4.5V to 5.5V, VDD2_ADC = 2V to 5.5V, VDD_IO = 1.7V to 1.9V, AGND = DGND = AGND2_ADC = 0V, Input Logic 0 = 0V, Input Logic 1 = VDD_IO, and C_{LOAD} = 20pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register, Register 0x14) enabled, unless otherwise noted.

These specifications are sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of VDD_IO and timed from a voltage level of VDD_IO/2. For the timing diagrams, see Figure 2 to Figure 8.

These specifications are not production tested but are supported by characterization data at initial product release.

Table 6. 1.8V Timing Specifications

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	MCLK_DIV[1:0] = 11		MCLK/2		Hz
		MCLK_DIV[1:0] = 10		MCLK/4		Hz
		MCLK_DIV[1:0] = 01		MCLK/8		Hz
		MCLK_DIV[1:0] = 00		MCLK/16		Hz
t$\overline{DRDY}$	Conversion period	Rising $\overline{DRDY}$ edge to next rising $\overline{DRDY}$ edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz
t$\overline{DRDY}_{HIGH}$	$\overline{DRDY}$ high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
$t_{MCLK\_\overline{DRDY}}$	MCLK to $\overline{DRDY}$	Rising MCLK edge to $\overline{DRDY}$ rising edge	13	19	25	ns
$t_{MCLK\_\overline{RDY}}$	MCLK to $\overline{RDY}$ indicator on the DOUT/$\overline{RDY}$ pin	Rising MCLK edge to $\overline{RDY}$ falling edge	13	19	25	ns
t_{UPDATE}	ADC data update	Time prior to $\overline{DRDY}$ rising edge where the ADC conversion register updates		1 × t_{MCLK}		ns
t$\overline{START}$	$\overline{START}$ pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to $\overline{SYNC\_OUT}$	Falling MCLK to falling $\overline{SYNC\_OUT}$, see the Synchronization of Multiple ADAQ7769-1 Devices sections			t_{MCLK} + 31	ns
t_{SCLK}	SCLK period		50			ns
t_1	$\overline{CS}$ falling to SCLK falling		0			ns
t_2	$\overline{CS}$ falling to data output enable				11	ns
t_3	SCLK falling edge to data output valid			14	19	ns
t_4	Data output hold time after SCLK falling edge		7			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	$\overline{CS}$ high time	4-wire interface	10			ns
t_8	SCLK high time		23			ns
t_9	SCLK low time		23			ns
t_{10}	SCLK rising edge to $\overline{DRDY}$ high	Time from last SCLK rising edge to DRDY high, if this is exceeded, conversion N + 1 is missed, single conversion read	1 × t_{MCLK}			ns
t_{11}	SCLK rising edge to $\overline{CS}$ rising edge		6			ns

SPECIFICATIONS

Table 6. 1.8V Timing Specifications (Continued)

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{12}	$\overline{CS}$ rising edge to DOUT/$\overline{RDY}$ output disable		7.5		13	ns
t_{13}	DOUT/$\overline{RDY}$ indicator pulse width	In continuous read mode with $\overline{RDY}$ on, DOUT enabled, with SCLK idling high		1 × t_{MCLK}		ns
t_{14}	$\overline{CS}$ falling edge to SCLK rising edge		2.5			ns
t_{15}	$\overline{SYNC\_IN}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{SYNC\_IN}$ pulse width		1.5 × t_{MCLK}			ns
t_{17}	SCLK rising edge to $\overline{RDY}$ indicator rising edge	In continuous read mode with $\overline{RDY}$ on, DOUT enabled	5.5			ns
t_{18}	$\overline{DRDY}$ rising edge to SCLK falling edge	In continuous read mode with $\overline{RDY}$ on, DOUT enabled	15			ns

Timing Diagrams

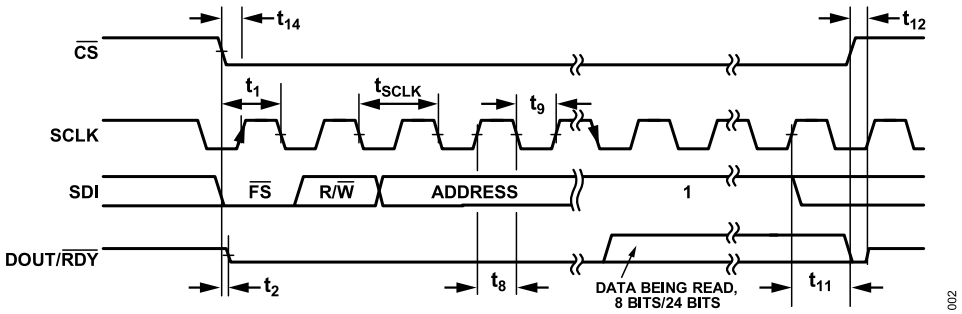

Figure 2. SPI Read Timing Diagram

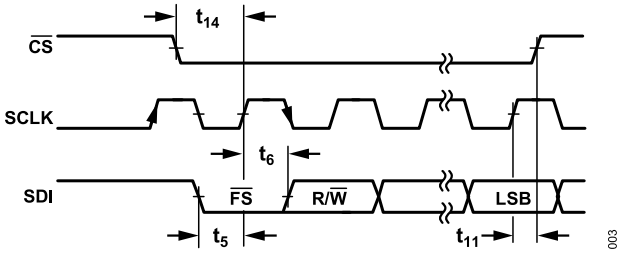

Figure 3. SPI Write Timing Diagram

SPECIFICATIONS

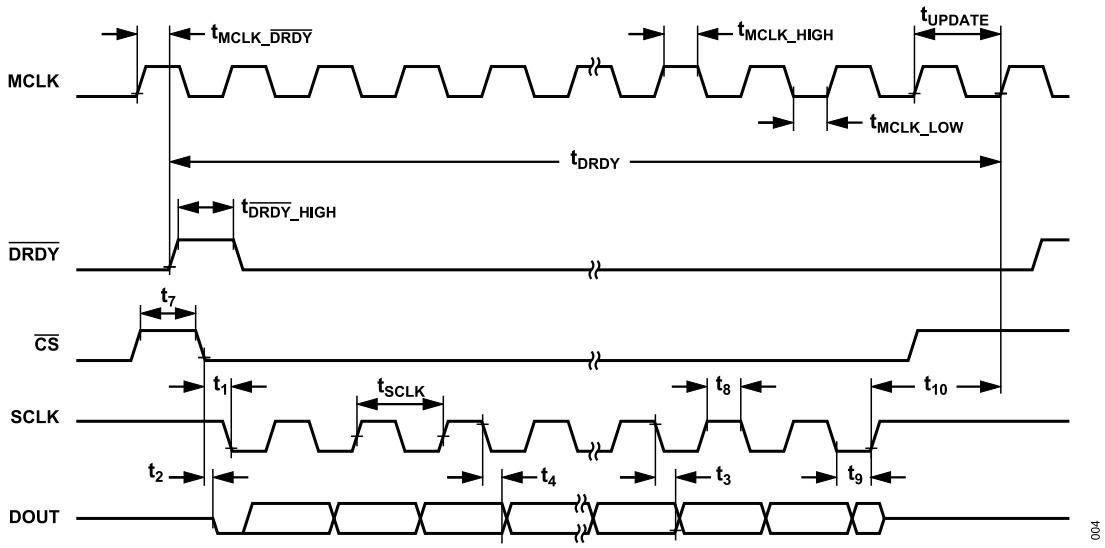

Figure 4. Reading Conversion Result in Continuous Conversion Mode ($\overline{CS}$ Toggling)

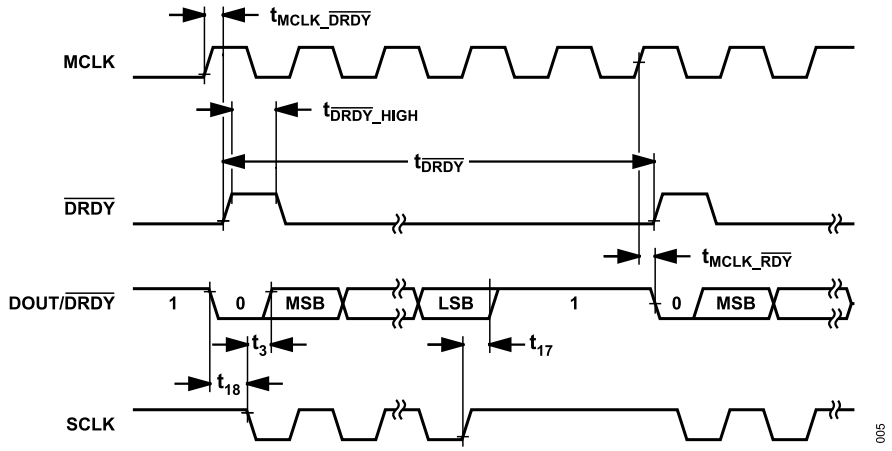

Figure 5. Reading Conversion Result in Continuous Conversion Mode, Continuous Read Mode with $\overline{RDY}$ Enabled ($\overline{CS}$ Held Low)

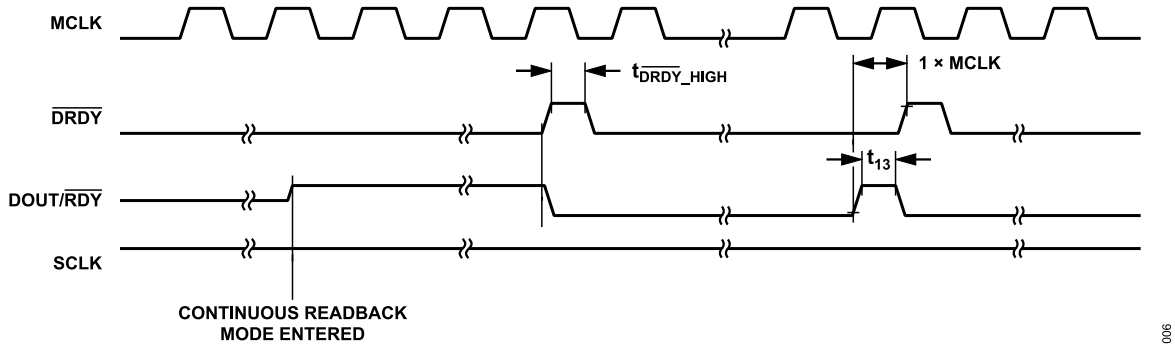

Figure 6. DOUT/$\overline{RDY}$ Behavior without SCLK Applied

SPECIFICATIONS

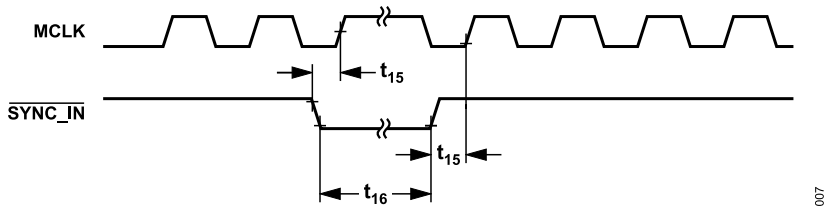

Figure 7. Synchronous $\overline{\text{SYNC\_IN}}$ Pulse

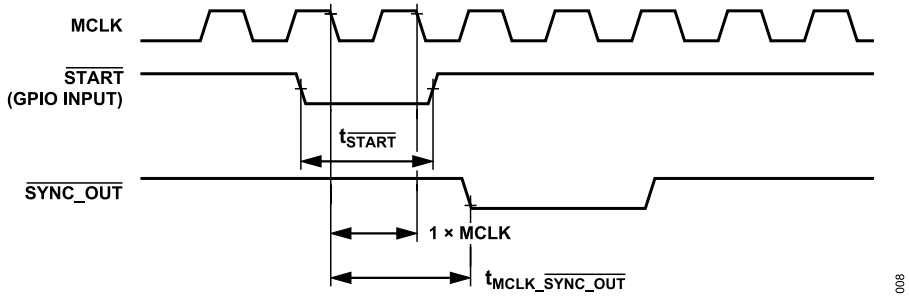

Figure 8. Asynchronous $\overline{\text{START}}$ and $\overline{\text{SYNC\_OUT}}$

ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute Maximum Ratings

Parameter	Rating
VDD_PGA to AGND	36V
VSS_PGA to AGND	−36V
VDD_PGA to VSS_PGA	36V
IN to AGND	VDD_PGA to VSS_PGA
IN Input Current[1]	±10mA
GAIN0, GAIN1, GAIN2, EN_PGA	VSS_PGA − 0.3V to VDD_PGA + 0.3V or 30mA, whichever occurs first
IN1_AAF+, IN1_AAF− to AGND	±15V
IN2_AAF+, IN2_AAF− to AGND	±15V
IN3_AAF+, IN3_AAF− to AGND	±36V
VDD_FDA to VDD_ADC	−0.3V to +0.3V
VDD_FDA to AGND	−0.3V to +6.5V
M0_FDA and M1_FDA to AGND	−0.3V to VDD_FDA +0.3V
IN_LDO to AGND	−0.3V to +6.5V
EN_LDO to AGND	−0.3V to +6.5V
OUT_LDO to AGND	−0.3V to IN_LDO
VDD_ADC to AGND	−0.3V to +6.5V
VDD2_ADC to AGND	−0.3V to +6.5V
VDD_IO to DGND	−0.3V to +6.5V
DGND to AGND	−0.3V to +0.3V
VDDIO, DREG_CAP to DGND (VDD_IO connected to DREG_CAP for 1.8V Operation)	−0.3V to +2.25V
REF+, REF− to AGND	−0.3V to VDD_ADC + 0.3V
Digital Input Voltage to DGND	−0.3V to VDD_IO + 0.3V
Digital Output Voltage to DGND	−0.3V to VDD_IO + 0.3V
XTAL1 to DGND	−0.3V to +2.1V
Temperature	
Operating Range	−40°C to +105°C
Storage Range	−65°C to +150°C
Pb-Free, Soldering Reflow (10sec to 30sec)	260°C
Maximum Package Classification	260°C

[1] The IN pin has clamp diodes connected to the VDD_PGA and VSS_PGA supply pins. Limit the input current to 10mA or less when input signals exceed the power supply rails by 0.3V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC_TOP} is the top junction-to-case thermal resistance and θ_{JC_BOTTOM} is the bottom junction-to-case thermal resistance. θ_{JB} is the junction-to-board thermal resistance. Ψ_{JT} is the junction-to-top thermal characterization and Ψ_{JB} is the junction-to-board thermal characterization.

Thermal resistance values shown in Table 8 are simulated based on JEDEC specs (unless specified otherwise) and must be used in compliance with JESD51-12.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOTTOM}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-84-4	31.0	20.5	20.0	24.1	8.4	24.2	(°C/W)

[1] Test Condition 1: Thermal impedance simulated values are based on use of a 2S2P with vias JEDEC PCB excluding the θ_{JC_TOP}, which uses 1S0P JEDEC PCB.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAQ7769-1

Table 9. ADAQ7769-1, 84-Ball CSP_BGA

ESD Model	Withstand Voltage (V)	Class
HBM	±2000	2
FICDM	±500	C2A

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

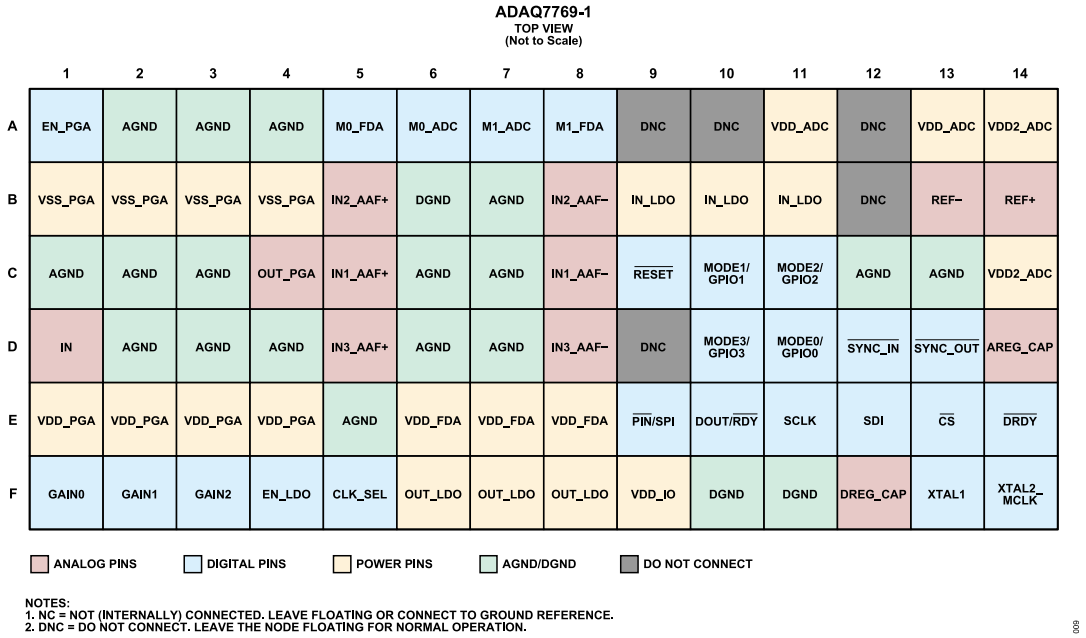

Figure 9. Pin Configuration

Table 10. ADAQ7769-1 Pin Function Descriptions

Pin Number	Mnemonic	Type[1]	Description
A1	EN_PGA	DI	Active High Digital Input. When low, the PGA is disabled, and all switches are off. When high, the GAINx logic inputs determine the PGA gain.
A2 to A4, B7, C1 to C3, C6, C7, C12, C13, D2 to D4, D6, D7, E5	AGND	P	Ground reference for VDD_FDA, IN_LDO, VDD_ADC, and VDD2_ADC supplies. Connect to system ground for normal operation.
A5	M0_FDA	DI	FDA Mode Control Input 0. Connect to M0_ADC for normal operation.
A6	M0_ADC	DO	FDA Mode Control Output 0. Connect to M0_FDA for normal operation.
A7	M1_ADC	DO	FDA Mode Control Output 1. Connect to M1_FDA for normal operation.
A8	M1_FDA	DI	FDA Mode Control Input 1. Connect to M1_ADC for normal operation.
A9, A10, A12, B12, D9	DNC	N/A[2]	Do not connect. Leave the node floating for normal operation.
A11, A13	VDD_ADC	P	ADC Analog Supply Voltage. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_FDA pin.
A14, C14	VDD2_ADC	P	ADC Secondary Analog Supply Voltage. Referenced to AGND.
B1 to B4	VSS_PGA	P	PGA Negative Supply. Referenced to AGND.
B5	IN2_AAF+	AI	AAF Signal Input, Noninverting, Gain of 0.364. Maximum differential input of 22Vpp.
B6, F10, F11	DGND	P	Ground reference for VDD_IO supplies. Connect to system ground for normal operation.
B8	IN2_AAF−	AI	AAF Signal Input, Inverting, Gain of 0.364. Maximum differential input of 22Vpp.
B9 to B11	IN_LDO	P	On-Device LDO Supply Input. Bypass IN_LDO to AGND with a capacitor of at least 1µF.
B13	REF−	AI	ADC Reference Input Negative Node. Connect to AGND for normal operation.
B14	REF+	AI	ADC Reference Input Positive Node. Apply an external reference between REF+ and REF− with voltage level ranging from VDD_ADC to AGND +1V.
C4	OUT_PGA	AO	PGA Signal Output. Connect to either IN1_AAF+, IN2_AAF+, or IN3_AAF+, while connecting corresponding negative AAF input to AGND, according to required AAF gain.
C5	IN1_AAF+	AI	AAF Signal Input, Noninverting, Gain of 1. Maximum differential input of 8Vpp.
C8	IN1_AAF−	AI	AAF Signal Input, Inverting, Gain of 1. Maximum differential input of 8Vpp.
C9	$\overline{\text{RESET}}$	DI	ADC Hardware Asynchronous Reset Input. After the device is fully powered up, it is recommended to do a hardware or software reset.
C10	MODE1/GPIO1	DI/O	In $\overline{\text{PIN}}$ control mode, MODE2 is the $\overline{\text{PIN}}$ control operating profile selection input 2.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 10. ADAQ7769-1 Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Type[1]	Description
			In $\overline{\text{PIN}}$ control mode, MODE1 is the $\overline{\text{PIN}}$ control operating profile selection input 1.
			In SPI control mode, GPIO1 is the general-purpose input and output pin with the logic level referenced to the VDD_IO and DGND pins.
C11	MODE2/GPIO2	DI/O	A Multifunction Pin.
			In $\overline{\text{PIN}}$ control mode, MODE2 is the $\overline{\text{PIN}}$ control operating profile selection input 2.
			In SPI control mode, GPIO2 is the general-purpose input and output pin with its logic level referenced to the VDD_IO and DGND pins.
D1	IN	AI	System/PGA Signal Input.
D5	IN3_AAF+	AI	AAF Signal Input, Noninverting, Gain of 0.143. Maximum differential input of 57Vpp.
D8	IN3_AAF−	AI	AAF Signal Input, Inverting, Gain of 0.143. Maximum differential input of 57Vpp.
D10	MODE3/GPIO3	DI/O	A Multifunction Pin.
			In $\overline{\text{PIN}}$ control mode, MODE3 is the $\overline{\text{PIN}}$ control operating profile selection input 3.
			In SPI control mode, GPIO3 is the general-purpose input and output pin with the logic level referenced to the VDD_IO and DGND pins. The pin can also be assigned a $\overline{\text{START}}$ function through the EN_GPIO_$\overline{\text{START}}$ bit.
D11	MODE0/GPIO0	DI/O	A Multifunction Pin.
			In $\overline{\text{PIN}}$ control mode, MODE0 is the $\overline{\text{PIN}}$ control operating profile selection input 0.
			In SPI control mode, GPIO0 is the general-purpose input and output pin with the logic level referenced to the VDD_IO and DGND pins.
D12	$\overline{\text{SYNC\_IN}}$	DI	$\overline{\text{SYNC\_IN}}$ receives the synchronization signal from $\overline{\text{SYNC\_OUT}}$ pin or from the main controller. The synchronization signal needs to be synchronous to MCLK. $\overline{\text{SYNC\_IN}}$ enables synchronization and simultaneous sampling of multiple ADAQ7769-1 devices.
D13	$\overline{\text{SYNC\_OUT}}$	DO	Synchronization Pulse Output Synchronous to MCLK. This pin allows one or multiple ADAQ7769-1 devices to be synchronized through SPI. Send a SYNC command over SPI interface to initiate a $\overline{\text{SYNC\_OUT}}$ output. If used, route $\overline{\text{SYNC\_OUT}}$ signal back to the $\overline{\text{SYNC\_IN}}$ pin of the same device and the $\overline{\text{SYNC\_IN}}$ pins of other ADAQ7769-1 devices for simultaneous sampling.
D14	AREG_CAP	AO	ADC's Internal Analog LDO Regulator Output. Decouple this pin to AGND with a 1µF capacitor. Do not use the voltage output from AREG_CAP in circuits external to the ADAQ7769-1.
E1	VDD_PGA	P	PGA Input and Output Stage Positive Supply. Referenced to AGND.
E2 to E4	VDD_PGA	P	PGA Positive Supply. Referenced to AGND.
E6 to E8	VDD_FDA	P	ADC Driver Amplifier Positive Supply. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_ADC pin.
E9	$\overline{\text{PIN}}$/SPI	DI	Device Mode Selection Input.
			0: Pin Mode Operation. Control and configure device operation through configuration pin logic.
			1: Control and configuration through register over SPI.
E10	DOUT/$\overline{\text{RDY}}$	DO	Serial Interface Data Output and Data Ready Signal Combined. This output data pin can be configured as either a DOUT pin only, or through the SPI control mode, include the ready signal ($\overline{\text{RDY}}$). The ability to program the device to provide a combined DOUT/$\overline{\text{RDY}}$ signal can reduce the number of required interface IO lines.
E11	SCLK	DI	Serial Interface Clock.
E12	SDI	DI	Serial Interface Data Input.
E13	$\overline{\text{CS}}$	DI	Serial Interface Chip-Select Input. Active low.
E14	$\overline{\text{DRDY}}$	DO	ADC Conversion Data Ready Output. Periodic signal output to signify conversion results are available.
F1	GAIN0	DI	PGA Gain Control Logic Input 0.
F2	GAIN1	DI	PGA Gain Control Logic Input 1.
F3	GAIN2	DI	PGA Gain Control Logic Input 2.
F4	EN_LDO	DI	On-Device LDO Enable Input. Active high.
F5	CLK_SEL	DI	ADC Clock Source Selection Input.
			In $\overline{\text{PIN}}$ control mode, 0 = CMOS clock option. Apply external CMOS clock signal to XTAL2_MCLK pin, connect XTAL1 pin to DGND, and 1 = crystal option. Connect external crystal across the XTAL1 and XTAL2_MCLK pins.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 10. ADAQ7769-1 Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Type[1]	Description
			In SPI control mode, connect CLK_SEL pin to DGND. Select the clock source through register access. The LVDS clock option is available only in SPI control mode.
F6 to F8	OUT_LDO	P	On-Device LDO Output. Bypass OUT_LDO to AGND with a capacitor of at least 1µF.
F9	VDD_IO	P	Digital Supply. The VDD_IO pin sets the logic levels for all interface pins. VDD_IO powers the digital processing through the internal digital LDO regulator. Referenced to DGND. Bypass VDD_IO to DGND with a capacitor of at least 1µF. For VDD_IO ≤ 1.8V, connect VDD_IO to DREG_CAP, decouple it with a 10µF capacitor and enable LV_BOOST (Bit 7 of Register 0x14) from the interface format control register (see the Interface Format Control Register section).
F12	DREG_CAP	AO	Internal Digital LDO Regulator Output for the ADC. Decouple DREG_CAP to DGND with a 1µF capacitor. For VDD_IO ≤ 1.8V, connect VDD_IO to DREG_CAP, decouple it with a 10µF capacitor and enable LV_BOOST (Bit 7 of Register 0x14) from the interface format control register (see the Interface Format Control Register section). Do not use the voltage output from DREG_CAP in circuits external to the ADAQ7769-1.
F13	XTAL1	DI	ADC Clock Input 1. External Crystal: Connect to one node of the external crystal. LVDS: Connect to one node of the LVDS clock source. CMOS Clock: Connect to DGND.
F14	XTAL2_MCLK	DI	ADC Clock Input 2. External Crystal: Connect to the second node of the external crystal. LVDS: Connect to the second node of the LVDS clock source. CMOS Clock: Connect to the CMOS clock source. Logic level referenced to VDD_IO and DGND.

[1] AI is analog input, AO is analog output, DI is digital input, DO is digital output, DI/O is bidirectional digital, and P is power or ground.

[2] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

AAF_GAIN = IN1_AAF

VDD_PGA = 15V, VSS_PGA = −15V, AGND = DGND = 0V, IN_LDO = EN_LDO = 5.1V to 5.5 V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2V to 5.5V, VDD_IO = 1.7V to 3.6V, REF+ = 4.096V, REF− = 0V, MCLK = SCLK = 16.384MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband low ripple, Decimation = 32, ODR = 256kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full-power mode, T_A = −40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

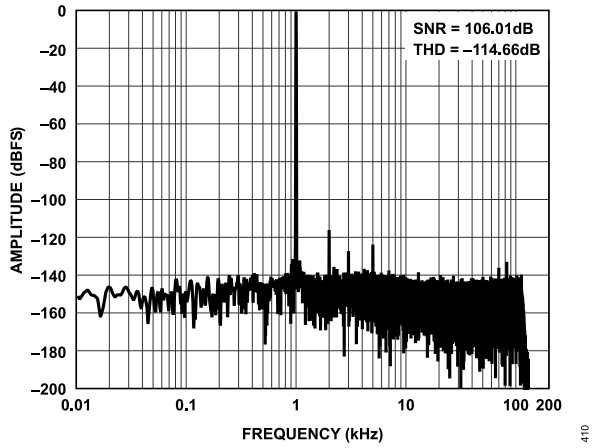

Figure 10. Wideband Low-Ripple FIR Filter, PGA_GAIN = 1V/V, IN1_AAF, Bipolar Single-Ended Input, −0.5dBFS (3.9Vp)

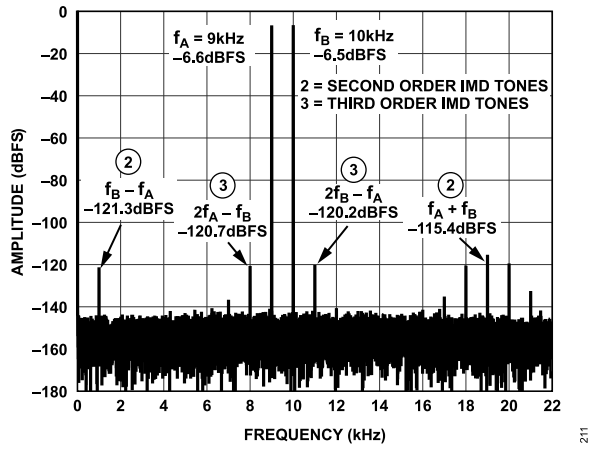

Figure 11. Two-Tone Input, PGA_GAIN = 1V/V, IN1_AAF, f_A = 9kHz and −6.6dBFS, and f_B = 10kHz and −6.5dBFS Sine, Wideband Low-Ripple Filter, ODR = 256kSPS

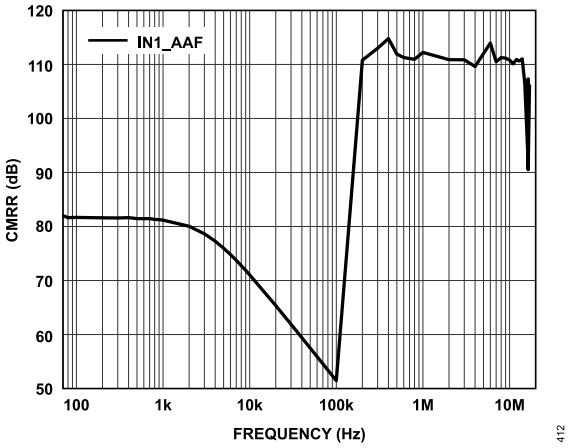

Figure 12. AC CMRR vs. Input Frequency, IN1_AAF

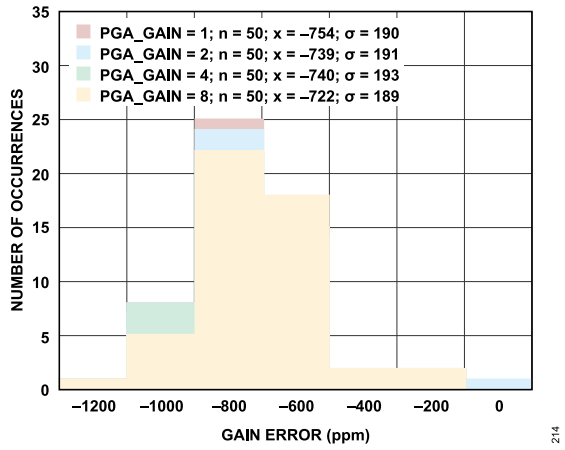

Figure 13. Gain Error Distribution, PGA_GAIN = 1 to PGA_GAIN = 8, IN1_AAF

TYPICAL PERFORMANCE CHARACTERISTICS

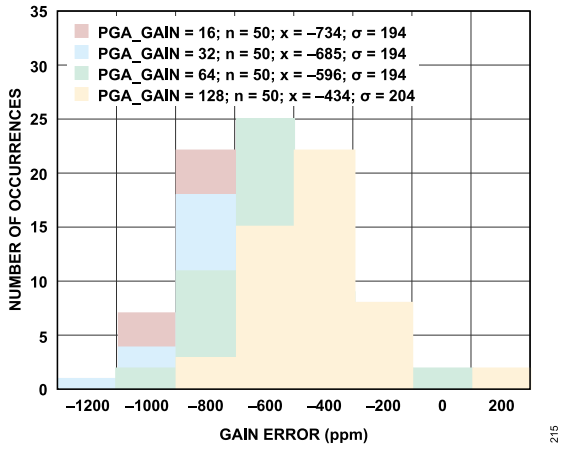

Figure 14. Gain Error Distribution, PGA_GAIN = 16 to PGA_GAIN = 128, IN1_AAF

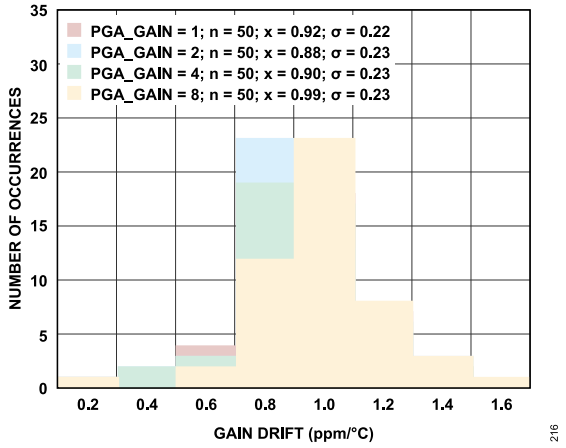

Figure 15. Gain Error Drift Distribution, PGA_GAIN = 1 to PGA_GAIN = 8, IN1_AAF

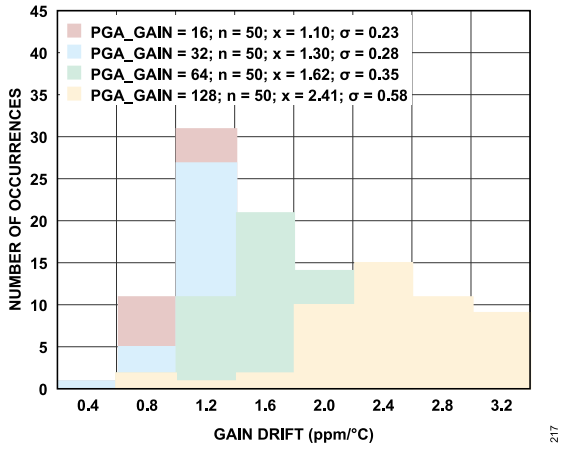

Figure 16. Gain Error Drift Distribution, PGA_GAIN = 16 to PGA_GAIN = 128, IN1_AAF

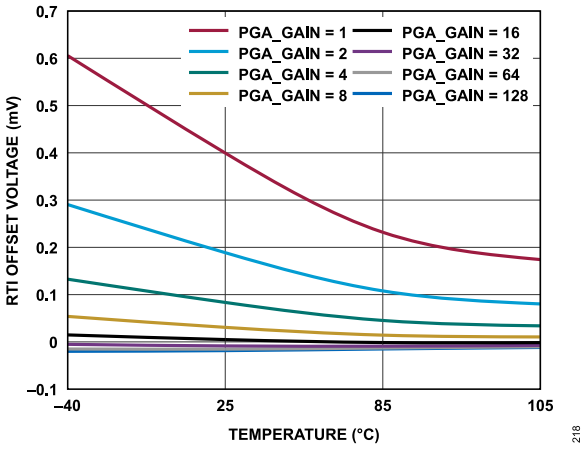

Figure 17. Offset Error vs. Temperature, IN1_AAF

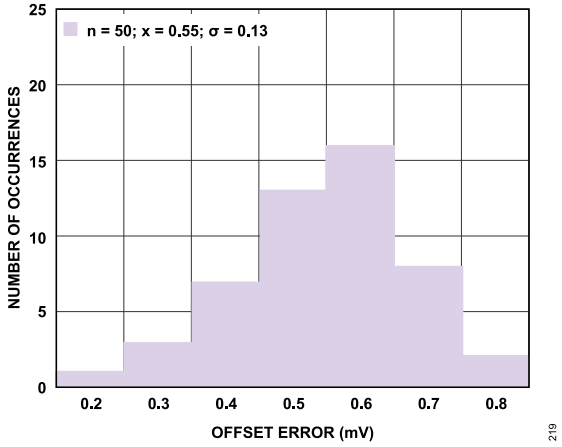

Figure 18. Offset Error Distribution, PGA_GAIN = 1V/V, IN1_AAF

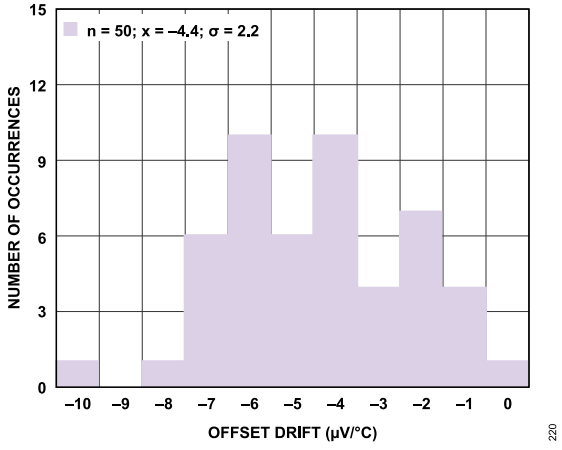

Figure 19. Offset Error Drift Distribution, PGA_GAIN = 1V/V, IN1_AAF

TYPICAL PERFORMANCE CHARACTERISTICS

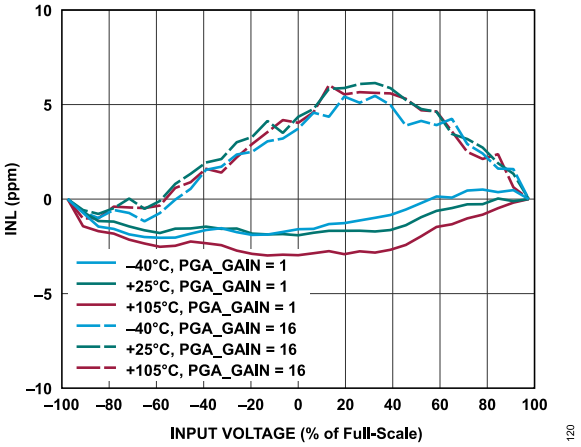

Figure 20. INL Error vs. Input Voltage over Temperature, PGA_GAIN = 1V/V and PGA_GAIN = 16V/V, IN1_AAF

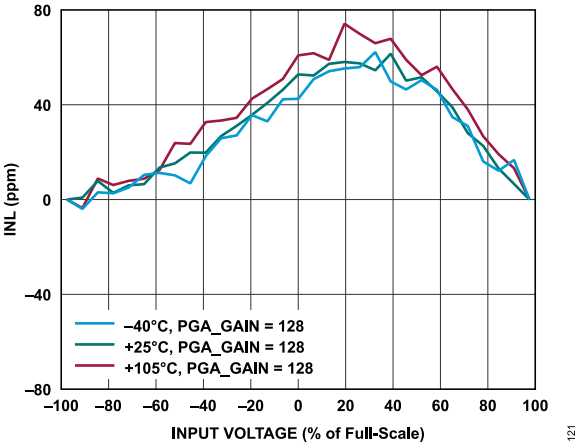

Figure 21. INL Error vs. Input Voltage over Temperature, PGA_GAIN = 128V/V, IN1_AAF

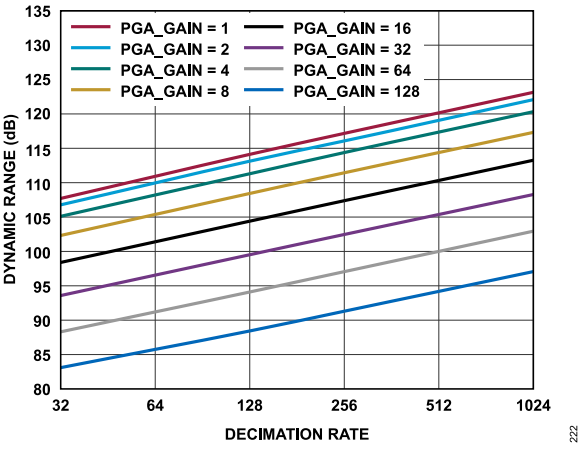

Figure 22. Dynamic Range vs. Decimation Rate, Various PGA_GAIN, IN1_AAF, Wideband Low-Ripple Filter, Shorted Input

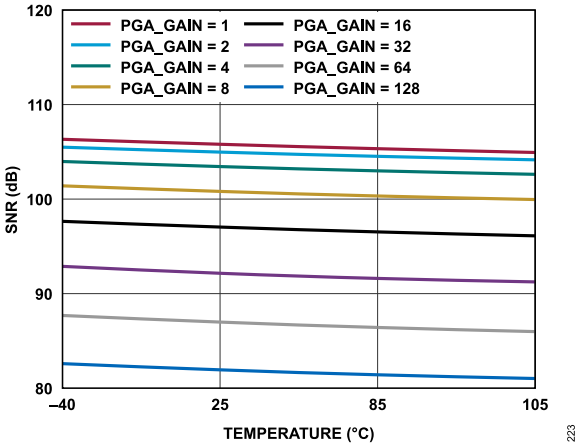

Figure 23. SNR vs. Temperature, Various PGA_GAIN, IN1_AAF, Wideband Low-Ripple Filter, −0.5dBFS (3.9Vp), 1kHz

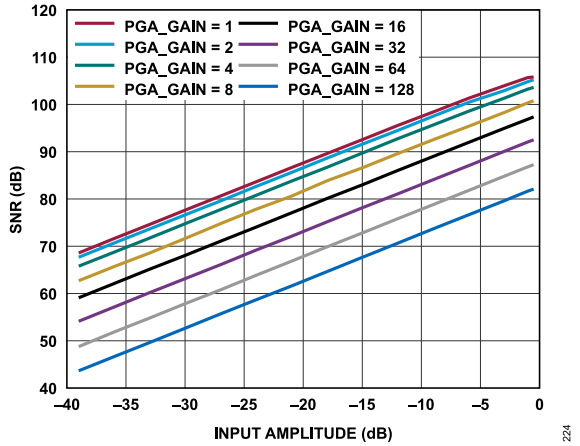

Figure 24. SNR vs. Input Amplitude, Various PGA_GAIN, IN1_AAF, Wideband Low-Ripple Filter, 1kHz

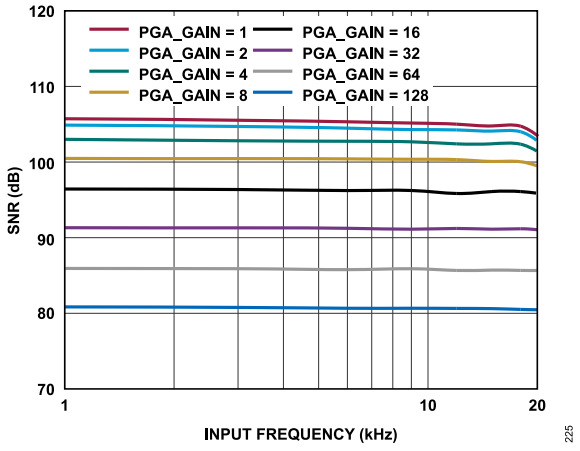

Figure 25. SNR vs. Input Frequency, Various PGA_GAIN, IN1_AAF, −0.5dBFS, FDA = Full Power

TYPICAL PERFORMANCE CHARACTERISTICS

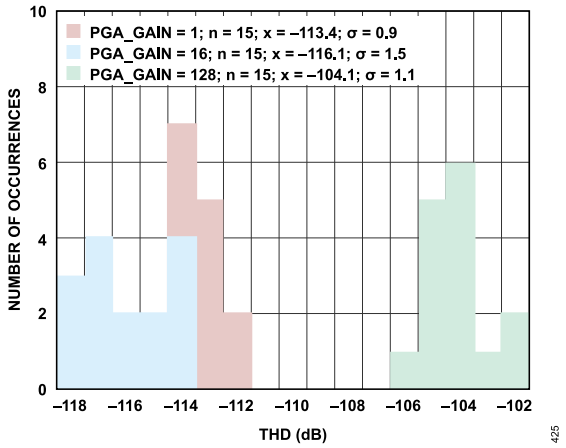

Figure 26. THD Distribution, Various PGA_GAIN, IN1_AAF, −0.5dBFS, 1kHz

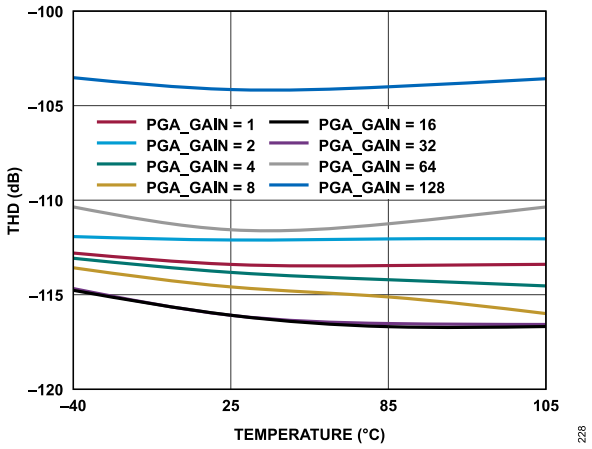

Figure 27. THD vs. Temperature, Various PGA_GAIN, IN1_AAF, −0.5dBFS (3.9Vp), 1kHz

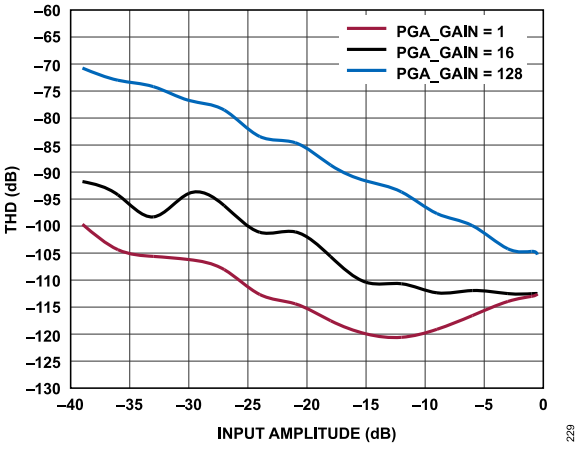

Figure 28. THD vs. Input Amplitude, Various PGA_GAIN, IN1_AAF, 1kHz

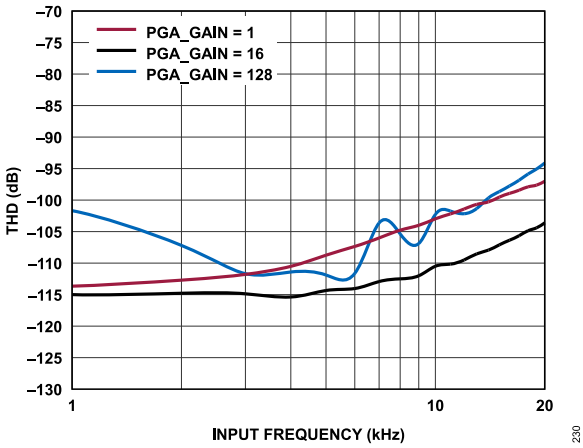

Figure 29. THD vs. Input Frequency across FDA Power Modes at 25°C, PGA_GAIN = 1V/V, IN1_AAF, −0.5dBFS

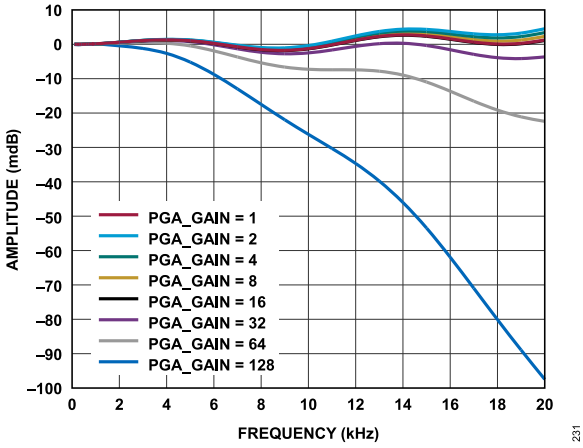

Figure 30. Wideband Low-Ripple FIR Filter Pass-Band Ripple, Various PGA_GAIN, IN1_AAF, ODR = 256kSPS, Normalized to 0dB at DC

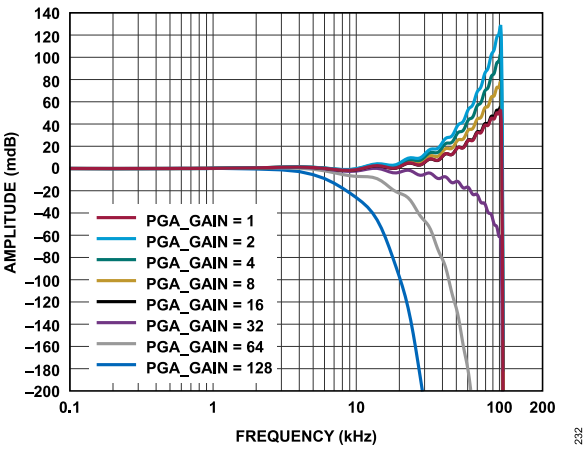

Figure 31. Wideband Low-Ripple FIR Filter Magnitude Flatness, Various PGA_GAIN, IN1_AAF, ODR = 256kSPS, Normalized to 0dB at DC

TYPICAL PERFORMANCE CHARACTERISTICS

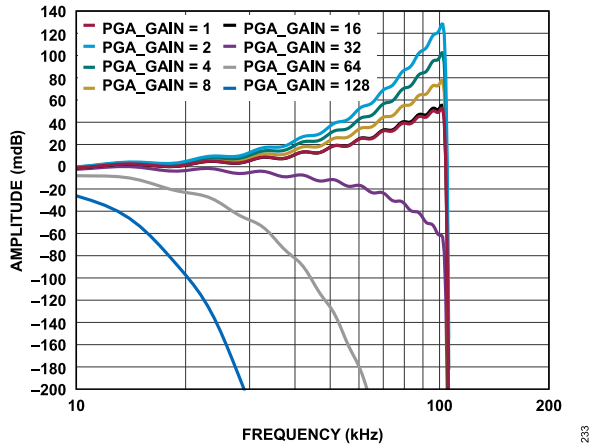

Figure 32. Wideband Low-Ripple FIR Filter Pass-Band Droop, Various PGA_GAIN, IN1_AAF, ODR = 256kSPS, Normalized to 0dB at DC

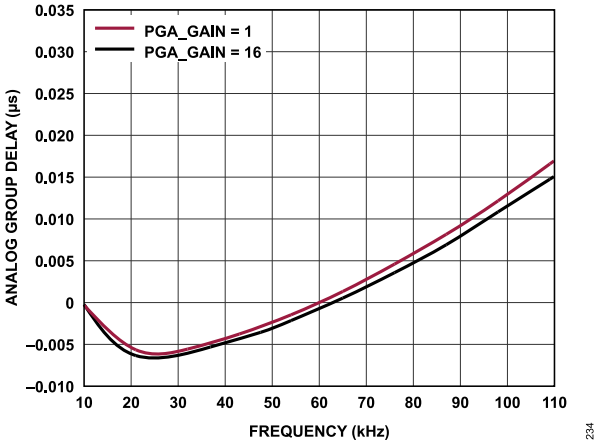

Figure 33. AFE Pass-Band Analog Group Delay vs. Frequency, PGA_GAIN = 1 and PGA_GAIN = 16, IN1_AAF, 25°C, Normalized to Delay at 10kHz

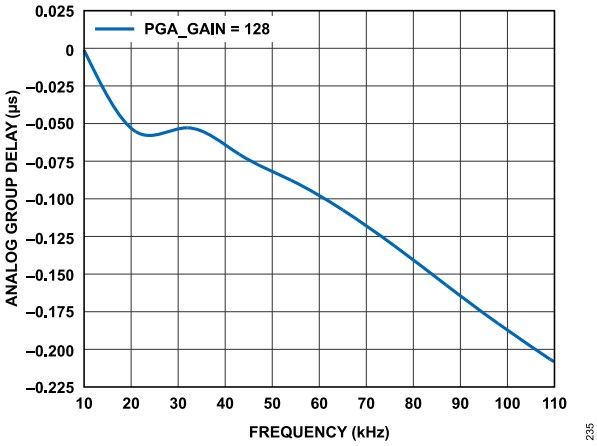

Figure 34. AFE Pass-Band Analog Group Delay vs. Frequency, PGA_GAIN = 128, IN1_AAF, 25°C, Normalized to Delay at 10kHz

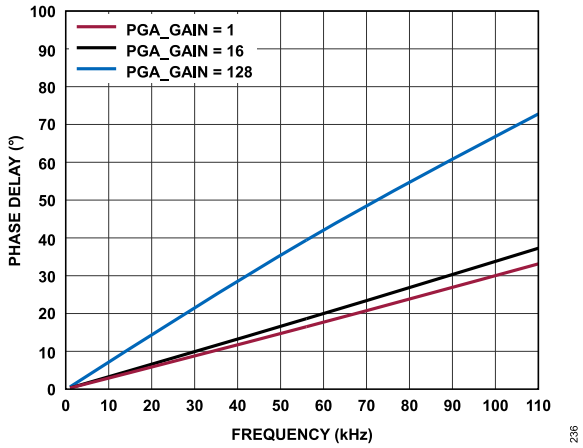

Figure 35. AFE Pass-Band Phase Response, IN1_AAF

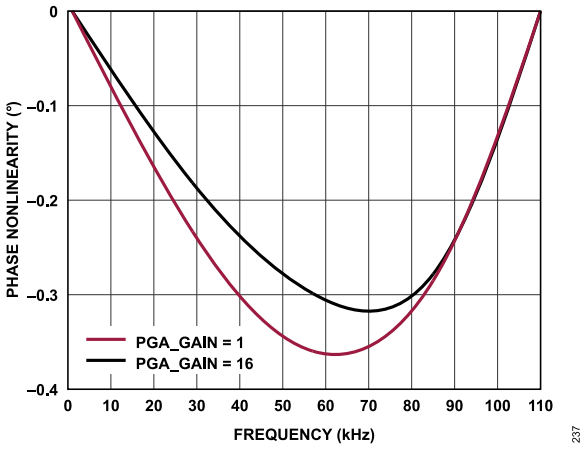

Figure 36. AFE Pass-Band Phase Nonlinearity, PGA_GAIN = 1 and PGA_GAIN = 16, IN1_AAF, Endpoint Method (100Hz to 110kHz)

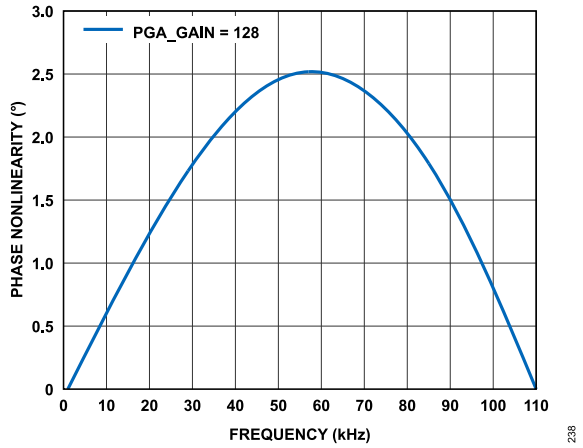

Figure 37. AFE Pass-Band Phase Nonlinearity, PGA_GAIN = 128, IN1_AAF, Endpoint Method (100Hz to 110kHz)

TYPICAL PERFORMANCE CHARACTERISTICS

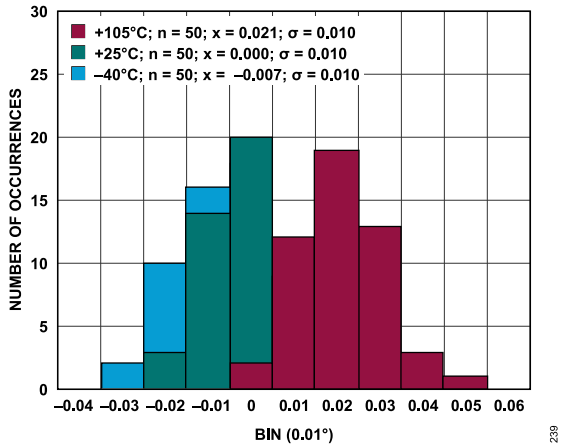

Figure 38. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 1V/V, IN1_AAF, Normalized to Mean Value at 25°C

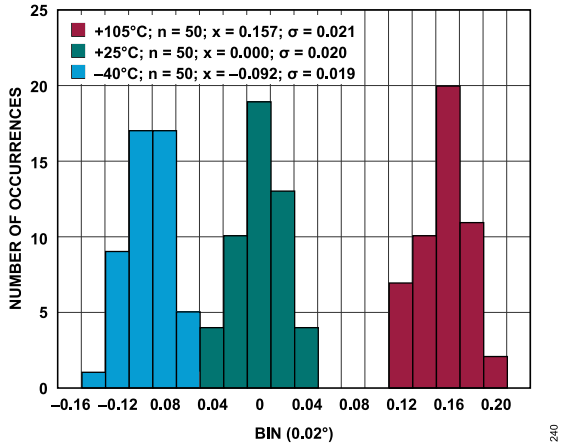

Figure 39. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 16V/V, IN1_AAF, Normalized to Mean Value at 25°C

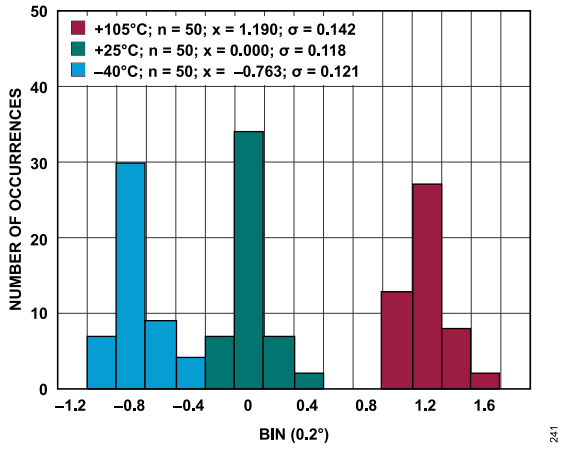

Figure 40. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 128V/V, IN1_AAF, Normalized to Mean Value at 25°C

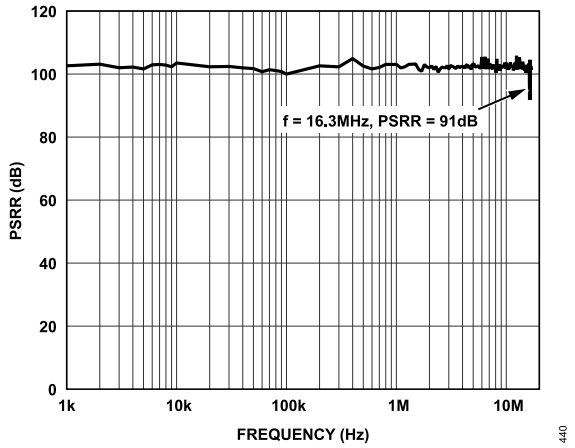

Figure 41. LDO AC PSRR, Connected to VDD_FDA, VDD_ADC, and VDD2_ADC, using Only the internal 0.1µF Supply Decoupling Capacitor

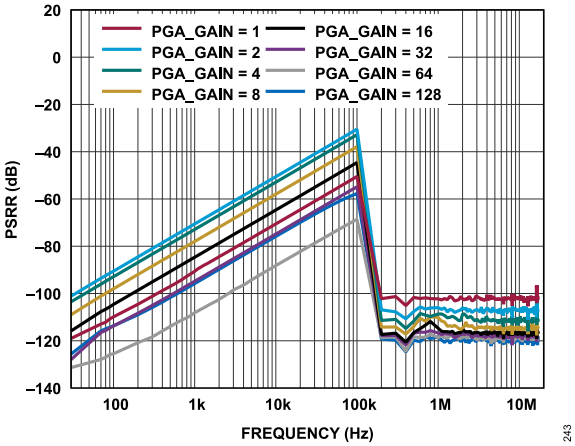

Figure 42. VDD_PGA AC PSSR across All PGA_GAIN, using Only the internal 0.1µF Supply Decoupling Capacitor

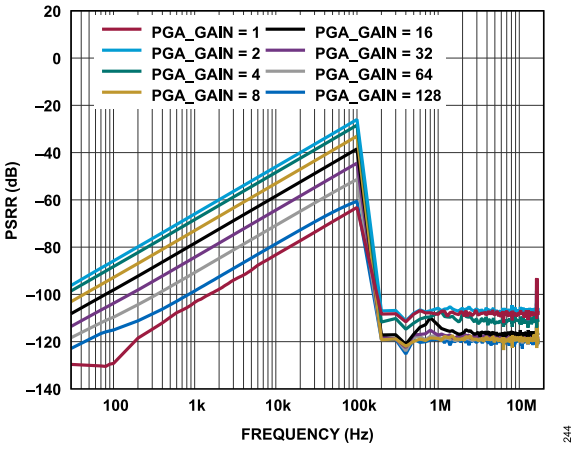

Figure 43. VSS_PGA AC PSSR across All PGA_GAIN, using Only the internal 0.1µF Supply Decoupling Capacitor

TYPICAL PERFORMANCE CHARACTERISTICS

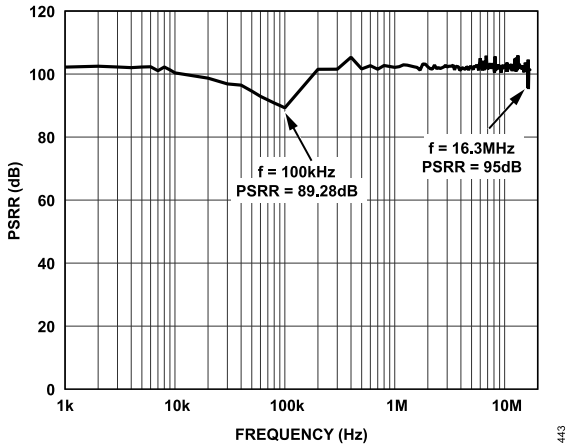

Figure 44. VDD_IO AC PSRR, using Only the internal 0.1µF Supply Decoupling Capacitor

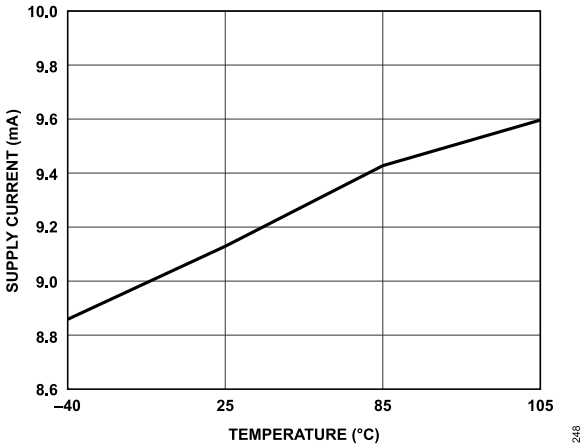

Figure 47. VDD_IO Supply Current vs. Temperature

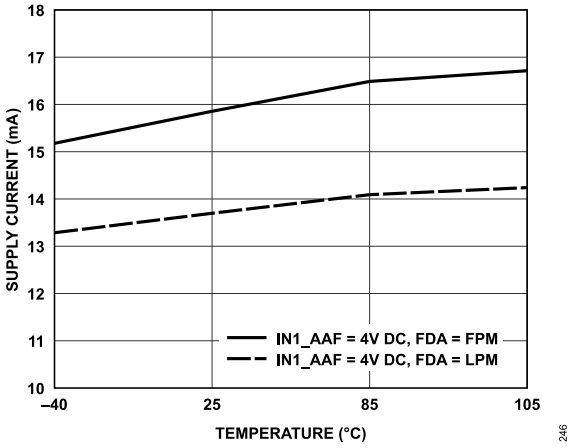

Figure 45. LDO Supply Current vs. Temperature, DC Input, OUT_LDO connected to VDD_FDA, VDD_ADC, and VDD2_ADC

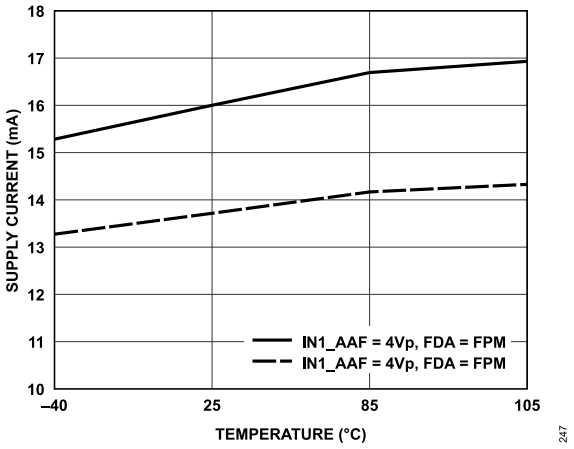

Figure 46. LDO Supply Current vs. Temperature, AC Input, OUT_LDO connected to VDD_FDA, VDD_ADC, and VDD2_ADC

TYPICAL PERFORMANCE CHARACTERISTICS

AAF_GAIN = IN2_AAF

VDD_PGA = 15V, VSS_PGA = −15V, AGND = DGND = 0V, IN_LDO = EN_LDO = 5.1V to 5.5V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2V to 5.5V, VDD_IO = 1.7V to 3.6V, REF+ = 4.096V, REF− = 0V, MCLK = SCLK = 16.384MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband low ripple, Decimation = 32, ODR = 256kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full-power mode, T_A = −40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

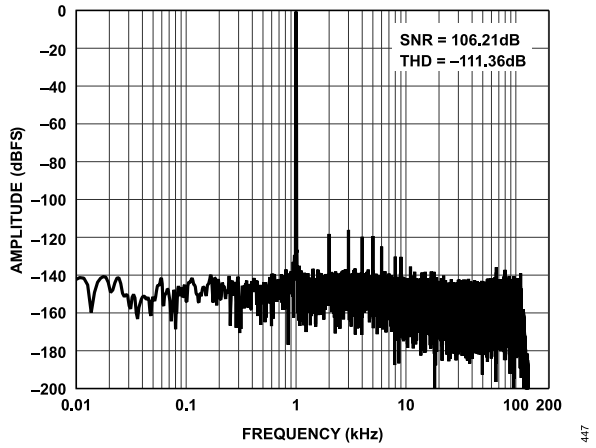

Figure 48. Wideband Low-Ripple FIR Filter, PGA_GAIN = 1V/V, IN2_AAF, Bipolar Single-Ended Input, −0.5dBFS (10.6Vp)

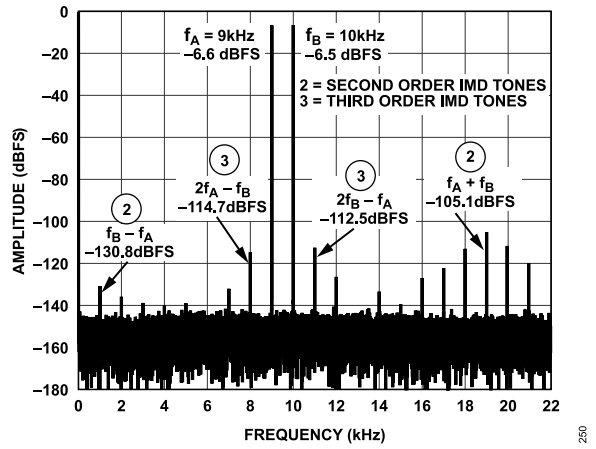

Figure 49. Two-Tone Input, PGA_GAIN = 1V/V, IN2_AAF, f_A = 9kHz and −6.6dBFS, and f_B = 10kHz and −6.5dBFS Sine, Wideband Low-Ripple Filter, ODR = 256kSPS

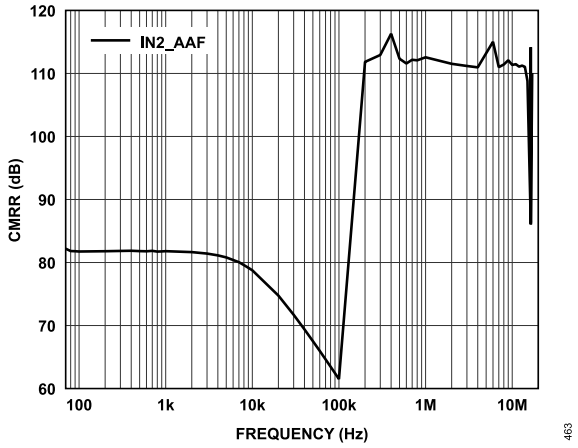

Figure 50. AC CMRR vs. Input Frequency, IN2_AAF

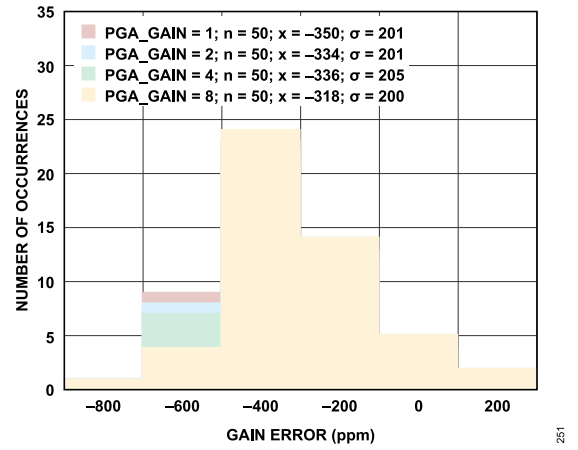

Figure 51. Gain Error Distribution, PGA_GAIN = 1 to PGA_GAIN = 8, IN2_AAF

TYPICAL PERFORMANCE CHARACTERISTICS

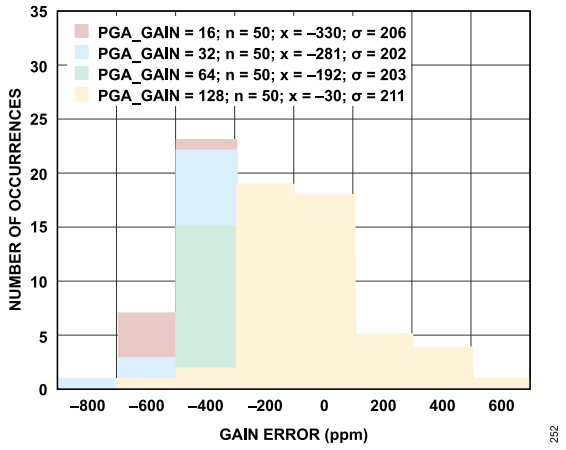

Figure 52. Gain Error Distribution, PGA_GAIN = 16 to PGA_GAIN = 128, IN2_AAF

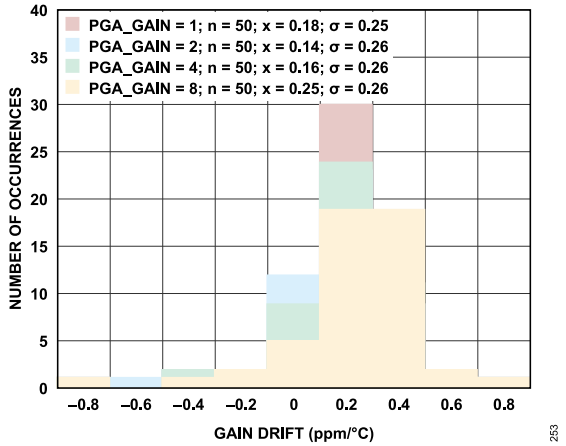

Figure 53. Gain Error Drift Distribution, PGA_GAIN = 1 to PGA_GAIN = 8, IN2_AAF

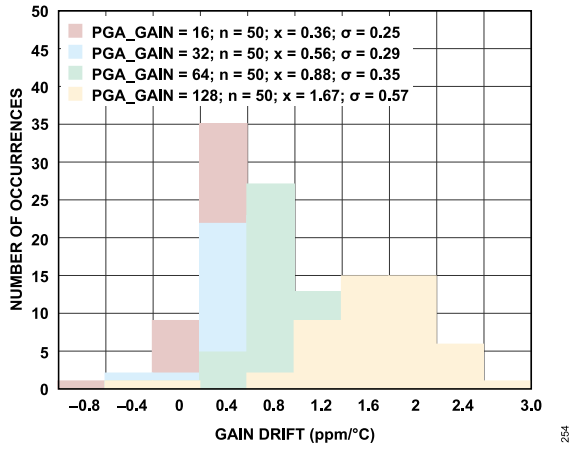

Figure 54. Gain Error Drift Distribution, PGA_GAIN = 16 to PGA_GAIN = 128, IN2_AAF

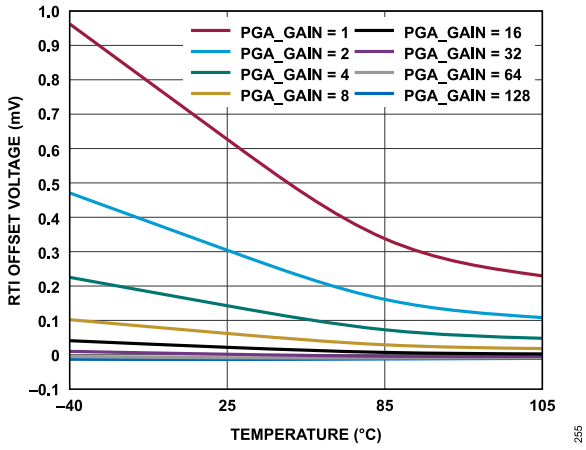

Figure 55. Offset Error vs. Temperature, IN2_AAF

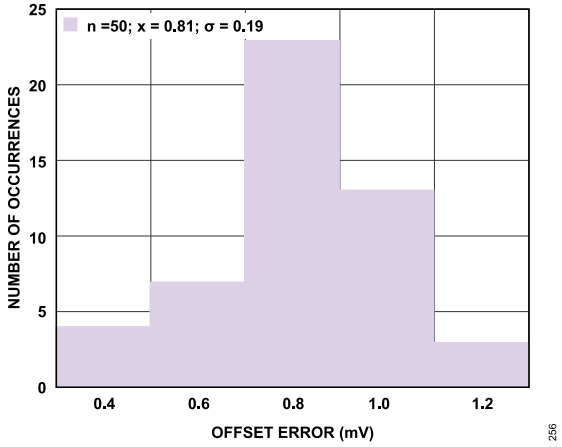

Figure 56. Offset Error Distribution, PGA_GAIN = 1V/V, IN2_AAF

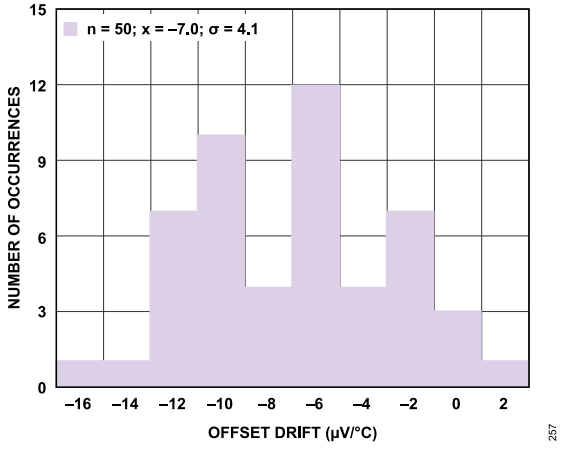

Figure 57. Offset Error Drift Distribution, PGA_GAIN = 1V/V, IN2_AAF

TYPICAL PERFORMANCE CHARACTERISTICS

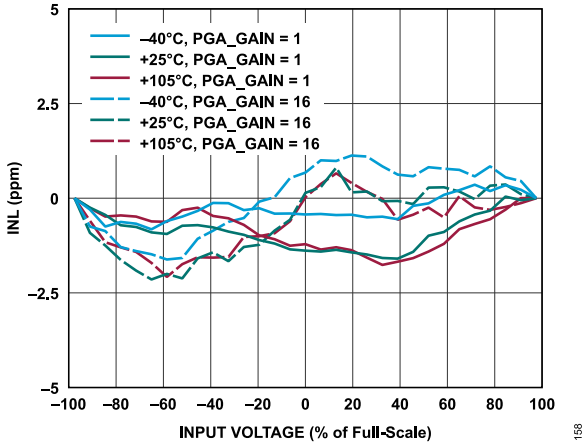

Figure 58. INL Error vs. Input Voltage over Temperature, PGA_GAIN = 1V/V and PGA_GAIN = 16V/V, IN2_AAF

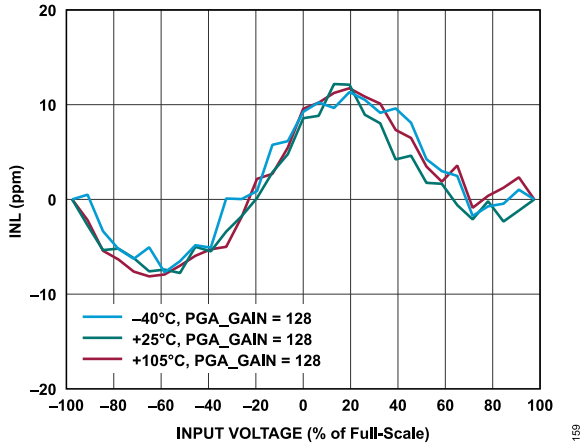

Figure 59. INL Error vs. Input Voltage over Temperature, PGA_GAIN = 128V/V, IN2_AAF

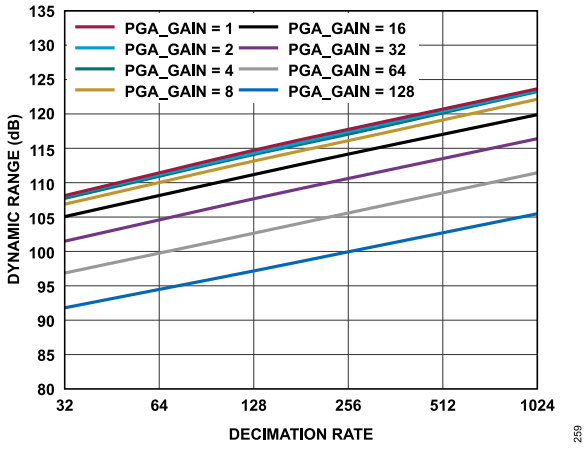

Figure 60. Dynamic Range vs. Decimation Rate, Various PGA_GAIN, IN2_AAF, Wideband Low-Ripple Filter, Shorted Input

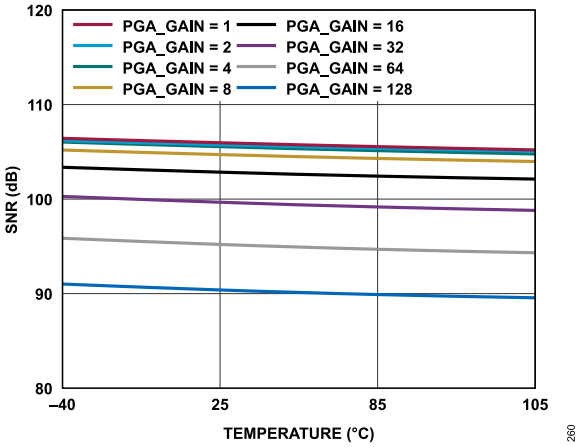

Figure 61. SNR vs. Temperature, Various PGA_GAIN, IN2_AAF, Wideband Low-Ripple Filter, −0.5dBFS (10.6Vp), 1kHz

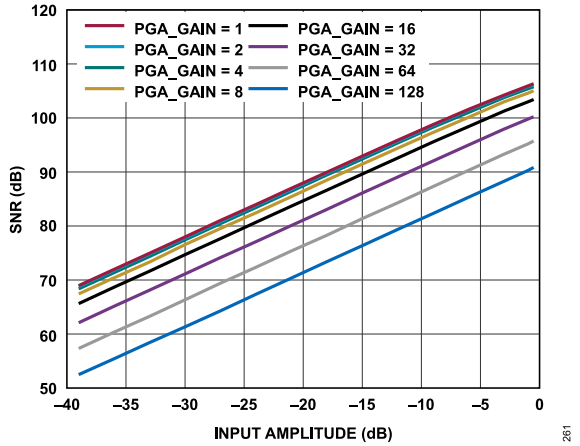

Figure 62. SNR vs. Input Amplitude, Various PGA_GAIN, IN2_AAF, Wideband Low-Ripple Filter, 1kHz

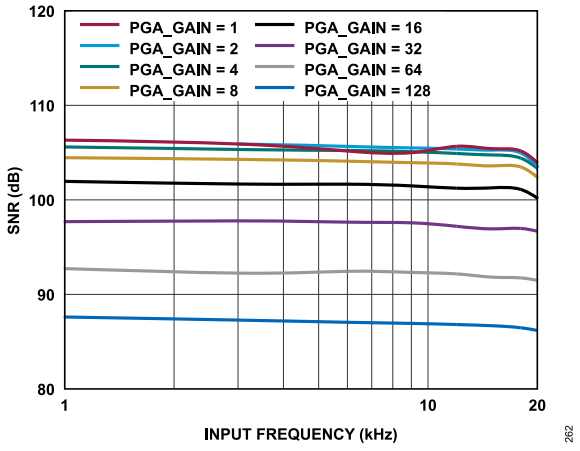

Figure 63. SNR vs. Input Frequency, Various PGA_GAIN, IN2_AAF, −0.5dBFS, FDA = Full Power

TYPICAL PERFORMANCE CHARACTERISTICS

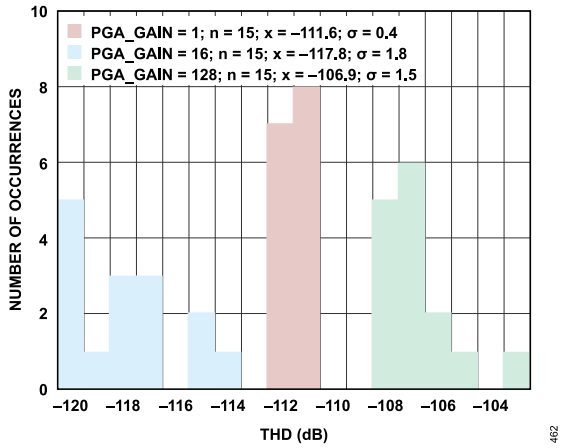

Figure 64. THD Distribution, Various PGA_GAIN, IN2_AAF, −0.5dBFS, 1kHz

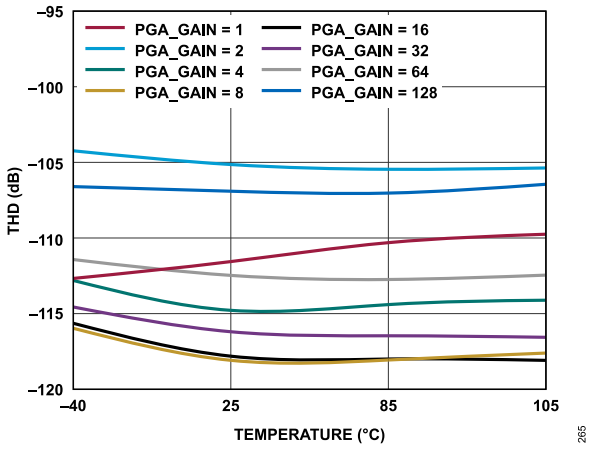

Figure 65. THD vs. Temperature, Various PGA_GAIN, IN2_AAF, −0.5dBFS (10.6Vp), 1kHz

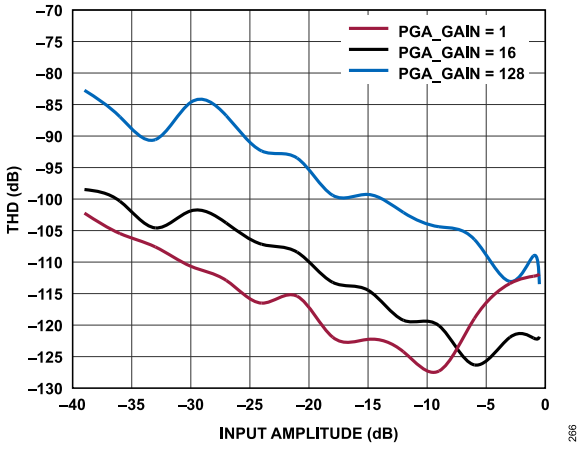

Figure 66. THD vs. Input Amplitude, Various PGA_GAIN, IN2_AAF, 1kHz

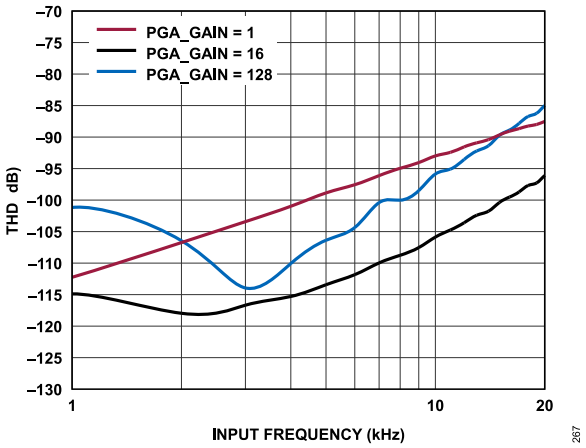

Figure 67. THD vs. Input Frequency across FDA Power Modes at 25°C, PGA_GAIN = 1V/V, IN2_AAF, −0.5dBFS

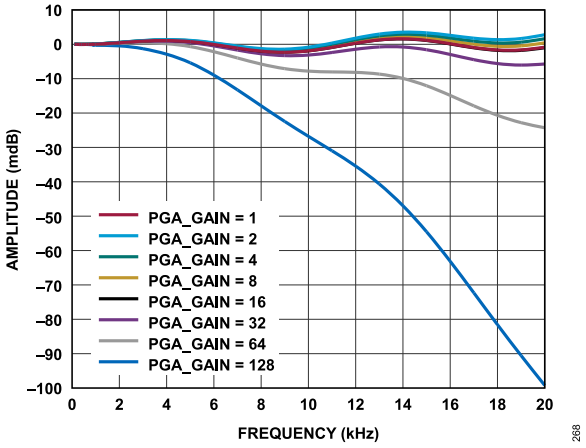

Figure 68. Wideband Low-Ripple FIR Filter Pass-Band Ripple, Various PGA_GAIN, IN2_AAF, ODR = 256kSPS, Normalized to 0dB at DC

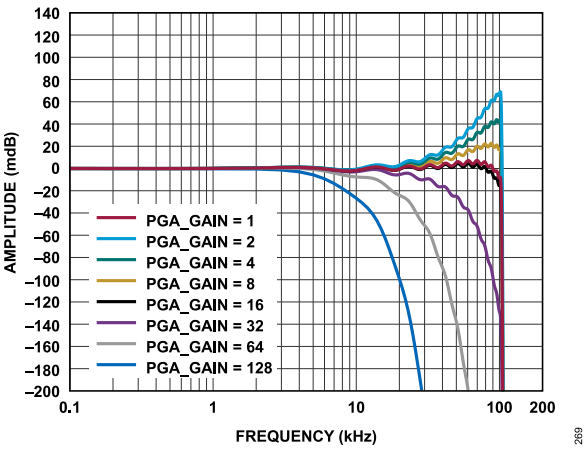

Figure 69. Wideband Low-Ripple FIR Filter Magnitude Flatness, Various PGA_GAIN, IN2_AAF, ODR = 256kSPS, Normalized to 0dB at DC

TYPICAL PERFORMANCE CHARACTERISTICS

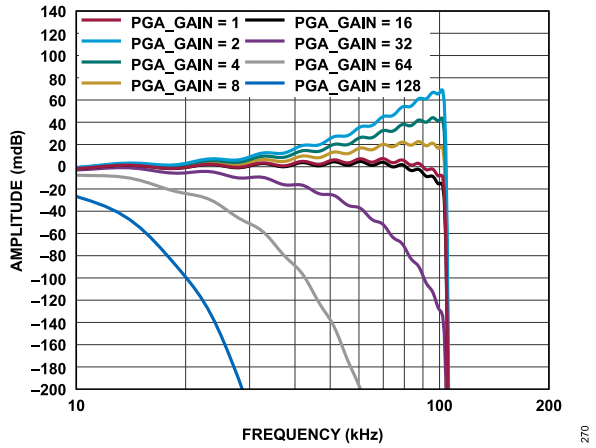

Figure 70. Wideband Low-Ripple FIR Filter Pass-Band Droop, Various PGA_GAIN, IN2_AAF, ODR = 256kSPS, Normalized to 0dB at DC

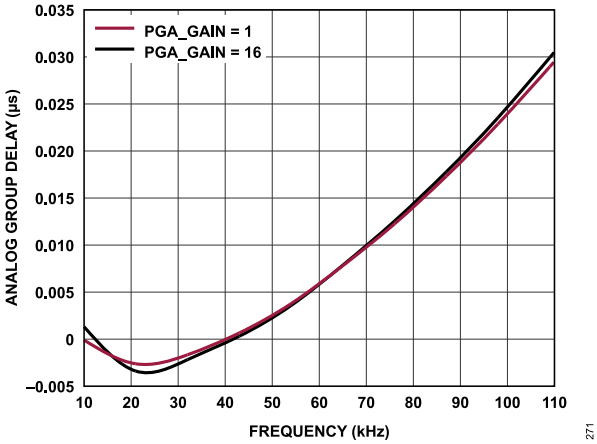

Figure 71. AFE Pass-Band Analog Group Delay vs. Frequency, PGA_GAIN = 1 and PGA_GAIN = 16, IN2_AAF, 25°C, Normalized to Delay at 10kHz

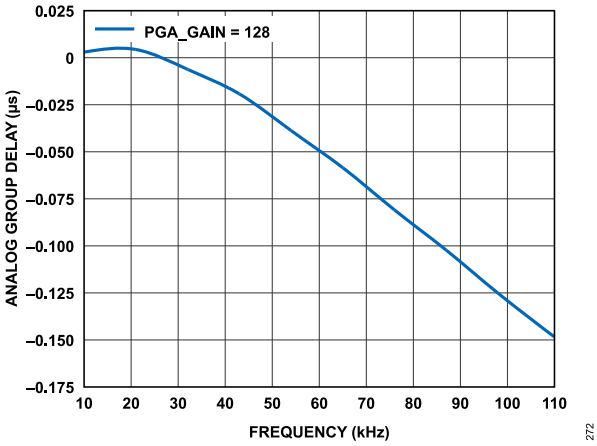

Figure 72. AFE Pass-Band Analog Group Delay vs. Frequency, PGA_GAIN = 128, IN2_AAF, 25°C, Normalized to Delay at 10kHz

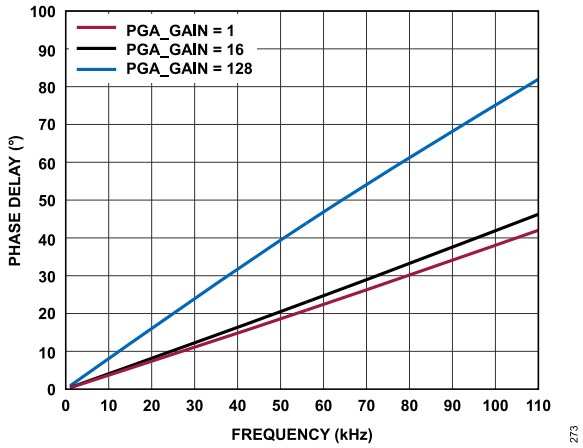

Figure 73. AFE Pass-Band Phase Response, IN2_AAF

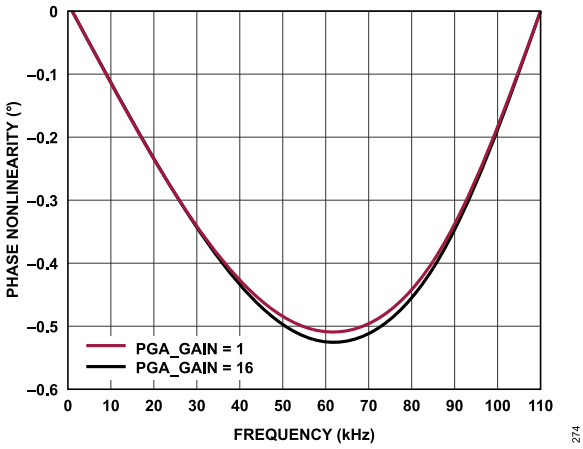

Figure 74. AFE Pass-Band Phase Nonlinearity, PGA_GAIN = 1 and PGA_GAIN = 16, IN2_AAF, Endpoint Method (100Hz to 110kHz)

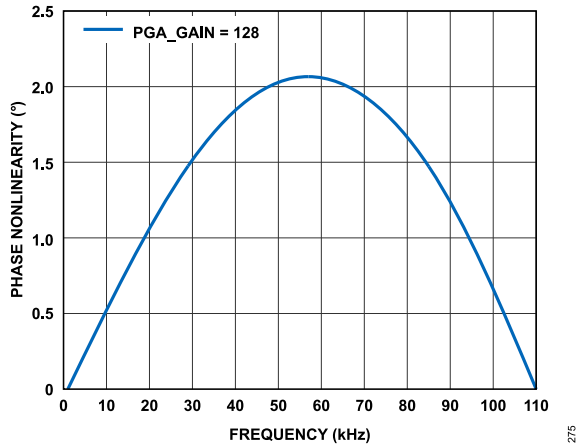

Figure 75. AFE Pass-Band Phase Nonlinearity, PGA_GAIN = 128, IN2_AAF, Endpoint Method (100Hz to 110kHz)

TYPICAL PERFORMANCE CHARACTERISTICS

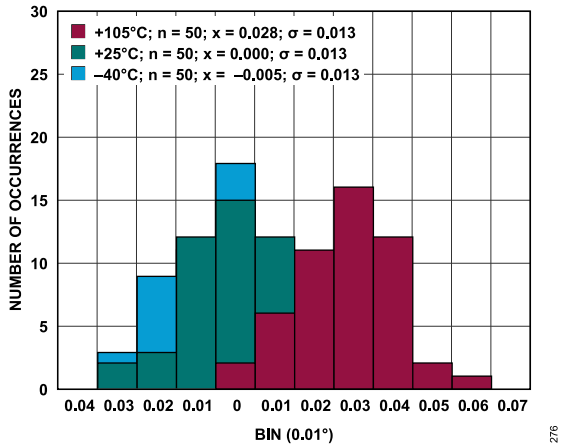

Figure 76. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 1V/V, IN2_AAF, Normalized to Mean Value at 25°C

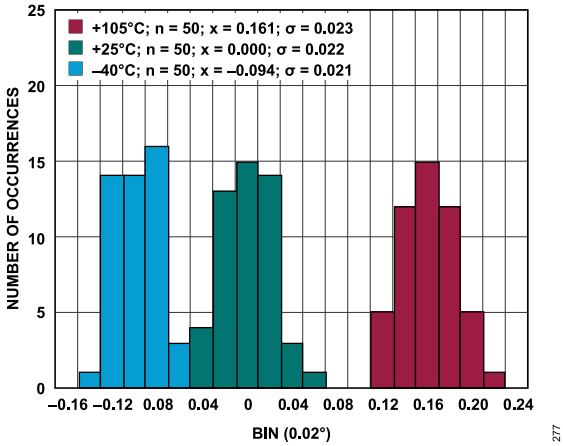

Figure 77. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 16V/V, IN2_AAF, Normalized to Mean Value at 25°C

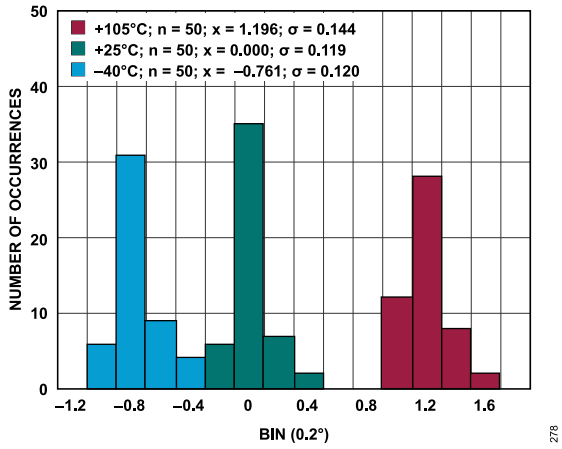

Figure 78. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 128V/V, IN2_AAF, Normalized to Mean Value at 25°C

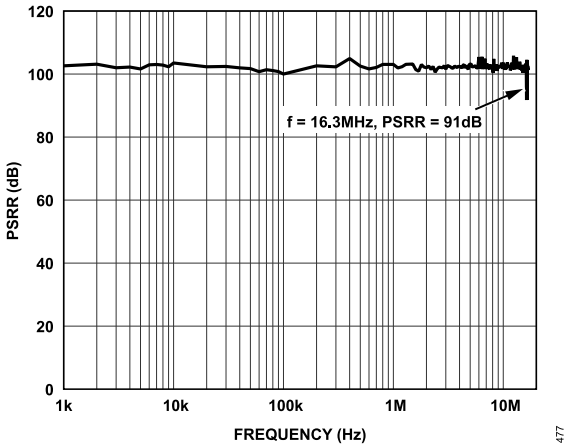

Figure 79. LDO AC PSRR, Connected to VDD_FDA, VDD_ADC, and VDD2_ADC, using Only the internal 0.1µF Supply Decoupling Capacitor

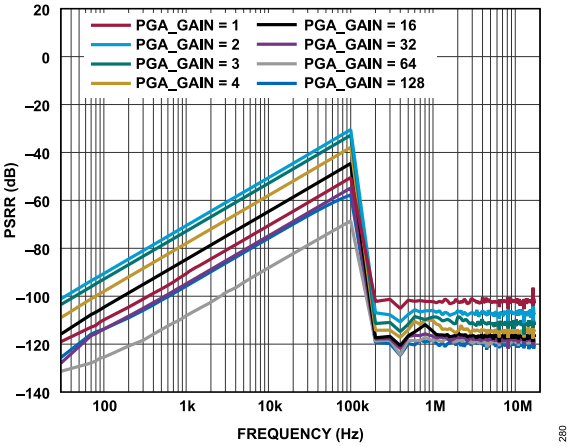

Figure 80. VDD_PGA AC PSSR across All PGA_GAIN, using Only the internal 0.1µF Supply Decoupling Capacitor

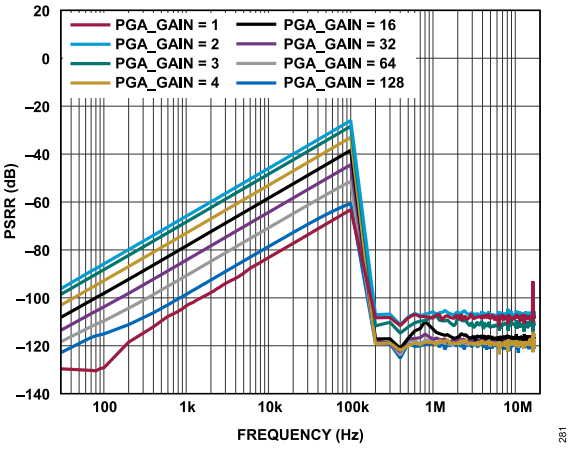

Figure 81. VSS_PGA AC PSSR across All PGA_GAIN, using Only the internal 0.1µF Supply Decoupling Capacitor

TYPICAL PERFORMANCE CHARACTERISTICS

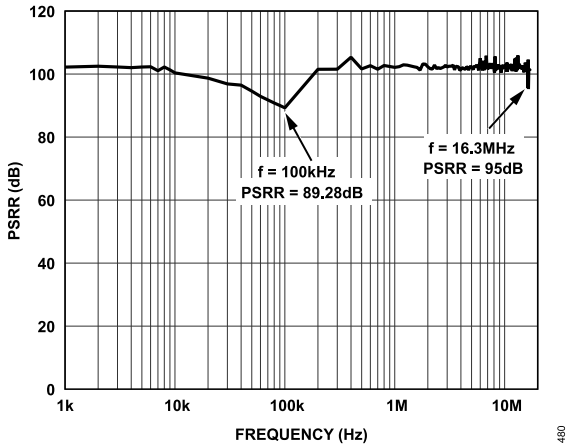

Figure 82. VDD_IO AC PSRR, using Only the internal 0.1µF Supply Decoupling Capacitor

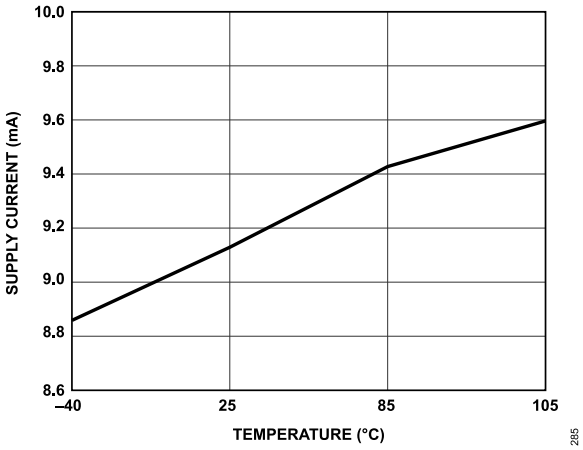

Figure 85. VDD_IO Supply Current vs. Temperature

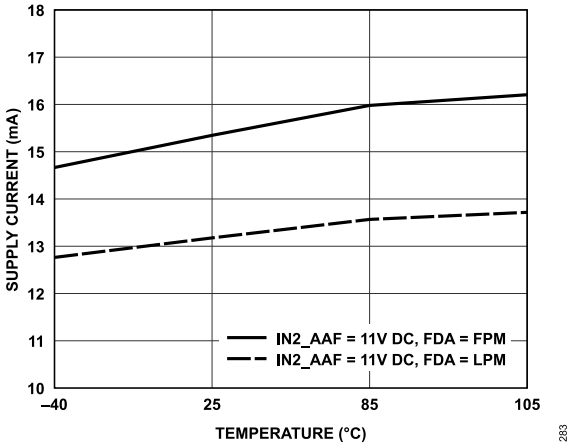

Figure 83. LDO Supply Current vs. Temperature, DC Input, OUT_LDO connected to VDD_FDA, VDD_ADC, and VDD2_ADC

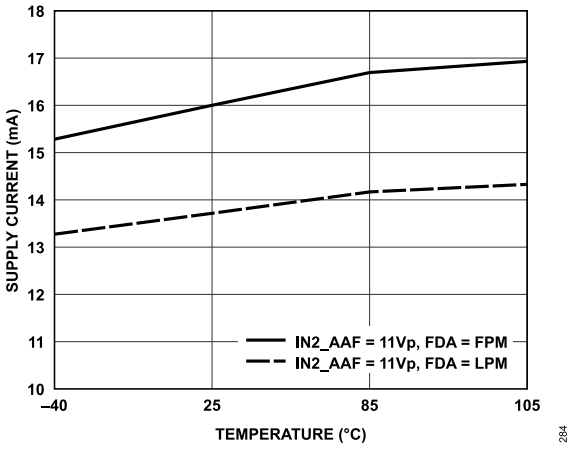

Figure 84. LDO Supply Current vs. Temperature, AC Input, OUT_LDO connected to VDD_FDA, VDD_ADC, and VDD2_ADC

TYPICAL PERFORMANCE CHARACTERISTICS

AAF_GAIN = IN3_AAF

VDD_PGA = 20V, VSS_PGA = −16V, AGND = DGND = 0V, IN_LDO = EN_LDO = 5.1V to 5.5 V, OUT_LDO = VDD_FDA = VDD_ADC, VDD2_ADC = 2V to 5.5V, VDD_IO = 1.7V to 3.6V, REF+ = 4.096V, REF− = 0V, MCLK = SCLK = 16.384MHz 50:50 duty cycle, f_{MOD} = MCLK/2, Filter = Wideband low ripple, Decimation = 32, ODR = 256kSPS, linearity boost buffer on, reference precharge buffers on, FDA = Full-power mode, T_A = −40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C.

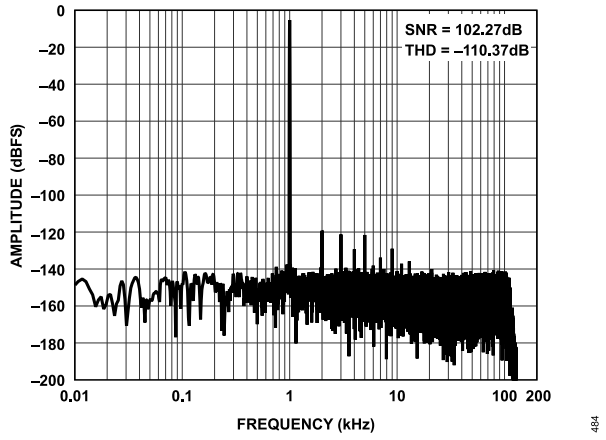

Figure 86. Wideband Low-Ripple FIR Filter, PGA_GAIN = 1V/V, IN3_AAF, Bipolar Single-Ended Input, −5.2dBFS (15.7Vp)

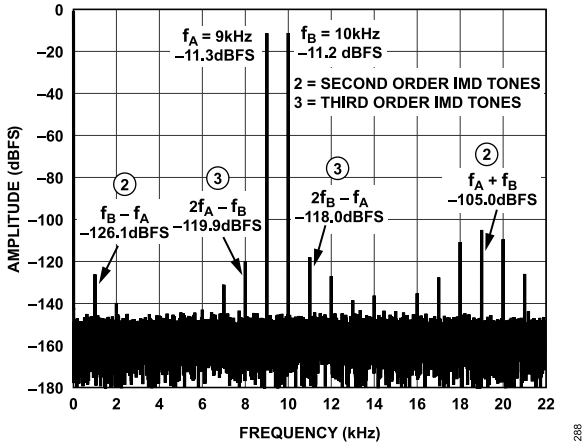

Figure 87. Two-Tone Input, PGA_GAIN = 1V/V, IN3_AAF, f_A = 9kHz and −11.3dBFS, and f_B = 10kHz and −11.2dBFS Sine, Wideband Low-Ripple Filter, ODR = 256kSPS

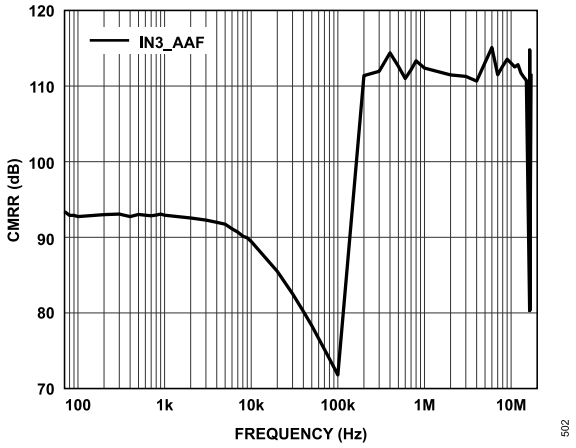

Figure 88. AC CMRR vs. Input Frequency, IN3_AAF

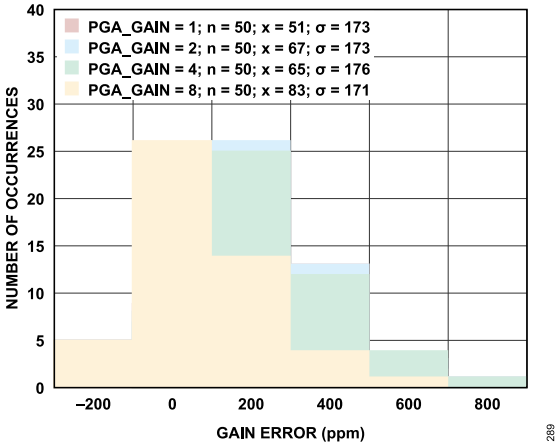

Figure 89. Gain Error Distribution, PGA_GAIN = 1 to PGA_GAIN = 8, IN3_AAF

TYPICAL PERFORMANCE CHARACTERISTICS

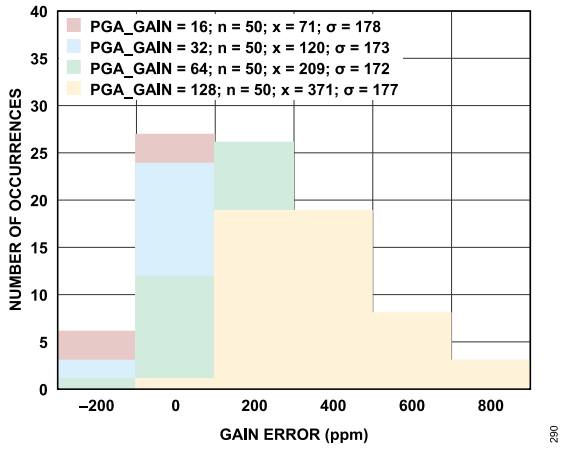

Figure 90. Gain Error Distribution, PGA_GAIN = 16 to PGA_GAIN = 128, IN3_AAF

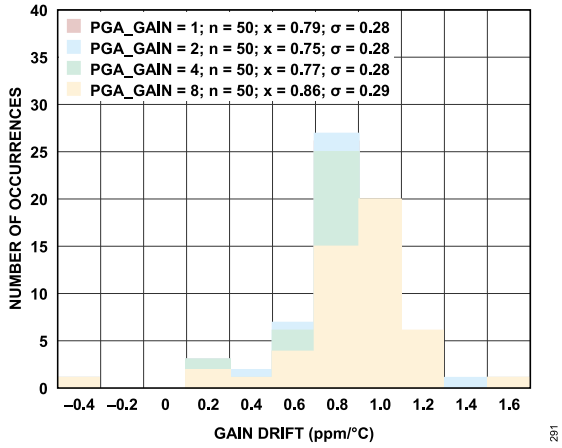

Figure 91. Gain Error Drift Distribution, PGA_GAIN = 1 to PGA_GAIN = 8, IN3_AAF

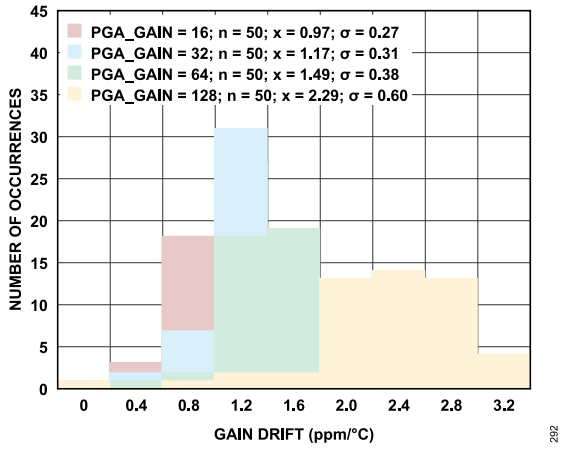

Figure 92. Gain Error Drift Distribution, PGA_GAIN = 16 to PGA_GAIN = 128, IN3_AAF

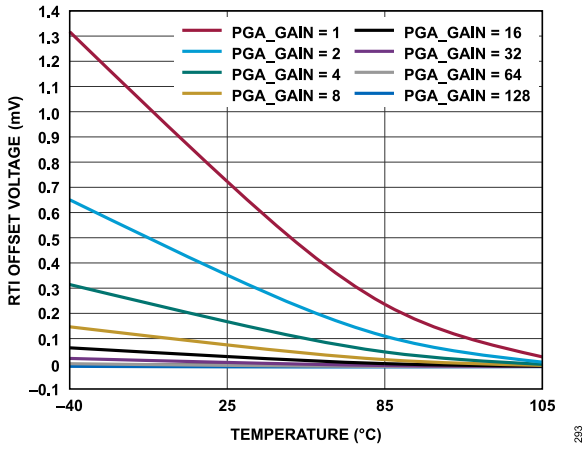

Figure 93. Offset Error vs. Temperature, IN3_AAF

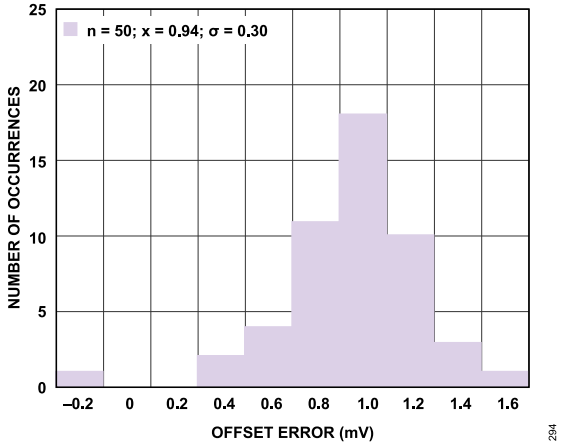

Figure 94. Offset Error Distribution, PGA_GAIN = 1V/V, IN3_AAF

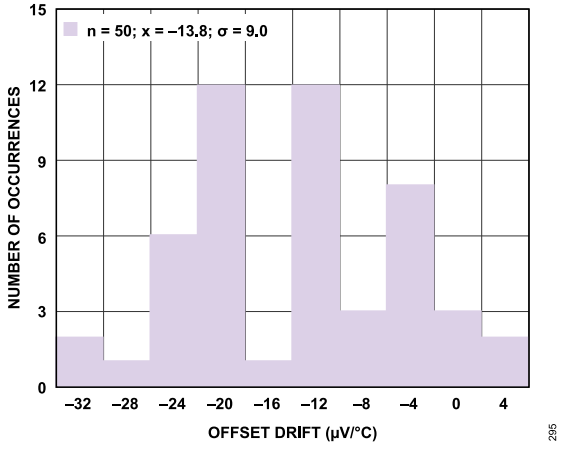

Figure 95. Offset Error Drift Distribution, PGA_GAIN = 1V/V, IN3_AAF

TYPICAL PERFORMANCE CHARACTERISTICS

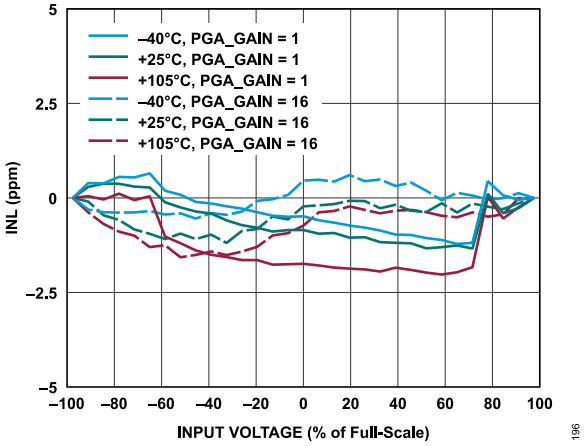

Figure 96. INL Error vs. Input Voltage over Temperature, PGA_GAIN = 1V/V and PGA_GAIN = 16V/V, IN3_AAF

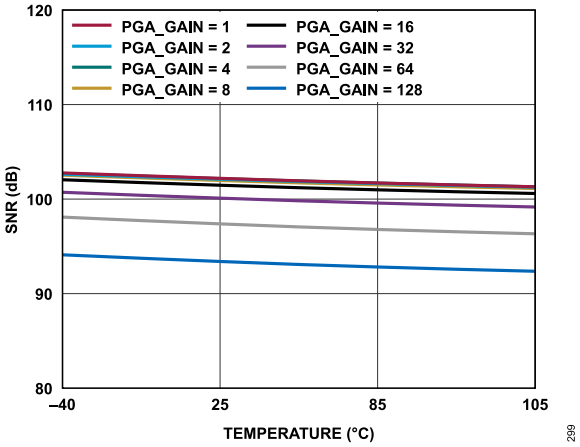

Figure 99. SNR vs. Temperature, Various PGA_GAIN, IN3_AAF, Wideband Low-Ripple Filter, −5.2dBFS (15.7Vp), 1kHz

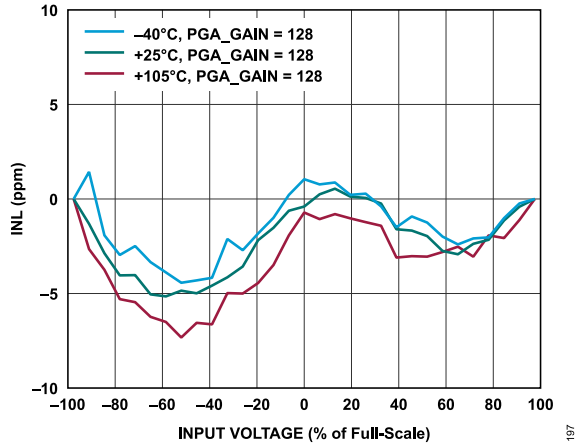

Figure 97. INL Error vs. Input Voltage over Temperature, PGA_GAIN = 128V/V, IN3_AAF

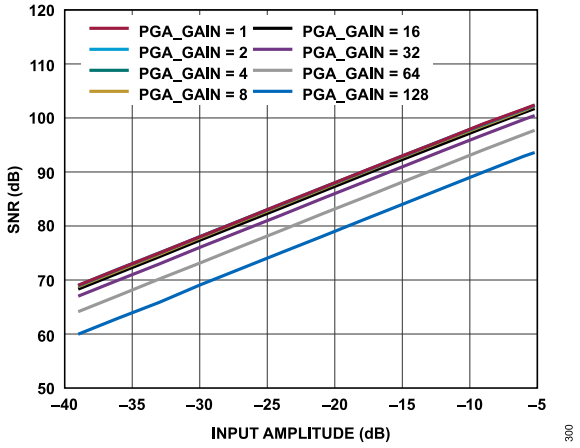

Figure 100. SNR vs. Input Amplitude, Various PGA_GAIN, IN3_AAF, Wideband Low-Ripple Filter, 1kHz

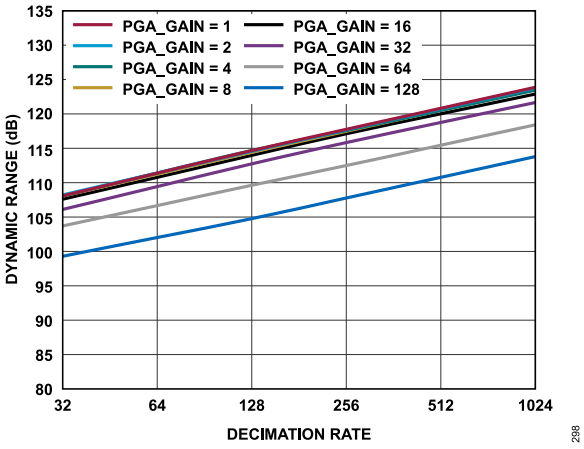

Figure 98. Dynamic Range vs. Decimation Rate, Various PGA_GAIN, IN3_AAF, Wideband Low-Ripple Filter, Shorted Input

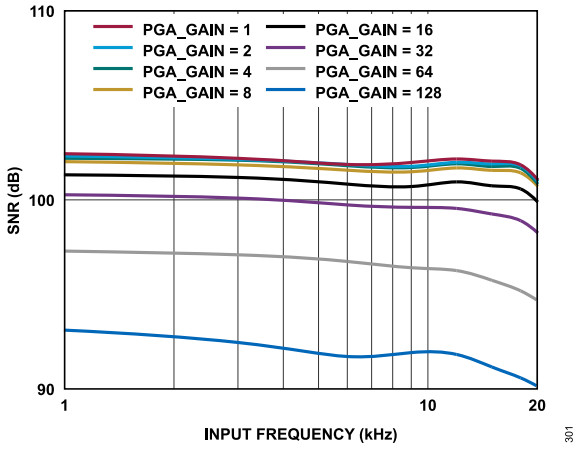

Figure 101. SNR vs. Input Frequency, Various PGA_GAIN, IN3_AAF, −5.2dBFS, FDA = Full Power

TYPICAL PERFORMANCE CHARACTERISTICS

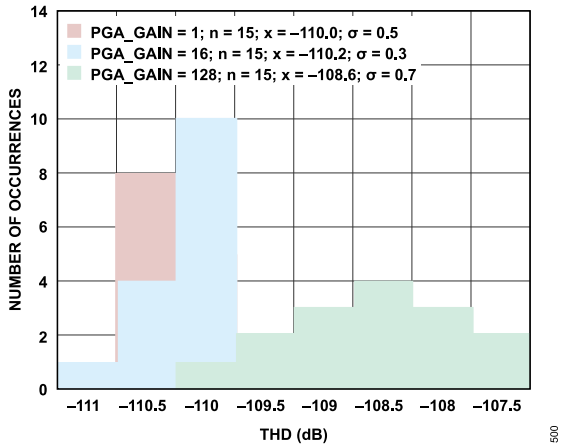

Figure 102. THD Distribution, Various PGA_GAIN, IN3_AAF, −7.2dBFS, 1kHz

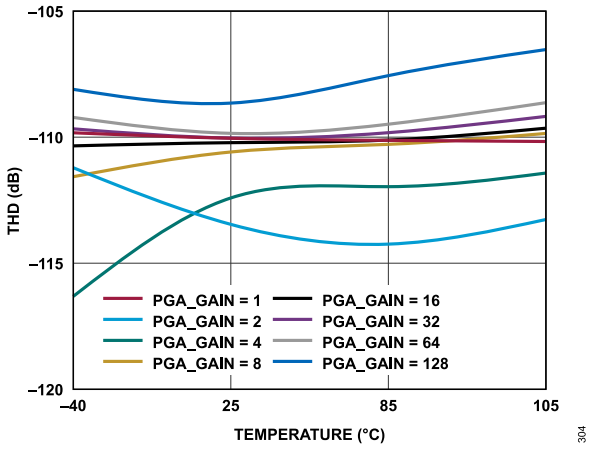

Figure 103. THD vs. Temperature, Various PGA_GAIN, IN3_AAF, −5.2dBFS (15.7Vp), 1kHz

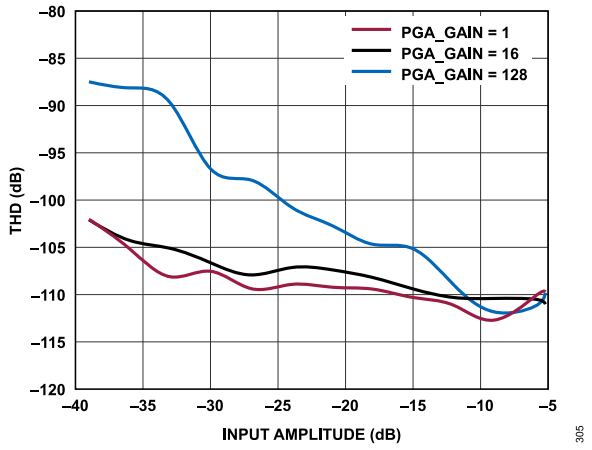

Figure 104. THD vs. Input Amplitude, Various PGA_GAIN, IN3_AAF, 1kHz

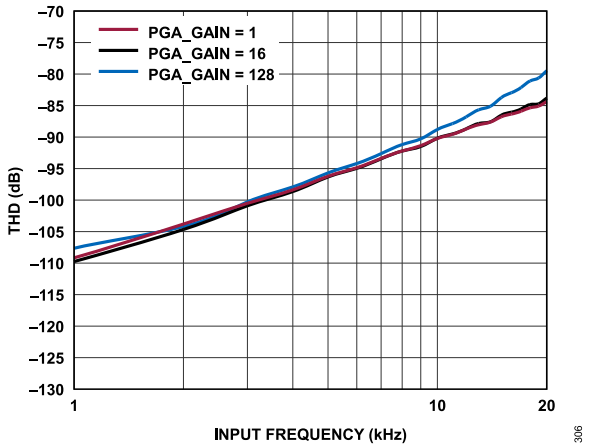

Figure 105. THD vs. Input Frequency across FDA Power Modes at 25°C, PGA_GAIN = 1V/V, IN3_AAF, −5.2dBFS

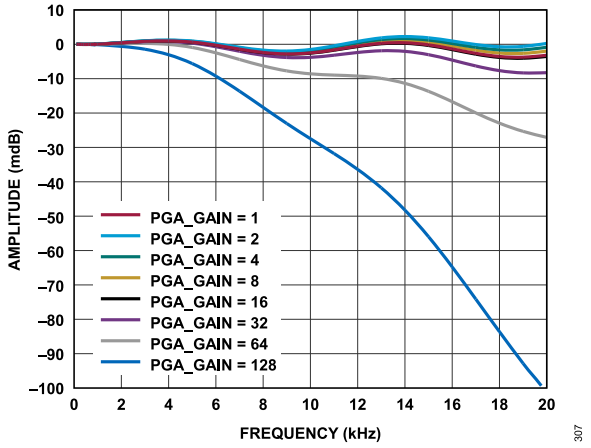

Figure 106. Wideband Low-Ripple FIR Filter Pass-Band Ripple, Various PGA_GAIN, IN3_AAF, ODR = 256kSPS, Normalized to 0dB at DC

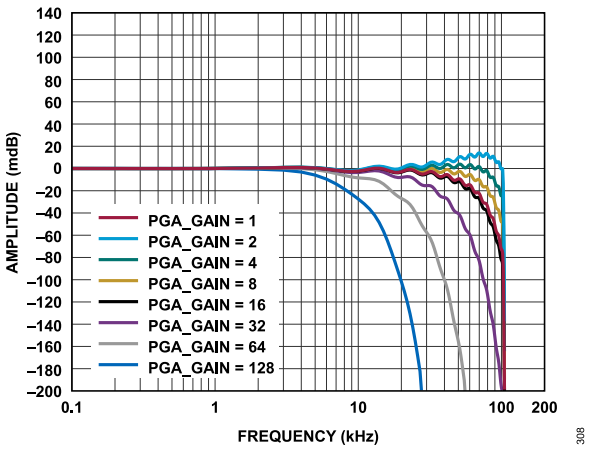

Figure 107. Wideband Low-Ripple FIR Filter Magnitude Flatness, Various PGA_GAIN, IN3_AAF, ODR = 256kSPS, Normalized to 0dB at DC

TYPICAL PERFORMANCE CHARACTERISTICS

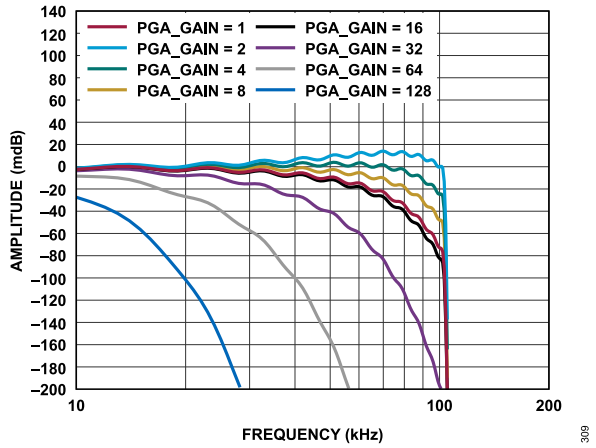

Figure 108. Wideband Low-Ripple FIR Filter Pass-Band Droop, Various PGA_GAIN, IN3_AAF, ODR = 256kSPS, Normalized to 0dB at DC

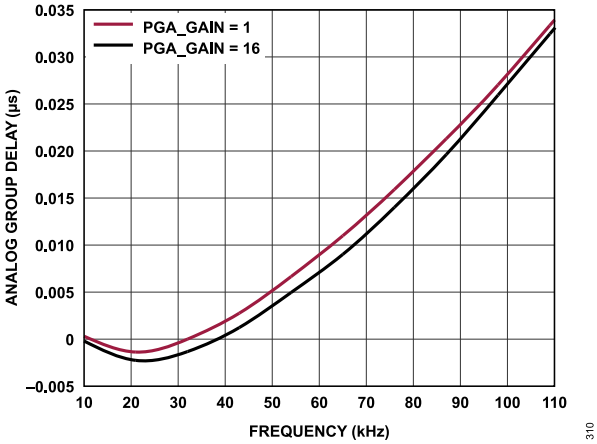

Figure 109. AFE Pass-Band Analog Group Delay vs. Frequency, PGA_GAIN = 1 and PGA_GAIN = 16, IN3_AAF, 25°C, Normalized to Delay at 10kHz

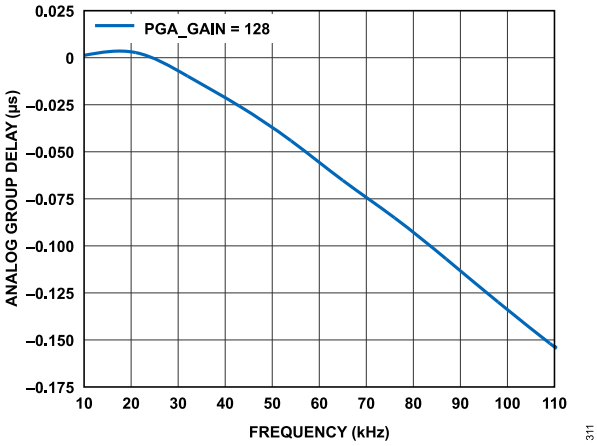

Figure 110. AFE Pass-Band Analog Group Delay vs. Frequency, PGA_GAIN = 128, IN3_AAF, 25°C, Normalized to Delay at 10kHz

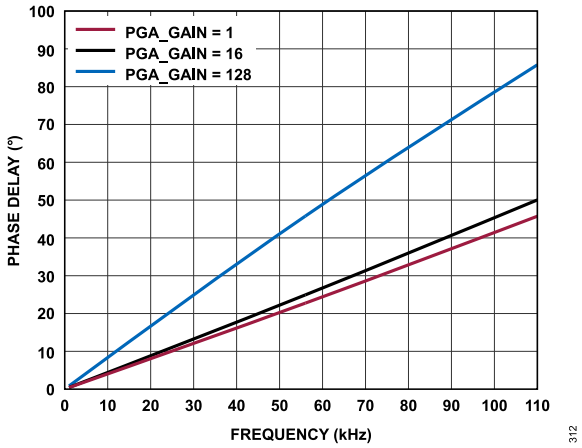

Figure 111. AFE Pass-Band Phase Response, IN3_AAF

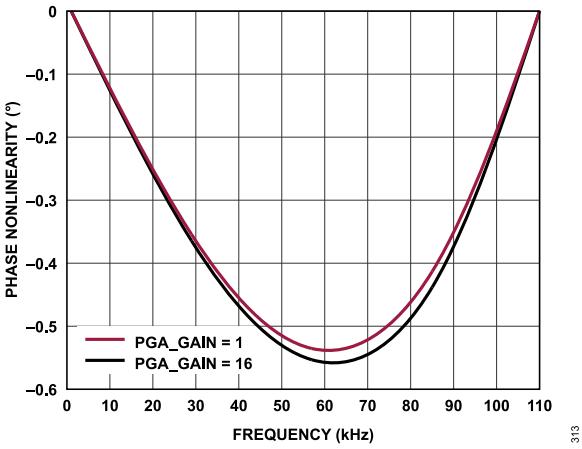

Figure 112. AFE Pass-Band Phase Nonlinearity, PGA_GAIN = 1 and PGA_GAIN = 16, IN3_AAF, Endpoint Method (100Hz to 110kHz)

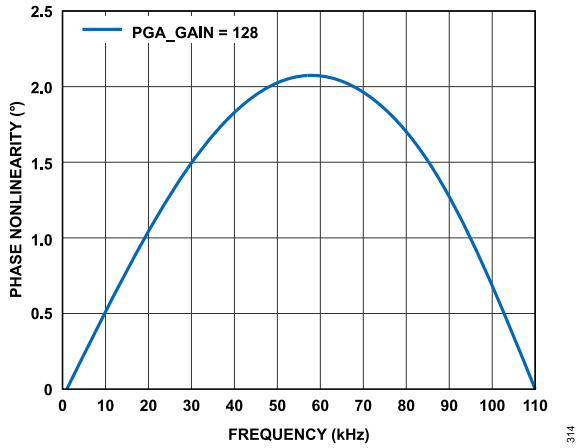

Figure 113. AFE Pass-Band Phase Nonlinearity, PGA_GAIN = 128, IN3_AAF, Endpoint Method (100Hz to 110kHz)

TYPICAL PERFORMANCE CHARACTERISTICS

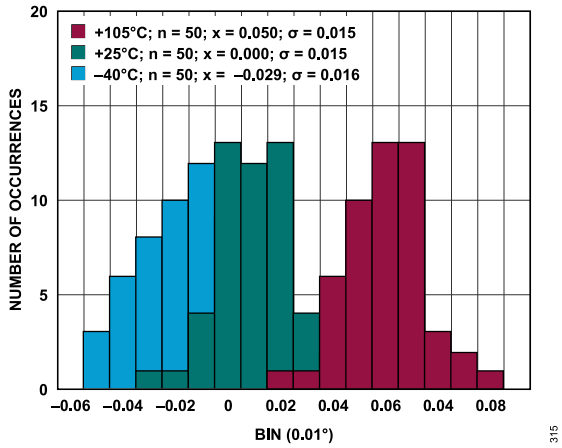

Figure 114. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 1V/V, IN3_AAF, Normalized to Mean Value at 25°C

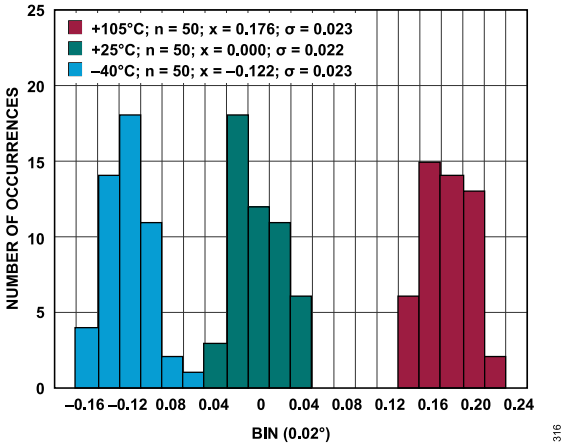

Figure 115. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 16V/V, IN3_AAF, Normalized to Mean Value at 25°C

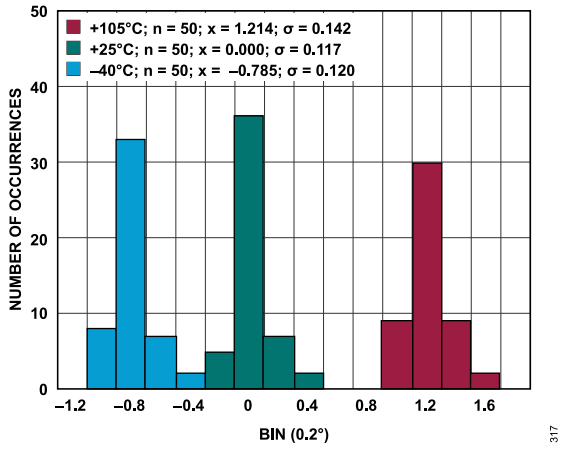

Figure 116. Device-to-Device Phase Angle Mismatch Histogram, 20kHz, PGA_GAIN = 128V/V, IN3_AAF, Normalized to Mean Value at 25°C

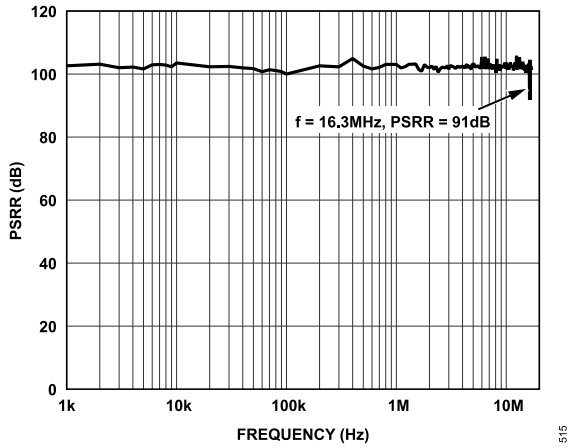

Figure 117. LDO AC PSRR, Connected to VDD_FDA, VDD_ADC, and VDD2_ADC, using Only the internal 0.1µF Supply Decoupling Capacitor

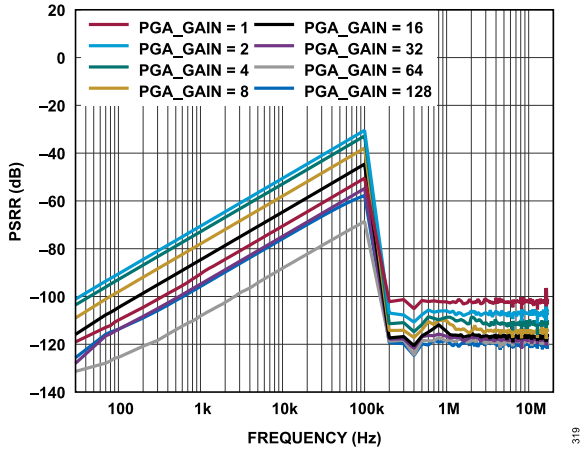

Figure 118. VDD_PGA AC PSSR across All PGA_GAIN, using Only the internal 0.1µF Supply Decoupling Capacitor

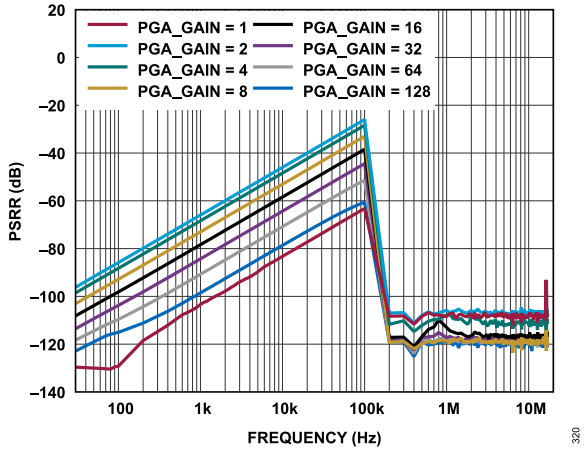

Figure 119. VSS_PGA AC PSSR across All PGA_GAIN, using Only the internal 0.1µF Supply Decoupling Capacitor

TYPICAL PERFORMANCE CHARACTERISTICS

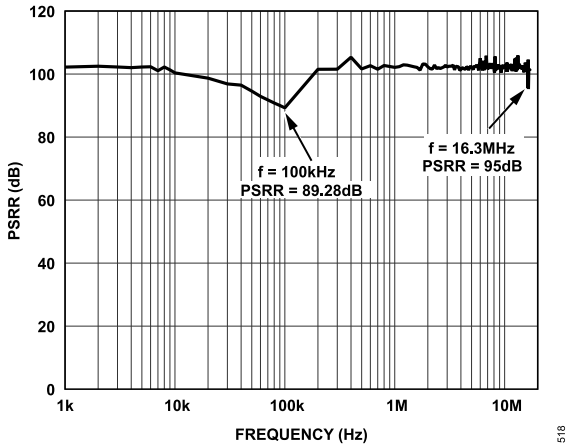

Figure 120. VDD_IO AC PSRR, using Only the internal 0.1µF Supply Decoupling Capacitor

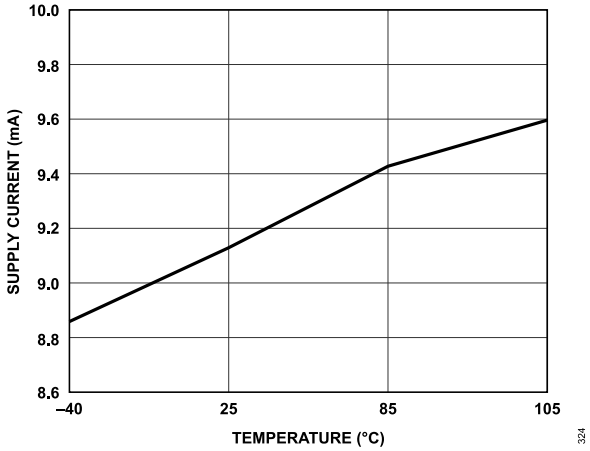

Figure 123. VDD_IO Supply Current vs. Temperature

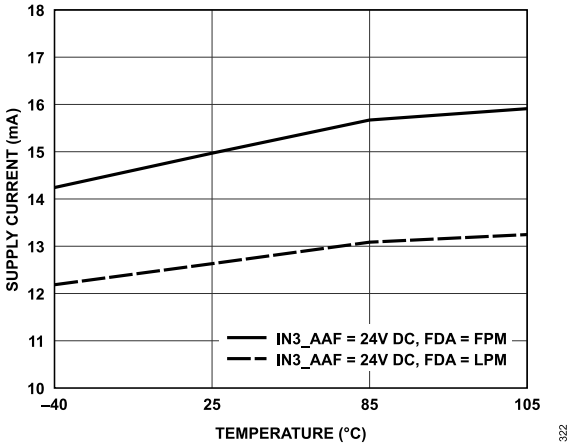

Figure 121. LDO Supply Current vs. Temperature, DC Input, OUT_LDO connected to VDD_FDA, VDD_ADC, and VDD2_ADC

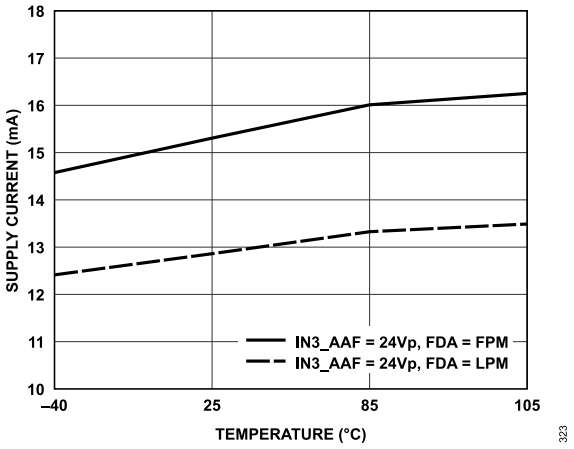

Figure 122. LDO Supply Current vs. Temperature, AC Input, OUT_LDO connected to VDD_FDA, VDD_ADC, and VDD2_ADC

TERMINOLOGY

Total Gain

The combined gain due to the PGA and AAF.

$$TOTAL\_GAIN = PGA\_GAIN \times AAF\_GAIN \quad (1)$$

Least Significant Bit (LSB)

The smallest increment that can be represented by a converter. For an ADC with N bits of resolution, the LSB expressed in volts is:

$$LSB\ (V) = \frac{V_{REF} \times 2}{2^N \times PGA\_GAIN \times AAF\_GAIN} \quad (2)$$

AC Common-Mode Rejection Ratio (CMRR)

The ratio of the sine wave, common-mode voltage applied to IN at frequency, f, to the voltage at the ADC output at the same frequency, f.

$$CMRR\ (dB) = 20log\left(\frac{V_{IN\_f} \times TOTAL\_GAIN}{V_{ADC\_f}}\right) \quad (3)$$

where:
V_{IN_f} is the sine wave, common-mode voltage applied to IN at frequency, f.
TOTAL_GAIN is the combined gain due to the PGA and AAF.
V_{ADC_f} is the voltage at the ADC output at the same frequency, f.

Gain Error

The first transition (from 100 … 000 to 100 …001) occurs at a level ½LSB more than nominal negative full scale (−4.0955999756V for the ±4.096V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½LSB less than the nominal full scale (+4.095999268V for the ±4.096V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift

The ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million per degree Celsius.

Offset Error

The difference between the ideal midscale input voltage (0V) and actual voltage producing the midscale output code.

Offset Error Drift

The ratio of the offset error change due to a temperature change of 1°C and the full-scale code range (2^N).

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1LSB apart. DNL is the maximum deviation from this ideal value, often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error

The deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½LSB before the first code transition. Positive full scale is defined as a level 1½LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range (DR)

The ratio of the root-mean-square (RMS) value of the linear voltage range to the input referred RMS noise measured when the IN pin is shorted to ground, using the same PGA_GAIN and AAF_GAIN. The value is expressed in decibels.

$$DR = 20 \times \log_{10}\left(\frac{Linear\ Input\ Range\ (RMS)}{RMS\ Noise}\right) \quad (4)$$

where:

$$Linear\ Input\ Range\ (RMS) = \frac{Vpp}{2\sqrt{2}} \quad (5)$$

Total System Dynamic Range

The ratio of the RMS value of the linear voltage range at PGA_GAIN = 1, to the input referred RMS noise measured at PGA_GAIN = 128 when the IN pin is shorted to ground, using the same AAF_GAIN. The value is expressed in decibels.

Peak-to-Peak Resolution

The number of bits unaffected by peak-to-peak noise or flicker. It is also sometimes called flicker-free resolution or noise-free code resolution. It follows this formula:

$$\log_2\left(\frac{Linear\ Input\ Range\ (Vpp)}{6.6 \times Low\ Frequency\ Noise\ (RMS)}\right) \quad (6)$$

Signal-to-Noise Ratio (SNR)

The ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components less than the Nyquist frequency, excluding harmonics and DC. The value is expressed in decibels.

Total Harmonic Distortion (THD)

The ratio of the RMS sum of the harmonics to the fundamental. THD is expressed in decibels. For the ADAQ7769-1, THD is defined as:

$$THD\ (dB) = 20log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}\right) \quad (7)$$

where:
V_2, V_3, V_4, V_5, and V_6 are the RMS amplitudes of the second to sixth harmonics.
V_1 is the RMS amplitude of the fundamental.

TERMINOLOGY

Signal-to-Noise and Distortion (SINAD) Ratio

The ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components less than the Nyquist frequency, including harmonics but excluding DC. The value is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

The difference, in decibels, between the RMS amplitude of the input signal and peak spurious signal (including harmonics).

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa and nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the RMS sum of the individual distortion products to the RMS amplitude of the sum of the fundamentals expressed in decibels.

Device-to-Device Phase Angle Mismatch

The device-to-device phase angle mismatch measures the deviation of the phase delay of a single ADAQ7769-1 device relative to the average phase delay of a group of ADAQ7769-1 devices at a given input signal frequency. The mismatch also shows how well the phase response of the data acquisition signal chain matches among channels. The typical specification is equal to ±1σ (standard deviation) of the distribution, while the maximum (or minimum) is four times this value.

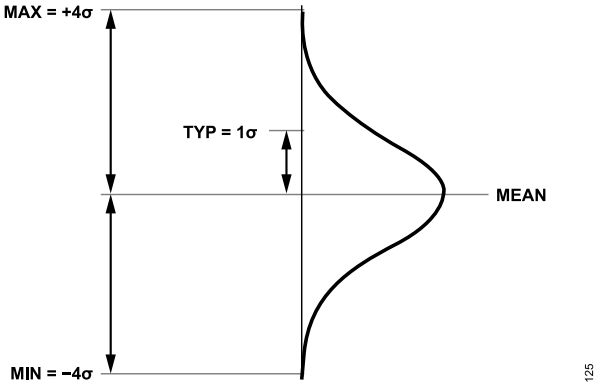

Figure 124. Device-to-Device Phase Angle Mismatch Calculation

Device-to-Device Phase Angle Mismatch Drift

It quantifies how much the device-to-device phase angle mismatch standard deviation (σ) widens/tightens across temperature at a given input signal frequency. A positive sign indicates a wider phase mismatch distribution as temperature increases, while a negative sign indicates a tighter phase mismatch distribution as temperature increases. This specification is calculated using the endpoint method over the full-operating temperature range. The typical specification is the change in |1σ| per °C, while the maximum is four times this value, as shown in Figure 125.

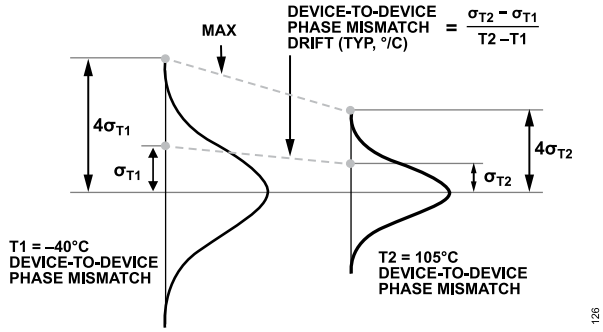

Figure 125. Device-to-Device Phase Angle Mismatch Drift Calculation

Power-Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

THEORY OF OPERATION

ANALOG INPUT

The wide and flexible input range of the ADAQ7769-1 accepts single-ended unipolar inputs such as from 0V to +24V or 0V to −24 V, or single-ended bipolar inputs ±16V applied to the IN pin, as shown in Figure 126. This shift of input range can be achieved by changing the VDD_PGA and VSS_PGA supplies, as shown in Figure 130 and Figure 131.

For smaller input signals, the eight programmable binary gain settings of the PGA and 3-pin selectable gain settings of the AAF offer additional system dynamic range. This makes ADAQ7769-1 a suitable DAQ solution for systems with varying sensors of different amplitudes.

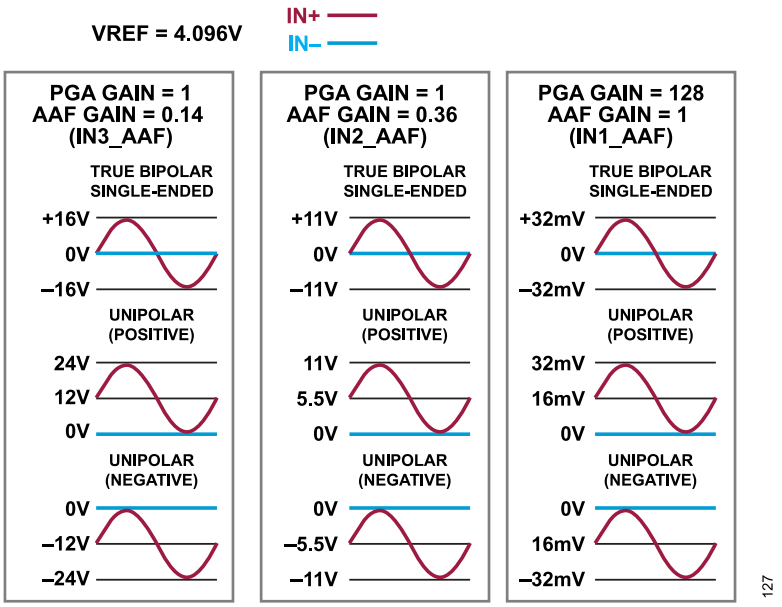

Figure 126. Examples of Different Input Signals

THEORY OF OPERATION

PGA Absolute Input Range

The ADAQ7769-1 absolute input range applied to the IN pin is limited to its supply voltages VDD_PGA and VSS_PGA.

AAF Input

The AAF stage is a network containing a fully-differential amplifier (FDA). As part of the ADAQ7769-1, one function of the AAF stage is to convert the single-ended signal coming from the PGA into a differential signal entering the differential ADC.

The ADAQ7769-1 presents the option to bypass the PGA stage and apply the input directly to the AAF, as shown in Figure 127. When bypassing the PGA and applying the input directly to any of the INx_AAF pins, the input can be single-ended, pseudo-differential, or differential.

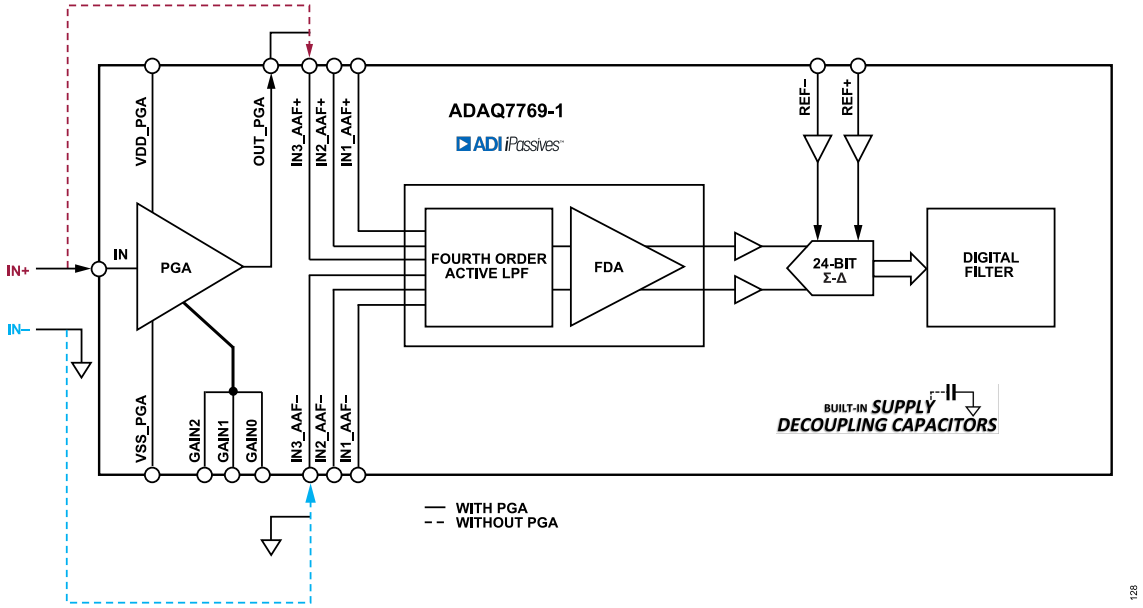

Figure 127. Option to Bypass the PGA

THEORY OF OPERATION

AAF Absolute Input Range

The absolute voltage that the AAF pins accept varies between the input pairs. For IN1_AAF+/− and IN2_AAF+/−, the absolute maximum input is at ±15V. For IN3_AAF+/−, the absolute maximum is at ±36V.

AAF Differential Input Range

The three AAF input pairs are differential, which means that the input signal which causes a swing to the ADC is the difference between the AAF input pairs, not the instantaneous voltage on individual pins.

The differential signal amplitude depends on the AAF_GAIN and the reference voltage level. The maximum differential input voltage can be calculated by:

$$V_{INx\_AAF+} - V_{INx\_AAF-} = \frac{\pm V_{REF}}{AAF\_GAIN} \quad (8)$$

where V_{INx_AAF+} is the INx_AAF+ voltage, and V_{INx_AAF-} is the INx_AAF− voltage.

AAF Common-Mode Input Range

The common-mode input signal (VICM) is the average of the absolute voltage across a particular pair of differential inputs, given by the formula:

$$V_{ICM} = \frac{V_{INx\_AAF+} + V_{INx\_AAF-}}{2} \quad (9)$$

The input signal common-mode range depends on the driver amplifier supply voltage (VDD_FDA) and the selected AAF input pair. To simplify selection of input pins, Table 11 lists maximum differential input range and common-mode input range for each of the AAF input pairs.

Operating within the linear input range for the PGA input (see Specifications) automatically satisfies the AAF common-mode input range. For example, applying +24V to the IN pin, setting the PGA_GAIN to 1, connecting OUT_PGA to IN3_AAF+, and IN3_AAF− to AGND, the resulting V_{ICM} between IN3_AAF+ and IN3_AAF− is:

$$V_{ICM} = \frac{24 \times 1 + 0}{2} = 12V \quad (10)$$

Table 11. AAF Differential and Common-Mode Input Ranges

AAF Input Pin	Gain (V/V)	AAF Differential Input Range with V_{REF} = 4.096V (V)	AAF Common-Mode Input Range with V_{REF} = 4.096V	
			Min (V)	Max (V)
IN1_AAF+/−	1	±4.096	−2.1	+4.5
IN2_AAF+/−	0.364	±11.264	−6.1	+6.2
IN3_AAF+/−	0.143	±28.672	−16	+12

Input Swings and Operating Regions

Figure 128 to Figure 131 show the relative scaling between the voltage at PGA output pin (OUT_PGA), connected to different AAF input pairs, and the respective 24-bit, twos complement digital outputs, expressed as hexadecimal codes. OUT_PGA is simply the product of the input to IN and the PGA_GAIN, given that there is sufficient supply headroom to avoid input or output clipping. Figure 128 shows the relative scaling using IN1_AAF and IN2_AAF, while Figure 129 to Figure 131 show the different operating regions using IN3_AAF and varying PGA supply voltages.

THEORY OF OPERATION

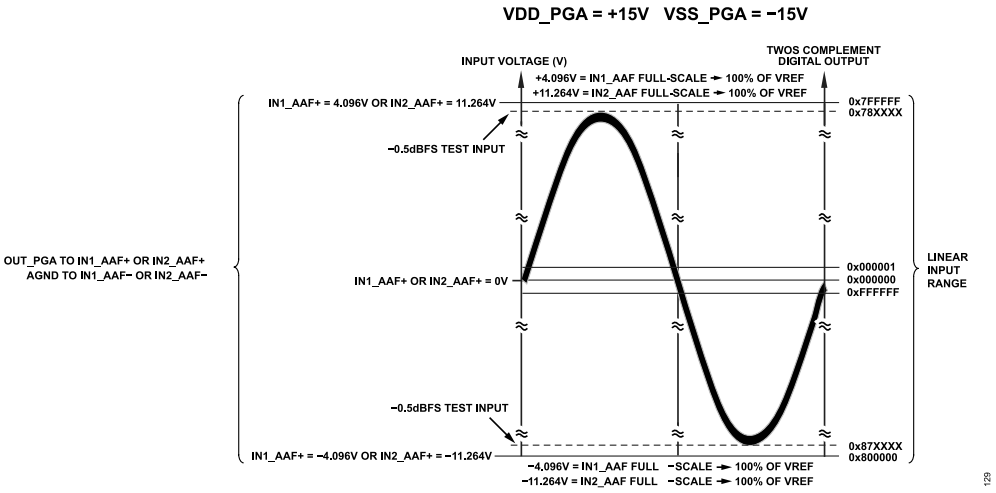

Figure 128. Detailed Input Voltage to ADC Output Code Conversion using IN1_AAF and IN2_AAF

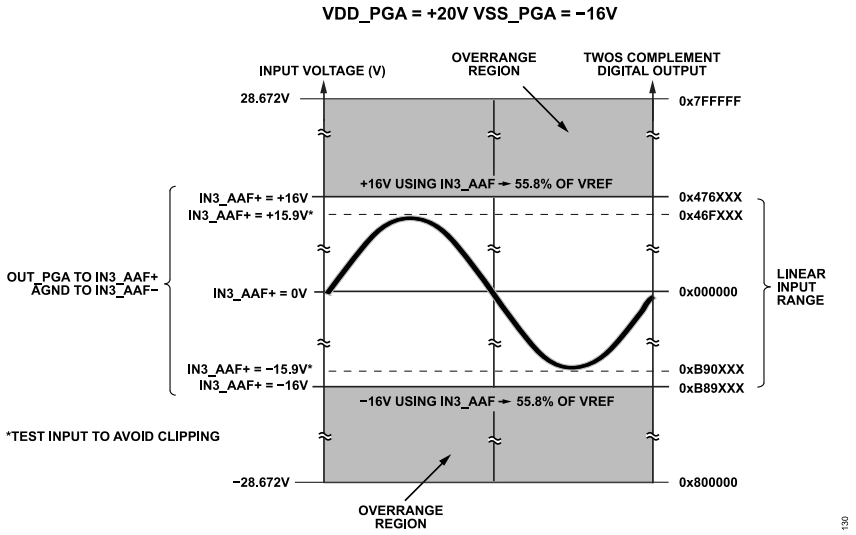

Figure 129. Detailed Bipolar Input Voltage to ADC Output Code Conversion using IN3_AAF

THEORY OF OPERATION

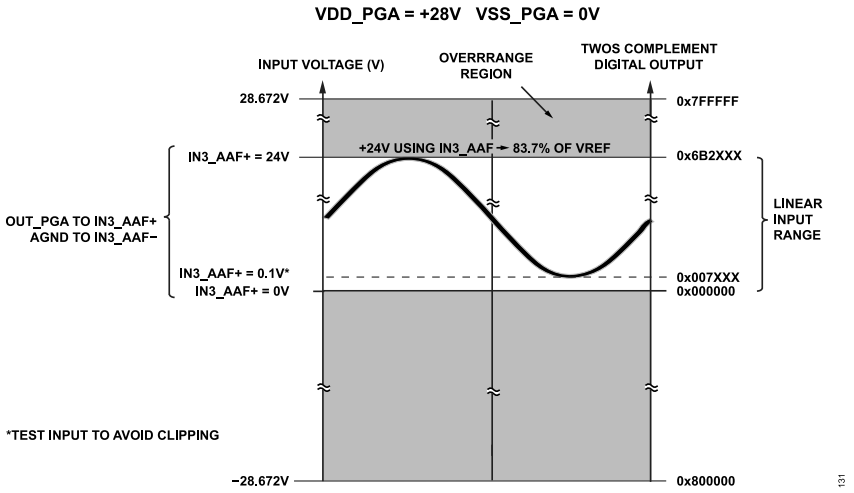

Figure 130. Detailed Positive Unipolar Input Voltage to ADC Output Code Conversion using IN3_AAF

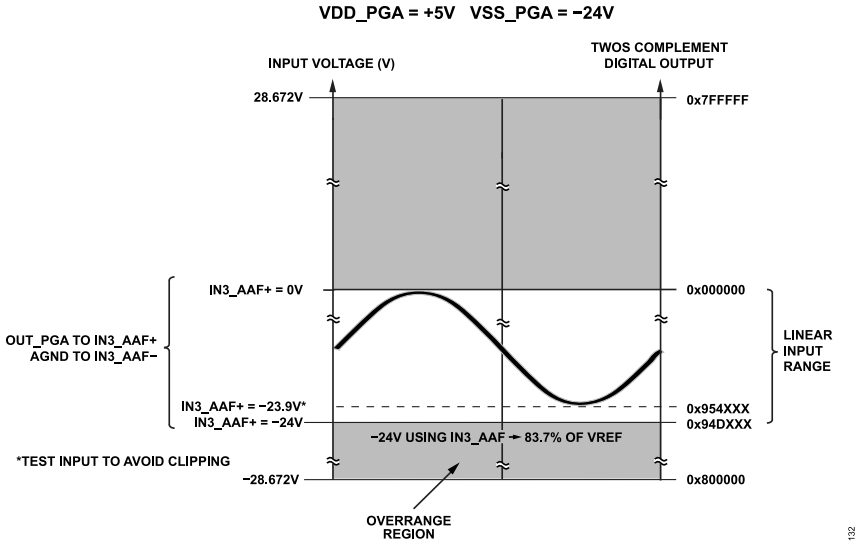

Figure 131. Detailed Negative Unipolar Input Voltage to ADC Output Code Conversion using IN3_AAF

THEORY OF OPERATION

Input Range Selection

To simplify selection of PGA_GAIN and AAF_GAIN, Table 12, Table 13, and Table 14 list the linear input range for each combination of gain settings. For Table 14, the linear input range using IN3_AAF is split into bipolar and unipolar ranges since the ranges are limited by the PGA supplies and the PGA common-mode input range.

Table 12. Input Range Selection using IN1_AAF (V_{REF} = 4.096V)

GAIN2 Pin Logic	GAIN1 Pin Logic	GAIN0 Pin Logic	PGA_GAIN (V/V)	AAF_GAIN (V/V)	TOTAL_GAIN (V/V)	Linear Input Range (V)
L	L	L	1	1	1	±4.096
L	L	H	2	1	2	±2.048
L	H	L	4	1	4	±1.024
L	H	H	8	1	8	±0.512
H	L	L	16	1	16	±0.256
H	L	H	32	1	32	±0.128
H	H	L	64	1	64	±0.064
H	H	H	128	1	128	±0.032

Table 13. Input Range Selection using IN2_AAF (V_{REF} = 4.096V)

GAIN2 Pin Logic	GAIN1 Pin Logic	GAIN0 Pin Logic	PGA_GAIN (V/V)	AAF_GAIN (V/V)	TOTAL_GAIN (V/V)	Linear Input Range (V)
L	L	L	1	0.364	0.364	±11.264
L	L	H	2	0.364	0.727	±5.632
L	H	L	4	0.364	1.455	±2.816
L	H	H	8	0.364	2.909	±1.408
H	L	L	16	0.364	5.818	±0.704
H	L	H	32	0.364	11.636	±0.352
H	H	L	64	0.364	23.273	±0.176
H	H	H	128	0.364	46.545	±0.088

Table 14. Input Range Selection using IN3_AAF (V_{REF} = 4.096V)

GAIN2 Pin Logic	GAIN1 Pin Logic	GAIN0 Pin Logic	PGA_GAIN (V/V)	AAF_GAIN (V/V)	TOTAL_GAIN (V/V)	Bipolar Linear Input Range (V)[1]	Unipolar Positive Linear Input Range (V)[2]	Unipolar Negative Linear Input Range (V)[3]
L	L	L	1	0.143	0.143	±16	0 to +24	0 to −24
L	L	H	2	0.143	0.286	±8	0 to +12	0 to −12
L	H	L	4	0.143	0.571	±4	0 to +6	0 to −6
L	H	H	8	0.143	1.143	±2	0 to +3	0 to −3
H	L	L	16	0.143	2.286	±1	0 to +1.5	0 to −1.5
H	L	H	32	0.143	4.571	±0.5	0 to +0.75	0 to −0.75
H	H	L	64	0.143	9.143	±0.25	0 to +0.375	0 to −0.375
H	H	H	128	0.143	18.286	±0.125	0 to +0.1875	0 to −0.1875

[1] VDD_PGA = 20V, VSS_PGA = −16V.

[2] Positive Unipolar (VDD_PGA = +28V, VSS_PGA = 0V).

[3] Negative Unipolar (VDD_PGA = +5V, VSS_PGA = −24V).

THEORY OF OPERATION

ANTI-ALIASING FILTER (AAF)

The input signal bandwidth of the ADAQ7769-1 is dominated by its digital filter. The user can program the decimation ratio to adjust the digital filter bandwidth. The filter bandwidth can also be fine-tuned by changing the MCLK frequency. For example, with the wideband low-ripple digital filter option and an ODR = 256kSPS, the −3dB bandwidth of the overall signal chain is equal to the digital filter bandwidth of $f_{3\ dB}$ = 0.433 × ODR = 110.85kHz. The same filter has a stop band of 0.499 × ODR and a minimum stop band attenuation of −105dB.

As with any discrete-time Σ-Δ ADC, the digital filter of the ADAQ7769-1 does not offer rejection to signals around the signal sampling frequency, f_S. The core ADC samples of the ADAQ7769-1 are at a frequency of 2 × f_{MOD}. In normal operating mode with f_{MOD} = MCLK/2, the f_S of the ADC is equal to MCLK. The digital filter has no rejection to signals within the $f_S \pm f_{3dB}$ frequency range, which allows noise and interference in this frequency range to fold in the pass band. As shown in Figure 132, an additional analog AAF is required to reject signals around f_S to prevent out-of-band signals from folding back to the band of interest.

The digital filter has no rejection to signals within frequency range of $f_S \pm f_{3dB}$. The ADAQ7769-1's core ADC samples at a frequency of 2 × f_{MOD}. In normal operating mode with f_{MOD} = MCLK/2, the ADC's sampling frequency f_S is equal to MCLK.

The ADAQ7769-1 features a fourth-order analog AAF that is designed to achieve greater than 65dB of rejection at 16.384MHz for all input pairs. Combining its analog AAF with its wideband low-ripple FIR filter, the ADAQ7769-1 is able to reject all out-of-band signals by a minimum of 90dB, as shown in Figure 132.

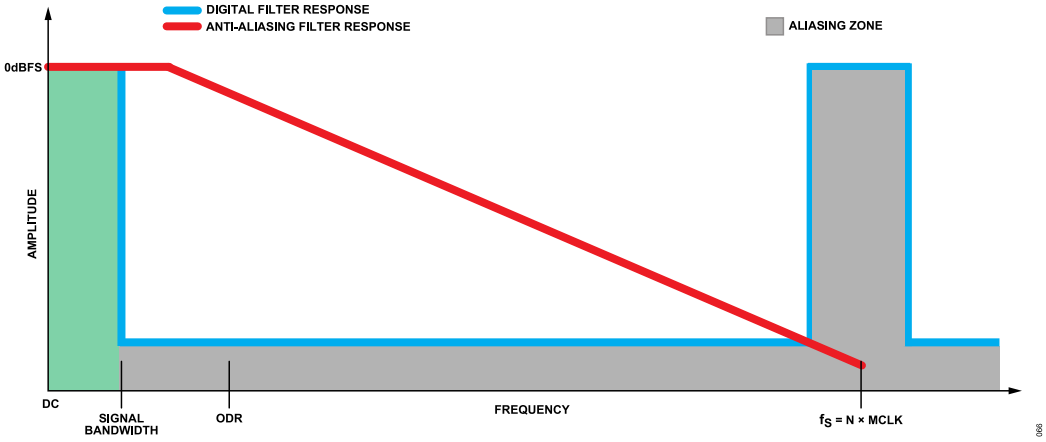

Figure 132. Simplified Illustration of AAF Requirement for Discrete-Time Oversampled Converters

THEORY OF OPERATION

Magnitude and Phase Response

The AAF is designed to achieve optimal aliasing rejection level with minimum magnitude and phase distortion to the in-band signal. As shown in Figure 36, the phase response of the filter in the pass band is highly linear. With the help of Analog Devices, Inc., iPassives technology, the filter has a tightly controlled −3dB corner, which allow for a minimal device-to-device phase angle mismatch, as shown in Figure 38 to Figure 40. This performance is highly required in simultaneously sampling applications, such as using three accelerometers for the x, y, and z axes to locate faults in machine health monitoring applications. These applications can be challenging and expensive to achieve in signal chains using discrete resistors and capacitors, which vary with respect to their tolerance and temperature drift behavior, which make this performance a key advantage of signal chain µModules.

Table 15. PGA + Analog AAF Profile

PGA_GAIN	AAF_GAIN	Analog Filter −3dB Bandwidth (kHz)	Relative to DC Attenuation at MCLK = 16.384MHz (dB)	DC to 100kHz Pass-Band Droop (mdB)	Change in Group Delay from DC to 100kHz (ns)
1	1	358.2	90	+50	59
1	0.364	299.3	90	−10	84
1	0.143	278.1	90	−80	88

THEORY OF OPERATION

Calculations on AFE Phase Performance

All mismatches on the phase angle across gain or temperature, or from device-to-device are due to the AFE, as the group delay of the digital filter is constant. The AFE includes the PGA, FDA, and its analog filters.

Phase Angle Over Frequency

The ADAQ7769-1 has a linear phase response. To interpolate the phase delay from one frequency to another, the ideal formula is:

$$\frac{\theta_1}{f_{IN\_1}} = \frac{\theta_2}{f_{IN\_2}} \quad (11)$$

where θ_x is the phase delay of the AFE using an input frequency of f_{IN_x}.

However, due to small nonlinearities, calibrate the formula in terms of its slope and intercept:

$$\theta = m \times f_{IN} + b + Nonlinearity \quad (12)$$

where:
m is the slope.
b is the y-intercept of the linear equation of the phase delay with respect to the input frequency over the span of the pass-band frequency using endpoint method, as shown in Figure 35.

Using the phase delay at 100Hz to 110kHz as endpoints, a typical device has a worst nonlinearity of approximately –0.4° to +3.0°, which depends on the input range, as shown in Figure 36 and Figure 37.

Phase Angle Drift

A phase angle drift defines the rate of change of the phase delay over temperature of a single device at a given input signal frequency. The drift in degrees/°C is calculated using the endpoint method over the full-operating temperature range of −40°C and 105°C. The typical specification is the average phase angle drift across a large number of devices, while the maximum (or minimum) specification is four standard deviations (σ) away from the typical value.

For example, typical Device A has a 5.8° phase delay from input to output at 20kHz at T_A = 25°C using PGA_GAIN = 1, IN1_AAF. At T_A = 105°C, the same Device A typically has:

5.8° + 0.00020°/°C (*Typical Specification*) × (105°C – 25°C) = 5.816° phase delay.

If a Device B is operating on the maximum phase angle drift specifications, then the same Device B typically has:

5.8° + 0.00026°/°C (*Maximum Specification*) × (105°C – 25°C) = 5.8208° phase delay.

Phase Angle Mismatch Over PGA Gain

The phase angle mismatch over PGA gain is the phase delay of PGA_GAIN = 2 to 128 relative to its phase delay at PGA_GAIN = 1 of the same device and AAF_GAIN. The typical specification is the average phase angle mismatch over PGA gain across a large number of devices, while the maximum (or minimum) specification is four standard deviations (σ) away from the typical value.

For example, typical Device A using IN1_AAF has 5.8° phase delay from input to output at 20kHz on PGA_GAIN = 1. On PGA_GAIN = 128, the same Device A typically has:

5.8° + 9.336° (*Typical Specification*) = 15.136° phase delay.

If a Device B is operating on the maximum phase angle mismatch over PGA gain specifications, then, on PGA_GAIN = 128, the same Device B has:

5.8° + 9.804° (*Maximum Specification*) = 15.604° phase delay.

Device-to-Device Phase Angle Mismatch

Device-to-device phase angle mismatch measures the deviation of the phase delay of a single ADAQ7769-1 device relative to the average phase delay of a group of ADAQ7769-1 devices at a given input signal frequency (see Figure 124). The mismatch shows how well the phase response of the data-acquisition signal chain matches between channels. The typical specification is equal to ±1σ (standard deviation) of the distribution, while the maximum (or minimum) is four times this value.

For example, measuring the phase delay of a large number of devices with 20kHz input using PGA_GAIN = 1, IN1_AAF, Device C has a phase delay on the minimum side of the distribution, which is (−) 0.038° earlier than the average. Again, Device D has a phase delay on the maximum side of the distribution, which is (+) 0.038° later than the average. The phase angle mismatch between Device C and Device D is:

+0.038° (max) – (−) 0.038° (min) = 0.076°

This is the worst-case phase angle mismatch between any two ADAQ7769-1 devices (using PGA_GAIN = 1, IN1_AAF, T_A = 25°C, 20kHz input).

Device-to-Device Phase Angle Mismatch Drift

Device-to-device phase angle mismatch drift quantifies how much the device-to-device phase angle mismatch standard deviation (σ) widens or tightens across temperature at a given input signal frequency. A positive sign indicates a wider phase mismatch distribution as temperature increases, while a negative sign indicates a tighter phase mismatch distribution as temperature increases. This specification is calculated using the endpoint method over the full-operating temperature range of −40°C and +105°C. The typical specification is the change in 1σ per °C, while the maximum is four times this value, as shown in Figure 125.

Measuring the device-to-device phase angle mismatch standard deviation (σ) of a large number of devices at 25°C with 20kHz input using PGA_GAIN = 1, IN1_AAF, it is observed that the σ of

THEORY OF OPERATION

the distribution is 0.013°. To interpolate the standard deviation at another temperature, use the following:

$\sigma_{T2} = \sigma_{T1} + \textit{Device-to-Device Phase Angle Mismatch Drift} \times (T_2 - T_1)$

For example, $\sigma_{-40°C} = 0.013° + (0.2\mu°/°C) \times (-40°C - 25°C) = 0.012987°$

FULLY-DIFFERENTIAL AMPLIFIER (FDA) POWER MODE

The FDA of the ADAQ7769-1 is a low noise, low distortion amplifier that can drive high resolution and high performance, Σ-Δ ADCs.

The FDA two selectable power modes are low-power mode and full-power mode. The FDA low-power mode is ideal for DC input applications due to its low 1/f noise. The full-power mode offers better linearity performance at a higher current consumption.

Figure 133 shows the connection between M0_FDA, M1_FDA, M0_ADC, and M1_ADC. The connection sets the FDA to full-power mode. To set the FDA to low-power mode, M0_FDA must be pulled to ground, while keeping M1_FDA and M1_ADC connected, as shown in Figure 134.

To conserve power when the ADC is in power-down mode or in standby mode, the FDA must be put on standby by pulling both M0_FDA and M1_FDA to ground. This is automatically done when M0_FDA and M1_FDA is connected to M0_ADC and M1_ADC. See Table 16.

Table 16. FDA Mode Truth Table

ADC Mode	Is M0/M1_FDA Connected to M0/M1_ADC?	M0_FDA Input Logic	M1_FDA Input Logic	FDA Mode
Fast[1]	Yes	M0_ADC = High	M1_ADC = High	Full-power mode
Median	Yes	M0_ADC = Low	M1_ADC = High	Low-power mode
Low	Yes	M0_ADC = Low	M1_ADC = Low	Standby
Standby	Yes	M0_ADC = Low	M1_ADC = Low	Standby
Power-Down	Yes	M0_ADC = Low	M1_ADC = Low	Standby

[1] In continuous conversion and one-shot conversion modes, the ADC is always active. In single conversion and duty-cycled conversion modes, the ADC alternates between active and standby states. For more details, see the Data Conversion Modes section.

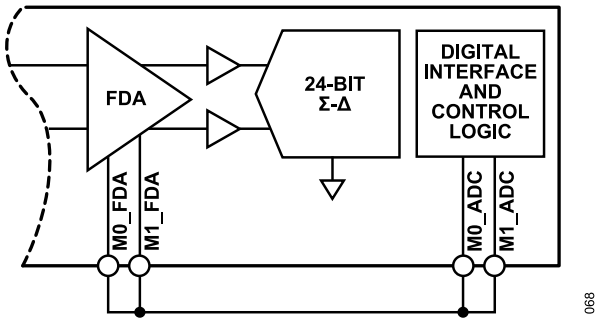

Figure 133. FDA Full-Power Mode Connection

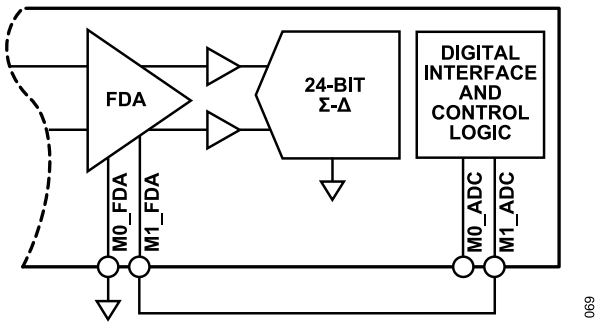

Figure 134. FDA Low-Power Mode Connection

LINEARITY BOOST BUFFER

The ADAQ7769-1 has a pair of linearity boost buffers placed between the driver amplifier and core ADC. There is the option to turn the buffers on to boost the linearity performance of the device. The linearity boost buffers add no noise to the signal chain performance and consume an additional 2mA typical current (as a pair) on the VDD_ADC supply.

The linearity boost buffers are enabled by default. Turn the buffers off in SPI control mode by setting the LINEARITY_BOOST_A_OFF and LINEARITY_BOOST_B_OFF bits in the Analog Buffer Control Register section (Register 0x16, Bit 1 and Bit 2, respectively) to 0. The linearity buffers are always enabled in $\overline{\text{PIN}}$ control mode.

REFERENCE INPUT AND BUFFERING

The ADAQ7769-1 has differential reference inputs, REF+ and REF−. The absolute input reference voltage range is from 1V to VDD_ADC − AGND.

The reference inputs can be configured for a fully buffered input on each of the REF+ and REF− pins, a precharge buffered input, or to bypass both buffers.

Use of either the full buffers or the precharge buffers reduce the burden on the external reference when driving large loads or multiple devices. The fully buffered input to the reference pins provides a high-impedance input node and enables the use of the ADAQ7769-1 in ratiometric applications, where the ultra-low source impedance of a traditional external reference is not available.

THEORY OF OPERATION

In $\overline{\text{PIN}}$ control mode, the reference precharge buffers are on by default. In SPI mode, there is a choice of either fully buffered or precharge buffers.

The reference input current scales linearly with the modulator clock rate.

For MCLK = 16.384MHz in fast mode, the reference input current is ~80µA/V unbuffered and ~20µA with the precharge buffers enabled.

With the precharge buffers off, REF+ = 5V and REF− = 0V.

REF± = 5V × 80µA/V = +400µA

With the precharge buffers on, REF+ = 5V, and REF− = 0V.

REF± = approximately 20µA

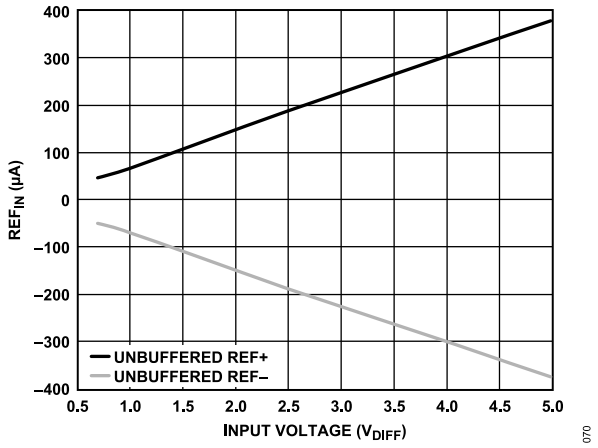

Figure 135. Reference Input Current (REF_{IN}) vs. Input Voltage, Unbuffered REF+ and REF−

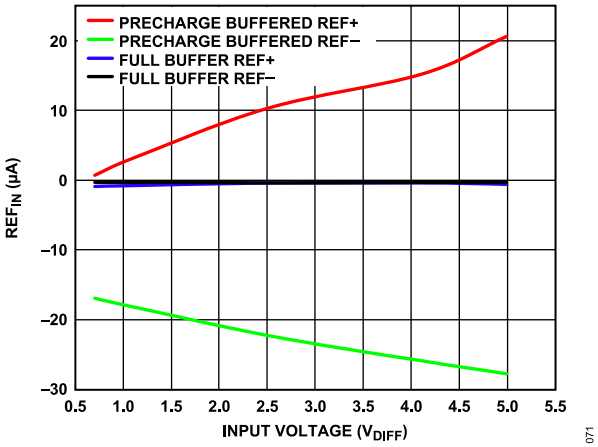

Figure 136. Reference Input Current (REF_{IN}) vs. Input Voltage, Precharge Buffered REF+ and REF− and Full Buffer REF+ and REF−

For the best performance and headroom, use a 4.096V reference, such as the ADR444 or ADR4540, which can both be supplied by a 5V rail and shared to the VDD_ADC supply.

A reference detect function is available in SPI control mode. For more details, see the SPI Mode Diagnostic Features section.

CORE CONVERTER

The ADAQ7769-1 can use up to a 5V reference and convert the differential voltage between any input pair to a digital output. The 24-bit conversion result is in MSB first, twos complement format. Figure 137 shows the ideal transfer function, and Table 17 lists the ideal input voltages and their output codes.

Use the following equation to convert from codes to volts, assuming the codes are first converted from twos complement to straight binary:

$$Voltage = \frac{(Code - Midscale\ Code) \times 2 \times V_{REF}}{2^{24} \times TOTAL\_GAIN} \quad (13)$$

where the midscale code is 0x800000 in straight binary and 0x7FFFFF in Table 17 is converted to 0xFFFFFF in straight binary. Use the Equation 13 to calculate the input voltage in the V_{REF}/TOTAL_GAIN range, assuming the signal is not clipped and is within the linear input range, as shown in Input Swings and Operating Regions section.

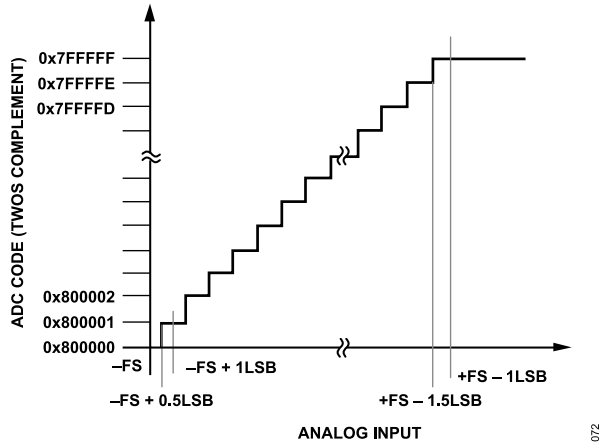

Figure 137. Ideal Transfer Function (FS is Full-Scale)

Table 17. Ideal Input Voltages and Output Codes

Description	Analog Input (V), IN1_AAF AAF_GAIN = 1, IN2_AAF AAF_GAIN = 4/11, and IN3_AAF AAF_GAIN = 1/7	Digital Output Code, 2s Complement (Hexadecimal)
FS − 1LSB	$+V_{REF}$/ TOTAL_GAIN × (1 − $1/2^{23}$)	0x7FFFFF
Midscale + 1LSB	$+V_{REF}$/ TOTAL_GAIN/2^{23}	0x000001
Midscale	0	0x000000
Midscale − 1LSB	$-V_{REF}$/ TOTAL_GAIN/2^{23}	0xFFFFFF
−FS + 1LSB	$-V_{REF}$/ TOTAL_GAIN × (1 − $1/2^{23}$)	0x800001
−FS	$-V_{REF}$/ TOTAL_GAIN	0x800000

THEORY OF OPERATION

POWER SUPPLIES

The ADAQ7769-1 has several supply pins, which may be connected to the internal LDO to simplify connections.

The internal LDO may be used with an input ranging from 5.1V to 5.5V to regulate an output of 5V for the use of pins VDD_FDA, VDD_ADC, VDD2_ADC, and the external reference such as ADR4540, as shown in Figure 138. For proper operation, it is recommended to use a 1µF capacitor at the input and output of the LDO. Figure 139 shows the use of an external power supply for VDD_FDA, VDD_ADC, VDD2_ADC, and the reference if the internal LDO is not preferred.

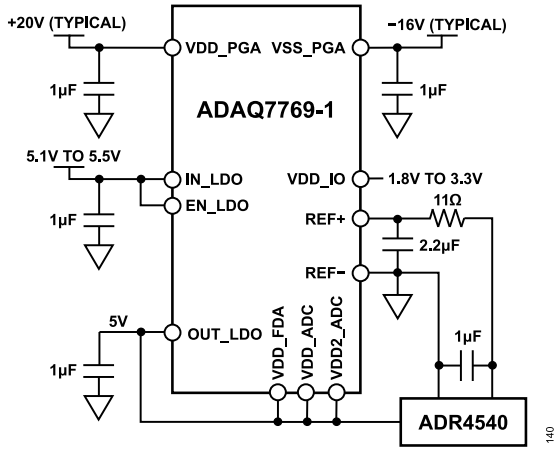

Figure 138. ADAQ7769-1 Power Supply Connection using Internal LDO

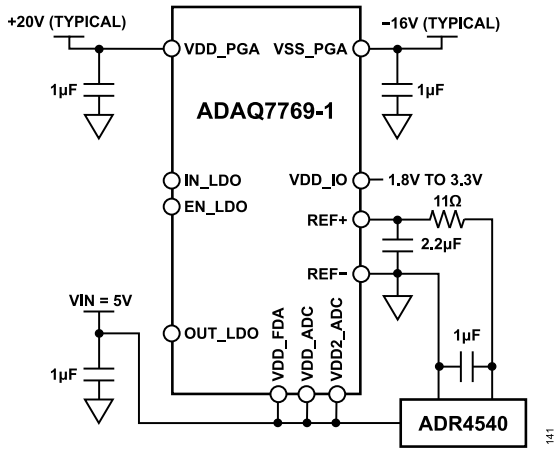

Figure 139. ADAQ7769-1 Power Supply Connection using External 5V Supply

The VDD_PGA and VSS_PGA supplies power to the input and output stage of the PGA.

The VDD_FDA supply powers the ADC driver.

The VDD_ADC supply powers the linearity boost buffer, core ADC front-end, and reference input.

The VDD2_ADC supply connects to an internal 1.8V analog LDO regulator. This regulator powers the ADC core. VDD2_ADC − AGND can range from 5.5V (maximum) to 2.0V (minimum). In applications requiring less power consumption, VDD2_ADC is recommended to be separately powered with a well-regulated 2.5V supply. With a typical current consumption of 4.7mA, this conserves 11.75mW compared to using the 5V from the internal LDO or an external 5V power supply.

VDD_IO powers the internal 1.8V digital LDO regulator. This regulator powers the digital logic of the ADC. VDD_IO sets the voltage levels for the SPI interface of the ADC. VDD_IO is referenced to DGND, and VDD_IO − DGND can vary from 3.6V (maximum) to 1.7V (minimum), but it requires a minimum of 2.5V when the GPIOs are used to control the PGA's GAIN pins in SPI mode.

POWER SUPPLY DECOUPLING

The ADAQ7769-1 has built-in 0.1µF supply decoupling capacitors on the VDD_PGA, VSS_PGA, VDD_FDA, VDD_ADC, VDD_ADC2, and VDD_IO supply pins. Externally, the ADC's own analog and digital LDOs must be decoupled to the ground with a 1µF capacitor through pins AREG_CAP and DREG_CAP.

Figure 41 shows the AC PSRR of the internal 5V LDO while it is connected to VDD_FDA, VDD_ADC, and VDD_ADC2 with their internal 0.1µF supply decoupling capacitors and the recommended 1µF external decoupling capacitor at the OUT_LDO pin, as shown in Figure 138. Figure 42 to Figure 44 show the AC PSRR of VDD_PGA, VSS_PGA, and VDD_IO, respectively.

POWER STANDBY

Each functional block of the ADAQ7769-1 can be put into standby mode or power-down mode. The ADAQ7769-1 can achieve 0.65mW of total power consumption while all functional blocks are put into standby mode or power-down mode. For more details, see the Fully-Differential Amplifier (FDA) Power Mode, ADC Power-Down Mode, and ADC Standby Mode sections.

CLOCKING AND SAMPLING TREE

The ADAQ7769-1 core ADC receives a controller clock signal (MCLK). The MCLK signal can be sourced from one of four options: a CMOS clock, a crystal connected between the XTAL1 and XTAL2 pins, an LVDS signal, and the internal clock. The MCLK signal received by the ADAQ7769-1 defines the core Σ-Δ modulator clock rate (f_{MOD}) of the ADC and, in turn, the sampling frequency of the modulator of 2 × f_{MOD}.

$$f_{MOD} = \frac{MCLK}{MCLK\_DIV} \quad (14)$$

To determine f_{MOD}, select and set one of four clock divider settings: MCLK/2, MCLK/4, MCLK/8, or MCLK/16 from the MCLK_DIV bits (Register 0x15, Bits[5:4]) shown in the Power and Clock Control Register section. For example, to maximize the ODR or input bandwidth, a MCLK rate of 16.384MHz is required. Select an MCLK divider (MCLK_DIV) equal to 2 for a modulator frequency of 8.192MHz.

THEORY OF OPERATION

Control of the settings for the modulator frequency differ in $\overline{\text{PIN}}$ control mode vs. SPI control mode.

In SPI control mode, the user can program the power mode and MCLK_DIV independently. Independent selection of the power mode and MCLK_DIV allows full freedom in the MCLK speed selection to achieve a target modulator frequency, which can also result in a small power saving. For example, if the power mode is low power, it is more power efficient to use MCLK = 2.048MHz with MCLK_DIV = 2 than MCLK = 16.384MHz with MCLK_DIV = 16. Both options are valid selections and result in an f_{MOD} frequency of 1.024MHz. Table 18 gives a recommendation on setting the ADC power mode with respect to the f_{MOD} frequency.

Table 18. Recommended f_{MOD} Range for Each ADC Power Mode

Power Mode	Recommended f_{MOD} Range (MHz)
Low	0.038 to 1.024
Median	1.024 to 4.096
Fast	4.096 to 8.192

In $\overline{\text{PIN}}$ control mode, the MODEx pins determine the modulator frequency (see Table 28). The MODEx pins are also used to select the filter type and decimation rate.

It is recommended to keep the f_{MOD} frequency high to maximize the out of band tone rejection from the front-end AAF. Increase the decimation rate if low input bandwidth is required.

Power vs. Noise Performance Optimization

Depending on the bandwidth of interest for the measurement, the user can choose a strategy of either lowest current consumption or highest resolution. This choice is due to an overlap in the coverage of each power mode. There are different ways to achieve the same ODR. Using a lower MCLK frequency in tandem with a lower decimation rate allows the user to achieve the same data rate as using a higher MCLK frequency with a higher decimation. Lower power can be achieved by using lower modulator clock frequencies. Conversely, to achieve the highest resolution, use higher modulator clock frequencies and maximize the amount of oversampling.

CLOCKING AND CLOCK SELECTION

In SPI control mode, the ADAQ7769-1 has an internal oscillator that is used for the initial power-up of the device. After the ADAQ7769-1 completes the start-up routine, a clock handover occurs to the external MCLK. The ADAQ7769-1 counts the falling edges of the external MCLK over a given number of internal clock cycles to determine if the clock is valid and of a frequency of at least 600kHz. If there is a fault with the external MCLK, the handover does not occur, the ADAQ7769-1 clock error bit is set, and the ADAQ7769-1 continues to operate from the internal clock.

Four clock options are available in SPI mode: internal oscillator, external CMOS, crystal oscillator, or LVDS. Use the CLOCK_SEL bits (Register 0x15, Bits[7:6]) shown in the Power and Clock Control Register section to set the MCLK source. Regarding the MCLK pin polarity, the MCLK shown in the timing diagrams Figure 4 to Figure 8 are in-phase with the MCLK source applied to the XTAL2_MCLK pin when using an external CMOS clock or crystal oscillator, while the MCLK is in-phase with the XTAL1 pin when using an LVDS clock.

In $\overline{\text{PIN}}$ control mode, the CLK_SEL pin sets the external MCLK source. Two clock options are available in $\overline{\text{PIN}}$ control mode: an external CMOS, or a crystal oscillator. The CLK_SEL pin is sampled on power-up.

For both $\overline{\text{PIN}}$ and SPI mode, it is suggested to reset the device whenever the clock source is changed.

Set the EN_ERR_EXT_CLK_QUAL bit (Register 0x29, Bit 0 shown in the ADC Diagnostic Feature Control Register section) to turn off the clock qualification. Turning off the clock qualification allows the use of slower external MCLK rates outside the recommended MCLK frequency.

CLK_SEL Pin

If CLK_SEL = 0 in $\overline{\text{PIN}}$ control mode, the CMOS clock option is selected and must be applied to the XTAL2_MCLK pin. In this case, connect the XTAL1 pin to DGND. The connection is shown in Figure 140.

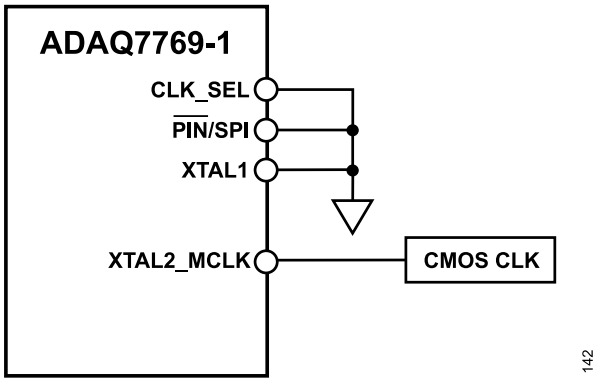

Figure 140. $\overline{\text{PIN}}$ Mode using an External CMOS Clock as MCLK

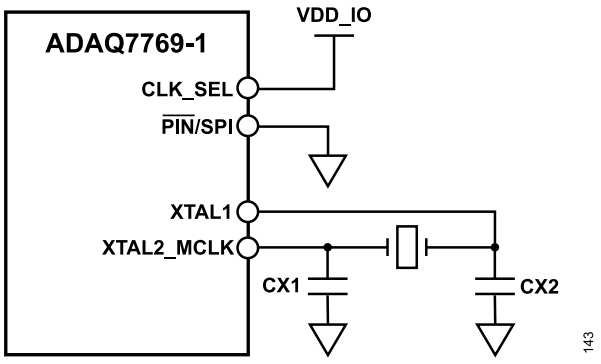

Figure 141. $\overline{\text{PIN}}$ Mode using an External Crystal as MCLK

THEORY OF OPERATION

If CLK_SEL = 1 in $\overline{\text{PIN}}$ control mode, the crystal option is selected and must be connected between the XTAL1 and XTAL2_MCLK pins, as shown in Figure 141. CX1 and CX2 are capacitors connected from each terminal of the crystal to DGND for circuit tuning. The values for these capacitors depend on the length and capacitance of the trace connections between the crystal and the XTAL1 and XTAL2_MCLK pins.

In SPI control mode, the CLK_SEL pin does not determine the MCLK source used and CLK_SEL must be connected to DGND.

Using the Internal Oscillator

In some cases, conversion using an internal clock oscillator may be preferred, such as in isolated applications where DC input voltages must be measured. Converting AC signals with the internal clock is not recommended because using the internal clock can result in degradation of SNR due to jitter.

DIGITAL FILTERING

The ADAQ7769-1 offers three types of digital filters. The digital filters available on the ADAQ7769-1 are the following:

- Wideband low-ripple FIR filter, −3dB at 0.433 × ODR (6 rates in SPI control mode).
- Sinc5, low latency filter, −3dB at 0.204 × ODR (8 rates in SPI control mode).
- Sinc3, low latency filter, –3dB at 0.2617 × ODR, widely programmable data rate in SPI control mode.

Decimation Rate Control

The ADAQ7769-1 has programmable decimation rates for the sinc and wideband low-ripple FIR digital filters, as shown in Table 19. The decimation rates allow the user to band limit the measurement, which reduces the speed and input bandwidth, but increases the resolution because there is further averaging in the digital filter. Control of the decimation rate on the ADAQ7769-1 when using SPI control is set in the Digital Filter and Decimation Control Register for the Sinc5 and wideband low ripple FIR filters.

The decimation rate of the Sinc3 filter is controlled using the SINC3 Decimation Rate (LSB) Register and the SINC3 Decimation Rate (MSB) Register. These registers combine to provide 13 bits of programmability. The decimation rate is set by incrementing the value in these registers by one and multiplying the value by 32. For example, setting a value of 0x5 in the SINC3 Decimation Rate (LSB) Register results in a decimation rate of 192 for the Sinc3 filter.

In $\overline{\text{PIN}}$ control mode, the MODE0 pin controls the decimation ratio. Only decimation rates of ×32 and ×64 are available for use with the Sinc5 and wideband filter options. For the full list of options available in $\overline{\text{PIN}}$ control mode, see Table 28.

Table 19. Decimation Rate Options

	Available Decimation Rates	
Filter Option	**SPI Control Mode**	**$\overline{\text{PIN}}$ Control Mode**
Wideband Low-Ripple FIR	×32, ×64, ×128, ×256, ×512, ×1024	×32, ×64
Sinc5	×8, ×16, ×32, ×64, ×128, ×256, ×512, ×1024	×8, ×32, ×64
Sinc3	Programmable decimation rate	50Hz and 60Hz output only, based on a 16.384MHz MCLK

THEORY OF OPERATION

Wideband Low-Ripple FIR Filter

The FIR filter is a low ripple, input pass band up to 0.433 × ODR. The wideband low-ripple FIR filter has almost full attenuation of 105dB at 0.5 × ODR (Nyquist), maximizing anti-alias protection. The frequency response of the wideband low-ripple FIR filter is shown in Figure 142. The wideband low-ripple FIR filter has a pass-band ripple of ±0.005dB, shown in Figure 143, and a stop-band attenuation of 105dB. The wideband low-ripple FIR filter is a 64-order digital filter. The group delay of the filter is 34/ODR. After a sync pulse, there is an additional delay from the $\overline{\text{SYNC\_IN}}$ rising edge to fully settled data. The time from a $\overline{\text{SYNC\_IN}}$ pulse to both the first $\overline{\text{DRDY}}$ and to fully settled data for various ODR values is shown in Table 20.

The wideband low-ripple FIR filter can be selected in one of six different decimation rates, which allows the user to choose the optimal input bandwidth and speed of the conversion vs. the required resolution.

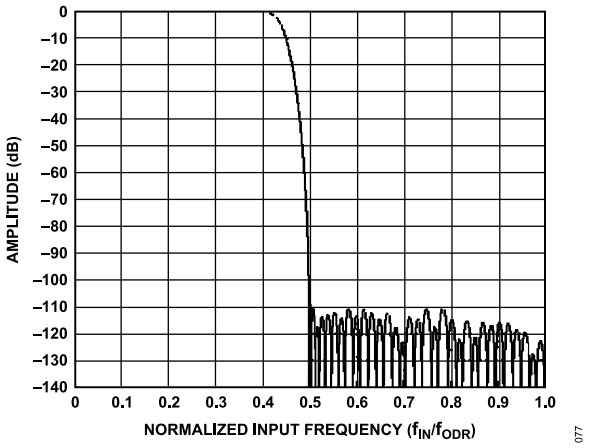

Figure 142. Wideband Low-Ripple FIR Filter Frequency Response

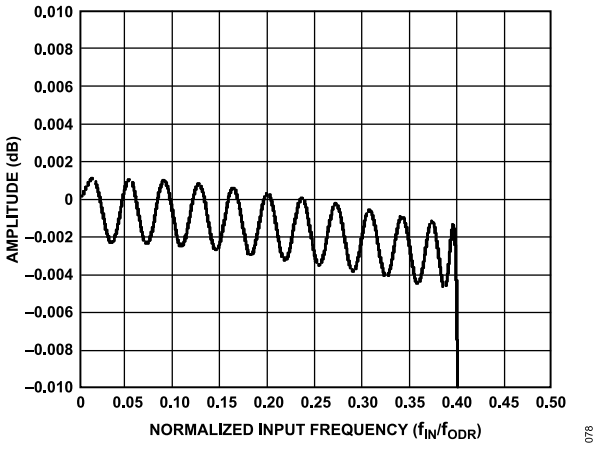

Figure 143. Wideband Low-Ripple FIR Filter Pass-Band Ripple

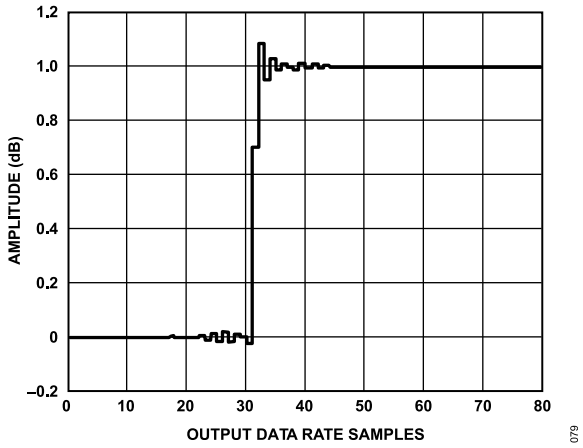

Figure 144. Wideband Low-Ripple FIR Filter Step Response

THEORY OF OPERATION

Table 20. Wideband Low-Ripple FIR Filter $\overline{SYNC\_IN}$ to Settled Data

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Rate	MCLK = 16.384MHz	MCLK = 13.107MHz	Delay from First MCLK Rise after $\overline{SYNC\_IN}$ Rise to First $\overline{DRDY}$ Rise	Delay from First MCLK Rise after $\overline{SYNC\_IN}$ Rise to Earliest Settled $\overline{DRDY}$ Rise
MCLK/2	32	256	204.8	284	4,252
	64	128	102.4	413	8,349
	128	64	51.2	797	16,669
	256	32	25.6	1,565	33,309
	512	16	12.8	3,101	66,589
	1,024	8	6.4	6,157	133,133
MCLK/4	32	128	102.4	428	8,364
	64	64	51.2	812	16,684
	128	32	25.6	1,580	33,324
	256	16	12.8	3,116	66,604
	512	8	6.4	6,188	133,164
	1,024	4	3.2	12,300	266,252
MCLK/16	32	32	25.6	1,674	33,418
	64	16	12.8	3,202	66,690
	128	8	6.4	6,274	133,250
	256	4	3.2	12,418	266,370
	512	2	1.6	24,706	532,610
	1,024	1	0.8	49,154	1,064,962

THEORY OF OPERATION

Sinc5 Filter

The Sinc5 filter offered in the ADAQ7769-1 enables a low latency signal path useful for DC inputs on control loops, or for where user-specific post processing is required. The Sinc5 filter has a −3dB bandwidth of 0.204 × ODR.

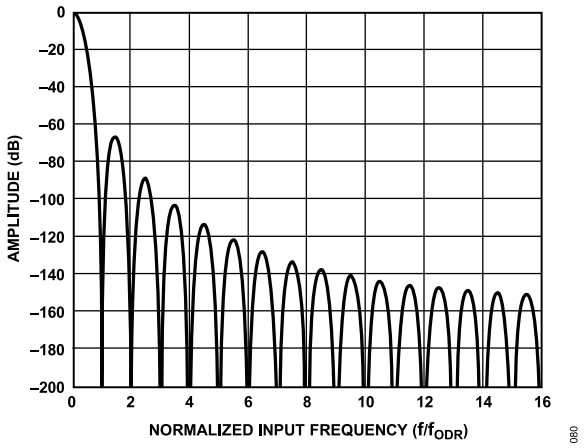

Figure 145. Sinc5 Filter Frequency Response

The impulse response of the filter is five times 1/ODR. For 250kSPS ODR, the time to settle data fully is 20µs. For the 1.024MSPS ODR, the time to settle data fully is 5µs.

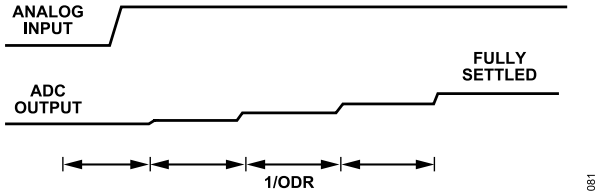

Figure 146. Sinc5 Filter Step Response

The time from a $\overline{\text{SYNC\_IN}}$ pulse to both the first $\overline{\text{DRDY}}$ and to fully settled data for various ODR values for the Sinc5 filter is shown in Table 21.

Table 21. Sinc5 Filter, $\overline{\text{SYNC\_IN}}$ to Settled Data

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Rate	MCLK = 16.384MHz	MCLK = 13.107MHz	Delay from First MCLK Rise after $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	Delay from First MCLK Rise after $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise
MCLK/2	8	1,024	819.2	46	110
	16	512	409.6	62	190
	32	256	204.8	94	350
	64	128	102.4	162	674
	128	64	51.2	295	1,319
	256	32	25.6	561	2,609
	512	16	12.8	1,093	5,189
	1,024	8	6.4	2,173	10,365
MCLK/4	8	512	409.6	79	207
	16	256	204.8	111	367
	32	128	102.4	175	687
	64	64	51.2	310	1,334
	128	32	25.6	576	2,624
	256	16	12.8	1,108	5,204
	512	8	6.4	2,172	10,364
	1,024	4	3.2	4,332	20,716
MCLK/16	8	128	102.4	278	790
	16	64	51.2	406	1,430
	32	32	25.6	662	2,710
	64	16	12.8	1,194	5,290
	128	8	6.4	2,258	10,450
	256	4	3.2	4,386	20,770
	512	2	1.6	8,642	41,410
	1,024	1	0.8	17,282	82,818

THEORY OF OPERATION

Programming for 1.024MSPS Output Data Rate

A 1.024MSPS Sinc5 filter path exists for users seeking an even higher ODR than is achievable using the wideband low-ripple FIR filter. This path is quantization noise limited. Therefore, it is best suited for customers requiring minimum latency for control loops or implementing custom digital filtering on an external field programmable gate array (FPGA) or digital signal processor (DSP).

To configure the Sinc5 FIR filter for 1.024MSPS output data rate, write 001 to FILTER bits (Register 0x19, Bits[6:4]) of Digital Filter and Decimation Control Register. The ADAQ7769-1 automatically changes the decimation rate to 8 and output data length is reduced to 16 bits from 24 bits due to the maximum speed limitation of digital serial interface.

For example, to program the ADAQ7769-1 to 1.024MSPS output data rate from power up using 16.384MHz MCLK, while using the CMOS MCLK as the clock source, the subsequent SPI writes that follow can be used:

- Data 0x33 to Register 0x15.
- Data 0x10 to Register 0x19.

Sinc3 Filter

The Sinc3 filter in the ADAQ7769-1 enables a low latency signal path useful for DC inputs on control loops, or eliminates unwanted known interferers at specific frequencies. The Sinc3 filter path incorporates a programmable decimation rate to reject known interferers. Decimation rates from 32 to 1,85,280 are achievable using the Sinc3 filter. The Sinc3 filter has a −3dB bandwidth of 0.2617 × ODR.

For example, to calculate the DEC_RATE of the Sinc3 filter with a 16.384MHz MCLK and an ODR of 50SPS with MCLK_DIV = 2, use the following equation:

$$DEC\_RATE = \frac{MCLK}{MCLK\_DIV \times ODR} \quad (15)$$

$$DEC\_RATE = \frac{16.384\text{MHz}}{2 \times 50} = 163,840$$

To program the Sinc3 decimation ratio, the user must first calculate the equivalent Sinc3 decimation ratio to be written on the SINC3 Decimation Rate (MSB) Register (Register 0x1A) and SINC3 Decimation Rate (LSB) Register (Register 0x1B) using the following equation:

$$Value = \frac{DEC\_RATE}{32} - 1 = 5,119 \quad (16)$$

To set the decimation ratio to 1,63,840, write the equivalent binary value of 5,119 to the SINC3 Decimation Rate (MSB) Register (Register 0x1A) and SINC3 Decimation Rate (LSB) Register (Register 0x1B) because the value in these registers are incremented by 1 and then multiplied by 32 to give the actual decimation rate.

Table 22 and Table 23 lists the values to be written to the Sinc3 decimation registers to achieve an ODR of 50SPS and 60SPS, respectively, for various MCLK and MCLK_DIV.

Table 22. Sinc3 Decimation Register Values for 50SPS ODR using Various MCLK and MCLK_DIV

MCLK (MHz)	MCLK_DIV	Decimation Rate	Value in DEC_RATE Register
16.384	2	163,840	5,119
	4	81,920	2,559
	8	40,960	1,279
	16	20,480	639
13.1072	2	131,072	4,095
	4	65,536	2,047
	8	32,768	1,023
	16	16,384	511

Table 23. Sinc3 Decimation Register Values for 60SPS ODR using Various MCLK and MCLK_DIV

MCLK (MHz)	MCLK_DIV	Decimation Rate	Value in DEC_RATE Register
16.384	2	136,533	4,266
	4	68,267	2,132
	8	34,133	1,066
	16	17,067	532
13.1072	2	109,227	3,412
	4	54,613	1,706
	8	27,307	852
	16	13,653	426

THEORY OF OPERATION

Programming for 50Hz, 60Hz, and 50Hz and 60Hz Rejection

To reject 50Hz tones, program the ODR of the Sinc3 filter to 50Hz (see Figure 147). It is also possible to achieve simultaneous rejection of both 50Hz and 60Hz by setting the EN_60HZ_REJ bit (Register 0x19, Bit 7) in the Digital Filter and Decimation Control Register. Rejection of both 50Hz and 60Hz line frequencies is possible in this configuration. Table 24 and Table 25 list the minimum rejection measured at the frequencies of interest with a 50SPS ODR.

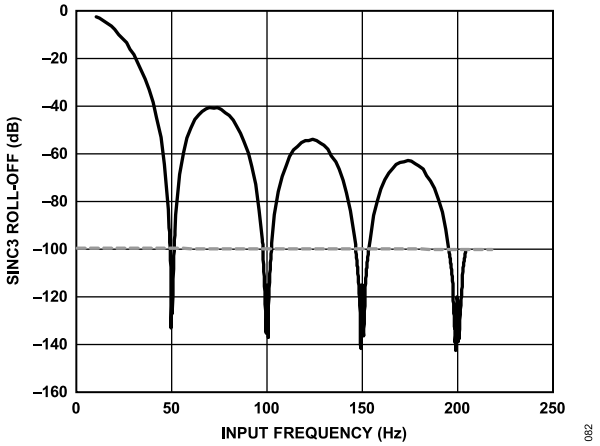

Figure 147. Sinc3 Filter Frequency Response Showing 50Hz Rejection, 50SPS ODR, ×1,63,840 Decimation

Table 24. Sinc3 Filter 50Hz Rejection, 50SPS ODR and Decimate by 1,63,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	101
100 ± 2	102
150 ± 3	102
200 ± 4	102

Table 25. Sinc3 Filter 50Hz and 60Hz Rejection, 50SPS ODR and Decimate by 1,63,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	81
60 ± 1	67
100 ± 2	83
120 ± 2	72
150 ± 3	86
180 ± 3	78
200 ± 4	90
240 ± 4	87

The impulse response of the filter is three times 1/ODR. For 250kSPS ODR, the time to settle data fully is 12µs.

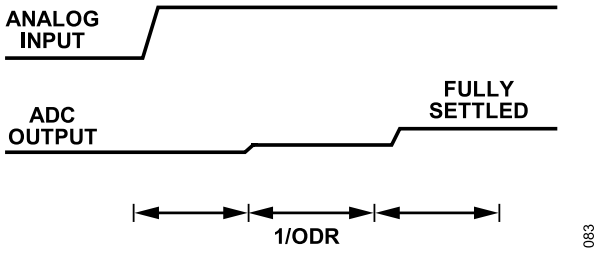

Figure 148. Sinc3 Filter Step Response

THEORY OF OPERATION

Table 26. Sinc3 Filter, $\overline{SYNC\_IN}$ to Settled Data

			ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Rate	Value in DEC_RATE Register	MCLK = 16.384MHz	MCLK = 13.107MHz	Delay from First MCLK Rise after $\overline{SYNC\_IN}$ Rise to First $\overline{DRDY}$ Rise	Delay from First MCLK Rise after $\overline{SYNC\_IN}$ Rise to Earliest Settled $\overline{DRDY}$ Rise
MCLK/2	32	0	256	204.8	127	255
	64	1	128	102.4	191	447
	128	3	64	51.2	319	831
	256	7	32	25.6	575	1,599
	512	15	16	12.8	1,087	3,135
	1,024	31	8	6.4	2,111	6,207
	163,840	5,119	0.05	0.04	327,743	983,103
MCLK/4	32	0	128	102.4	241	497
	64	1	64	51.2	369	881
	128	3	32	25.6	625	1,649
	256	7	16	12.8	1,137	3,185
	512	15	8	6.4	2,161	6,257
	1,024	31	4	3.2	4,209	12,401
	81,920	2,559	0.05	0.04	327,793	983,153
MCLK/16	32	0	32	25.6	926	1,950
	64	1	16	12.8	1,438	3,486
	128	3	8	6.4	2,462	6,558
	256	7	4	3.2	4,510	12,702
	512	15	2	1.6	8,606	24,990
	1,024	31	1	0.8	16,798	49,566
	20,480	639	0.05	0.04	328,094	983,454

THEORY OF OPERATION

TOTAL GROUP DELAY

The PGA, AAF, and the digital filter have a linear phase response and a constant group delay across the pass band. As a complete signal chain, the total group delay from the IN input to the ADC output is as follows:

$$Total\ Group\ Delay = Analog\ Group\ Delay + Digital\ Filter\ Group\ Delay \quad (17)$$

where:
Analog Group Delay is the delay from the PGA and AAF listed in the Specifications.
Digital Filter Group Delay is the delay from the selected digital filter and ODR, listed in the Specifications.

ADC SPEED AND PERFORMANCE

The ADAQ7769-1 offers a wide selection of ODR, which depends on the digital filter used. The ADAQ7769-1 can have an ODR as low as 1kSPS using the wideband low-ripple FIR filter and Sinc5 filter, and as low as 0.0125kSPS using the Sinc3 filter, which can be achieved using a high decimation ratio and operating the modulator at the lowest possible sampling rate. For example, with the wideband low-ripple FIR filter option, 1kSPS ODR can be achieved using MCLK = 16.384MHz, decimation rate = 1024, and f_{MOD} = MCLK/16.

Note that the ADAQ7769-1 modulator samples on the rising and falling edge of the f_{MOD} and outputs data to the digital filter at a rate of f_{MOD}. There is a zero in the frequency response profile of the modulator centered at the odd multiples of f_{MOD}, which means there is no foldback from frequencies at the f_{MOD} rate and at odd multiple rates. However, the modulator is open to noise for even multiples of f_{MOD}. There is no attenuation at these zones.

For optimum performance, it is recommended to use MCLK = 16.384MHz and MCLK_DIV = 2, which sets the f_{MOD} = 8.192MHz, and by keeping the f_{MOD} frequency high, it maximizes the out-of-band tone rejection from the front-end AAF.

The default controller clock divider setting for the ADAQ7769-1 is MCLK_DIV = 16. To configure the MCLK divider to MCLK_DIV = 2, write 11 to the MCLK_DIV bits (Register 0x15, Bits[5:4]) of the Power and Clock Control Register after power up.

Figure 149 shows the AAF rejection relative to f_S. Using a higher MCLK divider results in lower f_S with reduced rejection from the AAF.

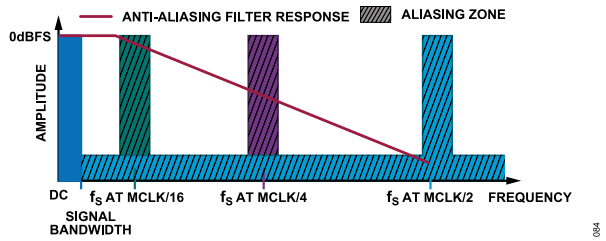

Figure 149. AAF Response vs. MCLK Divider

DEVICE CONFIGURATION METHOD

The ADAQ7769-1 has two options for controlling device functionality. On power-up, the mode is determined by the state of the $\overline{PIN}$/SPI pin. The two modes of configuration are as follow:

- SPI: Over a 3- or 4-wire SPI (complete configurability).
- $\overline{PIN}$: Pin-strapped digital logic inputs (a subset of complete configurability).

On power-up, apply a soft or hard reset to the ADAQ7769-1 when using either control mode. A $\overline{SYNC\_IN}$ pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or via pin connections only.

The first design decision is setting the ADC in either the SPI or $\overline{PIN}$ mode of configuration. In either mode, the digital host reads the ADC data over the SPI port lines.

$\overline{PIN}$ Control Mode

An overview of the $\overline{PIN}$ control mode features follows:

- No SPI write access to the device.
- Pins control all functions.
- ADC results read back over the SPI pins.
- ADC result includes an 8-bit status header output after each conversion result.
- The SDI pin can be used to create a daisy-chain of multiple devices operating in $\overline{PIN}$ mode.

SPI Control Mode

An overview of the SPI control mode features follows:

- The Standard SPI Mode 3 interface for register access, where the ADC always behaves as an SPI target.
- Indication of a new conversion via the $\overline{DRDY}$ pin output. A second method allows the user to merge the ready ($\overline{RDY}$) signal within the DOUT output stream, which allows a reduction in the number of lines across an isolation barrier.
- Reading back conversions can be performed by writing 8 bits to address the ADC register and reading back the result from the register.

THEORY OF OPERATION

- Continuous readback mode, which is enabled via an SPI write. There is no need to supply the 8 bits to address the Conversion Result Register (ADC_DATA, Register 0x2C). Data readback occurs on the application of SCLK. The $\overline{\text{DRDY}}$ pin indicates that a conversion result is complete and can be used to trigger a readback of the conversion result.
- In continuous readback mode, there is the option to append either the 8-bit status header or an 8-bit cyclic redundancy check (CRC) check, or both.

$\overline{\text{PIN}}$ CONTROL MODE OVERVIEW

$\overline{\text{PIN}}$ control mode eliminates the need for SPI communication to set the required mode of operation. It is best used for situations where the user requires a single, known configuration, to reduce routing signals to the digital host. $\overline{\text{PIN}}$ control mode is useful in digitally isolated applications where minimal configuration is needed. $\overline{\text{PIN}}$ control mode offers a subset of the core functionality and ensures a known state of operation after power-up, reset, or a fault condition on the power supply. In $\overline{\text{PIN}}$ control mode, the linearity boost buffers and the reference input precharge buffers are enabled by default for best performance.

An automatic sync pulse drives out on the $\overline{\text{SYNC\_OUT}}$ pin in $\overline{\text{PIN}}$ control mode when the device is either initially powered up or after a reset. A $\overline{\text{SYNC\_OUT}}$ pulse also occurs when a GPIOx pin toggles, which means after a change to the $\overline{\text{PIN}}$ control mode settings of the device, the synchronization is automatically performed. For this synchronization to work, connect $\overline{\text{SYNC\_OUT}}$ to $\overline{\text{SYNC\_IN}}$, which eliminates the need to provide a synchronous $\overline{\text{SYNC\_IN}}$ pulse. The $\overline{\text{SYNC\_OUT}}$ of one device can also be connected to the $\overline{\text{SYNC\_IN}}$ of many devices when the synchronization of multiple devices is required. If synchronization of multiple devices is required, all devices must share a common MCLK.

Data Output Format

$\overline{\text{PIN}}$ control mode has a set output format for conversion data. The rising $\overline{\text{DRDY}}$ edge indicates that a new conversion is ready. The next 24 serial clock falling edges clock out the 24-bit ADC result. The following eight serial clocks output the status bits of the ADAQ7769-1. The ADC data is output MSB first in twos complement format. If further SCLK falling edges are applied to the ADC after clocking out the status bits, the logic level applied to SDI is clocked out, similar to a daisy-chain scenario. In Figure 150, an extra serial clock edge (33rd falling edge) is shown. If an extra serial clock edge occurs, the logic level of the SDI pin clocks out.

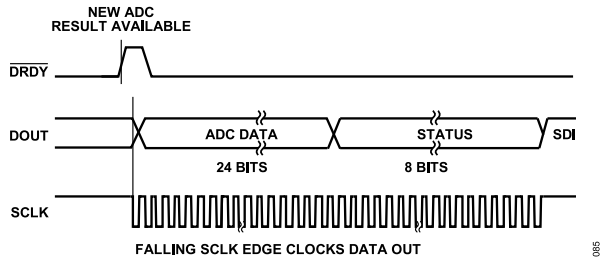

Figure 150. $\overline{\text{PIN}}$ Mode Data Output Format (No $\overline{\text{CS}}$ Signal)

Table 27. Differences in Control and Interface Pin Functions in $\overline{\text{PIN}}$ Control Mode and SPI Control Mode

	Pin Function	
Mnemonic	**$\overline{\text{PIN}}$ Control Mode**	**SPI Control Mode**
MODE0/GPIO0	MODE0 configuration pin.	GPIO0 pin.
MODE1/GPIO1	MODE1 configuration pin.	GPIO1 pin.
MODE2/GPIO2	MODE2 configuration pin.	GPIO2 pin.
MODE3/GPIO3	MODE3 configuration pin.	GPIO3 pin.
$\overline{\text{CS}}$	SPI pin for readback of ADC conversion results.	SPI interface for full configuration of the ADAQ7769-1 via a register read/write and readback of the ADC conversion results.
SCLK	SPI pin for readback of ADC conversion results.	SPI interface for full configuration of the ADAQ7769-1 via a register read/write and readback of the ADC conversion results.
SDI	SPI pin for readback of ADC conversion results.	SPI interface for full configuration of the ADAQ7769-1 via a register read/write and readback of the ADC conversion results.
DOUT/$\overline{\text{RDY}}$	SPI pin for readback of ADC conversion results.	SPI interface for full configuration of the ADAQ7769-1 via a register read/write and readback of the ADC conversion results.

THEORY OF OPERATION

Diagnostics and Status Bits

$\overline{\text{PIN}}$ control mode offers a subset of diagnostics features. Internal errors are reported in the status header output with the data conversion results for each channel.

The status header reports the internal CRC errors, memory map flipped bits, and the undetected external clock, which indicates a reset is required. The status header also reports filter settled and filter saturated signals. Users can determine when to ignore data by monitoring these error flags.

If a significant error shows in the status bits, a reset of the ADC using the $\overline{\text{RESET}}$ pin is recommended because, in $\overline{\text{PIN}}$ mode, there is no way to interrogate further for specific errors.

Daisy-Chaining—$\overline{\text{PIN}}$ Control Mode Only

Daisy-chaining devices allow multiple devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate ADAQ7769-1 devices. Daisy-chaining devices are only possible in $\overline{\text{PIN}}$ control mode.

When configured for daisy-chaining, only one ADAQ7769-1 device has its data interface in direct connection with the digital host.

For the ADAQ7769-1 cascading, the DOUT/$\overline{\text{RDY}}$ pin of the upstream ADAQ7769-1 device to the SDI pin of the next downstream ADAQ7769-1 device in the chain implements this daisy-chaining. The ability to daisy-chain devices and the limit on the number of devices that can be handled by the chain is dependent on the serial clock frequency used and the time available to clock through multiple 32-bit conversion outputs (24-bit conversion + 8-bit status) before the next conversion is complete.

The daisy-chaining feature is useful to reduce component count and to wire connections to the controller.

Figure 151 shows an example of daisy-chaining multiple ADAQ7769-1 devices.

The daisy-chain scheme depends on all devices receiving the same MCLK and SCLK, being synchronized, and being configured with the same decimation rate. The chip-select signal ($\overline{\text{CS}}$) gates each conversion chain of data, its rising edge resetting the SPI to a known state after each conversion ripples through. The ADAQ7769-1 device that is furthest from the controller must have its SDI pin connected to VDD_IO, logic high.

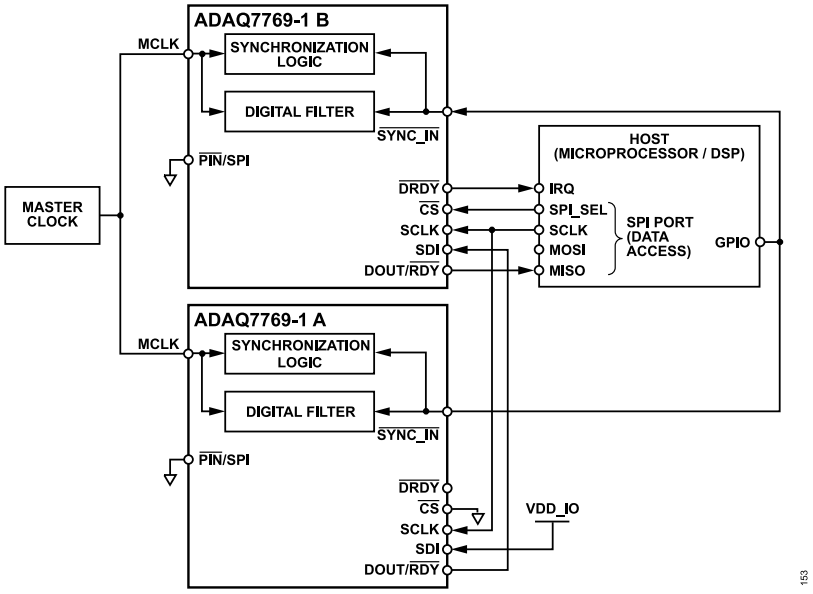

Figure 151. Daisy-Chaining Multiple ADAQ7769-1 Devices

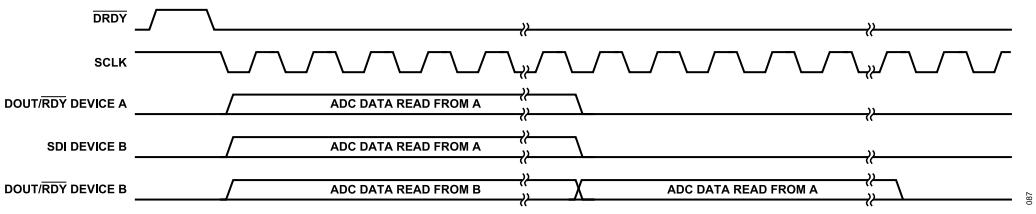

Figure 152. Data Output Format when Devices Daisy-Chained ($\overline{\text{PIN}}$ Control Mode Only)

THEORY OF OPERATION

Table 28. $\overline{PIN}$ Control Settings for MODEx Pins

MODEx Pin Settings					ADC Configuration			
MODEx (Hex)	MODE3/ GPIO3	MODE2/ GPIO2	MODE1/ GPIO1	MODE0/ GPIO0	f_{MOD} Frequency	Filter	Decimation	MCLK = 16.384MHz, ODR
0	0	0	0	0	MCLK/2	Wideband low-ripple FIR	×32	256kSPS
1	0	0	0	1	MCLK/2	Wideband low-ripple FIR	×64	128kSPS
2	0	0	1	0	MCLK/2	Sinc5	×32	256kSPS
3	0	0	1	1	MCLK/2	Sinc5	×64	128kSPS
4	0	1	0	0	MCLK/4	Wideband low-ripple FIR	×32	128kSPS
5	0	1	0	1	MCLK/4	Wideband low-ripple FIR	×64	64kSPS
6	0	1	1	0	MCLK/4	Sinc5	×32	128kSPS
7	0	1	1	1	MCLK/4	Sinc5	×64	64kSPS
8	1	0	0	0	MCLK/16	Wideband low-ripple FIR	×32	32kSPS
9	1	0	0	1	MCLK/16	Wideband low-ripple FIR	×64	16kSPS
A	1	0	1	0	MCLK/16	Sinc5	×32	32kSPS
B	1	0	1	1	MCLK/16	Sinc5	×64	16kSPS
C	1	1	0	0	MCLK/2	Sinc5	×8	833kSPS[1]
D	1	1	0	1	MCLK/2	Sinc3 50Hz and 60Hz rejection[2]	×1,63,840	50SPS
E	1	1	1	0	MCLK/16	Sinc3 50Hz and 60Hz rejection[2]	×20,480	50SPS
F	1	1	1	1	ADC standby			

[1] In $\overline{PIN}$ mode, only the Sinc5, MCLK/2, decimate by 8 configuration cannot be used with a 16.384MHz MCLK due to the lack of SCLK pulses to drive out the 24-bit output (16-bit ADC data + 8-bit status) given that the maximum SCLK is 20MHz. The maximum data rate possible when used with a 13.33MHz MCLK is 833kSPS.

[2] Sinc3 filter, rejection of 50Hz and 60Hz. Rejection of 50Hz and 60Hz is possible only if the MCLK applied in control mode is equal to 16.384MHz. The decimation rate is tuned internally for these $\overline{PIN}$ mode settings so that the sinc filter notches fall at 50Hz and 60Hz.

THEORY OF OPERATION

SPI CONTROL OVERVIEW

SPI control offers a superset of flexibility and diagnostics to the user, and the categories are shown in Table 29 define the major controls, conversion modes, and diagnostic monitoring abilities enabled in SPI control mode.

Table 29. SPI Control Capabilities

SPI Control	Capabilities	Meaning for the User
MCLK Division	MCLK/2 to MCLK/16	The ability to customize clock frequency relating to the bandwidth of interest.
MCLK Source	CMOS, crystal, LVDS, and internal clock	Allows the user a distributed or local clock capability.
Digital Filter Style	Wideband low-ripple FIR, Sinc5, Sinc3 (programmable)	The ability to customize the latency and frequency response to the measurement target of the user and its bandwidth.
Interface Format	Bit length	The ability to change between a 24-bit and a 16-bit conversion length in continuous read mode.
	Status bits	The ability to view output device status bits with the ADC conversion results.
	CRC	The ability to implement error checking when transmitting data.
	Data streaming	The ability to stream conversion data, eliminating interface write overhead.
Analog Buffers	Linearity boost buffer	Boost the linearity performance.
	Reference input precharge	Reduces reference input current, which makes it easier to filter the reference.
	Reference input full buffer	This full high-impedance buffer enables filtering of reference source and enables high impedance sources, that is, reference resistors.
Conversion Modes	Single conversion	The ability to return to standby after one conversion.
	One shot	The ability to perform a conversion similar to a timed successive approximation register (SAR) conversion, in which the ADAQ7769-1 converts on a timed pulse.
	Continuous conversion	Normal operation keeps the modulator continually converting, which offers the fastest response to a change on the input.
	Duty-cycled conversion	The ability to save more power for point conversions. Times the rate of conversion and sets the time for the ADC to remain in standby after the conversion completes.
	Calibration	The ability to run a calibration of the system and to save gain calibration or offset calibration results to the system settings of the user by reading back from the gain/offset registers.
Conversion Targets	ADC inputs	The ability to measure the input signal applied at the ADC input.
	Temperature sensor	The ability to measure local temperatures with an on-chip temperature sensor. Used for relative temperature measurement.
	Diagnostic sources	The ability to measure reference inputs and internal voltages for periodic functional safety checking.
GPIO Control	Up to four GPIOx pins	The ability to control other local hardware (such as gain stages), to power down other blocks in the signal chain, or read local status signals over the SPI interface of the ADAQ7769-1.
System Offset and Gain Correction	System calibration routines	The ability to correct offset and/or gain by writing to registers when the environment changes (that is, the temperature increases). Requires characterization of system errors to feed these registers.
Diagnostics	Internal checks and flags	Users can have the highest confidence in the conversion results.

THEORY OF OPERATION

SPI CONTROL MODE

MCLK Source and MCLK Division

MCLK division (MCLK_DIV) bits (Register 0x15, Bits[5:4]) control the divided ratio between the MCLK applied at the input to the ADAQ7769-1 and the clock used by the ADC modulator. Select the division ratio best for configuration of the clocks.

The following options are available as the MCLK input source in SPI mode:

- LVDS
- External crystal
- CMOS input MCLK

From the Power and Clock Control Register, set the CLOCK_SEL bits (Register 0x15, Bits[7:6]) to 00 to configure the ADAQ7769-1 for a CMOS clock, and set these bits to 01 to enable the use of an external crystal. Setting these bits to 10 enables the application of the LVDS clock to the XTAL2_MCLK pin. LVDS clocking is exclusive to SPI mode and requires register selection for operation.

ADC Power-Down Mode

All blocks on the core ADC are turned off. A specific code is required to wake the ADC up. All register contents are lost when entering power-down mode. Ensure the FDA is powered down or is in standby mode before entering the ADC into power-down mode. Connecting the M0_ADC and M1_ADC to M0_FDA and M1_FDA, respectively, automatically powers down the FDA when the ADC is in power-down mode. The ADC power-down mode can be set from the Power and Clock Control Register.

ADC Standby Mode

The analog clocking and power functions of the core ADC are powered down. The digital LDO regulator and register settings are retained when in standby mode. This mode is best used in scenarios where the ADC is not in use, briefly, and the user wants to save power. For more details on how to set the ADC to standby mode, see the Data Conversion Modes section.

SPI Synchronization

The ADAQ7769-1 can be synchronized over the SPI. The final SCLK rising edge of the command is the instance of synchronization. This command initiates the $\overline{\text{SYNC\_OUT}}$ pin to pulse active low and then back active high again. $\overline{\text{SYNC\_OUT}}$ is a signal synchronized internally to the MCLK of the ADC. Connecting the output of $\overline{\text{SYNC\_OUT}}$ to the $\overline{\text{SYNC\_IN}}$ input synchronizes that individual ADC. Routing $\overline{\text{SYNC\_OUT}}$ to other ADAQ7769-1 devices also ensures the devices are synchronized, as long as the devices share a common MCLK source, as shown in Figure 153.

It is recommended to perform synchronization functions directly after the $\overline{\text{DRDY}}$ pulse. If the ADAQ7769-1 $\overline{\text{SYNC\_IN}}$ pulse occurs too close to the upcoming $\overline{\text{DRDY}}$ pulse edge, the upcoming $\overline{\text{DRDY}}$ pulse may still be output because the $\overline{\text{SYNC\_IN}}$ pulse has not yet propagated through the device.

When using the $\overline{\text{SYNC\_OUT}}$ function with an VDD_IO voltage of 1.8V, it is recommended to set the $\overline{\text{SYNC_OUT}}$_POS_EDGE bit to 1 (Register 0x1D, Bit 6) in the Synchronization Modes and Reset Triggering Register.

THEORY OF OPERATION

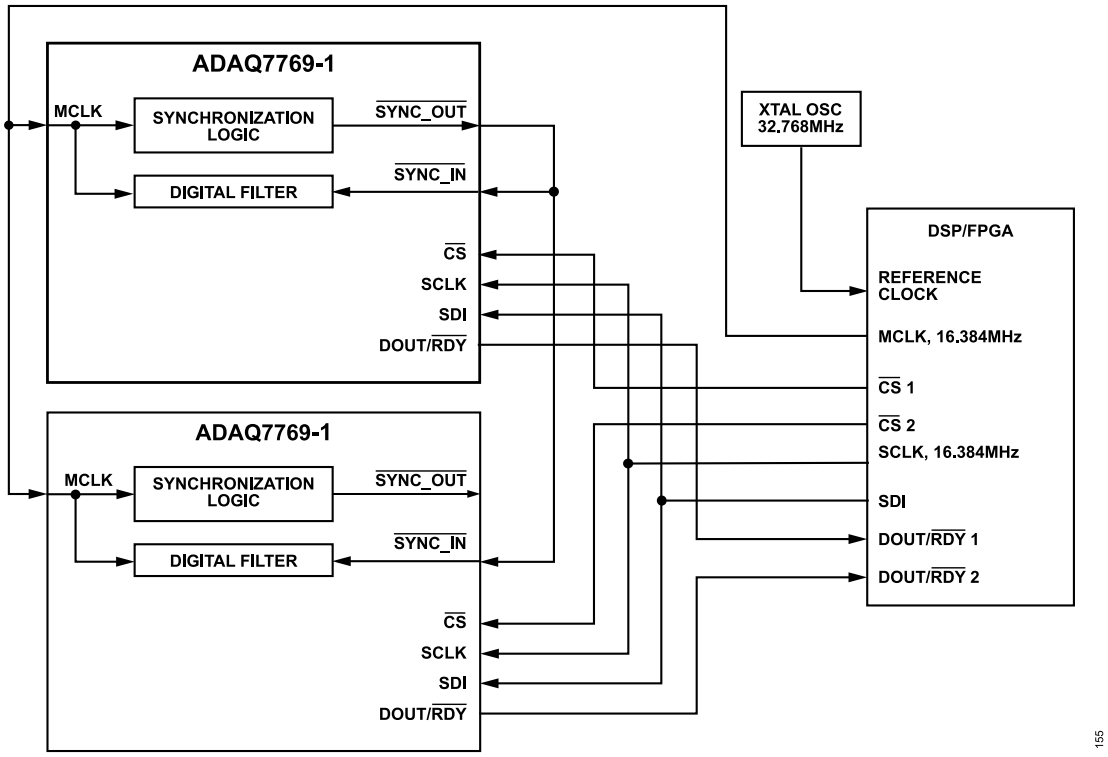

Figure 153. Basic SPI Synchronization Diagram

THEORY OF OPERATION

Offset Calibration

In SPI control mode, the ADAQ7769-1 has the ability to calibrate the offset and gain. There are options to alter the gain and offset of the ADAQ7769-1 and its subsystem. These options are available in SPI control mode only.

The offset correction registers provide 24-bit, signed, twos complement registers for channel offset adjustment. If the channel gain setting is at the ideal nominal value of 0x555555, an LSB of the offset register adjustment changes the digital output by −4/3LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133LSBs. Because offset calibration occurs before gain calibration, the LSB ratio of −4/3 changes linearly with gain adjustment through the gain correction registers.

For more details on the register information and calibration instructions, see the Offset Calibration MSB Register, Offset Calibration MID Register, and Offset Calibration LSB Register sections.

Gain Calibration

In the SPI control mode, alter the gain and offset of the ADAQ7769-1 and its subsystem. These options are available in SPI control mode only.

The ADC has an associated gain coefficient stored for each ADC after factory programming. Nominally, this gain is approximately 0x555555 value (for an ADC channel). Overwrite the gain register setting. However, after a reset or power cycle, the gain register values revert to the hard-coded, programmed factory setting.

$$ADC\_DATA = \left[\frac{3 \times V_{IN} \times TOTAL\_GAIN}{V_{REF}} \times 2^{21} - \left(OffsetCal\right)\right] \times \frac{GainCal}{4} \times \frac{4,194,300}{2^{42}} \quad (18)$$

where:
ADC_DATA (Register 0x2C, see the Conversion Result Register section) is in the twos complement format.
OffsetCal is the decimal value from the offset calibration registers (Register 0x21, Register 0x22, and Register 0x23, see the Offset Calibration MSB Register, Offset Calibration MID Register, and Offset Calibration LSB Register).
GainCal is the decimal value from the gain calibration registers (Register 0x24, Register 0x25, and Register 0x26). The gain calibration register sections provides further register information and calibration instructions (see the Gain Calibration MSB Register, Gain Calibration MID Register, and Gain Calibration LSB Register).

Reset over SPI Control Interface

Issue a reset command to the ADAQ7769-1 by writing to the SPI_$\overline{\text{RESET}}$ bits (Register 0x16, Bits[1:0]) in the Synchronization Modes and Reset Triggering Register. Two successive writes to these bits are required to initiate the device reset.

Resume from Shutdown

Shutdown mode features the lowest possible current consumption with all blocks on the device turned off, including the standard SPI. Therefore, to wake the ADC up from this mode, either a hardware reset on the $\overline{\text{RESET}}$ pin or a specific code on the SPI SDI input is required. The specific sequence required on SDI consists of a 1 followed by 63 zeros, clocked in by SCLK while $\overline{\text{CS}}$ is low, which allows the system to wake up the ADAQ7769-1 from shutdown without using the $\overline{\text{RESET}}$ pin. This reset function is useful in isolated applications where the number of pins brought across the isolation barrier must be minimized.

GPIO and $\overline{\text{START}}$ Functions

When operating in SPI mode, the ADAQ7769-1 has additional GPIO functionality. This fully-configurable mode allows the device to operate four GPIOs. These pins can be configured as read or write in any order.

GPIO read is a useful feature because it allows a peripheral device to send information to the input GPIO. Then, this information can be read from the SPI of the ADAQ7769-1.

The GPIOx pins can be set as inputs or outputs on a per pin basis, and there is an option to configure outputs as open-drain.

In SPI control mode, one of the GPIOx pins can be assigned the function of the $\overline{\text{START}}$ input. The $\overline{\text{START}}$ function allows a signal asynchronous to MCLK to be used to generate the $\overline{\text{SYNC\_OUT}}$ signal to reset the digital filter path of the ADAQ7769-1. The $\overline{\text{START}}$ pin function can be enabled on GPIO3.

SPI Mode Diagnostic Features

The ADAQ7769-1 includes diagnostic coverage across the internal blocks within the core ADC. The diagnostics in the following list allow the user to monitor the ADC and to increase confidence in the fidelity of the data acquired:

- Reference detection
- Clock qualification
- CRC on SPI transaction
- Flags for detection of an illegal register write
- CRC checks
- Power-on reset (POR) monitor
- MCLK counter

In addition, these diagnostics are useful in situations where instruments require remote checking of power supplies and references during initialization stages.

The diagnostics are selectable by the user via the SPI Diagnostic Control Register, ADC Diagnostic Feature Control Register, and Digital Diagnostic Feature Control Register. The flags for POR and the clock qualification are on by default. The flags are readable via

THEORY OF OPERATION

registers, but also ripple through to the top-level status bits that can be output with each ADC conversion, if required.

Reference Detection

Write 1 to the EN_ERR_REF_DET bit (Register 0x29, Bit 3) of the ADC Diagnostic Feature Control Register to enable the reference detection block in SPI control mode. When enabled, the error flags in the ADC Diagnostics Output Register (Register 0x2F). Any error flags then propagate through to the Device Error Flags Main Register (Register 0x2D). The reference error flags when the reference applied on the REF+ pin is less than 1/3 of (VDD_ADC − AGND).

Clock Qualification

The clock qualification check attempts to detect when a valid MCLK is detected. When the MCLK applied is greater than 600kHz, the clock qualification passes. The error flags in both the ADC Diagnostics Output Register (Register 0x2F) and the Device Error Flags Main Register (Register 0x2D). If the clock detected is less than the 600kHz frequency threshold, or if an external MCLK is not detected, the clock qualification error bit is set to 1. To disable the clock qualification check, write 0 to the EN_ERR_EXT_CLK_QUAL bit (Register 0x29, Bit 0) of the ADC Diagnostic Feature Control Register.

CRC on SPI Transaction

For more details, see the CRC Check on Serial Interface section.

Flags for Detection of Illegal Register Write

For more details, see the SPI Control Interface Error Handling section.

CRC Checks

Enable CRC checks in the Digital Diagnostic Feature Control Register (Register 0x2A) to check the state of the memory map of the ADAQ7769-1 and the internal random-access memory (RAM) and fuse settings. If any of these errors flag on the device, perform a reset to return the device to a valid state.

POR Monitor

The POR monitor flag appears in both the register and the status bits when output. The POR flag indicates that a reset or a temporary supply brown out occurred.

MCLK Counter

The MCLK Diagnostic Output Register (Register 0x31) updates every 64 MCLKs. The MCLK counter register verifies that the ADAQ7769-1 is still receiving a valid MCLK. Read the MCLK counter register according to the specific MCLK to SCLK ratio to ensure that a valid read occurs. The SCLK applied to read the MCLK_COUNTER register must be less than 2.1 × MCLK or greater than 4.6 × MCLK. For example, if MCLK = 2MHz, the SCLK applied cannot be in the 4.2MHz to 9.2MHz range. If the MCLK to SCLK ratio is not adhered to, the read may corrupt because the MCLK may update during the read of the register, which causes an error.

Product Identification (ID) Number

The ADAQ7769-1 contains ID registers that allow software interrogation of the silicon. The class of the product (precision ADC), product ID, device revision, and grade of device can all be read from the registry over the SPI. The vendor ID for Analog Devices, Inc., is also included in the registry for readback. These registers, in addition to a scratch pad that allows free reads from and writes to a specific register address, are methods of verifying the correct operation of the serial control interface.

Table 30. Product Identification Registers

Register Address (Hex)	Name	Bit Fields	
0x03	Chip type	Reserved	Class
0x04	Product ID [7:0]	PRODUCT_ID[7:0]	
0x05	Product ID [15:8]	PRODUCT_ID[15:8]	
0x06	Grade and revision	Grade	DEVICE_REVISION
0x0A	Scratch pad	Value	
0x0C	Vendor ID	VID[7:0]	
0x0D		VID[15:8]	

QUICK START-UP GUIDE

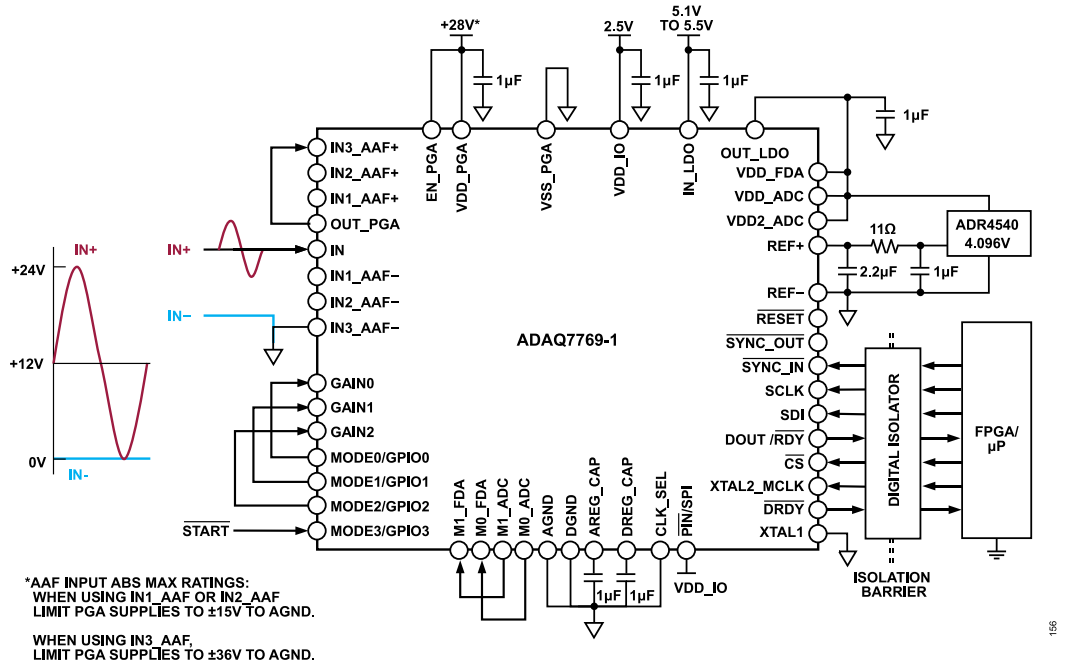

Figure 154. Typical Connection Diagram of ADAQ7769-1

POWER SUPPLY CONNECTION

The ADAQ7769-1 has several power supplies to power each block of the signal chain. To reduce the number of power supplies required to power up the device , the ADAQ7769-1 has a built-in LDO to supply power to VDD_FDA, VDD_ADC, and VDD2_ADC. The LDO regulator can also supply the power required by the recommended voltage reference, ADR4540. The LDO regulator can handle input voltage range of 5.1V to 5.5V. For proper operation, it is recommended to use a 1µF capacitor at the input and output of the LDO regulator. If the LDO regulator is not used during normal operation, it is recommended to keep all the LDO regulator pins floating.

Depending on the input signal, the VDD_PGA – VSS_PGA supplies can be set to a maximum of 30V. VDD_PGA must be at least 2.5V higher than the input, and at least as high as the PGA output, while VSS_PGA must be at least 2.5V more negative than the input, and at least as low as the PGA output, to avoid input and output clipping.

VDD_IO powers the internal regulator needed by the digital logic of the ADC, VDD_IO is referenced to DGND and can vary from 1.7V to 3.6V.

The ADAQ7769-1 has a built-in 0.1µF internal decoupling capacitor on each power supply. For more details on power supply connection and decoupling, see the Power Supplies and Power Supply Decoupling sections.

Table 31. Power-Supply Voltage Requirements

	Supply Voltage (V)		
Supplies	**Min**	**Typ**	**Max**
VDD_PGA	5		30
VSS_PGA	−25		0
VDD_PGA − VSS_PGA	5		30
IN_LDO	5.1	5.3	5.5
VDD_FDA	4.75	OUT_LDO (5V)	5.5
VDD_ADC	4.75	OUT_LDO (5V)	5.5
VDD2_ADC	2	OUT_LDO (5V) or 2.5	5.5
VDD_IO	1.7	2.5	3.6

QUICK START-UP GUIDE

DEVICE CONTROL MODE

The ADAQ7769-1 has two options to control device functionality. On power-up, the mode is determined by the state of the $\overline{\text{PIN}}$/SPI pin. The two modes of configuration are as follows:

- $\overline{\text{PIN}}$/SPI = VDD_IO = SPI control mode: Over a 3- or 4-wire SPI (complete configurability), suggested control mode.
- $\overline{\text{PIN}}$/SPI = DGND = $\overline{\text{PIN}}$ control mode: Pin-strapped digital logic inputs (a subset of complete configurability, daisy-chain is available only at this mode).

The first design decision is setting the ADC in either the SPI or $\overline{\text{PIN}}$ mode of configuration.

On power-up, apply a soft or hard reset to the device when using either control mode. A $\overline{\text{SYNC\_IN}}$ pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or through pin connections only.

The Device Configuration Method section provides a detailed discussion on the capability and limitations of the two control mode options.

INPUT RANGE SELECTION

The ADAQ7769-1 input is a low noise, low bias current, high-bandwidth programmable gain amplifier (PGA). The PGA has eight binary gain settings from 1 to 128, controlled from the GAIN2, GAIN1, and GAIN0 pins. The gain pins can be set using a logic controller or FPGA. Following the PGA is a low distortion, high-bandwidth ADC driver with a fourth-order AAF. It has three differential input pairs IN1_AAF, IN2_AAF, and IN3_AAF, from which the user selects from. Each input pair has a fixed gain, of 1, 0.364, and 0.143, respectively. Table 12 to Table 14 list down the combination of PGA gains and AAF gains, and their corresponding input ranges. For more details on noise performance across various input ranges and ADC configurations, see the Noise Performance section.

GPIO Pins

The PGA gain pins can be connected to the GPIO pins of the ADAQ7769-1 to enable the user to control the PGA gain over SPI. When the GPIO pins are used to control the gain, the user must configure the GPIO Port Control Register (Register 0x1E) to enable the GPIO and set the necessary GPIO ports as outputs. To set the logic output level for the GPIO pins, configure the GPIO Output Control Register (Register 0x1F).

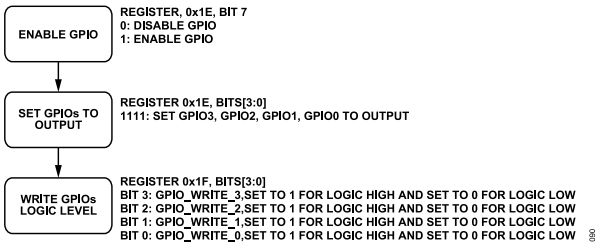

Figure 155. GPIO Gain Control Flowchart

For example, GAIN0, GAIN1, and GAIN2 are connected to GPIO0, GPIO1, and GPIO2, respectively. In SPI control mode, the user can enable the GPIO control port and set the necessary GPIO pins as outputs by writing 0x87 to the GPIO Port Control Register (Register 0x1E). By default, the GPIO Output Control Register (Register 0x1F) has an output logic low to GPIO0, GPIO1, and GPIO2, leading to a PGA gain of 1.

SELECTING THE MCLK DIVIDER AND SOURCE

MCLK Source Selection

Program the MCLK source using the two control mode options, $\overline{\text{PIN}}$ and SPI control modes.

In $\overline{\text{PIN}}$ control mode, the CLK_SEL pin sets the external MCLK source. Three clock options are available in $\overline{\text{PIN}}$ control mode: an internal oscillator, an external CMOS, or a crystal oscillator.

- Set CLK_SEL = 0 in $\overline{\text{PIN}}$ control mode to select the CMOS clock option and apply the external CMOS clock signal to the XTAL2_MCLK pin. In this case, tie the XTAL1 pin to DGND.
- Set CLK_SEL = 1 in $\overline{\text{PIN}}$ control mode to select the crystal option and connect the external crystal across the XTAL1 and XTAL2_MCLK pins.

In SPI control mode, the ADAQ7769-1 has an internal oscillator used for initial power-up of the device. After the ADAQ7769-1 completes the start-up routine, there is a clock handover to the external MCLK. The following options are available for the MCLK input source and can be set from the CLOCK_SEL bits (Register 0x15, Bits[7:6]) in the Power and Clock Control Register:

- CLOCK_SEL bits = 00: CMOS clock on the XTAL2_MCLK.
- CLOCK_SEL bits = 01: External crystal oscillator.
- CLOCK_SEL bits = 10: LVDS input enable (exclusive to SPI control mode).
- CLOCK_SEL bits = 11: Internal coarse RC clock (diagnostics).

When switching from one clock source to another, apply a soft reset to the device.

For optimum AC performance, it is not recommended to use the internal clock as the MCLK source.

QUICK START-UP GUIDE

MCLK Divider

The MCLK signal received by the ADAQ7769-1 defines the Σ-Δ modulator clock rate of the ADC core (f_{MOD}) and, in turn, the sampling frequency of the modulator of 2 × f_{MOD}. For optimum performance, it is recommended to use MCLK = 16.384MHz and MCLK_DIV = 2, which sets f_{MOD} = 8.192MHz, keeping the f_{MOD} frequency high and maximizing the out-of-band tone rejection from the front-end AAF.

$$f_{MOD} = \frac{MCLK}{MCLK\_DIV} \quad (19)$$

The default controller clock divider setting for the ADAQ7769-1 is MCLK divider = 16. To configure the MCLK divider to MCLK = 2, write 11 to the MCLK_DIV bits (Register 0x15, Bits[5:4]) in the Power and Clock Control Register after power up.

Control of the settings for the modulator frequency differs in $\overline{PIN}$ control mode vs. SPI control mode. For $\overline{PIN}$ control mode, see Table 28, and for SPI control mode, see the Power and Clock Control Register section.

MCLK and SCLK Alignment

The ADAQ7769-1 interface is flexible to allow the multiple modes of operation and various data output formats to work across different DSPs and microcontroller units (MCUs). To achieve maximum performance, it is recommended to have a synchronous SCLK and MCLK from the same clock source. It is also possible to set SCLK to be a divided down version of MCLK. The Recommended Interface section provides a detailed discussion about digital interface.

DIGITAL FILTER SETTING

The ADAQ7769-1 offers three types of digital filters. The digital filters available on the ADAQ7769-1 are as follows:

- Wideband low-ripple FIR filter, −3dB at 0.433 × ODR (6 rates).
- Sinc5, low latency filter, −3dB at 0.204 × ODR (8 rates).
- Sinc3, low latency filter, –3dB at 0.2617 × ODR, widely programmable data rate.

For more details on the digital filter setting, see the Digital Filtering section.

Decimation Rate and Output Data Rate

The ADAQ7769-1 has programmable decimation rates for the wideband low-ripple FIR, Sinc5, and Sinc3 digital filters. The decimation rates allow to band limit the measurement, which reduces the speed and input bandwidth but increases the resolution because there is further averaging in the digital filter. Filter selection and decimation rate setting when using $\overline{PIN}$ control mode are listed in Table 28, while the SPI control mode requires a register write to the Digital Filter and Decimation Control Register (Register 0x19). The SINC3 Decimation Rate (MSB) Register and SINC3 Decimation Rate (LSB) Register) are required when setting the decimation rate for sinc3 using the SPI.

Use the following equation to calculate the ODR of the ADAQ7769-1:

$$ODR = \frac{f_{MOD}}{DEC\_RATE} \quad (20)$$

ADC POWER MODE

Th ADC core power mode must match the MCLK_DIV setting. The default power setting of the ADAQ7769-1 is set to low-power mode. For optimum performance, change the ADC_MODE to fast-power mode by writing 11 to the ADC_MODE bits (Register 0x15, Bits[1:0]) in the Power and Clock Control Register with MCLK_DIV = 2.

BASIC REGISTER SETUP

Figure 156 shows the basic flow of register writes for ADAQ7769-1 upon power up.

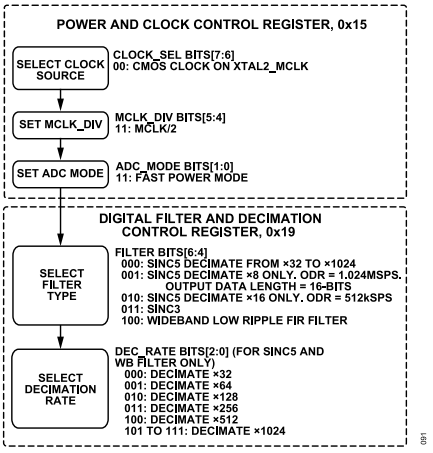

Figure 156. Basic Register Setup for ADAQ7769-1

QUICK START-UP GUIDE

QUICK START EXAMPLES

Wideband Low-Ripple FIR Filter

For example, to operate the ADAQ7769-1 under the following conditions:

- MCLK sourced from CMOS clock.
- The MCLK divider is set to 2 (recommended).
- The ADC power mode is set to fast-power mode (recommended).
- Wideband low-ripple FIR filter used.
- Decimation rate is set to 32.

The equivalent consecutive SPI writes are as follows:

- Data 0x33 to Power and Clock Control Register (Register 0x15).
- Data 0x40 to Digital Filter and Decimation Control Register (Register 0x19).

ODR = 1.024MSPS

If the application has an ODR = 1.024MSPS, it requires the following:

- A 16.384MHz MCLK.
- The MCLK divider set to 2.
- The ADC power mode set to fast mode.
- A Sinc5 filter.
- Decimation rate set to 8 (16-bit output data length).

Note that the ADAQ7769-1 automatically changes the output data length to 16 bit instead of 24 bit when using a Sinc5 filter specifically with the decimation rate of 8 because this particular use case is quantization noise limited. Assuming a CMOS MCLK source, equivalent consecutive SPI writes are as follows:

- Data 0x33 to Power and Clock Control Register (Register 0x15).
- Data 0x10 to Digital Filter and Decimation Control Register (Register 0x19).

NOISE PERFORMANCE

The noise performance of the signal chain is highly dependent on the input range of the application and the required ODR of the ADAQ7769-1. While the input range is varied by the selected PGA_GAIN and AAF_GAIN, the ODR of the device is dependent on the MCLK and the configured decimation rate. Use the following equations to calculate the ODR, for any digital filter:

$$f_{MOD} = \frac{MCLK}{MCLK\_DIV} \quad (21)$$

$$ODR = \frac{f_{MOD}}{DEC\_RATE} \quad (22)$$

where:
f_{MOD} is the ADC modulator frequency.
MCLK is the controller clock frequency.
MCLK_DIV is the ratio between the MCLK applied at the input to the ADAQ7769-1 and the clock used by the ADC modulator.
DEC_RATE is the decimation rate.

Noise performance also depends on the type of digital filter used, each having different −3dB bandwidths. The digital filters available on the ADAQ7769-1 are:

- Wideband low-ripple FIR filter, −3dB at 0.433 × ODR.
- Sinc5 low latency filter, −3dB at 0.204 × ODR.
- Sinc3 low latency filter, –3dB at 0.2617 × ODR.

The DEC_RATE, MCLK, MCLK_DIV, and type of digital filter can be varied by the user, and the manner of configuration varies between the $\overline{PIN}$ and SPI Modes (see the Device Configuration Method section).

Table 32 to Table 40 list the noise performance for the different digital filters of the ADAQ7769-1 for various ODR values, PGA_GAIN, and AAF_GAIN. The specified noise values are typical with an external 4.096V reference (V_{REF}). The RMS noise is measured with IN pin shorted to AGND.

AAF_GAIN = IN1_AAF

Table 32. Wideband Low-Ripple FIR Filter RMS Noise Performance (µV rms) vs. ODR (IN1_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	32	256	110.8	12.00	6.70	4.05	2.78	2.18	1.90	1.73	1.57
16.384	64	128	55.4	8.10	4.54	2.79	1.94	1.54	1.34	1.25	1.19
16.384	128	64	27.7	5.69	3.19	1.96	1.37	1.09	1.95	0.89	0.86
16.384	256	32	13.9	4.02	2.26	1.40	0.97	0.77	0.68	0.64	0.62
16.384	512	16	6.9	2.82	1.65	0.95	0.69	0.55	0.49	0.45	0.44
16.384	1,024	8	3.5	2.03	1.13	0.71	0.49	0.39	0.35	0.32	0.31
13.107	32	204.8	88.7	11.78	6.43	3.81	2.56	1.98	1.71	1.57	1.44
13.107	64	102.4	44.3	7.95	4.40	2.62	1.78	1.39	1.21	1.12	1.07
13.107	128	51.2	22.2	5.56	3.06	1.84	1.26	0.98	0.86	0.80	0.77
13.107	256	25.6	11.1	3.94	2.18	1.30	0.89	0.70	0.61	0.57	0.55

Table 33. Sinc5 RMS Noise Performance (µV rms) vs. ODR (IN1_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	8	1,024 (16-bit)	208.9	59.89	30.30	15.48	8.23	4.74	3.13	2.36	1.87
16.384	16	512	104.4	13.53	7.37	4.35	2.90	2.22	1.90	1.70	1.51
16.384	32	256	52.2	8.23	4.60	2.80	1.94	1.53	1.34	1.24	1.16
16.384	64	128	26.1	5.68	3.18	1.96	1.36	1.09	0.95	0.89	0.85
16.384	128	64	13.1	3.99	2.26	1.38	0.98	0.78	0.68	0.64	0.61
16.384	256	32	6.5	2.86	1.60	0.99	0.69	0.55	0.49	0.46	0.44
13.107	32	204.8	41.8	8.02	4.41	2.65	1.78	1.39	1.20	1.12	1.05
13.107	64	102.4	20.9	5.60	3.10	1.84	1.25	0.98	0.85	0.80	0.77
13.107	128	51.2	10.4	3.93	2.16	1.30	0.89	0.69	0.61	0.57	0.55
13.107	256	25.6	5.2	2.82	1.53	0.93	0.64	0.50	0.44	0.41	0.40

NOISE PERFORMANCE

Table 34. Sinc3 RMS Noise Performance (µV rms) vs. ODR (IN1_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	32	256	67.0	18.50	9.91	4.94	3.11	2.08	1.55	1.37	1.27
16.384	128	64	16.7	4.43	2.44	1.52	1.07	0.88	0.74	0.69	0.70
16.384	512	16	4.2	2.20	1.24	0.77	0.56	0.44	0.39	0.36	0.36
16.384	2,048	4	1.05	1.16	0.65	0.39	0.28	0.22	0.20	0.18	0.18
16.384	8,192	1	0.26	0.66	0.37	0.22	0.15	0.14	0.11	0.11	0.10
16.384	163,840	0.05	0.013	0.37	0.22	0.12	0.08	0.05	0.05	0.04	0.04

AAF_GAIN = IN2_AAF

Table 35. Wideband Low-Ripple FIR Filter RMS Noise Performance (µV rms) vs. ODR (IN2_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	32	256	110.848	31.47	15.82	8.34	4.56	2.82	2.12	1.77	1.58
16.384	64	128	55.4	21.21	11.05	5.48	3.09	1.90	1.45	1.30	1.20
16.384	128	64	27.7	14.49	7.54	3.94	2.17	1.98	1.03	0.91	0.85
16.384	256	32	13.9	10.24	5.43	2.80	1.57	0.98	0.73	0.65	0.63
16.384	512	16	6.9	7.40	3.75	1.98	1.10	0.68	0.52	0.47	0.46
16.384	1,024	8	3.5	5.21	2.71	1.36	0.78	0.51	0.38	0.33	0.33
13.107	32	204.8	88.7	31.51	15.88	8.68	4.68	2.84	2.11	1.78	1.59
13.107	64	102.4	44.3	21.70	10.57	5.62	3.20	1.97	1.47	1.26	1.22
13.107	128	51.2	22.2	14.79	7.47	3.95	2.15	1.43	1.04	0.90	0.86
13.107	256	25.6	11.1	10.27	5.34	2.74	1.60	1.01	0.74	0.65	0.61

Table 36. Sinc5 RMS Noise Performance (µV rms) vs. ODR (IN2_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	8	1,024 (16-bit)	208.9	166.49	84.02	43.95	20.32	10.46	5.19	2.74	1.56
16.384	16	512	104.4	32.37	16.70	8.48	4.33	2.14	1.20	0.78	0.66
16.384	32	256	52.2	20.40	10.20	5.06	2.67	1.39	0.80	0.55	0.47
16.384	64	128	26.1	14.5	7.27	3.49	1.80	0.97	0.57	0.40	0.34
16.384	128	64	13.1	9.80	4.97	2.49	1.28	0.67	0.40	0.28	0.24
16.384	256	32	6.5	6.95	3.32	1.75	0.88	0.48	0.28	0.22	0.19
13.107	32	204.8	41.8	21.46	10.81	5.73	3.18	2.04	1.49	1.30	1.17
13.107	64	102.4	20.9	14.30	7.43	3.99	2.07	1.39	1.04	0.92	0.86
13.107	128	51.2	10.4	10.45	5.20	2.76	1.51	0.95	0.76	0.65	0.61
13.107	256	25.6	5.2	7.31	3.86	1.95	1.07	0.70	0.54	0.47	0.45

NOISE PERFORMANCE

Table 37. Sinc3 RMS Noise Performance (µV rms) vs. ODR (IN2_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	32	256	67.0	48.00	24.40	12.30	6.05	3.02	1.66	0.89	0.63
16.384	128	64	16.7	11.79	5.98	3.07	1.80	1.12	0.84	0.73	0.70
16.384	512	16	4.2	6.07	3.04	1.60	0.90	0.58	0.43	0.37	0.36
16.384	2,048	4	1.05	3.05	1.50	0.85	0.47	0.29	0.22	0.20	0.19
16.384	8,192	1	0.26	1.68	0.93	0.46	0.28	0.16	0.12	0.12	0.11
16.384	163,840	0.05	0.013	1.08	0.73	0.25	0.12	0.08	0.08	0.06	0.07

AAF_GAIN = IN3_AAF

Table 38. Wideband Low-Ripple FIR Filter RMS Noise Performance (µV rms) vs. ODR (IN3_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	32	256	110.8	80.80	39.70	20.30	10.20	5.23	3.16	2.08	1.69
16.384	64	128	55.4	53.60	26.70	13.50	6.71	3.72	2.11	1.45	1.29
16.384	128	64	27.7	37.30	19.00	9.03	4.86	2.52	1.46	1.05	0.90
16.384	256	32	13.9	26.26	13.30	6.81	3.42	1.73	1.01	0.75	0.66
16.384	512	16	6.9	18.40	9.08	4.81	2.32	1.27	0.73	0.54	0.45
16.384	1,024	8	3.5	12.99	6.64	3.37	1.71	0.91	0.52	0.38	0.33
13.107	32	204.8	88.7	78.68	39.11	20.25	10.21	5.22	2.90	1.99	1.51
13.107	64	102.4	44.3	53.74	26.44	12.87	6.71	3.63	1.96	1.39	1.13
13.107	128	51.2	22.2	36.61	18.18	9.08	4.63	2.55	1.42	1.01	0.82
13.107	256	25.6	11.1	26.29	13.09	6.49	3.28	1.75	1.02	0.71	0.58

Table 39. Sinc5 RMS Noise Performance (µV rms) vs. ODR (IN3_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	8	1,024 (16-bit)	208.9	430.00	212.66	108.90	52.05	27.00	13.56	7.12	3.76
16.384	16	512	104.4	91.10	45.70	23.00	11.60	6.04	3.37	2.19	1.66
16.384	32	256	52.2	54.20	27.10	13.60	6.93	3.74	2.15	1.50	1.22
16.384	64	128	26.1	37.00	18.70	9.51	4.88	2.52	1.50	1.06	0.89
16.384	128	64	13.1	26.10	13.20	6.67	3.36	1.78	1.05	0.75	0.64
16.384	256	32	6.5	18.40	9.31	4.66	2.38	1.27	0.74	0.53	0.46
13.107	32	204.8	41.8	53.20	26.00	13.90	6.65	3.68	1.98	1.39	1.14
13.107	64	102.4	20.9	35.91	18.70	9.46	4.66	2.41	1.41	0.99	0.82
13.107	128	51.2	10.4	26.20	12.90	6.41	3.37	1.71	0.97	0.71	0.57
13.107	256	25.6	5.2	18.11	9.35	4.54	2.40	1.21	0.69	0.49	0.42

NOISE PERFORMANCE

Table 40. Sinc3 RMS Noise Performance (µV rms) vs. ODR (IN3_AAF, V_{REF} = 4.096V, f_{MOD} = MCLK/2)

MCLK (MHz)	DEC_RATE	ODR (kSPS)	−3dB Bandwidth (kHz)	RMS Noise Performance (µV rms)							
				PGA_GAIN = 1	PGA_GAIN = 2	PGA_GAIN = 4	PGA_GAIN = 8	PGA_GAIN = 16	PGA_GAIN = 32	PGA_GAIN = 64	PGA_GAIN = 128
16.384	32	256	67.0	134.43	64.75	33.85	16.45	8.30	4.47	2.49	1.65
16.384	128	64	16.7	29.47	15.34	7.76	3.80	2.03	1.01	0.85	0.71
16.384	512	16	4.2	15.03	7.47	3.63	1.92	1.04	0.57	0.43	0.36
16.384	2,048	4	1.05	7.39	3.75	1.94	0.99	0.52	0.32	0.22	0.19
16.384	8,192	1	0.26	4.65	2.06	1.05	0.57	0.28	0.17	0.12	0.10
16.384	163,840	0.05	0.013	2.15	1.11	0.51	0.25	0.15	0.08	0.05	0.04

DIGITAL INTERFACE

The ADAQ7769-1 has a 4-wire SPI. The interface operates in SPI Mode 3. In SPI Mode 3, SCLK idles high, the first data is clocked out on the first falling or drive edge of SCLK, and data is clocked in on the rising or sample edge. Figure 157 and Figure 158 show SPI Mode 3 operation where the falling edge of SCLK is driving out the data and the rising edge of SCLK is when the data is sampled.

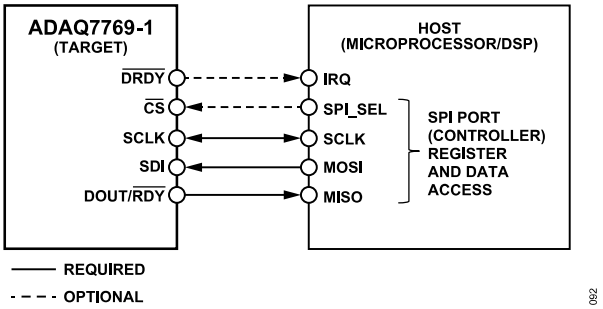

Figure 157. Basic Serial Port Connection Diagram

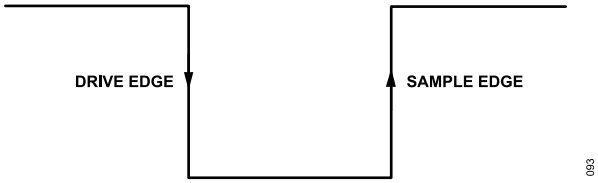

Figure 158. SPI Mode 3

DIGITAL INTERFACE

SPI READING AND WRITING

To use SPI control mode, set the PIN/SPI pin high. The SPI control operates as a 4-wire interface, which allows read and write access. In systems where CS can be connected low, such as those requiring isolation, the ADAQ7769-1 can operate in a 3-wire configuration. Figure 157 shows a typical connection between the ADAQ7769-1 and the digital host. The corresponding 3-wire interface involves tying the CS pin low and using SCLK, SDI, and DOUT/RDY.

The format of the SPI read or write is shown in Figure 159. The MSB is the first bit in both read and write operations. An active low-frame start signal (FS) begins the transaction, followed by the R/W bit that determines if the transaction being carried out is to a read (1) or a write (0). The next six bits are used for the address, and the eight bits of data to be written follow. All registers in the ADAQ7769-1 are 8 bits in width, except for the ADC_DATA register (Register 0x2C), which is 24 bits in width. In the case where CS is connected low, the last SCLK rising edge completes the SPI transaction and resets the interface. When reading back data with CS held low, it is recommended that SDI idle high to prevent an accidental reset of the device where SCLK is free running (see the Reset section).

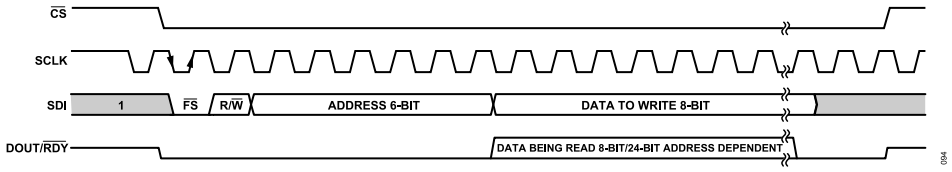

Figure 159. SPI Basic Read and Write Frame

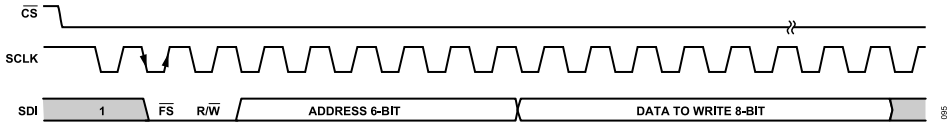

Figure 160. 3-Wire SPI Write Frame (CS = 0)

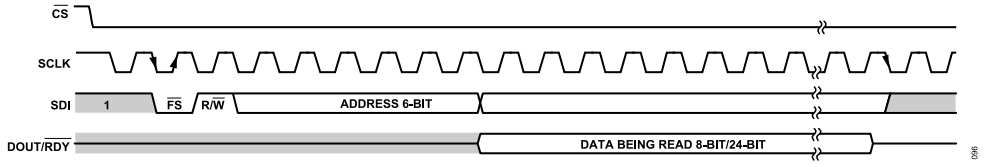

Figure 161. 3-Wire SPI Read Frame (CS = 0)

DIGITAL INTERFACE

SPI CONTROL INTERFACE ERROR HANDLING

The ADAQ7769-1 SPI control interface detects if an illegal command is received. An illegal command is a write to a read only register, a write to a register address that does not exist, or a read from a register address that does not exist. If any of these illegal commands are received by the ADAQ7769-1, error bits are set in the SPI_DIAG_STATUS register (Register 0x2E), see the SPI Error Register section.

Five sources of SPI error can be detected. These detectable error sources must be enabled in the SPI_DIAG_ENABLE register (Register 0x28), see the SPI Diagnostic Control Register section. Only the EN_ERR_SPI_IGNORE bit (Register 0x28, Bit 4) error is enabled on startup.

The five detectable sources of SPI error are as follows:

- SPI CRC error. This error occurs when the received CRC/XOR does not match the calculated CRC/exclusive OR (XOR).
- SPI read error. This error occurs when an incorrect read address is detected (for example, when the user attempts to access a register that does not exist).
- SPI write error. This error occurs when a write to an incorrect address is detected (for example, when the user attempts to write to a register that does not exist).
- SPI clock count error. When the SPI transaction is controlled by $\overline{CS}$, this error flags when the SPI clock count during the frame is not equal to 8, 16, 24, 32, or 40. This error can be detected in both continuous read mode and normal SPI mode.
- SPI ignore error. This error flags when an SPI transaction is attempted before initial power-up completes.

All SPI errors are sticky, meaning they can only be cleared if the user writes a 1 to the corresponding error location.

CRC CHECK ON SERIAL INTERFACE

The ADAQ7769-1 can deliver up to 40 bits with each conversion result, which consists of 24 bits of data and 8 status bits, with the option to add 8 further CRC/XOR check bits in the SPI mode only.

The status bits default per the description in the Status Header section. The CRC functionality is available only when operating in SPI control mode. When the CRC functionality is in use, the CRC message is calculated internally by the ADAQ7769-1. The CRC is then appended to the conversion data and optional status bits.

The ADAQ7769-1 uses a CRC polynomial to calculate the CRC message. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

To generate the checksum, shift the data by 8 bits to create a number ending in 8 Logic 0s.

The polynomial is aligned such that the MSB is adjacent to the leftmost Logic 1 of the command bits and register data. For example, when reading the ADC_DATA register containing 0xABCDEF, the following:

Initial Value = Frame Start Bit + R/W Bit + ADDR[5:0] + ADC_DATA[23:0]

Initial Value = 0x6CABCDEF

Apply an XOR function to the data to produce a new, shorter number. The polynomial is again aligned such that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum. In the example above, the CRC checksum = 0x9E.

If enabled, the SPI writes always use CRC, regardless of whether the XOR option is selected in the INTERFACE_FORMAT register (Register 0x14), see the Interface Format Control Register section. The initial CRC checksum for SPI transactions is 0x00, unless reading back data in continuous read mode, in which case, the initial CRC is 0x03.

If using the XOR option in continuous read mode, the initial value is set to 0x6C. The XOR option is only available for SPI reads.

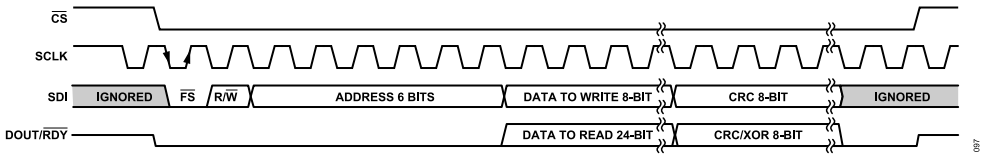

Figure 162. Data Output Format when using CRC

DIGITAL INTERFACE

Example of a Polynomial CRC Calculation (24-Bit Word: 0x654321 (8 Command Bits and 16-Bit Data))

An example to generate the 8-bit checksum using the polynomial-based checksum is as follows:

```
011001010100001100100001          = Initial Value
011001010100001100100001000000000 left shifted eight bits
 100000111                        = x^8 + x^2 + x + 1 polynomial value
  100100100000110010000100000000  XOR result
  100000111                       polynomial value
     100011000110010000100000000  XOR result
     100000111                    polynomial value
         111111100100001000000000  XOR result
         100000111                 polynomial value
          11111011100001000000000  XOR result
          100000111                polynomial value
           11110000000100000000  XOR result
           100000111               polynomial value
            1110011100010000000  XOR result
            100000111               polynomial value
             1100100100100000000  XOR result
             100000111               polynomial value
              100101010100000000  XOR result
              100000111           polynomial value
                 101101100000000  XOR result
                 100000111        polynomial value
                   1101011000000  XOR result
                   100000111      polynomial value
                    101010110000  XOR result
                    100000111     polynomial value
                      1010001000  XOR result
                      100000111   polynomial value
                        10000110  XOR result; checksum = 0x86
```

Example of an XOR Calculation (24-Bit Word: 0x654321 (8 Command Bits and 16-Bit Data))

Using the previous example, divide into 3 bytes (0x65, 0x43, and 0x21) as follows:

```
01100101 0x65
01000011 0x43
00100110 XOR result
00100001 0x21
00000111 XOR result; checksum = 0x07
```

DIGITAL INTERFACE

CONVERSION READ MODES

The digital interface of the ADAQ7769-1 is a 4-wire SPI implementation operating in Mode 3 SPI. An 8-bit write instruction is needed to access the memory map address space. All registers are 8-bits wide, with the exception of the ADC data register. The ADAQ7769-1 operates in a continuously converting mode by default. The user must decide whether to read the data. Two read modes are available to access the ADC conversion results: single-conversion and continuous read mode.

Single-conversion read mode is a basic SPI read cycle where the user must write an 8-bit instruction to read the ADC data register. The status register must be read separately, if required.

Write a 1 to the LSB of the Interface Format Control Register (Register 0x14) to enter continuous read mode. Subsequent data reads do not require an initial 8-bit write to query the ADC_DATA register. Simply provide the required number of SCLKs for continuous readback of the data. Single-Conversion Read Mode shows an SPI read in continuous read mode.

Key considerations for users on the interface are as follows:

- Conversion data is available for readback after the rising edge of $\overline{DRDY}$. In continuous read mode, the $\overline{RDY}$ function can be enabled, and the $\overline{DRDY}$ function can be ignored. Data is available for readback on the falling edge of $\overline{RDY}$.
- The ADC conversion data register is updated internally 1 MCLK period prior to the rising $\overline{DRDY}$ edge.
- MCLK has a maximum frequency of 16.384MHz.
- SCLK has a maximum frequency of 20MHz.
- The $\overline{DRDY}$ high time is 1 × t_{MCLK}.
- In fast-power mode, decimate by 32, the $\overline{DRDY}$ period is ~4µs, the fastest conversion can have a $\overline{DRDY}$ period of 1µs.
- The $\overline{CS}$ rising edge resets the serial data interface. If $\overline{CS}$ is connected low, the final rising SCLK edge of the SPI transaction resets the serial interface. The point at which the interface is reset corresponds to 16 × SCLKs for a normal read operation and up to 40 SCLKs when reading back ADC conversion data, plus the status and CRC headers.

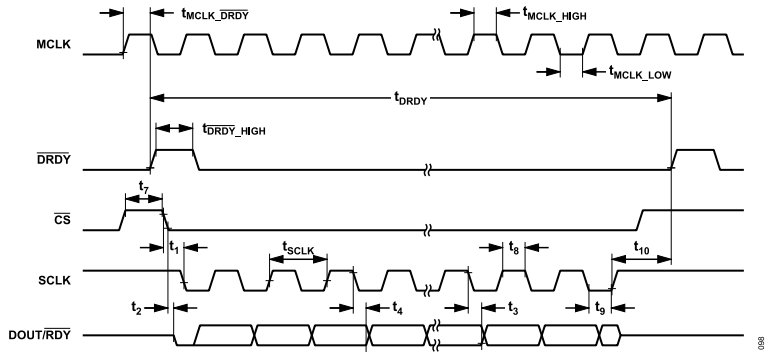

Figure 163. Serial Interface Timing Diagram, Example Reflects Reading an ADC Conversion in Continuous Read Mode

DIGITAL INTERFACE

Single-Conversion Read Mode

When using single-conversion read mode, the ADC_DATA register can be accessed in the same way as a normal SPI read transaction. The ADC_DATA register (Register 0x2C), is 24 bits wide, see the Conversion Result Register section. Therefore, 32 SCLKs are required to read a conversion result.

Continuous Read Mode

To eliminate the overhead of needing to write a command to read the ADC data register each time, the user can place the ADC in continuous read mode so that the ADC register can be read directly after the data ready signal is pulsed (see Figure 163). In continuous read mode, data is output on the falling edge of the first SCLK received. Therefore, only 24 SCLKs are required to read a conversion. In this continuous read mode, it is also possible to append one or both of the status or CRC headers (8 bits each) to the conversion result. If both the status and CRC headers are enabled, the data format is ADC data + status bits + CRC.

When the $\overline{RDY}$ function is not used, the ADC conversion result can be read multiple times in the $\overline{DRDY}$ period, as shown in Figure 164. When the $\overline{RDY}$ function is enabled, the DOUT/$\overline{RDY}$ pin goes high after reading the ADAQ7769-1 conversion result and, therefore, the data cannot be read more than once (see Figure 165). The $\overline{RDY}$ function can be enabled by setting a logic low to EN_RDY_DOUT bit (Register 0x14, Bit 2) of the Interface Format Control Register.

Continuous readback is the readback mode used in $\overline{PIN}$ control mode. However, in this mode, the data output format is fixed, and there is no option for $\overline{RDY}$ on the DOUT pin. For more details, see the PIN Control Mode Overview section.

When using continuous read mode with the LV_BOOST bit enabled (Bit 7 in the Interface Format Control Register, Register 0x14), it is necessary to reenable LV_BOOST each time continuous read mode is exited.

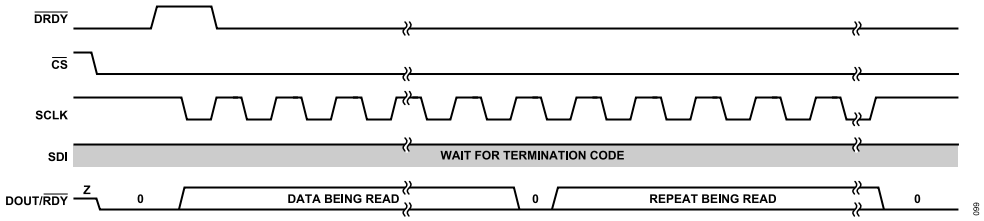

Figure 164. Continuous ADC Read Data Format with $\overline{RDY}$ Function Disabled

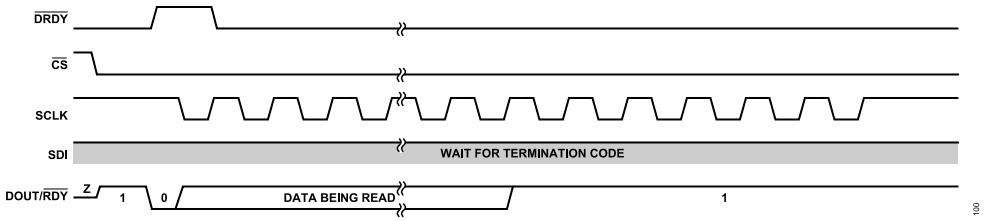

Figure 165. Continuous ADC Read Data Format with $\overline{RDY}$ Function Enabled on the DOUT/$\overline{RDY}$ Pin

DIGITAL INTERFACE

Exiting Continuous Read Mode

To exit continuous read mode, write a key of 0x6C on the SDI, which allows access to the register map one more time and that allows further configuration of the device. To comply with a normal SPI write, use the $\overline{CS}$ signal to reset the SPI after this key is entered. If $\overline{CS}$ cannot be controlled and is permanently held low, 16 SCLKs are required to complete the transaction so that the SPI remains synchronized. For example, when $\overline{CS}$ is permanently connected low, write 0x006C to exit continuous read mode when using the 3-wire version of the interface. The exit command must be written between $\overline{DRDY}$ pulses to ensure that the device exits correctly.

A software reset can also be written in this mode in the same way as the exit command, but by writing 0xAD instead of 0x6C.

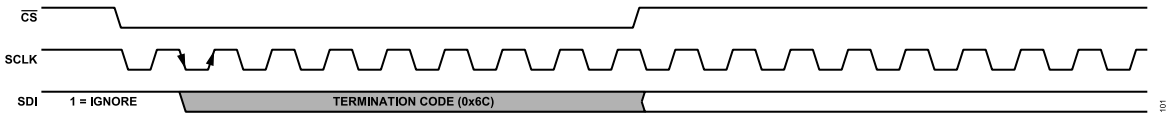

Figure 166. Exiting Continuous Read Mode ($\overline{CS}$ Toggling)

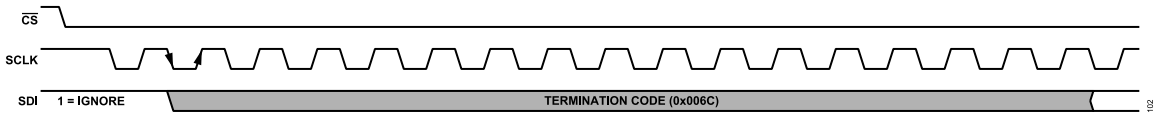

Figure 167. Exiting Continuous Read Mode ($\overline{CS}$ = 0)

DATA CONVERSION MODES

The four data conversion modes available in SPI control mode are as follows:

- Continuous conversion.
- One-shot conversion.
- Single conversion.
- Duty-cycled conversion.

The default conversion mode is continuous conversion. Write to the CONV_MODE bits (Register 0x18, Bits[2:0]) of the Conversion Source Select and Mode Control Register to change the conversion mode. A $\overline{\text{SYNC\_IN}}$ pulse must be provided to the ADAQ7769-1 after any change to the configuration of the device, including changing filter settings and data conversion modes.

CONTINUOUS CONVERSION MODE

In continuous conversion mode, the ADC continuously converts and a new ADC result is ready at an interval determined by the ODR, which is the default conversion operation in SPI control mode, and the only data conversion mode in which the wideband low-ripple FIR filter is available. Two methods of data readback are available to the user in SPI control mode and shown in the Conversion Read Modes section.

ONE-SHOT CONVERSION MODE

Figure 168 shows the device operating in one-shot conversion mode. In this mode, conversions occur on request by the controller device, for example, the DSP or FPGA. The $\overline{\text{SYNC\_IN}}$ pin receives the command initiating the data output.

In one-shot conversion mode, the ADC runs continuously. However, the $\overline{\text{SYNC\_IN}}$ pin rising controls the point in time from which data is output.

To receive data, the controller device must pulse the $\overline{\text{SYNC\_IN}}$ pin, which resets the filter and forces $\overline{\text{DRDY}}$ low. $\overline{\text{DRDY}}$ subsequently goes high to indicate to the controller device that the device has valid settled data available.

When the controller asserts $\overline{\text{SYNC\_IN}}$ and the ADAQ7769-1 receives the rising edge of this signal, the digital filter is reset, the full settling time of the filter elapses before the data is settled, and the output is available. The duration of the settling time depends on the filter path and decimation rate. One-shot conversion mode is only available for use with the Sinc5 or Sinc3 filters because these filters feature a minimal settling time. One-shot conversion mode is not available as an option for use with the wideband low-ripple FIR filter.

When settled data is available, the $\overline{\text{DRDY}}$ signal pulses. The time from the $\overline{\text{SYNC\_IN}}$ signal until the ADC path settles data ($t_{SETTLED}$) is shown in Figure 168. After settled data is available, $\overline{\text{DRDY}}$ is asserted high, and the user can read the conversion result. The device then waits for another $\overline{\text{SYNC\_IN}}$ signal before outputting more data.

The settling time is calculated relative to the settling time of the filter used, with some added latency for starting the one shot conversion. This settling time limits the overall throughput achievable in one-shot conversion mode.

Because the ADC is sampling continuously, one-shot conversion mode affects the sampling theory of the ADAQ7769-1. Periodically sending a $\overline{\text{SYNC\_IN}}$ pulse to the device is a form of subsampling of the ADC output. The bandwidth around this subsampling rate can now alias down to the baseband. Consider keeping the $\overline{\text{SYNC\_IN}}$ pulse synchronous with the controller clock to ensure coherent sampling and to reduce the effects of jitter on the frequency response, which otherwise heavily distort the output.

Any SPI configuration of the ADAQ7769-1 required is performed in continuous conversion mode before switching back to one-shot conversion mode.

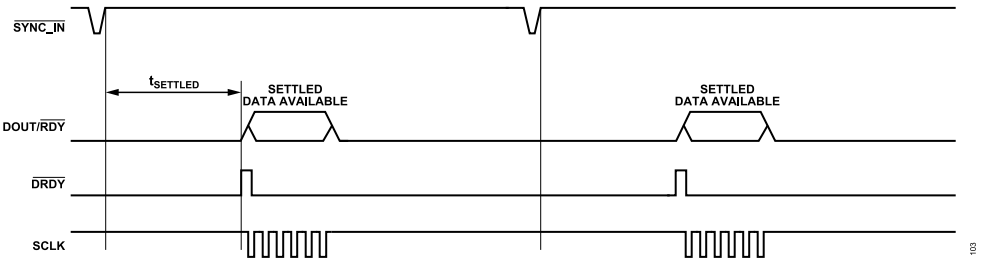

Figure 168. One-Shot Conversion Mode, $\overline{\text{SYNC\_IN}}$ Pin Driven with an External Source

DATA CONVERSION MODES

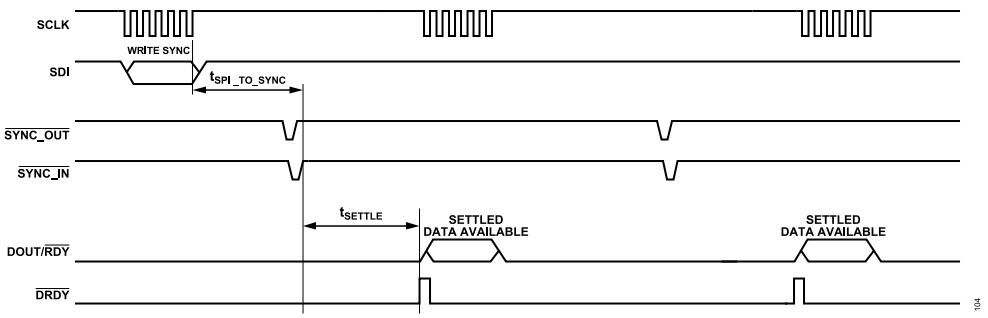

Figure 169. One-Shot Conversion Mode, SYNC_IN Pulse Initiated by a Register Write

SINGLE-CONVERSION MODE

In single-conversion mode, the ADC wakes up from standby, performs a conversion, and then returns to standby. Only use single-conversion mode when operating in low-power and median-power modes. The user must send a command to initiate the read and subsequently read back the ADC conversion result. Use a toggle of the SYNC_IN pin to exit the device from standby and to start a new conversion.

If M0_ADC and M1_ADC is connected to M0_FDA and M1_FDA, the FDA is automatically put in standby when the ADC is in standby (see the Fully-Differential Amplifier (FDA) Power Mode section).

Any SPI configuration of the ADAQ7769-1 required must be performed in continuous conversion mode before then switching back to single-conversion mode.

DUTY-CYCLED CONVERSION MODE

In duty-cycled conversion mode, the ADC wakes up from standby, performs a conversion, and then returns to standby. The user can set the period between each conversion, and the ADC automatically performs the single conversion before returning to standby, repeating the single conversion performed by the ADC at a period specified by the user. Only use duty-cycled conversion mode when operating in low-power and median-power modes. Duty-cycled conversion mode allows a method to reduce the power consumption for DC point conversions, and to eliminate any overhead in timing and initiating the conversion.

Use a toggle of the SYNC_IN pin to begin the duty-cycled conversion mode sequence. DRDY toggles once when a settled result is reached. Then, the device enters standby one more time. The Periodic Conversion Rate Control Register (Register 0x1C) controls the determined idle time.

If M0_ADC and M1_ADC is connected to M0_FDA and M1_FDA, the FDA is automatically put in standby when the ADC is in standby (see the Fully-Differential Amplifier (FDA) Power Mode section).

Any SPI configuration of the ADAQ7769-1 required must be performed in continuous conversion mode before switching back to duty-cycled conversion mode.

SYNCHRONIZATION OF MULTIPLE ADAQ7769-1 DEVICES

Synchronization is an important consideration when using multiple ADAQ7769-1 devices in a system. The basic provision for synchronizing multiple devices is that each device is clocked with the same base MCLK signal. Provide a $\overline{\text{SYNC\_IN}}$ pulse to the ADAQ7769-1 both after power-up and after any change to the configuration of the device. This pulse flushes out the digital filters and ensures that the device is in a known configuration, as well as synchronizing multiple devices in a system.

The ADAQ7769-1 has three options to ease system synchronization. Choosing among the options depends on the system. However, the most basic consideration is whether the user can supply a synchronization pulse that is truly synchronous with the base MCLK signal.

If a signal that is synchronous to the base MCLK signal cannot be provided, use one of the following methods:

- Configure the GPIOx pin of one of the ADAQ7769-1 devices in the system to be a $\overline{\text{START}}$ input. Apply a $\overline{\text{START}}$ pulse to the configured GPIOx pin. Route the $\overline{\text{SYNC\_OUT}}$ pin output to the $\overline{\text{SYNC\_IN}}$ input of that same device and all other devices to be synchronized. The ADAQ7769-1 samples the asynchronous $\overline{\text{START}}$ pulse and generates a $\overline{\text{SYNC\_OUT}}$ pulse related to the base MCLK signal for local distribution.
- Use synchronization over SPI (only available in the SPI control mode, see Figure 153). Write a synchronization command to one predetermined ADC device. Connect the $\overline{\text{SYNC\_OUT}}$ pin of this device to its own $\overline{\text{SYNC\_IN}}$ pin and to the $\overline{\text{SYNC\_IN}}$ pin of any other device locally. Similar to the $\overline{\text{START}}$ pin method, the SPI synchronization is received by one device and, subsequently, the $\overline{\text{SYNC\_OUT}}$ signal is routed to local devices to allow synchronization.

If a $\overline{\text{SYNC\_IN}}$ signal synchronous to the base MCLK can be provided, apply the $\overline{\text{SYNC\_IN}}$ synchronous signal to the $\overline{\text{SYNC\_IN}}$ pin from a star point and connect directly to the pin of each ADAQ7769-1 device. The $\overline{\text{SYNC\_IN}}$ signal is sampled on the rising MCLK edge and, therefore, setup and hold times are associated with the $\overline{\text{SYNC\_IN}}$ input relative to the ADAQ7769-1 MCLK rising edge (see Figure 7).

In this case, $\overline{\text{SYNC\_OUT}}$ is redundant and can remain open-circuit or connected to VDD_IO. GPIOx can be used for a different purpose because it is not required for the $\overline{\text{START}}$ function. Figure 170 shows synchronization in channel-to-channel isolated systems.

It is recommended to perform synchronization functions directly after the $\overline{\text{DRDY}}$ pulse. If the ADAQ7769-1 $\overline{\text{SYNC\_IN}}$ pulse occurs too close to the upcoming $\overline{\text{DRDY}}$ pulse edge, the upcoming $\overline{\text{DRDY}}$ pulse may still be output because the $\overline{\text{SYNC\_IN}}$ pulse has not yet propagated through the device.

When using the $\overline{\text{SYNC\_OUT}}$ function with a VDD_IO voltage of 1.8V, it is recommended to set the $\overline{\text{SYNC_OUT}}$_POS_EDGE bit (Register 0x1D, Bit 6) shown in the Synchronization Modes and Reset Triggering Register to 1.

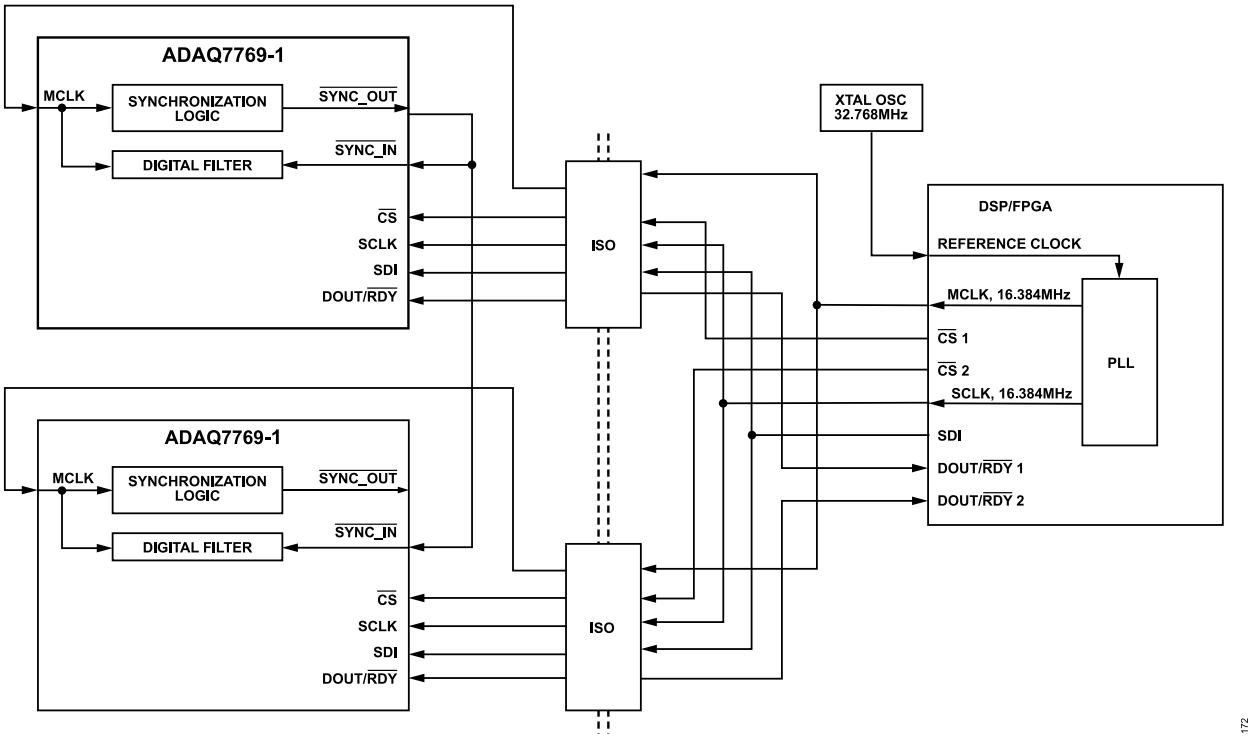

Figure 170. Synchronization in Channel-to-Channel Isolated Systems

ADDITIONAL FUNCTIONALITY OF THE ADAQ7769-1

RESET

After powering up the device, it is recommended to perform a full reset. There are multiple options available on the ADAQ7769-1 to perform a reset, which include:

- Using the dedicated $\overline{\text{RESET}}$ pin. For more details, see the Pin Configurations and Function Descriptions section.
- When in continuous read mode, the ADAQ7769-1 monitors for the exit command or a reset command of 0xAD. For more details, see the Conversion Read Modes section.
- A software reset can be performed by two consecutive writes to the Synchronization Modes and Reset Triggering Register (Register 0x1D).
- When $\overline{\text{CS}}$ is held low, it is possible to provide a reset by clocking in a 1 followed by 63 zeros on SDI, which is the SPI resume command reset function used to exit power-down mode.

The time taken from $\overline{\text{RESET}}$ to an SPI write must be at least 200µs.

STATUS HEADER

In SPI control mode, the status header can be output after the conversion result when operating the ADAQ7769-1 in continuous readback mode. The status header mirrors the MASTER_ STATUS register (Register 0x2D) shown in the Device Error Flags Main Register section.

In $\overline{\text{PIN}}$ control mode, the status header is output by default after the conversion result. The status header contains the following bits and functions:

- The MASTER_ERROR bit is an OR of all other errors present and can be monitored to provide a quick indication of a problem having occurred.
- The ADC_ERROR bit sets to 1 if any error is present in the ADC Diagnostics Output Register (Register 0x2F). It is an OR of the error bits in the ADC Diagnostics Output Register register.
- The DIG_ERROR bit sets to 1 if any error is present in the Digital Diagnostics Output Register (Register 0x30). It is an OR of the error bits in the Digital Diagnostics Output Register register.
- The ERR_EXT_CLK_QUAL bit (Register 0x2D, Bit 4 and Register 0x2F, Bit 0) sets if a valid clock is not detected (see the Clock Qualification section).
- The FILT_SATURATED bit (Register 0x2D, Bit 3 and Register 0x2F, Bit 2) sets to 1 if the digital filter is clipped on either positive or negative full scale. The clipping can be caused by the analog input exceeding the analog input range, or by a large step input to the device that causes a large overshoot in the digital filter. In addition, the filter may saturate if the ADC gain registers are incorrectly set. The combination of a full-scale signal and a large gain saturates the digital filter.
- The FILT_NOT_SETTLED bit (Register 0x2D, Bit2 and Register 0x2F, Bit 1) is set to 1 if the output of the digital filter is not settled. The digital filters are cleared following a $\overline{\text{RESET}}$ pulse, or after a $\overline{\text{SYNC\_IN}}$ command is received. Table 20, Table 21, and Table 26 list the time for $\overline{\text{SYNC\_IN}}$ to settled data for each filter type. When using the wideband low-ripple FIR filter, the FILT_NOT_SETTLED bit takes longer to update and propagate through the device than to read the status header. The FILT_NOT_SETTLED bit appears set when in fact the data output is settled. The worst-case update delay is 128 MCLK cycles for the wideband low-ripple FIR filter, decimate by 1024 setting. In this case, if the readback is delayed by 128 MCLK cycles, the filter not settled bit has time to update, and the time to settled data is equal to the data shown in Table 20, Table 21, and Table 26.
- The SPI_ERROR bit (Register 0x2D, Bit 1) sets to 1 if any error is present in the SPI Error Register (Register 0x2E). The bit is an OR of the error bits in the SPI Error Register.
- The POR_FLAG bit (Register 0x2D, Bit 0) detects if a reset or a temporary supply brown out occurred. In $\overline{\text{PIN}}$ control mode, instead of being the POR flag, this bit is always set to 1 and then detects if that the interface is operating correctly.

DIAGNOSTICS

Internal diagnostics are available on the ADAQ7769-1 that allow the user to check both the functionality of the ADC and the environment in which the ADC is operating. The internal diagnostics are enabled in the conversion register shown in the Conversion Source Select and Mode Control Register (Register 0x18). To use the diagnostics, the device must be configured to eco mode, MCLK_DIV = MCLK/16, and the linearity boost buffers must be enabled. The diagnostics available are as follows:

- The temperature sensor is an on-chip temperature sensor that determines the approximate temperature. Temperature changes measured give approximately a 0.6mV/°C, referred to output (RTO), change in the DC converted voltage. For example, at ambient temperature, the conversion result is approximately 180mV (RTO, ADC_DATA approximately = 0x059FFF). A 50°C increase in temperature reads back as approximately 210mV (RTO, ADC_DATA approximately = 0x068FFF), signaling, for example, a potential fault or the need to calibrate the system.
- The ADC input short disconnects the input pins of the core ADC from the FDA and creates an internal short across the core ADC input.
- The voltage converted is V_{REF+} for positive full scale, if selected.
- The voltage converted is V_{REF-} for negative full scale, if selected.

APPLICATIONS INFORMATION

CONDITION-BASED MONITORING (CBM) APPLICATION

A common application of the ADAQ7769-1 is CbM using piezoelectric sensors. In the application shown in Figure 171, an integrated electronics piezoelectric (IEPE) sensor can be interfaced with the ADAQ7769-1 with the use of ADG5421F as a fault protection switch and LT3092 as a current source to bias the sensor. A 3-wire negative voltage accelerometers have a slightly different interface, as shown in Figure 172. Whenever a voltage source is used to test the signal chain, the current source must be disconnected through the switch. These application solutions are designed to convert a unipolar input from either 0V to +24V or −24V to 0V by simply changing the power supply levels of the switch, current source, and PGA. In this setup, the PGA of ADAQ7769-1 is set at PGA_GAIN = 1 and connected to the IN3_AAF inputs. The excellent DC performance of the ADAQ7769-1 allows the sensors to be DC-coupled to the system and converts the signals with precision in the sub-Hz frequencies.

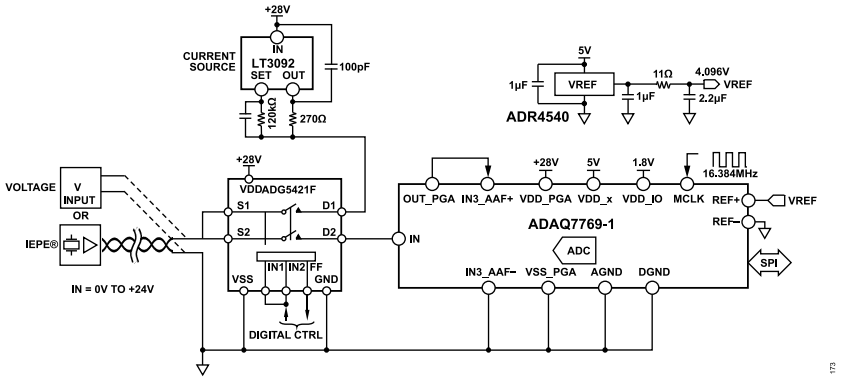

Figure 171. DC-Coupled IEPE Sensor Application, IN = 0V to +24V, PGA_GAIN = 1, IN3_AAF

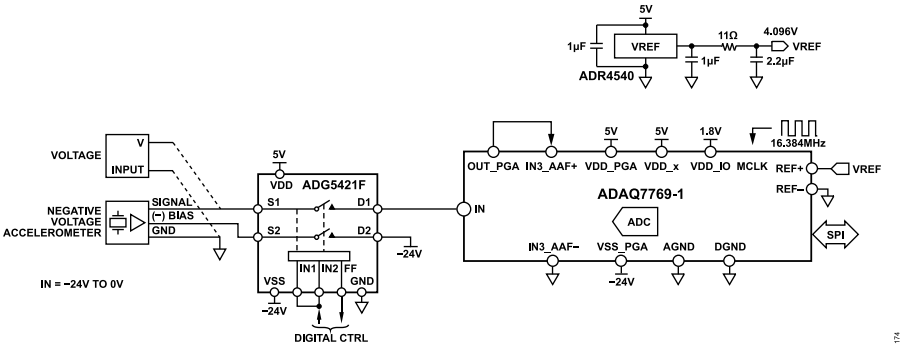

Figure 172. DC-Coupled, 3-Wire Negative Voltage Accelerometer Application, IN = −24V to 0V, PGA_GAIN = 1, IN3_AAF

ANALOG INPUTS

The ADAQ7769-1 can accept a wide range and different types of inputs. Figure 173 shows how varying the PGA supplies when using IN3_AAF can shift the wide input range into a 24Vpp positive unipolar swing, 32Vpp bipolar swing, and a 24Vpp negative unipolar swing. This allows the ADAQ7769-1 to work well with sensors of varying biases. Following this is the circuit connection for smallest full-scale bipolar input of ±32mV, as shown in Figure 174. With a TOTAL_GAIN up to 128, ADAQ7769-1 offers additional system dynamic range and improved signal chain noise performance for input signals of lower amplitude. Bypassing the PGA is also an option, as shown in Figure 175. This provision allows the user to connect the AAF and ADC stage to a preferred input op amp or PGA, or directly to a low output impedance sensor with a differential signal output. As a differential input circuit, the three AAF input pairs have varying differential input ranges and a common-mode input ranges. Figure 175 shows the differential and common-mode input range of IN3_AAF.

APPLICATIONS INFORMATION

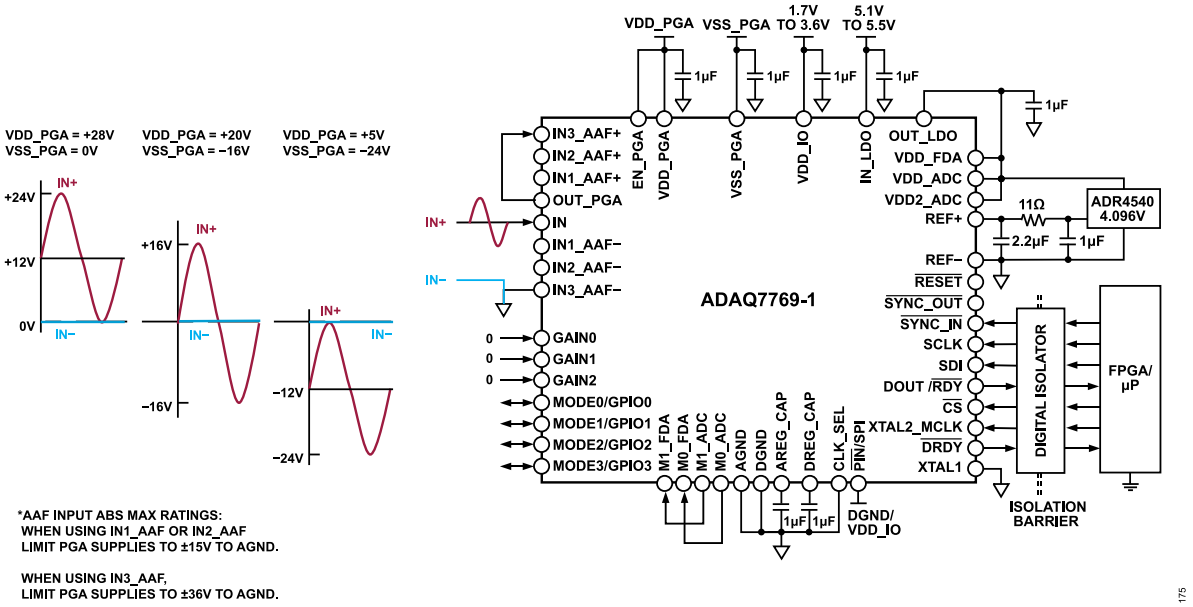

Figure 173. ADAQ7769-1 Linear Voltage Ranges vs. PGA Supply Voltages, using PGA_Gain = 1, IN3_AAF

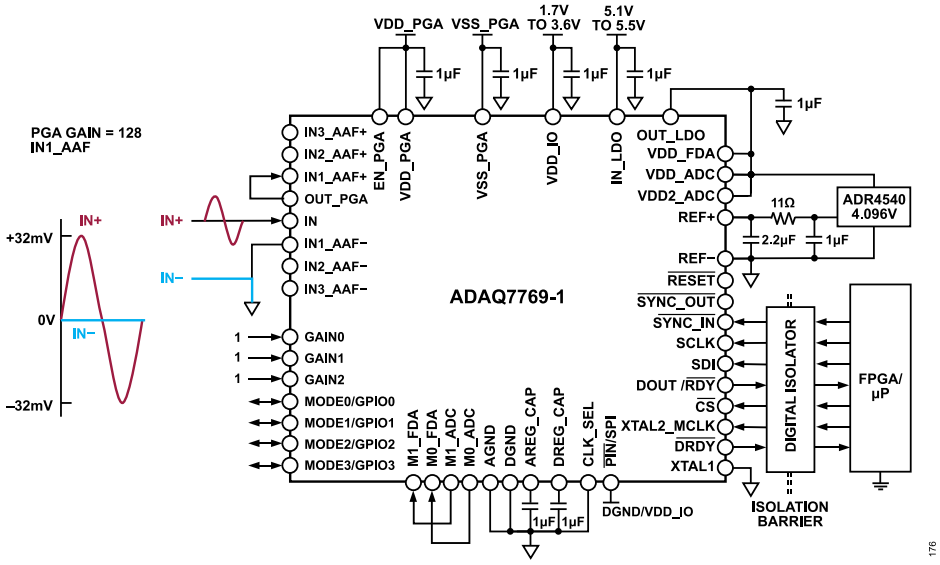

Figure 174. ADAQ7769-1 Smallest Full-Scale Voltage (±32mV), using PGA_Gain = 128, IN1_AAF

APPLICATIONS INFORMATION

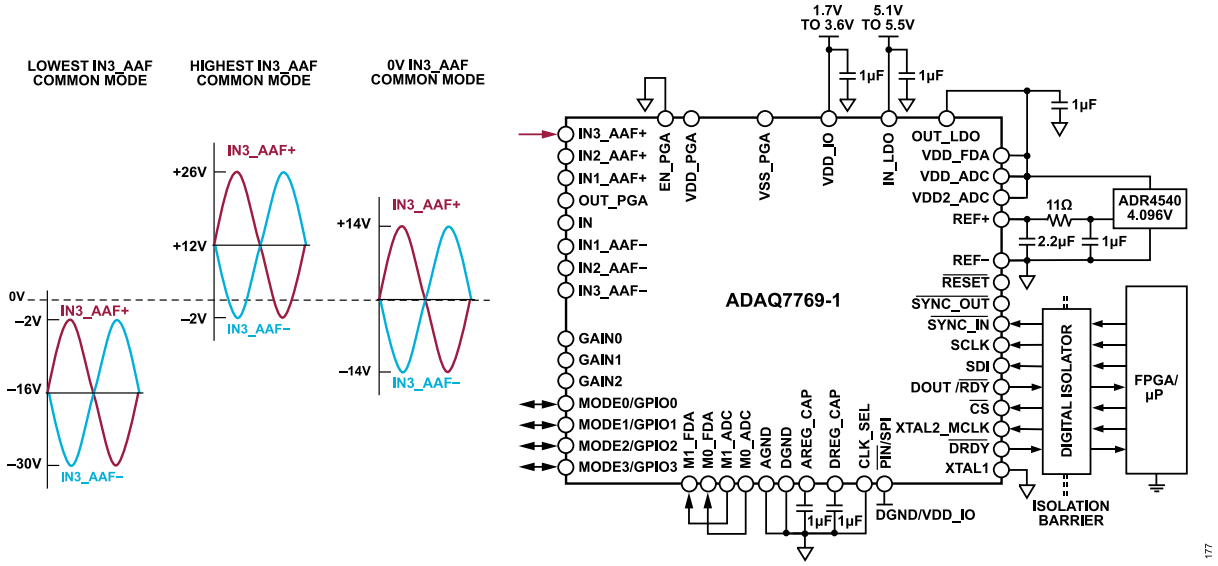

Figure 175. ADAQ7769-1 with the PGA Bypassed, applying Differential Input to IN3_AAF

APPLICATIONS INFORMATION

SENSOR INTERFACING

The applications diagram in Figure 176 shows how the ADAQ7769-1 is typically used with a single sensor. In the application, a fixed PGA gain may be set by the user if the sensor operates at a certain voltage level or it may be dynamically changed if the input amplitude settles at different levels for a period of time.

Figure 177 shows how the user may also use the ADAQ7769-1 using multiple sensors. In this case, an external multiplexer can be used to select from the different sensors. The PGA's GAIN pins can be linked to a logic controller or FPGA to vary accordingly with MUX select lines. In SPI mode, the ADAQ7769-1 features GPIO pins, which can be connected to the GAIN pins to set the PGA gain.

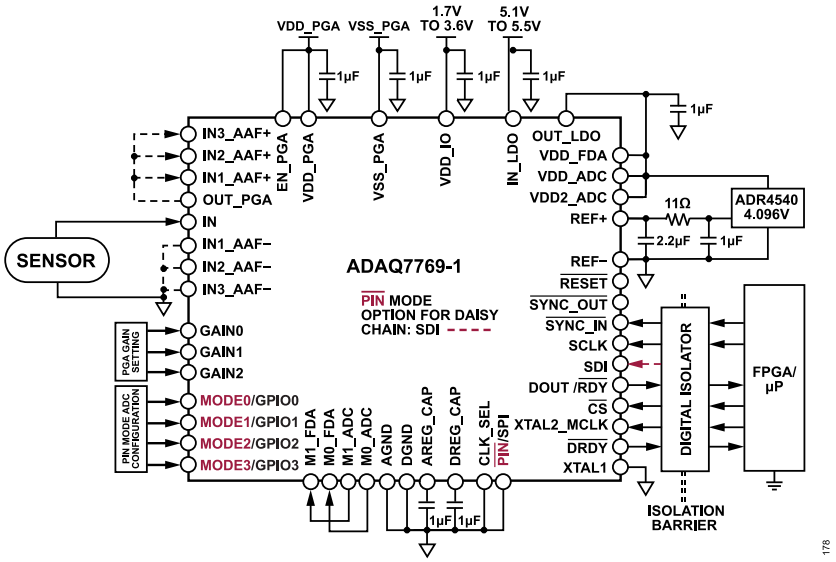

Figure 176. Typical Applications Diagram of DAQ System involving One Sensor Input and PIN Mode

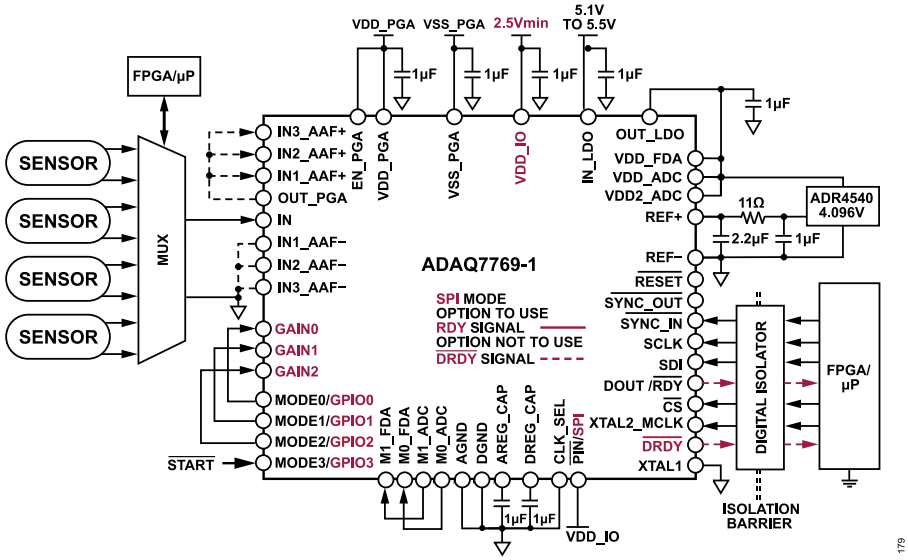

Figure 177. Typical Applications Diagram of DAQ System involving Multiple Sensor Inputs and SPI Mode

APPLICATIONS INFORMATION

$\overline{\text{PIN}}$ AND SPI CONTROL MODES

$\overline{\text{PIN}}$ Control Mode

The ADAQ7769-1 can be configured in either $\overline{\text{PIN}}$/SPI Mode, whose distinct advantages are shown in the Device Configuration Method section. One of the advantages of $\overline{\text{PIN}}$ Mode is shown in Figure 176, wherein the MODEx pins are used to set the ADC configurations such as f_{MOD} frequency, type of digital filter, and decimation rate from a list of predetermined modes, as shown in Table 28. This ability allows the user to make an easier choice of ADC configuration and eliminates the need to write to the ADC registers that control these configurations. Since a write is not allowed, the SDI pin can be used for daisy-chaining, which is only available in $\overline{\text{PIN}}$ control mode. To use the $\overline{\text{PIN}}$ control mode, ground the $\overline{\text{PIN}}$/SPI pin on startup.

SPI Control Mode

Figure 177 shows an application in SPI control mode, wherein the user utilizes the GPIOs, in this case, to control the gain of the PGA. This can be done by configuring the GPIO Port Control Register (Register 0x1E) and GPIO Output Control Register (Register 0x1F). The SPI mode also allows the complete flexibility in ADC configurations, conversion read modes, and data conversion modes. The SPI control mode in continuous read mode may use the $\overline{\text{RDY}}$ signal, which can be enabled through the Interface Format Control Register (Register 0x14), to merge the indication of new ADC data with the DOUT output stream, which eliminates the need for a digital line for $\overline{\text{DRDY}}$. To use SPI control mode, the $\overline{\text{PIN}}$/SPI pin must be connected to high (or VDD_IO) on startup.

POWER SUPPLIES

The power supplies shown in Figure 176 and Figure 177 are recommended in using ADAQ7769-1 for its typical applications. Instead of using an external LDO regulator to supply 5V to VDD_FDA, VDD_ADC, VDD2_ADC, and the external 4.096V reference, an internal LDO regulator that accepts a voltage of 5.1V to 5.5V is included in ADAQ7769-1 to conveniently output a well-regulated 5V supply. VDD_IO is supplied with a minimum of 1.7V to power the digital logic of the ADC driver, the GPIO, and the SPI of the ADC, but it requires a minimum of 2.5V when the GPIOs are used to control the GAIN pins of the PGA in SPI mode. For VDD_IO ≤ 1.8V, connect VDD_IO to DREG_CAP, decouple it with a 10µF capacitor, and enable LV_BOOST (Bit 7 of Register 0x14) from the Interface Format Control Register.

The ADAQ7769-1 has built-in 0.1µF supply decoupling capacitors on the VDD_PGA, VSS_PGA, VDD_FDA, VDD_ADC, VDD_ADC2, and VDD_IO supply pins. When the LDO is in use, it must be decoupled with a 1µF capacitor at IN_LDO and OUT_LDO. Additionally, the ADC's own analog and digital LDOs are also decoupled to the ground with a 1µF capacitor through pins AREG_CAP and DREG_CAP.

REFERENCE, REFERENCE BUFFER, AND LINEARITY BOOST BUFFER

While the ADC reference can range from VDD_ADC down to 1V, the typical application and specification of the ADAQ7769-1 is set with an input reference at 4.096V, which can be implemented by connecting the output of the integrated 5V LDO regulator to the ADR4540 voltage reference to output a voltage reference of 4.096V.

It is recommended to use the integrated reference precharge buffers of the ADC to lessen the burden on the external reference, as shown in the Reference Input and Buffering section.

It is also recommended to enable the linearity boost buffers, which ease the driving between the fully differential amplifier and core ADC input (see the Linearity Boost Buffer section).

In $\overline{\text{PIN}}$ mode, the reference precharge buffers and linearity boost buffers are enabled by default for enhanced performance, while the SPI mode requires a register write to the Analog Buffer Control Register to enable them.

RECOMMENDED INTERFACE

The ADAQ7769-1 interface is flexible to allow the many modes of operation and for data output formats to work across different DSPs and MCUs. To achieve maximum performance, the recommended interface configuration for reading conversion results is shown in Figure 178. This recommended implementation uses a synchronous SCLK to MCLK relationship.

Configure the interface as follows to achieve the recommended operation:

1. Connect the $\overline{\text{CS}}$ signal low during the conversion readback.
2. Enter continuous readback mode to avoid requiring to provide the address bits for the ADC_DATA register. Continuous readback mode is the default readback mode in $\overline{\text{PIN}}$ mode.
3. Clocking out 32 bits of data, consisting of the 24-bit conversion result plus 8 bits that can be either status or CRC bits. In $\overline{\text{PIN}}$ mode, these bits are always the conversion result plus the 8 status bits.
4. Provide an SCLK that is phase coherent to MCLK. SCLK can be identical to MCLK (SCLK = MCLK) or a divided down version of MCLK (SCLK = MCLK/N). For example, SCLK = MCLK/2 when decimate by 32 is selected.
5. Clocking 32 bits ensures that the data readback operation fills the entire $\overline{\text{DRDY}}$ period when SCLK = MCLK/2. SCLK runs continuously. The readback spans the full $\overline{\text{DRDY}}$ period, thus spreading the noise coupling due to the current on VDD_IO across the full ODR period.
6. The $\overline{\text{DRDY}}$ signal can synchronize the data read into the host controller.

APPLICATIONS INFORMATION

Figure 178 shows how the recommended interface operates. The data readback spans the entire length of the $\overline{DRDY}$ period, and the LSB remains until $\overline{DRDY}$ goes high for the next conversion.

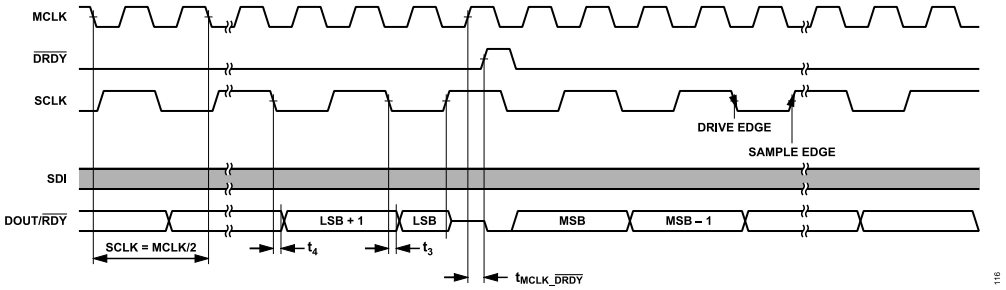

Figure 178. Recommended Interface for Reading Conversions, SPI Control, Continuous Readback Mode

APPLICATIONS INFORMATION

Initializing the Recommended Interface

To configure the recommended interface, do the following steps:

1. Configure the device settings, such as power mode, decimation ratio, and filter type.
2. Enter continuous readback mode.
3. Issue a synchronization pulse to apply the changes to the digital domain and to reset the digital filter. Issue the pulse immediately after $\overline{DRDY}$ goes high.

Recommended Interface for Reading Data

The recommended interface for reading data is as follows:

1. Synchronize the host controller with the $\overline{DRDY}$ or $\overline{RDY}$ pulse. For more details on the $\overline{RDY}$ behavior before data is clocked out, see Figure 6.
2. Generate SCLK based on the $\overline{DRDY}$ or $\overline{RDY}$ timing. SCLK is high when the $\overline{DRDY}$ signal goes high and transitions on the MCLK falling edges (see Figure 178) to ensure that the LSB can be read correctly as the DOUT/$\overline{RDY}$ output is reset on the $\overline{DRDY}$ rising edge. However, SCLK rising occurs before this transition.
3. The MSB is clocked out on the next falling edge of SCLK.
4. In $\overline{PIN}$ control mode, the LSB of the conversion output is the last bit of the status output. In $\overline{PIN}$ control mode, this bit is always 1 and, therefore, does not require to be read.

Resynchronization of the Recommended Interface

Because the full ODR period is for clocking data, the $\overline{RDY}$ signal no longer flags after each LSB outputs. This signal only flags if the ADAQ7769-1 is in continuous readback mode, or if the ADAQ7769-1 does not count 32 SCLKs within 1 × t_{MCLK} before $\overline{DRDY}$, as shown in Figure 178.

The $\overline{RDY}$ function is only available in continuous readback mode. In normal readback, where the ADC_DATA register must be addressed each time, the DOUT line is reset 1 × t_{MCLK} before $\overline{DRDY}$, as per t_{10} in the Timing Specifications section. If $\overline{DRDY}$ is used, the device operates as normal, and conversion readback is timed from the $\overline{DRDY}$ pulse. In the case where $\overline{RDY}$ detects the beginning of each sample, and where the data readback loses synchronization, the SCLK timing can be recovered by one of the following two methods:

- Using $\overline{CS}$ to reset the interface and to observe the $\overline{RDY}$ transition.
- Stopping SCLK toggling until the $\overline{RDY}$ transition is detected one more time.

PROGRAMMABLE DIGITAL FILTER

If there are additional filter requirements outside of the digital filters offered by default on the ADAQ7769-1, there is the added option of designing and uploading a custom digital filter to memory. This upload overwrites the default low-ripple FIR filter coefficients to be replaced by a set of user defined coefficients.

The ADAQ7769-1 filter path has three separate stages:

- Initial Sinc filter.
- Sinc compensation filter.
- Low-ripple FIR filter.

The user cannot change the first two stages. The only programmable stage is the third stage, where the default low-ripple FIR filter coefficients can be replaced by a set of user-defined coefficients.

The data rate into the third stage is double the final ODR due to a fixed decimation by two that occurs after the final stage of filtering. Therefore, the programmable FIR stage receives data at a rate that is decimated from f_{MOD} by rates of 16, 32, 64, 128, 256, and 512.

After the final decimation by 2, the overall decimation values are given and are in the range of decimate by 32 to decimate by 1024. The data rates into the final FIR stage are listed in Table 41 . Table 41 shows the data rate into the final filter stage for each power mode, assuming the correct MCLK_DIV setting is selected for the corresponding power mode. For example, when median-power mode is selected, MCLK_DIV must be MCLK/4.

Table 41. Data Rates into the Final FIR Input Stage

	Input to Third Stage, Programmable FIR (MCLK = 16.384MHz)								
Power Mode	**512kSPS**	**256kSPS**	**128kSPS**	**64kSPS**	**32kSPS**	**16kSPS**	**8kSPS**	**4kSPS**	**2kSPS**
Fast	Yes	Yes	Yes	Yes	Yes	Yes	N/A[1]	N/A[1]	N/A[1]
Median	N/A[1]	Yes	Yes	Yes	Yes	Yes	Yes	N/A[1]	N/A[1]
Low	N/A[1]	N/A[1]	N/A[1]	Yes	Yes	Yes	Yes	Yes	Yes

[1] N/A means not applicable.

APPLICATIONS INFORMATION

Filter Coefficients

The ADAQ7769-1 low-ripple FIR filter uses a set of 112 coefficients. By writing the appropriate key to the ADAQ7769-1, these coefficients can be overwritten. Then, the customized filter coefficients can upload and lock into memory. If the ADAQ7769-1 is reset, these coefficients must be rewritten.

The coefficients uploaded are subject to the following required conditions:

- The number of coefficients in a full set is 112, which is made up of 56 coefficients that are mirrored to make the total coefficients sum 112. Therefore, only 56 coefficients are written to during any one filter upload.
- Coefficients written must be in integer form. The format used is twos complement.
- The Coefficient Data Register to be written is 24 bits wide, which is the only 24-bit register write used on the ADAQ7769-1. Only 23 bits are used for the coefficients. The remaining MSB is a control bit, detailed in the Register 0x33.
- Filter coefficients are scaled such that the 56 coefficients must sum to 2^{22}. The total (112) coefficients, therefore, sum to 2^{23}.

For example, if the filter coefficient to be written to is −0.0123, this value is scaled to $-0.0123 \times 2^{22} = -51{,}590$. In twos complement format, this value is represented by 0x7F367A.

Each filter coefficient is written by first selecting the coefficient address. Then, a separate write of the data occurs, which is repeated for all 56 coefficients from Address 0 to Address 55.

Because the FIR size cannot be changed, the filter group delay remains fixed at 34/ODR when using the programmable filter option. If a shorter number of coefficients are required, padding zeros before the coefficients can achieve this requirement. The group delay of the uploaded filter must always be equal to the group delay of the default ADAQ7769-1 FIR filter that equals approximately 34/ODR.

Each time either the Coefficient Control Register or the Coefficient Data Register (COEFF_CONTROL or COEFF_DATA) are accessed, the user must wait a period before performing another read or write. The following equation determines the wait time:

$$t_{WAIT} = 512/MCLK$$

This wait time allows time for the register contents to update. Then, the coefficients are written to memory.

Upload Sequence

To program a user-defined set of filter coefficients, do the following steps:

1. Write 0x4 to the filter bits in the Digital Filter and Decimation Control Register (Register 0x19, Bits[6:4]).
2. The following key must be written to access the filter upload. First, write 0xAC to the Access Key Register (Register 0x34). Second, write 0x45 to the Access Key Register. Bit 0 (the key bit) of the Access Key Register can be readback to check if the key is entered correctly.
3. Write 0xC0 to the Coefficient Control Register (Register 0x32). Wait for t_{WAIT} sec to perform the following actions:
   a. Set the coefficient address to Address 0.
   b. Enable the access to memory (COEFF_ACCESS_EN = 1).
   c. Allow a write to the coefficient memory (COEFF_WRITE_EN = 1).
4. The address of the first coefficient is selected. Write the required coefficient to the Coefficient Data Register (Register 0x33), and then wait for t_{WAIT} sec. Always wait t_{WAIT} sec between writes to Register 0x32 and Register 0x33.
5. Repeat step 3 and step 4 for each of the 56 coefficients. For example, write 0xC1 to the Coefficient Control Register to select coefficient Address 1. After waiting t_{WAIT} sec, enter the coefficient data. Increment the data until Coefficient 55 is reached. (Coefficient 55 is a write of 0xF7 to Coefficient Control Register.)
6. Disable writing to the coefficients by first writing 0x80 to the Coefficient Control Register. Then, wait t_{WAIT} sec. Then, write 0x00 to the Coefficient Control Register to disable coefficient access.
7. Set USER_COEFF_EN = 1 by writing 0x800 to the Coefficient Data Register to allow the user to toggle the synchronization pulse and to begin reading data.
8. Exit the filter upload by writing 0x55 to the Access Key Register (Register 0x34).
9. Send a synchronization pulse to the ADAQ7769-1. One way of sending this pulse is by writing to the Synchronization Modes and Reset Triggering Register (Register 0x1D). The filter upload is now complete.

The RAM CRC error check fails when the digital filter uploads. To disable this check, use the Digital Diagnostic Feature Control Register (Register 0x2A).

APPLICATIONS INFORMATION

Example Filter Upload

The following sequence programs a Sinc1 filter. The coefficients in Address 0 to Address 23 = 0. The coefficients from Address 24 to Address 55 = 131,072 ($2^{22}/32$). When MCLK = 16.384MHz and ODR = 256kSPS, the filter notch appears at 8kHz and multiples of 8kHz. This filter provides low noise and is recognizable by the distinctive filter profile shown in Figure 179.

To program the filter, do the following steps:

1. Write 0x4 to the filter bits in the Digital Filter and Decimation Control Register (Register 0x19, Bits[6:4]).
2. Enter the key by writing to the Access Key Register (Register 0x34).
3. Write 0xC0 to the Coefficient Control Register, Register 0x32, (COEFF_ADDR = 0, COEFF_ACCESS_EN = 1, and COEFF_WRITE_EN = 1). Wait t_{WAIT} sec.
4. Write 0x000000 to the Coefficient Data Register (Register 0x33). Wait t_{WAIT} sec.
5. Write 0xC1 to the Coefficient Control Register (COEFF_ADDR = 1). Wait t_{WAIT} sec. In this case, the coefficient in Address 0 is equal to Address 1 and, therefore, the value in the Coefficient Data Register does not change.
6. Write 0xC2 to the Coefficient Control Register (COEFF_ADDR = 2). Wait t_{WAIT} sec.
7. Increment the address of the Coefficient Control Register (COEFF_ADDR = 23) until the write of 0xD7. Continue to wait t_{WAIT} sec.
8. Write 0xD8 to the Coefficient Control Register (COEFF_ADDR = 24).
9. Write 0x010000 to the Coefficient Data Register. Wait t_{WAIT} sec.
10. Write 0xD9 to the Coefficient Control Register (COEFF_ADDR = 25). Wait t_{WAIT} sec.
11. Write 0xDA to the Coefficient Control Register (COEFF_ADDR = 26) Wait t_{WAIT} sec.
12. Increment the address of the Coefficient Control Register (COEFF_ADDR = 55) until the write 0xF7. Wait t_{WAIT} sec.
13. Disable write and access by first writing 0x80 to the Coefficient Control Register. Wait t_{WAIT} sec. Then, write 0x00 to the Coefficient Control Register.
14. Set USER_COEFF_EN = 1 to allow the user to toggle synchronization without reloading the default coefficients. (Write 0x800000 to the Coefficient Data Register).
15. Exit the write by writing 0x55 to the Access Key Register.
16. Toggle synchronization.
17. Gather data. The resulting filter profile is shown in Figure 179.

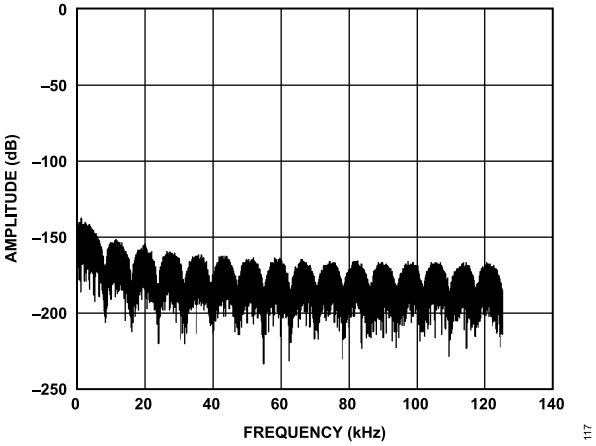

Figure 179. Example Filter Profile Upload

Filter Upload Verification

To check that the filter coefficients are uploaded correctly, it is possible to readback the values written to the Coefficient Data Register. To perform this read after an upload, do the following steps:

1. Enter the key by writing to the Access Key Register (Register 0x34). First, write 0xAC to the Access Key Register, and then write 0x45 to the Access Key Register.
2. Write 0x80 to the Coefficient Control Register, Register 0x32 (COEFF_ADDR = 0, COEFF_ACCESS_EN = 1, COEFF_WRITE_EN = 0). Wait t_{WAIT} sec.
3. Readback the contents of the 24-bit Coefficient Data Register (Register 0x33). Check that the coefficient matches the uploaded value.
4. Write 0x81 to the Coefficient Control Register (COEFF_ADDR = 1). Wait t_{WAIT} sec.
5. Read the 24-bit Coefficient Data Register for Address 1. Increment and continue to readback the data. Continue to wait t_{WAIT} sec between updates to the Coefficient Control Register.
6. Disable the coefficient access by writing 0x00 to the Coefficient Control Register.
7. Exit the readback process by writing 0x55 to the Access Key Register.

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

Design the PCB that houses the ADAQ7769-1 so that the analog and digital sections are separated and confined to different areas of the board. The ADAQ7769-1 pins are laid out with analog and digital pin partitioning. For ease of routing, the PGA input IN is located at D1, while OUT_PGA (C4) is adjacent to the three positive AAF input pins, and AGND pins are next to the three negative AAF input pins.

For the stack-up, use at least one ground plane that can be common or split between the digital and analog sections. In the case of the split plane, join the digital and analog ground planes in one place only, preferably as close as possible to the ADAQ7769-1.

If the ADAQ7769-1 is in a system where multiple devices require analog-to-digital ground connections, still make the connection at only one point: a star ground point that must be established as close as possible to the ADAQ7769-1. Ensure good connections are made to the ground plane. Avoid sharing one connection for multiple ground pins. Use individual vias or multiple vias to the ground plane for each ground pin.

Avoid running digital lines under the devices because it couples noise onto the die. Allow the analog ground plane to run under the ADAQ7769-1 to avoid noise coupling. Shield fast switching signals, like MCLK, with digital grounds to avoid radiating noise to other sections of the board and never run these fast switching signals near analog signal paths. Avoid crossover of digital and analog signals. Run traces on layers in close proximity on the PCB at right angles to each other to reduce the effect of feedthrough through the PCB.

Use as large traces as possible on the power supply lines to the VDD_PGA, VSS_PGA, IN_LDO, and VDD_IO pins on the ADAQ7769-1 to provide low impedance paths and reduce the effect of glitches on the power supply lines. When possible, use of supply planes to make good connections between the ADAQ7769-1 supply pins and the power supplies on the PCB. Use a single via or multiple vias for each supply pin.

Decouple the REF+, REF−, AREG_CAP, and DREG_CAP pins to AGND or DGND with minimal parasitic inductance by placing ceramic decoupling capacitors close to (ideally right up against) these pins and connect these pins with wide, low impedance traces.

REGISTER SUMMARY

This section contains details about the functions of each of the bit fields. The access column in the register tables specifies whether the bit fields are read-only (R), read/write (R/W), or write-1-to-clear (R/W1C) bits.

Table 42. ADAQ7769-1 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x03	CHIP_TYPE	[7:0]	RESERVED				CLASS				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x01	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	VALUE								0x00	R/W
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x14	INTERFACE_FORMAT	[7:0]	LV_BOOST	EN_SPI_CRC	CRC_TYPE	STATUS_EN	CONVLEN	EN_RDY_DOUT	RESERVED	EN_CONT_READ	0x00	R/W
0x15	POWER_CLOCK	[7:0]	CLOCK_SEL		MCLK_DIV		ADC_POWER_DOWN	RE-SERVED	ADC_MODE		0x00	R/W
0x16	ANALOG	[7:0]	REF_BUF_POS		REF_BUF_NEG		RESERVED		LINEAR-ITY_BOOST_A_OFF	LINEAR-ITY_BOOST_B_OFF	0x00	R/W
0x18	CONVERSION	[7:0]	DIAG_MUX_SELECT				CONV_DIAG_SELECT	CONV_MODE			0x00	R/W
0x19	DIGITAL_FILTER	[7:0]	EN_60HZ_REJ	FILTER			RESERVED	DEC_RATE			0x00	R/W
0x1A	SINC3_DEC_RATE_MSB	[7:0]	RESERVED				SINC3_DEC[12:8]				0x00	R/W
0x1B	SINC3_DEC_RATE_LSB	[7:0]	SINC3_DEC[7:0]								0x00	R/W
0x1C	DUTY_CYCLE_RATIO	[7:0]	IDLE_TIME								0x00	R/W
0x1D	SYNC_$\overline{\text{RESET}}$	[7:0]	SPI_$\overline{\text{START}}$	$\overline{\text{SYNC}}$_$\overline{\text{OUT}}$_POS_EDGE	RESERVED		EN_GPIO_$\overline{\text{START}}$	RE-SERVED	SPI_$\overline{\text{RESET}}$		0x80	R/W
0x1E	GPIO_CONTROL	[7:0]	UGPIO_EN	GPIO2_OPEN_DRAIN_EN	GPIO1_OPEN_DRAIN_EN	GPIO0_OPEN_DRAIN_EN	GPIO3_OP_EN	GPIO2_OP_EN	GPIO1_OP_EN	GPIO0_OP_EN	0x00	R/W
0x1F	GPIO_WRITE	[7:0]	RESERVED				GPIO_WRITE_3	GPIO_WRITE_2	GPIO_WRITE_1	GPIO_WRITE_0	0x00	R/W
0x20	GPIO_READ	[7:0]	RESERVED				GPIO_READ_3	GPIO_READ_2	GPIO_READ_1	GPIO_READ_0	0x00	R
0x21	OFFSET_HI	[7:0]	OFFSET[23:16]								0x00	R/W

REGISTER SUMMARY

Table 42. ADAQ7769-1 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x22	OFFSET_MID	[7:0]	OFFSET[15:8]								0x00	R/W
0x23	OFFSET_LO	[7:0]	OFFSET[7:0]								0x00	R/W
0x24	GAIN_HI	[7:0]	GAIN[23:16]								0x00	R/W
0x25	GAIN_MID	[7:0]	GAIN[15:8]								0x00	R/W
0x26	GAIN_LO	[7:0]	GAIN[7:0]								0x00	R/W
0x28	SPI_DIAG_ENABLE	[7:0]	RESERVED			EN_ERR_SPI_IGNORE	EN_ERR_SPI_CLK_CNT	EN_ERR_SPI_RD	EN_ERR_SPI_WR	RE-SERVED	0x10	R/W
0x29	ADC_DIAG_ENABLE	[7:0]	RESERVED		EN_ERR_DLDO_PSM	EN_ERR_ALDO_PSM	EN_ERR_REF_DET	EN_ERR_FILTER_SATUR-ATED	EN_ERR_FILTER_NOT_SETTLED	EN_ERR_EXT_CLK_QUAL0	0x07	R/W
0x2A	DIG_DIAG_ENABLE	[7:0]	RESERVED			EN_ERR_MEMMAP_CRC	EN_ERR_RAM_CRC	EN_ERR_FUSE_CRC	RESERVED	EN_FREQ_COUNT	0x0D	R/W
0x2C	ADC_DATA	[23:16]	ADC_READ_DATA[23:16]								0x000000	R
		[15:8]	ADC_READ_DATA[15:8]									
		[7:0]	ADC_READ_DATA[7:0]									
0x2D	MASTER_STATUS	[7:0]	MASTER_ERROR	ADC_ERROR	DIG_ERROR	ERR_EXT_CLK_QUAL	FILT_SATURATED	FILT_NOT_SETTLED	SPI_ERROR	POR_FLAG	0x00	R
0x2E	SPI_DIAG_STATUS	[7:0]	RESERVED			ERR_SPI_IGNORE	ERR_SPI_CLK_CNT	ERR_SPI_RD	ERR_SPI_WR	ERR_SPI_CRC	0x00	R/W
0x2F	ADC_DIAG_STATUS	[7:0]	RESERVED		ERR_DLDO_PSM	ERR_ALDO_PSM	ERR_REF_DET	FILT_SATURATED	FILT_NOT_SETTLED	ERR_EXT_CLK_QUAL	0x00	R
0x30	DIG_DIAG_STATUS	[7:0]	RESERVED			ERR_MEMMAP_CRC	ERR_RAM_CRC	ERR_FUSE_CRC	RESERVED		0x00	R
0x31	MCLK_COUNTER	[7:0]	MCLK_COUNTER								0x00	R
0x32	COEFF_CONTROL	[7:0]	COEFF_ACCESS_EN	COEFF_WRITE_EN	COEFF_ADDR						0x00	R/W
0x33	COEFF_DATA	[23:16]	USER_COEFF_EN	COEFF_DATA[22:16]							0x000000	R/W
		[15:8]	COEFF_DATA[15:8]									
		[7:0]	COEFF_DATA[7:0]									
0x34	ACCESS_KEY	[7:0]	RESERVED							KEY	0x00	R/W

REGISTER DETAILS

COMPONENT TYPE REGISTER

Register: 0x03, Reset: 0x07, Name: CHIP_TYPE

Table 43. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CLASS	Chip Type. 111: Analog-to-digital converter.	0x7	R

UNIQUE PRODUCT ID REGISTER

Register: 0x04, Reset: 0x01, Name: PRODUCT_ID_L

Table 44. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID.	0x1	R

Register: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

Table 45. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID.	0x0	R

DEVICE GRADE AND REVISION REGISTER

Register: 0x06, Reset: 0x00, Name: CHIP_GRADE

Table 46. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	Device Grade.	0x0	R
[3:0]	DEVICE_REVISION	Device Revision ID.	0x0	R

USER SCRATCH PAD REGISTER

Register: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

Table 47. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	VALUE	Scratch Pad. Read and write area communication and POR check.	0x0	R/W

REGISTER DETAILS

DEVICE VENDOR ID REGISTER

Register: 0x0C, Reset: 0x56, Name: VENDOR_L

Table 48. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Vendor ID.	0x56	R

Register: 0x0D, Reset: 0x04, Name: VENDOR_H

Table 49. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Vendor ID.	0x4	R

INTERFACE FORMAT CONTROL REGISTER

Register: 0x14, Reset: 0x00, Name: INTERFACE_FORMAT

Table 50. Bit Descriptions for INTERFACE_FORMAT

Bits	Bit Name	Description	Reset	Access
7	LV_BOOST	Boosts drive strength of SPI output for use with IOVDD levels of 1.8V, or when a high capacitive load is present on the DOUT/$\overline{\text{RDY}}$ pin. The default state is LV_BOOST enabled when in $\overline{\text{PIN}}$ control mode. 0: Disables LV_BOOST. 1: Enables LV_BOOST. Reenable this bit following an exit from the continuous read mode, if applicable.	0x0	R/W
6	EN_SPI_CRC	Activates CRC on all SPI transactions. 0: Disable CRC function on all SPI transfers. 1: Enable CRC function on all SPI transfers.	0x0	R/W
5	CRC_TYPE	Selects CRC method as XOR or 8-bit polynomial. 1: XOR instead of CRC (applied to read transactions only). 0: CRC bits are based on CRC-8 polynomial.	0x0	R/W
4	STATUS_EN	Enables output of the status bits. In SPI control mode, the status bits can be output after the ADC conversion result by setting the bits in this bit field. In $\overline{\text{PIN}}$ control mode, the status bits are output after the ADC conversion result. 0: Disable outputting status bits after ADC result in the continuous read mode. 1: Output status bits after ADC result in the continuous read mode.	0x0	R/W
3	CONVLEN	Conversion Result Output Length. 0: Outputs full 24 bits. 1: Outputs only 16MSB of the ADC result.	0x0	R/W
2	EN_RDY_DOUT	Enables $\overline{\text{RDY}}$ signal on DOUT/$\overline{\text{RDY}}$ pin. Enables $\overline{\text{RDY}}$ indicator on DOUT/$\overline{\text{RDY}}$ pin in continuous read mode. By default, the DOUT/$\overline{\text{RDY}}$ pin does not signal when new ADC conversion data is ready. Setting this bit causes DOUT/$\overline{\text{RDY}}$ to signal the availability of ADC conversion data. 0: Disables $\overline{\text{RDY}}$ function on DOUT/$\overline{\text{RDY}}$ pin in the continuous read mode after result is clocked out. 1: Enables RDY function on DOUT/$\overline{\text{RDY}}$ pin in continuous read mode after result is clocked out.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	EN_CONT_READ	Continuous Read Enable Bit. 0: Disables continuous read mode. 1: Enables continuous read mode.	0x0	R/W

REGISTER DETAILS

POWER AND CLOCK CONTROL REGISTER

Register: 0x15, Reset: 0x00, Name: POWER_CLOCK

Table 51. Bit Descriptions for POWER_CLOCK

Bits	Bit Name	Description	Reset	Access
[7:6]	CLOCK_SEL	Options for setting the clock used by the device. 00: CMOS clock on XTAL2_MCLK. 01: External crystal oscillator. 10: LVDS input enable (exclusive to SPI control mode). 11: Internal coarse RC clock (diagnostics).	0x0	R/W
[5:4]	MCLK_DIV	Sets the division of the MCLK to create the ADC modulator frequency f_{MOD}. 00: Modulator CLK is equal to controller clock divided by 16. 01: Modulator CLK is equal to controller clock divided by 8. 10: Modulator CLK is equal to controller clock divided by 4. 11: Modulator CLK is equal to controller clock divided by 2.	0x0	R/W
3	ADC_POWER_DOWN	Places ADC into a power-down state. All blocks including the SPI are powered down. The standard SPI is not active in this state. Power-down is the lowest power consumption mode. To enter power-down mode, write 0x08 to this register. If the user attempts to set Bit 3 while also setting other bits in this register, the SPI write command is ignored, the device does not enter power-down, and the other bits are not set. Power-down mode can be exited in three ways: by a reset using the $\overline{\text{RESET}}$ pin, by issuing the SPI resume command over SDI and SCLK, or by using the power cycle of the device.	0x0	R/W
2	RESERVED	Reserved.	0x0	R/W
[1:0]	ADC_MODE	Sets the operation mode of the ADC core. This setting in conjunction with MCLK_DIV creates the conditions for power scaling the ADC vs. input bandwidth and throughput. 00: Low-power mode. 01: Median-power mode. 11: Fast-power mode.	0x0	R/W

ANALOG BUFFER CONTROL REGISTER

Register: 0x16, Reset: 0x00, Name: ANALOG

Used to turn on or off the front-end buffering.

Table 52. Bit Descriptions for ANALOG

Bits	Bit Name	Description	Reset	Access
[7:6]	REF_BUF_POS	Buffering Options for the Reference Positive Input. 00: Precharge reference buffer on. 01: Unbuffered reference input. 10: Full reference buffer on.	0x0	R/W
[5:4]	REF_BUF_NEG	Buffering Options for the Reference Negative Input. 00: Precharge reference buffer on. 01: Unbuffered input. 10: Full reference buffer on.	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R
1	LINEARITY_BOOST_A_OFF	Linearity Boost Buffer A Disable Control. Setting this bit disables Linearity Boost Buffer A. Use in conjunction with LINEARITY_BOOST_B_OFF. 0: Linearity Boost Buffer A enabled. 1: Linearity Boost Buffer A disabled.	0x0	R/W
0	LINEARITY_BOOST_B_OFF	Linearity Boost Buffer B Disable Control. Setting this bit disables Linearity Boost Buffer B. Use in conjunction with LINEARITY_BOOST_A_OFF. 0: Linearity Boost Buffer B enabled.	0x0	R/W

REGISTER DETAILS

Table 52. Bit Descriptions for ANALOG (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Linearity Boost Buffer B disabled.		

CONVERSION SOURCE SELECT AND MODE CONTROL REGISTER

Register: 0x18, Reset: 0x00, Name: CONVERSION

Table 53. Bit Descriptions for CONVERSION

Bits	Bit Name	Description	Reset	Access
[7:4]	DIAG_MUX_SELECT	Selects which signal to route through diagnostic mux. Perform diagnostic checks in low-power mode only. 0000: Temperature sensor. 1000: ADC input short (zero check). 1001: Positive full scale. 1010: Negative full scale.	0x0	R/W
3	CONV_DIAG_SELECT	Selects the input of ADC for conversion as normal or diagnostic mux. 0: Converting signal through the normal signal chain. 1: ADC converting (and turning on) diagnostic subblocks.	0x0	R/W
[2:0]	CONV_MODE	Sets the conversion mode of the ADC. 000: Continuous conversion mode. The modulator is converting continuously. A continuous $\overline{\text{DRDY}}$ pulse for every filter conversion. 001: Continuous one-shot mode. One-shot mode is the method of using the $\overline{\text{SYNC\_IN}}$ time to start a conversion. It is similar to a conversion start signal when using the one-shot mode. The ADC modulator is continuously running while waiting on a $\overline{\text{SYNC\_IN}}$ rising edge. On release of a pulse (low-to-high transition) to the $\overline{\text{SYNC\_IN}}$ pin, a new conversion begins, converting and integrating over the settling time of the filter selected. $\overline{\text{DRDY}}$ toggles when the conversion completes, which indicates that it is available for readback over the SPI. 010: Single-conversion standby mode. In single-conversion standby mode, the ADC runs one conversion with the selected filter, sampling and integrating over the full settling time of the filter before providing a single conversion result. After the conversion is complete, the ADC goes into standby. Initiating another single conversion from standby means that there is a start-up time to come out of standby before the ADC begins converting to produce the single conversion. This mode is recommended for use in the low-power mode. 011: Duty-cycled conversion standby mode. Low-power periodic conversion is a method of setting the single conversion to run in a timed loop. A separate register sets the ratio for the time spent in standby vs. converting. The ADC automatically comes out of standby periodically, performs a single conversion, and then returns to standby without the need to initiate the single conversion over the SPI. 100: Standby. 101: Standby. 110: Standby. 111: Standby.	0x0	R/W

DIGITAL FILTER AND DECIMATION CONTROL REGISTER

Register: 0x19, Reset: 0x00, Name: DIGITAL_FILTER

Table 54. Bit Descriptions for DIGITAL_FILTER

Bits	Bit Name	Description	Reset	Access
7	EN_60HZ_REJ	For use with Sinc3 filter only. First, program the Sinc3 filter to output at 50Hz. Subsequently selecting the EN_60HZ_REJ bit allows one zero of the a Sinc3 filter to fall at 60Hz. This bit only enables rejection of both 50Hz and 60Hz if it is set in combination with programming the Sinc3 filter for 50Hz ODR. 0: Sinc3 filter optimized for single frequency rejection: 50Hz or 60Hz. 1: Filter operation is modified to allow both 50Hz and 60Hz rejection.	0x0	R/W
[6:4]	FILTER	Selects the style of filter for use.	0x0	R/W

REGISTER DETAILS

Table 54. Bit Descriptions for DIGITAL_FILTER (Continued)

Bits	Bit Name	Description	Reset	Access
		000: Sinc5 filter. Decimate ×32 to ×1024. Use DEC_RATE bits to select one of six available decimation rates from ×32 to ×1024. 001: Sinc5 filter. Decimate ×8 only. Enables a maximum data rate of 1MHz. This path allows viewing of a wider bandwidth. However, it is quantization noise limited, therefore, output data is reduced to 16 bits. 010: Sinc5 filter. Decimate ×16 only. Enables a maximum data rate of 512kHz. This path allows viewing of a wider bandwidth. 011: Sinc3 filter. Programmable decimation rate. Decimation rate is selected via the SINC3_DEC bits in the Sinc3 decimation rate MSB and LSB registers (Register 0x1A and Register 0x1B). The Sinc3 filter can be tuned to reject 50Hz or 60Hz. With the EN_60HZ_REJ bit set, it can allow rejection of both 50Hz and 60Hz when used with a 16.384MHz MCLK. 100: Wideband low-ripple filter. FIR filter with low-ripple pass band and sharp transition band. Use the DEC_RATE bits to select one of six available decimation rates from ×32 to ×1024.		
3	RESERVED	Reserved.	0x0	R
[2:0]	DEC_RATE	Selects the decimation rate for the Sinc5 filter and the wideband low-ripple FIR filter. 000: Decimate ×32. 001: Decimate ×64. 010: Decimate ×128. 011: Decimate ×256. 100: Decimate ×512. 101: Decimate ×1024. 110: Decimate ×1024. 111: Decimate ×1024.	0x0	R/W

SINC3 DECIMATION RATE (MSB) REGISTER

Register: 0x1A, Reset: 0x00, Name: SINC3_DEC_RATE_MSB

Table 55. Bit Descriptions for SINC3_DEC_RATE_MSB

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SINC3_DEC[12:8]	Determines the decimation rate of used with the Sinc3 filter. Value entered is incremented by 1 and multiplied by 32 to give actual decimation rate.	0x0	R/W

SINC3 DECIMATION RATE (LSB) REGISTER

Register: 0x1B, Reset: 0x00, Name: SINC3_DEC_RATE_LSB

Table 56. Bit Descriptions for SINC3_DEC_RATE_LSB

Bits	Bit Name	Description	Reset	Access
[7:0]	SINC3_DEC[7:0]	Determines the decimation rate of used with the Sinc3 filter. Value entered is incremented by 1 and multiplied by 32 to give actual decimation rate.	0x0	R/W

PERIODIC CONVERSION RATE CONTROL REGISTER

Register: 0x1C, Reset: 0x00, Name: DUTY_CYCLE_RATIO

Table 57. Bit Descriptions for DUTY_CYCLE_RATIO

Bits	Bit Name	Description	Reset	Access
[7:0]	IDLE_TIME	Sets idle time for periodic conversion when in standby. A 1 in this register corresponds to the time for one output from the filter selected. The value in this register is incremented by one and doubled.	0x0	R/W

REGISTER DETAILS

SYNCHRONIZATION MODES AND RESET TRIGGERING REGISTER

Register: 0x1D, Reset: 0x80, Name: SYNC_RESET

Table 58. Bit Descriptions for SYNC_RESET

Bits	Bit Name	Description	Reset	Access
7	SPI_START	Triggers START signal. Initiates a SYNC_OUT pulse over the SPI. Setting this bit low drives a low pulse through SYNC_OUT, which can be used as a SYNC_IN signal to the same device and other ADAQ7769-1 devices where synchronized sampling is required. This bit clears itself after use.	0x1	R
6	SYNC_OUT_POS_EDGE	SYNC_OUT drive edge selected. Setting this bit causes SYNC_OUT to be driven low by the positive edge of MCLK. Device default is that SYNC_OUT is driven low on the negative edge of MCLK.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R
3	EN_GPIO_START	Enables START function on the GPIO input. Allows to use one of the GPIO pins as a START input pin. When enabled, a low pulse on the START input generates a low pulse through SYNC_OUT that can be used as a SYNC_IN signal to the same device and other ADAQ7769-1 devices where synchronized sampling is required. When enabled, GPIO3 becomes the START input. While the START function is enabled, the GPIO pins cannot be used for general-purpose input and output reading and writing. The remaining GPIOs are set to outputs. 0: Disables. 1: Enables.	0x0	R/W
2	RESERVED	Reserved.	0x0	R
[1:0]	SPI_RESET	Enables device reset over the SPI. Two writes to these bits are required to initiate the reset. First, set the bits to 11, then set the bits to 10. Once this sequence is detected on these two bits, the reset occurs. It is not dependent on other bits in this register being set or cleared.	0x0	R/W

GPIO PORT CONTROL REGISTER

Register: 0x1E, Reset: 0x00, Name: GPIO_CONTROL

Table 59. Bit Descriptions for GPIO_CONTROL

Bits	Bit Name	Description	Reset	Access
7	UGPIO_EN	Universal Enabling of GPIO Pins. This bit must be set HI to change GPIO settings.	0x0	R/W
6	GPIO2_OPEN_DRAIN_EN	Change GPIO2 output from strong driver to open drain.	0x0	R/W
5	GPIO1_OPEN_DRAIN_EN	Change GPIO1 output from strong driver to open drain.	0x0	R/W
4	GPIO0_OPEN_DRAIN_EN	Change GPIO0 output from strong driver to open drain.	0x0	R/W
3	GPIO3_OP_EN	Output Enable for GPIO Pin. 0 -> input, 1-> output.	0x0	R/W
2	GPIO2_OP_EN	Output Enable for GPIO Pin. 0 -> input, 1-> output.	0x0	R/W
1	GPIO1_OP_EN	Output Enable for GPIO Pin. 0 -> input, 1-> output.	0x0	R/W
0	GPIO0_OP_EN	Output Enable for GPIO Pin. 0 -> input, 1-> output.	0x0	R/W

GPIO OUTPUT CONTROL REGISTER

Register: 0x1F, Reset: 0x00, Name: GPIO_WRITE

Table 60. Bit Descriptions for GPIO_WRITE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GPIO_WRITE_3	Write to this bit to set GPIO[3] HI.	0x0	R/W
2	GPIO_WRITE_2	Write to this bit to set GPIO[2] HI.	0x0	R/W
1	GPIO_WRITE_1	Write to this bit to set GPIO[1] HI.	0x0	R/W
0	GPIO_WRITE_0	Write to this bit to set GPIO[0] HI.	0x0	R/W

REGISTER DETAILS

GPIO INPUT READ REGISTER

Register: 0x20, Reset: 0x00, Name: GPIO_READ

Table 61. Bit Descriptions for GPIO_READ

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GPIO_READ_3	Read the value from GPIO3.	0x0	R
2	GPIO_READ_2	Read the value from GPIO2.	0x0	R
1	GPIO_READ_1	Read the value from GPIO1.	0x0	R
0	GPIO_READ_0	Read the value from GPIO0.	0x0	R

OFFSET CALIBRATION MSB REGISTER

Register: 0x21, Reset: 0x00, Name: OFFSET_HI

Table 62. Bit Descriptions for OFFSET_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[23:16]	User Offset Calibration Coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of the offset register adjustment changes the digital output by −4/3LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, therefore, the previous ratio changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION MID REGISTER

Register: 0x22, Reset: 0x00, Name: OFFSET_MID

Table 63. Bit Descriptions for OFFSET_MID

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[15:8]	User Offset Calibration Coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, therefore, the previous ratio changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION LSB REGISTER

Register: 0x23, Reset: 0x00, Name: OFFSET_LO

Table 64. Bit Descriptions for OFFSET_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[7:0]	User Offset Calibration Coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction, therefore, the previous ratio changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

REGISTER DETAILS

GAIN CALIBRATION MSB REGISTER

Register: 0x24, Reset: 0x00, Name: GAIN_HI

Table 65. Bit Descriptions for GAIN_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[23:16]	User Gain Calibration Coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming, and the nominal value is around 0x555555. The user can readback the factory programmed value and can overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION MID REGISTER

Register: 0x25, Reset: 0x00, Name: GAIN_MID

Table 66. Bit Descriptions for GAIN_MID

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[15:8]	User Gain Calibration Coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming, and the nominal value is around 0x555555. The user can readback the factory programmed value and can overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION LSB REGISTER

Register: 0x26, Reset: 0x00, Name: GAIN_LO

Table 67. Bit Descriptions for GAIN_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[7:0]	User Gain Calibration Coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming, and the nominal value is around 0x555555. The user can readback the factory programmed value and can overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

SPI DIAGNOSTIC CONTROL REGISTER

Register: 0x28, Reset: 0x10, Name: SPI_DIAG_ENABLE

Table 68. Bit Descriptions for SPI_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	EN_ERR_SPI_IGNORE	SPI Ignore Error Enable.	0x1	R/W
3	EN_ERR_SPI_CLK_CNT	SPI Clock Count Error Enable. The SPI clock count error is only valid for SPI transactions that use $\overline{CS}$.	0x0	R/W
2	EN_ERR_SPI_RD	SPI Read Error Enable.	0x0	R/W
1	EN_ERR_SPI_WR	SPI Write Error Enable.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

ADC DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x29, Reset: 0x07, Name: ADC_DIAG_ENABLE

Table 69. Bit Descriptions for ADC_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	EN_ERR_DLDO_PSM	Digital LDO Power Saving Mode (PSM) Error Enable.	0x0	R/W
4	EN_ERR_ALDO_PSM	Analog LDO PSM Error Enable.	0x0	R/W
3	EN_ERR_REF_DET	Reference Detection Error Enable.	0x0	R/W
2	EN_ERR_FILTER_SATURATED	Filter Saturated Error Enable.	0x1	R/W
1	EN_ERR_FILTER_NOT_SETTLED	Filter Not Settled Error Enable.	0x1	R/W
0	EN_ERR_EXT_CLK_QUAL	Enables qualification check on the external clock.	0x1	R/W

DIGITAL DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x2A, Reset: 0x0D, Name: DIG_DIAG_ENABLE

Table 70. Bit Descriptions for DIG_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	EN_ERR_MEMMAP_CRC	Memory Map CRC Error Enable.	0x0	R/W
3	EN_ERR_RAM_CRC	RAM CRC Error Enable.	0x1	R/W
2	EN_ERR_FUSE_CRC	Fuse CRC Error Enable.	0x1	R/W
1	RESERVED	Reserved.	0x0	R/W
0	EN_FREQ_COUNT	Enables MCLK counter.	0x1	R/W

CONVERSION RESULT REGISTER

Register: 0x2C, Reset: 0x000000, Name: ADC_DATA

Table 71. Bit Descriptions for ADC_DATA

Bits	Bit Name	Description	Reset	Access
[23:0]	ADC_READ_DATA	ADC Read Data.	0x0	R

DEVICE ERROR FLAGS MAIN REGISTER

Register: 0x2D, Reset: 0x00, Name: MASTER_STATUS

Table 72. Bit Descriptions for MASTER_STATUS

Bits	Bit Name	Description	Reset	Access
7	MASTER_ERROR	Any Device Error. An OR of all other errors present.	0x0	R
6	ADC_ERROR	Any ADC Error (OR).	0x0	R
5	DIG_ERROR	Any Digital Error (OR).	0x0	R
4	ERR_EXT_CLK_QUAL	No Clock Error, Applied to MASTER_STATUS Register Only.	0x0	R
3	FILT_SATURATED	Filter Saturated.	0x0	R
2	FILT_NOT_SETTLED	Filter Not Settled.	0x0	R
1	SPI_ERROR	Any SPI Error (OR).	0x0	R
0	POR_FLAG	POR Flag.	0x0	R

REGISTER DETAILS

SPI ERROR REGISTER

Register: 0x2E, Reset: 0x00, Name: SPI_DIAG_STATUS

Table 73. Bit Descriptions for SPI_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ERR_SPI_IGNORE	SPI Ignore Error.	0x0	R/W1C
3	ERR_SPI_CLK_CNT	SPI Clock Count Error.	0x0	R
2	ERR_SPI_RD	SPI Read Error.	0x0	R/W1C
1	ERR_SPI_WR	SPI Write Error.	0x0	R/W1C
0	ERR_SPI_CRC	SPI CRC Error.	0x0	R/W1C

ADC DIAGNOSTICS OUTPUT REGISTER

Register: 0x2F, Reset: 0x00, Name: ADC_DIAG_STATUS

Table 74. Bit Descriptions for ADC_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	ERR_DLDO_PSM	DLDO PSM Error.	0x0	R
4	ERR_ALDO_PSM	ALDO PSM Error.	0x0	R
3	ERR_REF_DET	REF DET Error.	0x0	R
2	FILT_SATURATED	Filter Saturated.	0x0	R
1	FILT_NOT_SETTLED	Filter Not Settled.	0x0	R
0	ERR_EXT_CLK_QUAL	No Clock Error, Applied to MASTER_STATUS Register Only.	0x0	R

DIGITAL DIAGNOSTICS OUTPUT REGISTER

Register: 0x30, Reset: 0x00, Name: DIG_DIAG_STATUS

Table 75. Bit Descriptions for DIG_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ERR_MEMMAP_CRC	Memory Map CRC Error.	0x0	R
3	ERR_RAM_CRC	RAM CRC Error.	0x0	R
2	ERR_FUSE_CRC	Fuse CRC Error.	0x0	R
[1:0]	RESERVED	Reserved.	0x0	R

MCLK DIAGNOSTIC OUTPUT REGISTER

Register: 0x31, Reset: 0x00, Name: MCLK_COUNTER

Table 76. Bit Descriptions for MCLK_COUNTER

Bits	Bit Name	Description	Reset	Access
[7:0]	MCLK_COUNTER	MCLK Counter. This register increments after every 64 MCLKs.	0x0	R

REGISTER DETAILS

COEFFICIENT CONTROL REGISTER

Register: 0x32, Reset: 0x00, Name: COEFF_CONTROL

Table 77. Bit Descriptions for COEFF_CONTROL

Bits	Bit Name	Description	Reset	Access
7	COEFF_ACCESS_EN	Setting this bit to a 1 allows access to the coefficient memory.	0x0	R/W
6	COEFF_WRITE_EN	Enables write to the coefficient memory. Write a 1 to enable.	0x0	R/W
[5:0]	COEFF_ADDR	Address to be accessed for the coefficient memory. The address ranges from 0 to 55 for 56 coefficients that form one symmetrical half of the 112 coefficients.	0x00	R/W

COEFFICIENT DATA REGISTER

Register: 0x33, Reset: 0x00, Name: COEFF_DATA

Table 78. Bit Descriptions for COEFF_DATA

Bits	Bit Name	Description	Reset	Access
23	USER_COEFF_EN	Setting this bit to a 1 prevents the coefficients from read only memory (ROM) over writing the user-defined coefficients after a synch toggle. A sync pulse is required after every change to the digital filter configuration, including a customized filter upload.	0x0	R/W
[22:0]	COEFF_DATA	Data read from or to be written to coefficient memory. These bits are 23 bits wide.	0x000000	R/W

ACCESS KEY REGISTER

Register: 0x34, Reset: 0x00, Name: ACCESS_KEY

Table 79. Bit Descriptions for ACCESS_KEY

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	Key	A specific key must be written to the ACCESS_KEY register prior to any filter upload. If written correctly, the key bit reads back as 1.	0x0	R/W

OUTLINE DIMENSIONS

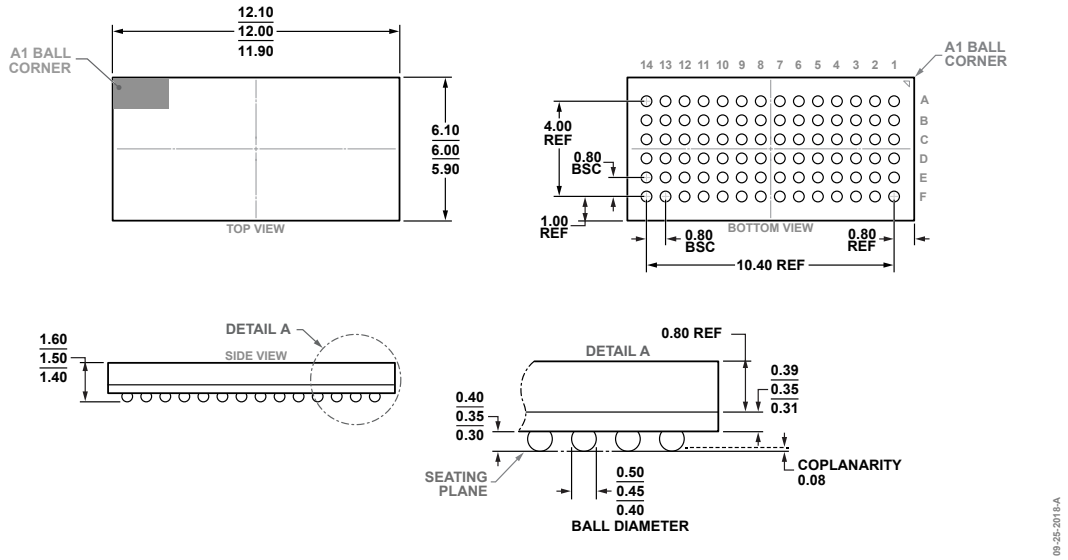

Figure 180. 84-Ball Chip-Scale Package Ball Grid Array [CSP_BGA]
(BC-84-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADAQ7769-1BBCZ	−40°C to +105°C	CHIP SCALE BGA	Tray, 280	BC-84-4

[1] Z = RoHS Compliant Part.

Updated: July 24, 2025

EVALUATION BOARDS

Evaluation Board[1]	Description
EV-ADAQ7769-1FMC1Z	Evaluation Board

[1] Z = RoHS Compliant Part.