Compact, Dual-Channel, Precision, Programmable Gain Transimpedance Amplifier (PGTIA)

FEATURES

- Small, dual-channel, complete PGTIA and AFE solution
- Small size package:16-lead LFCSP, 3 mm × 3 mm
  - Integrated switches, 2 external gains per channel
- Wide input current dynamic range from picoamps to milliamps
- Excellent DC precision
  - Low offset voltage: ±100 µV maximum, 25°C
  - Low offset voltage drift: ±0.85 µV/°C maximum, −40°C to +125°C
  - Low input bias current: ±9 pA maximum, 25°C
  - Low switch off leakage current : ±90 pA maximum (−40°C to +125°C)
- New integrated architecture eliminates gain error due to switch resistance
- Single-supply operation: +2.7 V to +5.5 V (dual-supply operation: ±1.85 V to ±2.75 V)
- Wide gain bandwidth product: 8.5 MHz
- Wide operating temperature range: −40°C to +125°C

APPLICATIONS

- Precision current to voltage (I to V) conversion
- Programmable gain TIAs
- Photodetector interface and amplification
- Optical networking equipment
- Optical power measurement
- Instrumentation—spectroscopy and chromatography
- Precision data acquisition systems (DAQ)

TYPICAL APPLICATION DIAGRAM

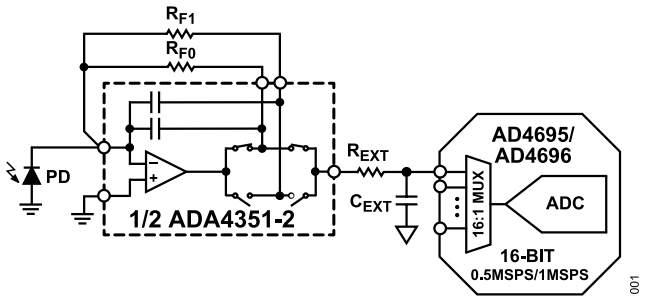


Figure 1. Compact Optical Measurement Signal Chain

GENERAL DESCRIPTION

The ADA4351-2 is a compact, monolithic, dual-channel, precision, programmable gain transimpedance amplifier (PGTIA). The ADA4351-2 is a breakthrough solution for precisely measuring small currents over a wide dynamic range. The precision of the ADA4351-2 over a wide temperature range of −40°C to +125°C enables users to perform one calibration of the end equipment at room temperature, thereby saving test time and cost. The ADA4351-2 integrates two low off leakage current switches per channel, and the gain is programmable using two user-selectable external resistors to provide a flexible, fully functional compact PGTIA solution. Separate analog and digital supplies allow the amplifier of the ADA4351-2 to operate on bipolar supplies, while the integrated logic level shifting allows the digital interface to remain ground referenced. Additionally, with its robust output stage and low noise, the ADA4351-2 can directly drive 16-bit precision analog-to-digital converters (ADCs, such as AD4696), providing a complete analog front-end (AFE) to address the most challenging precision current measurement applications.

The ADA4351-2 is offered in a 3 mm × 3 mm LFCSP, reducing the printed circuit board (PCB) area by up to 70% relative to a discrete design using standalone operational amplifiers (op amps) and switches. Additionally, there is no exposed pad (EPAD) on the back side of the LFCSP, eliminating the need for vias and allowing routing on all layers of the PCB beneath the device to further reduce the board area and to provide the most compact PGTIA and AFE solution.

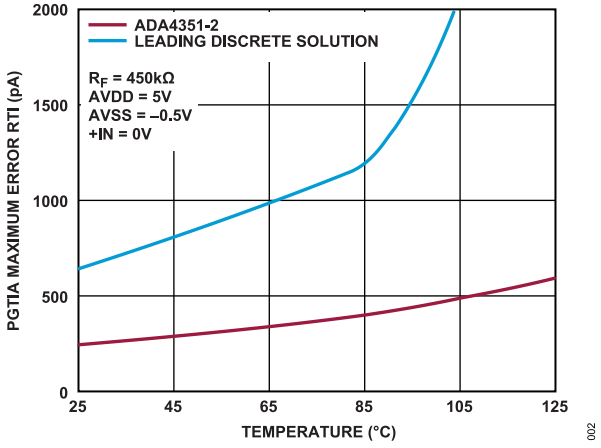


Figure 2. PGTIA Maximum Error RTI vs. Temperature (Includes Input Bias Current (I_B), Offset Voltage (V_{OS},) and Switch Off Leakage Current (I_{OFF}))

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REVISION HISTORY

7/2026—Rev. 0 to Rev. A

Changes to Ordering Guide ... 36

10/2023—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

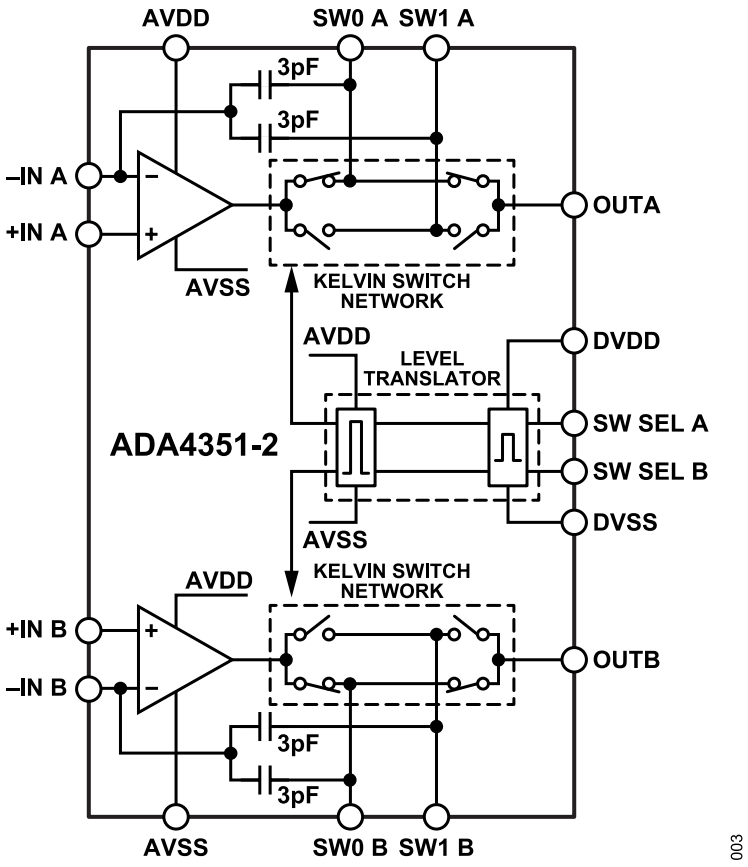


Figure 3. Functional Block Diagram

SPECIFICATIONS

5 V SPECIFICATIONS

T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, and +IN = 2.5 V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a symmetrical supply configuration with +IN biased to 0 V.

Table 1. 5 V Specifications

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Test Level
DC PERFORMANCE						
Offset Voltage (V_{OS}), Referred to Input (RTI)			±20	±100	µV	P
Offset Voltage Drift, RTI	T_A = 0°C to +85°C		±0.15	±0.8	µV/°C	C_B
	T_A = −40°C to +125°C		±0.16	±0.85	µV/°C	C_B
Input Bias Current at −IN						
			±2	±9	pA	P
	T_A = −40°C to +85°C			±45	pA	C_T
	T_A = −40°C to +105°C			±70	pA	C_T
	T_A = −40°C to +125°C			±100	pA	C_T
Input Bias Current at +IN			±2	±9	pA	P
	T_A = −40°C to +85°C			±70	pA	C_T
	T_A = −40°C to +105°C			±110	pA	C_T
	T_A = −40°C to +125°C			±150	pA	C_T
Open-Loop Gain (A_{OL})	R_F = 10 kΩ, V_{OUT} = 0.5 V to 4.5 V[2]	95	158		dB	P
	V_{OUT} = 0.1 V to 4.9 V, T_A = −40°C to +125°C	108			dB	C_T
INPUT CHARACTERISTICS						
Common-Mode Input Impedance at +IN			3.75/1		TΩ/pF	C_B
Common-Mode Input Impedance at −IN			3.75/3.5		TΩ/pF	C_B
Differential Mode Input Capacitance			2		pF	C_B
Internal Feedback Capacitance			3		pF	C_B
Input Common-Mode Voltage Range (V_{CM})	T_A = −40°C to +125°C	AVSS		AVDD − 1.5	V	C_B
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0.1 V to 1.9 V	74	87		dB	P
	V_{CM} = 2.6 V to 3.5 V	80	98		dB	P
	V_{CM} = 0.1 V to 3.5 V, T_A = −40°C to +125°C	78			dB	C_T
OUTPUT CHARACTERISTICS						
Saturated Output Voltage Swing to AVSS (V_{OUT} − AVSS)	R_F = 10 kΩ			10	mV	P
Saturated Output Voltage Swing to AVDD (AVDD − V_{OUT})	R_F = 10 kΩ			10	mV	P
Short-Circuit Output Current	Sinking/sourcing, V_{OUT} = 2.5 V		75/63		mA	C_B
Linear SW0, SW1 Current[3]	V_{OUT} = 2.5 V		±75		mA	C_B
DYNAMIC PERFORMANCE						
Gain Bandwidth Product (GBP)			8.5		MHz	C_B
Slew Rate	10% to 90%		8		V/µs	C_B
Total Harmonic Distortion (THD)	G = −1, R_F = 15 kΩ, f = 1 kHz, V_{OUT} = 1 V RMS		−126		dBc	C_B
ANALOG POWER SUPPLIES (AVDD AND AVSS)						
Operating Range V_S = AVDD − AVSS	Guaranteed by power supply rejection ratio (PSRR)	2.7		5.5	V	P
AVSS Range Below DVSS		−0.5		0	V	S
Quiescent Current Per Amplifier			3.3	3.5	mA	P
	T_A = −40°C to +125°C			4.35	mA	C_T
PSRR	Supply voltage (V_S) = 2.7 V to 5.5 V	81	92		dB	P
	V_S = 2.7 V to 5.5 V, T_A = −40°C to +125°C	76			dB	C_T

SPECIFICATIONS

Table 1. 5 V Specifications (Continued)

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Test Level
THRESHOLD VOLTAGES FOR SW SEL						
Input High Voltage (V_{IH})		DVDD − 0.7			V	S
Input Low Voltage (V_{IL})				DVSS + 0.5	V	S
SW SEL Pull-Down Resistance			865		kΩ	C_B
DIGITAL POWER SUPPLIES (DVDD AND DVSS)						
Operating Range (DVDD − DVSS)		1.62		5.5	V	P
Quiescent Current				1	µA	P
	T_A = −40°C to +125°C			10	µA	C_T
ANALOG SWITCH CHARACTERISTICS						
Switch On Resistance (R_{ON})			11	13	Ω	P
	T_A = −40°C to +125°C			19	Ω	C_T
Switch On-Resistance Drift	T_A = −40°C to +125°C		0.3		%/°C	C_T
SW0 and SW1 Switch Off Pin Capacitance			1.8		pF	C_B
Switch Off Leakage Current	SW0 and SW1 = 0.5 V		±1	±6	pA	P
	T_A = −40°C to +85°C			±22	pA	C_T
	T_A = −40°C to +105°C			±50	pA	C_T
	T_A = −40°C to +125°C			±90	pA	C_T
	SW0 and SW1 = 0.1 V		±2	±10	pA	P
	T_A = −40°C to +85°C			±30	pA	C_T
	T_A = −40°C to +105°C			±70	pA	C_T
	T_A = −40°C to +125°C			±110	pA	C_T
NOISE						
Input Voltage Noise Density (e_n)	f = 100 kHz		7.3		nV/√Hz	C_B
Integrated Voltage Noise	f = 0.1 Hz to 10 Hz		4.5		µV p-p	C_B

[1] To simplify terminology throughout this data sheet, because the two amplifiers inside the ADA4351-2 are interchangeable, R_{F1}, R_{F0}, SW0, SW1, SW SEL, +IN, and −IN refer to Channel A or Channel B. V_{OUT} refers to OUTA or OUTB, and within each channel, R_F refers to R_{F1} or R_{F0}.

[2] High speed production testing limits the accuracy of this specification.

[3] Linear current is the current that these pins can conduct while V_{OS} shifts by less than 20 µV.

SPECIFICATIONS

3 V SPECIFICATIONS

T_A = 25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, and +IN = 1.5 V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a symmetrical supply configuration with +IN biased to 0 V.

Table 2. 3 V Specifications

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Test Level
DC PERFORMANCE						
Offset Voltage (V_{OS}), Referred to Input (RTI)			±25	±150	µV	P
Offset Voltage Drift, RTI	T_A = 0°C to +85°C		±0.11	±0.85	µV/°C	C_B
	T_A = −40°C to +125°C		±0.22	±0.9	µV/°C	C_B
Input Bias Current at −IN			±1	±2	pA	P
	T_A = −40°C to +85°C			±20	pA	C_T
	T_A = −40°C to +105°C			±30	pA	C_T
	T_A = −40°C to +125°C			±30	pA	C_T
Input Bias Current at +IN			±1	±2	pA	P
	T_A = −40°C to +85°C			±35	pA	C_T
	T_A = −40°C to +105°C			±60	pA	C_T
	T_A = −40°C to +125°C			±70	pA	C_T
Open-Loop Gain (A_{OL})	R_F = 10 kΩ, V_{OUT} = 0.5 V to 2.5 V[2]	93	115		dB	P
	V_{OUT} = 0.1 V to 2.9 V, T_A = −40°C to +125°C	104			dB	C_T
INPUT CHARACTERISTICS						
Common-Mode Input Impedance at +IN			3.75/2.8		TΩ/pF	C_B
Common-Mode Input Impedance at −IN			3.75/3.5		TΩ/pF	C_B
Differential Mode Input Capacitance			2		pF	C_B
Internal Feedback Capacitance			3		pF	C_B
Input Common-Mode Voltage Range (V_{CM})	T_A = −40°C to +125°C	AVSS		AVDD − 1.5V	V	C_B
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0.1 V to 1.5 V	73	87		dB	P
OUTPUT CHARACTERISTICS						
Saturated Output Voltage Swing to AVSS (V_{OUT} − AVSS)	R_F = 10 kΩ			10	mV	P
Saturated Output Voltage Swing to AVDD (AVDD − V_{OUT})	R_F = 10 kΩ			10	mV	P
Short-Circuit Output Current	Sinking/sourcing, V_{OUT} = 1.5 V		27/23		mA	C_B
Linear SW0 and SW1 Current[3]			±30		mA	C_B
DYNAMIC PERFORMANCE						
Gain Bandwidth Product (GBP)			8.5		MHz	C_B
Slew Rate	10% to 90%		8		V/µs	C_B
ANALOG POWER SUPPLIES (AVDD AND AVSS)						
Operating Range V_S = AVDD − AVSS	Guaranteed by power supply rejection ratio (PSRR)	2.7		5.5	V	P
AVSS Range Below DVSS		−2.5		0	V	S
Quiescent Current Per Amplifier			3.05	3.25	mA	P
	T_A = −40°C to +125°C			4.1	mA	C_T
PSRR	Supply voltage (V_S) = 2.7 V to 5.5 V	81	92		dB	P
	V_S = 2.7 V to 5.5 V, T_A = −40°C to +125°C	76			dB	C_T
THRESHOLD VOLTAGES FOR SW SEL						
Input High Voltage (V_{IH})		DVDD − 0.7			V	S
Input Low Voltage (V_{IL})				DVSS + 0.5	V	S
SW SEL Pull-Down Resistance			865		kΩ	C_B
DIGITAL POWER SUPPLIES (DVDD AND DVSS)						

SPECIFICATIONS

Table 2. 3 V Specifications (Continued)

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit	Test Level
Operating Range (DVDD − DVSS)		1.62		5.5	V	P
Quiescent Current				1	µA	P
	T_A = −40°C to +125°C			10	µA	C_T
ANALOG SWITCH CHARACTERISTICS						
Switch On Resistance (R_{ON})			21	25	Ω	P
	T_A = −40°C to +125°C			33	Ω	C_T
Switch On-Resistance Drift	T_A = −40°C to +125°C		0.25		%/°C	C_T
SW0 and SW1 Switch Off Pin Capacitance			1.8		pF	C_B
NOISE						
Input Voltage Noise Density (e_n)	f = 100 kHz		7.3		nV/√Hz	C_B
Integrated Voltage Noise	f = 0.1 Hz to 10 Hz		4.5		µV p-p	C_B

[1] To simplify terminology throughout this data sheet, because the two amplifiers inside the ADA4351-2 are interchangeable, R_{F1}, R_{F0}, SW0, SW1, SW SEL, +IN, and −IN refer to Channel A or Channel B. V_{OUT} refers to OUTA or OUTB, and within each channel, R_F refers to R_{F1} or R_{F0}.

[2] High speed production testing limits the accuracy of this specification.

[3] Linear current is the current that these pins can conduct while V_{OS} shifts by less than 20 µV.

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
Voltage Between Any Two Pins	6 V
DVDD and AVDD to DVSS	−0.3 V to +6 V
DVDD, AVDD, and DVSS to AVSS	−0.3 V to +6 V
+IN and −IN Voltage	AVSS − 1 V to AVDD + 1 V
+IN and −IN Current	10 mA
SW0 and SW1 Voltage	AVSS − 0.3 V to AVDD + 0.3 V
SW SEL Voltage	DVSS − 0.3 V to DVDD + 0.3 V
SW SEL Current	10 mA
Op Amp Output Continuous Current	±20 mA[1], electromigration limited
Switch Continuous Current	±20 mA[1], electromigration limited
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +125°C
Junction, T_J	150°C
Case, T_C	260°C

[1] Specified at 100°C. See the derating curve for temperatures beyond 100°C (see Figure 4).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
CP-16-32	91	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4351-2 is limited by the associated rise in T_J on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses the package exerts on the die, permanently shifting the parametric performance of the ADA4351-2. Exceeding a T_J of 175°C for an extended period can result in changes in the silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package is the sum of the quiescent power dissipation and the power dissipated in the die due to the output load drive of the amplifier.

OUTPUT CURRENT DERATING CURVE

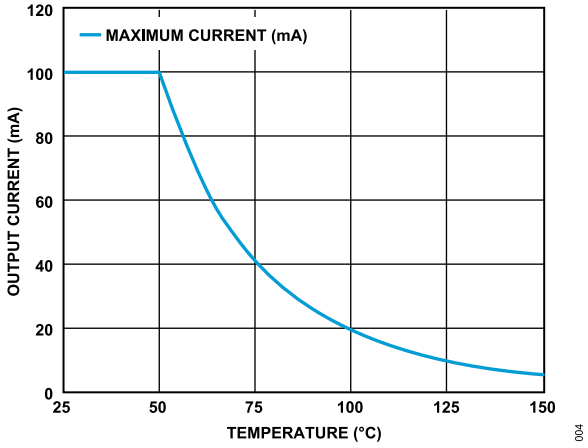


Figure 4. Maximum Output Current Derating Curve vs. Temperature

EXPLANATION OF TEST LEVELS

Table 5. Explanation of Test Levels

Test Level	Description
D	Definition
S	Design verification simulation
P	100% production tested
P_F	Functionally checked during production test
C_T	Characterized on tester
C_B	Characterized on bench

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADA4351-2

Table 6. ADA4351-2, 16-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±2000	1C
FICDM	±1250	C3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

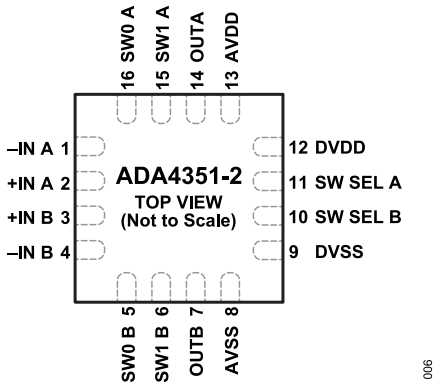


Figure 5. Pin Configuration

Table 7. Pin Function Description

Pin No.	Mnemonic	Description
1	−IN A	Inverting Input of Amplifier A.
2	+IN A	Noninverting Input of Amplifier A.
3	+IN B	Noninverting Input of Amplifier B.
4	−IN B	Inverting Input of Amplifier B.
5	SW0 B	Switch 0 Feedback Pin for Amplifier B.
6	SW1 B	Switch 1 Feedback Pin for Amplifier B.
7	OUTB	Output of Amplifier B.
8	AVSS	Analog Negative Supply Voltage.
9	DVSS	Digital Negative Supply Voltage.
10	SW SEL B	Switch Control for Amplifier B. The SW SEL B pin has an 865 kΩ pull-down resistor to DVSS.
11	SW SEL A	Switch Control for Amplifier A. The SW SEL A pin has an 865 kΩ pull-down resistor to DVSS.
12	DVDD	Digital Positive Supply Voltage.
13	AVDD	Analog Positive Supply Voltage.
14	OUTA	Output of Amplifier A.
15	SW1 A	Switch 1 Feedback Pin for Amplifier A.
16	SW0 A	Switch 0 Feedback Pin for Amplifier A.

TRUTH TABLE

Table 8. Truth Table

SW SEL A	SW SEL B	SW0 A	SW0 B	SW1 A	SW1 B
0	0	On	On	Off	Off
0	1	On	Off	Off	On
1	0	Off	On	On	Off
1	1	Off	Off	On	On

TYPICAL PERFORMANCE CHARACTERISTICS

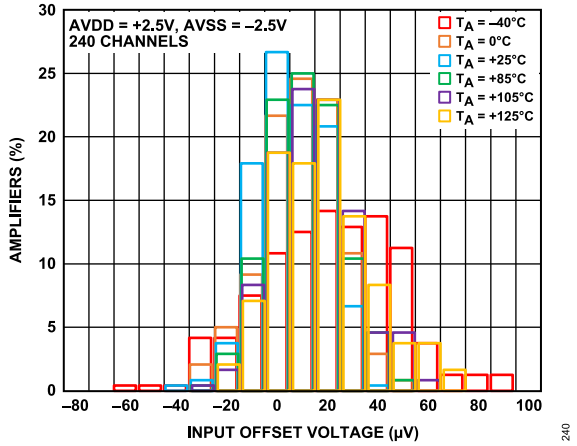


Figure 6. Offset Voltage Distribution, AVDD = +2.5 V, AVSS = –2.5 V

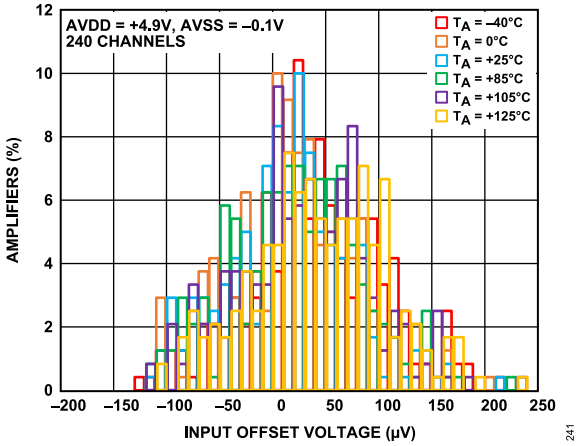


Figure 9. Offset Voltage Distribution, AVDD = +4.9 V, AVSS = –0.1 V

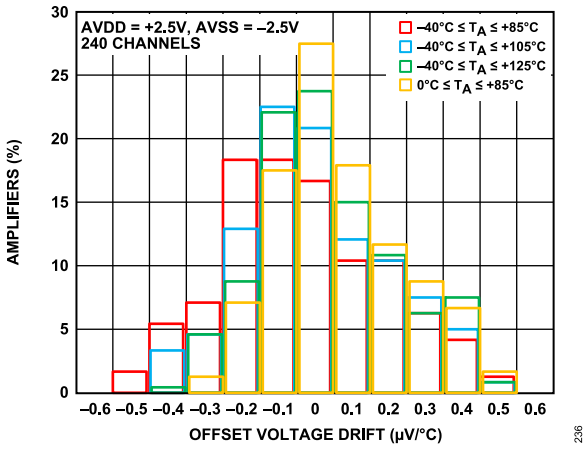


Figure 7. Offset Voltage Drift Distribution, AVDD = +2.5 V, AVSS = –2.5 V

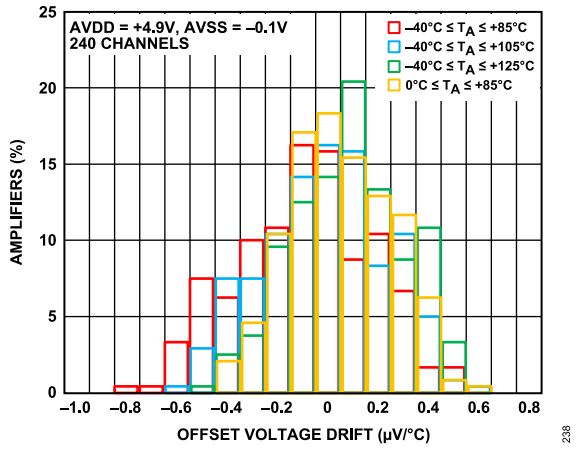


Figure 10. Offset Voltage Drift Distribution, AVDD = +4.9 V, AVSS = –0.1 V

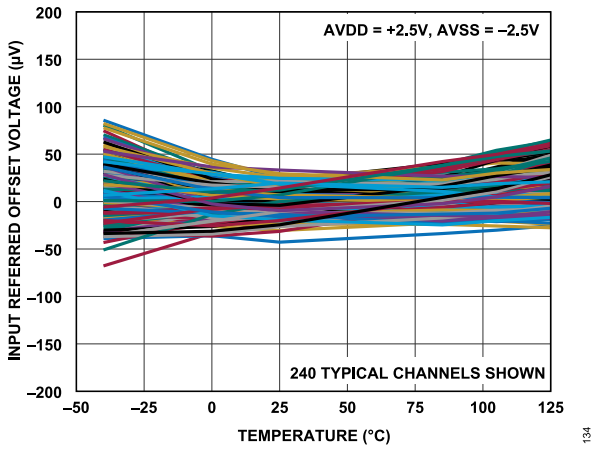


Figure 8. Input Referred Offset Voltage vs. Temperature, AVDD = +2.5 V, AVSS = –2.5 V

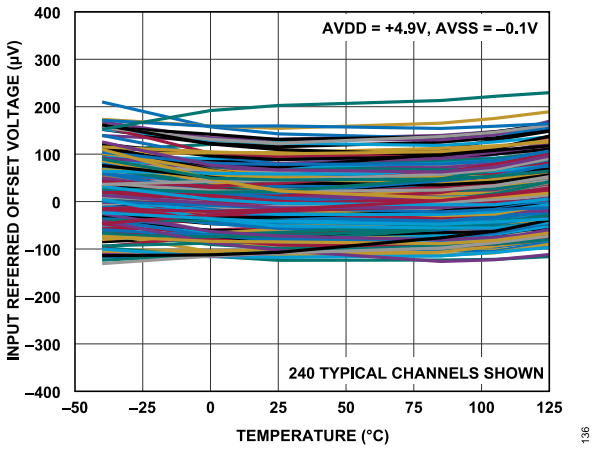


Figure 11. Input Referred Offset Voltage vs. Temperature, AVDD = +4.9 V, AVSS = –0.1 V

TYPICAL PERFORMANCE CHARACTERISTICS

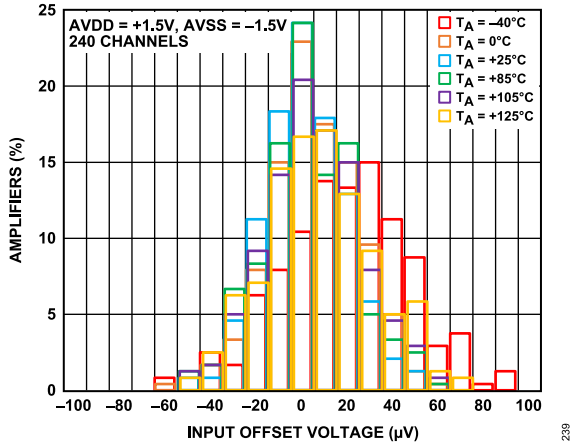


Figure 12. Offset Voltage Distribution, AVDD = +1.5 V, AVSS = –1.5 V

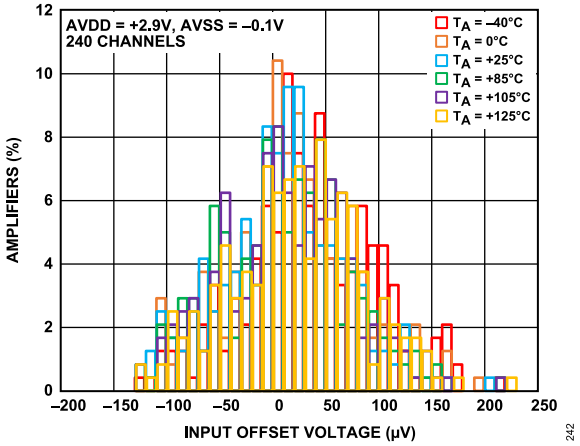


Figure 15. Offset Voltage Distribution, AVDD = +2.9 V, AVSS = –0.1 V

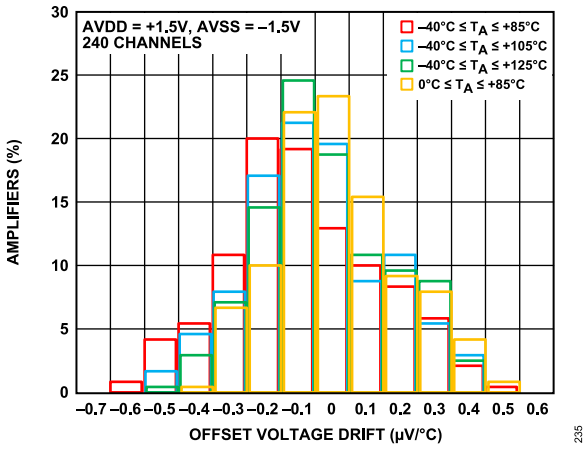


Figure 13. Offset Voltage Drift Distribution, AVDD = +1.5 V, AVSS = –1.5 V

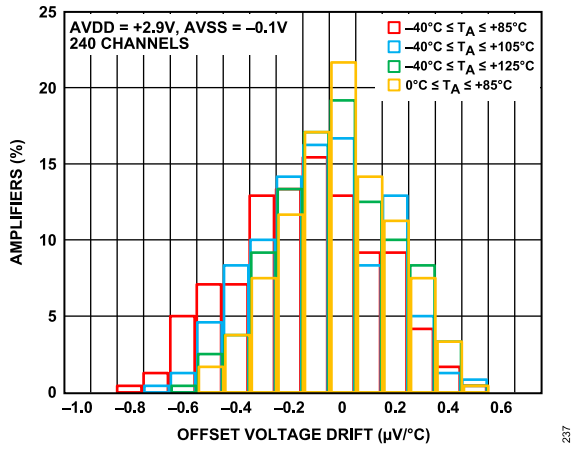


Figure 16. Offset Voltage Drift Distribution, AVDD = +2.9 V, AVSS = –0.1 V

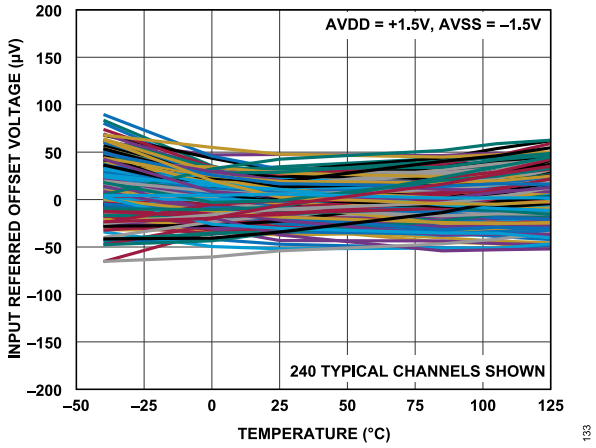


Figure 14. Input Referred Offset Voltage vs. Temperature, AVDD = +1.5 V, AVSS = –1.5 V

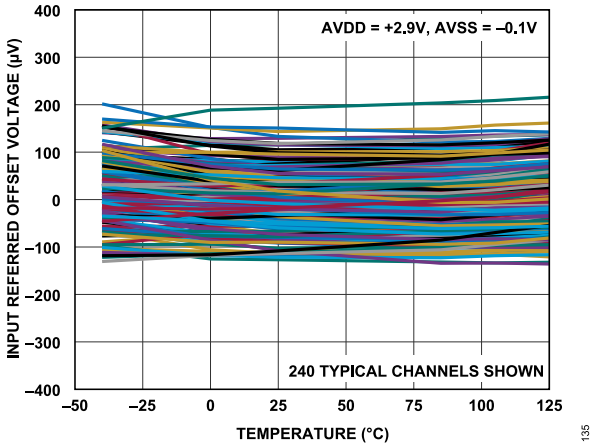


Figure 17. Input Referred Offset Voltage vs. Temperature, AVDD = +2.9 V, AVSS = –0.1 V

TYPICAL PERFORMANCE CHARACTERISTICS

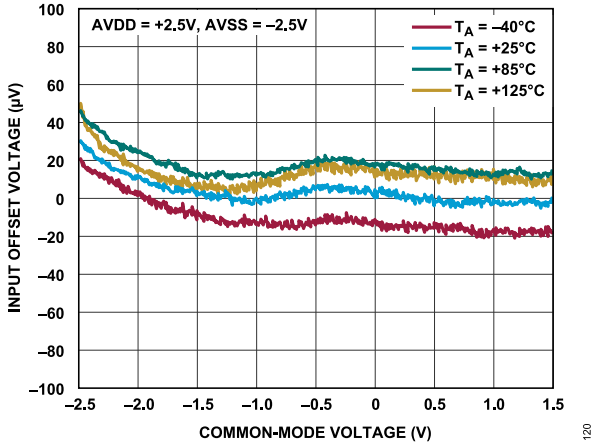


Figure 18. Input Offset Voltage vs. Common-Mode Voltage at Various Temperatures, AVDD = +2.5 V, AVSS = –2.5 V

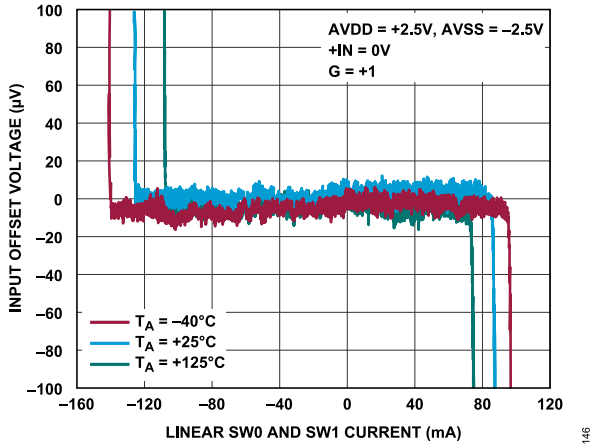


Figure 19. Input Offset Voltage vs. Linear SW0 and SW1 Current at Various Temperatures, AVDD = +2.5 V, AVSS = –2.5 V

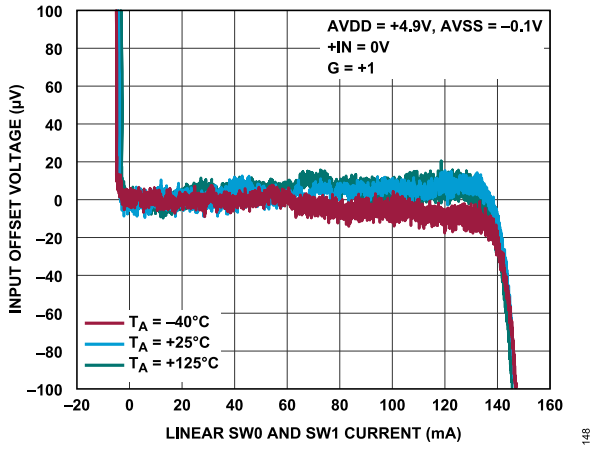


Figure 20. Input Offset Voltage vs. Linear SW0 and SW1 Current at Various Temperatures, AVDD = +4.9 V, AVSS = –0.1 V

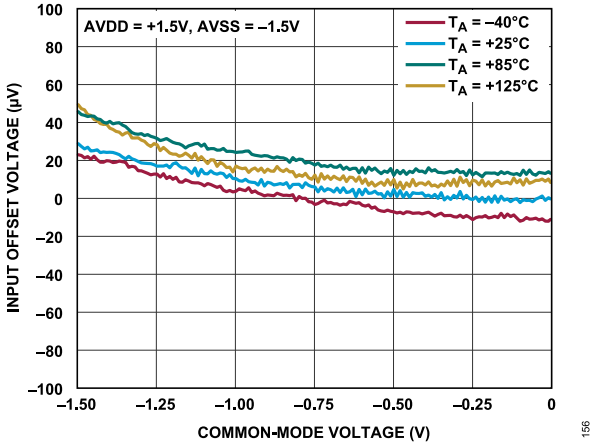


Figure 21. Input Offset Voltage vs. Common-Mode Voltage at Various Temperatures, AVDD = +1.5 V, AVSS = –1.5 V

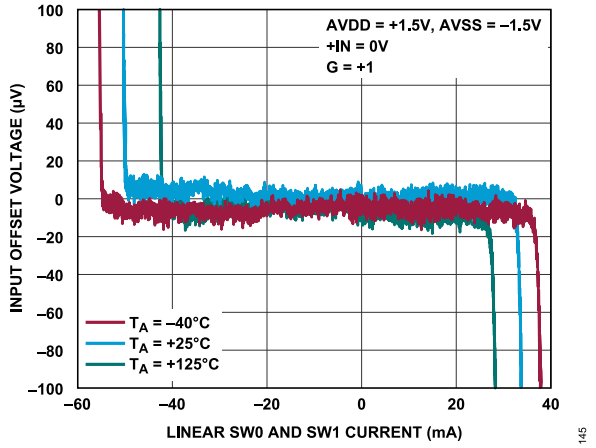


Figure 22. Input Offset Voltage vs. Linear SW0 and SW1 Current at Various Temperatures, AVDD = +1.5 V, AVSS = –1.5 V

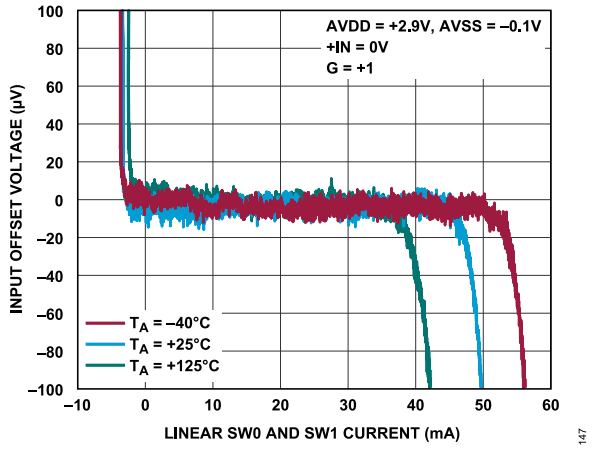


Figure 23. Input Offset Voltage vs. Linear SW0 and SW1 Current at Various Temperatures, AVDD = +2.9 V, AVSS = –0.1 V

TYPICAL PERFORMANCE CHARACTERISTICS

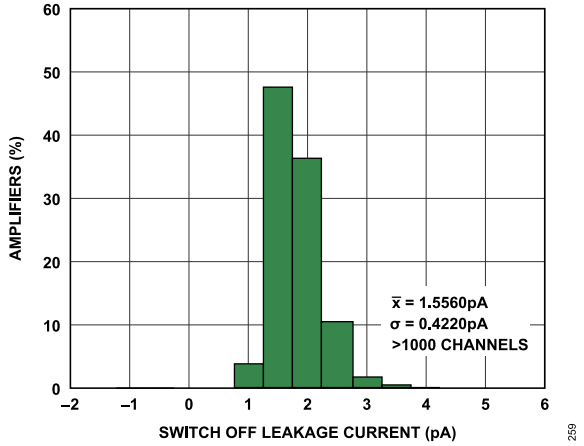


Figure 24. Switch Off Leakage Current Distribution, AVDD = +4.9 V, AVSS = −0.1 V, T_A = 25°C

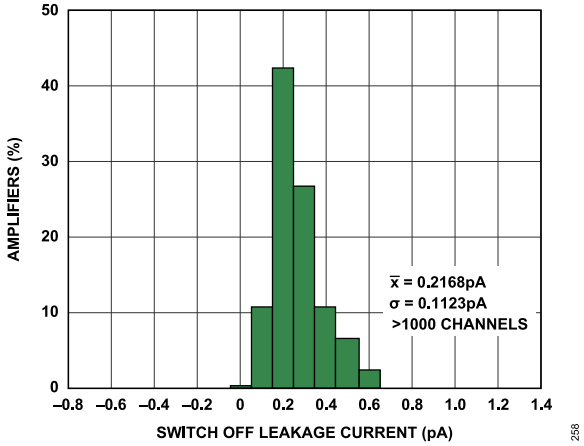


Figure 27. Switch Off Leakage Current Distribution, AVDD = +2.9 V, AVSS = −0.1 V, T_A = 25°C

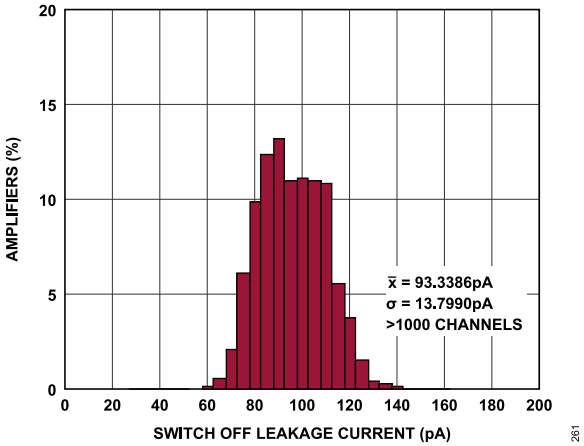


Figure 25. Switch Off Leakage Current Distribution, AVDD = +4.9 V, AVSS = −0.1 V, T_A = 125°C

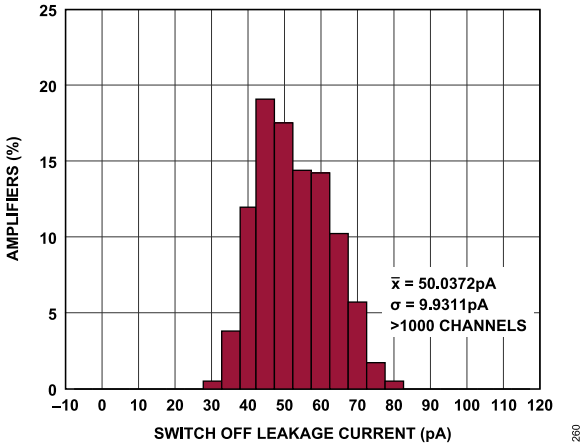


Figure 28. Switch Off Leakage Current Distribution, AVDD = +2.9 V, AVSS = −0.1 V, T_A = 125°C

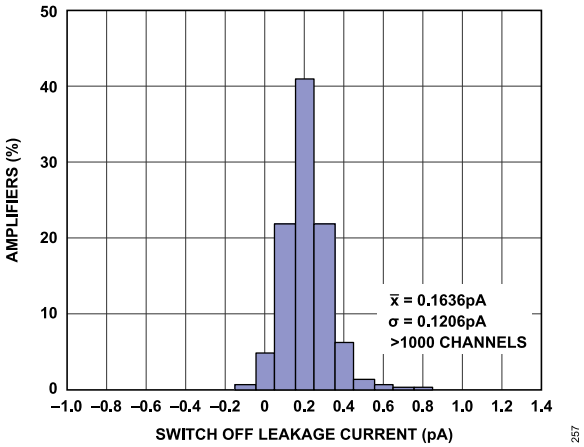


Figure 26. Switch Off Leakage Current Distribution, AVDD = +4.9 V, AVSS = −0.1 V, T_A = −40°C

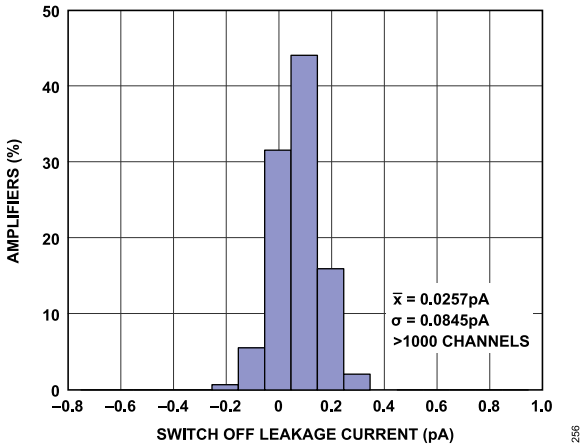


Figure 29. Switch Off Leakage Current Distribution, AVDD = +2.9 V, AVSS = −0.1 V, T_A = −40°C

TYPICAL PERFORMANCE CHARACTERISTICS

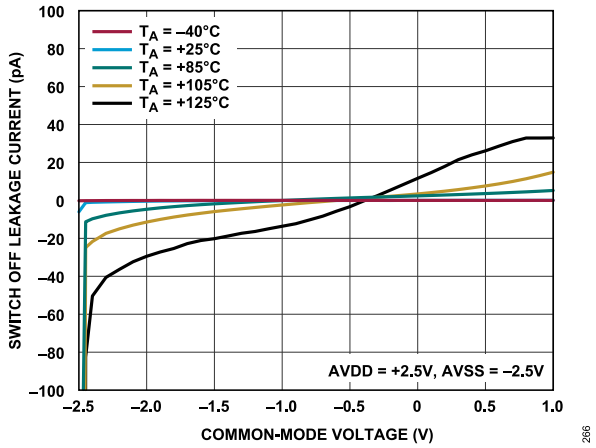


Figure 30. Switch Off Leakage Current vs. Common-Mode Voltage at Various Temperatures, AVDD = +2.5 V, AVSS = −2.5 V

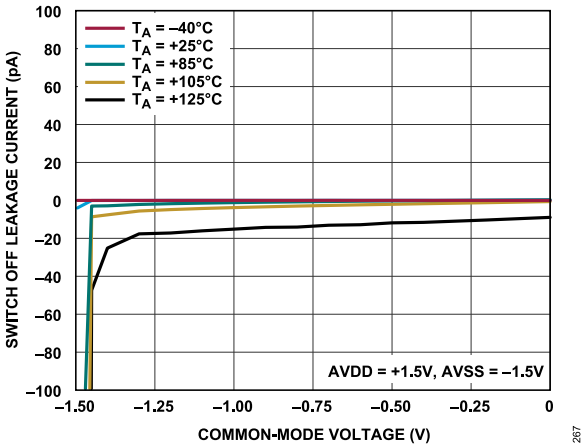


Figure 33. Switch Off Leakage Current vs. Common-Mode Voltage at Various Temperatures, AVDD = +1.5 V, AVSS = −1.5 V

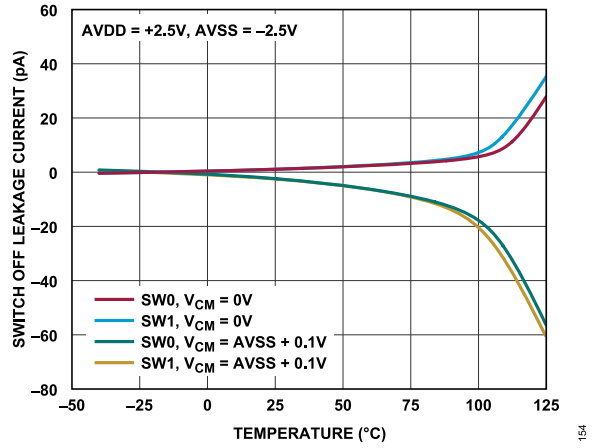


Figure 31. Switch Off Leakage Current vs. Temperature for Various SW0 and SW1 V_{CM} Values, AVDD = +2.5 V, AVSS = –2.5 V

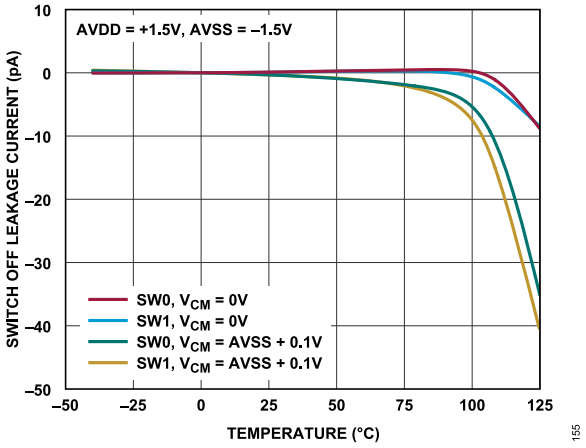


Figure 34. Switch Off Leakage Current vs. Temperature for Various SW0 and SW1 V_{CM} Values, AVDD = +1.5 V, AVSS = –1.5 V

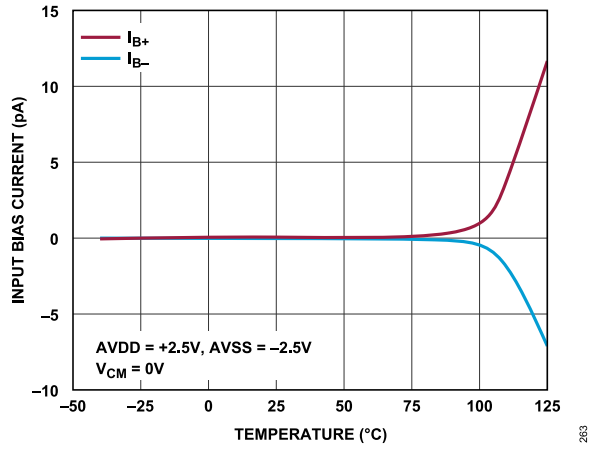


Figure 32. Input Bias Current vs. Temperature, AVDD = +2.5 V, AVSS = −2.5 V

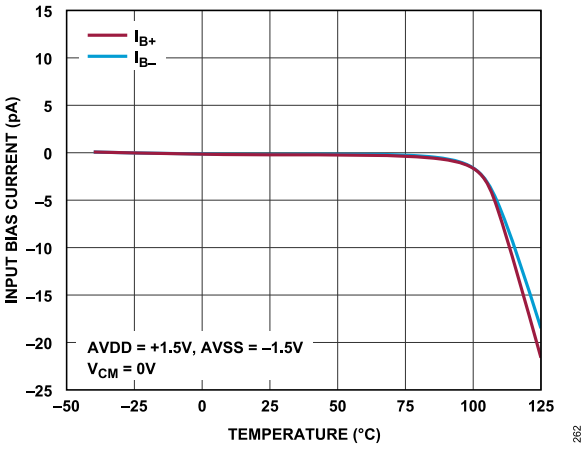


Figure 35. Input Bias Current vs. Temperature, AVDD = +1.5 V, AVSS = −1.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

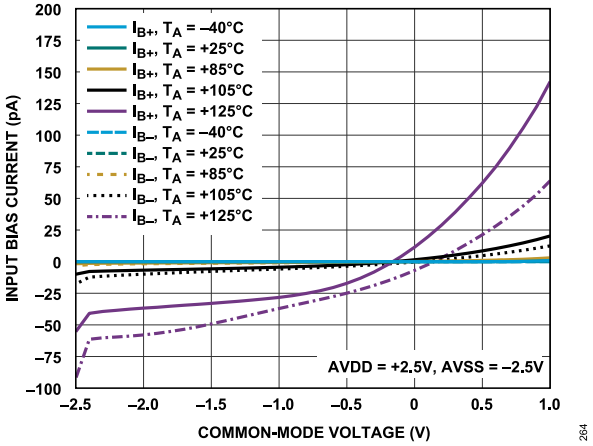


Figure 36. Input Bias Current vs. Common-Mode Voltage at Various Temperatures, AVDD = +2.5 V, AVSS = −2.5 V

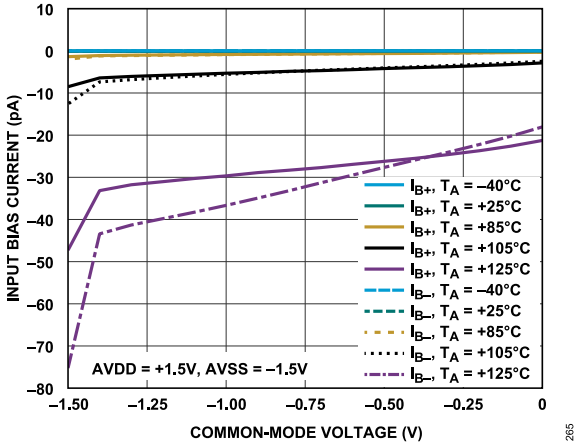


Figure 39. Input Bias Current vs. Common-Mode Voltage at Various Temperatures, AVDD = +1.5 V, AVSS = −1.5 V

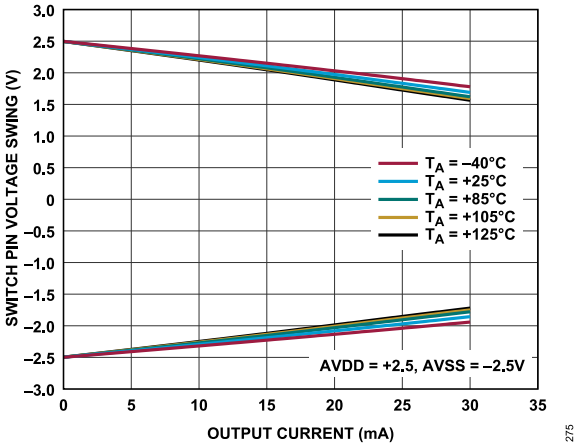


Figure 37. Switch Pin Voltage Swing vs Output Current at Various Temperatures, R_F = 10 kΩ, AVDD = +2.5 V, AVSS = −2.5 V

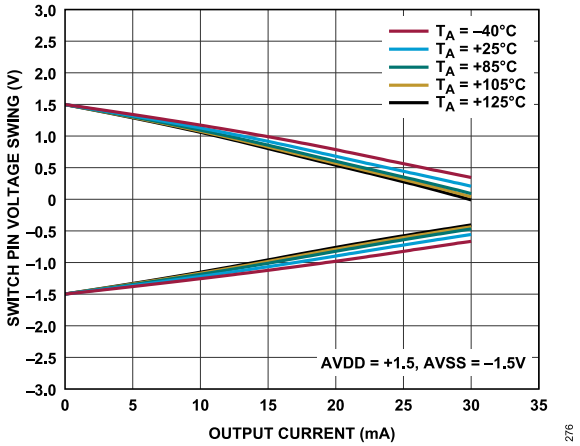


Figure 40. Switch Pin Voltage Swing vs. Output Current at Various Temperatures, R_F = 10 kΩ, AVDD = +1.5 V, AVSS = −1.5 V

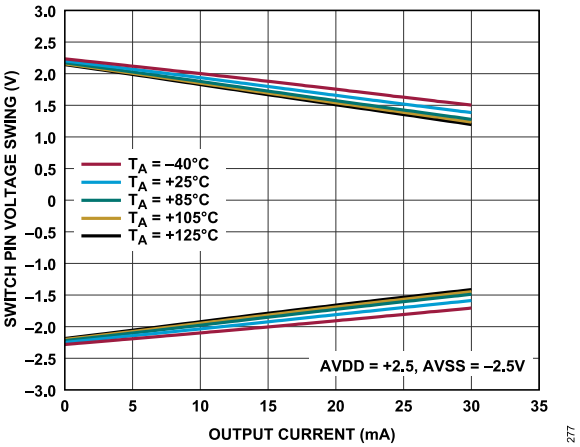


Figure 38. Switch Pin Voltage Swing vs. Output Current at Various Temperatures, R_F = 200 Ω, AVDD = +2.5 V, AVSS = −2.5 V

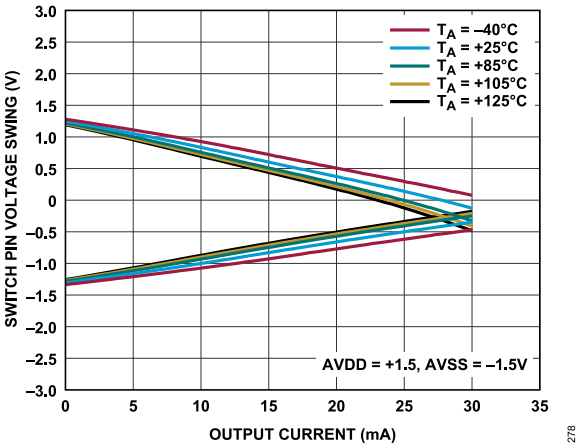


Figure 41. Switch Pin Voltage Swing vs. Output Current at Various Temperatures, R_F = 200 Ω, AVDD = +1.5 V, AVSS = −1.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

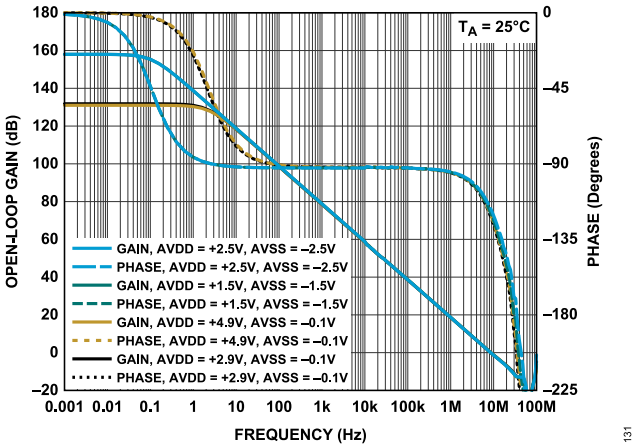


Figure 42. Open-Loop Gain and Phase vs. Frequency at Various Supplies

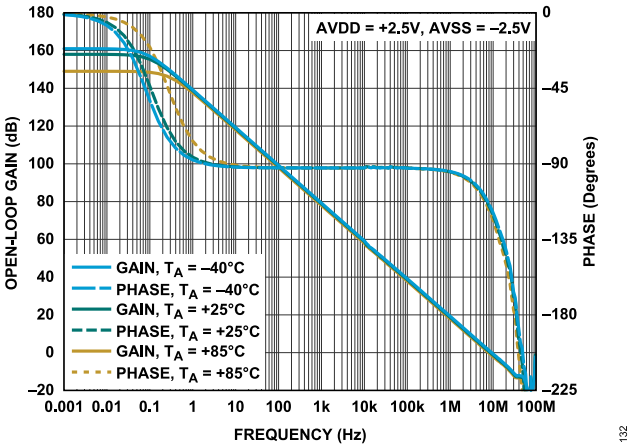


Figure 45. Open-Loop Gain and Phase vs. Frequency at Various Temperatures

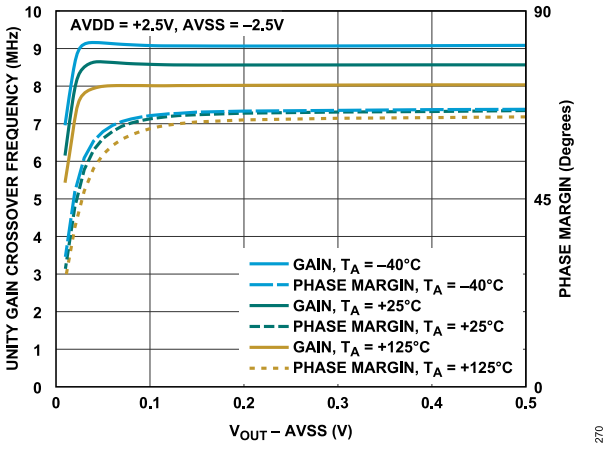


Figure 43. Unity Gain Crossover Frequency and Phase Margin vs. V_{OUT} − AVSS, No Load, AVDD = +2.5 V, AVSS = −2.5 V

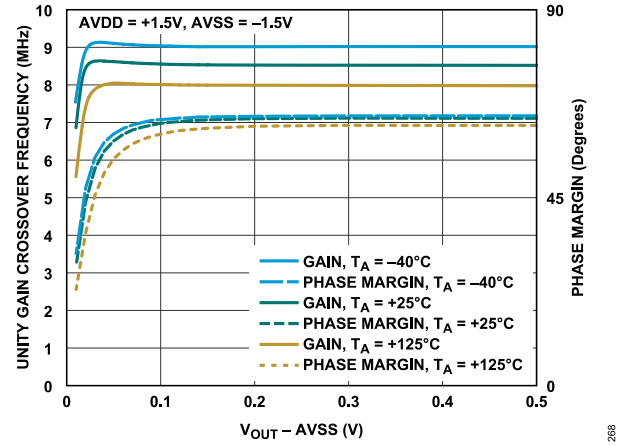


Figure 46. Unity Gain Crossover Frequency and Phase Margin vs. V_{OUT} − AVSS, No Load, AVDD = +1.5 V, AVSS = −1.5 V

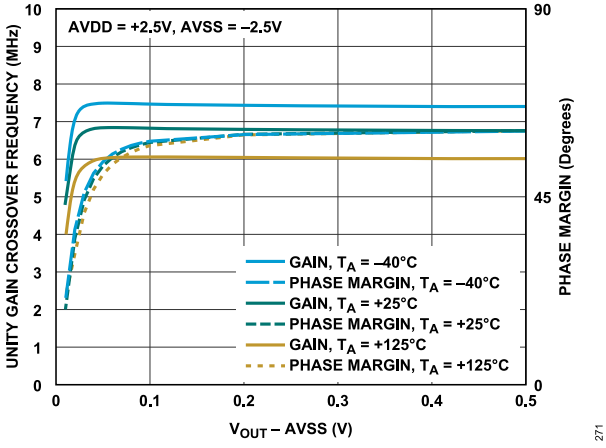


Figure 44. Unity Gain Crossover Frequency and Phase Margin vs. V_{OUT} − AVSS, Load = Low-Pass Output Filter (R_{EXT} = 25 Ω, C_{EXT} = 1 nF), AVDD = +2.5 V, AVSS = −2.5 V

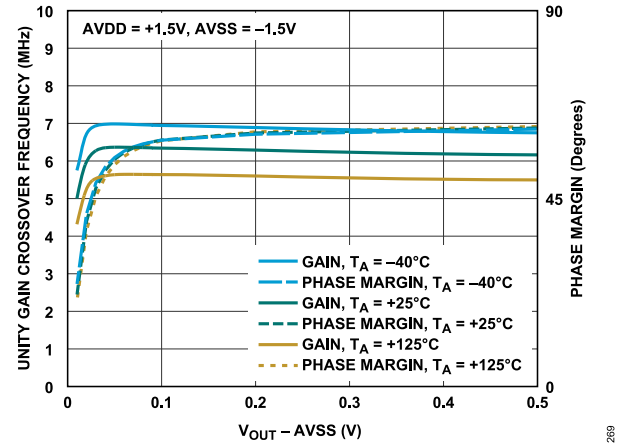


Figure 47. Unity Gain Crossover Frequency and Phase Margin vs. V_{OUT} − AVSS, Load = Low-Pass Output Filter (R_{EXT} = 25 Ω, C_{EXT} = 1 nF), AVDD = +1.5 V, AVSS = −1.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

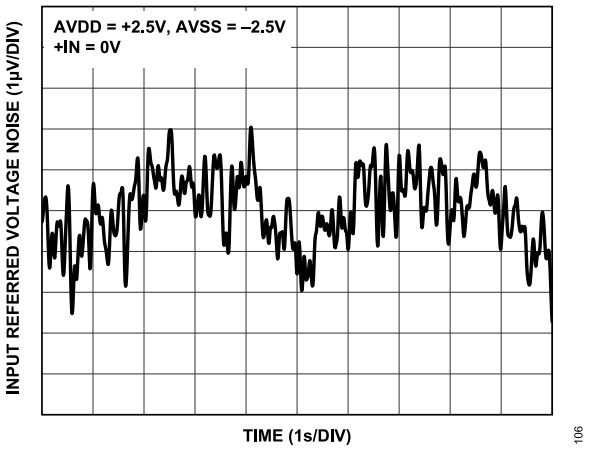


Figure 48. 0.1 Hz to 10 Hz Voltage Noise, AVDD = +2.5 V, AVSS = –2.5 V

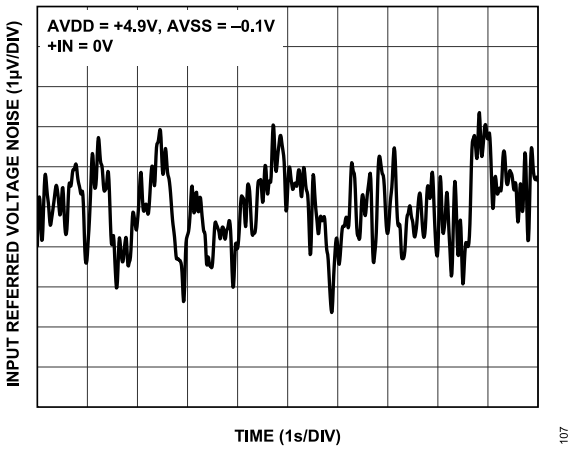


Figure 51. 0.1 Hz to 10 Hz Voltage Noise, AVDD = +4.9 V, AVSS = –0.1 V

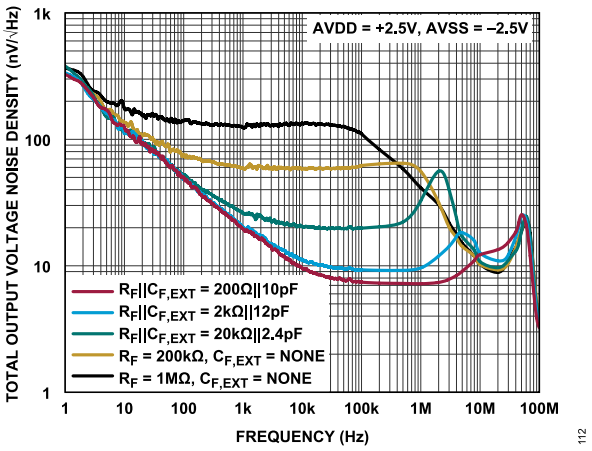


Figure 49. Total Output Voltage Noise Density vs. Frequency, AVDD = +2.5 V, AVSS = –2.5 V

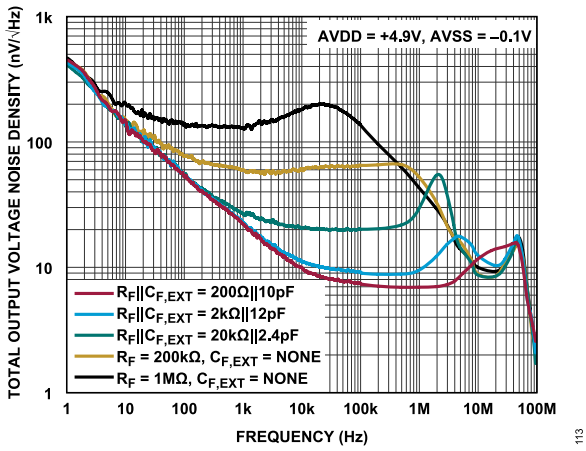


Figure 52. Total Output Voltage Noise Density vs. Frequency, AVDD = +4.9 V, AVSS = –0.1 V

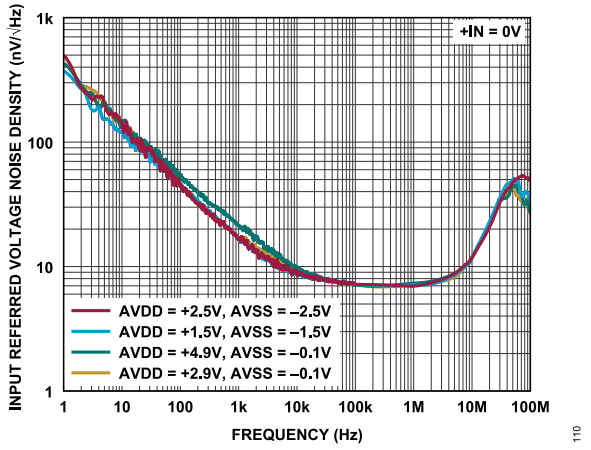


Figure 50. Input Referred Voltage Noise Density vs. Frequency

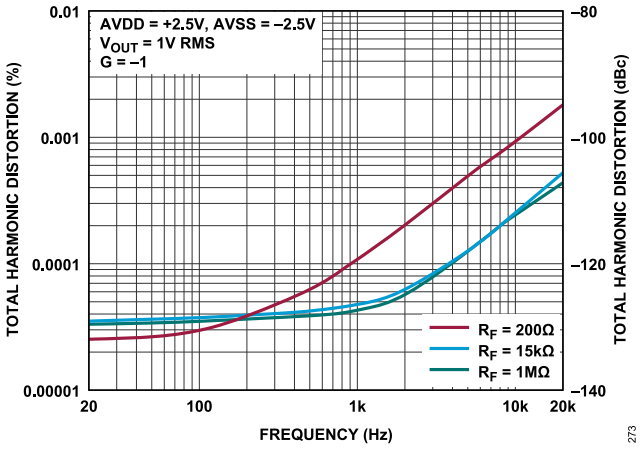


Figure 53. Total Harmonic Distortion vs. Frequency, AVDD = +2.5 V, AVSS = −2.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

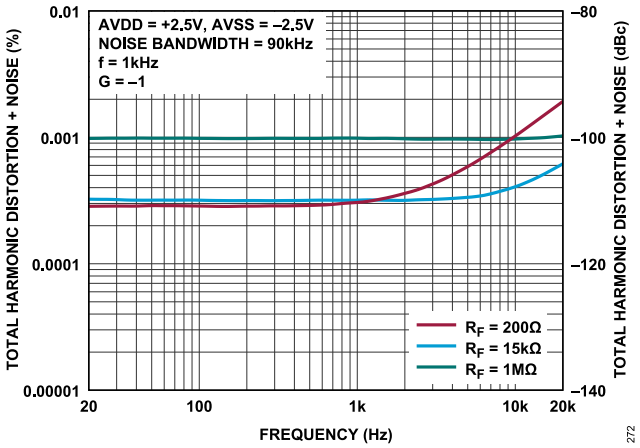


Figure 54. Total Harmonic Distortion + Noise vs. Frequency, AVDD = +2.5 V, AVSS = −2.5 V

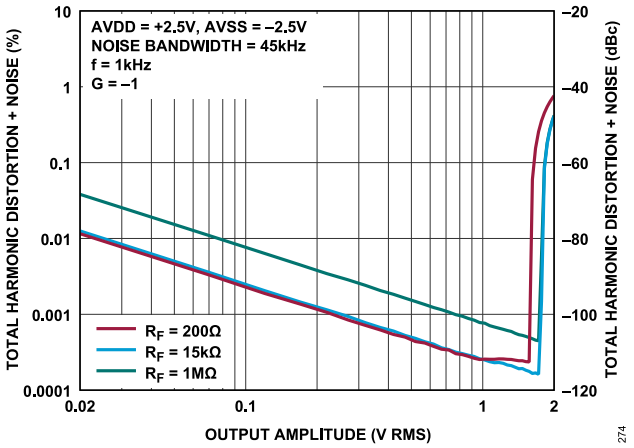


Figure 57. Total Harmonic Distortion + Noise vs. Output Amplitude, AVDD = +2.5 V, AVSS = −2.5 V

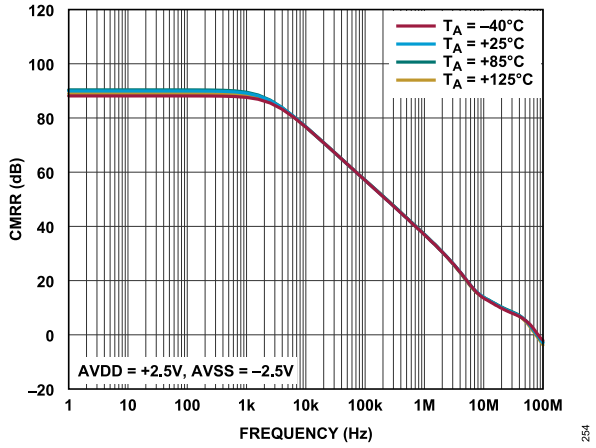


Figure 55. CMRR vs. Frequency over Various Temperatures, AVDD = +2.5 V, AVSS = −2.5 V

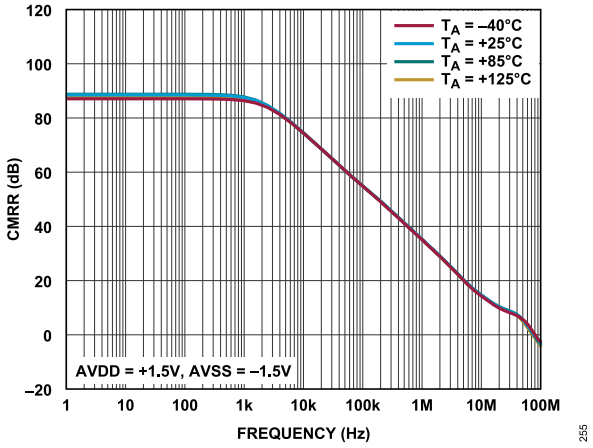


Figure 58. CMRR vs. Frequency over Various Temperatures, AVDD = 1.5 V, AVSS = −1.5 V

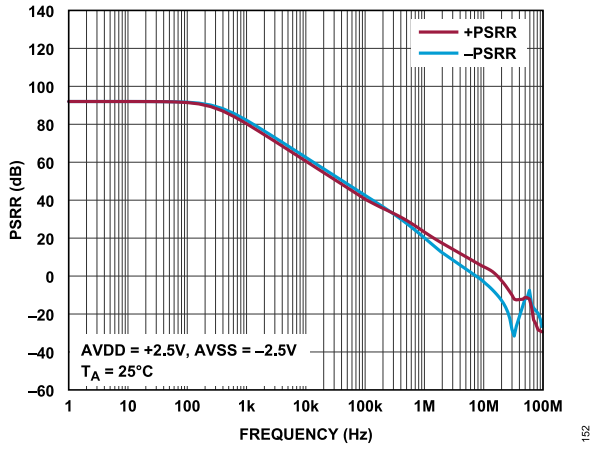


Figure 56. PSRR vs. Frequency, AVDD = +2.5 V, AVSS = –2.5 V

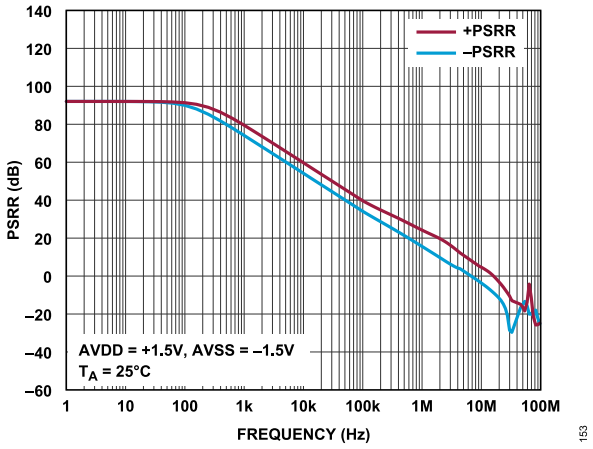


Figure 59. PSRR vs. Frequency, AVDD = +1.5 V, AVSS = –1.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

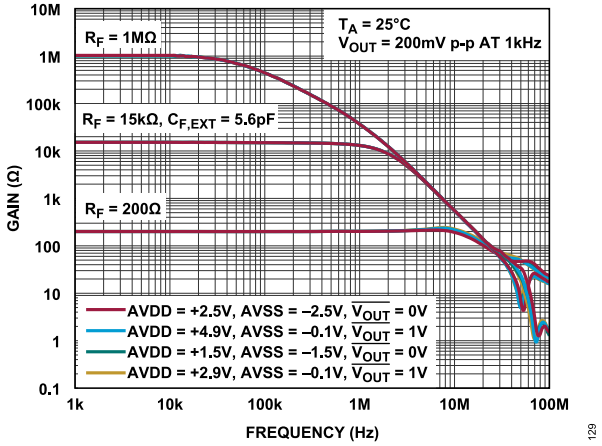


Figure 60. Small Signal Closed-Loop Gain vs. Frequency at Various Supplies

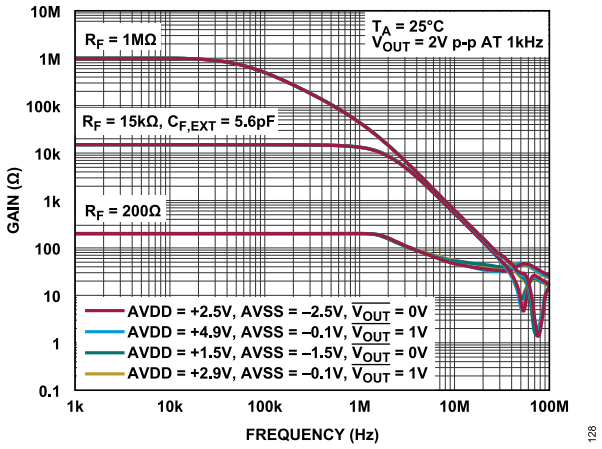


Figure 61. Large Signal Closed-Loop Gain vs. Frequency at Various Supplies

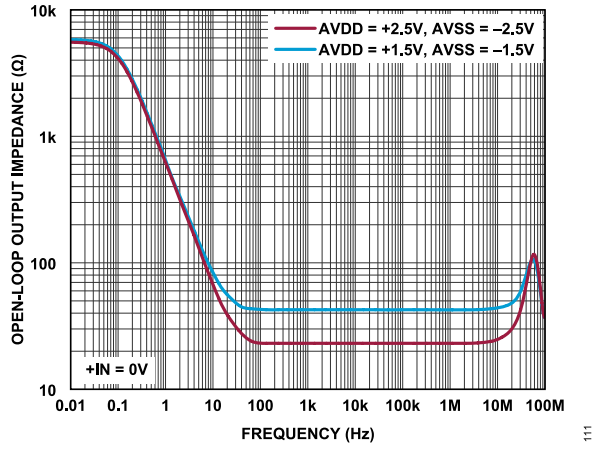


Figure 62. Open-Loop Output Impedance vs. Frequency

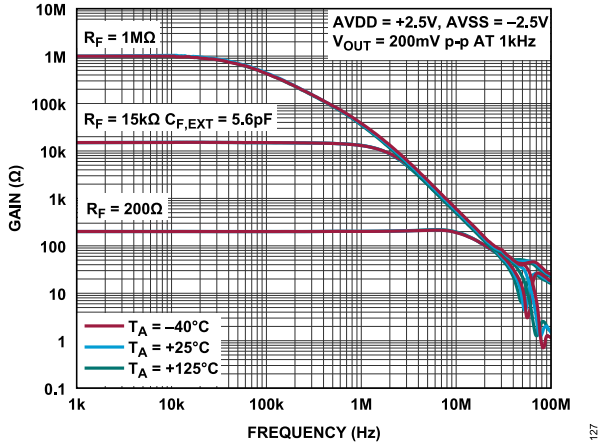


Figure 63. Small Signal Closed-Loop Gain vs. Frequency at Various Temperatures

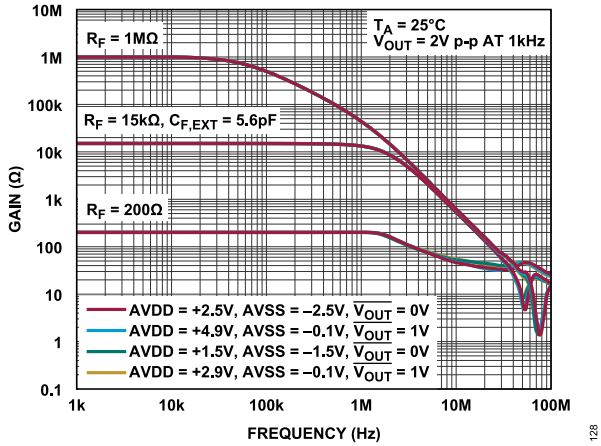


Figure 64. Large Signal Closed-Loop Gain vs. Frequency at Various Temperatures, AVDD = +2.5 V, AVSS = –2.5 V

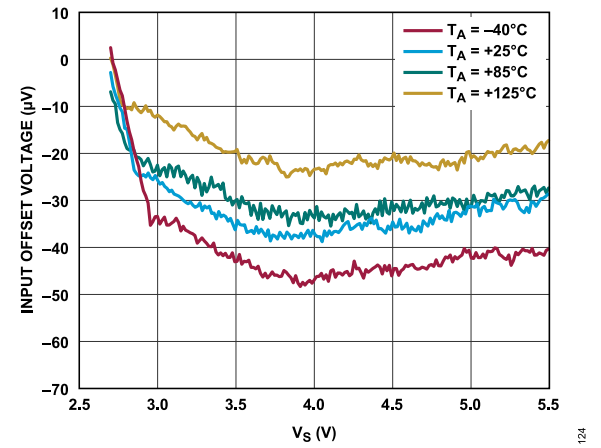


Figure 65. Input Offset Voltage vs. Analog Supply Voltage (V_S)

TYPICAL PERFORMANCE CHARACTERISTICS

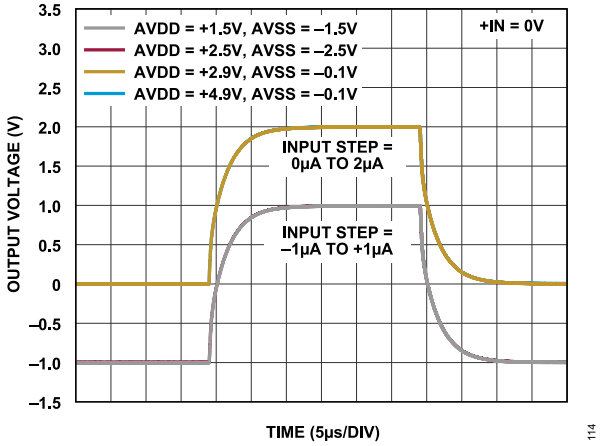


Figure 66. Large-Signal Step Response at Various Supplies, Input Capacitance (C_{IN}) = 10 pF, R_F = 1 MΩ

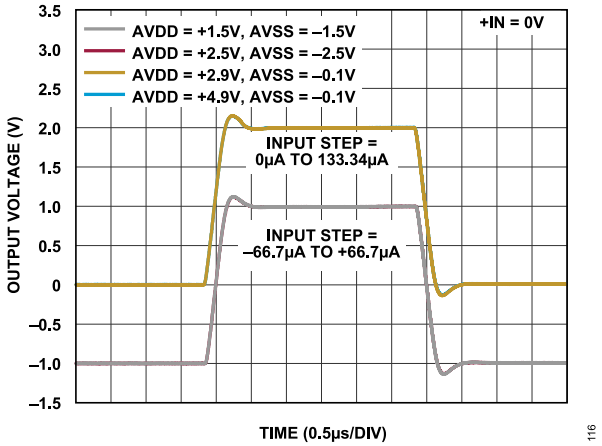


Figure 67. Large-Signal Step Response at Various Supplies, C_{IN} = 10 pF, R_F = 15 kΩ, External Feedback Capacitance ($C_{F,EXT}$) = 5.6 pF

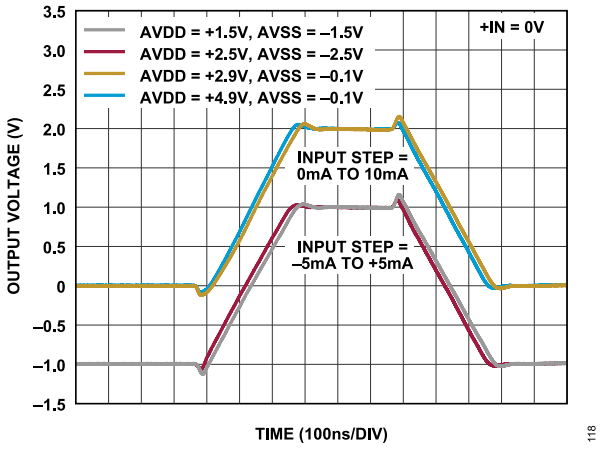


Figure 68. Large-Signal Step Response at Various Supplies, C_{IN} = 10 pF, R_F = 200 Ω

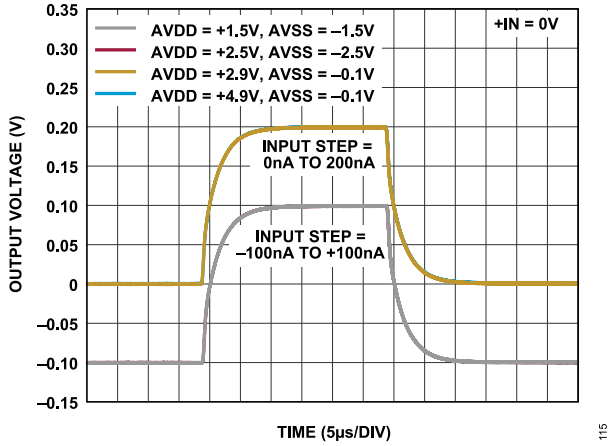


Figure 69. Small-Signal Step Response at Various Supplies, C_{IN} = 10 pF, R_F = 1 MΩ

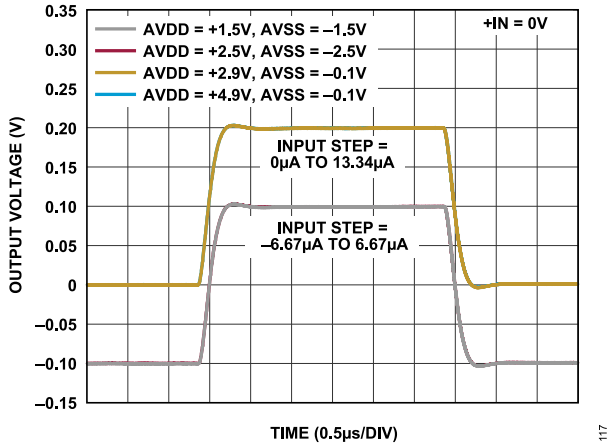


Figure 70. Small-Signal Step Response at Various Supplies, C_{IN} = 10 pF, R_F = 15 kΩ, $C_{F,EXT}$ = 5.6 pF

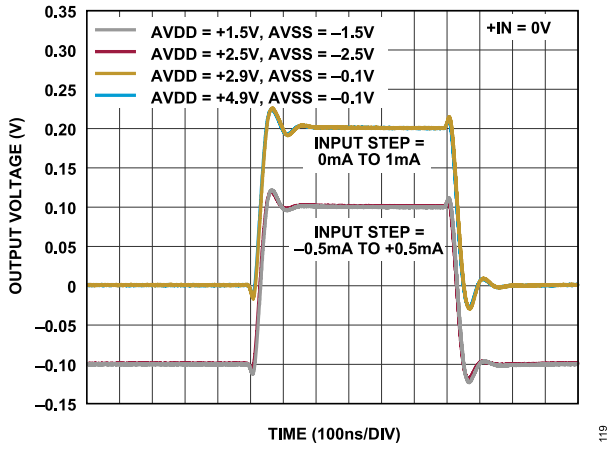


Figure 71. Small-Signal Step Response at Various Supplies, C_{IN} = 10 pF, R_F = 200 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

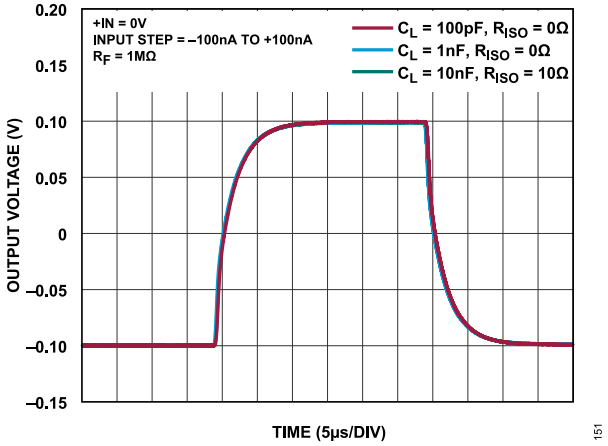


Figure 72. Small Signal Response for Various Capacitive Load (C_L) and Series Isolation Resistor (R_{ISO}) Values, R_F = 1 MΩ

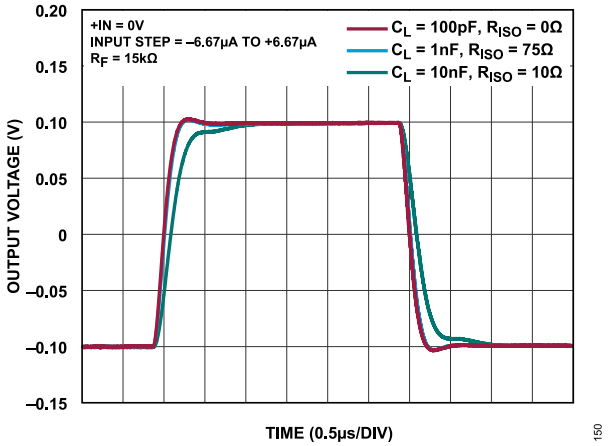


Figure 73. Small Signal Response for Various C_L and R_{ISO} Values, R_F = 15 kΩ, $C_{F,EXT}$ = 5.6 pF

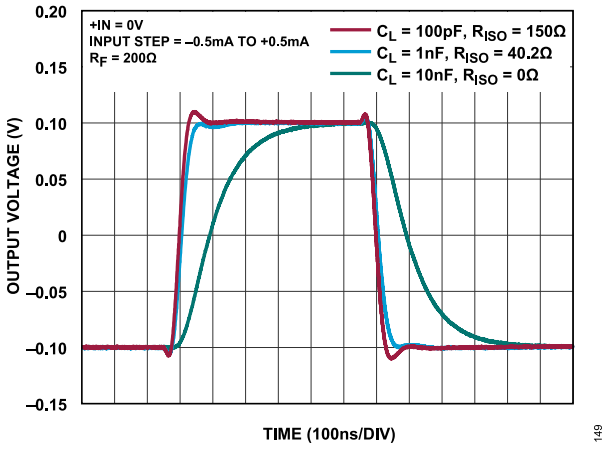


Figure 74. Small Signal Response for Various C_L and R_{ISO} Values, R_F = 200 Ω, $C_{F,EXT}$ = 47 pF

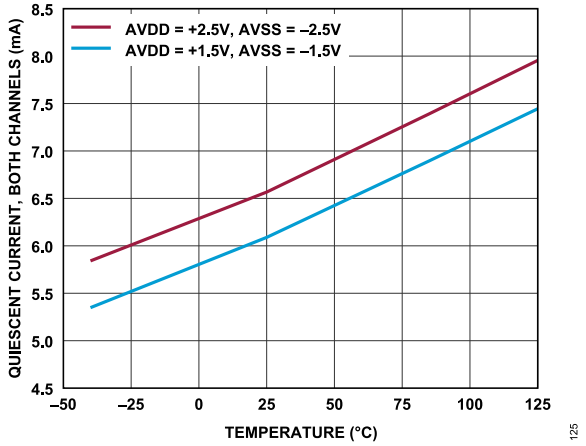


Figure 75. AVDD Quiescent Current, Both Channels vs. Temperature

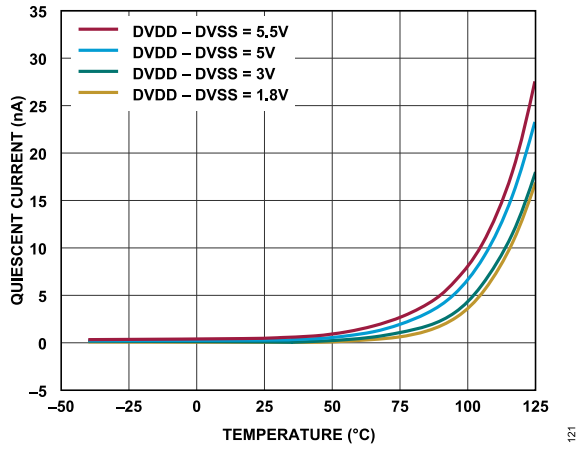


Figure 76. DVDD Quiescent Current vs. Temperature

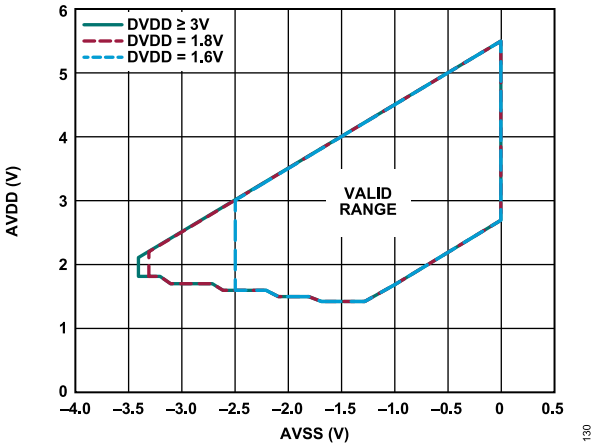


Figure 77. Valid Operating Range for AVSS Below DVSS, DVSS = 0 V

THEORY OF OPERATION

OVERVIEW

The ADA4351-2 is a small, dual-channel precision PGTIA designed to maximize system dynamic range by minimizing errors associated with a PGTIA signal chain while reducing overall PCB footprint requirements. The main amplifier has low offset voltage over temperature, low noise, and low input bias current and is designed to drive an analog-to-digital converter (ADC) directly. The proprietary low off-leakage switches used to select one of two feedback paths outperform typical CMOS switches of similar size and on resistance. The switches are arranged in a Kelvin configuration that removes the nonlinear behavior of the CMOS switch on resistance from the transfer function. With two possible external feedback paths and a direct ADC drive, this dual-channel PGTIA significantly reduces the PCB footprint requirements compared to a discrete solution. Additionally, the PGTIA is internally compensated with a 3 pF internal feedback capacitor for gains >50 kΩ, assuming a source capacitance (C_S) of approximately 10 pF, which eliminates the need for an external compensation capacitor, in most cases, further reducing the required PCB footprint.

The analog circuitry operates on either a single supply (+2.7 V to +5.5 V) or a dual supply (±1.35 V to ±2.75 V) with a rail-to-rail output stage and a negative-rail input stage to provide user flexibility for unidirectional or bidirectional input current signals as well as directly driving an ADC with a voltage reference up to 5.5 V. The digital input (switch control) operates on supplies between 1.62 V and 5.5 V to interface directly with standard logic levels (1.8, 3.3, or 5) based on the voltage applied to the digital supply (DVSS and DVDD). The voltage levels required for a logic low or high value (V_{IH}/V_{IL}) are based on the digital input voltage (SW SEL) relative to the corresponding digital rail (DVSS and DVDD).

The switches for Channel A and Channel B of the ADA4351-2 are controlled by the digital inputs, SW SEL A and SW SEL B, respectively. The logic low and high threshold is based on the digital power supply voltages (DVSS and DVDD, see Table 1 and Table 2 for more information). The digital supplies in the ADA4351-2 are included to provide the user flexibility to control the switch logic separately from the analog supply range as these two ranges are not typically the same. The ADA4351-2 includes level shifting circuitry to translate the switch control signals from digital domain to the analog domain which simplifies the design compared to a discrete solution. The two internal switch selections are make-before-break to maintain a closed feedback loop during switching to eliminate output overdrive glitches that would otherwise occur.

To simplify terminology, because the two amplifiers inside the ADA4351-2 are interchangeable, R_{F1}, R_{F0}, SW0, SW1, SW SEL, +IN, and −IN refer to Channel A or Channel B. V_{OUT} refers to OUTA or OUTB, and within each channel, R_F refers to R_{F1} or R_{F0}.

PGTIA ERRORS

PGTIA Measurements

The ADA4351-2 is designed for high accuracy transimpedance measurements for TIA gains from 200 Ω to beyond 10 MΩ. Because different and competing error sources dominate at the extremes of TIA gains, the ADA4351-2 is designed to be optimal for any gain configuration (see the Switch Off Leakage Current section for additional information). For lower TIA gain values, the dominant output DC error source is the input offset voltage, while for higher TIA gain values, the dominant output DC error source is the input bias current and the switch off leakage current. The following sections outline the leading errors in a PGTIA circuit.

The PGTIA circuit (see Figure 78) models a capacitive sensor with a current source (that is, a photodiode) into the inverting junction of a closed-loop op amp. This virtual ground passes the +IN bias voltage over to the inverting summing junction as part of the diode bias voltage and sinks all of the photodiode current from the output pin through the feedback resistor. The photodiode is modeled as a shunt capacitance (C_D) and shunt resistance (R_{SH}) in parallel with the current source. Any signal current from the sensor flows through the selected feedback path of the PGTIA, where the ideal transfer function of the PGTIA is V_{OUT} = diode current (I_D) × R_{F0} (because the R_{F0} gain path is selected). When photodiode DC dark current (I_{DARK}) is significant, such as when a large reverse bias voltage ($-V_B$) is applied), it may also be included in the source model.

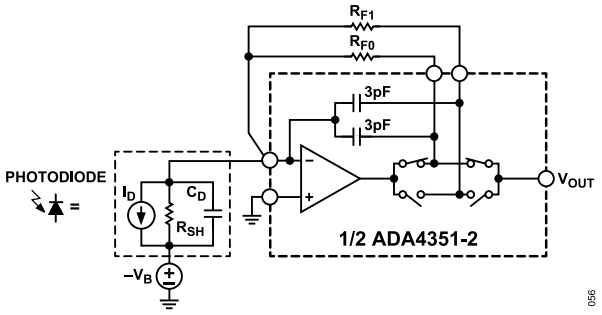


Figure 78. PGTIA Circuit

Offset Voltage

The offset voltage of the amplifier in a PGTIA limits the minimum detectable signal in the system at low gains. The error at the output of the PGTIA due to the amplifier TIA offset is gained up by the (DC) noise gain of the amplifier ($1 + R_F/R_{SH}$ for a typical inverting amplifier), where R_{SH} is any shunt resistance in the photodiode model. For $R_{SH} >> R_F$, this reduces to 1. Because the offset is a voltage error, it impacts the usable and accurate codes of the ADC for all TIA gains in a similar way. The ADA4351-2 uses proprietary in-package offset and offset-drift trim that allow it to achieve a maximum of 100 µV offset voltage at 25°C and 0.85 µV/°C drift from −40°C to +125°C at a 5 V supply.

THEORY OF OPERATION

For example, a 16-bit ADC with a 4.5 V reference has a 68.7 µV step size. If R_{SH} = 10 MΩ, for R_F = 1 MΩ, the output-referred offset is 100 µV × (1 + 1 MΩ/10 MΩ) = 110 µV, while the same circuit with an R_F = 1 kΩ has a 25°C maximum 100.01 µV of output-referred offset. In both cases, the output-referred offset is less than 2 codes indicating that the output error due to the offset voltage is relatively fixed vs. the R_F value. The ±0.85 µV/°C (−40°C to +125°C) maximum leads to a 140 µV shift maximum over the full −40°C to +125°C span, or a worst case of 2 codes.

Input Bias Current

Input bias current (I_B) adds to the total output DC error if the TIA gain (R_F) or +IN source resistance (R_S) are large enough to exceed this relatively small input offset voltage related error. These input bias currents increase exponentially with T_J where operating at <105°C is a typical constraint for improved accuracy. On the inverting input, I_B adds with switch off leakage current (I_{OFF}) from the inactive channel, refer to Figure 79, summing back from the inactive feedback channel into the active channel. If the inactive channel does not have a feedback resistor installed, ignore this additive term. Adding the maximum ±50 pA switch off leakage to the ±70 pA inverting input bias current (−40°C to +105°C) adds an output error greater than the 100 µV maximum offset voltage error for R_F values > 100 µV/120 pA = 883 kΩ.

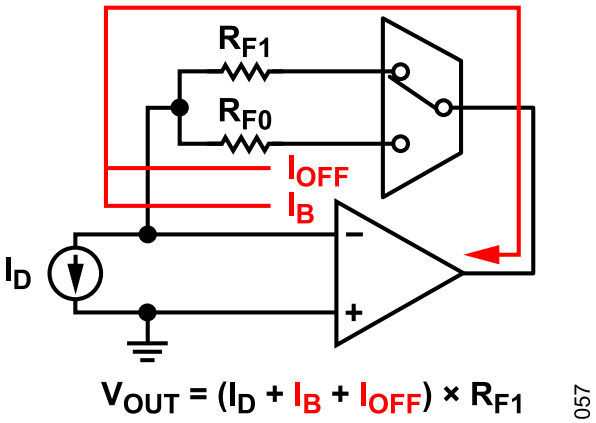


Figure 79. Error Currents in Switched Gain Transimpedance Amplifier

Similarly, the input bias current from the noninverting input (maximum 110 pA from −40°C to +125°C) has negligible impact on the TIA circuit if the bias current induces error less than the 100 µV offset voltage error, which occurs when the sensor output impedance (R_S) is less than 100 µV/110 pA = 909 kΩ. When using the ADA4351-2 to measure a high impedance voltage sensor at the noninverting input, as shown in Figure 80, this may not be the case. Instead, the input bias current results in a voltage error at the noninverting input equal to the sensor output impedance times the bias current. This voltage error adds to the input offset voltage error and is gained up to the output by the noninverting signal gain of the circuit (1 + R_F/gain resistor (R_G)).

Note that the contribution of the input bias current to the DC error is normally a trivial design constraint, and in many cases, is usually dominated by that of the offset voltage.

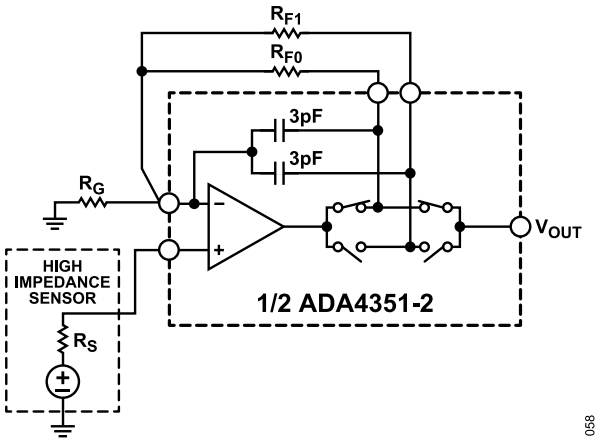


Figure 80. Using the ADA4351-2 to Measure a High Impedance Voltage Output Sensor at the Noninverting Input

Typically for an amplifier with CMOS input devices, the input bias current is dominated by the electrostatic discharge (ESD) protection diodes. For the ADA4351-2, the input protection diodes are bootstrapped to reduce the reverse-biased leakage of these protection diodes that results in the specified low input bias current, as shown in Figure 81.

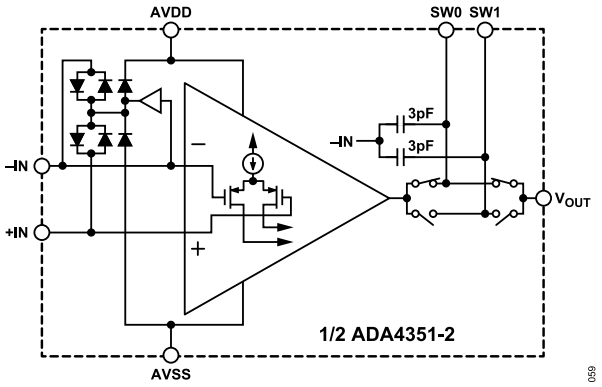


Figure 81. Using Bootstrapped ESD Protection Diodes to Reduce Input Bias Current

As temperature increases, the input bias current due to the ESD protection diodes increases exponentially. The input bias current for the inverting input ADA4351-2 is <70 pA up to 105°C at a 5 V supply. Using a 100 µV maximum input offset voltage, this error term is less than V_{OS} for R_F < 1.42 MΩ. This maximum input bias current increases to 100 pA over the full −40°C to 125°C range adding more error to the output voltage.

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Switch Off Leakage Current

In a PGTIA, the I_{OFF} of the switches also adds to the total error current in the system. The I_{OFF} increases exponentially with temperature. For a CMOS switch, there is a trade-off between on resistance (R_{ON}) and I_{OFF}. For systems that require the use of low R_F values, minimize the gain error by using a low R_{ON} switch. However, a system with a large R_F value is much more sensitive to I_{OFF} and requires a switch with a lower I_{OFF}, and therefore, higher R_{ON}. Another important aspect of CMOS switches is the I_{OFF} when operating the switch near the supply rail. Typical CMOS switches exhibit excessive leakage when operating within 0.5 V from the supply rail and, therefore, the leakage is not typically specified in this region. Not only does the ADA4351-2 have low I_{OFF} switches (considering their low R_{ON}), but also the low leakage performance extends to 0.1 V from the rail, yielding a wider usable range for the TIA circuit.

Improved TIA Gain Accuracy Using a Kelvin Connection for Channel Select

A typical switched gain TIA places the switches in series with the different feedback resistors (see Figure 82), and therefore, the switch on resistance is part of the transimpedance gain function. The improved Kelvin approach used in the ADA4351-2 (see Figure 83) places half of the switches inside the loop to provide a Kelvin connection. The on resistance of the left side switch shown in Figure 83 then becomes part of the open-loop output impedance and is corrected by the loop gain of the amplifier. Using the typical open-loop gain (A_{OL}) of 158 dB and the DC noise gain of 1 in a TIA, the maximum on resistance of 19 Ω gives a vastly lower error term of 19 Ω/(1 + $10^{158/20}$) = 0.24 µΩ to the output. Assuming no load current, the on resistance of the right side switch does not contribute any IR drop, so the voltage at the output is $I_D \times R_F$. The SW0 and SW1 pins have internal series resistances of 0.2 Ω and 0.56 Ω, respectively. To minimize parasitic resistance error, connect the lower of the external R_F values to the pin with the lower internal resistance, SW0.

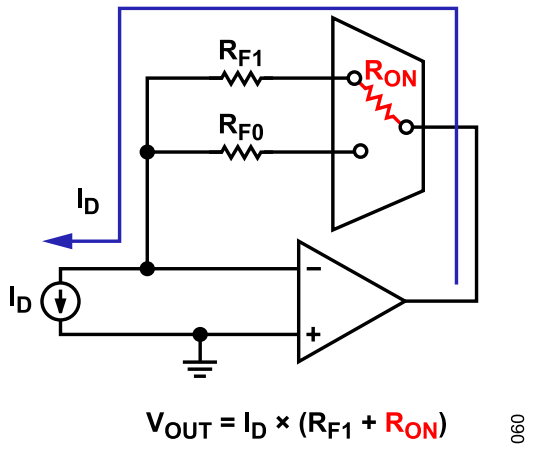


Figure 82. Switched Gain Transimpedance Amplifier with Error due to R_{ON}

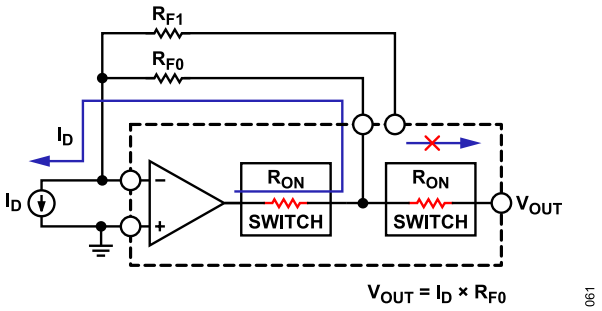


Figure 83. Switched Gain Transimpedance Amplifier with Kelvin Switching

With the switch traditionally in series with R_F, the R_{ON} of the switch can vary over temperature and over signal level, which can also result in gain error drift and nonlinearity.

The two trade-offs of Kelvin sensing are loss of headroom due to $I_D \times R_{ON}$ and an I_{OFF} contribution because there is an off switch in parallel feeding back through the inactive feedback resistor into the summing junction. The loss of headroom is minimized by the low R_{ON} of the switches in the ADA4351-2 (11 Ω at 5 V). Additionally, the total I_{OFF} of the parallel switches in the ADA4351-2 still has a much lower I_{OFF} than typical discrete CMOS switches.

Linear Output Voltage Range Considerations

Most photodiode amplifier applications are single supply. While the ADA4351-2 input pins can swing to the negative supply, the output stage starts to lose linearity within 0.1 V of either supply rail. For feedback resistors R_F more than 10 kΩ, and for best linearity, design for a maximum output swing of 0.1 V less than the positive supply (AVDD). For smaller TIA gains down to 200 Ω, additional positive output headroom is required to accommodate for an additional IR drop through the channel select switches inside the amplifier loop. A conservative estimate of the maximum available linear output voltage swing including this effect is given by the following equation:

$$V_{O,MAX} = \frac{AVDD - V_{HR}}{1 + \frac{R_{ON}}{R_F}} \quad (1)$$

where:
V_{HR} is the no load headroom.
R_{ON} is the resistance of the switch inside the loop.

For example, assume V_{HR} = 0.1 V, and R_{ON} = 33 Ω at 3 V and 19 Ω at 5 V over temperature (−40°C to +125°C). The resulting output headroom vs. R_F curves for 3 V and 5 V are shown in Figure 84). Carefully consider these effects to maintain the best signal path linearity with the lowest DC errors.

The previous example assumed no load, and thus, no IR drop across the switch on the right side in Figure 83. If there is a load, there is also an IR drop through the right side switch outside the loop in series with the output.

THEORY OF OPERATION

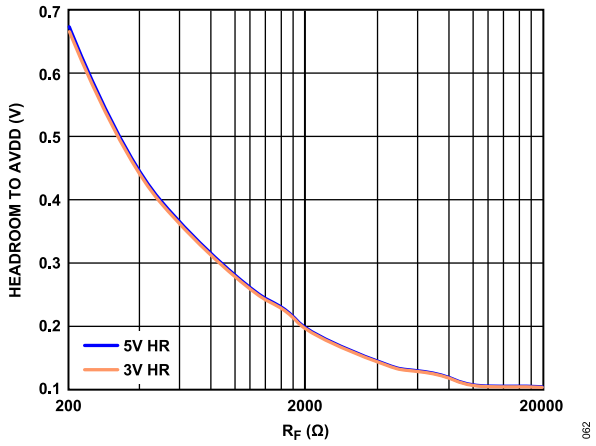


Figure 84. Output Headroom (HR) to AVDD vs. R_F

MAIN AMPLIFIER (CMOS)

Rail-to-Rail Output Stage

For a TIA in a single-supply configuration with a unidirectional input signal (see Figure 85), the minimum detectable signal is directly impacted by the input and output swing limits of the amplifier. For this circuit to maintain best linearity, the reference voltage, V_{REF}, (noninverting input) must be biased at 0.1 V or higher to satisfy the 0.1 V output headroom above the negative supply.

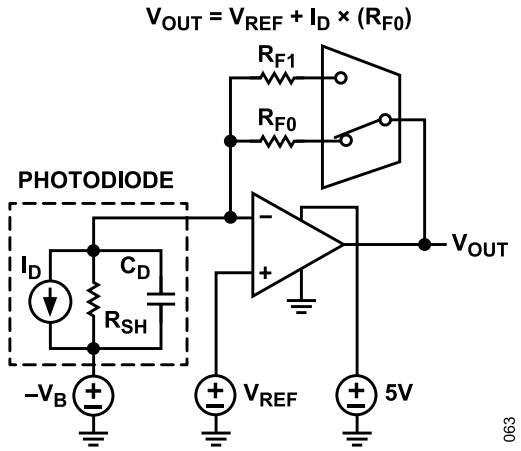


Figure 85. ADA4351-2 Single-Supply Operation

For the output to be able to swing to GND, the analog part of the amplifier must be operated on a negative supply that is less than GND, usually −0.2 V to −0.5 V. Because the ADA4351-2 has separate digital supplies, DVDD and DVSS, the logic threshold levels are independent of the analog supplies, so the analog portion can run on split supplies or a negative supply slightly less than GND. The ADA4351-2 was designed with a rail-to-rail output stage and can operate to within 100 mV from the power supplies with A_{OL} > 110 dB, which provides flexibility for the system and eases design constraints.

Bottom Rail Input Stage

The V_{REF} shown in Figure 85 is constrained by the input common-mode range of the main amplifier. In a single-supply configuration, V_{REF} sets the minimum output voltage value; therefore, the dynamic range is constrained between V_{REF} and the maximum ADC input voltage. The ADA4351-2 was designed with a PMOS input differential pair to allow the analog inputs to swing to AVSS, where AVSS can be set to as much as 0.5 V less than DVSS. It is less common in TIA designs for the input common-mode voltage across the inputs to approach the positive supply. The ADA4351-2 input stage requires 1.5 V headroom to the positive supply. Alternative approaches to supporting a rail-to-rail input are to either add a second input pair or an on-board charge pump to bias the input stage more than the supply. However, the first approach creates a large offset voltage in the crossover region, while the second approach adds quiescent power and switching noise to the design.

Low Noise Operation

In a transimpedance amplifier, having low op-amp input voltage noise is particularly crucial. At low frequency, the noise gain is near 1 V/V. However, at higher frequencies, the noise gain increases from zero due to C_S (see the TIA Design Theory section). Additionally, more noise is integrated (per decade) at higher frequencies, which contributes to the total output integrated noise. While there is usually a design trade-off between noise and power consumption, the ADA4351-2 contributes 7.3 nV/√Hz of wideband noise while requiring only 3.3 mA per channel.

THEORY OF OPERATION

Current Noise

When using large transimpedance gains, the current noise of the main amplifier can be a major source of noise in a system. The current noise flows through the feedback resistor and appears at the output as a voltage (current noise × R_F). Similar to the leakage and bias current errors in the TIA, the current noise becomes more dominant at higher TIA gains. Also, if the photodiode is reverse biased, users must include its dark current noise contribution, which can, in some cases, become the dominant current noise term.

In CMOS amplifiers, the input bias current noise increases over frequency and, therefore, can have a major impact on the total integrated noise. The ADA4351-2 was designed to have low current noise, but it increases with frequency. A 110 fA/√Hz flat current noise spectral density from 10 kHz to 100 kHz is used in the Photodiode Circuit Design Wizard to represent the worst case, high frequency noise.

Using a TIA gain of 1 MΩ, the Johnson noise of the resistor itself at the output is 127 nV/√Hz (at room temperature), while the 110 fA/√Hz current noise spectral density of the amplifier times the TIA gain at 10 kHz is a comparable 110 nV/√Hz . Both of these noise sources are usually dominated by the voltage noise contribution in most applications (see the Noise Contributions for Transimpedance Amplifiers section).

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TIA DESIGN THEORY

With its low input bias current and 8.5 MHz gain bandwidth product, the ADA4351-2 offers an effective solution for programmable gain photodiode amplifier applications. Figure 86 shows a typical design setup using one of the two possible feedback channels available. The example in Figure 86 shows the external RC values for the 15 kΩ, 100 pF photodiode capacitance (C_D), 16 pF external feedback, $C_{F,EXT}$, example shown in Figure 96.

Example Transimpedance Design with Overcompensated Response

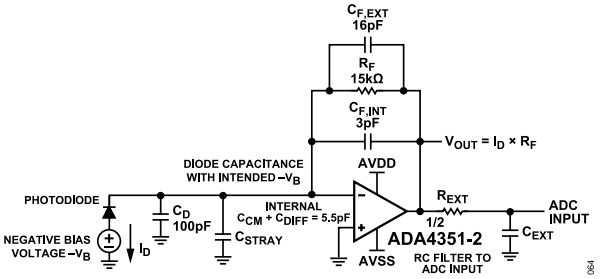


Figure 86. Example Transimpedance Design Giving the Overcompensated Frequency Response Shown in Figure 96

For transimpedance design, a photodiode capacitance and any layout parasitic and internal parasitic capacitance for the amplifier must be taken into consideration. The shunt resistance (R_{SH}) of the photodiode is normally some orders of magnitude greater than R_F (R_{SH} >> R_F) and is usually neglected for the design. Determine the C_D at the reverse bias voltage ($-V_B$) using the curve in the user-selected diode data sheet. The total source capacitance (C_S) at the inverting input is as follows:

$$C_S = C_D + C_{CM} + C_{DIFF} + C_{STRAY}$$

where:
C_{CM} is the internal, common-mode capacitance.
C_{DIFF} is the internal, differential capacitance (with C_{CM} + C_{DIFF} = 5.5 pF).
C_{STRAY} is the stray capacitance due to the PCB.

Calculate the total C_F as follows:

$$C_F = C_{F,EXT} + C_{F,INT}$$

where:
$C_{F,EXT}$ is the external feedback capacitance.
$C_{F,INT}$ is the internal, 3 pF feedback capacitance of the ADA4351-2.

The DC gain is set by the R_F value. The overall frequency response is determined by multiple frequency elements whose effects lay over each other. To approximate the characteristic frequency (f_0), calculate the geometric mean of the noise gain zero formed by R_F and C_S, given by Z1 in Figure 87, and the GPB of the amplifier. While some designs can force the closed-loop response to single pole (making the feedback pole, P1, much lower than the characteristic frequency), most designs either try to drive the gain up as high as possible for a target bandwidth or try to drive the bandwidth up as high as possible for a target R_F. Figure 87 shows these key frequencies in a loop gain Bode plot of the single-pole, open-loop response of the op amp and the inverse of the feedback divider (1/β) superimposed on that. This 1/β is the noise gain frequency response and also is the gain over frequency for the 7.3 nV/√Hz input voltage noise.

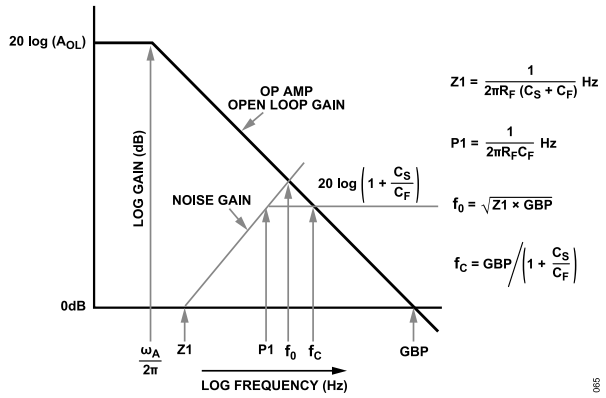


Figure 87. Loop Gain Plot for Any Transimpedance Amplifier Design

Because C_S is often much larger than C_F, it is a good approximation to drop C_F out of the equation for Z1 (see Figure 87). In that circumstance, the equations for P1 and f_0 are now independent of each other; therefore, P1 can be adjusted without affecting f_0 significantly. Normally, P1 is less than f_0 and produces a closed-loop second-order response with either two real poles (Q ≤ 0.5) or complex poles (Q > 0.5) giving a classic second-order response. The example overcompensated design of Figure 86 shows these loop gain magnitude elements in Figure 88. The A_{OL} is the open-loop, single-pole gain response, and the noise gain starts at 0 dB at DC and then rises at ≈101 kHz (noise gain zero, Z1) and flattens back out at P1 = 573 kHz with the higher noise gain set by 1 + C_S/C_F = 1 + 105.4 pF/19 pF = 6.5 V/V (or 16.3 dB), crossing over the A_{OL} curve with excellent phase margin as seen in Figure 89. The approximate $f_0 = \sqrt{8.5\ \text{MHz} \times 101\ \text{kHz}} = 926\ \text{kHz}$, where the resulting closed-loop transimpedance response (see Figure 88) shows the rolled off response for the Q ≈ 0.62 in this test circuit giving $f_{-3\ dB}$ ≈ 745 kHz. A good approximation when C_S > 5 × C_F is that Q ≈ ($P1/f_0$), where it solves to 573 kHz/926 kHz = 0.62 = Q.

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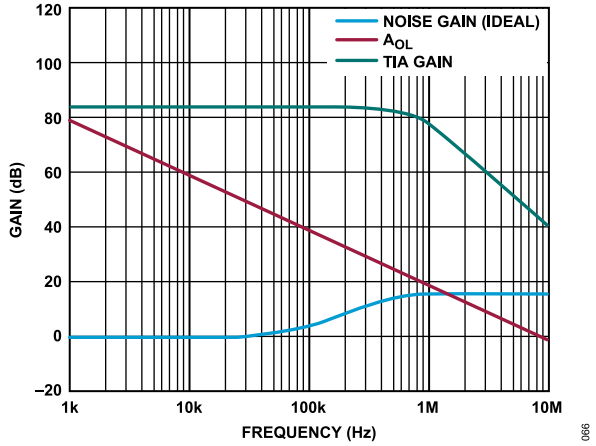


Figure 88. Loop Gain Elements and Closed-Loop Transimpedance Frequency Response for the Overcompensated Response in Figure 86

The noise gain here intersects the ADA4351-2 A_{OL} curve at about 1.1 MHz, where the loop gain is at the 0 dB crossover with the loop-gain phase curve showing a stable 71° phase margin in Figure 89. Higher frequency poles in the ADA4351-2 open-loop response reduce this phase margin slightly but still yield a stable design.

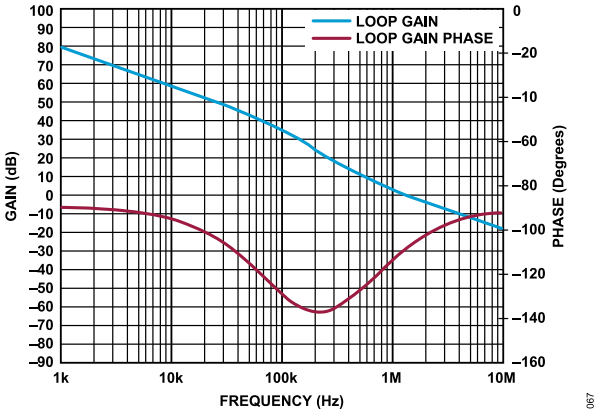


Figure 89. Loop Gain Magnitude and Phase for the Design of Figure 88

Generally, a good starting point for a design is to set the feedback pole as shown in Equation 2, which is in Hertz. Setting the feedback pole, P1, at 0.707 × f_0 yields an approximate Butterworth response, giving a maximally flat closed-loop response with only 4% step response overshoot.

$$P1 = \frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_S}} = \frac{f_0}{\sqrt{2}} \quad (2)$$

If P1 is set as shown in Equation 2, the closed-loop transimpedance response has a $f_{-3dB} \approx f_0$.

Example Transimpedance Design for Higher Gain, Lower Bandwidth

Re-executing the design shown in Figure 86 for a higher gain, and setting P1 to approximate a Butterworth closed-loop design, results in the design shown in Figure 90.

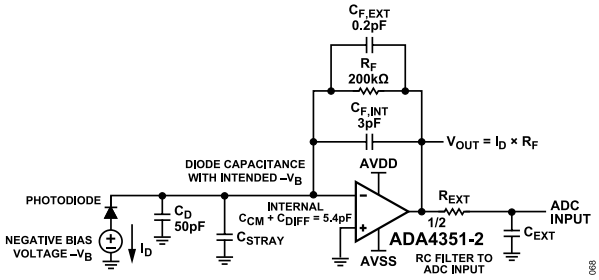


Figure 90. Higher Gain, Lower Bandwidth Butterworth Design Example with C_D = 50 pF

This simplified design equation is effective when $C_S > 5 \times C_F$, as it is here. Under those conditions, the approximate zero, Z1, is 1/(2π × 200 kΩ × 55.4 pF) = 14.4 kHz (note that this is neglecting C_F in the Z1 equation shown in Figure 87).

The characteristic frequency is approximately the following:

$$f_0 = \sqrt{GBP \times Z1} = \sqrt{8.5\ \text{MHz} \times 14.4\ \text{kHz}} = 348\ \text{kHz} \quad (3)$$

The feedback pole is placed at 0.707 × f_0 = 246 kHz, and the resulting $f_{-3\ dB}$ must be near 350 kHz = f_0. Rerunning the loop gain and response shape curves for the updated design of Figure 90 gives a close fit as shown in Figure 91 with an $f_{-3\ dB}$ = 340 kHz showing a flat Butterworth response. The required feedback capacitor in this example is largely the internal 3 pF ($C_{F,\ INT}$), where that 0.2 pF externally across the 200 kΩ feedback shown in Figure 90 is approximately the parasitic capacitance for a surface-mount resistor.

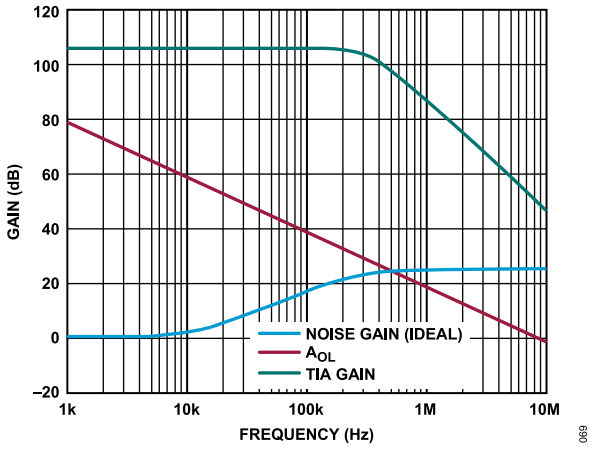


Figure 91. Redesigned TIA Design for a R_F = 200 kΩ Butterworth Response with C_D = 50 pF

Sticking with the Butterworth solution, a simple expression for the maximum achievable gain given a target $f_{-3\ dB}$ bandwidth and a C_S can be derived as follows:

$$R_{F,MAX} = \frac{GBP}{(f_{-3\ dB})^2 2\pi C_S} \quad (4)$$

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Conversely, Equation 3 can be solved for the maximum $f_{-3\ dB}$ for a target R_F to achieve a Butterworth response. Or, Equation 3 can be used to solve for the minimum required GBP for the desired R_F and $f_{-3\ dB}$.

In general, to place P1 (the feedback pole) to get any Q for the second-order closed-loop response, simply set P1 = Q × f_0, which is more applicable in designs where $C_S > 5 \times C_F$. With a f_0 largely determined by C_S and the GBP of the amplifier, the resulting $f_{-3\ dB}$ for any Q is given by the following equation. Evaluating the following equation at Q = 0.707 gives a ratio of 1. Evaluating the following equation at Q = 0.62 and R_F = 15 kΩ, C_D = 100 pF, and C_F = 16 pF for the first example design gives 0.85, where then $f_{-3\ dB}$ = 0.85 × 926 kHz = 782 kHz ≈ 745 kHz (actual, see Figure 88).

$$\frac{f_{-3\ dB}}{f_0} = \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \quad (5)$$

These are approximate guidelines and making slight adjustments in the C_F value can tune a design into the desired frequency response shape and/or pulse response.

NOISE CONTRIBUTIONS FOR TRANSIMPEDANCE AMPLIFIERS

There are three main sources of noise in photodiode TIA applications that set the current noise floor (referred to the output). The three noise sources include the following:

1. The Johnson noise of the feedback resistor
2. The current noise due to the input bias or leakage currents of the amplifier
3. The effect of the input voltage noise on the output of the op amp

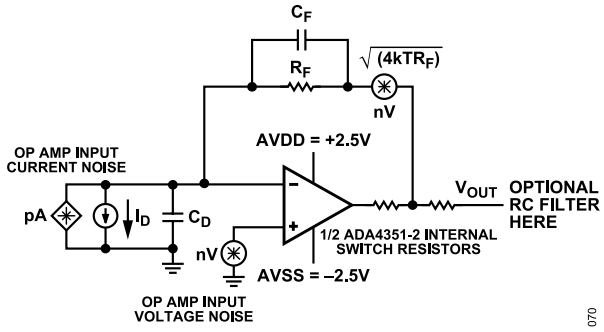


Figure 92. Noise Sources in the ADA4351-2

Each of these noise sources is referred to the output at the SW0 or SW1 pins. The spectral densities of these noise sources are integrated over their respective noise bandwidths and then root mean squared to provide the total output integrated noise.

- The feedback resistor produces a temperature dependent Johnson noise given by $\sqrt{4kTR_F}$, which results in a gain to the output of 1 V/V and is band limited by the feedback pole, P1. Estimating a single-pole roll-off for this noise source gives a noise power bandwidth (NPBW) of 1.57 × P1. A good starting point for 4kT = 1.65 × 10^{-20} at 25°C.
- The input current noise for the op amp itself has a shot noise current term set by the DC input bias or leakage current, which can be low. The current noise of the CMOS input devices rises over frequency, and an estimate for the maximum current noise over frequency is a flat 110 fA/√Hz density in the 10 kHz to 100 kHz region. This estimate for the input bias current noise term is referred to the output by a factor of R_F and has the same 1.57 × P1 noise power bandwidth as the resistor noise.
- The noise gain of the input voltage noise of 7.3 nV/√Hz is the same as the noise gain in the TIA loop gain plot (see Figure 87). Hence, this noise starts out at a gain of 1 until Z1 (see Figure 87) and then rises with a one-zero response to the feedback P1 pole. The noise gain then flattens out at 1 + C_S/C_F until the roll-off of the GBP, which is normally the dominant integrated noise term, and adding a post-output filter (R_{EXT} and C_{EXT}) can band-limit its contribution to the total output integrated noise.

Continuing with the overcompensated design example shown in Figure 86, each output noise term can be estimated as follows. Here, the feedback pole frequency, P1, is 1/(2π × 15 kΩ × 19 pF) = 558 kHz, where its noise power bandwidth to use for some of the terms is (π/2) × 558 kHz = 1.57 × 558 kHz = 877 kHz.

1. The 15 kΩ resistor noise has a gain of 1 to the SW0 or SW1 pins. Its 15.7 nV/√Hz term adds a 15.7 nV/√Hz × √877 kHz = 14.7 µV RMS output noise term.
2. An approximate 110 fA/√Hz input current noise is gained up by 15 kΩ R_F and then has the same noise power bandwidth as the resistor noise, which is a 15 kΩ × 110 fA/√Hz × √877 kHz = 1.5 µV RMS.
3. The input voltage noise adds three terms to the output RMS noise total. The noise has a gain of 1 through the Z1 frequency (= 1/(2π × 15 kΩ × 105.5 pF) = 101 kHz), then a rising region following the noise gain peaking region (see Figure 87), then a flat higher gain region from P1 to whatever higher frequency pole is in the system. Here, a self-limited intersection with the GBP is used.
   a. The gain of 1 region adds a 7.3 nV/√Hz × √Z1 = 7.3 nV/√Hz × √(101 kHz) = 2.3 µV RMS.
   b. The rising region can be approximated by running an integral from Z1 to P1 and extracting a single-output voltage noise value that integrates to the same power as the actual response shape. This solution is given by e_n ($2\pi R_F C_S P1$)/(√3) = e_n(P1/(Z1 × √3)), where P1 and Z1 are in Hz. Evaluating this equation for the circuit shown in Figure 86 and the overcompensated response of Figure 96 gives an equivalent flat spot noise voltage at the output of 23.5 nV/√Hz. Integrating that from Z1 to P1 gives an approximate output integrated noise contribution of 23.5 nV/√Hz × $\sqrt{558\ kHz - 101\ kHz}$ = 15.9 µV RMS.
   c. Then, from P1 to the final single-pole roll-off (f_C) shown in Figure 87 at GBP/(1 + C_S/C_F) there is a flat spot noise integrating over a wide span. Here, the high frequency noise gain (N_{GHI}) is 1 + 105.5 pF/19 pF = 6.55 to

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give a single-pole roll-off at GBP/ N_{GHI} = 8.5 MHz/6.55 = 1.3 MHz. Because the noise up to P1 has already been integrated, the integration span for this 6.55 × 7.3 nV/√Hz = 47.8 nV/√Hz output spot noise due to this term is $\sqrt{(1.57 \times 1.3\ \text{MHz} - 558\ \text{kHz})}$, which gives a 47.8 nV/√Hz × √1.48 MHz = 58.2 µV RMS term, which is by far the most dominant term. Where possible, a post RC filter at lower than the self-limited frequency can be used to reduce this total integrated noise and reduce the spot noise voltage shown in Figure 50.

Table 9 summarizes each of the separate integrated noise contributions and the total RMS of these to a combined integrated output noise. The total output is formed by squaring each term, summing those, and then taking the square root again. The percent of output noise power contribution is the ratio of each term squared to the total RMS noise voltage squared.

Clearly, the dominant term is the output spot noise that is integrated from P1 to the 1.3 MHz $f_{-3\ dB}$. Note that reducing the integration span using a lower frequency external RC filter, where possible, can reduce the total integrated noise rapidly. This approximate calculation of 62 µV RMS closely matches the example set up in the Photodiode Circuit Design Wizard, where it reports a 69 µV RMS total noise.

When the photodiode is reverse biased, there is a DC dark current, I_{DARK}, in the diode that adds a noise term given by $\sqrt{2q \times I_{DARK}}$. If present, RMS this term with the input bias current noise term before computing its RMS contribution to the output. Note that, sometimes, these is also a relatively low shunt resistance across the photodiode. To the extent that it is not >> R_F, it may add a small added noise term. If present, get its Johnson noise term and give it a gain to the output equal to R_F/R_{SH} and apply the same noise power bandwidth as used for the R_F noise.

These calculations give an output RMS noise floor before any signal current is considered. To combine its effects with a noise source from an input signal, refer this output integrated noise back to the input as an equivalent spot noise, which can be done by dividing by the R_F gain element, which gives the input referred integrated noise. Then, divide the input referred RMS noise current by the square root of the input current noise power bandwidth. Making the calculation for the 62 µV RMS derived previously gives, first, an input referred 4.1 nA RMS integrated input noise, and then dividing by √877 kHz gives an equivalent total input referred spot current noise of 4.4 pA/√Hz. As the signal current increases from zero, it also adds its own current noise term to the output using the same NPBW as the bias current noise. To calculate the total input RMS noise with an input signal, take the RMS of the input signal noise and the equivalent total input referred spot current noise as previously described.

Table 9. Summary Pieces Combining to a Total RMS Noise Voltage at the Output

Separate Output Noise Terms Integrating into the V RMS Pieces	Noise Term	Spectral Density	Integrated Noise Term (µV RMS)	Percent of Output Noise Power
Input Current Noise of the Op Amp	I_N	110 fA/√Hz	1.5	0.06%
RF Noise with G =1 to the Output and 1.57 × P1 Integrated Bandwidth	R_F term	25.8 nV/√Hz	14.7	5.59%
e_n with G =1 to the Output through Z1	e_n G =1 term	7.3 nV/√Hz	2.3	0.14%
Rising Integrated Equivalent Spot Noise from Z1 to P1	e_n Z1 to P1 integrated	7.3 nV/√Hz	15.9	6.54%
Flat from P1 to Final Single-Pole Roll-Off Frequency ($f_{-3\ dB}$)	$e_n \times N_{GHI}$ P1 to $f_{-3\ dB}$	24.8 nV/√Hz	58.2	87.67%
RMS Total Output Noise	Not applicable	Not applicable	62.16	Not applicable

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ERROR BUDGET

The output offset error contributed by the ADA4351-2 in a transimpedance application consists of three major sources: I_{OFF}, I_B, and V_{OS}. In addition, there are error contributions from CMRR and PSRR, although these errors can be reduced by using accurate supplies and calibration. The gain error of the transimpedance amplifier is the tolerance of the feedback resistance.

For a 5 V nominal supply voltage, calculate the full output error by using the following equation:

$$\text{Output Error (V)} = V_{OS} + (I_{OFF} + I_{B-})(R_F) + (I_{B+})(R_{IN+}) + 10^{\frac{-CMRR}{20}}\left|\frac{V_S}{2} - V_{CM}\right| + 10^{\frac{-PSRR}{20}}\left(5 - V_S\left(1 - \frac{\Delta V_S}{100}\right)\right) + (I_D)(\Delta R_F) \quad (6)$$

where:
I_{B-} is the input bias current at the inverting input.
I_{B+} is the input bias current at the noninverting input.
R_{IN+} is the source resistance at the noninverting input.
CMRR and PSRR are in dB.
ΔV_S is the highest the supply can be in the application minus the lowest the supply can be in the application.
ΔR_F is the percent tolerance × 100 of R_F.

If the noninverting resistance is kept at a minimum, the $I_{B-} \times R_{IN+}$ is insignificant. The CMRR term is reduced by operating at V_{CM} equal to midsupply; however, this may not be suitable for many applications. An initial calibration can alleviate the error related to CMRR. The error contributed by PSRR can be reduced by using accurate supplies or by an initial calibration. The gain error can be reduced by using more accurate feedback resistors.

It is also useful to look at the input-referred error at different values of feedback resistance to define a given TIA application. Figure 93 shows the input-referred percent error for transimpedance values of 5 kΩ and 500 kΩ.

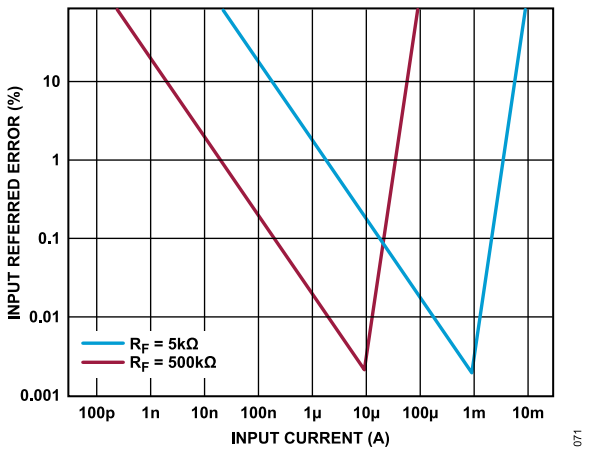


Figure 93. DC Input Referred Error vs. Input Current (I_D)

At a low I_D and a low R_F, the offset voltage dominates the input error. At a low I_D and a high R_F, the bias and leakage currents dominate the input error. The input error reduces with an increased current level until the amplifier clips and error shoots up.

ADC DRIVING

The ADA4351-2 can be used for directly driving a successive approximation register (SAR) ADC. The slew rate and THD of the ADA4351-2 contribute to the low distortion even at larger output levels. The ADA4351-2 also draws low supply current and can thus be paired with low power, high resolution ADCs.

Selecting the External RC Filter Components

Figure 94 shows a typical single-supply application using the AD4696, a high accuracy, low power, 16-channel, 16-bit SAR ADC. The ADA4351-2 is configured as an ADC driver that can switch between gains. At the output of the ADA4351-2, which is also at the analog front end of the ADC, is an external low-pass filter formed by R_{EXT} and C_{EXT}. Note that these components reduce the wideband noise and nonlinear voltage kickback in the analog inputs of the ADCs.

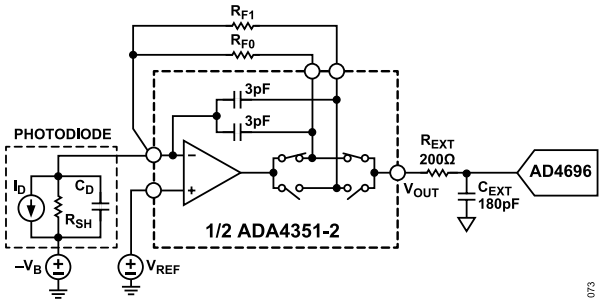


Figure 94. Typical Single-Supply Application Using the AD4696

The selection for the RC filter is an iterative process, and the best combination depends on the intended application. For example, in lower frequency applications, the designer can opt to reduce the corner frequency by choosing a higher value RC to introduce less noise, but the designer must also make sure that this RC combination allows the signal to settle faster than the selected acquisition phase duration of the ADC.

For detailed information on selecting an RC filter configuration, see the Analog Devices, Inc., Analog Dialogue article, *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter*. In addition, refer to the ADC data sheet when selecting these components as well.

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COMPENSATED AND NONCOMPENSATED FREQUENCY RESPONSE

For any given source capacitance and desired TIA gain (R_F), the small signal frequency response may or may not be acceptable to the application. Some response shape tuning is possible by adding a compensation capacitor in parallel with R_F. Figure 95 through Figure 97, over a wide range of gains, show some typical response shape trade-offs.

The lowest feedback (R_F = 200 Ω) has the highest bandwidth because the noise gain zero is relatively higher in frequency than the higher gains with the same source capacitance. As previously mentioned, at the lowest R_F value, the output swing range is reduced by the IR drop through the inside of the loop switch impedance (approximately 0.7 V, see Figure 84). In each of the conditions reported in Figure 95 through Figure 97, $C_{IN} = C_D + C_{STRAY}$ (refer to the TIA Design Theory section for definitions of the terms). To get the total C_S, add the internal input capacitances ($C_{CM} + C_{DIFF}$) of 5.5 pF to C_{IN}. Similarly, to get the total C_F, add the internal 3 pF to the $C_{F,EXT}$ shown in Figure 95 through Figure 97. For both of the 10 pF source C_{IN} curves shown in Figure 95, the noise gain zero and pole frequencies are beyond the 8.5 MHz GBP; therefore, typical TIA analysis does not apply. The circuit with C_{IN} = 10 pF whose frequency response is shown in Figure 95 is essentially operating as a unity-gain stage with a flat frequency response with a 10 MHz $f_{-3\ dB}$.

The 100 pF C_{IN} puts the noise gain zero just less than the GBP. With no external $C_{F,EXT}$, this zero gives a relatively low phase margin and about 1.1 dB peaking because the noise gain pole is much higher in frequency. Adding a 150 pF C_{FEXT} moves the noise gain zero down to 3 MHz with a noise gain pole at 5.2 MHz (see Figure 95) giving a nicely overcompensated design with Q ≈ 0.62 and an $f_{-3\ dB}$ near 4.5 MHz.

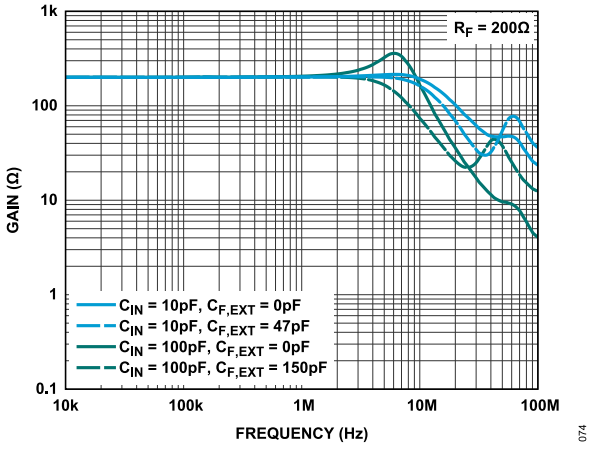


Figure 95. Small Signal Responses for R_F = 200 Ω with a Range of Input C_{IN} ($C_D + C_{STRAY}$) and External Feedback ($C_{F,EXT}$) Capacitors

Going to a midrange feedback gain of 15 kΩ gives the family of curves shown in Figure 96.

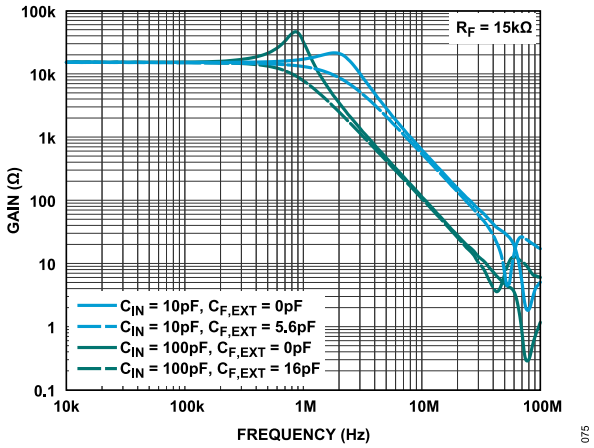


Figure 96. Small Signal Responses for R_F = 15 kΩ with a Range of Input C_{IN} ($C_D + C_{STRAY}$) and External Feedback ($C_{F,EXT}$) Capacitors

The initial 10 pF source with only an internal 3 pF feedback capacitor forms a noise gain zero below f_0 (see the solid blue line in Figure 96) but a feedback pole more than f_0 giving the typical peaked response shown by the solid blue curve shown in Figure 96. The peaking noise gain is crossing over the A_{OL} curve with slightly less than a 40 dB closure rate giving the approximate Q = 1.1 and the 20log(21 kΩ/15 kΩ) = 2.9 dB peaking. Adding the external 5.6 pF retunes the response shape to a controlled Q = 0.56 and $f_{-3\ dB}$ ≈ 1.4 MHz, as shown by the dotted blue line shown in Figure 96.

Testing an 100 pF external C_{IN}, with only the internal 3 pF $C_{F,INT}$, again undercompensates the design (Q ≈ 2.7 with ≈9 dB peaking). For this R_F value, $C_{F,EXT}$ is required and the 16 pF shown in Figure 96 compensates this design back to Q = 0.62 with a $f_{-3\ dB}$ = ≈730 kHz. Figure 96 is used to illustrate a typical TIA design flow and an integrated noise analysis in those applications sections.

Using a large external R_F (1 MΩ) results in the overcompensated response shown in Figure 97 due to the internal 3 pF capacitor.

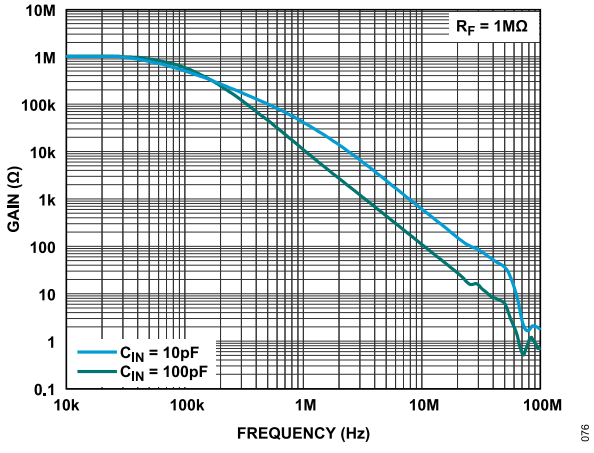


Figure 97. Small Signal Responses for R_F = 1 MΩ with a Range of Input C_{IN} ($C_D + C_{STRAY}$) Capacitors

APPLICATIONS INFORMATION

The feedback pole (1/(2π × 1 MΩ × 3 pF) = 53 kHz) shown in Figure 97 is well under f_0, giving an approximate single-order pole at that feedback pole frequency. Adding an additional external $C_{F,EXT}$ can tune this roll-off to lower frequencies; however, it is not possible to extend the frequency span starting out with an internal 3 pF $C_{F,INT}$. Increasing the C_{IN} to 100 pF decreases f_0 moving the feedback pole closer to that but still giving an approximate first-order response at the feedback pole frequency (53 kHz). Increasing the C_{IN} to more than 200 pF with a 1 MΩ feedback and an internal 3 pF $C_{F,INT}$ starts to show a second-order closed-loop response extending the $f_{-3\ dB}$ more than the simple feedback pole.

ACHIEVING LOW INPUT BIAS CURRENT

There are several factors to consider in a low input bias current circuit. Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of picoamp signals. At the picoamp level, leakage current can come from unexpected sources, including adjacent traces on the PCB (whether on the same layer or even from internal layers), contamination on the PCB (from the assembly process or the environment), or other components on the signal path. Take care in the design of the system can mitigate these sources and preserve optimal performance.

An appropriate cleaning process after assembly is essential to avoid leakages from solder flux and other contaminants. Relative humidity also must be considered because PCB materials and the plastic mold compound of the package itself can absorb moisture and cause additional leakage paths.

APPLICATIONS INFORMATION

PCB LAYOUT

In high source impedance applications, the low input bias current of the ADA4351-2 requires a clean PCB layout to minimize additional leakage current into a high impedance signal node. A layout recommendation for any PCB designed with this device is to strip the conductor around the signal carrying trace as shown in Figure 98. This stripping makes it more difficult for leakage currents from the PCB to couple into the signal path, causes output errors, and minimizes parasitic capacitance at the inputs.

It is important to keep the high impedance signal path as short as possible on the PCB. A node with high impedance is susceptible to picking up any stray signals in the system; therefore, keeping the path as short as possible reduces this effect. Additionally, the longer the signal trace into the PCB (on the inverting input) the more stray capacitance at the input of the device under test (DUT). A trace capacitance as low as 5 pF can greatly impact board performance, especially if the photodiode or current source used is around the same order of magnitude of capacitance .

Other signals must be routed well away from the signal path, and there must be no internal power planes under the high impedance node. The best defense from coupling signals is shielding; however, this increases capacitance in the area, which impacts the noise gain of the PCB. Another method to decouple signals is distance, which includes vertically (though layers of the PCB) as well as on the surface of the PCB. The package of the ADA4351-2 aids with this routing process because there is no exposed pad (EPAD) on the back side of the package, eliminating the need for vias and allowing routing on all layers of the PCB beneath the device. In cases where the space is limited, the designer can cut slots in the PCB around the high impedance input nodes to provide additional isolation and to reduce the chance of contamination on the surface of the PCB.

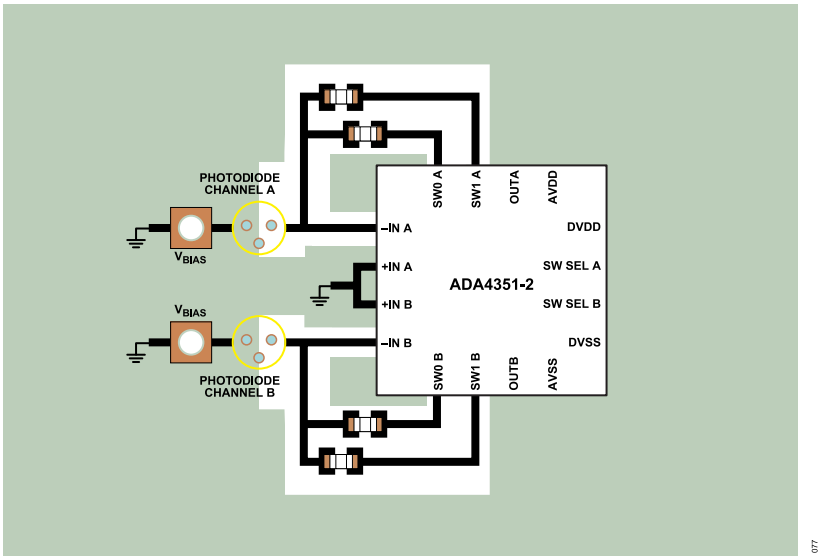
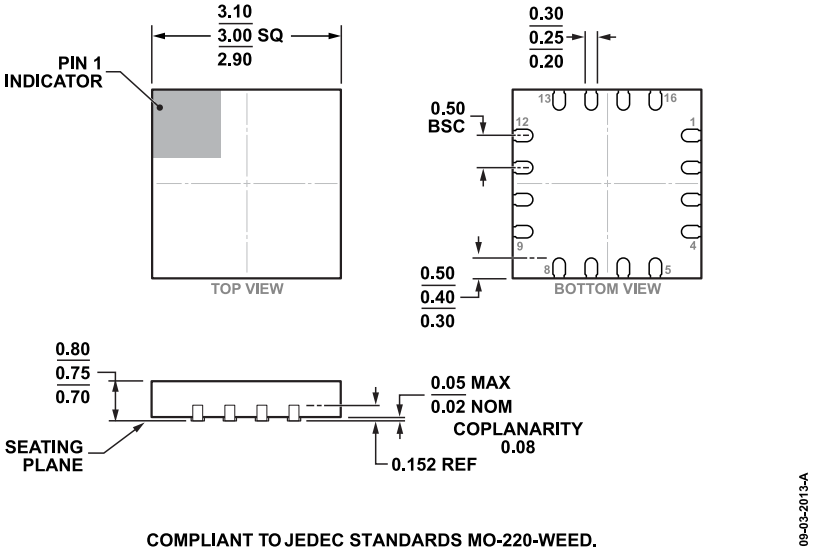


Figure 98. Example PCB Layout for Low Surface Leakage

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.

Figure 99. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm x 3 mm Body and 0.78 mm Package Height
(CP-16-32)
Dimensions shown in millimeters

Updated: July 01, 2026

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
ADA4351-2ACPZ	−40°C to +125°C	16-Lead LFCSP	Tray, 714	CP-16-32	A4P
ADA4351-2ACPZ-R7	−40°C to +125°C	16-Lead LFCSP	Reel, 1500	CP-16-32	A4P
ADA4351-2ACPZ-RL	−40°C to +125°C	16-Lead LFCSP	Reel, 5000	CP-16-32	A4P

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 10. Evaluation Boards

Model[1]	Description
EVAL-ADA4351-2EBZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

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