32-Channel, High Voltage, Matched Precision Resistor Divider

FEATURES

- 32-channel, matched precision resistor divider
- Channel division: 52 typical
- ±10 ppm typical resistor matching ratio long-term drift per channel
- 5.2 MΩ total series resistance per channel
- Up to a 225 V maximum input voltage
- 100-lead LQFP
- −10°C to +85°C T_A range

APPLICATIONS

- High-voltage monitoring

GENERAL DESCRIPTION

The AD45336 is a 32-channel, matched precision resistor divider. Each channel consists of two accurately matched resistors with a resistor matching ratio long-term drift of ±10 ppm typical and a total series resistance of 5.2 MΩ typical.

Each channel of the AD45336 can divide down input voltages up to 225 V.

The AD45336 is designed to operate as a monitoring companion to the AD45335 high voltage, digital-to-analog converter (DAC).

FUNCTIONAL BLOCK DIAGRAM

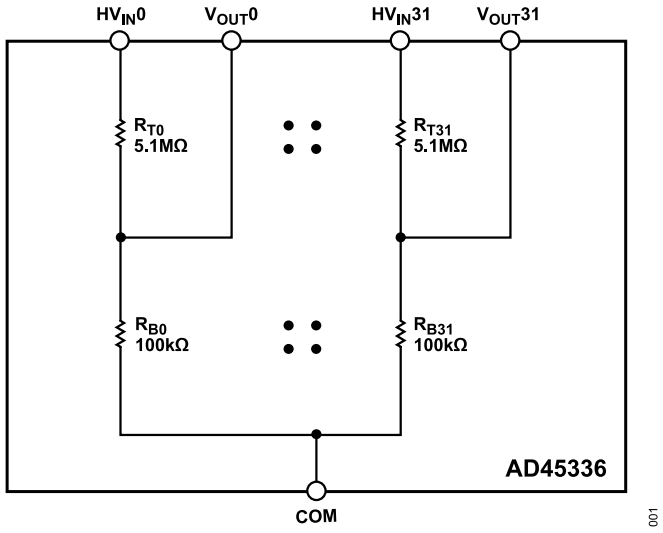

Figure 1. Functional Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

9/2025—Rev. B to Rev. C
Added Electrostatic Discharge (ESD) Ratings Section and Table 4; Renumbered Sequentially ... 4

8/2025—Rev. A to Rev. B
Changes to Figure 3 ... 8

4/2025—Rev. 0 to Rev. A
Changes to Figure 7 ... 10

12/2024—Revision 0: Initial Version

SPECIFICATIONS

$HV_{IN}x$ to COM = 175 V (where x is 0 to 31), and T_A = 25°C for all typical specifications, unless otherwise noted. All specification are design targets; final values are determined post device characterization.

Table 1. Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE					
Top x Resistor (R_{Tx})[1]		5.1		MΩ	
Bottom x Resistor (R_{Bx})[1]		100		kΩ	
CHANNEL DIVISION	51.986	52	52.014		
INPUT VOLTAGE[1]					
$HV_{IN}x$ to COM			225	V	
Across Any $HV_{IN}x$ to $HV_{IN}x$ Pins			225	V	
CONTINUOUS CURRENT[2]			55	µA	Per channel
RESISTOR-MATCHING RATIO DRIFT					
Long-Term[2]		±10	±100	ppm	Per channel, 70°C for 1000 hours
Temperature		−0.2		ppm/°C	Per channel
T_A	−10		+85	°C	

[1] Where x is 0 to 31.

[2] Guaranteed by design and characterization, not production tested.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
$HV_{IN}x$ to COM[1, 2]	240 V
Across any $HV_{IN}x$ to $HV_{IN}x$ Pins[1, 2]	240 V
$V_{OUT}x$ to COM[1, 2]	7 V
Temperature	
Operating Range	−10°C to +85°C
Junction Temperature	150°C
Storage Range	−65°C to +150°C
Lead Temperature, Soldering	260°C as per J-STD-020

1 Polarity inversion is possible.

2 Where x is 0 to 31.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, Ψ_{JT} is the characterization parameter that measures the temperature change between the junction temperature and the temperature of the top of the package, and Ψ_{JB} is the junction-to-board thermal characterization parameter. θ_{JC} is the junction-to-case thermal resistance, and θ_{JB} is the thermal resistance from the junction to board.

Simulated values based on the JEDEC JESD-51 series of specifications.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	Ψ_{JT}[1]	Ψ_{JB}[1]	θ_{JC}[2]	θ_{JB}[3]	Unit
ST-100-1	44.9	0.3	25.3	8.6	27.2	°C/W

1 θ_{JA}, Ψ_{JT}, and Ψ_{JB} are modeled using a JEDEC 2S2P test PCB in a JEDEC natural convection environment.

2 θ_{JC} is modeled using a JEDEC 1S test PCB, with an infinite heat sink attached directly to the package surface.

3 θ_{JB} is modeled using a JEDEC 2S2P test PCB in a JEDEC junction to board environment.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Table 4. AD45336, 100-Lead LQFP

ESD Model	Withstand Threshold (V)	Class
HBM	1500	1C
FICDM	1000	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

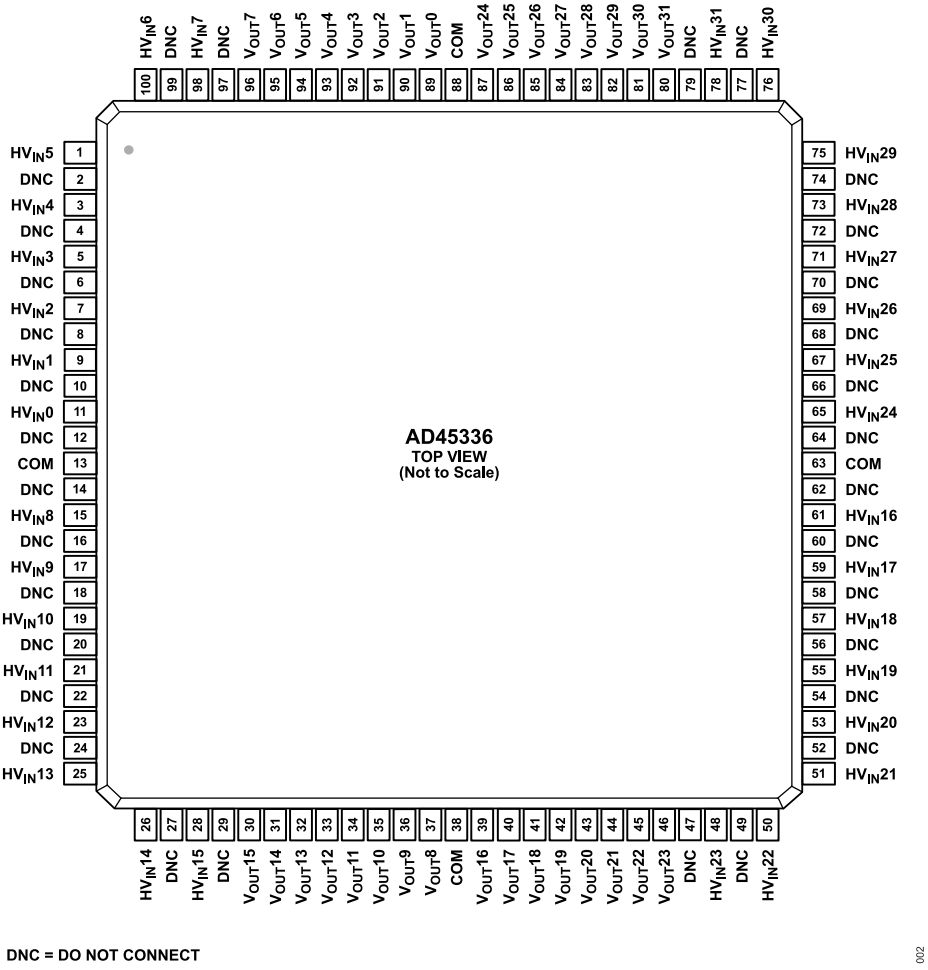

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$HV_{IN}5$	High-Voltage Analog Input Channel 5.
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 27, 29, 47, 49, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72, 74, 77, 79, 97, 99	DNC	Do Not Connect. Do not add any conductive material on these pins to prevent any potential damage or malfunction of the device.
3	$HV_{IN}4$	High-Voltage Analog Input Channel 4.
5	$HV_{IN}3$	High-Voltage Analog Input Channel 3.
7	$HV_{IN}2$	High-Voltage Analog Input Channel 2.
9	$HV_{IN}1$	High-Voltage Analog Input Channel 1.
11	$HV_{IN}0$	High-Voltage Analog Input Channel 0.
13	COM	Common GND or Reference Pin.
15	$HV_{IN}8$	High-Voltage Analog Input Channel 8.
17	$HV_{IN}9$	High-Voltage Analog Input Channel 9.
19	$HV_{IN}10$	High-Voltage Analog Input Channel 10.
21	$HV_{IN}11$	High-Voltage Analog Input Channel 11.
23	$HV_{IN}12$	High-Voltage Analog Input Channel 12.
25	$HV_{IN}13$	High-Voltage Analog Input Channel 13.
26	$HV_{IN}14$	High-Voltage Analog Input Channel 14.
28	$HV_{IN}15$	High-Voltage Analog Input Channel 15.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
30	$V_{OUT}15$	Analog Output Voltage from Channel 15.
31	$V_{OUT}14$	Analog Output Voltage from Channel 14.
32	$V_{OUT}13$	Analog Output Voltage from Channel 13.
33	$V_{OUT}12$	Analog Output Voltage from Channel 12.
34	$V_{OUT}11$	Analog Output Voltage from Channel 11.
35	$V_{OUT}10$	Analog Output Voltage from Channel 10.
36	$V_{OUT}9$	Analog Output Voltage from Channel 9.
37	$V_{OUT}8$	Analog Output Voltage from Channel 8.
38	COM	Common GND or Reference Pin.
39	$V_{OUT}16$	Analog Output Voltage from Channel 16.
40	$V_{OUT}17$	Analog Output Voltage from Channel 17.
41	$V_{OUT}18$	Analog Output Voltage from Channel 18.
42	$V_{OUT}19$	Analog Output Voltage from Channel 19.
43	$V_{OUT}20$	Analog Output Voltage from Channel 20.
44	$V_{OUT}21$	Analog Output Voltage from Channel 21.
45	$V_{OUT}22$	Analog Output Voltage from Channel 22.
46	$V_{OUT}23$	Analog Output Voltage from Channel 23.
48	$HV_{IN}23$	High-Voltage Analog Input Channel 23.
50	$HV_{IN}22$	High-Voltage Analog Input Channel 22.
51	$HV_{IN}21$	High-Voltage Analog Input Channel 21.
53	$HV_{IN}20$	High-Voltage Analog Input Channel 20.
55	$HV_{IN}19$	High-Voltage Analog Input Channel 19.
57	$HV_{IN}18$	High-Voltage Analog Input Channel 18.
59	$HV_{IN}17$	High-Voltage Analog Input Channel 17.
61	$HV_{IN}16$	High-Voltage Analog Input Channel 16.
63	COM	Common GND or Reference Pin.
65	$HV_{IN}24$	High-Voltage Analog Input Channel 24.
67	$HV_{IN}25$	High-Voltage Analog Input Channel 25.
69	$HV_{IN}26$	High-Voltage Analog Input Channel 26.
71	$HV_{IN}27$	High-Voltage Analog Input Channel 27.
73	$HV_{IN}28$	High-Voltage Analog Input Channel 28.
75	$HV_{IN}29$	High-Voltage Analog Input Channel 29.
76	$HV_{IN}30$	High-Voltage Analog Input Channel 30.
78	$HV_{IN}31$	High-Voltage Analog Input Channel 31.
80	$V_{OUT}31$	Analog Output Voltage from Channel 31.
81	$V_{OUT}30$	Analog Output Voltage from Channel 30.
82	$V_{OUT}29$	Analog Output Voltage from Channel 29.
83	$V_{OUT}28$	Analog Output Voltage from Channel 28.
84	$V_{OUT}27$	Analog Output Voltage from Channel 27.
85	$V_{OUT}26$	Analog Output Voltage from Channel 26.
86	$V_{OUT}25$	Analog Output Voltage from Channel 25.
87	$V_{OUT}24$	Analog Output Voltage from Channel 24.
88	COM	Common GND or Reference Pin.
89	$V_{OUT}0$	Analog Output Voltage from Channel 0.
90	$V_{OUT}1$	Analog Output Voltage from Channel 1.
91	$V_{OUT}2$	Analog Output Voltage from Channel 2.
92	$V_{OUT}3$	Analog Output Voltage from Channel 3.
93	$V_{OUT}4$	Analog Output Voltage from Channel 4.
94	$V_{OUT}5$	Analog Output Voltage from Channel 5.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
95	$V_{OUT}6$	Analog Output Voltage from Channel 6.
96	$V_{OUT}7$	Analog Output Voltage from Channel 7.
98	$HV_{IN}7$	High-Voltage Analog Input Channel 7.
100	$HV_{IN}6$	High-Voltage Analog Input Channel 6.

TYPICAL PERFORMANCE CHARACTERISTICS

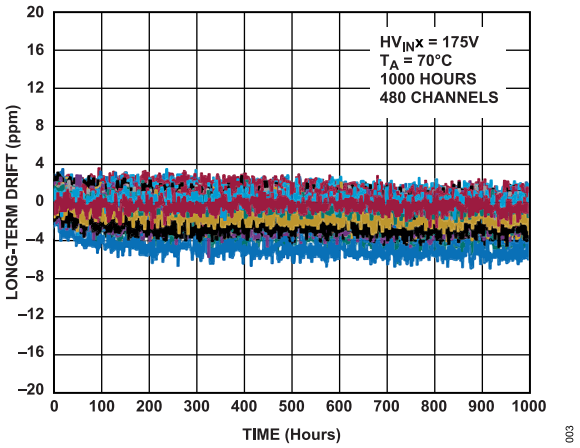

Figure 3. Resistor-Matching Ratio Long-Term Drift Over 1000 Hours at 70°C

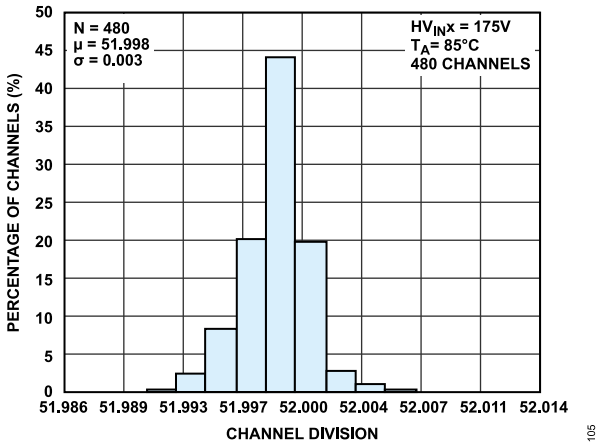

Figure 5. Channel Division Distribution at 85°C

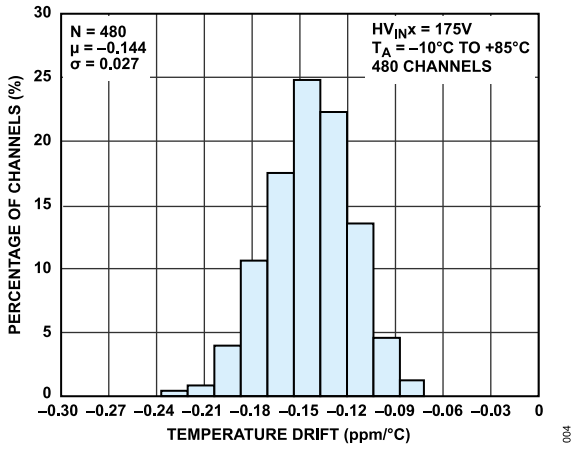

Figure 4. Resistor-Matching Ratio Temperature Drift Distribution

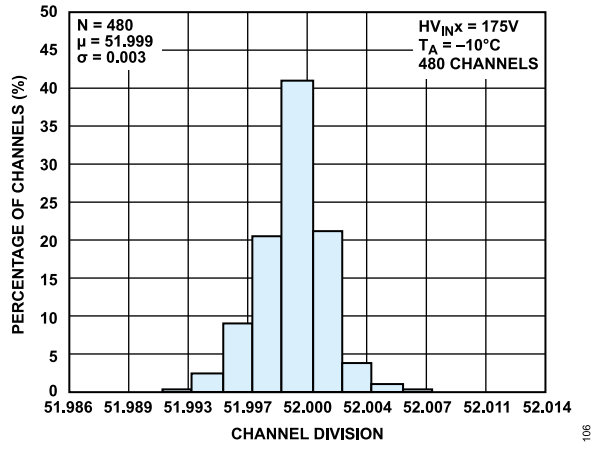

Figure 6. Channel Division Distribution at −10°C

THEORY OF OPERATION

The AD45336 is a 32-channel, matched precision resistor divider network designed for high-voltage monitoring applications. Each channel consists of two precisely matched resistors, with a long-term resistor matching ratio drift of ±10 ppm (typical) and a total series resistance of 5.2 MΩ (typical).

The device divides input voltages by 52 per channel, handling voltages up to 225 V. Each resistor network of the channel comprises a 5.1 MΩ R_{Tx} connected in series with a 100 kΩ R_{Bx}, where x is 0 to 31.

The AD45336 maintains high precision across a broad temperature range (−10°C to +85°C) with a resistor-matching ratio temperature drift of −0.2 ppm/°C. Each channel is capable of continuously handling currents up to 55 µA.

APPLICATION INFORMATION

HIGH-VOLTAGE MONITORING APPLICATION

The AD45336 is a 32-channel, matched precision resistor divider network, designed to divide high-voltage signals by a factor of 52. In a typical application, the AD45336 operates in companion with the AD45335 32-channel high-voltage DAC. The AD45336 divides the high-voltage output of the AD45335 (0 V to 200 V) by a factor of 52, reducing this output to a 0 V to 3.85 V range. Figure 7 illustrates this configuration.

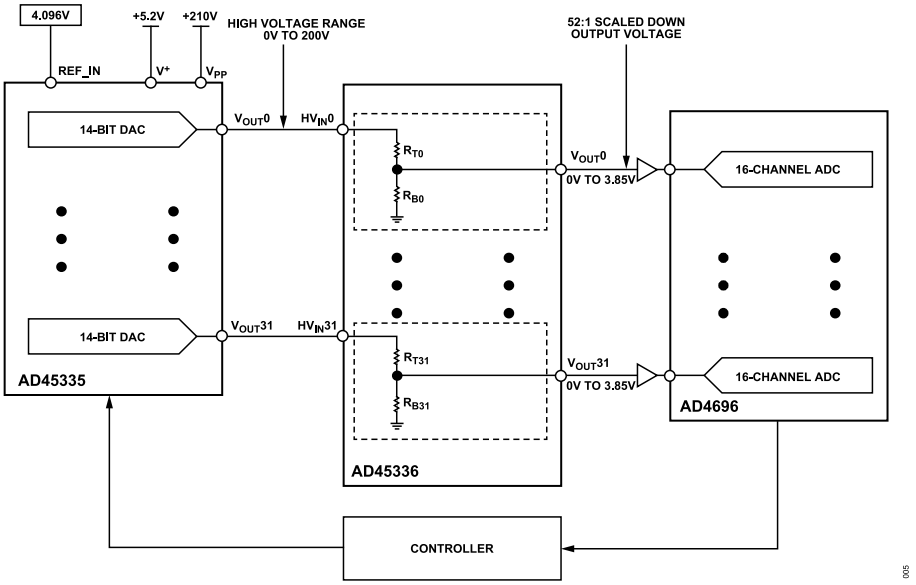

Figure 7. AD45336 as a Companion Product of the AD45335, 32-Channel High-Voltage DAC

OUTLINE DIMENSIONS

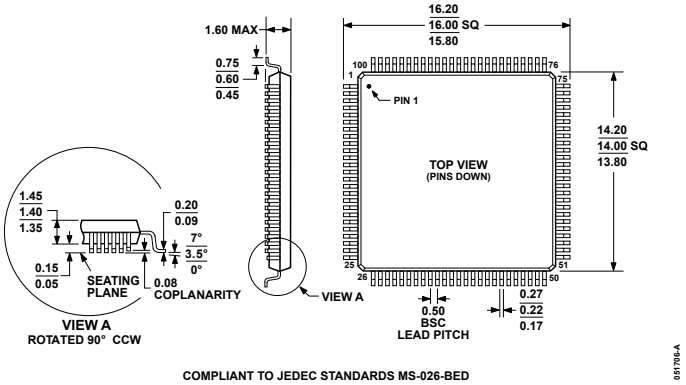

Figure 8. 100-Lead Low Profile Quad Flat Package [LQFP]
(ST-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD45336KSTZ	−10°C to +85°C	100-Lead Low Profile Quad Flat Package [LQFP]	Tray, 90	ST-100-1
AD45336KSTZ-RL	−10°C to +85°C	100-Lead Low Profile Quad Flat Package [LQFP]	Reel, 1000	ST-100-1

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model[1]	Model
EVAL-AD45336EBZ	Evaluation Board

[1] Z = RoHS-Compliant Part.