24-Bit, 62.5kSPS, Multichannel, Low-Noise Precision Sigma-Delta ADC

FEATURES

- Input referred noise: 10nV at 3.8SPS, Gain = 128
- Crosspoint multiplexed analog inputs
- 4 Differential/8 Pseudodifferential inputs
- Ultra-low noise integrated PGA, gains of 0.5 to 128
- Output data rate: 3.8SPS to 62.5kSPS
- Flexible digital filters
  - Low latency sinc filters
  - Simultaneous 50Hz/60Hz rejection
- Band-gap reference with 5ppm/°C drift typical
- Internal oscillator
- Analog power supply: 4.75V to 5.25V or ±2.5V
- Digital power supply: 1.7V to 5.25V
- Matched programmable excitation current sources
- Low-side power switches
- On-chip bias voltage generator
- Internal temperature sensor
- Four general-purpose inputs/outputs
- Internal and system calibration
- Sensor burnout detection
- Diagnostic functions
- Per channel configuration
- Flexible automatic channel sequencer
- 3- or 4-wire serial interface (Schmitt trigger on SCLK)
  - SPI, QSPI, MICROWIRE, and DSP compatible
- TDM compatible interface for data streaming
- Performance temperature range: −40°C to +105°C
- Functional temperature range: −40°C to +125°C
- Available in 32-lead 4mm x 6mm LFCSP package

APPLICATIONS

- Industrial process control: PLC/DCS modules
- Temperature measurement
- Pressure measurement
- Medical and scientific instrumentation
- Chromatography
- Environmental monitoring
- Electrical test and measurement
- Instrumentation
- Weigh scale

FUNCTIONAL BLOCK DIAGRAM

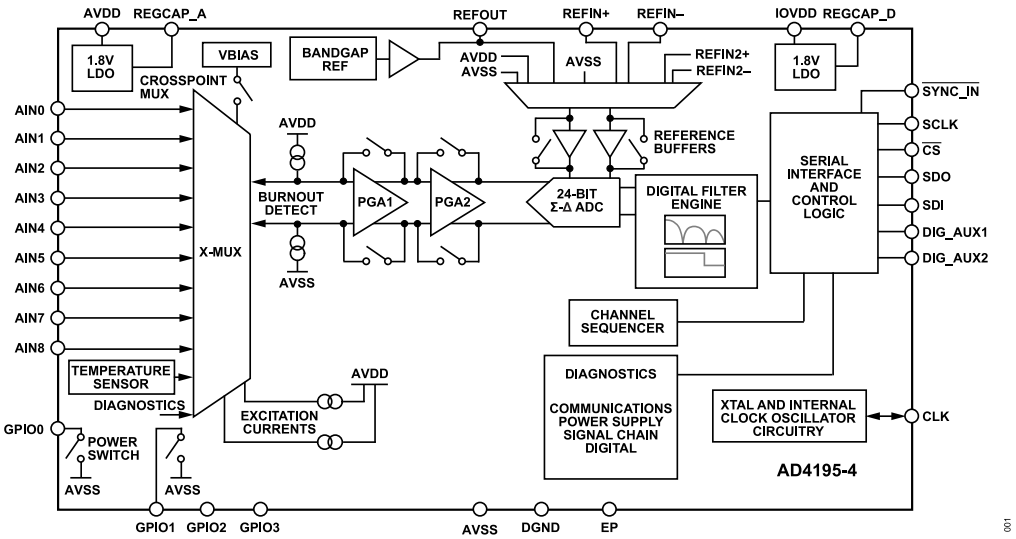

Figure 1. AD4195-4 Functional Block Diagram

TABLE OF CONTENTS

TABLE OF CONTENTS

REVISION HISTORY

1/2025—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD4195-4 is a low noise, completely integrated analog front end for high precision measurement applications. The device contains a low noise, 24-bit Σ-Δ analog-to-digital converter (ADC) and can be configured to have four differential or eight single-ended or pseudodifferential inputs. The on-chip low-noise gain stage ensures that signals of small amplitude can be interfaced directly to the ADC.

The AD4195-4 offers the highest degree of signal chain integration. The device contains an internal reference and accepts two external differential references, which can be internally buffered. Other key integrated features include:

- Programmable gain amplifier (PGA). Due to the programmable gain (0.5 to 128), the PGA allows direct interfacing to transducers with low output amplitudes such as resistive bridges, thermocouples, and resistance temperature detectors (RTDs).
- The PGA has a wide common-mode input range, which gives designers a greater margin for widely varying input common modes.
- Low drift, well matched precision current sources. Use the excitation current sources to excite 2-, 3-, and 4-wire RTDs or bridge type sensors. Excitation current output options include 10µA, 50µA, 100µA, 250µA, 500µA, 1mA, and 1.5mA. The currents can also be added if higher currents are required.
- Use the low-side power switch (PDSW) to power down bridge sensors between conversions.
- Voltage bias for thermocouples (the VBIAS source sets the common-mode voltage of a channel to (AVDD + AVSS)/2.
- The smart sequencer allows the conversion of each enabled preconfigured channel in a predetermined order, which allows a mix of transducer, system checks, and diagnostic measurements to be interleaved. The sequencer eliminates the need for repetitive serial interface communication with the device to change configuration. Configure the 16-channels in the sequence. Each of these channels selects from eight user-defined ADC setups that allow selection of gain, filter type, output data rate, buffering, and reference source.

The AD4195-4 also has extensive diagnostic functionality integrated as part of its comprehensive feature set. These diagnostics include a cyclic redundancy check (CRC), signal chain checks, and serial interface checks, which lead to a more robust solution.

The device also offers a multitude of filter options, which ensure that the user has the highest degree of flexibility. The part contains sinc filters, which allow faster settling. In addition, the AD4195-4 offers multiple options for simultaneous 50Hz and 60Hz rejection.

The device operates with a single analog power supply from 4.75V to 5.25V or a bipolar 2.5V power supply. The digital supply has a range of 1.7V to 5.25V. It is specified for a temperature range of −40°C to +105°C. The AD4195-4 is housed in a 32-lead LFCSP package.

SPECIFICATIONS

AVDD = 4.75V to 5.25V, IOVDD = 1.7V to 5.25V, AVSS = DGND = 0V, REFIN+ = 2.5V (external reference), REFIN− = AVSS, MCLK = 16MHz, $T_A = T_{MIN}$ to T_{MAX} (−40°C to +105°C), unless otherwise noted.

Table 1. Specifications

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED CODING AND PERFORMANCE					
Output Data Rate (ODR)					
Sinc5		976.5		62,500	SPS
Sinc5 + Avg		3.8		62,500	SPS
Sinc3		3.8		62,500	SPS
50Hz/60Hz Post Filters		16.67	20	25	SPS
No Missing Codes[2]		24			Bits
Data output coding	Bipolar mode	2s complement			
	Unipolar mode	Straight Binary			
Resolution		See the RMS and Noise Performance section			
Noise		See the RMS and Noise Performance section			
ACCURACY					
Gains			0.5, 1, 2, 4, 8, 16, 32, 64, 128		
Integral Nonlinearity (INL)	Gain = 1, Gain = 1 precharge	−3	±1	+3	ppm of FSR
	All other gains	−12	±3	+12	ppm of FSR
Precalibration Offset Error[3]	Gain = 1 precharge	−70	±30	+70	µV
	Gain < 16	−45 − (40/gain)	±(15 + (40/gain))	+45 + (40/gain)	µV
	Gain ≥ 16	−43	±6	+43	µV
Offset Error Drift vs. Temperature[2]	Gain = 1 precharge	−55	±20	+55	nV/°C
	Gain < 8	−140/gain	±50/gain	+140/gain	nV/°C
	Gain = 8, 16, 32	−35	±20	+35	nV/°C
	Gain = 64, 128	−50	±20	+50	nV/°C
Gain Error[3]	Gain = 1 precharge, T_A = 25°C	−50	±10	+50	ppm of FSR
	All other gains, T_A = 25°C	−250	±50	+250	ppm of FSR
Gain Error Drift vs. Temperature[2]	All gains	−1	±0.5	+1	ppm/°C
REJECTION					
DC Power Supply Rejection	V_{IN} = 1V/gain, All supplies				
	Gain = 0.5		98		dB
	Gain = 1 precharge and Gains of 1 to 8	88	104		dB
	Gain of 16 to 128	100	116		dB
Common-Mode Rejection[4]	V_{IN} = 1V/gain				
At DC	Gain = 0.5		106		dB
	Gain = 1 precharge and Gains of 1 to 8	98	108		dB
	Gains of 16 to 128	107	125		dB
At 50Hz, 60Hz	50ms settling postfilter, 50Hz ± 1Hz and 60Hz ± 1Hz	120			dB
Normal Mode Rejection[2]	50Hz ± 1Hz and 60Hz ± 1Hz				
	Internal clock, 50ms settling postfilter	74	89		dB
	External clock, 50ms settling postfilter	89			dB
ANALOG INPUTS					

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Differential Input Voltage Range[5]	VREF = (REF+ - REF−) or internal reference	$-V_{REF}$/gain		$+V_{REF}$/gain	V
Single-Ended Input Voltage Range		0		V_{REF}/Gain	V
Absolute AIN Voltage Limits[2]		AVSS		AVDD	V
Input Capacitance			8		pF
Analog Input Current	Absolute input current measured with AIN between AVSS + 0.1V and AVDD − 0.1V				
	Differential input current measured with full-scale input, V_{CM} = (AVDD+AVSS)/2				
Gain = 1 precharge					
Absolute Input Current		−225	±140	+225	nA
Differential Input Current		−64	±28	+64	nA
Absolute Input Current Drift[2]			280		pA/°C
Gain = 1					
Absolute Input Current		−15	±2	+15	nA
Differential Input Current		−11	±2	+11	nA
Absolute Input Current Drift[2]			12		pA/°C
Gain = 0.5					
Absolute Input Current		−15	±2	+15	nA
Differential Input Current		−22	±4	+22	nA
Absolute Input Current Drift[2]			38		pA/°C
Gain = 128					
Absolute Input Current		−20	±2	+20	nA
Differential Input Current		−10	±2	+10	nA
Absolute Input Current Drift[2]			45		pA/°C
All other gains					
Absolute Input Current		−15	±2	+15	nA
Differential Input Current		−10	±2	+10	nA
Absolute Input Current Drift[2]			70		pA/°C
INTERNAL REFERENCE	100nF external capacitor to AVSS				
Initial Accuracy[6]	REFOUT with respect to AVSS, T_A = 25°C	2.495	2.5	2.505	V
Temperature Coefficient			±5	+15	ppm/°C
Reference Load Current, I_{LOAD}		−10		+10	mA
Thermal Hysteresis	Cycle of 25°C, +75°C, −25°C, +25°C		44		ppm
Power Supply Rejection	AVDD (line regulation)		100		dB
Load Regulation	$\Delta V_{OUT}/\Delta I_{LOAD}$		12		ppm/mA
Voltage Noise	e_N, 0.1Hz to 10Hz, 2.5V reference		4.5		µV rms
Voltage Noise Density	e_N, 1kHz, 2.5V reference		215		nV/√Hz
Turn-On Settling Time	100nF REFOUT capacitor		200		µs
Short-Circuit Current, I_{SC}			28		mA
EXTERNAL REFERENCE INPUTS					
Differential Input Range[2]	V_{REF} = REF+ − REF−	1	2.5	AVDD − AVSS	V
Absolute Voltage Limits[2]					
Reference Buffers Disabled		AVSS − 0.05		AVDD + 0.05	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Reference Buffers Enabled	Full buffer or precharge buffer	AVSS		AVDD	V
REFIN Input Current (Reference Buffers Disabled)					
Reference Input Current			±22		µA/V
Reference Input Current Drift	External clock		±1.2		nA/V/°C
	Internal clock		±6		nA/V/°C
Reference Buffers Enabled					
Reference Input Current	Precharge buffer		±6		µA
	Full buffer		±55		nA
Reference Input Current Drift	Precharge buffer		40		nA/°C
	Full buffer		1.25		nA/°C
Normal Mode Rejection	See the Rejection parameter				
VBIAS					
Output voltage setting			(AVDD + AVSS)/2		V
Output Impedance			1		kΩ
Start-up time	Dependent on the capacitance connected to AINn		9		µs/nF
EXCITATION CURRENTS					
Current Settings			10, 50, 100, 250, 500, 1000, 1500		µA
Output Compliance[2]	10µA, 50µA, 100µA, 1% accuracy			AVDD − 1.25	V
	250µA/500µA/1mA/1.5mA, 1% accuracy			AVDD – 1.45	V
Initial Accuracy	T_A = 25°C, 10µA		±3		%
	T_A = 25°C, 50µA, 100µA	−1	±0.1	+1	%
	T_A = 25°C, >100µA	−2	±0.2	+2	%
Drift[2]	10µA		±20		ppm/°C
	50µA, 100µA	−30	±5	+30	ppm/°C
	>100µA	−80	±25	+80	ppm/°C
Current Mismatch					
Same Current Matching[2]	10µA		±1.3		%
	250µA, 1mA	−1.2	±0.1	+1.2	%
	50µA/100µA/500µA/1.5mA	−0.7	±0.1	+0.7	%
Different Current Matching			±1		%
Drift Matching[2]	Current sources at the same value				
	10µA		±3		ppm/°C
	50µA, 100µA, 250µA	−7	±2	+7	ppm/°C
	> 250µA	−4	±1	+4	ppm/°C
Line Regulation (AVDD)	AVDD = 5V ± 5%		150		ppm/V
Load Regulation	>10µA		40		ppm/V
Start-up time	R_{LOAD} = 1kΩ, C_{LOAD} = 0pF Dependent on the load connected to AINn		7		µs
TEMPERATURE SENSOR					
Accuracy	After user calibration at 25°C		±2		°C
Sensitivity			477		µV/K
LOW-SIDE POWER SWITCH					

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Ron			10	15	Ω
Current Through Switch[2]			25		mA
PULL-UP CURRENTS					
Source Current			100		nA
BURNOUT CURRENTS					
Source/Sink Current			±0.1, 2, 10		µA
Accuracy	Sinking/Sourcing				
	±0.1µA		25		%
	±2µA, ±10µA		10		%
GENERAL-PURPOSE I/O (GPIO0 to GPIO3)[2]	With respect to AVSS				
Input Mode Leakage Current		−1		+1	µA
Floating State Output Capacitance			5		pF
Output High Voltage, V_{OH}	I_{SOURCE} = 200µA	AVSS + 4			V
Output Low Voltage, V_{OL}	I_{SINK} = 800µA			AVSS + 0.4	V
Input High Voltage, V_{IH}		AVSS + 3			V
Input Low Voltage, V_{IL}				AVSS + 0.7	V
DIAGNOSTIC TRIP POINTS					
Reference Detect Level		0.6		0.85	V
Reference/AIN OV/UV Trip Level					
Overvoltage		AVDD + 0.065			V
Undervoltage				AVSS – 0.065	V
Reference/AIN OV/UV Clear Level					
Overvoltage		AVDD + 0.015			V
Undervoltage				AVSS − 0.01	V
Excitation Current Source Compliance	10µA to 100µA	AVDD − 1.3		AVDD − 0.8	V
	>100µA	AVDD − 1.6		AVDD − 1	V
ALDO Trip Point			1.5		V
DLDO Trip Point			1.6		V
CLOCK					
Internal Clock					
Frequency			16		MHz
Accuracy		−2.5		+2.5	%
Duty Cycle			50:50		%
External Clock (CLK)		1	16	17	MHz
Minimum Low Time		27.6			ns
Minimum High Time		27.6			ns
LOGIC INPUTS[2]					
Input High Voltage, V_{INH}		0.8 × IOVDD			V
Input Low Voltage, V_{INL}				0.2 × IOVDD	V
Hysteresis			0.04		V
Leakage Currents	$\overline{\text{SYNC\_IN}}$ Pin			+15	uA
	All other pins	−1		+1	uA
Input Capacitance	All digital inputs		10		pF
LOGIC OUTPUT[2] (CLK, DIG_AUX1, DIG_AUX2, SDO)					
Output High Voltage, V_{OH}[2]	I_{SOURCE} = 1mA	0.8 × IOVDD			V
Output Low Voltage, V_{OL}[2]	I_{SINK} = 2mA			0.4	V
Leakage Current	Floating state	−1		+1	µA
Output Capacitance	Floating state		10		pF

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM CALIBRATION[2]					
Full-Scale (FS) Calibration Limit				1.05 × FS	V
Zero-Scale Calibration Limit		−1.05 × FS			V
Input Span		0.8 × FS		2.1 × FS	V
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD to AVSS		4.75		5.25	V
AVSS to DGND		−2.625		0	V
IOVDD to DGND		1.7		5.25	V
IOVDD to AVSS	For AVSS < DGND			6.35	V
POWER SUPPLY CURRENTS[7]					
AVDD Current, External Reference					
Gain = 1 precharge			5	6.2	mA
Gain < 16 except Gain = 1 precharge			7	8.8	mA
Gain ≥ 16			10	12.2	mA
I_{AVDD} Increase Due To					
Both Reference Buffers					
Precharge			0.7	0.9	mA
Full Buffer			1.7	2.2	mA
Internal Reference			0.5	0.6	mA
Diagnostics			0.1		mA
Excitation Currents			0.06		mA
VBIAS			0.05		mA
IOVDD Current	External clock		1	1.35	mA
	Internal clock		1.3	1.65	mA
AVDD Standby Mode	LDOs on only		70	135	µA
AVDD Power-Down Mode			0.2	1.2	µA
IOVDD Standby Mode	LDOs on only		15	280	µA
IOVDD Power-Down Mode			0.8	1.5	µA
POWER DISSIPATION[7]	IOVDD = 5.25V, AVDD = 5.25V				
Full Operating Mode	Gain = 1 precharge, reference buffers disabled, external clock and reference		32	40	mW
	Gain > 16, reference buffers enabled, internal clock and reference		71	88	mW
Standby Mode	LDOs on only		447	2,180	µW
Power-Down Mode			5.25	14.2	µW

1 Temperature range is −40°C to +105°C.

2 These specifications are not production tested but are supported by characterization data at the initial product release.

3 The offset error is in the order of the noise for the programmed ODR selected following a system or internal zero-scale calibration. A system full-scale calibration reduces the gain error to the order of the noise for the programmed ODR.

4 The minimum and maximum voltage on AINP and AINM are AVSS + 0.1V and AVDD − 0.1V.

5 The maximum allowed differential analog input range is ±(AVDD − 0.65V)/gain while the maximum allowed single-ended analog input range is 0V to (AVDD − 0.65V)/gain which applies when higher reference voltages are used.

6 This specification includes moisture sensitivity level (MSL) preconditioning effects.

7 This specification is with no load on the REFOUT, excitation currents, and digital output pins. Digital inputs are connected to IOVDD or DGND.

SPECIFICATIONS

TIMING CHARACTERISTICS

IOVDD = 1.7V to 5.25V with Bit DIG_OUT_STR set when IOVDD < 3V, DGND = 0V, Input Logic 0 = 0V, Input Logic 1 = IOVDD, C_{LOAD} = 20pF, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Test Conditions/Comments[1, 2]
SCLK			
t_3	25	ns min	SCLK high pulse width
t_4	25	ns min	SCLK low pulse width
t_{12}	8.25/f_{MOD}	ns min	$\overline{RDY}$ high time if $\overline{RDY}$ is low and the next conversion is available(f_{MOD} = MCLK/8)
t_{13}	2/MCLK	ns min	$\overline{SYNC\_IN}$ low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to SDO active time
	12.5	ns max	4.75V < IOVDD ≤ 5.25V
	17.5	ns max	3V ≤ IOVDD ≤ 4.75V
	25	ns max	1.7V ≤ IOVDD < 3V
t_2[3]	5	ns min	SCLK active edge to data valid delay[4]
	12.5	ns max	4.75V < IOVDD ≤ 5.25V
	17.5	ns max	3V ≤ IOVDD ≤ 4.75V
	25	ns max	1.7V ≤ IOVDD < 3V
t_5[5]	2.5	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	20	ns max	
t_6	5	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	9	ns min	SCLK inactive edge to $\overline{RDY}$ high. SDO and $\overline{RDY}$ use separate pins or SDO and $\overline{RDY}$ share a pin with Bit SDO_RDYB_DLY cleared. Shared pin returns to functioning as $\overline{RDY}$ after the SCLK inactive edge
t_{7A}	t_5	ns min	Data valid after $\overline{CS}$ inactive edge (when SDO and $\overline{RDY}$ share a pin). Bit SDO_RDYB_DLY is set. Shared pin continues to function as SDO until $\overline{CS}$ is taken high
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	8	ns min	Data valid to SCLK edge setup time
t_{10}	8	ns min	Data valid to SCLK edge hold time
t_{11}	5	ns min	$\overline{CS}$ rising edge to SCLK edge hold time
CONTINUOUS TRANSMIT OPERATION			
t_{14}	2	ns max	DCLK active edge to $\overline{RDY}$ falling edge setup time
t_{15}			Difference between (data valid to DCLK edge setup time) and DCLK low time
	t_{DCLK_LOW} − 1	ns max	4.75V < IOVDD ≤ 5.25V
	t_{DCLK_LOW} − 3.5	ns max	3V ≤ IOVDD ≤ 4.75V
	t_{DCLK_LOW} − 2.5	ns max	1.7V ≤ IOVDD < 3V
t_{16}	t_{DCLK_HIGH} − 3.5	ns max	Difference between (data valid to DCLK edge hold time) and DCLK high time
t_{17}	3.5	ns min	DCLK rising edge to $\overline{RDY}$ high time
t_{18}			Difference between DCLK high pulse width and applied external MCLK high time. Valid for divide by 1 option
	−2	ns max	4.75V < IOVDD ≤ 5.25V
	−6.5	ns max	3V ≤ IOVDD ≤ 4.75V
	−4	ns max	1.7V ≤ IOVDD < 3V
t_{19}			Difference between DCLK low pulse width and applied external MCLK low time. Valid for divide by 1 option
	1.5	ns max	4.75V < IOVDD ≤ 5.25V
	3.5	ns max	3V ≤ IOVDD ≤ 4.75V

SPECIFICATIONS

Table 2. Timing Characteristics (Continued)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Test Conditions/Comments[1, 2]
	2	ns max	1.7V ≤ IOVDD < 3V

1 Sample tested during initial release to ensure compliance.

2 See Figure 4 and Figure 5.

3 This parameter is defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

4 The SCLK active edge is the falling edge of SCLK.

5 $\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care must be taken to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

TIMING DIAGRAMS

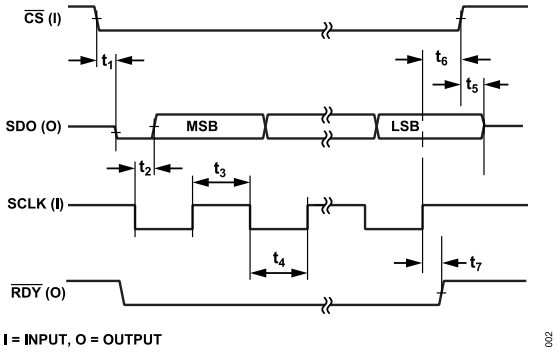

Figure 2. Read Cycle Timing Diagram (SDO and $\overline{RDY}$ Use Separate Pins)

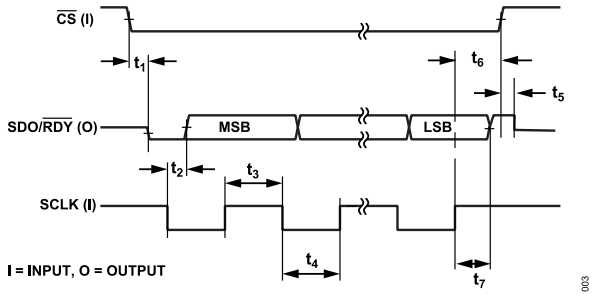

Figure 3. Read Cycle Timing Diagram (SDO and $\overline{RDY}$ Share a Pin with Bit SDO_RDYB_DLY Cleared)

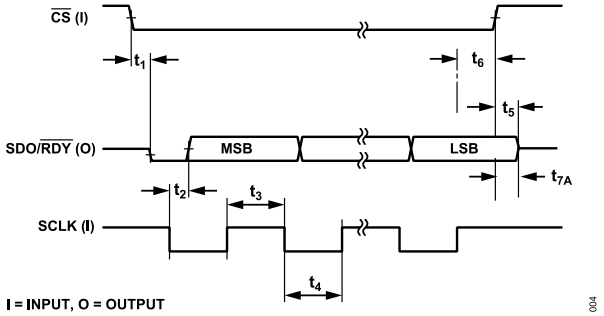

Figure 4. Read Cycle Timing Diagram (SDO and $\overline{RDY}$ Share a Pin with Bit SDO_RDYB_DLY Set)

SPECIFICATIONS

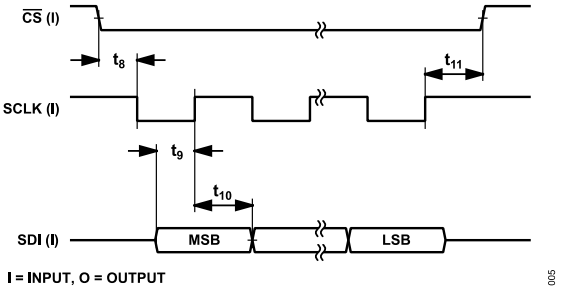

Figure 5. Write Cycle Timing Diagram

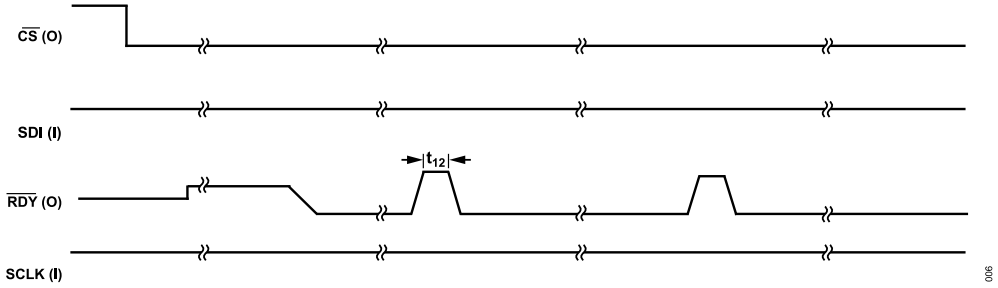

Figure 6. DOUT/RDY High Time when RDY is Initially Low and the Next Conversion is Available

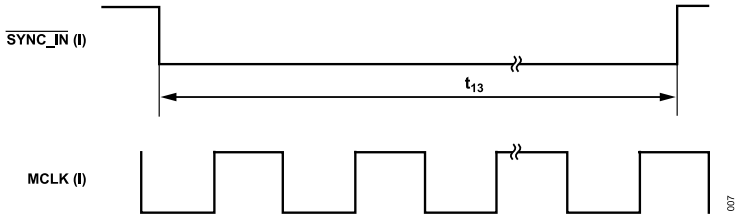

Figure 7. SYNC_IN Pulse Width

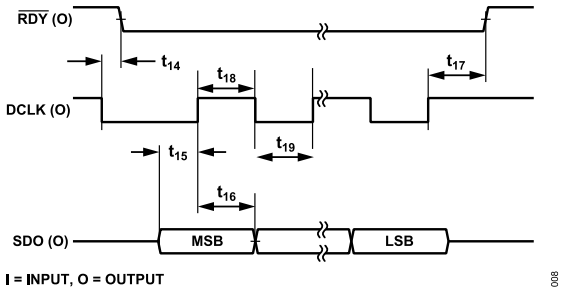

Figure 8. Continuous Transmit

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings

Parameter	Rating
AVDD to AVSS	−0.3V to +6.5V
AVDD to DGND	−0.3V to +6.5V
IOVDD to DGND	−0.3V to +6.5V
IOVDD to AVSS	−0.3V to +7.5V
AVSS to DGND	−3.25V to +0.3V
Analog Input Voltage to AVSS	−0.3V to AVDD + 0.3V
Reference Input Voltage to AVSS	−0.3V to AVDD + 0.3V
GPIO Input Voltage to AVSS	−0.3V to AVDD + 0.3V
GPIO Output Voltage to AVSS	−0.3V to AVDD + 0.3V
REFOUT to AVSS	−0.3V to AVDD + 0.3V
Digital Input Voltage to DGND	−0.3V to IOVDD + 0.3V
Digital Output Voltage to DGND	−0.3V to IOVDD + 0.3V
Analog Input/Digital Input Current	10mA
Temperature	
Operating Range	−40°C to +105°C
Storage Range	−65°C to +150°C
Maximum Junction	150°C
Lead Soldering, Reflow	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JB} is the junction-to-board thermal resistance. θ_{JC} is the junction-to-case thermal resistance. Thermal resistance values specified in Table 4 are calculated based on JEDEC specifications and must be used in compliance with JESD51-12. The worst-case junction temperature is reported. The values in Table 4 are calculated based on the standard JEDEC 2S2P thermal test board in a natural convection test environment. For more details, refer to the JEDEC JESD51 series.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC_TOP}	Unit
CP-32-34	39.49	9.93	14.86	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field-induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4195-4

Table 5. AD4195-4, 32-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM	4	3A
FICDM	1.25	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

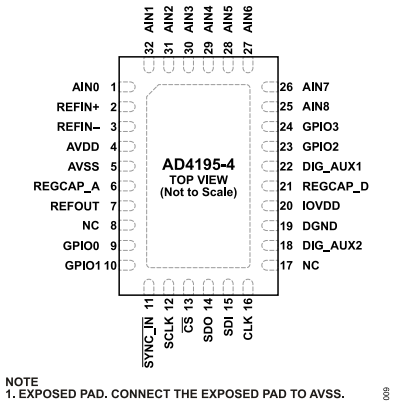

Figure 9. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AIN0	Analog Input 0/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn register to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.
2	REFIN+	Positive Reference Input. Apply an external reference between REFIN+ and REFIN−. REFIN+ can be anywhere between AVDD and AVSS + 1V. The nominal reference voltage (REFIN+ − REFIN−) is 2.5V, but the device functions with a reference from 1V to AVDD.
3	REFIN-	Negative Reference Input. This reference input can be anywhere between AVSS and AVDD – 1V.
4	AVDD	Analog Supply Voltage. This is relative to AVSS.
5	AVSS	Analog Supply Voltage. The voltage on AVDD is referenced to AVSS. The differential between AVDD and AVSS must be between 4.75V and 5.25V. Take the AVSS below 0V to provide a bipolar power supply to the AD4195-4. For example, connect the AVSS to −2.5V and the AVDD to +2.5V, respectively, which provides a ±2.5V supply to the ADC.
6	REGCAP_A	Analog Low Dropout (LDO) Regulator Output. Decouple this pin to AVSS with a 1µF capacitor in parallel with a 0.1µF capacitor.
7	REFOUT	Internal Reference Output. This is relative to AVSS. The buffered output of the internal 2.5V voltage reference can be output to this pin. Decouple this pin to AVSS with a 0.1µF capacitor
8	NC	No Connect.
9	GPIO0	General-Purpose Input or Output/Positive Reference Input/Power Switch/Excitation Current. Configure this pin as a general-purpose input/output bit, referenced between AVSS and AVDD. This pin also functions as a positive reference input for REFIN2±. REFIN2+ can be anywhere between AVDD and AVSS + 1V. The nominal reference voltage (REFIN2+ to REFIN2−) is 2.5V, but the device functions with a reference from 1V to AVDD. The pin can also function as a low-side power switch to AVSS. Any of the internal programmable excitation current sources can also be made available at this pin.
10	GPIO1	General-Purpose Input or Output/Negative Reference Input/Power Switch/Excitation Current. Configure this pin as a general-purpose input/output bit, referenced between AVSS and AVDD. This pin also functions as a negative reference input for REFIN2±. REFIN2− can be anywhere between AVSS and AVDD − 1V. The pin can also function as a low-side power switch to AVSS. Any of the internal programmable excitation current sources can also be made available at this pin.
11	$\overline{\text{SYNC\_IN}}$	Synchronization Input. This pin is a logic input that allows synchronization of the digital filters and analog modulators when using multiple AD4195-4 devices. In the default mode, taking $\overline{\text{SYNC\_IN}}$ low resets the nodes of the digital filter, the filter control logic, the calibration control logic, and the analog modulator is held in a reset state. $\overline{\text{SYNC\_IN}}$ does not affect the digital interface but does reset $\overline{\text{RDY}}$ to a high state if $\overline{\text{RDY}}$ is low. If multiple channels are enabled, using the $\overline{\text{SYNC\_IN}}$ function forces the sequence to be reset. Therefore, when $\overline{\text{SYNC\_IN}}$ is taken high, the conversion sequence begins from the first enabled channel. This input is also used in ALT_SYNC mode. When multiple channels are enabled in ALT_SYNC mode, the sequencer is not reset and the $\overline{\text{SYNC\_IN}}$ pin is used to control the instant at which the ADC begins sampling on the newly selected channel in the sequence. Therefore, following the channel change, the ADC waits until $\overline{\text{SYNC\_IN}}$ is taken high to begin sampling. For more details on using this pin, see the ADC Synchronization section.
12	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt triggered input, which makes the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
13	$\overline{\text{CS}}$	Chip Select Input. This is an active low logic input that selects the ADC. Use $\overline{\text{CS}}$ to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{\text{CS}}$ can be hardwired low with only SCLK, DIN, and SDO

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
		interfacing with the device. When $\overline{CS}$ is hardwired low, the SDO pin is always enabled. Therefore, the SDO pin requires a dedicated pin on the microprocessor.
14	SDO	Serial Data Output/Data Ready Output. SDO functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, SDO can operate as a data ready pin $\overline{RDY}$, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The SDO falling edge can also be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the SDO pin. When $\overline{CS}$ is low, the data/control word information is placed on the SDO pin on the SCLK falling edge and is valid on the SCLK rising edge. Note that the data ready function can be made available on pin DIG_AUX1, which is useful when a user wants independent serial data out and data ready functions. The AD4195-4 also includes a continuous transmit mode, which simplifies the reading of conversions. The AD4195-4 provides the DCLK and frame synchronization signal. Therefore, conversion results are automatically placed on SDO when available. When this mode is enabled, the SDO pin is dedicated to outputting conversion results until the continuous transmit mode is disabled.
15	SDI	Serial Data Input to the Input Shift Register on the ADC. Data in the input shift register is transferred to the control registers within the ADC, with the register address selected during the instruction phase.
16	CLK	Clock Input or Output. Based on the CLOCKSEL bits in the CLOCK_CTRL register. The following three options are available for selecting the MCLK source: Internal oscillator: no output, Internal oscillator: output to CLK pin and External clock: input to CLK pin (input must be at IOVDD logic levels).
17	NC	No Connect.
18	DIG_AUX2	Clock DCLK in the Continuous Transmit mode/START Input. In the continuous transmit mode, this pin provides the data clock DCLK. The pin can also be used in conjunction with the DIG_AUX1 pin to force synchronization on multiple devices, which share a common main clock. This mode internally generates a synchronization signal SYNC_OUT from the applied START signal, SYNC_OUT being synchronized with the internal main clock. SYNC_OUT is applied to all AD4195-4 ADCs in a multi AD4195-4 system to force all the ADCs to have synchronous conversion behavior.
19	DGND	Digital Ground Reference Point.
20	IOVDD	Serial Interface Supply Voltage, 1.7V to 5.25V. IOVDD is independent of AVDD. For example, the serial interface can operate at 1.7V with AVDD at 5.25V.
21	REGCAP_D	Digital LDO Regulator Output. Decouple this pin to DGND with a 1µF capacitor in parallel with a 0.1µF capacitor.
22	DIG_AUX1	Data Ready for SPI interface/Data Ready in the Continuous Transmit mode/Synchronization Out. When using the serial interface, the data ready function can be output on this pin to dedicate the SDO pin to being a serial data output pin only. When the continuous transmit mode is used, this pin again functions as a data ready pin with DIG_AUX2 providing the clock DCLK for the data transmissions. The pin can also be used in conjunction with the DIG_AUX2 pin to force synchronization on multiple devices, which share a common main clock. This mode internally generates a synchronization signal SYNC_OUT from the applied START signal, SYNC_OUT being synchronized with the internal main clock. SYNC_OUT is applied to all AD4195-4 ADCs in a multi AD4195-4 system to force all the ADCs to have synchronous conversion behavior.
23	GPIO2	General-Purpose Input or Output/Excitation Current. Configure this pin as a general-purpose input/output bit, referenced between AVSS and AVDD. Any of the internal programmable excitation current sources can also be made available at this pin.
24	GPIO3	General-Purpose Input or Output/Excitation Current. Configure this pin as a general-purpose input/output bit, referenced between AVSS and AVDD. Any of the internal programmable excitation current sources can also be made available at this pin.
25	AIN8	Analog Input 8/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn registers to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.
26	AIN7	Analog Input 7/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn registers to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.
27	AIN6	Analog Input 6/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn registers to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.
28	AIN5	Analog Input 5/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn registers to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.
29	AIN4	Analog Input 4/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn registers to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.
30	AIN3	Analog Input 3/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn registers to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
31	AIN2	Analog Input 2/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn registers to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.
32	AIN1	Analog Input 1/Excitation Current/Bias Voltage. This input pin is configured through the CHANNEL_MAPn registers to be the positive or negative terminal of a differential or pseudodifferential input. Alternatively, any of the internal programmable excitation current sources can be output to this pin. A bias voltage midway between the analog power supply rails can be output at this pin.
	EP	Exposed Pad. Connect the exposed pad to AVSS.

TYPICAL PERFORMANCE CHARACTERISTICS

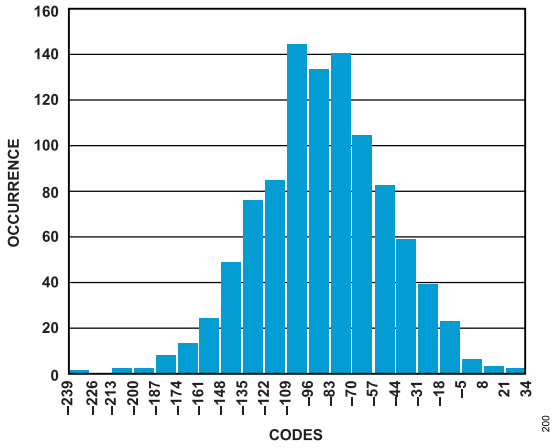

Figure 10. Noise Histogram (Sinc^5 + Avg Filter, 62.5kSPS, PGA_Gain = 1)

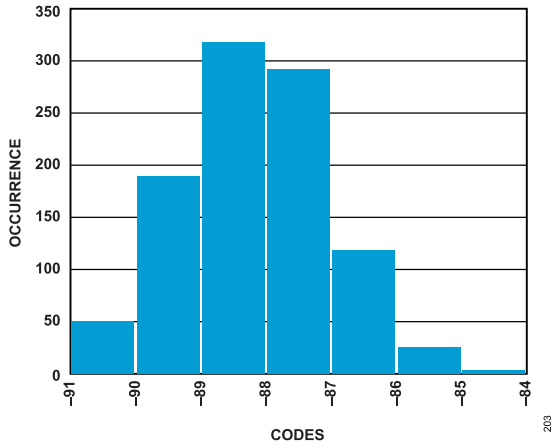

Figure 13. Noise Histogram (Sinc^5 + Avg Filter, 50SPS, PGA_Gain = 1)

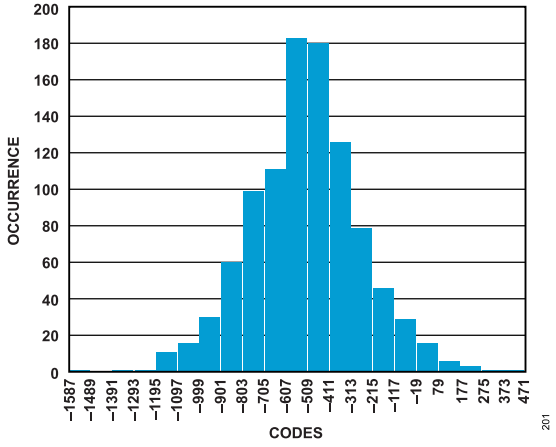

Figure 11. Noise Histogram (Sinc^5 + Avg Filter, 62.5kSPS, PGA_Gain = 16)

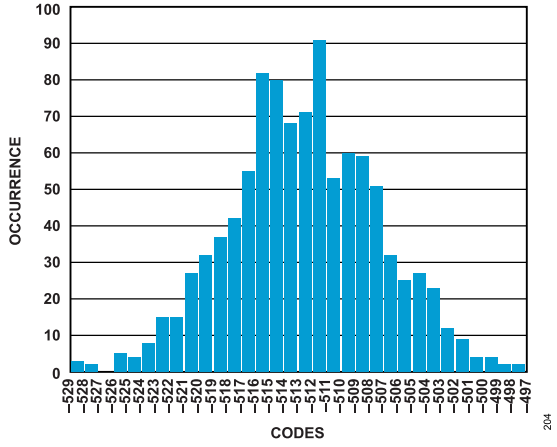

Figure 14. Noise Histogram (Sinc^5 + Avg Filter, 50SPS, PGA_Gain = 16)

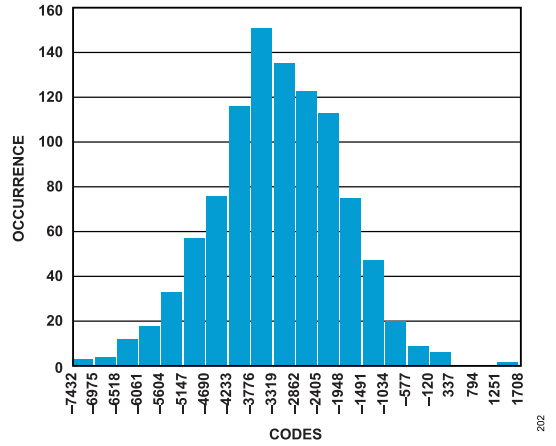

Figure 12. Noise Histogram (Sinc^5 + Avg Filter, 62.5kSPS, PGA_Gain = 128)

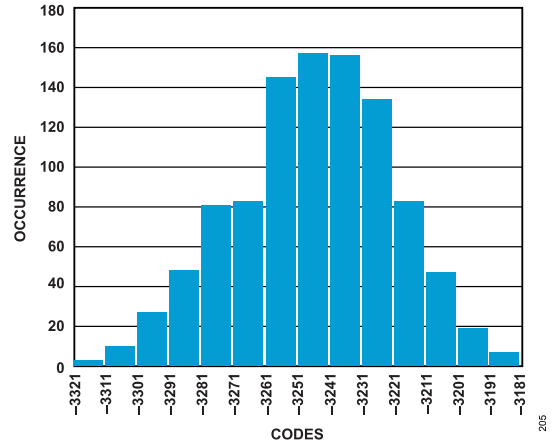

Figure 15. Noise Histogram (Sinc^5 + Avg Filter, 50SPS, PGA_Gain = 128)

TYPICAL PERFORMANCE CHARACTERISTICS

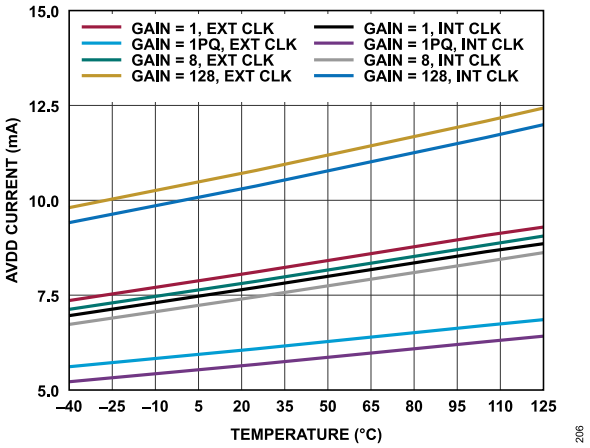

Figure 16. AVDD Current vs. Temperature (Internal Reference)

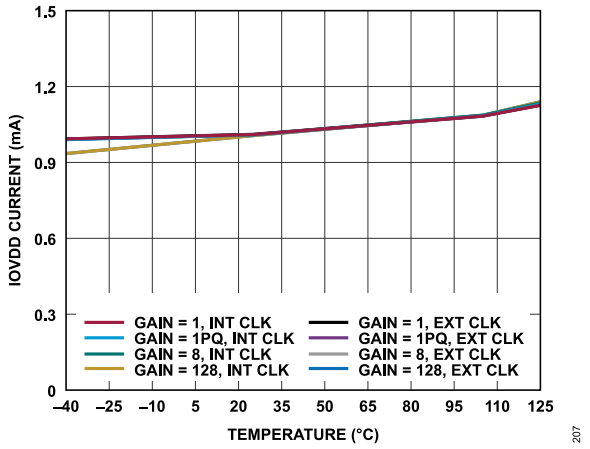

Figure 17. IOVDD Current vs. Temperature (Internal Reference)

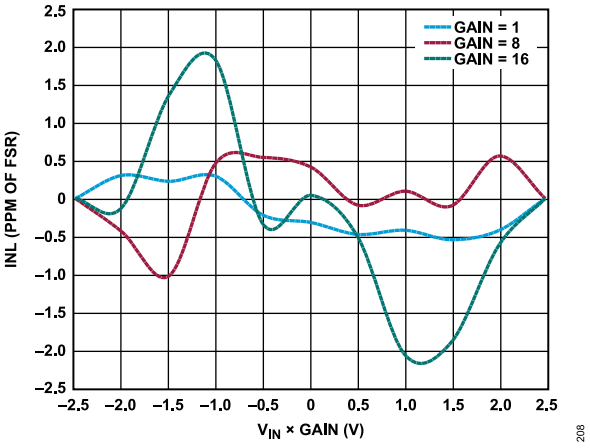

Figure 18. INL vs. Differential Input Signal (Analog Input × Gain) at 25°C

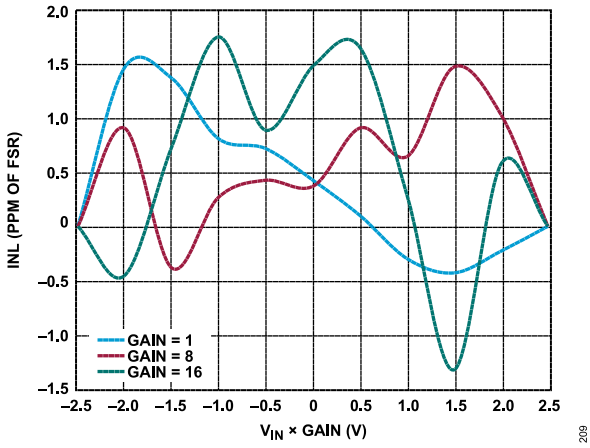

Figure 19. INL vs. Differential Input Signal (Analog Input × Gain) at −40°C

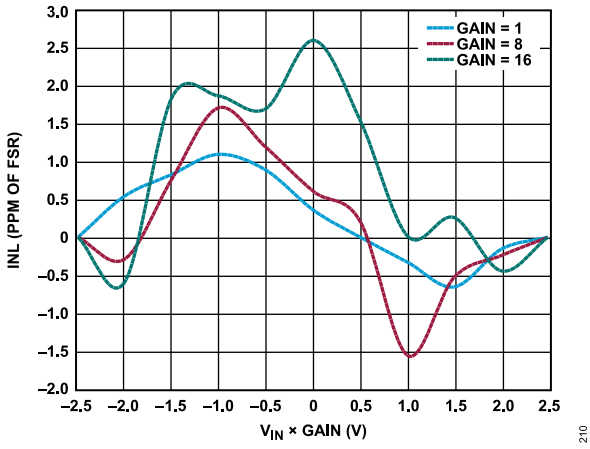

Figure 20. INL vs. Differential Input Signal (Analog Input × Gain) at 125°C

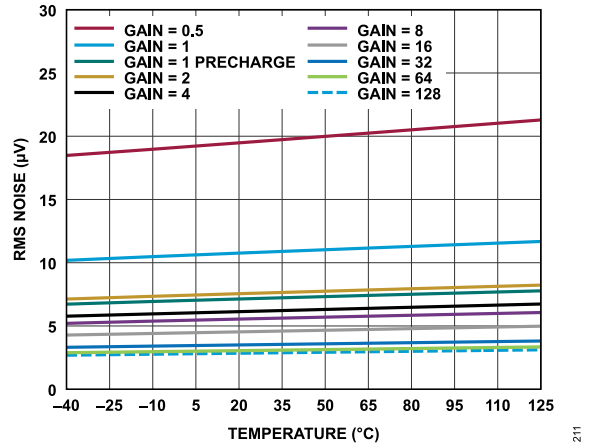

Figure 21. Input Referred RMS Noise vs. Temperature (Internal Reference, Sinc^5 + Avg Filter, 62.5kSPS)

TYPICAL PERFORMANCE CHARACTERISTICS

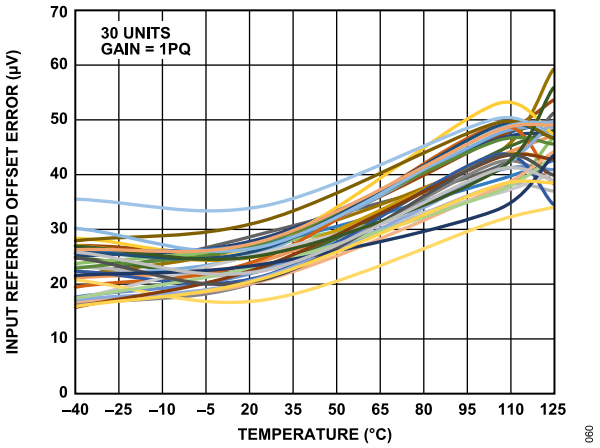

Figure 22. Input Referred Offset vs. Temperature (Gain = 1 Precharge)

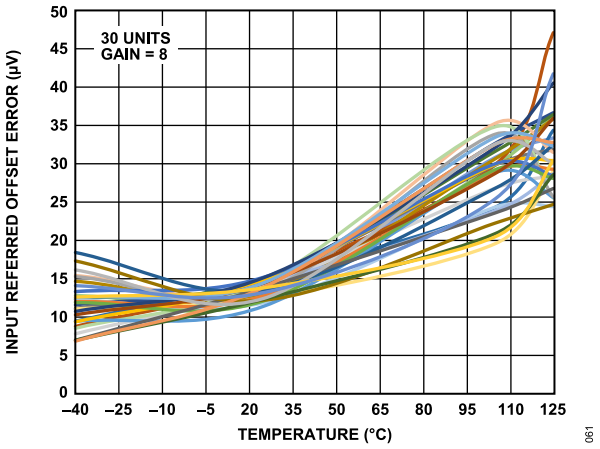

Figure 23. Input Referred Offset vs. Temperature (Gain = 8)

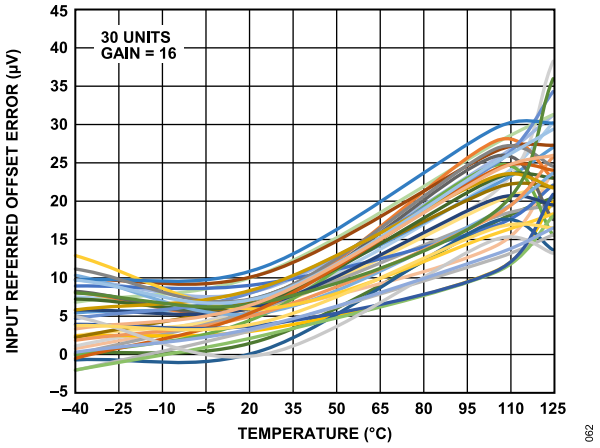

Figure 24. Input Referred Offset vs. Temperature (Gain = 16)

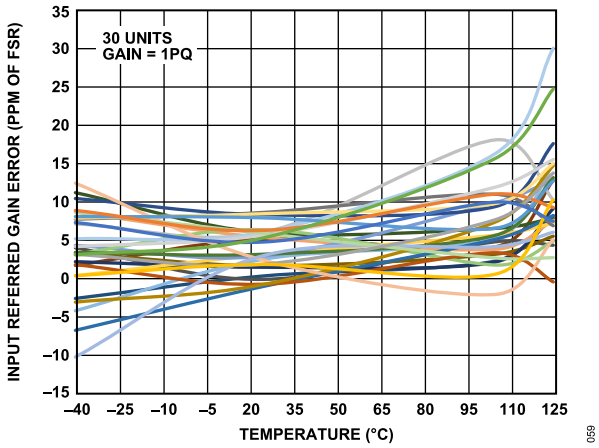

Figure 25. Input Referred Gain Error vs. Temperature (Gain = 1 Precharge)

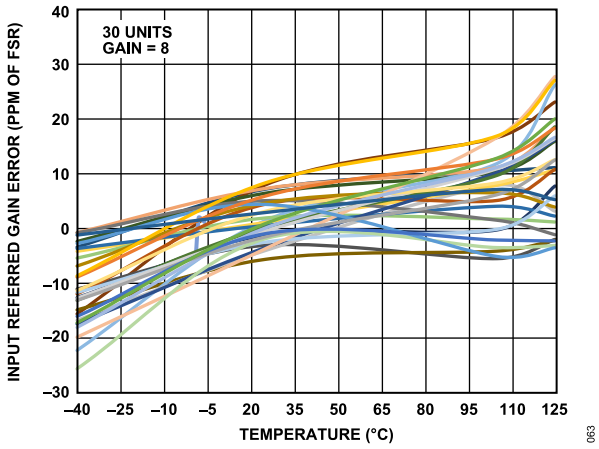

Figure 26. Input Referred Gain Error vs. Temperature (Gain = 8)

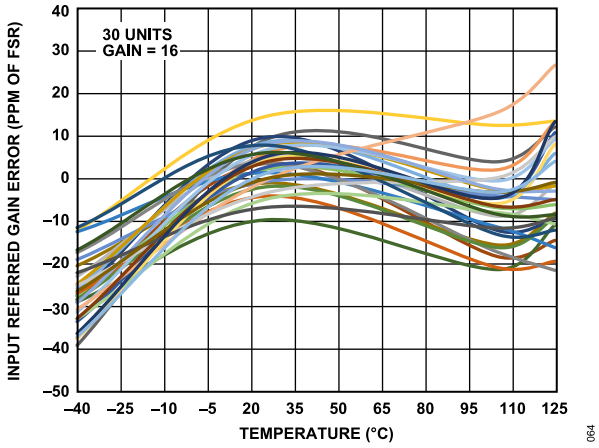

Figure 27. Input Referred Gain Error vs. Temperature (Gain = 16)

TYPICAL PERFORMANCE CHARACTERISTICS

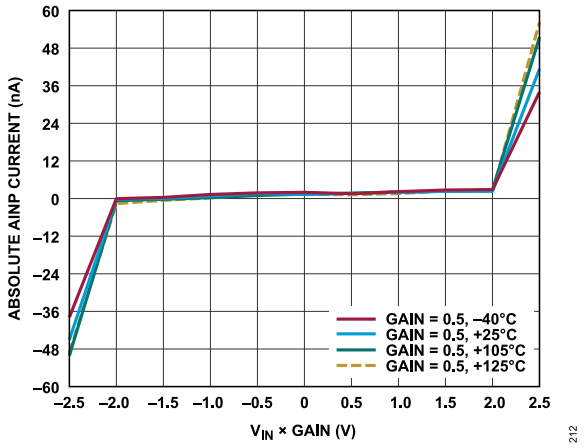

Figure 28. Absolute AINP Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain = 0.5)

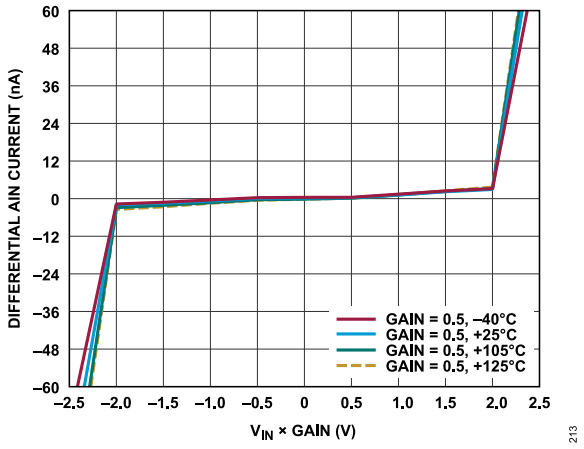

Figure 29. Differential AIN Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain = 0.5)

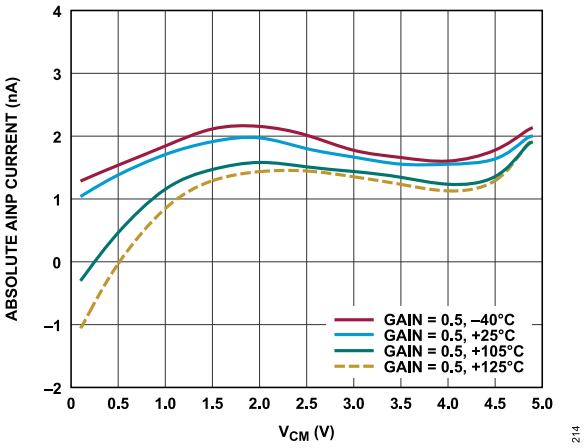

Figure 30. Absolute AINP Current vs. V_{CM} (V_{IN} = 0, Gain = 0.5)

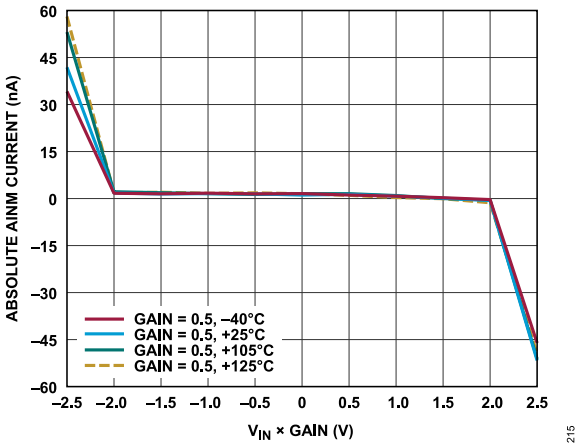

Figure 31. Absolute AINM Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain = 0.5)

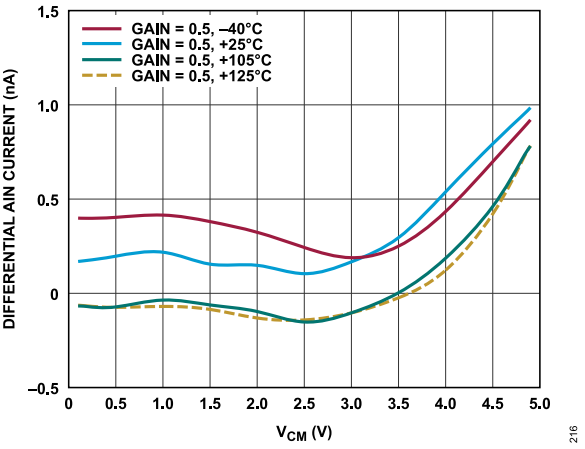

Figure 32. Differential AIN Current vs. V_{CM} (V_{IN} = 0, Gain = 0.5)

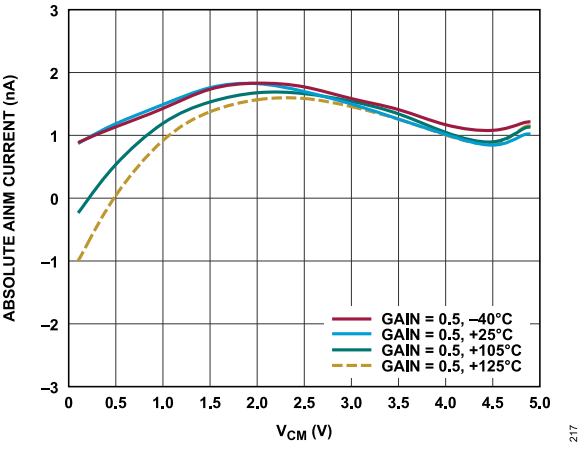

Figure 33. Absolute AINM Current vs. V_{CM} (V_{IN} = 0, Gain = 0.5)

TYPICAL PERFORMANCE CHARACTERISTICS

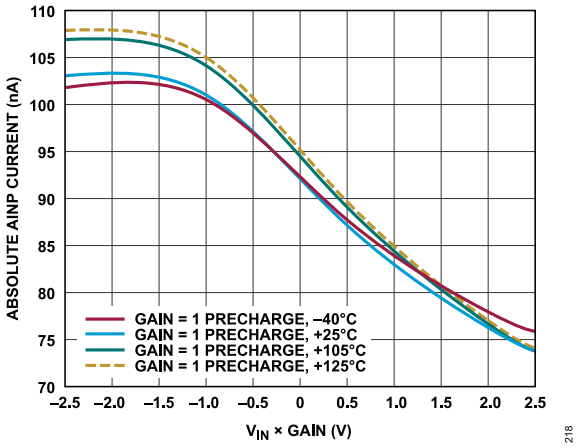

Figure 34. Absolute AINP Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain = 1 Precharge)

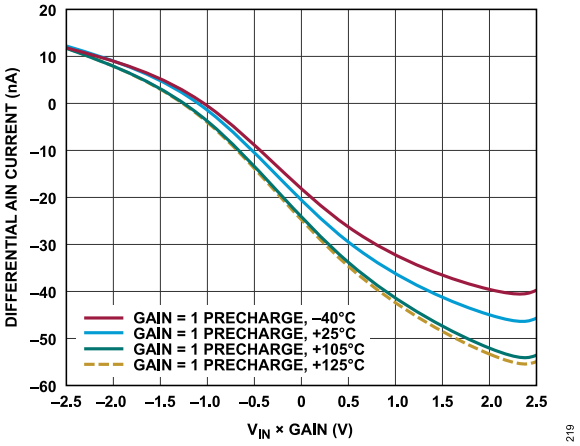

Figure 35. Differential AIN Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain = 1 Precharge)

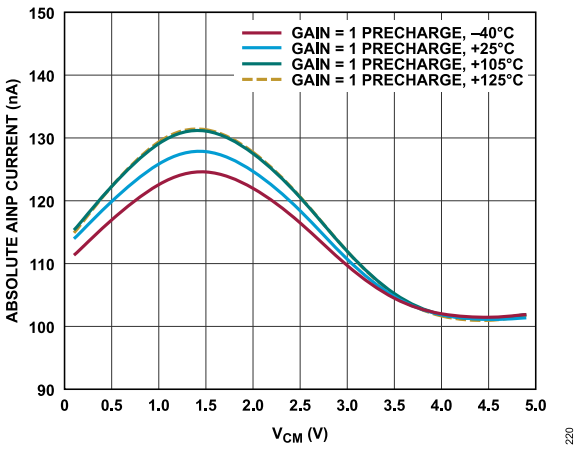

Figure 36. Absolute AINP Current vs. V_{CM} (V_{IN} = 0, Gain = 1 Precharge)

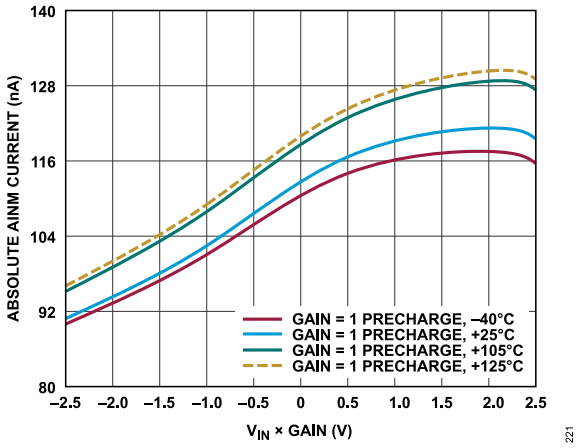

Figure 37. Absolute AINM Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain = 1 Precharge)

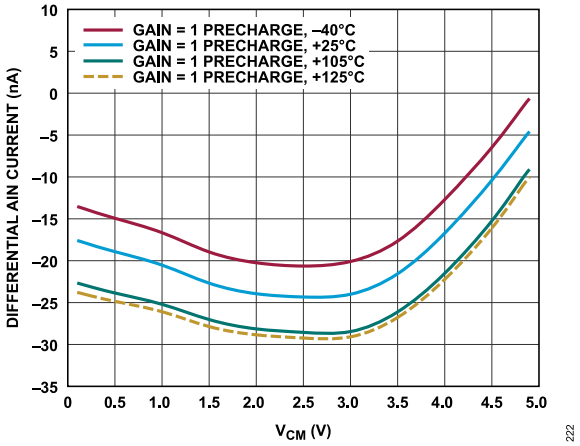

Figure 38. Differential AIN Current vs. V_{CM} (V_{IN} = 0, Gain = 1 Precharge)

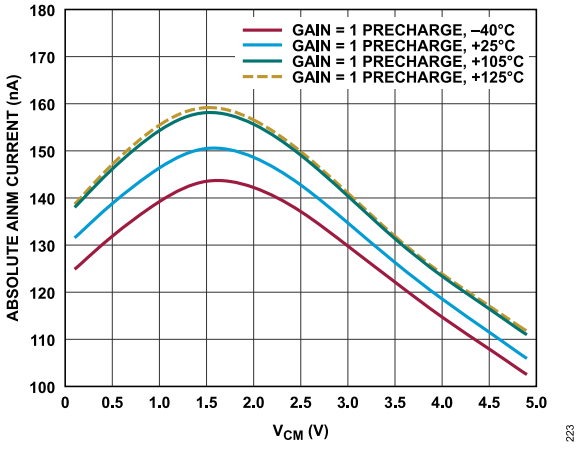

Figure 39. Absolute AINM Current vs. V_{CM} (V_{IN} = 0, Gain = 1 Precharge)

TYPICAL PERFORMANCE CHARACTERISTICS

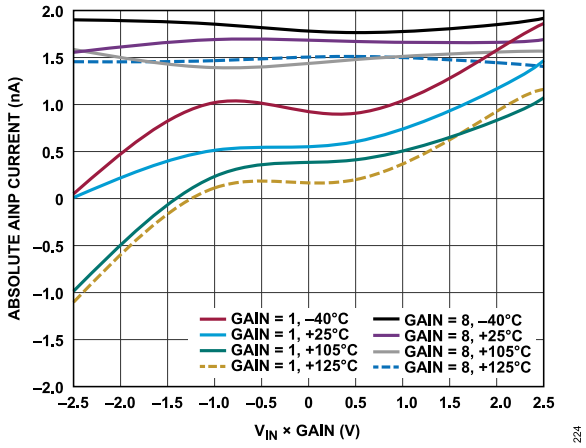

Figure 40. Absolute AINP Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain 1 to Gain 8)

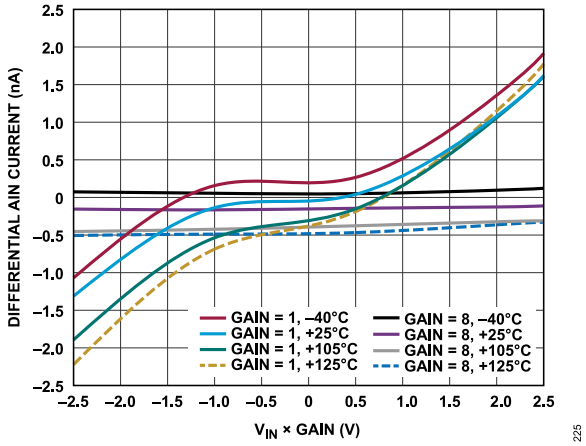

Figure 41. Differential AIN Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain 1 to Gain 8)

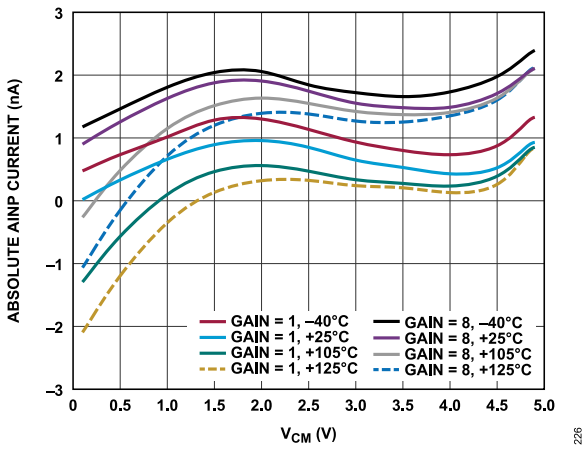

Figure 42. Absolute AINP Current vs. V_{CM} (V_{IN} = 0, Gain 1 to Gain 8)

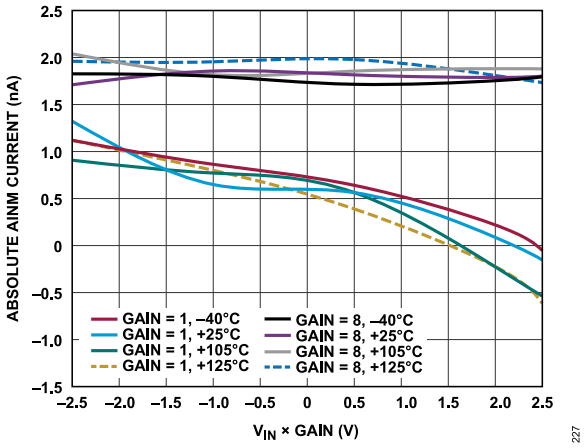

Figure 43. Absolute AINM Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain 1 to Gain 8)

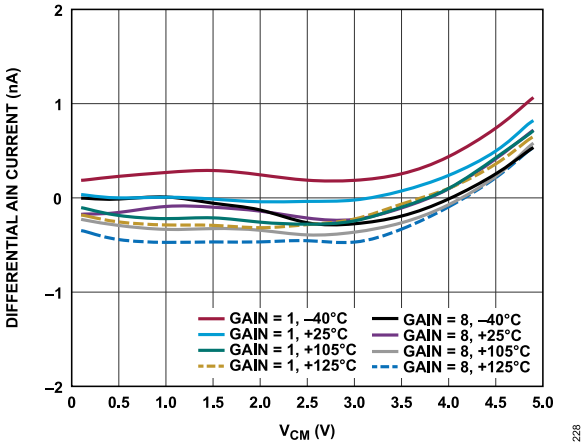

Figure 44. Differential AIN Current vs. V_{CM} (V_{IN} = 0, Gain 1 to Gain 8)

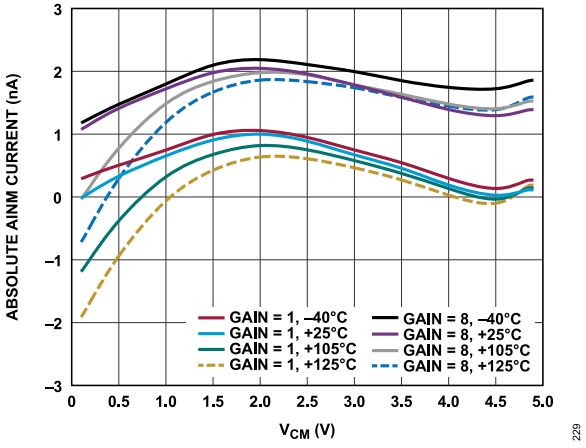

Figure 45. Absolute AINM Current vs. V_{CM} (V_{IN} = 0, Gain 1 to Gain 8)

TYPICAL PERFORMANCE CHARACTERISTICS

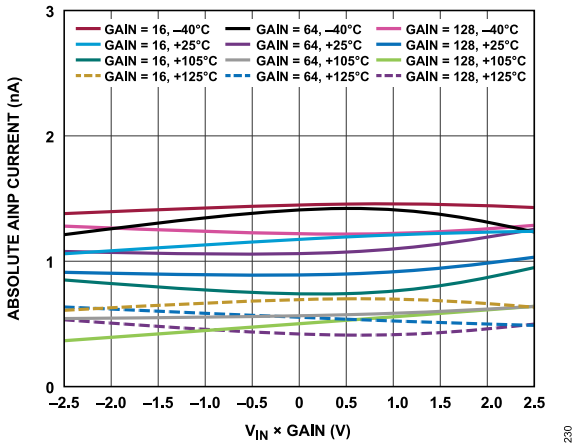

Figure 46. Absolute AINP Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain 16 to Gain 128)

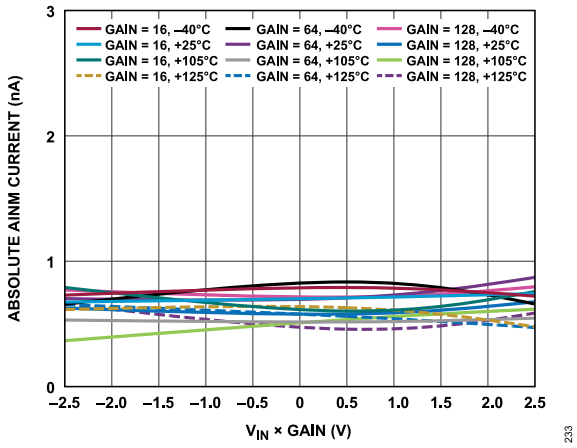

Figure 49. Absolute AINM Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain 16 to Gain 128)

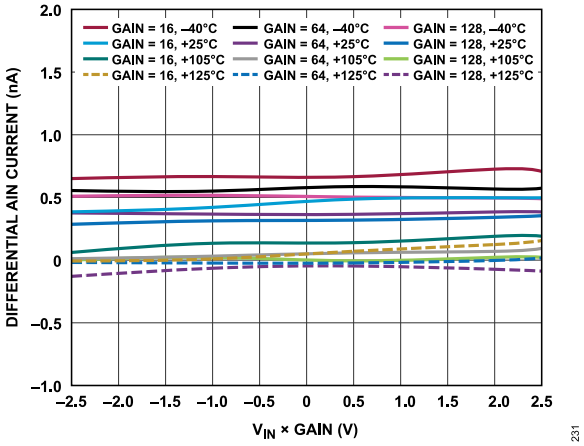

Figure 47. Differential AIN Current vs. V_{IN} (V_{CM} = (AVDD + AVSS)/2, Gain 16 to Gain 128)

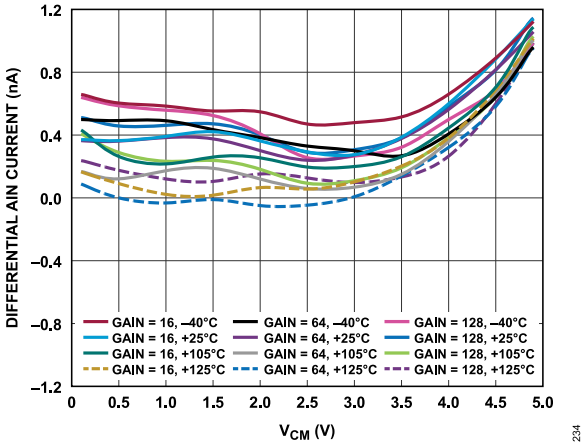

Figure 50. Differential AIN Current vs. V_{CM} (V_{IN} = 0, Gain 16 to Gain 128)

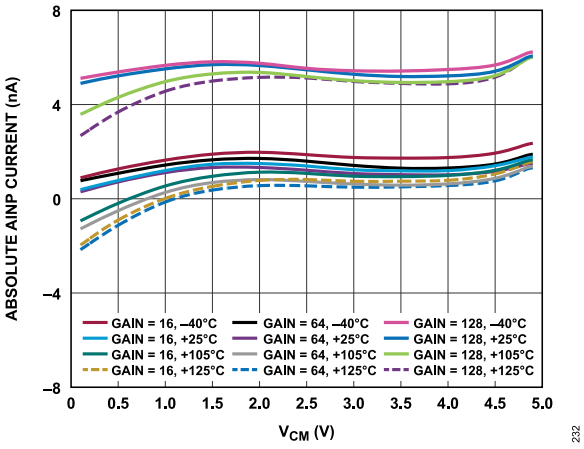

Figure 48. Absolute AINP Current vs. V_{CM} (V_{IN} = 0, Gain 16 to Gain 128)

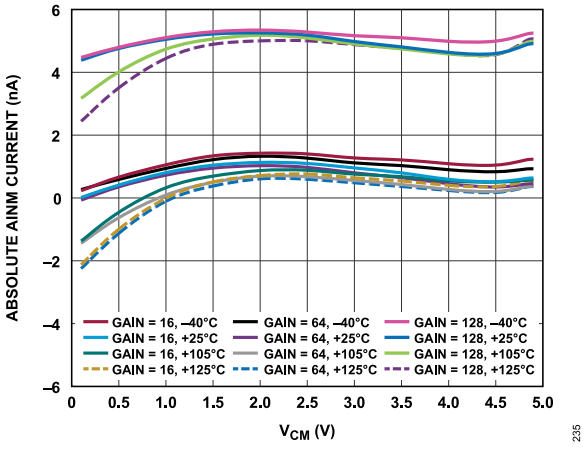

Figure 51. Absolute AINM Current vs. V_{CM} (V_{IN} = 0, Gain 16 to Gain 128)

TYPICAL PERFORMANCE CHARACTERISTICS

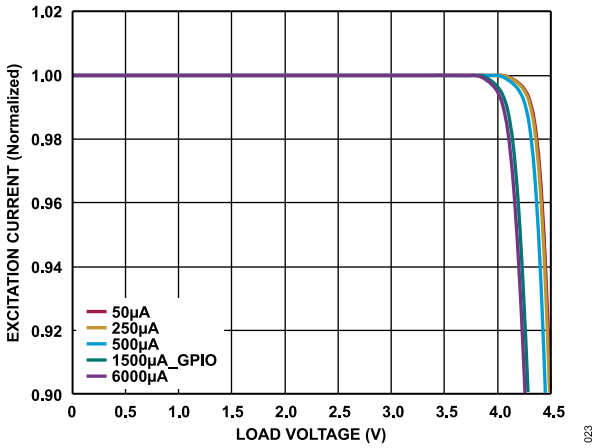

Figure 52. Excitation Current Output Compliance

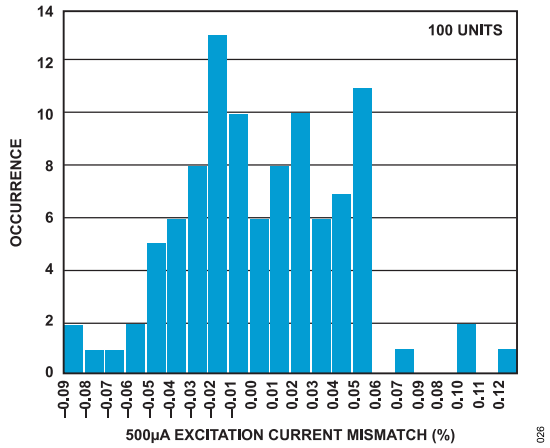

Figure 55. IOUTn Excitation Current Initial Matching (500µA)

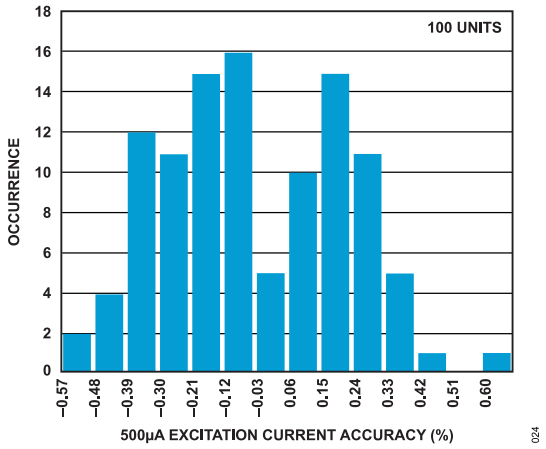

Figure 53. IOUTn Excitation Current Initial Accuracy (500µA)

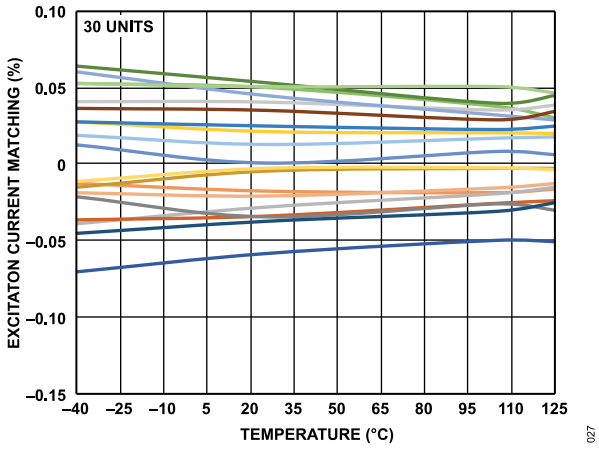

Figure 56. IOUTn Excitation Current Matching vs. Temperature (500µA)

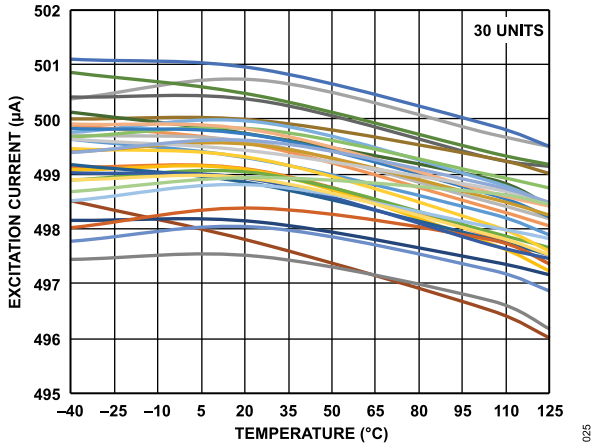

Figure 54. IOUTn Excitation Current vs. Temperature (500µA)

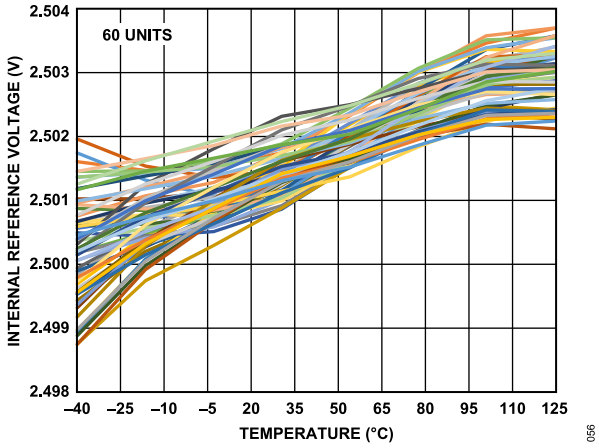

Figure 57. Internal Reference Voltage vs. Temperature (Soldered Devices)

TYPICAL PERFORMANCE CHARACTERISTICS

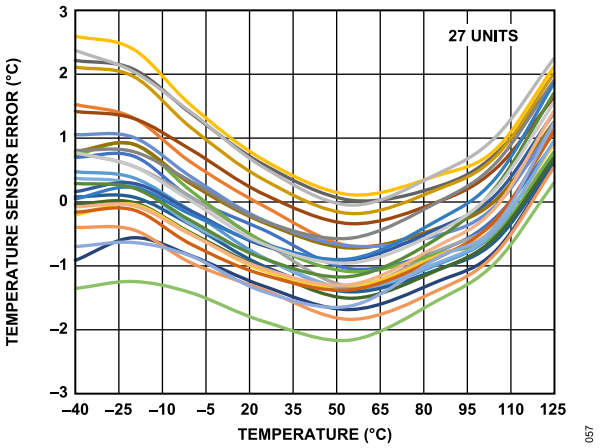

Figure 58. Internal Temperature Sensor Accuracy

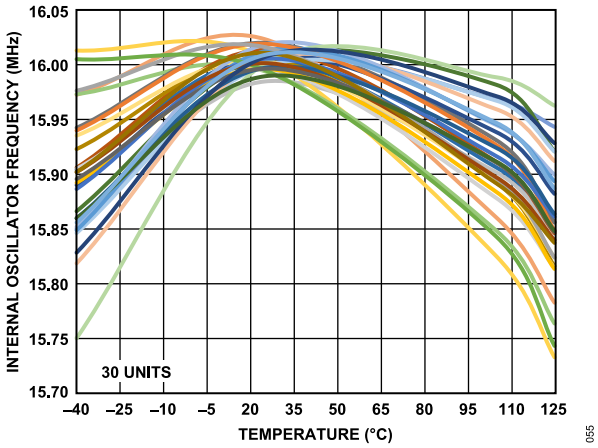

Figure 59. Internal Oscillator vs. Temperature

RMS AND NOISE PERFORMANCE

Table 7 to Table 16 show the RMS noise, peak-to-peak noise, effective resolution, and noise-free (peak-to-peak) resolution of the AD4195-4 for various output data rates, gain settings, and filters. The numbers given are for the bipolar input range with an external 2.5V reference. These numbers are typical and are generated by gathering 1000 samples with a differential input voltage of 0V when the ADC is continuously converting on a single channel. It is important to note that the effective resolution is calculated using the RMS noise, whereas the peak-to-peak resolution (shown in parentheses) is calculated based on peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

Effective Resolution = Log_2 (Input Range/RMS Noise)

Peak-to-Peak Resolution = Log_2 (Input Range/Peak-to-Peak Noise)

$SINC^5$ + AVG

Table 7. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
65,532	3.81	0.21 (1.2)	0.12 (0.60)	0.09 (0.60)	0.07 (0.30)	0.04 (0.22)	0.03 (0.19)	0.03 (0.19)	0.02 (0.12)	0.01 (0.09)	0.01 (0.09)
25,000	10	0.33 (1.8)	0.16 (0.89)	0.17 (0.89)	0.10 (0.60)	0.07 (0.37)	0.05 (0.30)	0.04 (0.26)	0.03 (0.20)	0.02 (0.15)	0.02 (0.13)
20,000	12.5	0.34 (1.8)	0.16 (0.89)	0.19 (0.89)	0.10 (0.60)	0.07 (0.45)	0.06 (0.30)	0.05 (0.28)	0.03 (0.20)	0.03 (0.17)	0.02 (0.17)
10,000	25	0.45 (3)	0.21 (1.5)	0.25 (1.5)	0.14 (1)	0.09 (0.60)	0.08 (0.52)	0.06 (0.37)	0.05 (0.35)	0.04 (0.23)	0.03 (0.19)
5,000	50	0.64 (4.2)	0.28 (1.5)	0.33 (2.1)	0.20 (1.3)	0.13 (0.82)	0.11 (0.71)	0.09 (0.58)	0.07 (0.44)	0.05 (0.31)	0.04 (0.28)
4,160	60.1	0.71 (4.8)	0.31 (1.8)	0.35 (2.1)	0.22 (1.5)	0.15 (0.89)	0.12 (0.75)	0.10 (0.65)	0.07 (0.48)	0.06 (0.36)	0.04 (0.27)
2,000	125	1 (6.6)	0.45 (2.7)	0.52 (3.6)	0.30 (1.8)	0.21 (1.3)	0.17 (1)	0.15 (0.99)	0.10 (0.70)	0.08 (0.51)	0.07 (0.47)
500	500	1.9 (13.1)	0.86 (5.7)	1 (6.3)	0.59 (3.7)	0.41 (2.7)	0.35 (2.3)	0.29 (1.9)	0.21 (1.5)	0.17 (1)	0.14 (0.95)
320	781.25	2.5 (16.7)	1.1 (7.5)	1.3 (7.8)	0.78 (5.5)	0.53 (3.2)	0.45 (2.8)	0.36 (2.4)	0.27 (1.8)	0.20 (1.4)	0.17 (1.1)
160	1,562.5	3.4 (22.6)	1.5 (10.3)	1.8 (11.7)	1.1 (7.3)	0.76 (5.7)	0.63 (4.2)	0.52 (3.2)	0.37 (2.5)	0.30 (1.9)	0.25 (1.7)
100	2,500	4.3 (28.2)	1.9 (12.6)	2.3 (15.6)	1.4 (9.4)	0.98 (6.9)	0.81 (5.2)	0.67 (4.8)	0.49 (3.3)	0.39 (2.6)	0.33 (2.2)
40	6,250	6.8 (42.5)	3 (18.9)	3.6 (23.2)	2.2 (14.6)	1.6 (11)	1.4 (9.3)	1.1 (7.5)	0.82 (5.4)	0.67 (4.4)	0.59 (3.5)
20	12,500	9.7 (63.3)	4.1 (25.2)	5.1 (34.7)	3.3 (22.2)	2.4 (16)	2.1 (13.7)	1.7 (10.5)	1.3 (8.6)	1.1 (7.4)	0.94 (6.2)
16	15,625	10.9 (75.2)	4.5 (24.6)	5.8 (38.3)	3.7 (24.5)	2.8 (18.1)	2.5 (16.5)	2 (13.5)	1.5 (10.4)	1.3 (8.7)	1.1 (7.6)
12	20833.3	12.6 (88.5)	5.1 (34.4)	6.8 (44.1)	4.4 (29.5)	3.4 (22.9)	3 (16.5)	2.4 (15.9)	1.8 (11.3)	1.6 (11)	1.4 (9.3)
8	31,250	15.4 (103.9)	6 (40.4)	8.4 (52.4)	5.6 (33.4)	4.5 (30.9)	3.9 (25.2)	3.2 (21.2)	2.5 (16.9)	2.1 (13.8)	2 (13.3)
4	62,500	19.4 (121.7)	7.1 (47.9)	10.8 (72.3)	7.6 (50)	6.1 (43.4)	5.6 (34.9)	4.5 (30.6)	3.5 (23.1)	3.1 (20.8)	2.9 (20.4)

Table 8. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
65,532	3.81	24.0 (23.0)	24.0 (23.0)	24.0 (23.0)	24.0 (23.0)	24.0 (22.4)	24.0 (21.7)	23.5 (20.7)	23.0 (20.3)	22.4 (19.8)	21.7 (18.8)
25,000	10	24.0 (22.4)	24.0 (22.4)	24.0 (22.4)	24.0 (22.0)	24.0 (21.7)	23.5 (21.0)	22.8 (20.2)	22.4 (19.6)	21.7 (19.0)	20.9 (18.2)
20,000	12.5	24.0 (22.4)	24.0 (22.4)	24.0 (22.4)	24.0 (22.0)	24.0 (21.4)	23.4 (21.0)	22.7 (20.1)	22.2 (19.6)	21.5 (18.8)	20.8 (17.8)
10,000	25	24.0 (21.7)	24.0 (21.7)	24.0 (21.7)	24.0 (21.2)	23.7 (21.0)	23.0 (20.2)	22.2 (19.7)	21.6 (18.8)	21.0 (18.4)	20.3 (17.6)
5,000	50	23.9 (21.2)	24.0 (21.7)	23.8 (21.2)	23.6 (20.8)	23.2 (20.5)	22.4 (19.8)	21.7 (19.0)	21.1 (18.4)	20.5 (18.0)	19.8 (17.1)
4,160	60.1	23.7 (21.0)	23.9 (21.4)	23.7 (21.2)	23.4 (20.7)	23.0 (20.4)	22.3 (19.7)	21.5 (18.9)	21.1 (18.3)	20.4 (17.7)	19.7 (17.1)
2,000	125	23.3 (20.5)	23.4 (20.8)	23.2 (20.4)	23.0 (20.4)	22.5 (19.8)	21.8 (19.2)	21.0 (18.3)	20.5 (17.8)	19.9 (17.2)	19.1 (16.3)
500	500	22.3 (19.5)	22.5 (19.8)	22.2 (19.6)	22.0 (19.4)	21.5 (18.8)	20.8 (18.0)	20.1 (17.3)	19.5 (16.7)	18.8 (16.2)	18.1 (15.3)
320	781.25	21.9 (19.2)	22.2 (19.4)	21.9 (19.3)	21.6 (18.8)	21.2 (18.6)	20.4 (17.8)	19.7 (17.0)	19.2 (16.4)	18.6 (15.8)	17.8 (15.1)
160	1,562.5	21.5 (18.8)	21.7 (18.9)	21.4 (18.7)	21.1 (18.4)	20.6 (17.7)	19.9 (17.2)	19.2 (16.6)	18.7 (15.9)	18.0 (15.3)	17.2 (14.5)
100	2,500	21.1 (18.4)	21.3 (18.6)	21.1 (18.3)	20.8 (18)	20.3 (17.5)	19.6 (16.9)	18.8 (16.0)	18.3 (15.5)	17.6 (14.9)	16.9 (14.1)
40	6,250	20.5 (17.8)	20.7 (18)	20.4 (17.7)	20.1 (17.4)	19.6 (16.8)	18.8 (16)	18.1 (15.3)	17.5 (14.8)	16.8 (14.1)	16.0 (13.4)
20	12,500	20.0 (17.3)	20.2 (17.6)	19.9 (17.1)	19.5 (16.8)	19.0 (16.3)	18.2 (15.5)	17.5 (14.9)	16.9 (14.1)	16.2 (13.4)	15.3 (12.6)
16	15,625	19.8 (17)	20.1 (17.6)	19.7 (17)	19.4 (16.6)	18.8 (16.1)	18.0 (15.2)	17.3 (14.5)	16.7 (13.9)	15.9 (13.1)	15.1 (12.3)
12	20,833.3	19.6 (16.8)	19.9 (17.1)	19.5 (16.9)	19.1 (16.4)	18.5 (15.7)	17.7 (15.2)	17.0 (14.3)	16.4 (13.8)	15.6 (12.8)	14.8 (12)

RMS AND NOISE PERFORMANCE

Table 8. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits) (Continued)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
8	31,250	19.3 (16.6)	19.7 (16.9)	19.2 (16.5)	18.8 (16.2)	18.1 (15.3)	17.3 (14.6)	16.6 (13.8)	16.0 (13.2)	15.2 (12.5)	14.3 (11.5)
4	62,500	19.0 (16.3)	19.4 (16.7)	18.8 (16.1)	18.3 (15.6)	17.6 (14.8)	16.8 (14.1)	16.1 (13.3)	15.4 (12.7)	14.6 (11.9)	13.7 (10.9)

SINC^5

Table 9. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
256	976	1.8 (12.5)	0.76 (5.1)	0.93 (6.2)	0.57 (3.7)	0.39 (2.6)	0.32 (2.2)	0.25 (1.7)	0.20 (1.2)	0.15 (0.99)	0.12 (0.80)
192	1,302	2 (13.5)	0.91 (6.5)	1.1 (7.1)	0.65 (4.1)	0.46 (3.5)	0.38 (2.5)	0.31 (2.1)	0.22 (1.5)	0.17 (1.2)	0.14 (0.91)
128	1,953	2.5 (16.5)	1.1 (7.2)	1.3 (8.5)	0.81 (5.5)	0.55 (3.6)	0.46 (3.2)	0.38 (2.5)	0.27 (1.9)	0.21 (1.4)	0.18 (1.2)
64	3,906	3.6 (23.4)	1.6 (10.7)	1.9 (12.5)	1.1 (7.1)	0.79 (5.5)	0.65 (4.3)	0.53 (3.6)	0.38 (2.5)	0.30 (2.1)	0.25 (1.7)
32	7,812.5	5.1 (33.9)	2.2 (14.4)	2.7 (18.2)	1.6 (11.1)	1.1 (7.2)	0.93 (6.3)	0.77 (5.1)	0.55 (3.7)	0.43 (2.6)	0.37 (2.5)
16	15,625	7.4 (49.0)	3.2 (21.6)	3.9 (25.9)	2.4 (15.4)	1.7 (11.2)	1.4 (9.8)	1.2 (7.1)	0.84 (5.5)	0.69 (4.6)	0.59 (4.1)
8	31,250	11.2 (73.2)	4.6 (30.1)	6.0 (40)	3.8 (25.9)	2.8 (20.2)	2.5 (17.3)	2 (13.7)	1.5 (10.6)	1.3 (8.6)	1.2 (8)
4	62,500	19.4 (127)	7.1 (45.8)	10.9 (70.8)	7.6 (51)	6.2 (40.7)	5.6 (33.2)	4.5 (30)	3.5 (24)	3 (20.7)	2.9 (20.4)

Table 10. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
256	976	22.4 (19.6)	22.6 (19.9)	22.4 (19.6)	22.1 (19.4)	21.6 (18.9)	20.9 (18.1)	20.2 (17.5)	19.6 (17.0)	19.0 (16.3)	18.3 (15.6)
192	1,302	22.2 (19.5)	22.4 (19.6)	22.1 (19.4)	21.9 (19.2)	21.4 (18.4)	20.7 (17.9)	20.0 (17.2)	19.4 (16.7)	18.8 (16)	18.1 (15.4)
128	1,953	21.9 (19.2)	22.1 (19.4)	21.8 (19.2)	21.6 (18.8)	21.1 (18.4)	20.4 (17.6)	19.7 (16.9)	19.1 (16.3)	18.5 (15.8)	17.8 (15)
64	3,906	21.4 (18.7)	21.6 (18.8)	21.3 (18.6)	21.1 (18.4)	20.6 (17.8)	19.9 (17.1)	19.2 (16.4)	18.7 (15.9)	18.0 (15.2)	17.3 (14.5)
32	7,812.5	20.9 (18.2)	21.1 (18.4)	20.8 (18.1)	20.6 (17.8)	20.1 (17.4)	19.4 (16.6)	18.6 (15.9)	18.1 (15.4)	17.5 (14.9)	16.7 (13.9)
16	15,625	20.4 (17.6)	20.6 (17.8)	20.3 (17.6)	20.0 (17.3)	19.5 (16.8)	18.8 (16)	18.0 (15.4)	17.5 (14.8)	16.8 (14.1)	16.0 (13.2)
8	31,250	19.8 (17.1)	20.0 (17.3)	19.7 (16.9)	19.3 (16.6)	18.7 (15.9)	17.9 (15.1)	17.2 (14.5)	16.6 (13.8)	15.9 (13.1)	15.0 (12.3)
4	62,500	19.0 (16.3)	19.4 (16.7)	18.8 (16.1)	18.3 (15.6)	17.6 (14.9)	16.8 (14.2)	16.1 (13.3)	15.4 (12.7)	14.7 (11.9)	13.7 (10.9)

SINC^3

Table 11. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
65,532	3.81	0.21 (1.2)	0.12 (1.2)	0.12 (1.2)	0.07 (0.60)	0.03 (0.30)	0.03 (0.20)	0.02 (0.15)	0.01 (0.09)	0.01 (0.07)	0.01 (0.05)
25,000	10	0.28 (1.2)	0.15 (1.2)	0.14 (1.2)	0.07 (0.60)	0.05 (0.3)	0.04 (0.20)	0.03 (0.19)	0.02 (0.13)	0.02 (0.13)	0.01 (0.12)
20,000	12.5	0.29 (1.2)	0.11 (1.2)	0.14 (1.2)	0.09 (0.60)	0.05 (0.37)	0.04 (0.27)	0.03 (0.24)	0.02 (0.15)	0.02 (0.12)	0.02 (0.10)
10,000	25	0.37 (1.8)	0.17 (1.2)	0.19 (1.2)	0.11 (0.89)	0.07 (0.45)	0.06 (0.40)	0.05 (0.28)	0.03 (0.23)	0.03 (0.19)	0.02 (0.15)
5,000	50	0.49 (3)	0.22 (1.2)	0.25 (1.2)	0.15 (0.89)	0.10 (0.60)	0.08 (0.48)	0.07 (0.45)	0.05 (0.30)	0.04 (0.26)	0.03 (0.20)
4,160	60.1	0.55 (3.6)	0.25 (1.2)	0.28 (1.8)	0.16 (1.1)	0.11 (0.75)	0.09 (0.60)	0.07 (0.47)	0.05 (0.36)	0.04 (0.27)	0.03 (0.23)
2,000	125	0.72 (4.8)	0.32 (2.1)	0.39 (2.6)	0.24 (1.3)	0.16 (0.89)	0.13 (0.89)	0.11 (0.61)	0.08 (0.48)	0.06 (0.39)	0.05 (0.33)
500	500	1.4 (9.3)	0.64 (4.2)	0.78 (5.1)	0.47 (2.7)	0.31 (2)	0.27 (1.8)	0.22 (1.3)	0.15 (1.1)	0.13 (0.70)	0.10 (0.60)
320	781.25	1.8 (11.1)	0.78 (5.1)	0.93 (6)	0.56 (3.4)	0.40 (2.8)	0.32 (2.1)	0.28 (1.8)	0.19 (1.1)	0.15 (1.1)	0.13 (0.85)
160	1,562.5	2.6 (17.7)	1.1 (7.6)	1.3 (8.4)	0.80 (5.5)	0.56 (3.7)	0.46 (3.1)	0.39 (2.6)	0.27 (1.8)	0.22 (1.5)	0.18 (1.2)
100	2,500	3.2 (21.4)	1.4 (9.3)	1.7 (11.7)	1 (6.2)	0.71 (4.7)	0.59 (3.9)	0.48 (3.2)	0.34 (2.3)	0.27 (1.8)	0.23 (1.6)
40	6,250	5.2 (34.3)	2.3 (15.2)	2.7 (17.9)	1.6 (10.5)	1.2 (8)	0.94 (6.7)	0.78 (5.2)	0.56 (3.4)	0.44 (2.9)	0.37 (2.5)

RMS AND NOISE PERFORMANCE

Table 11. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV) (Continued)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
20	12,500	7.5 (51.4)	3.3 (21.1)	3.9 (25.6)	2.4 (15.8)	1.7 (11.2)	1.4 (9.9)	1.2 (7.9)	0.86 (5.7)	0.70 (4.8)	0.60 (4.1)
16	15,625	8.4 (56.8)	3.6 (23.2)	4.5 (29.9)	2.8 (18.9)	2 (13.3)	1.7 (11.2)	1.4 (9.3)	1 (6.1)	0.84 (5.4)	0.72 (4.8)
12	20,833.3	10.2 (68.1)	4.2 (27.2)	5.4 (35.9)	3.4 (22.1)	2.5 (16.7)	2.2 (14.5)	1.8 (11.3)	1.3 (8.8)	1.1 (7.1)	0.98 (6.6)
8	31,250	13.7 (91)	5.5 (36.7)	7.5 (51.7)	4.8 (30.5)	3.7 (24.9)	3.3 (21.8)	2.7 (17.8)	2 (13.1)	1.7 (11)	1.6 (10.5)
4	62,500	39.5 (258)	17.6 (120)	20.7 (138)	12.9 (85.2)	9.5 (62.3)	8.1 (52.3)	6.5 (45.3)	5 (31.3)	4.4 (30.7)	4.1 (27.7)

Table 12. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
65,532	3.81	24.0 (23.0)	24.0 (22.0)	24.0 (22.0)	24.0 (22.0)	24.0 (22.0)	24.0 (21.6)	24.0 (21.0)	23.5 (20.7)	22.8 (20.1)	22.0 (19.5)
25,000	10	24.0 (23.0)	24.0 (22.0)	24.0 (22.0)	24.0 (22.0)	24.0 (22.0)	23.9 (21.6)	23.3 (20.7)	22.7 (20.2)	22.1 (19.2)	21.3 (18.3)
20,000	12.5	24.0 (23.0)	24.0 (22.0)	24.0 (22.0)	24.0 (22.0)	24.0 (21.7)	23.8 (21.1)	23.1 (20.3)	22.6 (20.0)	21.9 (19.4)	21.2 (18.5)
10,000	25	24.0 (22.4)	24.0 (22)	24.0 (22.0)	24.0 (21.4)	24.0 (21.4)	23.3 (20.6)	22.7 (20.1)	22.2 (19.4)	21.5 (18.7)	20.8 (18)
5,000	50	24.0 (21.7)	24.0 (22.0)	24.0 (22.0)	24.0 (21.4)	23.6 (21.0)	22.9 (20.3)	22.1 (19.4)	21.6 (19)	21.0 (18.2)	20.3 (17.6)
4,160	60.1	24.0 (21.4)	24.0 (22.0)	24.0 (21.4)	23.9 (21.1)	23.5 (20.7)	22.7 (20.0)	22.0 (19.4)	21.5 (18.7)	20.8 (18.1)	20.1 (17.4)
2,000	125	23.7 (21.0)	23.9 (21.2)	23.6 (20.9)	23.3 (20.8)	22.9 (20.4)	22.2 (19.4)	21.5 (19.0)	20.9 (18.3)	20.3 (17.6)	19.6 (16.9)
500	500	22.8 (20)	22.9 (20.2)	22.6 (19.9)	22.3 (19.8)	21.9 (19.2)	21.1 (18.4)	20.5 (17.9)	20.0 (17.2)	19.3 (16.8)	18.6 (16.0)
320	781.25	22.4 (19.8)	22.6 (19.9)	22.4 (19.7)	22.1 (19.5)	21.6 (18.8)	20.9 (18.2)	20.1 (17.4)	19.6 (17.1)	19.0 (16.2)	18.3 (15.5)
160	1562.5	21.9 (19.1)	22.1 (19.3)	21.8 (19.2)	21.6 (18.8)	21.1 (18.4)	20.4 (17.6)	19.6 (16.9)	19.1 (16.4)	18.5 (15.7)	17.7 (15)
100	2,500	21.6 (18.8)	21.7 (19)	21.5 (18.7)	21.2 (18.6)	20.8 (18)	20.0 (17.3)	19.3 (16.6)	18.8 (16.1)	18.1 (15.4)	17.4 (14.6)
40	6,250	20.9 (18.2)	21.1 (18.3)	20.8 (18.1)	20.5 (17.9)	20.1 (17.3)	19.3 (16.5)	18.6 (15.9)	18.1 (15.5)	17.4 (14.7)	16.7 (13.9)
20	12,500	20.3 (17.6)	20.5 (17.6)	20.3 (17.6)	20.0 (17.3)	19.5 (16.8)	18.7 (15.9)	18.0 (15.3)	17.5 (14.7)	16.8 (14)	16.0 (13.2)
16	15,625	20.2 (17.4)	20.4 (17.7)	20.1 (17.4)	19.8 (17)	19.2 (16.5)	18.5 (15.8)	17.8 (15)	17.2 (14.6)	16.5 (13.8)	15.7 (13)
12	20,833.3	19.9 (17.2)	20.2 (17.5)	19.8 (17.1)	19.5 (16.8)	18.9 (16.2)	18.1 (15.4)	17.4 (14.8)	16.9 (14.1)	16.1 (13.4)	15.3 (12.5)
8	31,250	19.5 (16.7)	19.8 (17.1)	19.4 (16.6)	19.0 (16.3)	18.4 (15.6)	17.5 (14.8)	16.8 (14.1)	16.2 (13.5)	15.5 (12.8)	14.6 (11.9)
4	62,500	18.0 (15.2)	18.1 (15.3)	17.9 (15.1)	17.6 (14.8)	17.0 (14.3)	16.2 (13.5)	15.6 (12.8)	14.9 (12.3)	14.1 (11.3)	13.2 (10.5)

POST FILTERS

Table 13. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Sinc^5 + Avg Filter, FILTER_FS = 208

Settling Time (ms)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
40	25	0.51 (3)	0.23 (1.5)	0.29 (1.8)	0.16 (0.89)	0.12 (0.67)	0.09 (0.52)	0.07 (0.54)	0.05 (0.33)	0.04 (0.25)	0.03 (0.21)
50	20	0.49 (3)	0.22 (1.5)	0.24 (1.5)	0.16 (0.89)	0.10 (0.67)	0.08 (0.52)	0.07 (0.47)	0.05 (0.30)	0.04 (0.24)	0.03 (0.21)
60	16.7	0.49 (28.9)	0.21 (1.5)	0.24 (1.5)	0.15 (0.89)	0.10 (0.67)	0.08 (0.52)	0.07 (0.43)	0.05 (0.32)	0.04 (0.22)	0.03 (0.22)

Table 14. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Sinc^5 + Avg Filter, FILTER_FS = 208

Settling Time (ms)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
40	25	24.0 (21.7)	24.0 (21.7)	24.0 (21.4)	23.9 (21.4)	23.4 (20.8)	22.8 (20.2)	22.0 (19.1)	21.6 (18.9)	20.9 (18.2)	20.2 (17.5)
50	20	24.0 (21.7)	24.0 (21.7)	24.0 (21.7)	23.9 (21.4)	23.5 (20.8)	22.9 (20.2)	22.1 (19.4)	21.6 (19.0)	20.9 (18.3)	20.1 (17.5)
60	16.7	24.0 (21.7)	24.0 (21.7)	24.0 (21.7)	24.0 (21.4)	23.6 (20.8)	22.9 (20.2)	22.2 (19.5)	21.6 (18.9)	21.0 (18.4)	20.3 (17.4)

RMS AND NOISE PERFORMANCE

Average by 16 Post Filter

Table 15. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (µV), Sinc^5 + Avg Filter

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2000	7.81	0.33 (1.8)	0.22 (0.89)	0.21 (1.2)	0.18 (1.1)	0.18 (0.9)	0.18 (0.8)	0.11 (0.7)	0.12 (0.55)	0.12 (0.42)	0.10 (0.36)
500	31.25	0.53 (3)	0.28 (1.5)	0.31 (2.1)	0.23 (1.2)	0.19 (1)	0.19 (0.97)	0.13 (0.8)	0.13 (0.56)	0.12 (0.56)	0.11 (0.44)
320	48.83	0.63 (3.6)	0.32 (1.8)	0.35 (2.1)	0.25 (1.3)	0.21 (1)	0.20 (1)	0.14 (0.8)	0.13 (0.62)	0.13 (0.59)	0.11 (0.54)
160	97.66	0.87 (5.8)	0.42 (2.8)	0.48 (3.2)	0.31 (2.1)	0.25 (1.7)	0.23 (1.4)	0.16 (1.1)	0.15 (0.96)	0.14 (0.85)	0.12 (0.70)
100	156.25	1.1 (7.3)	0.51 (3.4)	0.59 (3.5)	0.37 (2.5)	0.29 (2.1)	0.26 (1.9)	0.19 (1.3)	0.16 (1.1)	0.15 (0.95)	0.13 (0.79)
40	390.63	1.7 (11.7)	0.77 (5)	0.91 (6.1)	0.56 (3.8)	0.41 (2.7)	0.35 (2.4)	0.28 (1.9)	0.21 (1.5)	0.19 (1.3)	0.16 (1.1)
20	781.25	2.4 (15.9)	1.1 (7.3)	1.3 (9.1)	0.77 (5.1)	0.55 (3.2)	0.46 (3.1)	0.38 (2.5)	0.28 (1.9)	0.23 (1.6)	0.20 (1.3)
16	976.56	2.7 (17.9)	1.2 (7.9)	1.4 (10)	0.86 (5.9)	0.61 (4.1)	0.51 (3.5)	0.41 (2.7)	0.31 (2.1)	0.25 (1.7)	0.22 (1.5)
12	1302.08	3.1 (20.3)	1.4 (9.2)	1.6 (10.7)	1.00 (6.5)	0.71 (4.7)	0.59 (4)	0.48 (3.3)	0.35 (2.3)	0.29 (2)	0.24 (1.6)
8	1953.13	3.8 (25.6)	1.7 (11)	2 (13.1)	1.22 (8.3)	0.86 (5.7)	0.72 (4.7)	0.59 (4)	0.43 (2.8)	0.35 (2.3)	0.30 (1.9)
4	3906.25	5.7 (34.7)	2.5 (16.5)	3 (20.3)	1.84 (12.6)	1.3 (8.5)	1.11 (7.7)	0.90 (5.9)	0.66 (4.4)	0.54 (3.6)	0.47 (3.1)

Table 16. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Sinc^5 + Avg Filter

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 0.5	Gain = 1PQ	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2000	7.81	24.0 (22.4)	24.0 (22.4)	24.0 (22.0)	23.7 (21.1)	22.8 (20.4)	21.8 (19.6)	21.4 (18.8)	20.4 (18.1)	19.3 (17.5)	18.5 (16.7)
500	31.25	24.0 (21.7)	24.0 (21.7)	23.9 (21.2)	23.4 (21.0)	22.6 (20.2)	21.6 (19.3)	21.2 (18.6)	20.2 (18.1)	19.3 (17.1)	18.5 (16.4)
320	48.83	23.9 (21.4)	23.9 (21.4)	23.8 (21.2)	23.3 (20.8)	22.5 (20.2)	21.6 (19.2)	21.1 (18.6)	20.2 (17.9)	19.2 (17.0)	18.4 (16.1)
160	97.66	23.4 (20.7)	23.5 (20.8)	23.3 (20.6)	22.9 (20.2)	22.3 (19.5)	21.4 (18.8)	20.9 (18.1)	20.0 (17.3)	19.1 (16.5)	18.3 (15.8)
100	156.25	23.1 (20.4)	23.2 (20.5)	23.0 (20.4)	22.7 (19.9)	22.0 (19.2)	21.2 (18.4)	20.6 (17.9)	19.9 (17.1)	19.0 (16.3)	18.2 (15.6)
40	390.63	22.5 (19.7)	22.6 (19.9)	22.4 (19.6)	22.1 (19.3)	21.5 (18.8)	20.8 (18)	20.1 (17.3)	19.5 (16.7)	18.7 (15.9)	17.9 (15.2)
20	781.25	22.0 (19.3)	22.2 (19.4)	21.9 (19.1)	21.6 (18.9)	21.1 (18.6)	20.4 (17.6)	19.7 (16.9)	19.1 (16.3)	18.3 (15.6)	17.6 (15)
16	976.56	21.8 (19.1)	22.0 (19.3)	21.7 (18.9)	21.5 (18.7)	21.0 (18.2)	20.2 (17.4)	19.5 (16.8)	18.9 (16.2)	18.2 (15.5)	17.5 (14.7)
12	1302.08	21.6 (18.9)	21.8 (19.1)	21.6 (18.8)	21.3 (18.6)	20.8 (18)	20.0 (17.3)	19.3 (16.5)	18.8 (16.1)	18.1 (15.3)	17.3 (14.6)
8	1953.13	21.3 (18.6)	21.5 (18.8)	21.2 (18.5)	21.0 (18.2)	20.5 (17.7)	19.7 (17)	19.0 (16.3)	18.5 (15.4)	17.8 (15.1)	17.0 (14.3)
4	3906.25	20.7 (18.1)	20.9 (18.2)	20.7 (17.9)	20.4 (17.6)	19.9 (17.2)	19.1 (16.3)	18.4 (15.7)	17.8 (15.1)	17.1 (14.4)	16.3 (13.6)

THEORY OF OPERATION

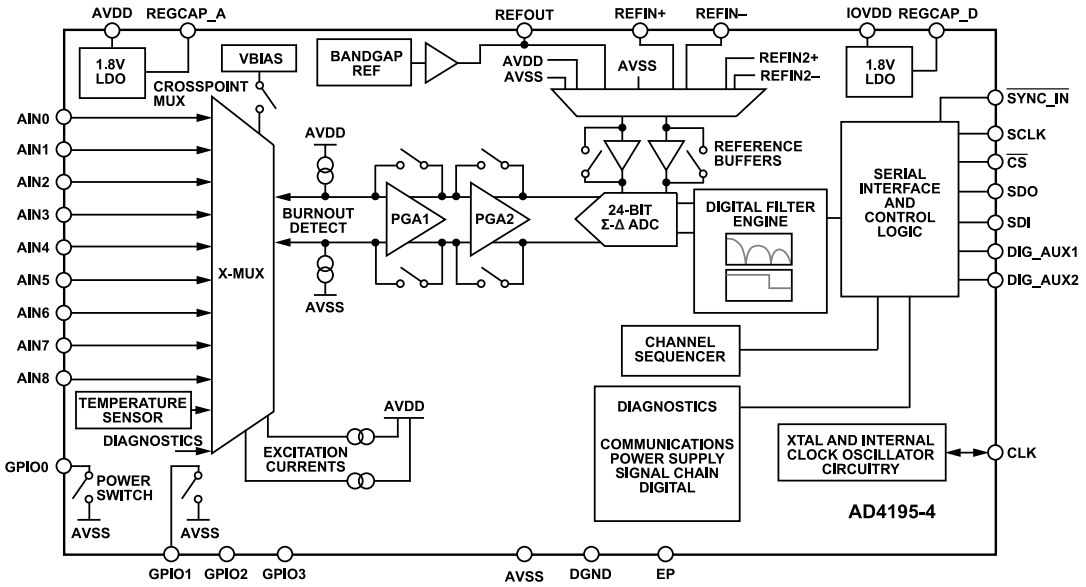

Figure 60. AD4195-4 Basic Connection Diagram

OVERVIEW

The AD4195-4 is a precision ADC that incorporates a Σ-Δ modulator, buffer, reference, gain stage, and on-chip digital filtering, which is intended for the measurement of DC signals. It is a platform solution that can be used in multiple end systems such as pressure, temperature, and weigh scale applications.

Analog Inputs

The device can have four differential analog inputs, eight pseudodifferential analog inputs, or a combination of differential and pseudo-differential analog inputs. The AD4195-4 uses flexible multiplexing. Therefore, any analog input pin can be selected as a positive input (AINP) and/or negative input (AINM).

Multiplexer

The on-chip crosspoint multiplexer offers flexibility in terms of the analog input pairs. Diagnostics such as measuring the analog and digital power supply voltages are selected using the multiplexer.

Reference

The device contains a 2.5V reference, which has a drift of ±5ppm/°C typical.

Reference buffers are also included on chip, which can be used with both internal and externally applied references.

Programmable Gain Amplifier (PGA)

The analog input signal can be amplified or attenuated using the PGA. The PGA allows gains of 0.5, 1, 2, 4, 8, 16, 32, 64, and 128. The gain = 1 precharge setting bypasses the PGA but continues to use the precharge buffer. Using gain = 1 precharge reduces the analog power supply current. However, the absolute and differential input currents increase.

Burnout Currents

Two burnout currents, which can be programmed to ±100nA, ±2µA, or ±10µA, are included on chip to detect the presence of the external sensor.

Σ-Δ ADC and Filter

The AD4195-4 contains a Σ-Δ modulator followed by a digital filter. The device has the following filter options:

- $Sinc^5$
- $Sinc^3$
- $Sinc^5$ + Avg
- Post filter

Channel Sequencer

The AD4195-4 allows up to 16 channels. The multiplexer selections for these channels can consist of analog inputs, reference inputs, or power supplies such that diagnostic functions, for example, power supply monitoring, can be interleaved with conversions. The sequencer automatically converts all enabled channels. The AD4195-4 accommodates performing multiple conversions on a channel when it is selected. The AD4195-4 also supports adding a delay before commencing conversions on the selected channel as front-end circuitry may require some settling time.

Per Channel Configuration

The AD4195-4 allows up to eight different setups, each setup consisting of a PGA gain, ODR, filter type, reference source, ADC/

THEORY OF OPERATION

excitation current chopping, offset register, and gain register. Each channel is then linked to a setup.

Serial Interface

The AD4195-4 has a 4-wire SPI ($\overline{CS}$, SDI, SDO, SCLK). $\overline{CS}$ can be tied low. Therefore, only three pins are required for communication between the ADC and the microprocessor. The on-chip registers are accessed through the serial interface.

Main Clock

The device has an internal 16MHz clock. The clock is divided by 2 internally. Use the internal clock or an external clock as the clock source for the device. The internal clock can also be made available on Pin CLK if a clock source is required for external circuitry.

Temperature Sensor

The on-chip temperature sensor monitors the die temperature.

General-Purpose Inputs/Outputs

The AD4195-4 has four general-purpose inputs/outputs. These can be used for driving external circuitry. For example, an external multiplexer can be controlled by these outputs.

Calibration

Both internal offset calibration, and system offset and full-scale calibration are included on chip. Therefore, the user has the option of removing offset errors internal to the device only, or removing the offset or gain errors of the complete end system. The full-scale error for all gains is factory calibrated. Therefore, no further internal full-scale calibrations are required.

Excitation Currents

The device contains two excitation currents that can be set independently to 10µA, 50µA, 100µA, 250µA, 500µA, 1mA, or 1.5mA. The excitation currents can be added by outputting them on the same pin.

Bias Voltage

A bias voltage generator is included on chip. Therefore, signals from thermocouples can be biased suitably. The bias voltage is set to (AVDD + AVSS)/2 and can be made available on any analog input pin.

Bridge Power-Down Switches (PDSW)

Two low-side power switches allow the user to power down bridges that are interfaced to the ADC.

Diagnostics

The AD4195-4 includes numerous diagnostics such as the following:

- Reference detection
- Overvoltage/Undervoltage detection
- CRC on SPI communications
- CRC on the memory map
- SPI read/write checks

These diagnostics allow a high level of fault coverage in an application.

POWER SUPPLIES

The AD4195-4 operates with an analog power supply voltage from 4.75V to 5.25V. The device accepts a digital power supply from 1.7V to 5.25V.

The device has two independent power supply pins: AVDD and IOVDD:

- AVDD is referred to AVSS. AVDD powers the internal analog regulator that supplies the ADC.
- IOVDD is referred to DGND. This supply sets the interface logic levels on the SPI interface and powers an internal regulator for operation of the digital processing.

Unipolar Analog Supply Operation (AVSS = DGND)

When the AD4195-4 is powered from a unipolar analog supply, AVSS and DGND can be shorted together on one single ground plane. With this setup, an external level shifting circuit is required when using truly bipolar inputs to shift the common-mode voltage. Recommended regulators include the LT1962EMS8-5, which has a low quiescent current.

Bipolar Analog Supply Operation (AVSS ≠ DGND)

The AD4195-4 can operate with AVSS set to a negative voltage, which allows true bipolar inputs to be applied. This allows a truly fully-differential input signal centered around 0V to be applied to the AD4195-4 without the need for an external level shifting circuit. For example, with a 5V split supply, AVDD = +2.5V and AVSS = −2.5V. In this use case, the AD4195-4-internally level shifts the signals, which allows the digital output to function between DGND (nominally 0V) and IOVDD.

The maximum difference allowed between AVSS and IOVDD is 6.35V. Therefore, if AVSS = −2.5V, IOVDD can equal +3.85V or less.

THEORY OF OPERATION

DIGITAL COMMUNICATION

The AD4195-4 has a 4-wire SPI interface ($\overline{CS}$, SDI, SDO, SCLK) that is compatible with QSPI, MICROWIRE, and DSPs. $\overline{CS}$ can be hardwired low, which reduces the SPI connections between the ADC and microprocessor to three. The interface operates in SPI Mode 3. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

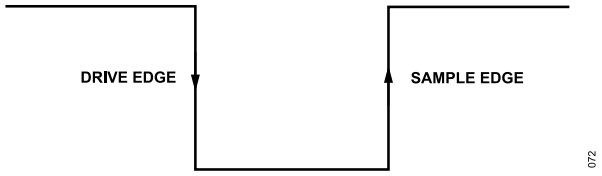

Figure 61. SPI Mode 3, SCLK Edges

For more details, see the Digital Interface section.

CONFIGURATION OVERVIEW

After power on or reset, the AD4195-4 default configuration is as follows:

- Channel: Channel 0 is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. Setup 0 is selected.
- Setup: Reference precharge buffers are enabled, the gain is set to 1, and the internal reference is enabled and selected as the reference source.
- ADC control: The AD4195-4 is in continuous conversion mode, and the internal oscillator is enabled and selected as the main clock source.

Note that only a few of the register setting options are shown, this list is just an example. For full register details, see the On-Chip Register Map section.

A suggested flow for changing the ADC configuration is as follows:

- Channel configuration: Select AINP and AINM for each channel. Select one of the eight allowable setups for each channel.
- Setup: For each setup being used, select the filter type, ODR, gain, reference source, and polarity.
- Diagnostics: Enable SPI CRC, overvoltage/undervoltage checks on AINP and AINM, and reference detect.
- ADC control: Select ADC operating mode and main clock source.

Channel/Sequencer Slot Configuration

The AD4195-4 has 16 channel selections or sequencer slots, and eight independent setups. The user can select any of the analog input pairs on any channel, as well as any of the eight setups for any channel/sequencer slot, which give the user full flexibility in the channel configuration. This also allows per channel configuration when using all four differential inputs or eight pseudodifferential inputs because each channel can have its own dedicated setup.

Along with the analog inputs, signals such as the power supply or reference can also be used as multiplexer inputs. They are routed to the multiplexer internally when selected. This allows diagnostics to be interleaved with conversions.

Channel Registers

Use the CHANNEL_MAPn registers to select the positive analog input or the negative analog input for that channel. Use the CHANNEL_SETUPn registers to assign one of the eight available setups to the channel, to set the number of conversions to be performed on the channel each time it is selected, and also to set the delay required before performing conversions on the channel when it is selected.

Channels are enabled using the CHANNEL_EN register.

When the AD4195-4 is operating with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 15. If a channel is disabled, it is skipped by the sequencer. Channel 0 must always be used when more than one channel is enabled. Details of the channel registers for Channel 0 are shown in Table 17 and Table 18, respectively. The CHANNEL_EN register is shown in Table 19.

Table 17. CHANNEL_SETUP0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x81	CHANNEL_SETUP0	[15:8]	REPEAT_N								0x0000	R/W
0x80		[7:0]	RESERVED	DELAY_N			RESERVED	SETUP_N				

Table 18. CHANNEL_MAP0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x83	CHANNEL_MAP0	[15:8]	RESERVED				AINP_N				0x0001	R/W
0x82		[7:0]	RESERVED				AINM_N					

THEORY OF OPERATION

Table 19. CHANNEL_EN Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x79	CHANNEL_EN	[15:8]	CH_15	CH_14	CH_13	CH_12	CH_11	CH_10	CH_9	CH_8
0x78		[7:0]	CH_7	CH_6	CH_5	CH_4	CH_3	CH_2	CH_1	CH_0

ADC Setups

The AD4195-4 has eight independent setups. Each setup consists of the following six registers:

- Miscellaneous (MISC) register
- Analog front end (AFE) register
- Filter (FILTER) register
- FILTER_FS register
- Offset register (OFFSET)
- Gain register (GAIN)

For example, Setup 0 consists of registers MISC0, AFE0, FILTER0, FILTER_FS0, OFFSET0, and GAIN0. Figure 62 shows the grouping of these registers. The setup is selectable from the CHANNEL_SETUPn registers detailed in the Channel/Sequencer Slot Configuration section. This allows each channel to be assigned to one of eight separate setups. Table 20 to Table 25 show the registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 7.

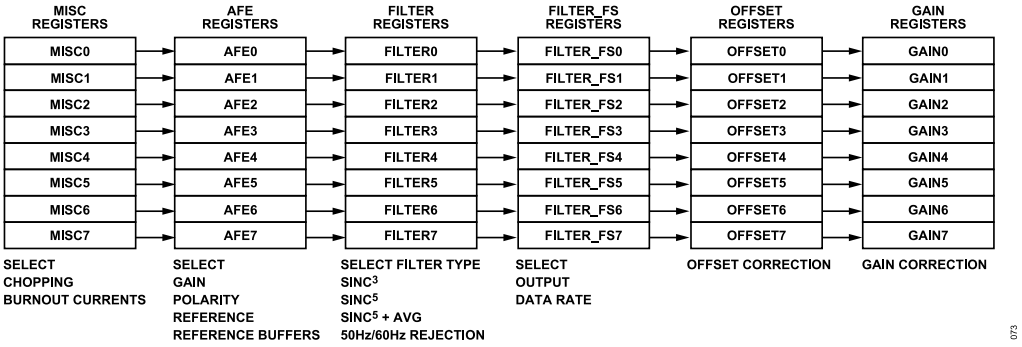

Figure 62. Setup Structure

THEORY OF OPERATION

Miscellaneous (MISC) Registers

The miscellaneous registers allow the user to select multiplexer chopping, excitation current chopping, and enable/disable the burn-out currents. With multiplexer chopping, the analog input pair are continuously swapped and a conversion is generated for each phase. The two conversions are then averaged which minimizes offset and offset drift. Chopping/swapping of the excitation currents removes any mismatch of the excitation currents. This is useful in 3-wire RTDs where well-matched excitation currents are required to minimize any error due to lead resistance.

Analog Front End (AFE) Registers

The AFE registers allow the user to configure the reference buffers, select the reference source, and set the gain and the polarity.

Table 20. MISC0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xC1	MISC0	[15:8]	CHOP_IEXC		RESERVED				CHOP_ADC		0x0000	R/W
0xC0		[7:0]	RESERVED						BURNOUT			

Table 21. AFE0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xC3	AFE0	[15:8]	RESERVED				REF_BUF_M		REF_BUF_P		0x0050	R/W
0xC2		[7:0]	RESERVED	REF_SELECT		BIPOLAR	PGA_GAIN					

Table 22. FILTER0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xC5	FILTER0	[15:8]	RESERVED								0x0000	R/W
0xC4		[7:0]	POST_FILTER_SEL				FILTER_TYPE					

Table 23. FILTER_FS0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xC7	FILTER_FS0	[15:8]	FS[15:8]								0x0004	R/W
0xC6		[7:0]	FS[7:0]									

Table 24. OFFSET0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xCA	OFFSET0	[23:16]	OFFSET[23:16]								0x000000	R/W
0xC9		[15:8]	OFFSET[15:8]									
0xC8		[7:0]	OFFSET[7:0]									

Table 25. GAIN0 Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xCD	GAIN0	[23:16]	GAIN[23:16]								0x555555	R/W
0xCC		[15:8]	GAIN[15:8]									
0xCB		[7:0]	GAIN[7:0]									

THEORY OF OPERATION

Filter Registers

The filter registers select which sinc digital filter is used at the output of the ADC modulator. The filter type is selected by setting the bits in this register. For more details, see the Digital Filter section.

FILTER_FS Registers

The FILTER_FS registers select the ODR. For more details, see the Digital Filter section.

Offset Registers

The offset registers hold the offset calibration coefficient for the ADC. The power-on reset value of an offset register is 0x000000. The offset registers are 24-bit read/write registers. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user or if the offset registers are written to by the user.

Gain Registers

The gain registers are 24-bit registers that hold the gain calibration coefficient for the ADC. The gain registers are read/write registers. The default value is automatically overwritten if a system full-scale calibration is initiated by the user. For more details on calibration, see the Calibration section.

Diagnostics

The ERROR_EN and INTERFACE_CONFIG_C registers enable and disable the numerous diagnostics on the AD4195-4. Diagnostics include the following:

- SPI read and write checks, which ensure that only valid registers are accessed.
- SCLK counter, which ensures that the correct number of SCLK pulses are used.
- SPI CRC.
- Memory map CRC.
- LDO checks.
- Overvoltage/undervoltage detection on the analog inputs and reference inputs.
- Reference detect.

SPI CRC is enabled using the INTERFACE_CONFIG_C while the remaining diagnostics are enabled using the ERROR_EN register. When a diagnostic is enabled, the corresponding flag is contained in the ERROR register. The INTERFACE_STATUS_A register indicates errors that occur on the SPI. By setting Bit SPI_ERR_EN in the ERROR_EN register, any SPI errors set Bit SPI_ERR in the ERROR register. INTERFACE_STATUS_A can then be read to get more details on the error. All enabled flags in the ERROR register are OR'ed to control the MAIN_ERR_S flag in the STATUS register. Therefore, if an error occurs (for example, the SPI CRC check detects an error), the relevant flag (for example, the SPI_ERR flag) in the ERROR register is set. The MAIN_ERR_S flag in the status register is also set. This is useful when the status bits are appended to conversions. The MAIN_ERR_S bit indicates if an error has occurred. For more details on the error source, the user can then read the INTERFACE_STATUS_A and ERROR registers. For more details on the diagnostic registers, see Table 26 to Table 29. For more details on the diagnostics available, see the Diagnostics section.

ADC Control Register

The ADC_CTRL register configures the mode for the digital interface. The mode of operation is also selected, for example, continuous conversion or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes.

The details of this register are shown in Table 30.

Table 26. INTERFACE_CONFIG_C Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x10	INTERFACE_CONFIG_C	[7:0]	CRC_ENABLE		STRICT_REGISTER_ACCESS	SEND_STATUS	ACTIVE_INTERFACE_MODE		CRC_ENABLEB		0x27	R/W

Table 27. INTERFACE_STATUS_A Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x11	INTERFACE_STATUS_A	[7:0]	NOT_READY_ERR	RESERVED		CLOCK_COUNT_ERR	CRC_ERR	WR_TO_RD_ONLY_REG_ERR	REGISTER_PARTIAL_ACCESS_ERR	ADDRESS_INVALID_ERR	0x00	R/W

THEORY OF OPERATION

Table 28. ERROR_EN Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x73	ERROR_EN	[15:8]	RESERVED		DLDO_PSM_ERR_EN	ALDO_PSM_ERR_EN	IOUT3_COMP_ERR_EN	IOUT2_COMP_ERR_EN	IOUT1_COMP_ERR_EN	IOUT0_COMP_ERR_EN	0x0000	R/W
0x72		[7:0]	REF_DIFF_MIN_ERR_EN	REF_OV_UV_ERR_EN	AINM_OV_UV_ERR_EN	AINP_OV_UV_ERR_EN	ADC_CONV_ERR_EN	SPI_ERR_EN	MM_CRC_ERR_EN	ROM_CRC_ERR_EN		

Table 29. ERROR Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x75	ERROR	[15:8]	DEVICE_ERROR	RESERVED	DLDO_PSM_ERR	ALDO_PSM_ERR	IOUT3_COMP_ERR	IOUT2_COMP_ERR	IOUT1_COMP_ERR	IOUT0_COMP_ERR	0x0000	R/W
0x74		[7:0]	REF_DIFF_MIN_ERR	REF_OV_UV_ERR	AINM_OV_UV_ERR	AINP_OV_UV_ERR	ADC_CONV_ERR	SPI_ERR	MM_CRC_ERR	ROM_CRC_ERR		

Table 30. ADC Control Register

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x71	ADC_CTRL	[15:8]	RESERVED								0x0000	R/W
0x70		[7:0]	MULTI_DATA_REG_SEL	CONT_READ_STATUS_EN	CONT_READ		MODE					

THEORY OF OPERATION

Understanding Configuration Flexibility and Sequencer

In Figure 63, Figure 64, and Figure 65, the registers shown in black font are programmed for this configuration. The registers shown in gray font are redundant.

The most straightforward implementation of the AD4195-4 is to use differential inputs with adjacent analog inputs and run all of them with the same setup. For example, the user requires four differential inputs. In this case, the user selects the following differential inputs: AIN1/AIN2, AIN3/AIN4, AIN5/AIN6, and AIN7/AIN8.

Programming the gain and offset registers is optional for any use case. If an internal or system offset, or system full-scale calibration is performed, the gain and offset registers in the setup associated with the selected channel are automatically updated.

An alternative way to implement these four fully-differential inputs is by taking advantage of the eight available setups. Motivation for this includes having a different speed, noise, or gain requirement on some of the four-differential inputs vs. other inputs, or there may be a specific offset or gain correction for particular channels. Figure 64 shows how each of the differential inputs can use a separate setup, which allows full flexibility in the configuration of each channel.

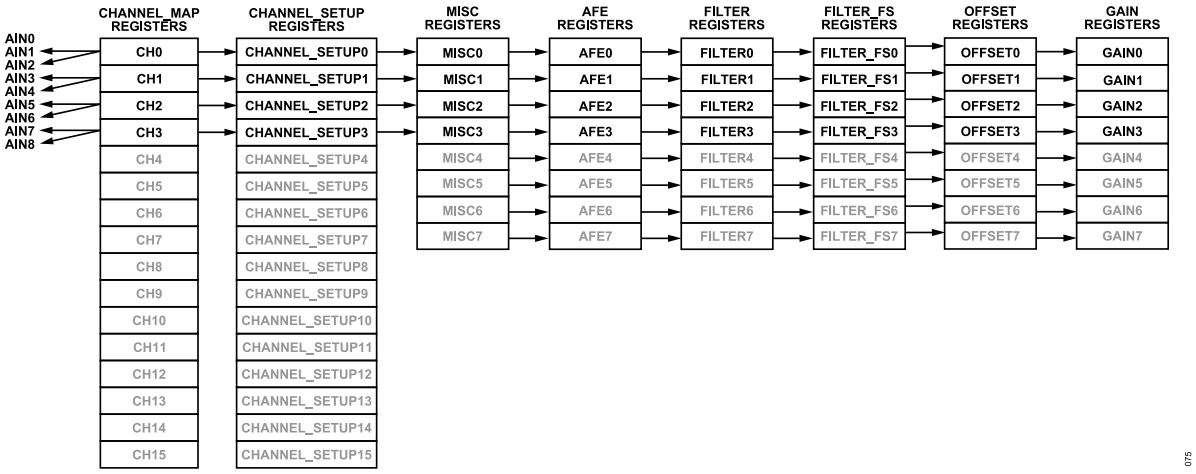

Figure 63. Four Fully-Differential Inputs, All Using a Single Setup (MISC0, AFE0, FILTER0, FILTER_FS0, GAIN0, OFFSET0)

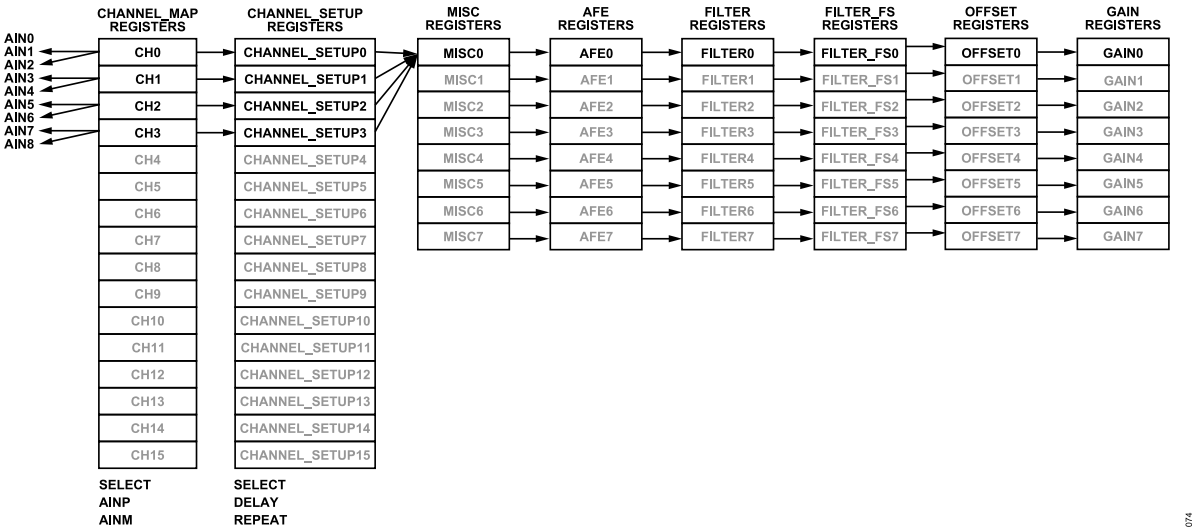

Figure 64. Four Fully-Differential Inputs with a Separate Setup per Channel

Figure 65 shows an example of how the channel registers span between the analog input pins and the setup configurations downstream. In this random example, two differential inputs and two single-ended inputs are required. The single-ended inputs are the AIN2/AIN7 and AIN8/AIN7 combinations. The first differential input pair (AIN1/AIN2) uses Setup 0. The two single-ended input pairs (AIN2/AIN7 and AIN8/AIN7) are set up as diagnostics. Therefore, they use a separate setup (Setup 1). The final differential input (AIN3/AIN4) also uses a separate setup, Setup 2. Given that three setups are selected for use, the MISC, AFE, FILTER, and FILTER_FS registers associated with each setup are programmed as required. Optional gain and offset correction can be employed on

THEORY OF OPERATION

a per setup basis by programming the OFFSET and GAIN registers associated with each setup.

In the example shown in Figure 65, Channel CH0 to Channel CH3 are used.

The channels are enabled through the CHANNEL_EN register. When more than one channel is enabled, Channel 0 must always be used. When the AD4195-4 converts, the sequencer transitions in ascending sequential order from the lowest enabled channel to the highest enabled channel. Any unabled channels are bypassed. When a channel is selected, the DELAY programmed for the channel is timed out. This delay allows the external analog circuitry to settle before the ADC begins sampling the analog input. Eight programmable settings, ranging from 0 to 16384/MOD_CLK, can be set using the DELAY bits in the CHANNEL_SETUPn register. The AD4195-4 then produces conversions, the number of conversions determined by the REPEAT function in the CHANNEL_SETUPn register. REPEAT can have a value from 1 to 255. When the sequence is complete, the AD4195-4 loops back to the beginning of the sequencer if continuous conversion mode is selected. In single conversion mode, the AD4195-4 enters standby mode when the sequence is complete.

Note that the REPEAT function can only be used when all channels share a DATA register (Bit MULTI_DATA_REG_SEL in the ADC_CTRL register is set to 1). When Bit MULTI_DATA_REG_SEL in the ADC_CTRL register is set to 0, each enabled channel has its own DATA register. In this case, $\overline{RDY}$ goes low only when conversions on all enabled channels are complete.

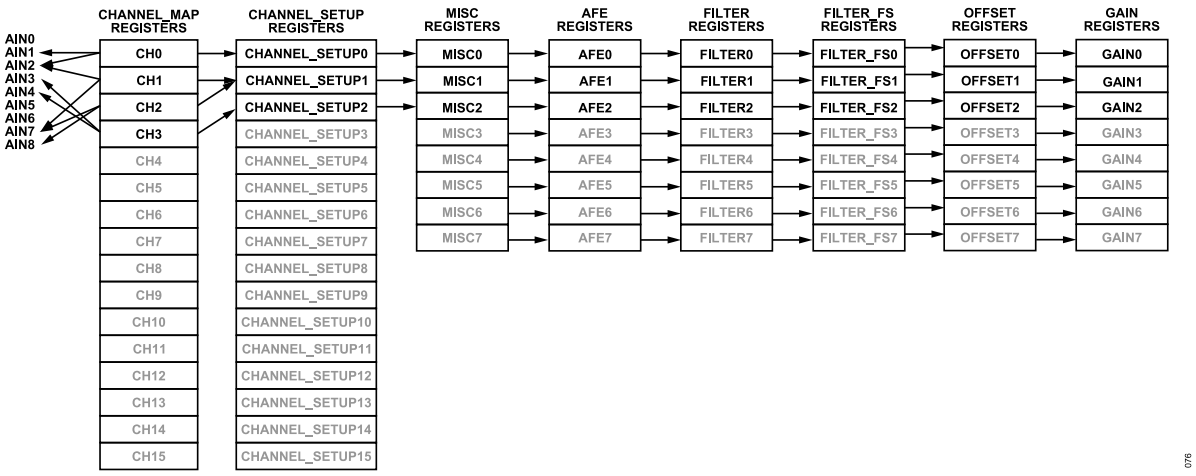

Figure 65. Mixed Differential and Single-Ended Configuration Using Multiple Shared Setups

ADC CIRCUIT INFORMATION

ANALOG INPUT CHANNEL

The AD4195-4 uses flexible multiplexing, thus, any of the analog input pins, AIN0 to AIN8, can be selected as a positive input or a negative input. This feature allows the user to perform diagnostics such as checking that pins are connected. It also simplifies the printed circuit board (PCB) design. For example, the same PCB can accommodate 2-wire, 3-wire, and 4-wire resistance temperature detectors (RTDs).

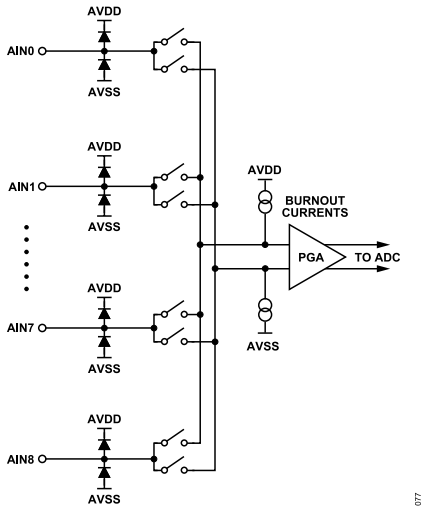

Figure 66. Analog-Input Multiplexer Circuit

The channels are configured using the AINP[5:0] bits and the AINM[5:0] bits in the CHANNEL_MAP Registers. The device can be configured to have four differential inputs, eight pseudodifferential inputs, or a combination of both. When using differential inputs, use adjacent analog input pins to form the input pair. Using adjacent pins minimizes any mismatch between the channels on the PCB.

For Gain = 1 Precharge, the PGA is bypassed but a precharge buffer is used to ensure the analog input is settled when sampled by that ADC. For all other gain settings, the PGA along with the precharge buffer is used. Using the PGA leads to lower input currents. Therefore, the input can tolerate significant source impedance and is tailored for direct connection to external resistive type sensors such as strain gauges or RTDs.

When the device is operated in Gain = 1 Precharge, the device has a higher analog input current. Therefore, resistor/capacitor (RC) combinations on the input pins can cause gain errors, which depends on the output impedance of the source that is driving the ADC input.

The absolute input voltage range is restricted to a range between AVSS and AVDD. To minimize input current, use an absolute input range between AVSS – 0.1V and AVDD + 0.1V. The common-mode voltage must not exceed these limits, otherwise, linearity and noise performance degrade.

EXTERNAL MULTIPLEXER CONTROL

If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled through the AD4195-4 GPIOn pins. With the CHAN_TO_GPIO bit in the PIN_MUXING register set to 1, the GPIOn pins output the active channel number for the external multiplexer. The timing is controlled by the AD4195-4. Therefore, the channel change is synchronized with the ADC, which eliminates any need for external synchronization.

PROGRAMMABLE GAIN AMPLIFIER (PGA)

When the gain stage is enabled (all gains except Gain = 1 Precharge), the output from the multiplexer is applied to the input of the PGA. The presence of the PGA means that signals of small amplitude can be gained within the AD4195-4 and still maintain excellent noise performance. The PGA also includes a gain of 0.5. Therefore, the applied signal can be attenuated by 2 rather than amplified.

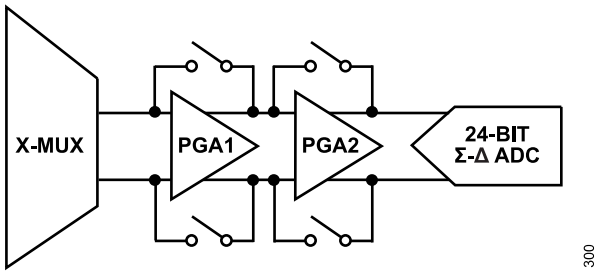

Figure 67. PGA

The AD4195-4 can be programmed to have a gain of 0.5, 1, 2, 4, 8, 16, 32, 64, or 128 by using the PGA bits in the AFEn registers (see Table 103). The PGA consists of two stages. For gains less than 16 (except Gain = 1 Precharge), a single stage is used, whereas for gains greater than 8, both stages are used.

The analog input range is $\pm V_{REF}$/gain. Therefore, with an external 2.5V reference, the unipolar ranges are from 0mV to 19.53mV to 0V to 5V, and the bipolar ranges are from ±19.53mV to ±5V. For high reference values, for example, V_{REF} = AVDD, the analog input range must be limited. The maximum allowed differential analog input range is ±(AVDD – 0.65V)/gain while the maximum allowed single-ended analog input range is 0 to (AVDD – 0.65V)/gain.

REFERENCE

The AD4195-4 has an embedded 2.5V reference with a temperature coefficient of 5ppm/°C typical. Embedding the reference on the AD4195-4 reduces the number of external components required in applications such as thermocouples, which leads to a reduced PCB size.

The internal reference is enabled by default but can be disabled through the REF_EN bit in the REF_CONTROL register (see Table 113). When the internal reference is enabled, it is available on the REFOUT pin. A 0.1µF decoupling capacitor is required on REFOUT when the internal reference is active.

ADC CIRCUIT INFORMATION

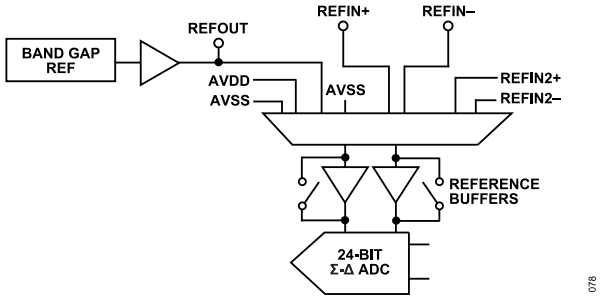

Figure 68. Reference Connections

This reference can be used to supply the ADC (by setting the REF_SELECT bits in the AFEn register to 10 binary) or an external reference can be applied. For external references, the ADC has a fully-differential input capability for the channel. In addition, the user can select one of two external reference options (REFIN or REFIN2). REFIN2 is available using GPIO0 (REFIN2+) and GPIO1 (REFIN2−). The reference source for the AD4195-4 is selected using the REF_SELECT bits in the AFEn register (see Table 103).

The absolute voltage allowed on the REFINn+ and REFINn− pins is from AVSS − 50mV to AVDD + 50mV when the reference buffers are disabled. With the reference buffers enabled or in precharge mode, the buffers are rail-to-rail. Therefore, the absolute voltage on each reference pin is from AVSS to AVDD. The reference voltage of REFINn (REFINn+ − REFINn−) is 2.5V nominal, but the AD4195-4 is functional with reference voltages from 1V to AVDD.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the devices, the effect of the low frequency noise in the excitation source is removed because the application is ratiometric. If the AD4195-4 is used in nonratiometric applications, use a low noise reference.

The recommended 2.5V reference voltage sources for the AD4195-4 include the ADR4525 and the LTC6655LN-2.5, which are low noise references. Note that the reference input provides a high impedance, dynamic load when unbuffered. Because the input impedance of each reference input is dynamic, RC combinations on these inputs can cause DC gain errors if the reference inputs are unbuffered, which depends on the output impedance of the source driving the reference inputs.

Reference voltage sources typically have low output impedance. Therefore, these sources are tolerant to having decoupling capacitors on REFINn+ without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. In this situation, using the reference buffers is required. Figure 69 shows the connections for the ADR4525 and LTC6655LN-2.5 to the AD4195-4. Connections for the LTC6655LN-4.096 to the AD4195-4 are similar.

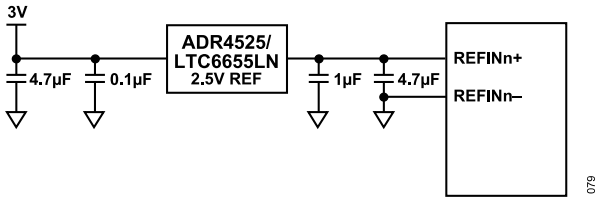

Figure 69. ADR4525/LTC6655LN-2.5 to AD4195-4 Connections

BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD4195-4 can accept either unipolar or bipolar input voltage ranges, which allows the user to tune the ADC input range to the sensor output range. When a bipolar power supply is used, the device accepts truly bipolar inputs. When a unipolar power supply is used, a bipolar input range does not imply that the device can tolerate negative voltages with respect to system AVSS.

Unipolar and bipolar signals on the AINP input are referenced to the voltage on the AINM input. For example, if AINM is 2.5V and the ADC is configured for unipolar mode with a gain of 1, the input voltage range on the AINP input is 2.5V to 5V when V_{REF} = 2.5V, AVDD = 5V. If the ADC is configured for bipolar mode, the analog input range on the AINP input is 0V to AVDD. The bipolar/unipolar option is chosen by programming the bipolar bit in the AFEn register.

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero-differential input voltage resulting in a code of 00…00, a midscale voltage resulting in a code of 100…000, and a full-scale input voltage resulting in a code of 111…111. The output code for any analog input voltage can be represented as:

$$Code = (2^N \times A_{IN} \times Gain)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is twos complement with a negative full-scale voltage resulting in a code of 100…000, a zero-differential input voltage resulting in a code of 000…000, and a positive full-scale input voltage resulting in a code of 011…111.

Table 31. Output Codes and Ideal Input Voltages (FS = Full-Scale)

Description	Analog Input	Code (Hex)
FS – 1LSB	$+V_{REF}/gain \times (1 - 2^{-N+1})$	0x7FFFFF
+1LSB	$(V_{REF}/gain)/2^{N-1}$	0x000001
Midscale	0	0x000000
−1LSB	$-(V_{REF}/gain)/2^{N-1}$	0xFFFFFF
−FS + 1LSB	$-V_{REF}/gain \times (1 - 2^{-N+1})$	0x800001
−FS	$-V_{REF}/gain$	0x800000

ADC CIRCUIT INFORMATION

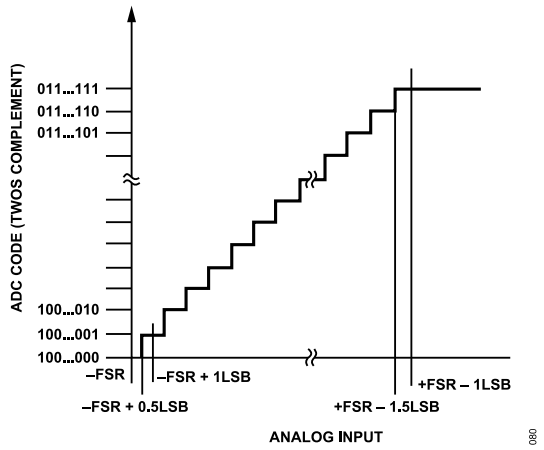

Figure 70. ADC Ideal Transfer Function (FS = Full-Scale)

EXCITATION CURRENTS

The AD4195-4 also contains two software configurable, constant current sources that can be programmed to equal 10µA, 50µA, 100µA, 250µA, 500µA, 1mA, or 1.5mA. These current sources can be used to excite external resistive bridges or RTD sensors. The current sources source currents from AVDD and can be directed to any of the analog input pins or the GPIO pins (see Figure 71).

The pins on which the currents are made available are programmed using the I_OUT_PIN bits in the CURRENT_SOURCEn register (see Table 119). The magnitude of each current source is individually programmable using the I_OUT_VAL bits in its CURRENT_SOURCEn register. In addition, all currents can be output to the same analog input pin or GPIO pin.

Note that the on-chip reference must be enabled when using the excitation currents.

For applications such as 3-wire RTD sensors, both excitation currents can be used to compensate for lead wire resistance. The excitation current mismatch and mismatch drift is optimized to minimize any error due to the excitation current mismatch. To further reduce any error due to excitation current mismatch, the currents can be swapped or chopped. When the CHOP_IEXC bits in the MISCn register are set appropriately, the two currents are swapped for each conversion and subsequent conversions are averaged by the AD4195-4. This swapping or chopping cancels any error due to excitation current mismatch.

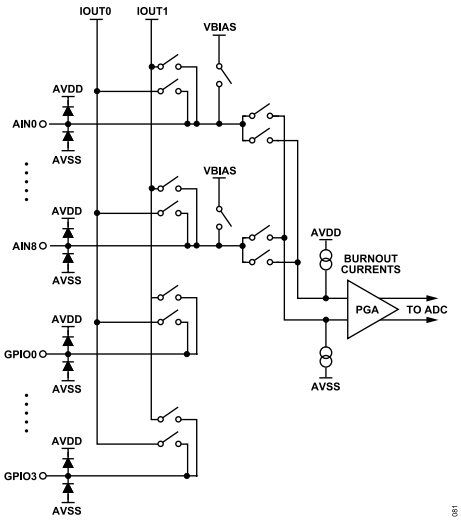

Figure 71. Excitation Current and Bias Voltage Connections

BRIDGE POWER-DOWN SWITCH

In bridge applications such as strain gauges and load cells, the bridge itself consumes significant current. For example, a 350Ω load cell requires 14.3mA of current when excited with a 5V supply. To reduce the current consumption of the system, the bridge can be disconnected (when it is not being used) using the bridge power-down switch. The AD4195-4 includes two bridge power-down switches. GPIO pins GPIO0 and GPIO1 can be configured as power-down switch0 (PDSW0) and power-down switch1 (PDSW1), respectively. The switches themselves are then controlled through the PDSW bits in the POWER_DOWN_SW register (see Table 87). Each switch can withstand 25mA typically of continuous current, and it has an on resistance of 10Ω typical. When the AD4195-4 is placed in standby mode, the power-down switches are opened by default. To retain control of the switches, set the STB_PDSWn bits in the STANDBY_CTRL register.

GENERAL-PURPOSE INPUTS/OUTPUTS (GPIO0 TO GPIO3)

The AD4195-4 has four general-purpose inputs/outputs: GPIO0 to GPIO3. These are configured as general-purpose inputs/outputs using the GPIO_MODE bits in the GPIO_MODE register (see Table 121). When configured as outputs, the pins can be pulled high or low using the GPIO_OUTPUT_DATA bits in the register GPIO_OUTPUT_DATA register (see Table 123), that is, the value at the pin is determined by the setting of the GPIO_DATn bits. The logic levels for these pins are determined by AVDD rather than by IOVDD. When the GPIO_OUTPUT_DATA register is read, the GPIO_OUTPUT_DATA bits reflect the actual value at the pins. This is useful for short-circuit detection.

The GPIO pins are multifunctional, that is, other features such as the power-down switches and excitation currents can be enabled on these pins also. If multiple functions are enabled at the same time, the priority of functionality is as follows:

ADC CIRCUIT INFORMATION

1. Power-down switches (which can be enabled on GPIO0 and GPIO1).
2. GPIO_OUTPUT_DATA. Any GPIOs not used as power-down switches can function as general-purpose output pins.
3. CHANNEL_TO_GPIO. The relevant bits of the current channel in the sequencer are output on any pins not used for functions as mentioned in priority 1 and 2 above.

Note that it is possible to enable excitation currents or enable REFIN2 (GPIO0/GPIO1) on these pins also. Therefore, the user must review all settings to ensure the pins have correct function in the application.

BIAS VOLTAGE GENERATOR

A bias voltage generator is included on the AD4195-4 (see Figure 71). When enabled on an analog input, it biases the pin to (AVDD + AVSS)/2. This function is useful in unbiased thermocouple applications, as the voltage generated by the thermocouple must be biased around some DC voltage if the ADC operates from a unipolar power supply. The bias voltage generator is controlled using the VBIAS bits in the V_BIAS register (see Table 115). The power-up time of the bias voltage generator is dependent on the load capacitance. For more details, see the Specifications section.

MULTIPLEXER CHOPPING

The AD4195-4 includes multiplexer chopping (enabled using the CHOP_ADC bits in Table 101). With chop enabled (the two bits are set to 01 binary), the ADC offset and offset drift are minimized. When chop is enabled, the analog input pins are continuously swapped. Therefore, with the analog input pins connected in one direction, the settling time of the filter is allowed to elapse until a valid conversion is available. The analog input pins are then inverted and another valid conversion is obtained. Subsequent conversions are then averaged to minimize the offset. This continuous swapping of the analog input pins and the averaging of subsequent conversions means that the offset drift is also minimized. As two conversions are being averaged, the RMS noise improves by √2. Therefore, the p-p resolution improves by 0.5 bits approximately.

Chopping may affect the output data rate and settling time. For example, with the $Sinc^3$ filter, the output data rate is reduced by a factor of three approximately while the settling time is increased by a factor of two approximately when comparing chopping enabled versus chopping disabled. For other filters such as the post filters, chopping has only a small impact on the output data rate and settling time. The Digital Filter section lists the settling times for the different filter types with chop disabled. With chop enabled, the first conversion takes a time of twice this settling time while subsequent conversions occur at the settling time specified for the filter. Chopping also adds first order notches at odd integer multiples of $nf_{ADC}/2$. For example, using the $Sinc^3$ filter with an output data rate of 50SPS, notches are placed at 25Hz, 75Hz, and 125Hz.

CLOCK

The AD4195-4 includes an internal 16MHz clock on chip. Use either the internal or an external clock as the clock source to the AD4195-4. The clock source is selected using the CLOCKSEL bits in the CLOCK_CTRL register (see Table 83).

The internal clock can also be made available at the CLK pin. This is useful when several ADCs are used in an application and the devices must be synchronized. The internal clock from one device can be used as the clock source for all ADCs in the system. For more details, see the ADC Synchronization section.

The AD4195-4 can also use an externally supplied clock connected to the CLK pin. The logic levels of this clock input are defined by the voltage applied to the IOVDD pin.

The AD4195-4 includes an internal divide by 2, 4, 8, which is selectable through the CLOCKDIV bits in the CLOCK_CTRL register. This divider divides the internal or external clock source selected for the ADC. The default setting is an internal divide by 2.

STANDBY AND POWER-DOWN MODES

In standby mode, most blocks are powered down. The LDOs remain active so that registers maintain their contents. By default, all other functions are disabled in standby mode. However, through the STANDBY_CTRL Register, a user can select which functions to remain active in standby mode. The excitation currents, internal reference, power-down switches, pull-up currents, bias voltage, and internal clock, if enabled in the system, can remain active in standby mode by setting bits in the STANDBY_CTRL register appropriately. Diagnostics are disabled in standby mode.

When exiting standby mode, the AD4195-4 requires 160 MCLK cycles approximately to power up and settle. MCLK is the main clock being used by the ADC rather than the applied clock frequency (internal oscillator or external clock frequency). Therefore, if the applied clock is divided by 4 or 8, the time to exit standby is longer. If an external main clock is being used, ensure that it is active before issuing the command to exit standby mode. Do not write to the ADC_ CTRL register again until the ADC has powered up and settled.

In power-down mode, all blocks are powered down, including the LDOs. All registers lose their contents, and the digital outputs GPIO0 to GPIO3 are placed in tristate. To prevent accidental entry to power-down mode, the ADC must first be placed into standby mode. If an external main clock is being used, keep it active until the device is placed in power-down mode. Exiting power-down mode requires the pattern of 63 1s and one 0 repeated three times on SDI with $\overline{CS}$ low. The AD4195-4 requires 1.4ms approximately to power up and settle. After this time, the user can access the on-chip registers.

ADC CIRCUIT INFORMATION

CALIBRATION

The AD4195-4 provides three calibration modes that can be used to eliminate the offset and gain errors on a per setup basis:

- Internal zero-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

The internal gain error is factory calibrated. Therefore, internal full-scale calibration is not supported on the AD4195-4. Only one channel can be active during calibration. When converting an analog input, the internal ADC conversion result is scaled using the ADC calibration registers before being written to the DATA register.

The default value of the OFFSET register is 0x000000, and the nominal value of the GAIN register is 0x555555. The calibration range of the ADC gain is from 0.4 × V_{REF}/gain to 1.05 × V_{REF}/gain. For more details, see the Span and Offset Limits section.

The following equations show how the values in the OFFSET and GAIN registers are used within the AD4195-4. Note that the OFFSET register uses twos complement. In unipolar mode, the ideal relationship, that is, not taking into account the ADC gain error and offset error, is as follows:

$$Data = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - Offset\right) \times \frac{Gain}{0 \times 400000} \times 2 \quad (1)$$

In bipolar mode, the ideal relationship, that is, not taking into account the ADC gain error and offset error, is as follows:

$$Data = \left(\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - Offset\right) \times \frac{Gain}{0 \times 400000} \quad (2)$$

To start a calibration, write the relevant value to the mode bits in the ADC_CTRL register (see Table 89). The $\overline{RDY}$ pin (shared with SDO by default but can be output on DIG_AUX1) and the RDYB bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding OFFSET or GAIN register are updated, the RDYB bit in the status register is reset, the $\overline{RDY}$ pin returns low, and the AD4195-4 reverts to idle mode. Note that if the $\overline{RDY}$ pin is shared with SDO, the pin is tristated when $\overline{CS}$ is high.

During an internal offset calibration, the selected positive analog input pin is disconnected, and it is connected internally to the selected negative analog input pin. For this reason, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference.

System calibrations expect the system zero-scale (offset) voltage or system full-scale (gain) voltage to be applied to the selected positive and negative pins before initiating the calibration mode. As a result, errors external to the ADC are removed. The system zero-scale calibration must be performed before the system full-scale calibration.

From an operational point of view, treat a calibration like another ADC conversion. Set the system software to monitor the RDYB bit in the status register or the $\overline{RDY}$ pin to determine the end of a calibration via a polling sequence or an interrupt-driven routine.

An internal/system offset calibration and system full-scale calibration requires a time equal to the settling time of the selected filter to be completed.

A calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy and is accurate for all output data rates. The internal gain error is factory calibrated for all gains. Therefore, if the default value in the GAIN register is not overwritten by a system full-scale calibration or a direct write to the GAIN register, the AD4195-4 automatically applies the appropriate gain coefficient internally when the PGA gain is changed. If a system full-scale calibration has been performed or the GAIN register has been written to, a new calibration is then required for a given channel if the reference source or the PGA gain for that channel is changed.

The AD4195-4 provides the user with access to the on-chip calibration registers, which allows the microprocessor to read the calibration coefficients from the device and to write its own calibration coefficients from prestored values in the electronically erasable programmable read-only memory (EEPROM). A read or write of the OFFSET and GAIN registers can be performed at any time except during an internal or self-calibration. The values in the calibration registers are 24 bits wide. The span and offset of the device can also be controlled using the registers.

SPAN AND OFFSET LIMITS

System calibration can be used to compensate for offset or gain errors in the external circuit and to control the input span and offset of the device. Whenever system calibration is performed, the amount of input offset and span adjustments that can be accommodated is limited. The input span is the difference between the input voltage that corresponds to the positive full-scale code and the input voltage that corresponds to the negative full-scale code. The range of input span achievable with system calibration has a minimum value of 0.8 × V_{REF}/gain and a maximum value of 2.1 × V_{REF}/gain.

The input span and offset adjustment must also account for the limitation on the positive full-scale code voltage (1.05 × V_{REF}/gain) and negative full-scale code voltage (−1.05 × V_{REF}/gain). Therefore, to determine the limits for system offset (zero-scale) and gain (full-scale) calibrations, the user must ensure that the offset after adjustment plus the maximum positive span range after adjustment does not exceed 1.05 × V_{REF}/gain.

The amount of offset and span adjustment that can be accommodated depends also on whether the configuration is unipolar or bipolar. This is the best shown by the following examples.

ADC CIRCUIT INFORMATION

If the device is used in unipolar mode with a required span of 0.8 × V_{REF}/gain, the offset range that the system calibration can handle is from −1.05 × V_{REF}/gain to +0.25 × V_{REF}/gain. If the device is used in unipolar mode with a required span of V_{REF}/gain, the offset range that the system calibration can handle is from −1.05 × V_{REF}/gain to +0.05 × V_{REF}/gain. Similarly, if the device is used in unipolar mode and required to remove an offset of 0.2× V_{REF}/gain, the span range that the system calibration can handle is 0.85 × V_{REF}/gain.

If the device is used in bipolar mode with a required span of ±0.4 × V_{REF}/gain, then the offset range that the system calibration can handle is from −0.65 × V_{REF}/gain to +0.65 × V_{REF}/gain. If the device is used in bipolar mode with a required span of ±V_{REF}/gain, the offset range the system calibration can handle is from −0.05 × V_{REF}/gain to +0.05 × V_{REF}/gain. Similarly, if the device is used in bipolar mode and required to remove an offset of ±0.2 × V_{REF}/gain, the span range that the system calibration can handle is ±0.85 × V_{REF}/gain.

DIGITAL FILTER

The AD4195-4 offers a great deal of flexibility in the digital filter. The device has several filter options. The option selected affects the output data rate, settling time, and 50Hz and 60Hz rejection. The following sections describe each filter type, which indicate the available output data rates for each filter option. The filter response along with the settling time and 50Hz and 60Hz rejection is also discussed.

The FILTER_TYPE bits in the FILTER register (see Table 105) select between the different filter types while the value in the FILTER_FS register sets the output data rate.

SINC^5 + AVG FILTER

When the AD4195-4 is powered up, the Sinc^5 + Avg filter is selected by default. The settling time is approximately equal to 1/output data rate for slow output data rates but increases to 5/output data rate at the high output data rates. Therefore, the conversion time is near constant when converting on a single channel or when converting on several channels at the lower output data rates. This filter gives excellent noise performance over the complete range of output data rates. In Figure 72, the blocks shown in gray are unused.

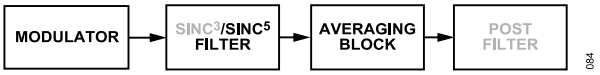

Figure 72. Sinc^5 + Avg Filter

Enable the Sinc^5 + Avg using the FILTER_TYPE bits in the FILTER register (see Table 105). With this filter, an averaging filter is included after the Sinc^5 filter. The Sinc^5 filter operates at a constant output data rate of 62.5kSPS. The value written to the FILTER_FS register indicates the amount of averaging to be performed (in the averaging block). Averaging is (FILTER_FS[15:0]/4). FILTER_FS can have a value between 4 and 65532 with increasing step size of 4 (the 2LSBs of the 16-bit word must be set to 0). Therefore, allowable FILTER_FS values are 4, 8, 12, 16, 20……..65532. At FILTER_FS = 4, the averaging is equal to 1 so the Sinc^5 filter only is used, which gives an output data rate of 62.5kSPS. For higher FILTER_FS values, the averaging block is used.

Output Data Rate and Settling Time, Sinc^5 + Avg Filter

When continuously converting on a single channel, the output data rate is:

$$f_{ADC} = f_{CLK} / (128 \times Avg) \quad (3)$$

where:

f_{ADC} is the output data rate.

f_{CLK} is the main clock frequency/clock divide where clock divide refers to the CLOCKDIV bits in the CLOCK_CTRL register (see Table 83).

Avg = FILTER_FS[15:0]/4. *FILTER_FS[15:0]* is the decimal equivalent of the FILTER_FS[15:0] bits in the FILTER_FS register (see Table 107).

When a channel is manually selected by the user, there is an extra delay in the first conversion. The time required (settling time) is equal to:

$$t_{SETTLE} = ((4 + Avg) \times 128 + PT) / f_{CLK} \quad (4)$$

where PT = *Processing Time* = 96 when FILTER_FS = 4 and 98 for all other FILTER_FS values.

Table 32 lists sample FILTER_FS[15:0] settings and the corresponding output data rates and settling times.

Table 32. Examples of Output Data Rates and the Corresponding Settling Times (Sinc^5 + Avg Filter, 16MHz Clock, Clock Divide = 2)

FILTER_FS[15:0]	First Notch (Hz)	Output Data Rate (SPS)	Settling Time (ms)
4,160	60.04	60.04	16.7
5,000	50	50	20.076
4	62,500	62,500	0.092

When a channel change occurs, the modulator and filter are reset. The settling time is allowed to generate the first conversion after the channel change. Subsequent conversions on this channel occur at $1/f_{ADC}$. For slow output data rates, the settling time and $1/f_{ADC}$ time are very similar.

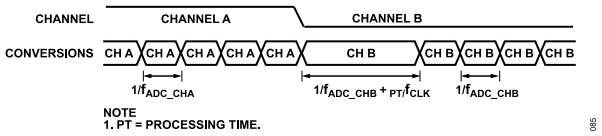

Figure 73. Sinc^5 + Avg Filter (FS >16)

When the device is converting on a single channel and a step change occurs on the analog input, the ADC does not detect the change and continues to output conversions. If the step change is synchronized with the conversion, one intermediate conversion is output from the ADC for FILTER_FS > 16 (see Figure 74). For FILTER_FS = 4, the filter performs as a Sinc^5 filter. Therefore, there are four intermediate conversions. If the step change is asynchronous to the conversion process, there are up to two intermediate conversions when FILTER_FS > 16 and five intermediate conversions when FILTER_FS = 4.

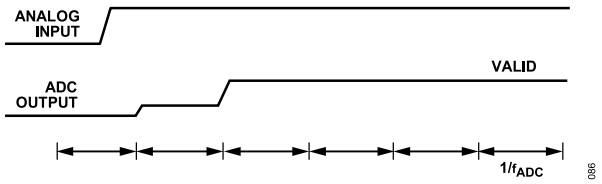

Figure 74. Synchronous Step Change on the Analog Input, Sinc^5 + Avg Filter (FILTER_FS > 16)

DIGITAL FILTER

For FILTER_FS = 8, 12, and 16, the number of intermediate conversions is listed in Table 33.

Table 33. Step Change on Analog Input

FILTER_FS[15:0]	Intermediate Conversions Synchronous	Intermediate Conversions Asynchronous
16	1 to 2	2
12	2	2 to 3
8	2 to 3	3

Sequencer

The description in the Output Data Rate and Settling Time, Sinc5 + Avg Filter section is valid when manually switching channels or when changing operating mode. When multiple channels are enabled, the on-chip sequencer is automatically used. The device automatically sequences between all enabled channels. In this case, the first conversion on the first channel in the sequence takes the complete settling time as listed in Table 32.

For all subsequent conversions, the time required for the first conversion on a channel is the filter settling time (PT = 0). If multiple conversions are read from a channel (REPEAT > 1), the second conversion and subsequent conversions on the selected channel take a time of $1/f_{ADC}$.

50Hz and 60Hz Rejection, Sinc^5 + Avg Filter

Figure 75 shows the frequency response when FILTER_FS[15:0] is set to 5,000.

Table 32 lists the corresponding output data rate. The Sinc^5 filter places the first notch at:

$$f_{NOTCH} = f_{CLK}/128 \quad (5)$$

The averaging block places notches at f_{NOTCH}/Avg (Avg = FILTER_FS/4). Notches are also placed at multiples of this frequency. Therefore, when FILTER_FS[15:0] is set to 5,000, a notch is placed at 62,500Hz due to the Sinc^5 filter and notches are placed at 50Hz and multiples of 50Hz due to the averaging.

The notch at 50Hz is a first-order notch. Therefore, the notch is not wide. This means that the rejection at exactly 50Hz is good, assuming a stable main clock. However, in a band of 50Hz ± 0.5Hz, the rejection degrades significantly. The rejection at 50Hz ± 0.5Hz is 40dB minimum, assuming a stable clock. Therefore, a good main clock source is recommended when using the Sinc^5 + Avg filter if optimum 50Hz rejection is required.

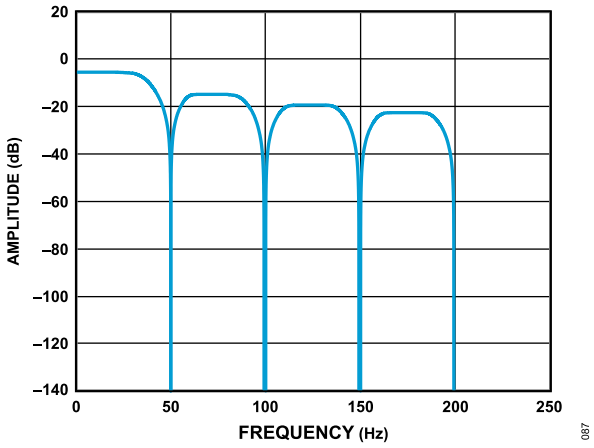

Figure 75. 50Hz Rejection

Figure 76 shows the filter response when FILTER_FS[15:0] is set to 4160. In this case, a notch is placed at 60Hz and multiples of 60Hz. The rejection at 60Hz ± 0.5Hz is equal to 40dB minimum.

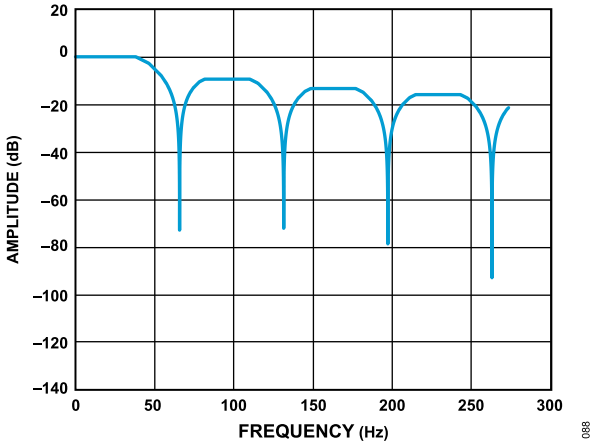

Figure 76. 60Hz Rejection

Simultaneous 50 Hz/60Hz rejection is achieved when FILTER_FS[15:0] is set to 25,000. Notches are placed at 10Hz and multiples of 10Hz, thereby, give simultaneous 50Hz and 60Hz rejection (see Figure 77). The rejection at 50Hz ± 0.5Hz and 60Hz ± 0.5Hz is 40dB typically.

DIGITAL FILTER

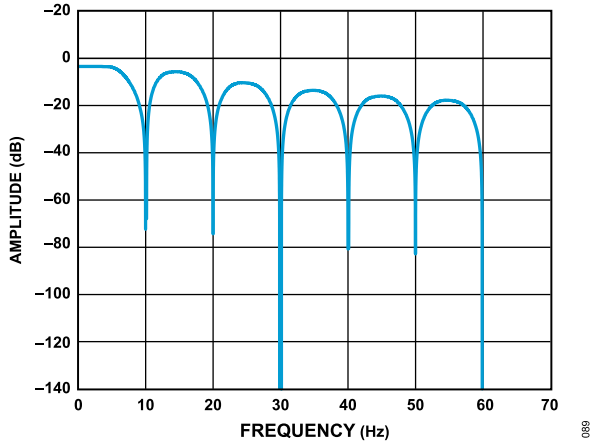

Figure 77. Simultaneous 50Hz and 60Hz Rejection

SINC^5 FILTER

The filter is selected using the FILTER_TYPE bits in the FILTER register (see Table 105). This filter supports high output data rates, that is, from 976.5SPS to 62,500SPS. This filter is useful at high output data rates as a higher order sinc filter suppresses high frequency noise better than a Sinc^3 filter, which leads to better peak-peak resolution. This filter has good noise performance and moderate settling time. Note that this filter option does not support 50Hz and 60Hz rejection. In Figure 78, the blocks shown in gray are unused.

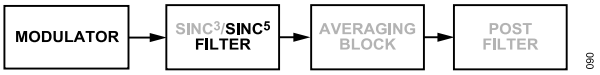

Figure 78. Sinc^5 Filter

Sinc^5 Output Data Rate and Settling Time

The output data rate (the rate at which conversions are available on a single channel when the ADC is continuously converting) equals

$$f_{ADC} = f_{CLK}/(32 \times FILTER\_FS[8:0]) \quad (6)$$

where:

f_{ADC} is the output data rate.

f_{CLK} is the main clock frequency/clock divide where clock divide refers to the CLOCKDIV bits in the CLOCK_CTRL register (see Table 83).

FILTER_FS[8:0] is the decimal equivalent of the FILTER_FS[8:0] bits in the FILTER_FS register (see Table 107). FILTER_FS[8:0] can have a value of 4, 8, 12, 16, 20, 24…..256. The 2LSBs of FILTER_FS[8:0] must be set to 0.

When a channel is manually selected by the user or there is an operating mode change, there is an extra delay in the first conversion. The time required (settling time) when using the Sinc^5 filter is equal to:

$$t_{SETTLE} = (5 \times 32 \times FILTER\_FS[8:0] + PT) / f_{CLK} \quad (7)$$

where PT = *Processing Time* = 96.

Table 34 gives some examples of FILTER_FS[8:0] settings and the corresponding output data rates and settling times.

Table 34. Examples of Output Data Rates and the Corresponding Settling Times for the Sinc^5 Filter (16MHz Clock, Clock Divide = 2)

FILTER_FS[8:0]	Output Data Rate (SPS)	Settling Time (ms)
256	976.5	5.132
4	62,500	0.092

When a channel change occurs, the modulator and filter are reset. The complete settling time is allowed to generate the first conversion after the channel change (see Figure 79). Subsequent conversions on this channel are available at 1/f_{ADC}.

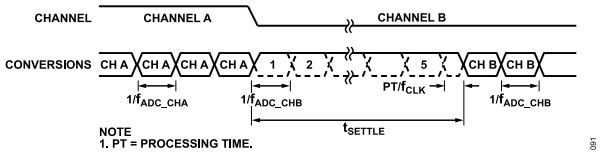

Figure 79. Sinc^5 Channel Change

When conversions are performed on a single channel and a step change occurs, the ADC does not detect the change in the analog input. Therefore, it continues to output conversions at the programmed output data rate. However, it is at least five conversions later before the output data accurately reflects the analog input. If the step change occurs while the ADC is processing a conversion, the ADC takes six conversions after the step change to generate a fully settled result (see Figure 80).

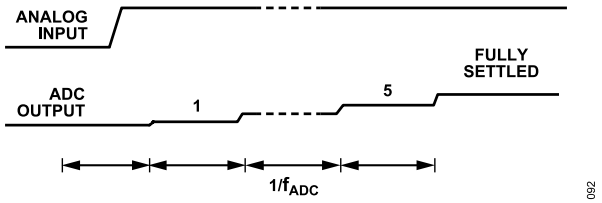

Figure 80. Asynchronous Step Change in the Analog Input

Sequencer

The description in the Sinc5 Output Data Rate and Settling Time section is valid when manually switching channels or changing operating mode. When multiple channels are enabled, the on-chip sequencer is automatically used. The device automatically sequences between all enabled channels. In this case, the first conversion on the first channel in the sequence takes the complete settling time as listed in Table 34.

For all subsequent conversions, the time required for the first conversion is the filter settling time (PT = 0).

DIGITAL FILTER

If REPEAT is greater than 1 when using the sequencer, the second conversion and subsequent conversions on the selected channel take a time of $1/f_{ADC}$.

Sinc^5 50Hz and 60Hz Rejection

The Sinc^5 filter does not support 50Hz and 60Hz rejection because this filter can be used at the higher output data rates only on this ADC.

SINC^3 FILTER

A Sinc^3 filter is also available on the AD4195-4. The filter is selected using the FILTER_TYPE bits in the FILTER register (see Table 105). This filter has good noise performance, moderate settling time, and good 50Hz and 60Hz (±1Hz) rejection. In Figure 81, the blocks shown in gray are unused.

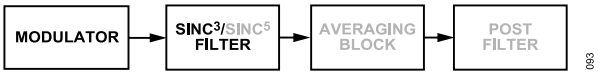

Figure 81. Sinc^3 Filter

Sinc^3 Output Data Rate and Settling Time

The output data rate (the rate at which conversions are available on a single channel when the ADC is continuously converting) equals:

$$f_{ADC} = f_{CLK}/(32 \times FILTER\_FS[15:0]) \quad (8)$$

where:

f_{ADC} is the output data rate.

f_{CLK} is the main clock frequency/clock divide where clock divide refers to the CLOCKDIV bits in the CLOCK_CTRL register (see Table 83).

FILTER_FS[15:0] is the decimal equivalent of the FILTER_FS[15:0] bits in the FILTER_FS register (see Table 107).

FILTER_FS[15:0] can have a value of 4, 8, 12, 16, 20…..65532 (the 2LSBs of the 16-bit word must be set to 0. The output data rate can be programmed from 3.8SPS to 62,500SPS.

The settling time when using the Sinc^3 filter is equal to:

$$t_{SETTLE} = (3 \times 32 \times FILTER\_FS[15:0] + PT)/f_{CLK} \quad (9)$$

where *PT* = *Processing Time* = 92.

Table 35 gives some examples of FILTER_FS[15:0] settings and the corresponding output data rates and settling times.

Table 35. Examples of Output Data Rates and the Corresponding Settling Times for the Sinc^3 Filter (16MHz Clock, Clock Divide = 2)

FS[15:0]	Output Data Rate (SPS)	Settling Time (ms)
4160	60.04	49.93
5,000	50	60.01

Table 35. Examples of Output Data Rates and the Corresponding Settling Times for the Sinc^3 Filter (16MHz Clock, Clock Divide = 2) (Continued)

FS[15:0]	Output Data Rate (SPS)	Settling Time (ms)
4	62,500	0.0595

When a channel change occurs, the modulator and filter are reset. The complete settling time is allowed to generate the first conversion after the channel change (see Figure 82). Subsequent conversions on this channel are available at $1/f_{ADC}$.

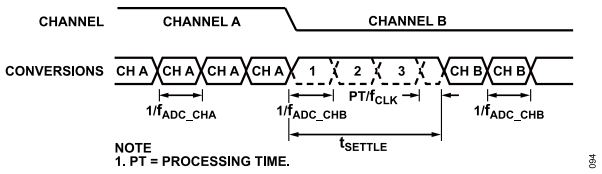

Figure 82. Sinc^3 Channel Change

When conversions are performed on a single channel and a step change occurs, the ADC does not detect the change in the analog input. Therefore, it continues to output conversions at the programmed output data rate. However, it is at least three conversions later before the output data accurately reflects the analog input. If the step change occurs while the ADC is processing a conversion, the ADC takes four conversions after the step change to generate a fully settled result (see Figure 83).

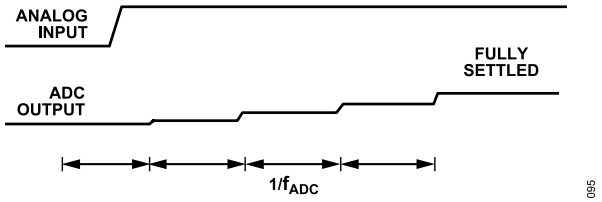

Figure 83. Asynchronous Step Change in the Analog Input

Sequencer

The description in the Sinc3 Output Data Rate and Settling Time section is valid when manually switching channels or changing operating mode. When multiple channels are enabled, the on-chip sequencer is automatically used. The device automatically sequences between all enabled channels. In this case, the first conversion on the first channel in the sequence takes the complete settling time as listed in Table 35.

For all subsequent conversions, the time required for the first conversion on a channel is the filter settling time (PT = 0).

If REPEAT is greater than 1 when using the sequencer, the second conversion and subsequent conversions on the selected channel take a time of $1/f_{ADC}$.

DIGITAL FILTER

Sinc^3 50Hz and 60Hz Rejection

Figure 84 shows the frequency response of the Sinc^3 filter when the output data rate is programmed to 50SPS. The Sinc^3 filter gives 50Hz ± 1Hz rejection of 95dB minimum for a stable main clock.

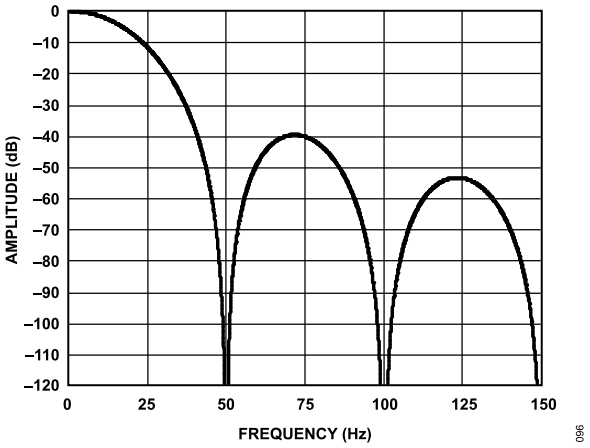

Figure 84. Sinc^3 Filter Response (50SPS Output Data Rate)

Figure 85 shows the frequency response of the Sinc^3 filter when the output data rate is programmed to 60SPS. The Sinc^3 filter has rejection of 95dB minimum at 60Hz ± 1Hz, assuming a stable main clock.

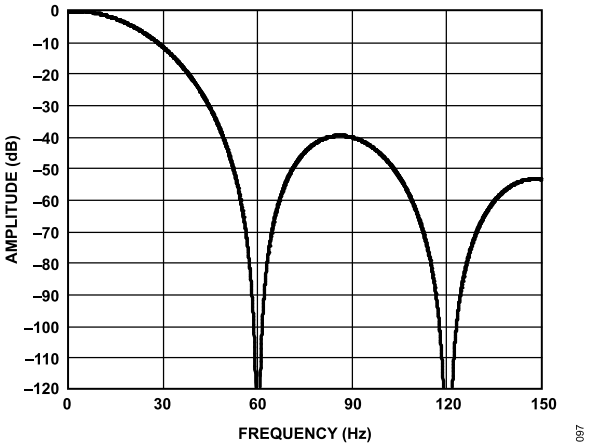

Figure 85. Sinc^3 Filter Response (60SPS Output Data Rate)

When the output data rate is 10SPS, simultaneous 50Hz and 60Hz rejection is obtained. The Sinc^3 filter has rejection of 100dB minimum at 50Hz ± 1Hz and 60Hz ± 1Hz (see Figure 86).

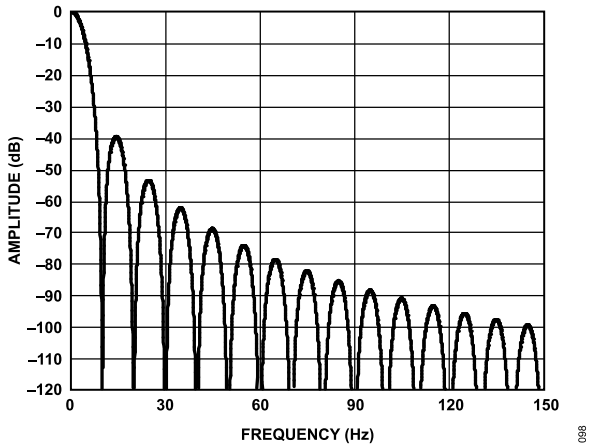

Figure 86. Sinc^3 Filter Response (10SPS Output Data Rate)

POST FILTERS

The 40ms, 50ms, and 60ms post filters provide rejection of 50Hz and 60Hz simultaneously and allow the user to trade off settling time and rejection. These filters can operate up to 25SPS or can reject up to 89dB of 50Hz ± 1Hz and 60Hz ± 1Hz interference. These filters are realized by post filtering the output of the Sinc^5 + Avg filter.

Note that the Sinc^3 or Sinc^5 + Avg filter can be used before the post filters.

However, the Sinc^5 + Avg filter is recommended as both options give similar noise performance but the Sinc^5 + Avg filter gives lower settling time. The sinc filter must have an output data rate close to 1200SPS to obtain 50Hz and 60Hz rejection (FILTER_FS = 208 when default main clock settings are used). The filters can be used with other FILTER_FS values, but the notches are no longer at 50Hz and 60Hz. With the average by 16 post filter option, the settling time is close to the inverse of the first filter notch. Therefore, the filter allows rejection of 50Hz or 60Hz with a settling time close to 1/50Hz and 1/60Hz. The FILTER_FS bits in the FILTER_FS Registers are used to vary the notch position. It is recommended to use the Sinc^5 + Avg filter before the average by 16 option as it gives lower settling time than the Sinc^3 filter, and the noise performance is similar for both options.

Note that the Sinc^5 + Avg filter itself also supports 50Hz or 60Hz with a settling time at 1/50Hz or 1/60Hz.

The post filter option to use is selected using the POST_FILTER_SEL bits in the FILTER register (see Table 105). In Figure 87, the blocks shown in gray are unused.

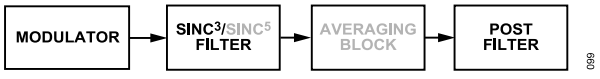

Figure 87. Post Filters

Table 36 shows the output data rates with the accompanying settling times and the rejection.

DIGITAL FILTER

When continuously converting on a single channel, the first conversion requires a time of t_{SETTLE}. Subsequent conversions occur at $1/f_{ADC}$. When multiple channels are enabled (either manually or using the sequencer), the settling time is required to generate the first valid conversion on each channel when it is enabled. If multiple conversions are being performed when the channel is enabled, the second conversion and subsequent conversions occur at $1/f_{ADC}$. Allowable FILTER_FS values are from 4, 8, 12....1024 (the 2LSBs must be set to 0).

Table 36. AD4195-4 Post Filters: Output Data Rate, Settling Time (t_{SETTLE}), and Rejection (FILTER_FS = 208, 16MHz Main Clock, Clock Divide = 2, Sinc^5 + Avg filter)

Conversion Time (ms)	Output Data Rate (SPS)	f_{3dB} (Hz)	t_{SETTLE} (ms)	Simultaneous Rejection of 50Hz ± 1Hz and 60Hz ± 1Hz (dB)[1]
40	25.04	15.14	39.98	62
50	20.03	13.4	49.96	85
60	16.69	12.82	59.94	89

[1] Stable main clock used.

Table 37. Average by 16 Post Filter: Output Data Rate, Settling Time (t_{SETTLE}), and Rejection, Sinc^5 + Avg Filter, 16MHz Clock, Clock Divide = 2

FILTER_FS	Output Data Rate (SPS)	f_{3dB} (Hz)	t_{SETTLE} (ms)	Simultaneous Rejection of 50Hz ± 1Hz and 60Hz ± 1Hz (dB)[1]
260	60.1	26.57	16.68	40 (60Hz only)
312	50.1	22.14	20.01	38 (50Hz only)

[1] Stable main clock used.

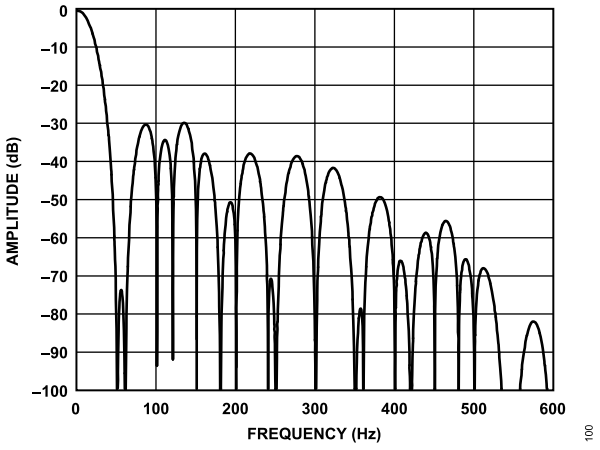

Figure 88. DC to 600Hz, 50ms Settling Time Post Filter

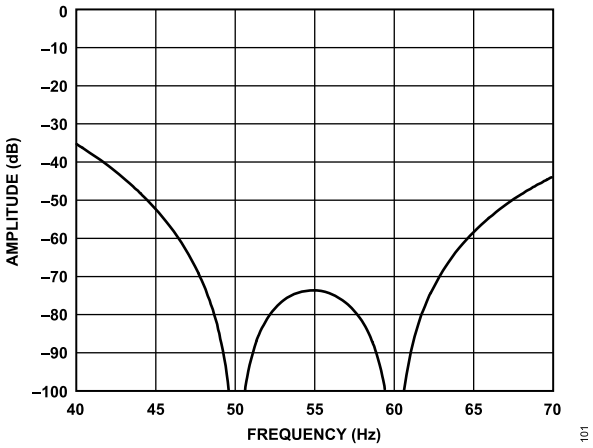

Figure 89. Zoom in 40Hz to 70Hz, 50ms Settling Time Post Filter

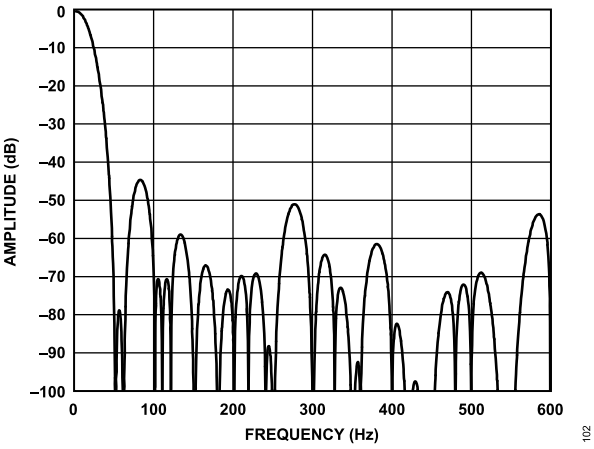

Figure 90. DC to 600Hz, 60ms Settling Time Post Filter

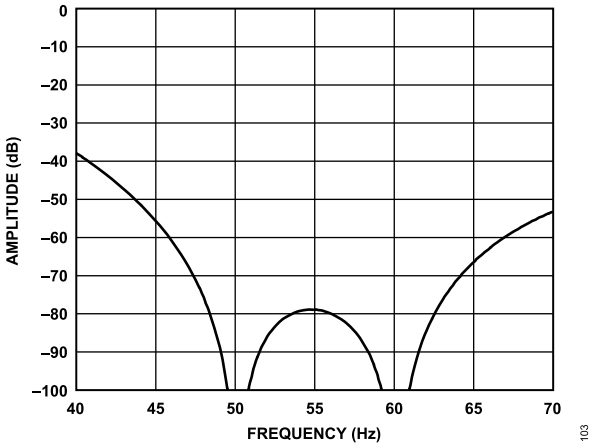

Figure 91. DC to 600Hz, 60ms Settling Time Post Filter

DIGITAL FILTER

ANTI-ALIASING FILTER

The AD4195-4 modulator samples on the rising and falling edge of f_{MOD} and outputs data to the digital filter at a rate of f_{MOD}. There is a zero in the frequency response profile of the modulator centered at odd multiples of f_{MOD}, which means that there is no foldback from frequencies at the f_{MOD} rate and at odd multiples of this rate. The fact that there is no foldback from frequencies at the f_{MOD} rate pushes the first unprotected zone of the AD4195-4 out to 2 × f_{MOD}. However, the modulator is open to noise for even multiples of f_{MOD}. There is no attenuation at these zones.

In addition, the AD4195-4 uses a chopping technique in the modulator similar to that of a chopped amplifier to remove offset, offset drift, and 1/f noise. The rate of chopping may result in out of band tones being aliased back to the bandwidth of interest. Figure 92 shows the rejection of out of band tones for f_{CHOP} = f_{MOD}/8, the chop frequency used on the AD4195-4.

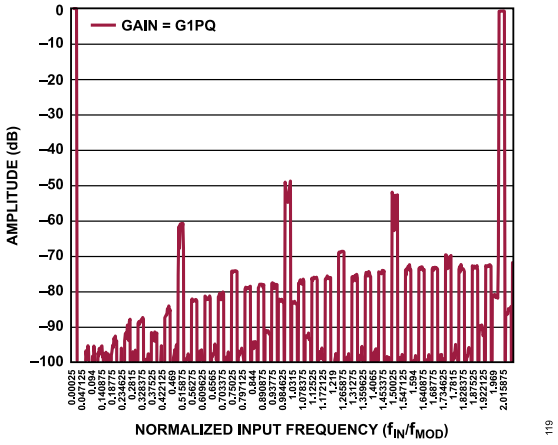

Figure 92. Rejection of Out of Band Tones (ADC Only)

The PGA also uses chopping, its chopping frequency being f_{MOD}/16. To protect against out of band tones aliasing back into the bandwidth of interest, an anti-aliasing filter must be used. A passive (resistor-capacitor) filter is sufficient. The profile of the filter depends on the environment of operation.

DIGITAL INTERFACE

The AD4195-4 digital interface is used to access the user configuration registers, initiate the ADC conversions, perform diagnostic tests, and readback conversion results. The interface uses 4 wires ($\overline{CS}$, SCLK, SDI, and SDO). The part can also be operated with $\overline{CS}$ hardwired low. The interface is compatible with QSPI™ and MICROWIRE interface standards as well as most digital signal processors (DSPs). For both read and write SPI transactions, data is sampled on the rising edge of SCLK. For all SPI transactions, the most significant bit (MSB) of each byte is shifted first. The SDO line also acts as a data ready signal ($\overline{RDY}$) by default. When data is available to be read from the AD4195-4 device, the SDO line is brought low. Alternatively, a dedicated data ready signal can be brought out on DIG_AUX1.

All communication to the AD4195-4 begins with an instruction phase, which indicates whether the operation is a read or write operation and which register is being accessed. This is followed by the data phase where the data is written to the ADC (using SDI) or read from the ADC using SDO.

The logic level of the AD4195-4 digital interface is set by the IOVDD voltage, and can range from 1.7V to 5.25V.

For a detailed description of the addresses and functions of each of the AD4195-4 user configuration registers, see the On-Chip Register Map section.

ADC CONVERSION MODES AND ACCESSING CONVERSIONS

By default, the ADC continuously converts using the Sinc^5 + Avg filter (MODE bits in Table 89 set to 000b). Each enabled channel has a dedicated data register (Bit MULTI_DATA_REG_SEL in Table 89 is set to 0). Register DATA_PER_CHANNELn holds the conversion result for CHANNELn. The RDYB bit in Table 69 goes low each time a conversion on all enabled channels is complete. If $\overline{CS}$ is low, the SDO line also goes low when conversions on all enabled channels are complete because the $\overline{RDY}$ signal is available on SDO by default. $\overline{RDY}$ can alternatively be output on DIG_AUX1. When per channel data registers are used, STATUS bits cannot be automatically appended to the conversion result. To read each data register, an instruction phase is required, which indicates that the next operation is a read of the data register. $\overline{RDY}$ returns high when the conversion results from the enabled channels have been read.

Enabled channels can also share a data register (Bit MULTI_DATA_REG_SEL in Table 89 is set to 1). The RDYB bit in Table 69 goes low each time a conversion is complete. The $\overline{RDY}$ signal also goes low if $\overline{CS}$ is low or $\overline{RDY}$ is output on DIG_AUX1. When reading the conversions, the 24-bit conversion can be accessed through the DATA_24B register. To read the contents of the STATUS register along with the conversion result, read Register DATA_24B_STATUS. The AD4195-4 also supports 16-bit conversion reads where the 16MSBs only of the conversion result can be read. The relevant registers are DATA_16B to read the 16-bit conversion and DATA_16B_STATUS to read the status bits along with the conversion result. When the conversion result is read from the data register, $\overline{RDY}$ goes high.

The user can read the data registers additional times when the data register is shared or when per channel data registers are used, if required. However, the user must ensure that a data register is not being accessed at the completion of the next conversion if the register is to be updated. Otherwise, the new conversion word is lost.

When several channels are enabled, the ADC automatically sequences through the enabled channels. When per channel data registers are used, the user must configure the part for a single conversion on each enabled channel (REPEAT bits in Table 97 for the channel set to 0). When the enabled channels share a data register, multiple conversions can be performed on a channel each time it is selected in the sequence (again using the REPEAT bits in Table 97 for the channel). When all channels are converted, the sequence starts again with the first channel. The channels are converted in order from lowest enabled channel to highest enabled channel. The appropriate data register is updated as soon as each conversion is available.

When the MODE bits in Table 89 are set to 100b, the sequence is performed once and the ADC is then placed in standby mode. If one channel only is enabled, a single conversion is performed.

Rather than having an instruction and a data phase when reading back the conversions, there are two further options to simplify the readback of conversions: continuous read and continuous transmit. For more details, see the Continuous Read and the Continuous Transmit sections.

CONTINUOUS READ

Continuous read is designed to provide maximum throughput from the ADC. Access to the register map is disabled to allow simple shift register access to the ADC conversion data.

Continuous read is enabled using the CONT_READ bits in Table 89 (setting 01b enables continuous read), which turns the SPI interface into a simple (duplex) shift register that can only shift out an ADC conversion result while simultaneously checking for an exit command and/or software reset. No instruction phase is required when reading ADC data. Continuous read can only be used when all enabled channels share a data register.

This interface option only supports read access from the ADC data register plus optionally appended status register and/or CRC. Conversion data is 24-bit wide in this mode. $\overline{CS}$ can be toggled at the end of the read or held permanently low. Taking $\overline{CS}$ high three-states SDO and resets the SPI state. If $\overline{CS}$ is not brought high after performing the ADC read, the LSB of data continues to drive SDO (or revert to $\overline{RDY}$, depending on the DIG_AUX1 configuration).

Continuous read must only be used if the ADC is enabled in a continuous conversion mode. The SDI pin must be kept low or high

while in continuous read mode to avoid triggering a software reset. Also, the host must be able to read data at the required throughput rate to avoid aborted transfers. The ongoing data read back is aborted if not completed before the next ADC result is ready.

$\overline{RDY}$ is used to gate SCLK in this mode. $\overline{RDY}$ is set to 0 when a new ADC data result is written into the data register and set to 1 after the ADC data read is completed. Only the first 24 SCLKs (plus the optional status bits plus optional CRC) are acted on by the AD4195-4. Therefore, each ADC result can only be read once. Any additional SCLKs are ignored until $\overline{RDY}$ next goes low.

To exit continuous read, write 0xA5 to the ADC during the first 8 SCLKs of the ADC data read. After sending the command to exit, the remaining bits of the conversion result can be read. A reset can also be used to exit continuous read. Writing a pattern of 63 1s and one 0 three times resets the device. However, the registers are set to the default values.

If CRC is enabled (using the CONT_READ_STATUS_EN bit in Table 89) prior to enabling continuous read, a seed value of 0xA5 is used.

CONTINUOUS TRANSMIT

With the continuous transmit option, data, when available, is automatically transmitted accompanied by the appropriate number of data clocks (DCLKs). The Host does not need to react to an interrupt from $\overline{RDY}$ to retrieve the ADC data, which eases the timing burden on the Host. The data clocks are generated from the selected device main clock (with a divide by 2, 4, 8 option through the DCLK_DIVIDE bits in Table 83). Continuous transmit mode is enabled by setting the CONT_READ bits in Table 89 to 10b. Continuous transmit can only be used when all enabled channels share a data register.

Similar to continuous read, access to the register map is disabled apart from allowing a write to the CONT_READ bits to exit continuous transmit. Continuous transmit must only be used if the ADC is enabled in a continuous conversion mode. The SDI pin must be kept low while using this mode to avoid triggering a software reset. The SDO line becomes a dedicated ADC Data output. DIG_AUX1 is used to output the $\overline{RDY}$ signal and DIG_AUX2 is configured to output the data clock (DCLK).

This mode uses either a 32-bit or 64-bit data frame depending on the inclusion of CRC (enabled using the CONT_READ_STATUS_EN bit in Table 89). The data frame may include padding bytes of 0x00 (see Table 38 and Table 39). Therefore, only a 32-bit data frame is transferred if CRC is disabled.

$\overline{RDY}$ (available on DIG_AUX1) goes low when a new ADC result is available, as per any other operating mode, and returns high during the last bit of the ADC data (+Status/CRC) transmission, which ends the continuous transmit frame. Either 32 or 64 DCLKs are output after $\overline{RDY}$ goes low, depending on the chosen output format. Each ADC result is only transmitted once. DCLK idles high between data transmissions. If $\overline{CS}$ is not brought high after the data transmission, the LSB of the last slot continues to drive SDO. Note that taking $\overline{CS}$ high during a transmission aborts the transmission. If $\overline{CS}$ is high when $\overline{RDY}$ goes low, no transmission occurs.

Table 38. Data Transmission Format (32-Bit Data Frame with CRC Disabled or First 32 Bits of a 64-Bit Data Frame)

Byte 1	Byte 2	Byte 3	Byte 4
STATUS or 0x00	ADC_DATA[23:16]	ADC_DATA[15:8]	ADC_DATA[7:0]

Table 39. Data Transmission Format (Second 32 Bits of a 64-Bit Data Frame with CRC Enabled)

Byte 5	Byte 6	Byte 7	Byte 8
STATUS	0x00	0x00	CRC

SPI FRAME SYNCHRONIZATION

The $\overline{CS}$ pin can be used to frame data during an SPI transaction. A falling edge on $\overline{CS}$ enables the digital interface and initiates an SPI transaction. When writing to the AD4195-4, the data on SDI is latched on rising edges of SCLK. When a read transaction is initiated, it shifts data out on SDO on the falling edges of SCLK. Each SPI transaction consists of at least one instruction phase and data phase, which are described in more detail in the Instruction Phase and the Data Phase sections. For all SPI transactions, data is aligned with the MSB first on a register byte level. Taking $\overline{CS}$ high during an SPI transaction terminates the data transfer and disables the digital interface. Figure 93 and Figure 94 show the stages of a basic SPI write and read frame, respectively, for the AD4195-4. $\overline{CS}$ can be permanently connected low. To enable synchronization of the SPI between the processor and the AD4195-4, the MSB of the instruction phase is always 0. Therefore, with SDI idling high between data transfers, any SCLK pulses are ignored by the AD4195-4. A 0 on SDI indicates the beginning of an instruction phase.

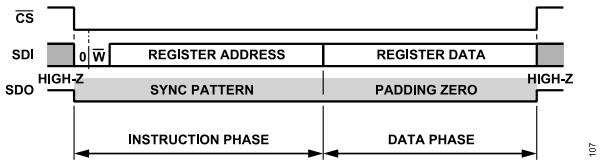

Figure 93. Basic SPI Write Frame (CRC Error Detection Disabled)

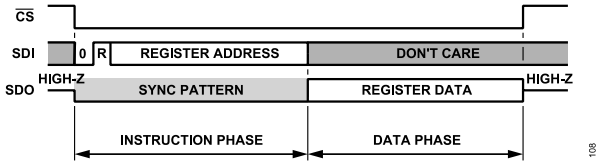

Figure 94. Basic SPI Read Frame (CRC Error Detection Disabled)

Figure 2 and Figure 3 show detailed timing diagrams for performing register reads and writes through the SPI interface (for more details on the timing specifications, see the Timing Characteristics section).

DIGITAL INTERFACE

Instruction Phase

Each register access starts with the instruction phase. Figure 93 and Figure 94 show the basic read and write operations with $\overline{CS}$ being controlled by the microprocessor. $\overline{CS}$ can be hardwired low also.

The instruction phase consists of a 0 followed by a read/$\overline{write}$ bit (R/$\overline{W}$) followed by a 14-bit register address. Setting R/$\overline{W}$ low initiates a write instruction (see Figure 93), whereas setting R/$\overline{W}$ high initiates a read instruction (see Figure 94). The register address specifies the address of the register to be accessed. The register address is 14-bit in length (14-bit addressing) by default. The 14-bit addressing allows access to the full memory map. When addressing memory locations below Address 0x40, the addressing can be changed to 6-bit (6-bit addressing) with the SHORT_INSTRUCTION bit in the INTERFACE_CONFIG_B Register. The 6-bit addressing allows shorter instruction phases when accessing memory locations up to Address 0x3F (63 decimal). Above that, 14-bit addressing must be selected. A synchronization pattern is output on SDO during the instruction phase for the processor to determine if synchronization is lost. When using 16-bit instructions, the pattern is 0x2645. When the instruction phase is 8-bit, the synchronization pattern is 0x26. The microprocessor must check Bits[14:0] (16-bit instructions) or Bits[6:0] (8-bit instructions) only as the MSB of the pattern may not be captured reliably by the microprocessor. Note that this function can be disabled using the SEND_STATUS bit, in which case 0 is output on SDO.

Data Phase

The data phase immediately follows the instruction phase (as shown in Figure 93 and Figure 94). The data phase can include the data for a single-byte register or a multibyte register, which depends on the selected register.

The addressed register contents are updated immediately after the SCLK rising edge, which shifts in the last bit of the register data. For a single-byte register, the last bit is the eighth SCLK rising edge of the data phase. For a description of when multibyte register data is updated, see the Multibyte Registers section.

Data must be written to the AD4195-4 configuration registers in full bytes to ensure they are updated. If the data phase of an SPI write transaction does not include the entire byte of data for the register being updated, the contents of the register are not updated, and the CLOCK_COUNT_ERR bit in Table 67 is set.

If CRC is enabled, the AD4195-4 registers only update if a valid CRC is received by the device. If the CRC is invalid or is not provided, the target register does not update. For more details on the CRC feature, see the Checksum Protection section.

Multibyte Registers

Some AD4195-4 configuration registers consist of multiple bytes of data stored in adjacent addresses and are referred to as multibyte registers. For more details on a list of multibyte registers on the AD4195-4, see the On-Chip Register Map section.

When writing to a multibyte register of the AD4195-4, all bytes must be written in a single SPI transaction. If an SPI write transaction to a multibyte register is attempted on a per byte basis, the register contents are not updated on the device, and the REGISTER_PARTIAL_ACCESS_ERR bit in Table 67 is set. A write transaction to a multibyte register of the AD4195-4 takes effect after the last SCLK rising edge of the data phase, which shifts in the last bit of the register data.

The address of a multibyte register always depends on the ADDR_ASCENSION bit in Table 43. With addresses descending, the first byte accessed in the data phase must be the most significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next lowest address. With addresses ascending, the first byte accessed in the data phase must be the least significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next highest address. For example, the 16-bit ADC_DATA register is two bytes long, and the addresses of its least significant byte and most significant byte are 0x16 and 0x17, respectively.

Multibyte registers can be read in a single SPI transaction or each byte can be addressed separately. If an SPI read transaction of a multibyte register is attempted on a per byte basis, the REGISTER_PARTIAL_ACCESS_ERR bit in Table 67 is set.

Figure 95 and Figure 96 show write and read transactions to a multibyte register (two bytes) for address ascending and descending, respectively. If the ADDR_ASCENSION bit in Table 43 is set to 0, the address decrements after each byte are accessed. If ADDR_ASCENSION is set to 1, the address increments after each byte are accessed.

When accessing multibyte registers, use descending addresses to shift in most significant byte first.

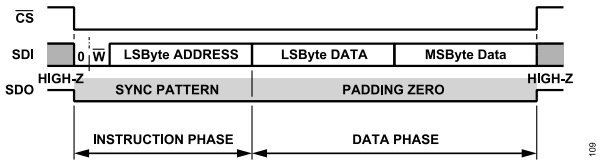

Figure 95. Multibyte Register Address Ascending Write Access

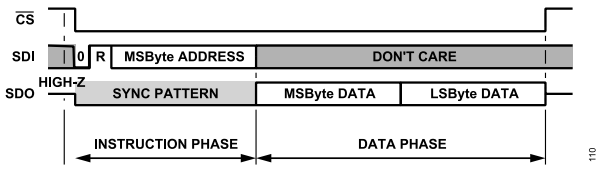

Figure 96. Multibyte Register Address Descending Read Access

DIGITAL INTERFACE

DEVICE IDENTIFICATION

The following registers contain identification information about the AD4195-4. The VENDOR_ID register, to identify Analog Devices, Inc., as the vendor of the device, the CHIP_TYPE register to identify the category of Analog Devices products the device belongs to, the PRODUCT_ID register to be used in conjunction with CHIP_TYPE to identify a device, and the CHIP_GRADE register to record the device revision and performance grade. The SPI_REVISION register offers information on the SPI interface revision.

The AD4195-4 identifies as follows:

- VENDOR_ID = 0x0456
- CHIP_TYPE = 0x07
- PRODUCT_ID = 0x004C
- CHIP_GRADE = 0x04
- SPI_REVISION = 0x83

DEVICE RESET

The AD4195-4 provides three options for performing a device reset: a hardware reset, a software reset, and a reset by writing a specific sequence to the SDI pin. A reset sets the state of all user configuration registers listed in the on-chip register map to their default values (for more details, see the On-Chip Register Map section). The POR_FLAG_S bit in Table 69 is set when a reset occurs.

A POR hardware reset is initiated by taking the IOVDD/REGCAP_D power supply below a threshold voltage and the AD4195-4 remains in a reset state until the voltage returns above the threshold voltage. The threshold voltage has hysteresis to ensure the voltage recovers sufficiently before exiting POR.

To implement a software reset, Bit SW_RESET and Bit RESET_SW in Table 43 both need to be set to 1. These bits are automatically reset to 0 when the reset has occurred.

Another reset option is to write a specific pattern to the AD4195-4. This is required when the SPI is operated with $\overline{CS}$ hardwired low. To initiate a reset, write a pattern of 63 1s followed by one 0 three times to the AD4195-4while $\overline{CS}$ is held low.

Note that a software reset is not possible in continuous read or continuous transmit. A reset by writing the specific sequence of 1s and 0s works for all operating modes.

The AD4195-4 requires a short period of time to reset. If the digital host attempts to perform an SPI transaction before the device is ready, the transaction may not succeed and the NOT_READY_ERR bit in Table 67 is set. The bit can be cleared by writing 1 to its location. Interrogate the NOT_READY_ERR bit in Table 67 and the DEVICE_ERROR bit in Table 93 to verify complete initialization. If any error bit is flagged, perform a device reset.

IO DRIVE STRENGTH

The serial interface can operate with a power supply as low as 1.7V. However, at this low voltage, the digital outputs may not have sufficient drive strength if there is moderate parasitic capacitance on the board or the SCLK frequency is high. The DIG_OUT_STR bit in Table 81 increases the drive strength of all digital output pins.

SDO_RDYB_DLY

The serial interface uses a shared SDO and $\overline{RDY}$ pin by default. During a data read, this pin outputs the data from the register being read. After the read is complete, the pin reverts to outputting the $\overline{RDY}$ signal after a short fixed period of time (see the parameter t7 in the Timing Characteristics section). However, this time may be too short for some microcontrollers to reliably sample the last data bit and can be extended until the $\overline{CS}$ pin is brought high by setting the SDO_RDYB_DLY bit in the PIN_MUXING register (see Table 81) to 1. This means that $\overline{CS}$ must be used to frame each read operation and complete the serial interface transaction.

Note that $\overline{RDY}$ can also be output on the DIG_AUX1 pin if separate SDO and $\overline{RDY}$ pins are required. In this case, the SDO pin continues to output the LSB of the data register.

ADC SYNCHRONIZATION

The AD4195-4 offers several synchronization options, which allow the user to control the start of conversions on a single device or to ensure synchronization of multiple devices in a multi AD4195-4 design.

STANDARD SYNCHRONIZATION

When the SYNC_CTRL bits in the PIN_MUXING register (see Table 81) are set to 01b, the $\overline{\text{SYNC\_IN}}$ pin functions as a synchronization input. The $\overline{\text{SYNC\_IN}}$ input lets the user reset the modulator and the digital filter without affecting any of the setup conditions on the device. The sequencer is also reset. This feature allows the user to control the start of sampling. $\overline{\text{SYNC\_IN}}$ must be low for at least two main clock cycles to ensure that synchronization occurs.

If multiple AD4195-4 devices are operated from a common main clock, they can be synchronized to sample their analog inputs simultaneously. This synchronization is normally done after each AD4195-4 device has performed its own calibration or has calibration coefficients loaded into its calibration registers. A falling edge on the $\overline{\text{SYNC\_IN}}$ input resets the digital filter and the analog modulator and places the AD4195-4 into a consistent known state. While $\overline{\text{SYNC\_IN}}$ is low, the AD4195-4 is maintained in this known state. The device is taken out of reset on the main clock rising edge following the $\overline{\text{SYNC\_IN}}$ input low to high transition. Therefore, when multiple devices are being synchronized, take the $\overline{\text{SYNC\_IN}}$ input high on the main clock falling edge to ensure that all devices sample $\overline{\text{SYNC\_IN}}$ as high on the main clock rising edge.

If the $\overline{\text{SYNC\_IN}}$ input is not taken high sufficiently before the main clock edge, a difference of one main clock cycle between the devices is possible, that is, the instant at which conversions are available differs from device to device by a maximum of one main clock cycle. $\overline{\text{SYNC\_IN}}$ can also be used as a start conversion command for a single channel when in standard synchronization mode. Taking $\overline{\text{SYNC\_IN}}$ high starts a conversion, and the falling edge of the $\overline{\text{RDY}}$ output indicates when the conversion is complete. The settling time is required for each data register update. After the conversion is complete, bring $\overline{\text{SYNC\_IN}}$ low in preparation for the next conversion start signal.

ALTERNATE SYNCHRONIZATION

In alternate synchronization mode (SYNC_CTRL bits in Table 81 are set to 10b), the $\overline{\text{SYNC\_IN}}$ input operates as a start conversion command when several channels of the AD4195-4 are enabled. When the $\overline{\text{SYNC\_IN}}$ input is taken low, the ADC completes the conversion on the current channel, selects the next channel in the sequence, and then waits until the $\overline{\text{SYNC\_IN}}$ input is taken high to commence the conversion. The $\overline{\text{RDY}}$ output goes low when the conversion is complete on the current channel, and the data register is updated with the corresponding conversion. Therefore, the $\overline{\text{SYNC\_IN}}$ input does not interfere with the sampling on the currently selected channel but allows the user to control the instant at which the conversion begins on the next channel in the sequence. Alternate synchronization mode can be used only when several channels are enabled. It is not recommended to use this mode when a single channel is enabled.

ADC SYNCHRONIZATION

SYNCHRONIZING MULTIPLE AD4195-4 DEVICES

The AD4195-4 supports synchronization of multiple AD4195-4 devices in a system. DIG_AUX1 and DIG_AUX2 can be used to synchronize the devices. The devices must share a common main clock. On one ADC, the main ADC, DIG_AUX2 is configured as a START pin using the DIG_AUX2_CTRL bits in the PIN_MUXING register (see Table 81). DIG_AUX1 is configured as a SYNC_OUT pin using the DIG_AUX1_CTRL bits in Table 81. From the START signal applied to the main ADC, a synchronization signal SYNC_OUT is generated, SYNC_OUT being synchronized with the internal main clock. SYNC_OUT is then applied to the $\overline{\text{SYNC\_IN}}$ pins of all ADCs to force all ADCs to have synchronous conversion behavior.

DIAGNOSTICS

The AD4195-4 has numerous diagnostic functions on chip. Use the following features to ensure that:

- There are no overvoltages or undervoltages on the external reference/analog inputs.
- The external reference, if used, is present.
- The excitation currents, if used, are within specification.
- Only valid data is written to the on-chip registers.
- The power supply rails/internal LDOs are at expected levels.

DEVICE ERROR

If an error occurs when the AD4195-4 powers up and initializes, the DEVICE_ERROR flag in the ERROR register (see Table 93) is set. A device reset is recommended. The DEVICE_ERROR bit is cleared when the device initializes correctly from power-up or after a device reset. This bit cannot be cleared through a read operation.

REFERENCE DETECT

The AD4195-4 includes on-chip circuitry to detect if there is a valid reference for conversions or calibrations when the user selects an external reference as the reference source. This is a valuable feature in applications such as RTDs or strain gauges where the reference is derived externally.

This feature is enabled when the REF_DIFF_MIN_ERR_EN bit in ERROR_EN register (see Table 91) is set to 1. If the voltage between the selected REFINn+ and REFINn− pins goes below 0.6V, the AD4195-4 detects that it no longer has a valid reference. In this case, the REF_DIFF_MIN_ERR bit in Table 93 is set to 1. The MAIN_ERR_S bit in the STATUS register (see Table 69) is also set. To clear the REF_DIFF_MIN_ERR bit, write a 1 to the bit.

REFERENCE OVERVOLTAGE/UNDERVOLTAGE DETECTION

The absolute voltage on the REFINn+ input pin can also be monitored. The REF_OV_UV_ERR_EN bit in the ERROR_EN register (see Table 91) enables the overvoltage/undervoltage reference diagnostic. An overvoltage is flagged when the voltage on REFINn+ exceeds AVDD by at least 65mV, whereas an undervoltage is flagged when the voltage on REFINn+ goes below AVSS by at least 65mV. The REF_OV_UV_ERR bit in the ERROR register (see Table 93) is set to 1 if an overvoltage or undervoltage is detected. To clear the REF_OV_UV_ERR bit, write a 1 to the bit. Note that the absolute voltage on the affected pin must be reduced to AVDD + 0.015V to reset the bit for an overvoltage condition, whereas the voltage on the pin must be reduced to AVSS − 0.01V to reset the bit for an undervoltage condition.

CONVERSION ERRORS

The conversion process can also be monitored by the AD4195-4. The function can be enabled using the ADC_CONV_ERR_EN bit in the ERROR_EN register (see Table 91). With this function enabled, the ADC_CONV_ERR bit is set if an error occurs. The ADC_CONV_ERR flag is set if there is a saturation (overflow or underflow) of the ADC result. This flag is updated in conjunction with the update of the data register and can be cleared by writing 1 to the bit.

ANALOG INPUT OVERVOLTAGE/ UNDERVOLTAGE DETECTION

The overvoltage/undervoltage monitor checks the absolute voltage on the internal multiplexer output pins, MUX+ and MUX−. MUX+ and MUX− can be separately checked for overvoltages and undervoltages. AINP_OV_UV_ERR_EN enables the undervoltage and overvoltage checks on MUX+. An overvoltage occurs when the voltage on MUX+ exceeds AVDD by at least 65mV, whereas an undervoltage occurs when the voltage on MUX+ goes below AVSS by at least 65mV. Similarly, an overvoltage/undervoltage check on MUX− is enabled using the AINM_OV_UV_ERR_EN bit in the ERROR_EN register (see Table 91). The error bits are AINP_OV_UV_ERR and AINM_OV_UV_ERR in the ERROR register (see Table 93) and these are set to 1 if an overvoltage/undervoltage is detected. To clear either bit, write 1 to the bit. Note that the absolute voltage on the affected pin must be reduced to AVDD + 0.015V for an overvoltage condition before the bit is cleared, whereas the voltage on the pin must be reduced to AVSS − 0.01V for an undervoltage condition before the bit is cleared.

EXCITATION CURRENT COMPLIANCE

The internal excitation currents require headroom to supply the specified excitation current value. The IOUTn_COMP_ERR flags in the ERROR register (see Table 93) are set to 1 when the excitation current magnitude is less than expected due to insufficient headroom. The flags can be enabled through the IOUTn_COMP_ERR_EN bits in the ERROR_EN register (see Table 91). To clear an error flag, write 1 to the appropriate bit.

POWER SUPPLY MONITORS

Along with converting external voltages, the ADC can monitor the analog and digital power supply voltages. When the inputs of (AVDD to AVSS) or (IOVDD to DGND) are selected, the voltage (AVDD to AVSS or IOVDD to DGND) is internally attenuated by 5, and the resulting voltage is applied to the Σ-Δ modulator. This is useful because variations in the power supply voltage can be monitored.

LDO MONITORING

There are several LDO checks included on the AD4195-4. Similar to the external power supplies, the voltage generated by the analog and digital LDOs are selectable as inputs to the ADC. The voltage generated by ALDO and DLDO can also be monitored by enabling the ALDO_PSM_ERR_EN bit and the DLDO_PSM_ERR_EN bit, respectively, in the ERROR_EN register (see Table 91). When enabled, the output voltage of LDO is continuously monitored. If the ALDO voltage drops below 1.5V typically, the ALDO_PSM_ERR flag is asserted. If the DLDO voltage drops below 1.6V typically, the

DIAGNOSTICS

DLDO_PSM_ERR flag is asserted. To clear the flag, write 1 to the appropriate bit.

SPI SCLK COUNTER

The SCLK counter counts the number of SCLK pulses used in each read and write operation. $\overline{CS}$ must frame every read and write operation to use this function. All read and write operations are multiples of eight SCLK pulses (16, 32, 40, 48). If the SCLK counter counts the SCLK pulses and the result is not a multiple of eight, an error is flagged and the CLOCK_COUNT_ERR bit in the INTERFACE_STATUS_A register (see Table 67) is set.

The SCLK counter is always enabled. To clear the CLOCK_COUNT_ERR bit, write a 1 to this location in Table 67.

SPI READ/WRITE ERRORS

Along with the SCLK counter, the AD4195-4 can also check the read and write operations to ensure that valid registers are being addressed. If the user attempts to write to or read from an invalid address, an error is flagged and the ADDRESS_INVALID_ERR bit in the INTERFACE_STATUS_A register (see Table 67) is set.

If the user attempts to write to a read only register, the WR_TO_RD_ONLY_REG_ERR bit in Table 67 is set. If the complete number of bytes in a read/write operation is not transferred, the REGISTER_PARTIAL_ACCESS_ERR bit is set. To reset the WR_TO_RD_ONLY_REG_ERR bit or the REGISTER_PARTIAL_ACCESS_ERR bit, 1 must be written to these locations in Table 67. Note that all of these diagnostics are always enabled.

NOT READY ERROR

At certain times, the on-chip registers are not accessible. For example, during power-up, the on-chip registers are set to their default values. The user must wait until this operation is complete before writing to registers. If the user writes to registers during these busy periods, the NOT_READY_ERR flag is set, which indicates that the ADC is busy and the write operation is ignored. The NOT_READY_ERR flag is cleared by writing a 1 to this bit in the INTERFACE_STATUS_A register (see Table 67). This diagnostic cannot be disabled. Note that $\overline{RDY}$ can also be monitored to detect when the ADC is ready if $\overline{CS}$ is hardwired low.

CHECKSUM PROTECTION

CRC Error Detection

The AD4195-4 features optional cyclic redundancy check (CRC) to provide error detection for SPI transactions between the digital Host and the AD4195-4. CRC error detection is also supported in continuous read and continuous transmit operation. CRC is disabled by default.

CRC error detection allows the processor and the AD4195-4 to detect bit transfer errors with significant reliability. The CRC algorithm involves using a seed value and polynomial division to generate a CRC code. The processor and the AD4195-4 both calculate the CRC code independently to determine the validity of transferred data.

The AD4195-4 uses the CRC-8 standard with the following polynomial:

$$x^8 + x^2 + x + 1 \quad (3)$$

CRC error detection is enabled with the CRC_ENABLE and CRC_ENABLEB bits in the INTERFACE_CONFIG_C register (see Table 65). The value of CRC_ENABLE is only updated if CRC_ENABLEB is set to the CRC_ENABLE inverted value in the same register write instruction. To enable the CRC, CRC_ENABLE must therefore be set to 01b while CRC_ENABLEB is set to 10b in the same write transaction.

To disable the CRC, CRC_ENABLE must therefore be set to 00b while CRC_EN_B is set to 11b in the same write transaction. Writing inverted values to two separate fields reduces the chances of CRC being enabled in error.

Figure 97 and Figure 98 show how a CRC code is appended to the write or read, respectively, for the digital Host or AD4195-4 to validate the data. For register writes, the digital Host must generate the CRC byte. For register reads, the Host must also send the correct CRC byte that is checked by the AD4195-4. This allows the AD4195-4 to confirm that it received the correct instruction from the Host processor. In the same read transaction, the AD4195-4 provides the CRC code for the digital Host to verify.

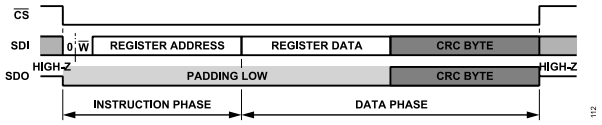

Figure 97. Basic SPI Write Frame (CRC Error Detection Enabled)

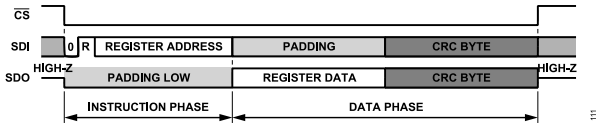

Figure 98. Basic SPI Read Frame (CRC Error Detection Enabled)

When accessing multibyte registers with CRC error detection enabled, the CRC code is placed after all bytes of register data.

When CRC error detection is enabled, the AD4195-4 does not update its register contents in response to a register write transaction unless it receives a valid CRC code at the end of the register data on SDI. If the CRC code is invalid, or the digital Host fails to transmit the CRC code, the AD4195-44 does not update its register contents, and the CRC_ERR flag in the INTERFACE_ STATUS_A register (see Table 67) is set. The CRC_ERR flag is write-1-to-clear (W1C) and the correct CRC is required for the write to clear to take effect.

Table 40 shows the seed value used in the CRC code calculation.

DIAGNOSTICS

Table 40. CRC Seed Values

SPI Transaction Type	Pin	Phase
Read	SDI	0xA5, instruction phase, padding
	SDO	0xA5, instruction phase, read data
Write	SDI	0xA5, instruction phase, write data
	SDO	0xA5, instruction phase, write data

Every CRC code in an SPI frame uses 10100101. This ensures that a register value of 0x000000 does not generate a CRC code of 0x00. A short between SDO and DGND causes a CRC of 0x00. Therefore, a fault condition is easily detectable.

Figure 99 shows an example where CRC is enabled in the first SPI transaction, and how the CRC codes are provided by the AD4195-4 during a read transaction and by the Host during a write transaction. In this example, the AD4195-4 is configured with the address descending (configuration writes not shown in Figure 99). This example shows the following sequence:

1. Register write of 0x66 to the INTERFACE_CONFIG_C register to enable the CRC.
2. $\overline{CS}$ is pulsed high.
3. Register read of the 16-bit ADC data plus status register (a multibyte register with the most significant byte at Address 0x1A).
4. Register write of 0x27 to the INTERFACE_CONFIG_C register to disable the CRC while still providing the CRC code.
5. $\overline{CS}$ is brought high.

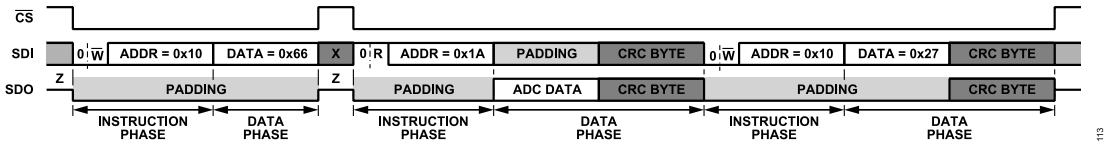

Figure 99. CRC Code SPI Transactions Example (Address Descending)

CRC Calculation

The checksum, which is 8 bits wide, is generated using the polynomial:

$x^8 + x^2 + x + 1$

To generate the checksum, the data is left shifted by 8 bits to create a number ending in eight Logic 0s. The polynomial is aligned to make its MSB adjacent to the leftmost Logic 1 of the data. An XOR (exclusive OR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned to make its MSB adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

DIAGNOSTICS

Example of a Polynomial CRC Calculation − 24-Bit Word: 0x654321 (8-Bit Instruction and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

Initial value 011001010100001100100001

011001010100001100100001000000000 left shifted 8 bits

$x^8 + x^2 + x + 1$ = 100000111 polynomial

100100100000110010000100000000 XOR result

100000111 polynomial

100011000110010000100000000 XOR result

100000111 polynomial

111111100100001000000000 XOR result

100000111 polynomial value

111110111000010000000 XOR result

100000111 polynomial value

111100000000100000000 XOR result

100000111 polynomial value

11100111000100000000 XOR result

100000111 polynomial value

11001001001000000000 XOR result

100000111 polynomial value

10010101010000000000 XOR result

100000111 polynomial value

101101100000000 XOR result

100000111 polynomial value

1101011000000 XOR result

100000111 polynomial value

101010110000 XOR result

100000111 polynomial value

1010001000 XOR result

100000111 polynomial value

10000110 checksum = 0x86

MEMORY MAP CHECKSUM PROTECTION

When this bit is set, a CRC calculation is performed on the memory map. Following this, periodic CRC checks are performed on the on-chip registers. If the register contents change due to register corruption or further register writes, the MM_CRC_ERR bit is set.

The memory map CRC function is enabled by setting the MM_CRC_ERR_EN bit in the ERROR_EN register (see Table 91) to 1. If an error occurs, the MM_CRC_ERR bit in the ERROR register (see Table 93) is set to 1. To clear the flag, write 1 to its location in the ERROR register.

BURNOUT CURRENTS

The AD4195-4 contains two constant current generators that can be programmed to 0.1µA, 2µA, or 10µA. One generator sources current from AVDD to MUXP, and one sinks current from MUXM to AVSS. These currents enable open-wire detection.

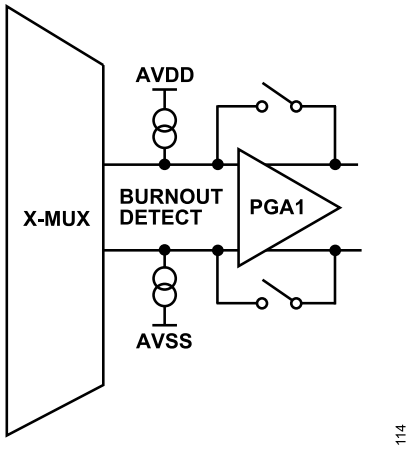

Figure 100. Burnout Currents

Both currents are either on or off. The BURNOUT bits in the MISCn register (see Table 101) enable/disable the burnout currents along with setting the amplitude. Therefore, the burnout currents are enabled/disabled on a per-channel basis. However, if enabled for a channel, the currents are only active when the channel is selected. Use these currents to verify that an external transducer is still operational. After the burnout currents are turned on, they flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resulting voltage measured is near full-scale, the user must verify why this is the case. A near full-scale reading can mean that the front-end sensor is open circuit. It can also mean that the front-end sensor is overloaded and is justified in outputting full-scale, or that the reference may be absent.

When a conversion is close to full-scale, the user must check these three cases before making a judgment. If the voltage measured is 0V, it may indicate that the transducer has short-circuited. For normal operation, these burnout currents are turned off by setting the BURNOUT bits to zero.

DIAGNOSTICS

PULL-UP CURRENTS

While the burnout currents are only active while a channel is being converted, the AD4195-4 also includes 100nA pull-up currents. These currents, if enabled, remain active on the AIN pins continuously. These currents can be enabled/disabled on a per pin basis through the I_PULL_UP register. If an AIN pin is floating, it is pulled to AVDD when the pull-up current is enabled. Therefore, an open on the pin is detectable. Note that if both AIN pins are floating and the pull-up currents are enabled, both pins are pulled to AVDD. Therefore, an open is not directly detectable. However, a conversion on each AIN pin with respect to AVSS can be used to detect the open.

TEMPERATURE SENSOR

Embedded in the AD4195-4 is a temperature sensor that is useful to monitor the die temperature. This is selected using the AINP[4:0] and AINM[4:0] bits in the CHANNEL_MAPn register. The sensitivity is 477µV/K, approximately. Subtract 5°C from the temperature sensor result.

The temperature sensor has an accuracy of ±2°C typically.

GROUNDING AND LAYOUT

The analog inputs and reference inputs are differential. Therefore, most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the device removes common-mode noise on these inputs. The analog and digital supplies to the AD4195-4 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of 2 x f_{MOD} (f_{MOD} being 2MHz when the main clock is 16MHz and clock divide = 2).

The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD4195-4 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD4195-4 is high and the noise levels from the converter are so low, care must be taken with regard to grounding and layout.

The PCB that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it results in the best shielding.

In any layout, the user must keep in mind the flow of currents in the system, which ensure that the paths for all return currents are as close as possible to the paths the currents took to reach their destinations.

Avoid running digital lines under the device because this couples noise onto the die. Allow the analog ground plane to run under the AD4195-4 to prevent noise coupling. The power supply lines to the AD4195-4 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, whereas signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. The AD4195-4 has two power supply pin: AVDD and IOVDD. The AVDD pin is referenced to AVSS, and the IOVDD pin is referenced to DGND. Decouple AVDD with a 1µF tantalum capacitor in parallel with a 0.1µF capacitor to AVSS. Place the 0.1µF capacitor as close as possible to the device, ideally right up against the device. Decouple IOVDD with a 1µF tantalum capacitor in parallel with a 0.1µF capacitor to DGND. All analog inputs must be decoupled to AVSS. If an external reference is used, decouple the REFINn+ and REFINn− pins to AVSS.

The AD4195-4 also has two on-board LDO regulators: one that regulates the AVDD supply and one that regulates the IOVDD supply. For the REGCAPA pin, it is recommended that a 0.1µF capacitor in parallel with a 1µF capacitor to AVSS be used. Similarly, for the REGCAPD pin, it is recommended that a 0.1µF capacitor in parallel with a 1µF capacitor to DGND be used.

If using the AD4195-4 with bipolar supply operation, a separate plane must be used for AVSS.

APPLICATIONS INFORMATION

The AD4195-4 offers a high-resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, the device is more immune to noisy environments, which makes it ideal for use in sensor measurement, and industrial and process control applications.

WEIGH SCALE

Figure 101 shows the AD4195-4 being used in a weigh scale application. The load cell is arranged in a bridge network and gives a differential output voltage between its OUT+ and OUT– terminals. Assuming a 5V excitation voltage, the full-scale output range from the transducer is 10mV when the sensitivity is 2mV/V. The excitation voltage for the bridge can be used to directly provide the reference for the ADC because the reference input range includes the supply voltage.

A second advantage of using the AD4195-4 in transducer-based applications is that the bridge power-down switch can be fully utilized to minimize the power consumption of the system. The bridge power-down switch is connected in series with the low side of the bridge. In normal operation, the switch is closed, and measurements can be taken. In applications in which current consumption is being minimized, the AD4195-4 can be placed in standby mode, which significantly reduces the power consumed in the application. In addition, the bridge power-down switch can be opened while in standby mode, which avoids unnecessary power consumption by the front-end transducer. Note that the bridge power-down switch can be opened or closed while in standby mode (setting the STB_PDSWn bit in Table 85 to 1 ensures that the switch stays active in standby mode). Therefore, the switch can be closed while in standby mode to allow the bridge to power up and settle as the front-end circuitry may need some time to settle before the ADC core is powered up and conversions are performed.

A typical procedure for reading the load cell is as follows:

1. Reset the ADC.
2. Set the CHANNEL_MAP0 register analog input to AIN5/AIN6. Assign Setup 0 to this channel through the CHANNEL_SETUP0 register. Configure Setup 0 to have a gain of 128 and select the reference source REFIN through the AFE0 register. Select the filter type through the FILTER0 register and set the output data rate through the FILTER_FS0 register.
3. Wait until $\overline{\text{RDY}}$ goes low. Read the conversion value.
4. Repeat step 3.

The AD4195-4 on-chip diagnostics allow the user to check the circuit connections, monitor the power supply, reference, and LDO voltages, check all conversions for any errors, as well as monitor any read/write operations. In weigh scale applications, the circuit connections are verified using the reference detect and the burnout currents. The REF_DIFF_MIN_ERR flag is set if the external reference REFIN is missing. The burnout currents (available in the MISC0 register) detect an open wire.

As part of the conversion process, the analog input overvoltage/undervoltage monitors are useful to detect any excessive voltages on AINP and AINM. The power supply voltages and reference voltages are selectable as inputs to the ADC. Therefore, the user can periodically check these voltages to confirm whether they are within the system specification. Also, the user can check the LDO voltages.

Finally, the CRC check, SCLK counter, and the SPI read/write checks make the interface more robust as any read/write operation that is not valid is detected. The CRC check highlights if any bits are corrupted when being transmitted between the processor and the ADC.

APPLICATIONS INFORMATION

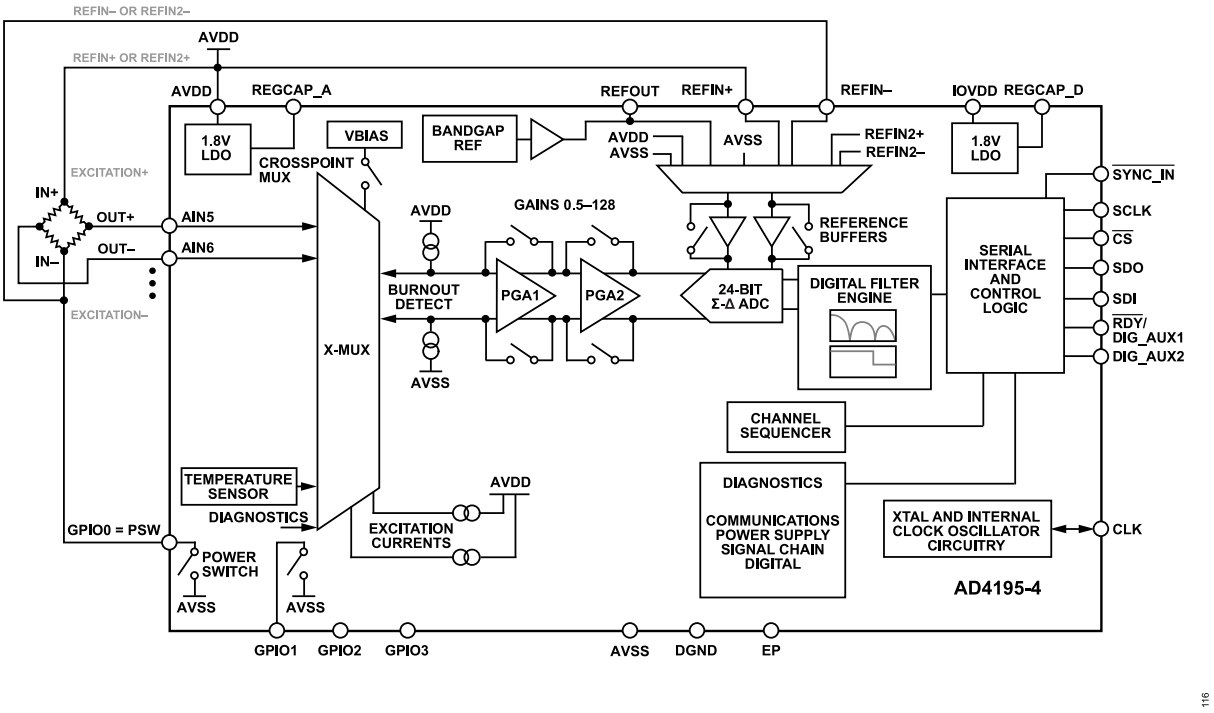

Figure 101. Weigh Scale Application

TEMPERATURE MEASUREMENT USING AN RTD

To optimize a 3-wire RTD configuration, two identically matched current sources are required. The AD4195-4, which contains two well matched current sources, is ideally suited to these applications. One possible 3-wire configuration is shown in Figure 102. In this 3-wire configuration, the lead resistances result in errors if only one current (output at GPIO3) is used, as the excitation current flows through RL1, which develop a voltage error between AIN0 and AIN1. In the scheme outlined, the second RTD current source (available at GPIO2) compensates for the error introduced by the excitation current flowing through RL1. The second RTD current flows through RL2. Assuming that RL1 and RL2 are equal (the leads are normally of the same material and of equal length) and that the excitation currents match, the error voltage across RL2 equals the error voltage across RL1, and no error voltage is developed between AIN0 and AIN1. Twice the voltage is developed across RL3. However, because this is a common-mode voltage, it does not introduce errors. The reference voltage for the AD4195-4 is also generated using the matched current sources. It is developed using a precision resistor and applied to the differential reference pins of the ADC. This scheme ensures that the analog input voltage span remains ratiometric to the reference voltage. Any errors in the analog input voltage due to the temperature drift of the excitation currents are compensated by the variation of the reference voltage.

As an example, the PT100 measures temperature from −200°C to +600°C. The resistance is 100Ω typically at 0°C and 313.71Ω at 600°C. If the 500µA excitation currents are used, the maximum voltage generated across the RTD when using the full temperature range of the RTD (ignoring the excitation current initial accuracy and excitation current temperature coefficient) is:

500µA × 313.71Ω = 156.86mV

This is amplified to 2.51V within the AD4195-4 if the gain is programmed to 16.

The voltage generated across the reference resistor must be at least 2.51V. Therefore, the reference resistor value must equal at least:

2.51V/500µA = 5020Ω

Therefore, a 5.11 kΩ resistor can be used as:

5.11kΩ × *Excitation Current* = 5.11kΩ × 500µA = 2.555V

One other consideration is the output compliance. The output compliance equals AVDD − 1.45V for the 500µA excitation current. If a 5V analog supply is used, the voltage at AIN0 must be less than (5V − 1.45V) = 3.55V. When the absolute voltage on an AIN pin is above 100mV, input leakage current is minimized, Therefore, a headroom resistor is shown in Figure 102. Assuming a 100Ω headroom resistor, the voltage on AIN1 is 100Ω × 2 × *Excitation Current* = 100Ω × 2 × 500µA = 0.1V. The output compliance specification is met because the maximum voltage at AIN0 equals the voltage across the reference resistor plus the voltage across the RTD plus the voltage across the headroom resistor, which equals:

2.555V + 156.86mV + 0.1V = 2.812V

APPLICATIONS INFORMATION

A typical procedure for reading the RTD is as follows:

1. Reset the ADC.
2. Set the CHANNEL_MAP0 register analog input to AIN0/AIN1. Assign Setup 0 to this channel through the CHANNEL_SETUP0 register. Configure Setup 0 to have a gain of 16 and select the reference source REFIN through the AFE0 register. Select the filter type through the FILTER0 register and set the output data rate through the FILTER_FS0 register.
3. Program the excitation currents to 500µA and output the currents on the GPIO2 and GPIO3 pins through the CURRENT_SOURCE0 and CURRENT_SOURCE1 registers.
4. Wait until $\overline{RDY}$ goes low. Read the conversion value.
5. Repeat step 4.

In the processor, implement the linearization routine for the PT100.

The external anti-alias filter is omitted for clarity. However, such a filter is required to reject any interference.

The AD4195-4 on-chip diagnostics allow the user to check the circuit connections, monitor the power supply, reference, and LDO voltages, check all conversions for any errors, as well as monitor any read/write operations. In RTD applications, the circuit connections are verified using the reference detect and the burnout currents. The REF_DIFF_MIN_ERR flag is set if the external reference REFIN is missing. The burnout currents can be enabled periodically (available in the MISC0 register) to detect an open wire. The burnout currents must be turned off when reading the conversions from AIN0/AIN1 for optimum system performance.

As part of the conversion process, the analog input overvoltage/undervoltage monitors are useful to detect any excessive voltages on AINP and AINM. The power supply voltages and reference voltage are selectable as inputs to the ADC. Therefore, the user can periodically check these voltages to confirm whether they are within the system specification. Also, the user can check the LDO voltages.

Finally, the CRC check, SCLK counter, and the SPI read/write checks make the interface more robust as any read/write operation that is not valid is detected. The CRC check highlights if any bits are corrupted when being transmitted between the processor and the ADC.

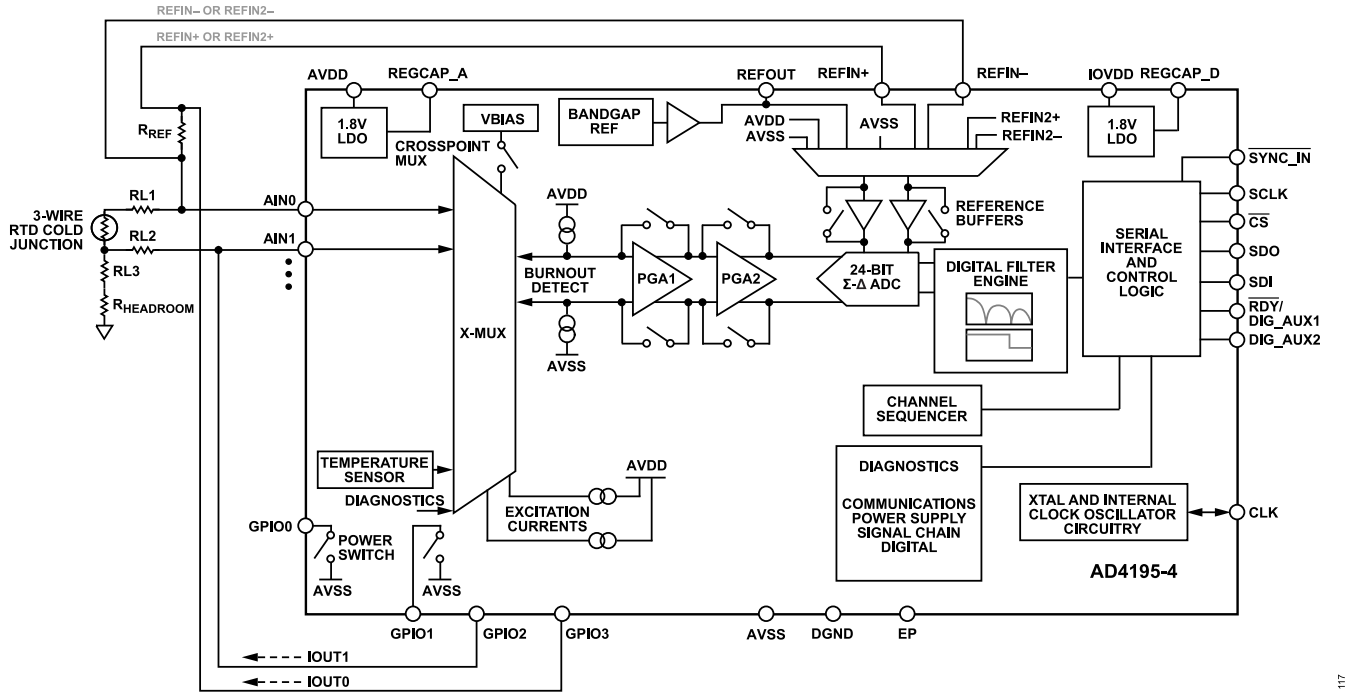

Figure 102. 3-Wire RTD Application

ON-CHIP REGISTER MAP

This section contains details about the functions of each of the bit fields. The access column in the register tables specifies whether the bit fields are read-only (R), read/write (R/W), or write-1-to-clear (R/W1C) bits.

Table 41. AD4195-4 Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET	RESERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			RESET_SW	0x10	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	RESERVED			SHORT_INSTRUCTION	RESERVED			0x80	R/W
0x02	DEVICE_CONFIG	[7:0]	RESERVED								0x00	R/W
0x03	CHIP_TYPE	[7:0]	RESERVED				CHIP_TYPE				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x48	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x04	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		VERSION						0x83	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x10	INTERFACE_CONFIG_C	[7:0]	CRC_ENABLE		STRICT_REGISTER_ACCESS	SEND_STATUS	ACTIVE_INTERFACE_MODE		CRC_ENABLEB		0x27	R/W
0x11	INTERFACE_STATUS_A	[7:0]	NOT_READY_ERR	RESERVED		CLOCK_COUNT_ERR	CRC_ERR	WR_TO_RD_ONLY_REG_ERR	REGISTER_PARTIAL_ACCESS_ERR	ADDRESS_INVALID_ERR	0x00	R/W
0x15	STATUS	[15:8]	RESERVED								0x0060	
0x14		[7:0]	MAIN_ERR_S	POR_FLAG_S	RDYB	RESERVED	CH_ACTIVE					
0x17	DATA_16B	[15:8]	ADC_DATA[15:8]								0x0000	
0x16		[7:0]	ADC_DATA[7:0]									
0x1A	DATA_16B_STATUS	[23:16]	ADC_DATA[15:8]								0x000060	
0x19		[15:8]	ADC_DATA[7:0]									
0x18		[7:0]	MAIN_ERR_S	POR_FLAG_S	RDYB	RESERVED	CH_ACTIVE					
0x1E	DATA_24B	[23:16]	ADC_DATA[23:16]								0x000000	
0x1D		[15:8]	ADC_DATA[15:8]									
0x1C		[7:0]	ADC_DATA[7:0]									
0x23	DATA_24B_STATUS	[31:24]	ADC_DATA[23:16]								0x00000060	
0x22		[23:16]	ADC_DATA[15:8]									
0x21		[15:8]	ADC_DATA[7:0]									
0x20		[7:0]	MAIN_ERR_S	POR_FLAG_S	RDYB	RESERVED	CH_ACTIVE					

ON-CHIP REGISTER MAP

Table 41. AD4195-4 Register Summary (Continued)

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x28 to 0x64 by 4	DATA_PER_CHANNELn	[23:16]	ADC_CH_DATA[23:16]								0x000000	
		[15:8]	ADC_CH_DATA[15:8]									
		[7:0]	ADC_CH_DATA[7:0]									
0x69	PIN_MUXING	[15:8]	RESERVED	CHAN_TO_GPIO	RESERVED						0x0004	R/W
0x68		[7:0]	DIG_AUX2_CTRL		DIG_AUX1_CTRL		SYNC_CTRL		DIG_OUT_STR	SDO_RDYB_DLY		
0x6B	CLOCK_CTRL	[15:8]	RESERVED								0x0000	R/W
0x6A		[7:0]	DCLK_DIVIDE		CLOCKDIV		RESERVED		CLOCKSEL			
0x6D	STANDBY_CTRL	[15:8]	RESERVED							STB_EN_CLOCK	0x0000	R/W
0x6C		[7:0]	STB_EN_IPULLUP	RESERVED		STB_PDSW1	STB_PDSW0	STB_EN_VBIAS	STB_EN_IEXC	STB_EN_REFERENCE		
0x6F	POWER_DOWN_SW	[15:8]	RESERVED								0x0000	R/W
0x6E		[7:0]	RESERVED						PDSW_1	PDSW_0		
0x71	ADC_CTRL	[15:8]	RESERVED								0x0000	R/W
0x70		[7:0]	MULTI_DATA_REG_SEL	CONT_READ_STATUS_EN	CONT_READ		MODE					
0x73	ERROR_EN	[15:8]	RESERVED		DLDO_PSM_ERR_EN	ALDO_PSM_ERR_EN	RESERVED	RESERVED	IOUTB_COMP_ERR_EN	IOUTA_COMP_ERR_EN	0x0000	R/W
0x72		[7:0]	REF_DIFF_MIN_ERR_EN	REF_OV_UV_ERR_EN	AINM_OV_UV_ERR_EN	AINP_OV_UV_ERR_EN	ADC_CONV_ERR_EN	SPI_ERR_EN	MM_CRC_ERR_EN	RESERVED		
0x75	ERROR	[15:8]	DEVICE_ERROR	RESERVED	DLDO_PSM_ERR	ALDO_PSM_ERR	RESERVED	RESERVED	IOUTB_COMP_ERR	IOUTA_COMP_ERR	0x0000	R/W
0x74		[7:0]	REF_DIFF_MIN_ERR	REF_OV_UV_ERR	AINM_OV_UV_ERR	AINP_OV_UV_ERR	ADC_CONV_ERR	SPI_ERR	MM_CRC_ERR	RESERVED		
0x79	CHANNEL_EN	[15:8]	CH_15	CH_14	CH_13	CH_12	CH_11	CH_10	CH_9	CH_8	0x0001	R/W
0x78		[7:0]	CH_7	CH_6	CH_5	CH_4	CH_3	CH_2	CH_1	CH_0		
0x80 to 0xBC by 4	CHANNEL_SETUPn	[15:8]	REPEAT								0x0000	R/W
		[7:0]	RESERVED	DELAY			RESERVED	SETUP				
0x82 to 0xBE by 4	CHANNEL_MAPn	[15:8]	RESERVED			AINP_N					0x0001	R/W
		[7:0]	RESERVED			AINM_N						
0xC0 to 0x122 by 14	MISCn	[15:8]	CHOP_IEXC		RESERVED				CHOP_ADC		0x0000	R/W
		[7:0]	RESERVED						BURNOUT			
0xC2 to 0x124 by 14	AFEn	[15:8]	RESERVED				REF_BUF_M		REF_BUF_P		0x0050	R/W

ON-CHIP REGISTER MAP

Table 41. AD4195-4 Register Summary (Continued)

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
		[7:0]	RESERVED	REF_SELECT		BIPOLAR	PGA_GAIN					
0xC4 to 0x126 by 14	FILTERn	[15:8]	RESERVED								0x0000	R/W
		[7:0]	POST_FILTER_SEL				FILTER_TYPE					
0xC6 to 0x128 by 14	FILTER_FSn	[15:8]	FS[15:8]								0x0004	R/W
		[7:0]	FS[7:0]									
0xC8 to 0x12A by 14	OFFSETn	[23:16]	OFFSET[23:16]								0x000000	R/W
		[15:8]	OFFSET[15:8]									
		[7:0]	OFFSET[7:0]									
0xCB to 0x12D by 14	GAINn	[23:16]	GAIN[23:16]								0x555555	R/W
		[15:8]	GAIN[15:8]									
		[7:0]	GAIN[7:0]									
0x131	REF_CONTROL	[15:8]	RESERVED								0x0001	R/W
0x130		[7:0]	RESERVED							REF_EN		
0x135	V_BIAS	[15:8]	RESERVED							VBIAS_IN8_EN	0x0000	R/W
0x134		[7:0]	VBIAS_IN7_EN	VBIAS_IN6_EN	VBIAS_IN5_EN	VBIAS_IN4_EN	VBIAS_IN3_EN	VBIAS_IN2_EN	VBIAS_IN1_EN	VBIAS_IN0_EN		
0x137	I_PULLUP	[15:8]	RESERVED							I_PULLUP_IN8_EN	0x0000	R/W
0x136		[7:0]	I_PULLUP_IN7_EN	I_PULLUP_IN6_EN	I_PULLUP_IN5_EN	I_PULLUP_IN4_EN	I_PULLUP_IN3_EN	I_PULLUP_IN2_EN	I_PULLUP_IN1_EN	I_PULLUP_IN0_EN		
0x138 to 0x13E by 2	CURRENT_SOURCEn	[15:8]	RESERVED			I_OUT_PIN					0x0000	R/W
		[7:0]	RESERVED					I_OUT_VAL				
0x191	GPIO_MODE	[15:8]	RESERVED								0x0000	R/W
0x190		[7:0]	CH3_MODE		CH2_MODE		CH1_MODE		CH0_MODE			
0x193	GPIO_OUTPUT_DATA	[15:8]	RESERVED								0x0000	R/W
0x192		[7:0]	RESERVED				CH3_OUTPUT	CH2_OUTPUT	CH1_OUTPUT	CH0_OUTPUT		
0x195	INPUT_DATA	[15:8]	RESERVED								0x0000	R
0x194		[7:0]	RESERVED				CH3_INPUT	CH2_INPUT	CH1_INPUT	CH0_INPUT		

ON-CHIP REGISTER MAP

INTERFACE_CONFIG_A REGISTER

Address: 0x00, Reset: 0x10

The operation of the serial interface is configured in this register.

Table 42. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SW_RESET	RESERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			RESET_SW

Table 43. Bit Descriptions for INTERFACE_CONFIG_A Register

Bits	Bit Name	Settings	Description	Reset	Access
7	SW_RESET		First of Two Software Reset Bits. This bit appears in two locations in this register. Both locations must be set to 1 at the same time to trigger a software reset of the part. All registers except this register are reset to their default values. Bits SW_RESET and RESET_SW are reset to 0 by the reset operation.	0x0	R/W
6	RESERVED		Reserved.	0x0	R
5	ADDR_ASCENSION		Determines Sequential Addressing Behavior.	0x0	R/W
		0	Address accessed is decremented by one for each data byte when accessing multibyte registers.		
		1	Address accessed is incremented by one for each data byte when accessing multibyte registers.		
4	SDO_ENABLE		SDO Pin Enable.	0x1	R
[3:1]	RESERVED		Reserved.	0x0	R
0	RESET_SW		Second of Two Software Reset Bits. This bit appears in two locations in this register. Both locations must be set to 1 at the same time to trigger a software reset of the part. All registers except this register are reset to their default values. Bits SW_RESET and RESET_SW are reset to 0 by the reset operation.	0x0	R/W

INTERFACE_CONFIG_B REGISTER

Address: 0x01, Reset: 0x80

The operation of the serial interface is configured in this register.

Table 44. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SINGLE_INST	RESERVED			SHORT_INSTRUCTION	RESERVED		

Table 45. Bit Descriptions for INTERFACE_CONFIG_B Register

Bits	Bit Name	Settings	Description	Reset	Access
7	SINGLE_INST		Single Instruction Mode.	0x1	R
		1	Single instruction mode is enabled.		
[6:4]	RESERVED		Reserved.	0x0	R
3	SHORT_INSTRUCTION		Set the instruction phase address to 6- or 14-bits.	0x0	R/W
		0	14-bit Addressing.		
		1	6-bit Addressing.		
[2:0]	RESERVED		Reserved.	0x0	R

DEVICE_CONFIG REGISTER

Address: 0x02, Reset: 0x00

ON-CHIP REGISTER MAP

This is a read only register.

Table 46. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							

Table 47. Bit Descriptions for DEVICE_CONFIG Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	RESERVED		Reserved.	0x0	R

CHIP_TYPE REGISTER

Address: 0x03, Reset: 0x07

The chip type is used to identify the family of ADI devices a given device belongs to. It must be used in conjunction with the Product ID to uniquely identify a given product.

Table 48. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED				CHIP_TYPE			

Table 49. Bit Descriptions for CHIP_TYPE Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
[3:0]	CHIP_TYPE		Precision ADC.	0x7	R

PRODUCT_ID_L REGISTER

Address: 0x04, Reset: 0x4C

This register contains the low byte of the Product ID.

Table 50. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRODUCT_ID[7:0]							

Table 51. Bit Descriptions for PRODUCT_ID_L Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]		This is Device Chip Type/Family. The product ID must be used in conjunction with the CHIP_TYPE register to identify a product.	0x4C	R

PRODUCT_ID_H REGISTER

Address: 0x05, Reset: 0x00

This register contains the high byte of the Product ID.

Table 52. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRODUCT_ID[15:8]							

Table 53. Bit Descriptions for PRODUCT_ID_H Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]		This is Device Chip Type/Family. The product ID must be used in conjunction with the CHIP_TYPE register to identify a product.	0x0	R

ON-CHIP REGISTER MAP

CHIP_GRADE REGISTER

Address: 0x06, Reset: 0x04

This register identifies the product variations and device revision.

Table 54. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GRADE				DEVICE_REVISION			

Table 55. Bit Descriptions for CHIP_GRADE Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	GRADE		This is the Device Performance Grade.	0x0	R
[3:0]	DEVICE_REVISION		This is the Device Hardware Revision.	0x4	R

SCRATCH_PAD REGISTER

Address: 0x0A, Reset: 0x00

This register can be used to test write and read operations between the processor and the AD4195-4.

Table 56. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCRATCH_VALUE							

Table 57. Bit Descriptions for SCRATCH_PAD Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SCRATCH_VALUE		Software Scratchpad. Software can write to and read from this location without any device side effects.	0x0	R/W

SPI_REVISION REGISTER

Address: 0x0B, Reset: 0x83

Indicates the SPI interface revision.

Table 58. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI_TYPE		VERSION					

Table 59. Bit Descriptions for SPI_REVISION Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SPI_TYPE		Analog Devices SPI type.	0x2	R
[5:0]	VERSION		Analog Devices SPI Version.	0x3	R

VENDOR_L REGISTER

Address: 0x0C, Reset: 0x56

The low byte of the Vendor ID is stored in this register.

Table 60. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VID[7:0]							

ON-CHIP REGISTER MAP

Table 61. Bit Descriptions for VENDOR_L Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VID[7:0]		Analog Devices Vendor ID.	0x56	R

VENDOR_H REGISTER

Address: 0x0D, Reset: 0x04

The high byte of the Vendor ID is stored in this register.

Table 62. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VID[15:8]							

Table 63. Bit Descriptions for VENDOR_ H Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VID[15:8]		Analog Devices Vendor ID.	0x4	R

INTERFACE_CONFIG_C REGISTER

Address: 0x10, Reset: 0x27

The serial interface is configured using this register.

Table 64. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRC_ENABLE		STRICT_REGISTER_ACCESS	SEND_STATUS	ACTIVE_INTERFACE_MODE		CRC_ENABLEB	

Table 65. Bit Descriptions for INTERFACE_CONFIG_C Register

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CRC_ENABLE		CRC Enable. These bits enable/disable CRC on the serial interface. The CRC_ENABLEB bits must also be written with the inverted value of the CRC_ENABLE bits for CRC to be enabled/disabled. Settings not listed are reserved.	0x0	R/W
		00	CRC Disabled.		
		01	CRC Enabled.		
5	STRICT_REGISTER_ACCESS		Multibyte Registers Must Be Read/Written in Full. When this mode is enabled, all bytes of a multibyte register must be read/written in full.	0x1	R
		1	Strict mode, multibyte registers require all bytes read/written.		
4	SEND_STATUS		Enables sending of synchronization pattern on SDO during every instruction phase. When cleared, a fixed synchronization pattern of 0x2645 is sent when a 16-bit instruction is used while the pattern is 0x26 for 8-bit instructions. When set, no synchronization pattern is sent during the instruction phase.	0x0	R/W
[3:2]	ACTIVE_INTERFACE_MODE	1	This is the active mode that the SPI interface is operating in.	0x1	R
[1:0]	CRC_ENABLEB		Inverted CRC Enable. This must be written with the inverted value of the CRC_ENABLE setting.	0x3	R/W

INTERFACE_STATUS_A REGISTER

Address: 0x11, Reset: 0x00

This register indicates the status of all read and write operations. The appropriate bit is set to 1 if an error occurs. Set bits are cleared by writing a 1 to the corresponding bit location.

ON-CHIP REGISTER MAP

Table 66. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NOT_READY_ERR	RESERVED		CLOCK_COUNT_ERR	CRC_ERR	WR_TO_RD_ONLY_REG_ERR	REGISTER_PARTIAL_ACCESS_ERR	ADDRESS_INVALID_ERR

Table 67. Bit Descriptions for INTERFACE_STATUS_A Register

Bits	Bit Name	Settings	Description	Reset	Access
7	NOT_READY_ERR		Device Not Ready for Transaction. This error bit is set if the user attempts to execute an SPI transaction before the completion of the digital initialization.	0x0	R/W1C
[6:5]	RESERVED		Reserved.	0x0	R
4	CLOCK_COUNT_ERR		Set if an incorrect number of clock pulses is detected in a transaction. $\overline{CS}$ must be used to frame the transactions for this error check.	0x0	R/W1C
3	CRC_ERR		Invalid/No CRC Received. This is set when the processor fails to send a CRC or when the AD4195-4 calculates and checks the CRC and finds the CRC value is incorrect.	0x0	R/W1C
2	WR_TO_RD_ONLY_REG_ERR		Write to Read-Only Register Attempted. This is set when a write to a register that is read-only is attempted.	0x0	R/W1C
1	REGISTER_PARTIAL_ACCESS_ERR		Set when fewer than the expected number of bytes is read/written. This bit is only valid when strict register access is enabled.	0x0	R/W1C
0	ADDRESS_INVALID_ERR		Attempt to Read/Write Non-existent Register Address.	0x0	R/W1C

STATUS REGISTER

Address: 0x14/0x15 (low/high byte), Reset: 0x0060

The STATUS register contains ADC and serial interface status information.

Table 68. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
MAIN_ERR_S	POR_FLAG_S	RDYB	RESERVED	CH_ACTIVE			

Table 69. Bit Descriptions for STATUS Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED		Reserved.	0x0	R
7	MAIN_ERR_S		Set if any of the enabled error flags in the ERROR register are set.	0x0	R
6	POR_FLAG_S		Set when a power-on reset or a reset via register or reset sequence has occurred.	0x1	R/W1C
5	RDYB		ADC Conversion Ready Indicator.	0x1	R
4	RESERVED		Reserved.	0x0	R
[3:0]	CH_ACTIVE		Indicates active channel for previous conversion.	0x0	R

DATA_16B REGISTER

Address: 0x16/0x17 (low/high byte), Reset: 0x0000

The 16-bit conversion result is stored in this register when all enabled channels use a single data register.

Table 70. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC_DATA[15:8]							
ADC_DATA[7:0]							

ON-CHIP REGISTER MAP

Table 71. Bit Descriptions for DATA_16B Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	ADC_DATA[15:0]		16-bit ADC Conversion Result.	0x0	R

DATA_16B_STATUS REGISTER

Address: 0x18/0x19/0x1A (low/mid/high byte), Reset: 0x000060

This register contains the status bits along with the 16-bit conversion result. The conversion result and status bits can be read from this register when all enabled channels share a data register.

Table 72. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC_DATA[15:8]							
ADC_DATA[7:0]							
MAIN_ERR_S	POR_FLAG_S	RDYB	RESERVED	CH_ACTIVE			

Table 73. Bit Descriptions for DATA_16B_STATUS Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:8]	ADC_DATA[15:0]		16-bit ADC Conversion Result (16MSBs of the 24-bit Conversion Result).	0x0	R
7	MAIN_ERR_S		Set if any of the enabled error flags in the ERROR register are set.	0x0	R
6	POR_FLAG_S		Set when a power-on reset or a reset by register or reset sequence has occurred.	0x1	R/W1C
5	RDYB		ADC Conversion Ready Indicator.	0x1	R
4	RESERVED		Reserved.	0x0	R
[3:0]	CH_ACTIVE		Indicates active channel for previous conversion.	0x0	R

DATA_24B REGISTER

Address: 0x1C/0x1D/0x1E (low/mid/high byte), Reset: 0x000000

The 24-bit conversion result is stored in this register when all enabled channels use a single data register.

Table 74. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC_DATA[23:16]							
ADC_DATA[15:8]							
ADC_DATA[7:0]							

Table 75. Bit Descriptions for DATA_24B Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	ADC_DATA[23:0]		24-bit ADC Conversion Result.	0x0	R

DATA_24B_STATUS REGISTER

Address: 0x20 (low byte) to 0x23 (high byte), Reset: 0x00000060

This register contains the status bits along with the 24-bit conversion result. The conversion result and status bits can be read from this register when all enabled channels share a data register.

Table 76. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC_DATA[23:16]							
ADC_DATA[15:8]							
ADC_DATA[7:0]]							

ON-CHIP REGISTER MAP

Table 76. Bit Names (Continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MAIN_ERR_S	POR_FLAG_S	RDYB	RESERVED	CH_ACTIVE			

Table 77. Bit Descriptions for DATA_24B_STATUS Register

Bits	Bit Name	Settings	Description	Reset	Access
[31:8]	ADC_DATA[23:0]		24-bit ADC Result.	0x0	R
7	MAIN_ERR_S		Set if any of the enabled error flags in the ERROR register are set.	0x0	R
6	POR_FLAG_S		Set when a power-on reset or a reset by register or reset sequence has occurred.	0x1	R/W1C
5	RDYB		ADC Conversion Ready Indicator.	0x1	R
4	RESERVED		Reserved.	0x0	R
[3:0]	CH_ACTIVE		Indicates active channel for previous conversion.	0x0	R

DATA_PER_CHANNEL REGISTER

Address: 0x28 (low byte of Channel 0) to 0x64 (high byte of Channel 15) in increments of 4, Reset: 0x000000

If data per channel capability is enabled, the conversion results from the enabled channels are available using the DATA_PER_CHANNELn registers. DATA_PER_CHANNEL0 contains the conversion result from Channel 0 while DATA_PER_CHANNEL15 holds the conversion result from Channel 15.

Table 78. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC_CH_DATA[23:16]							
ADC_CH_DATA[15:8]							
ADC_CH_DATA[7:0]							

Table 79. Bit Descriptions for DATA_PER_CHANNELn Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	ADC_CH_DATA		Conversion result from the corresponding channel.	0x0	R

PIN_MUXING REGISTER

Address: 0x68/0x69 (low/high byte), Reset: 0x0004

This register contains synchronization options. Also, the operation of the SDO pin can be configured. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 80. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	CHAN_TO_GPIO	RESERVED					
DIG_AUX2_CTRL		DIG_AUX1_CTRL		SYNC_CTRL		DIG_OUT_STR	SDO_RDYB_DLY

Table 81. Bit Descriptions for PIN_MUXING Register

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		Reserved.	0x0	R
14	CHAN_TO_GPIO		Current channel number output to GPIO pins. This bit enables the current ADC channel number to be output to the GPIO pins. This allows control of an external multiplexer while the ADC sequences through multiple channels. GPIO3 operates as the MSB with GPIO0 operating as the LSB, which supports up to 16 possible channels. Other shared functions of the GPIO pins may affect the functionality of this feature.	0x0	R/W
		0	Active channel number is not output to GPIO pins.		
		1	Active channel number is output to GPIO pins.		
[13:8]	RESERVED		Reserved.	0x0	R

ON-CHIP REGISTER MAP

Table 81. Bit Descriptions for PIN_MUXING Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DIG_AUX2_CTRL		Configures functionality of pin DIG_AUX2. When continuous transmit is enabled, DIG_AUX2 functions as DCLK.	0x0	R/W
		00	DIG_AUX2 Pin Disabled. High Impedance.		
		01	Reserved.		
		10	DIG_AUX2 Pin Configured as START Input. This must be used in conjunction with the SYNC_OUT functionality of DIG_AUX1. SYNC_OUT outputs a synchronized version of the START signal. SYNC_OUT can drive the $\overline{\text{SYNC\_IN}}$ pin of multiple AD4195-4 devices to force synchronization of all the devices. For main clock divide by 2, the signal is output to SYNC_OUT after 3 to 4 positive MCLK edges. For MCLK divide by 4, the delay is 5 to 8 MCLK positive edges. For MCLK divide by 8, the delay is 9 to 16 MCLK positive edges.		
		11	Reserved.		
[5:4]	DIG_AUX1_CTRL		Configures functionality of pin DIG_AUX1.	0x0	R/W
		00	DIG_AUX1 Pin Disabled. High impedance.		
		01	DIG_AUX1 Pin Configured as ADC Data Ready Output ($\overline{\text{RDY}}$). This configures DIG_AUX1 as an active-low ADC Data-Ready indicator. This disables the shared $\overline{\text{RDY}}$ function on SDO.		
		10	DIG_AUX1 Pin Configured as SYNC_OUT Output. This must be used in conjunction with the START functionality of DIG_AUX2.		
		11	Reserved.		
[3:2]	SYNC_CTRL		Configures the $\overline{\text{SYNC\_IN}}$ Pin for ADC Synchronization.	0x1	R/W
		00	$\overline{\text{SYNC\_IN}}$ Pin Disabled.		
		01	$\overline{\text{SYNC\_IN}}$ Has Default Synchronization Functionality. $\overline{\text{SYNC\_IN}}$ is an active low input. Taking $\overline{\text{SYNC\_IN}}$ low holds the modulator, digital filter, and control logic in a reset state. This includes resetting the state of the channel sequencer.		
		10	$\overline{\text{SYNC\_IN}}$ Has Alternative Synchronization Functionality. The alternate synchronization functionality is only relevant if multiple channels are enabled in the sequencer. Taking $\overline{\text{SYNC\_IN}}$ low prevents the sequencer from advancing to the next channel in the sequence. The sequencer only advances to the next channel in the sequence when $\overline{\text{SYNC\_IN}}$ is taken high. This allows external control of the start of ADC sampling for a channel without resetting the state of the sequencer.		
		11	Reserved.		
1	DIG_OUT_STR		Digital Output Driver Strength. This bit can be used to increase the drive strength of the digital outputs. This can improve SPI timing at lower values of IOVDD.	0x0	R/W
		0	Default Drive Strength. Recommended for higher IOVDD voltages.		
		1	Increased Drive Strength.		
0	SDO_RDYB_DLY		Reset Interface on $\overline{\text{CS}}$ or SCLK rising edge. This bit determines whether a shared SDO/$\overline{\text{RDY}}$ pin returns to functioning as a $\overline{\text{RDY}}$ pin after the last SCLK of a register read or on a rising edge of $\overline{\text{CS}}$. It has no effect if $\overline{\text{RDY}}$ is output on the DIG_AUX1 pin.	0x0	R/W
		0	Reset on last SCLK rising edge.		
		1	Reset on $\overline{\text{CS}}$ rising edge.		

CLOCK_CTRL REGISTER

Address: 0x6A/0x6B (low/high byte), Reset: 0x0000

The main clock source and the internal divide factor is selected using this register. The frequency of DCLK for continuous transmit mode is also set using this register. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 82. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
DCLK_DIVIDE		CLOCKDIV		RESERVED		CLOCKSEL	

ON-CHIP REGISTER MAP

Table 83. Bit Descriptions for CLOCK_CTRL Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED		Reserved.	0x0	R
[7:6]	DCLK_DIVIDE		Continuous Transmit Data Clock Divider. These bits allow adjustment of the data clock used in the continuous transmit mode. The data clock is based off the selected main clock, with an optional divide-down.	0x0	R/W
		00	DCLK Equals Main Clock Divide by 1.		
		01	DCLK Equals Main Clock Divide by 2.		
		10	DCLK Equals Main Clock Divide by 4.		
		11	DCLK Equals Main Clock Divide by 8.		
[5:4]	CLOCKDIV		Main Clock Divider. These bits allow a programmable divider of the external or internal clock frequency.	0x0	R/W
		00	Divide by 2.		
		01	Divide by 2.		
		10	Divide by 4.		
		11	Divide by 8.		
[3:2]	RESERVED		Reserved.	0x0	R
[1:0]	CLOCKSEL		ADC Clock Select. These bits are used to select the ADC clock source. Selecting the internal oscillator powers up the oscillator.	0x0	R/W
		00	Internal Oscillator.		
		01	Internal Oscillator, Output to CLK Pin.		
		10	External Clock Input on CLK Pin.		
		11	Reserved.		

STANDBY_CTRL REGISTER

Address: 0x6C/0x6D (low/high byte), Reset: 0x0000

Functions such as the main clock, internal pull-ups, power-down switches, VBIAS, excitation currents, and the internal reference can remain enabled during standby. The functions to remain enabled in standby are selected using this register. The functions must be individually enabled in their respective control registers for the bits in this register to have any effect.

Table 84. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							STB_EN_CLOCK
STB_EN_IPULLUP	RESERVED		STB_PDSW1	STB_PDSW0	STB_EN_VBIAS	STB_EN_IEXC	STB_EN_REFERENCE

Table 85. Bit Descriptions for STANDBY_CTRL Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	RESERVED		Reserved.	0x0	R
8	STB_EN_CLOCK		When set, the main clock remains active in standby mode.	0x0	R/W
7	STB_EN_IPULLUP		When set, the pull-up currents remain active in standby mode.	0x0	R/W
[6:5]	RESERVED		Reserved.	0x0	R
4	STB_PDSW1		When set, PSW1 remains active in standby mode.	0x0	R/W
3	STB_PDSW0		When set, PSW0 remains active in standby mode.	0x0	R/W
2	STB_EN_VBIAS		When set, VBIAS remains active in standby mode.	0x0	R/W
1	STB_EN_IEXC		When set, the internal excitation currents remain active in standby mode.	0x0	R/W
0	STB_EN_REFERENCE		When set, the internal reference remains active in standby mode. The internal reference must remain enabled if the excitation currents remain active in standby mode.	0x0	R/W

POWER_DOWN_SW REGISTER

Address: 0x6E/0x6F (low/high byte), Reset: 0x0000

ON-CHIP REGISTER MAP

The low-side power switches are enabled/disabled using this register. The two power switches are available on GPIO0 (PDSW0) and GPIO1(PDSW1).

Table 86. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
RESERVED						PDSW_1	PDSW_0

Table 87. Bit Descriptions for POWER_DOWN_SW Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:2]	RESERVED		Reserved.	0x0	R
1	PDSW_1		PDSW1 Pin Enable.	0x0	R/W
		0	Disable PDSW1 Switch on GPIO1 to AVSS.		
		1	Enable PDSW1 Switch on GPIO1 to AVSS.		
0	PDSW_0		PDSW0 Pin Enable.	0x0	R/W
		0	Disable PDSW0 Switch on GPIO0 to AVSS.		
		1	Enable PDSW0 Switch on GPIO0 to AVSS.		

ADC_CTRL REGISTER

Address: 0x70/0x71 (low/high byte), Reset: 0x0000

The mode of operation is set using this register. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 88. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
MULTI_DATA_REG_SEL	CONT_READ_STATUS_EN	CONT_READ		MODE			

Table 89. Bit Descriptions for ADC_CTRL Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED		Reserved.	0x0	R
7	MULTI_DATA_REG_SEL		Selects Between One or Multiple Data Registers. Channels can be configured to share a common data register (with optional status byte) or have separate data registers addressed individually over SPI. The $\overline{RDY}$ behavior for multichannel sequences changes depending on which option is selected.	0x0	R/W
		0	Each Channel Has Its Own Data Register. Each enabled ADC channel has its result written into a dedicated data register. These registers can be individually addressed over the serial interface. In this configuration, $\overline{RDY}$ is asserted after all enabled channels in a sequence have completed ADC conversions. This allows the results for all data registers to be read after a single interrupt to the host. The REPEAT function is not allowed when this feature is enabled.		
		1	Channels Share Data Register. $\overline{RDY}$ asserts after each channel. All enabled ADC channels share a common ADC data register. A status byte can optionally be obtained with the conversion by addressing the relevant register. In this configuration, $\overline{RDY}$ is asserted after any channel in a sequence completes a conversion. The conversion must be read before the next conversion is available as the data register is updated with the new conversion result once it is available.		
6	CONT_READ_STATUS_EN		Enables Status Output in Continuous Read/Transmit. This bit determines whether a status byte is output with the conversion when continuous read or continuous transmit is enabled. In continuous read, the status byte follows immediately after the conversion. In continuous transmit, the status byte is the first byte transmitted. It is repeated in the second slot if CRC is enabled.	0x0	R/W
		0	Status byte is not output.		

ON-CHIP REGISTER MAP

Table 89. Bit Descriptions for ADC_CTRL Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		1	Status byte is output. $\overline{CS}$ must be kept low for the entire data + status read.		
[5:4]	CONT_READ		Continuous Data Register Read/Transmit Enable. This enables continuous read or continuous transmit of the ADC data register. The ADC must be in a continuous conversion mode.	0x0	R/W
		00	Disable Continuous Read/Transmit.		
		01	Enable Continuous Read. This enables continuous read of the ADC data register. The ADC must be in a continuous conversion mode. In continuous read, only reads of the ADC DATA register can be performed over the SPI interface, and an instruction byte is not required to address the data register. If a data register read takes too long, the read is aborted shortly before the next ADC conversion result is due to be written into the data register. To exit continuous read, write the command 0xA5 to the SPI interface as the first byte of data after $\overline{RDY}$ goes low. Alternatively, a serial interface reset can be performed at any time by writing a pattern of 63 1s and one 0 three times to the ADC. Note that a reset by writing to the INTERFACE_CONFIG_A register is not an option to exit continuous read.		
		10	Enable Continuous Transmit. This enables continuous transmit of the ADC data register. The ADC must be in a continuous conversion mode. In this mode, ADC data is automatically transmitted on SDO when a new conversion result becomes available, using the DIG_AUX2 pin as a data clock, DCLK. Pin DIG_AUX1 is automatically used as a Frame-Sync. Other functions of DIG_AUX1 and DIG_AUX2 are automatically disabled. The data frame consists of one or two 32-bit slots. The ADC status register and a CRC byte is included if enabled. CRC requires the use of the second slot. The data clock, DCLK, is derived from the main clock, with an optional additional divide. The divide factor must allow sufficient DCLKs for the transmission to complete before the next ADC result. The SPI serial clock, SCLK, is not used for the ADC data transmission in this mode. Register reads are not possible because the SDO pin is used exclusively to transmit ADC data. To exit continuous transmit, write to this register and set the CONT_READ bits to 0. Alternatively, a serial interface reset (writing 63 1s and one 0 three times to the ADC) can be performed at any time.		
		11	Reserved.		
[3:0]	MODE		ADC Operating Mode. These bits control the operating mode of the ADC. Settings not listed are reserved.	0x0	R/W
		0000	Continuous Conversion Mode (Default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. $\overline{RDY}$ goes low when a conversion is complete. The user can read these conversions by reading the appropriate register or by enabling the continuous read or continuous transmit options.		
		0100	Single Conversion Mode. The ADC performs a single conversion (possibly repeated) on each enabled channel(s). The ADC enters standby on completion of the conversion(s).		
		0101	Standby Mode. By default, all sections of the AD4195-4 are powered down except the LDOs and the serial interface. The on-chip registers retain their contents in standby mode. Functions such as the internal reference, bias voltage generator, excitation currents, and on-chip oscillator can remain enabled in standby mode. The state of these functions in standby mode is controlled using the STANDBY_CTRL register.		
		0110	Power-Down Mode. In power-down mode, all the circuitry is powered down. The LDOs are also powered down. The on-chip registers do not retain their contents. Therefore, coming out of power-down mode, all registers must be reprogrammed. To enter power-down mode, the device must first be placed in standby mode. To exit power-down mode, a serial interface reset by writing 63 1s and one 0 to the ADC three times is required.		
		0111	Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state even though the modulator clocks continue to be provided.		

ON-CHIP REGISTER MAP

Table 89. Bit Descriptions for ADC_CTRL Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		1000	System Zero-Scale (Offset) Calibration. Connect the system zero-scale input to the channel input pins of the selected channel. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. Select only one channel when full-scale calibration is being performed.		
		1001	System Full-Scale (Gain) Calibration. Connect the system full-scale input to the channel input pins of the selected channel. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the gain register of the selected channel. Select only one channel when full-scale calibration is being performed.		
		1010	Internal Zero-Scale (Offset) Calibration. An internal short is automatically connected to the input. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. Select only one channel when zero-scale calibration is being performed.		

ERROR_EN REGISTER

Address: 0x72/0x73 (low/high byte), Reset: 0x0000

All the diagnostic functions can be enabled or disabled by setting the appropriate bits in this register. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 90. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED		DLDO_PSM_ERR_EN	ALDO_PSM_ERR_EN	RESERVED		IOUT1_COMP_ERR_EN	IOUT0_COMP_ERR_EN
REF_DIFF_MIN_ERR_EN	REF_OV_UV_ERR_EN	AINM_OV_UV_ERR_EN	AINP_OV_UV_ERR_EN	ADC_CONV_ERR_EN	SPI_ERR_EN	MM_CRC_ERR_EN	RESERVED

Table 91. Bit Descriptions for ERROR_EN Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	RESERVED		Reserved.	0x0	R
13	DLDO_PSM_ERR_EN		When this bit is set, the digital LDO voltage is continuously monitored. The DLDO_PSM_ERR bit in the error register is set if the voltage being output from the digital LDO is less than 1.6V typically.	0x0	R/W
12	ALDO_PSM_ERR_EN		When this bit is set, the analog LDO voltage is continuously monitored. The ALDO_PSM_ERR bit in the error register is set if the voltage being output from the analog LDO is less than 1.5V typically.	0x0	R/W
[11:10]	RESERVED		Reserved	0x0	R
9	IOUT1_COMP_ERR_EN		When this bit is set, excitation current IOUT1 is continuously monitored. The IOUT1_COMP_ERR bit in the error register is set if the current magnitude decreases.	0x0	R/W
8	IOUT0_COMP_ERR_EN		When this bit is set, excitation current IOUT0 is continuously monitored. The IOUT0_COMP_ERR bit in the error register is set if the current magnitude decreases.	0x0	R/W
7	REF_DIFF_MIN_ERR_EN		When this bit is set, the differential voltage on the selected reference source is monitored. If the voltage is less than the specified value, the REF_DIFF_MIN_ERR bit in the error register is set.	0x0	R/W
6	REF_OV_UV_ERR_EN		When this bit is set, the overvoltage/undervoltage monitor on the REFINn+ pin of the channel being converted is enabled.	0x0	R/W

ON-CHIP REGISTER MAP

Table 91. Bit Descriptions for ERROR_EN Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
5	AINM_OV_UV_ERR_EN		When this bit is set, the overvoltage/undervoltage monitor on the AINM pin of the channel being converted is enabled.	0x0	R/W
4	AINP_OV_UV_ERR_EN		When this bit is set, the overvoltage/undervoltage monitor on the AINP pin of the channel being converted is enabled.	0x0	R/W
3	ADC_CONV_ERR_EN		When this bit is set, the conversions are monitored and the ADC_CONV_ERR bit is set if the analog input is over-range or under-range.	0x0	R/W
2	SPI_ERR_EN		SPI Error Enable. This bit controls whether an SPI interface error (INTERFACE_STATUS_A register) also asserts the SPI_ERR bit in the ERROR register.	0x0	R/W
1	MM_CRC_ERR_EN		When this bit is set, a CRC calculation is performed on the memory map. Following this, periodic CRC checks are performed on the on-chip registers. If the register contents have changed due to register corruption or further register writes, the MM_CRC_ERR bit is set.	0x0	R/W
0	RESERVED		Reserved.	0x0	R

ERROR REGISTER

Address: 0x74/0x75 (low/high byte), Reset: 0x0000

Diagnostics such as checking overvoltages, undervoltages, and the SPI interface, are included on the AD4195-4. The ERROR register contains the flags for the different diagnostic functions. The functions can be enabled or disabled using the ERROR_EN register. Error status flags are set to 1 if an error is detected. Error status flags can be cleared by writing a 1 to the relevant bit of this register, provided the error condition no longer exists.

Table 92. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEVICE_ERROR	RESERVED	DLDO_PSM_ERR	ALDO_PSM_ERR	RESERVED		IOUT1_COMP_ERR	IOUT0_COMP_ERR
REF_DIFF_MIN_ERR	REF_OV_UV_ERR	AINM_OV_UV_ERR	AINP_OV_UV_ERR	ADC_CONV_ERR	SPI_ERR	MM_CRC_ERR	RESERVED

Table 93. Bit Descriptions for ERROR Register

Bits	Bit Name	Settings	Description	Reset	Access
15	DEVICE_ERROR		Device Initialization Status Bit. A device reset is recommended if this bit is set. This bit cannot be cleared.	0x0	R
14	RESERVED		Reserved.	0x0	R
13	DLDO_PSM_ERR		Digital LDO Status Bit.	0x0	R/W1C
12	ALDO_PSM_ERR		Analog LDO Status Bit.	0x0	R/W1C
[11:10]	RESERVED		Reserved.	0x0	R
9	IOUT1_COMP_ERR		Compliance Voltage Error for IOUT1 Status Bit.	0x0	R/W1C
8	IOUT0_COMP_ERR		Compliance Voltage Error for IOUT0 Status Bit.	0x0	R/W1C
7	REF_DIFF_MIN_ERR		Reference Differential Voltage Too Small Status Bit.	0x0	R/W1C
6	REF_OV_UV_ERR		REFIN Overvoltage/Undervoltage Status Bit.	0x0	R/W1C
5	AINM_OV_UV_ERR		AINM Overvoltage/Undervoltage Status Bit.	0x0	R/W1C
4	AINP_OV_UV_ERR		AINP Overvoltage/Undervoltage Status Bit.	0x0	R/W1C
3	ADC_CONV_ERR		Analog Input Overrange/Underrange Status Bit.	0x0	R/W1C
2	SPI_ERR		SPI Interface Error Status Bit.	0x0	R/W1C
1	MM_CRC_ERR		Memory Map CRC Error Status Bit.	0x0	R/W1C
0	RESERVED		Reserved.	0x0	R

ON-CHIP REGISTER MAP

CHANNEL_EN REGISTER

Address: 0x78/0x79 (low/high byte), Reset: 0x0001

Channels are enabled using the CHANNEL_EN register. If only one channel is enabled, there is no sequencing through channels. If multiple channels are enabled, the AD4195-4 automatically sequences through all the enabled channels (from lowest numbered enabled channel to highest numbered enabled channel), automatically applying the setup conditions associated with the channel and generating conversion from each of the enabled channels (the number of conversions being set using the CHANNEL_SETUPn register). When using the sequencer, Channel 0 must always be one of the enabled channels. Certain ADC Modes (calibrations) are only performed on a single channel basis. If no channel is enabled, the AD4195-4 internally selects Channel 0. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 94. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_15	CH_14	CH_13	CH_12	CH_11	CH_10	CH_9	CH_8
CH_7	CH_6	CH_5	CH_4	CH_3	CH_2	CH_1	CH_0

Table 95. Bit Descriptions for CHANNEL_EN Register

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_15		Enables Channel 15 in the Sequencer.	0x0	R/W
14	CH_14		Enables Channel 14 in the Sequencer.	0x0	R/W
13	CH_13		Enables Channel 13 in the Sequencer.	0x0	R/W
12	CH_12		Enables Channel 12 in the Sequencer.	0x0	R/W
11	CH_11		Enables Channel 11 in the Sequencer.	0x0	R/W
10	CH_10		Enables Channel 10 in the Sequencer.	0x0	R/W
9	CH_9		Enables Channel 9 in the Sequencer.	0x0	R/W
8	CH_8		Enables Channel 8 in the Sequencer.	0x0	R/W
7	CH_7		Enables Channel 7 in the Sequencer.	0x0	R/W
6	CH_6		Enables Channel 6 in the Sequencer.	0x0	R/W
5	CH_5		Enables Channel 5 in the Sequencer.	0x0	R/W
4	CH_4		Enables Channel 4 in the Sequencer.	0x0	R/W
3	CH_3		Enables Channel 3 in the Sequencer.	0x0	R/W
2	CH_2		Enables Channel 2 in the Sequencer.	0x0	R/W
1	CH_1		Enables Channel 1 in the Sequencer.	0x0	R/W
0	CH_0		Enables Channel 0 in the Sequencer. Note that if multiple channels are being enabled, Channel 0 must always be used.	0x1	R/W

CHANNEL_SETUP REGISTERS

Address: 0x80 (low byte of CHANNEL_SETUP0) to 0xBC (high byte of CHANNEL_SETUP15) in increments of 4, Reset: 0x0000

Sixteen channel setup registers are included on the AD4195-4, CHANNEL_SETUP0 to CHANNEL_SETUP15. Using each register, the user can select the setup. The setup is selectable from eight different options defined by the user. When the ADC converts, it automatically sequences through all enabled channels. The REPEAT function indicates the number of conversions to be performed on the channel every time it is selected. This allows the user to sample some channels multiple times in a sequence, if required. Each time a channel is selected, a delay can be added to allow the front-end circuitry to settle before the ADC begins converting. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 96. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
REPEAT							
RESERVED	DELAY			RESERVED	SETUP		

ON-CHIP REGISTER MAP

Table 97. Bit Descriptions for CHANNEL_SETUP Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	REPEAT		Number of Times to Repeat This Channel. This setting allows for multiple conversions on a given channel before moving onto the next channel in the sequence. A single conversion only is performed on the channel when REPEAT is set to 0. Note that this function cannot be used when the per-channel data registers are used (all channels must share a DATA register).	0x0	R/W
7	RESERVED		Reserved.	0x0	R
[6:4]	DELAY		Delay to Add After Channel Switch. These bits allow a programmable delay to be added after the ADC selects the channel. This delay occurs before the ADC begins gathering samples on the channel. This is useful if external front-end circuitry needs some settling time. The delays specified are relative to the modulator clock frequency, f_{MOD} (MCLK/4), where MCLK is main clock/clock divide, configured using the CLOCK_CTRL register.	0x0	R/W
		000	0 Delay.		
		001	Delay 16 × f_{MOD}.		
		010	Delay 256 × f_{MOD}.		
		011	Delay 1024 × f_{MOD}.		
		100	Delay 2048 × f_{MOD}.		
		101	Delay 4096 × f_{MOD}.		
		110	Delay 8192 × f_{MOD}.		
		111	Delay 16384 × f_{MOD}.		
3	RESERVED		Reserved.	0x0	R
[2:0]	SETUP		Setup select. These bits identify which of the eight setups are used to configure the ADC for this channel. A setup comprises of: AFE, FILER, FILER_FS, MISC, offset register, and gain register. All channels can use the same setup, in which case the same 3-bit value must be written to these bits on all active channels. Alternatively, up to 8 channels can be configured differently.	0x0	R/W

CHANNEL_MAP REGISTERS

Address: 0x82 (low byte of CHANNEL_MAP0) to 0xBE (high byte of CHANNEL_MAP15) in increments of 4, Reset: 0x0001

Sixteen channel registers are included on the AD4195-4, CHANNEL_MAP0 to CHANNEL_MAP15. Using each register, the user can configure the channel (AINP input and AINM input). Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 98. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED			AINP_N				
RESERVED			AINM_N				

Table 99. Bit Descriptions for CHANNEL_MAP Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		Reserved.	0x0	R
[12:8]	AINP_N		Multiplexer Positive Input for This Channel.	0x0	R/W
		00000	AIN0.		
		00001	AIN1.		
		00010	AIN2.		
		00011	AIN3.		
		00100	AIN4.		
		00101	AIN5.		
		00110	AIN6.		
		00111	AIN7.		
		01000	AIN8.		
		01001	Reserved.		
		01010	Reserved.		

ON-CHIP REGISTER MAP

Table 99. Bit Descriptions for CHANNEL_MAP Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		01011	Reserved.		
		01100	Reserved.		
		01101	Reserved.		
		01110	Reserved.		
		01111	Reserved.		
		10000	Reserved.		
		10001	TEMP_SENSOR+.		
		10010	(AVDD − AVSS)/5+.		
		10011	(IOVDD − DGND)/5+.		
		10100	Reserved.		
		10101	ALDO.		
		10110	DLDO.		
		10111	AVSS.		
		11000	DGND.		
		11001	REFIN+.		
		11010	REFIN−.		
		11011	REFIN2+.		
		11100	REFIN2−.		
		11101	REFOUT.		
		11110	Reserved.		
		11111	Reserved.		
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	AINM_N		Multiplexer Negative Input for This Channel.	0x1	R/W
		00000	AIN0.		
		00001	AIN1.		
		00010	AIN2.		
		00011	AIN3.		
		00100	AIN4.		
		00101	AIN5.		
		00110	AIN6.		
		00111	AIN7.		
		01000	AIN8.		
		01001	Reserved.		
		01010	Reserved.		
		01011	Reserved.		
		01100	Reserved.		
		01101	Reserved.		
		01110	Reserved.		
		01111	Reserved.		
		10000	Reserved.		
		10001	TEMP_SENSOR−.		
		10010	(AVDD − AVSS)/5−.		
		10011	(IOVDD − DGND)/5−.		
		10100	Reserved.		
		10101	ALDO.		
		10110	DLDO.		
		10111	AVSS.		
		11000	DGND.		

ON-CHIP REGISTER MAP

Table 99. Bit Descriptions for CHANNEL_MAP Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		11001	REFIN+.		
		11010	REFIN−.		
		11011	REFIN2+.		
		11100	REFIN2−.		
		11101	RFEOUT.		
		11110	Reserved.		
		11111	Reserved.		

MISCELLANEOUS (MISC) REGISTERS

Address: 0xC0 (low byte of MISC0) to 0x122 (high byte of MISC7) in increments of 14, Reset: 0x0000

The AD4195-4 has eight miscellaneous registers, MISC0 to MISC7. Each MISC register is associated with a setup, MISCn is associated with Setup n. Chopping of the excitation currents, chopping of the multiplexer are configured using these registers. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 100. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHOP_IEXC		RESERVED				CHOP_ADC	
RESERVED						BURNOUT	

Table 101. Bit Descriptions for MISCn Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	CHOP_IEXC		Excitation Current Chopping Control. This enables chopping of the excitation currents for applications where better matching of excitation currents is required such as 3-wire RTD. The currents should have the same value.	0x0	R/W
		00	No Chopping of Excitation Currents. Excitation currents are not swapped/chopped.		
		01	Chopping of IOUT0 and IOUT1 Excitation Currents. The output pin selections for the IOUT0 and IOUT1 excitation currents are periodically swapped conversions are taken on each phase and the two conversions are averaged.		
		10	Reserved.		
		11	Reserved.		
[13:10]	RESERVED		Reserved.	0x0	R
[9:8]	CHOP_ADC		ADC/Mux Chopping. This enables chopping functionality, which can reduce offset errors. The channel settling time generally increases if chopping is enabled, because internal conversions must be performed for both polarities of chop.	0x0	R/W
		00	No Chopping. No chopping is performed.		
		01	Chops Internal Multiplexer. The internal multiplexer periodically swaps the positive and negative analog inputs, the ADC performs internal conversions on each of these selections and then averages the two conversions. This minimizes offset and offset drift.		
		10	Reserved.		
		11	Reserved.		
[7:2]	RESERVED		Reserved.	0x0	R
[1:0]	BURNOUT		Burnout Current Values. These currents are available on MUXP and MUXM so, if enabled for a channel, the currents are only active when the channel is selected.	0x0	R/W
		00	Off.		
		01	±100nA.		
		10	±2µA.		
		11	±10µA.		

ON-CHIP REGISTER MAP

AFE REGISTERS

Address: 0xC2 (low byte of AFE0) to 0x124 (high byte of AFE7) in increments of 14, Reset: 0x0050

The AD4195-4 has eight AFE registers, AFE0 to AFE7. Each AFE register is associated with a setup, AFEn is associated with Setup n. In the AFE register, the PGA gain, reference source, polarity, and reference buffers are configured. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 102. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED				REF_BUF_M		REF_BUF_P	
RESERVED	REF_SELECT		BIPOLAR	PGA_GAIN			

Table 103. Bit Descriptions for AFE Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Reserved.	0x0	R
[11:10]	REF_BUF_M		REFINn Buffer− Enable.	0x0	R/W
		00	Precharge Buffer.		
		01	Full Buffer.		
		10	Bypass.		
		11	Reserved.		
[9:8]	REF_BUF_P		REFINn Buffer+ Enable.	0x0	R/W
		00	Precharge Buffer.		
		01	Full Buffer.		
		10	Bypass.		
		11	Reserved.		
7	RESERVED		Reserved.	0x0	R
[6:5]	REF_SELECT		ADC Reference Selection.	0x2	R/W
		00	REFIN+, REFIN−.		
		01	REFIN2+, REFIN2−.		
		10	REFOUT, AVSS. The 2.5V REFOUT must be enabled separately in the REF_CONTROL register.		
		11	AVDD, AVSS.		
4	BIPOLAR		Select Bipolar or Unipolar ADC Span.	0x1	R/W
		0	Unipolar. Nominal Span is 0V to V_{REF}/PGA_GAIN. ADC data encoding is straight binary: 0V differential results in 0x000000 and +Full-Scale results in 0xFFFFFF.		
		1	Bipolar. Nominal Span is $-V_{REF}$/PGA_GAIN to $+V_{REF}$/PGA_GAIN. ADC data encoding is twos complement: 0V differential results in 0x000000, +Full-Scale results in 0x7FFFFF and −Full-Scale results in 0x800000.		
[3:0]	PGA_GAIN		PGA Gain Selection. Settings not listed are reserved.	0x0	R/W
		0000	PGA Gain = 1.		
		0001	PGA Gain = 2.		
		0010	PGA Gain = 4.		
		0011	PGA Gain = 8.		
		0100	PGA Gain = 16.		
		0101	PGA Gain = 32.		
		0110	PGA Gain = 64.		
		0111	PGA Gain = 128.		
		1000	PGA Gain = 0.5.		
		1001	PGA Gain = 1 Precharge Buffer.		

ON-CHIP REGISTER MAP

FILTER REGISTERS

Address: 0xC4 (low byte of FILTER0) to 0x126 (high byte of FILTER7) in increments of 14, Reset: 0x0000

The AD4195-4 has eight filter registers, FILTER0 to FILTER7. Each filter register is associated with a setup, FILTERn is associated with Setup n. In the FILTER register, the filter type is selected. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 104. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
POST_FILTER_SEL				FILTER_TYPE			

Table 105. Bit Descriptions for FILTER Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED		Reserved.	0x0	R
[7:4]	POST_FILTER_SEL		Post Filter. The post filters allow simultaneous rejection of 50Hz and 60Hz interference with reasonable settling time while giving good rejection. Settings not listed are reserved.	0x0	R/W
		0000	No Post Filter.		
		0001	Post Filter for Simultaneous 50Hz/60Hz Rejection with 40ms Settling. This post filter provides rejection of 50Hz and 60Hz with approximately 40ms settling when the output data rate of the preceding $Sinc^5$ + Avg filter is configured to 1,200Hz ((FILTER_FS = 208 for 16MHz clock with clock divide set to 2 and ADC chopping disabled).		
		0010	Post Filter for Simultaneous 50Hz/60Hz Rejection with 50ms Settling. This post filter provides rejection of 50Hz and 60Hz with approximately 50ms settling when the output data rate of the preceding $Sinc^5$ + Avg filter is configured to 1,200Hz (FILTER_FS = 208 for 16MHz clock with clock divide set to 2 and ADC chopping disabled).		
		0011	Post Filter for 50Hz/60Hz Rejection with 60ms Settling. This post filter provides rejection of 50Hz and 60Hz with approximately 60ms settling when the output data rate of the preceding $Sinc^5$ + Avg filter is configured to 1,200Hz (FILTER_FS = 208 for 16MHz clock with clock divide set to 2 and ADC chopping disabled).		
		0101	Post Filter for Average-By-16. The sinc filter ($Sinc^5$ + Avg) is followed by an averaging block. The sinc filter can use FILTER_FS values of 4, 8, 12....1024 (the 2LSBs must be set to 0).		
[3:0]	FILTER_TYPE		Filter Mode. This determines the type of digital filter to be used. There are restrictions on the allowed FILTER_FS values depending on the filter type, and whether any post filtering is performed. Settings not listed are reserved.	0x0	R/W
		0000	$Sinc^5$ + Avg. This digital filter option uses a fixed $Sinc^5$ filter followed by a programmable amount of averaging. Allowed FILTER_FS values are 4, 8, 12, multiples of 4 up to 65532.		
		0100	$Sinc^5$. This digital filter option uses a programmable $Sinc^5$ filter. Allowed FILTER_FS values are 4, 8, 12, multiples of 4 up to 256.		
		0110	$Sinc^3$. This digital filter option uses a programmable $Sinc^3$ filter. Allowed FILTER_FS values are 4, 8, multiples of 4 up to 65532.		

FILTER_FS REGISTERS

Address: 0xC6 (low byte of FILTER_FS0) to 0x128 (high byte of FILTER_FS7) in increments of 14, Reset: 0x0004

The AD4195-4 has eight FILTER_FS registers, FILTER_FS 0 to FILTER_FS 7. Each FILTER_FS register is associated with a setup, FILTER_FSn is associated with Setup n. The output data rate is set using this register. Writes to this register trigger a reset of the Digital Filter/Control Logic/Sequencer.

Table 106. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FS[15:8]							
FS[7:0]							

ON-CHIP REGISTER MAP

Table 107. Bit Descriptions for FILTER_FS Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	FS		Filter Select Word for Digital Filters. This configures the digital filter, which determines the ADC conversion speed and the noise performance. For the $Sinc^5$ filter, allowed FS values are 4, 8, multiples of 4 up to 256. For the $Sinc^3$ and $Sinc^5$ + Avg filters, allowed FS values are 4, 8, 12, multiples of 4 up to 65532.	0x4	R/W

OFFSET REGISTERS

Address: 0xC8 (low byte of OFFSET0) to 0x12A (high byte of OFFSET7) in increments of 14, Reset: 0x000000

The AD4195-4 has eight offset registers, OFFSET0 to OFFSET7. Each offset register is associated with a setup, OFFSETn is associated with Setup n. The OFFSET registers are 24-bit registers and hold the offset calibration coefficient for the ADC and its power-on reset value is 0x000000. Each of these registers is a read/write register. These registers are used in conjunction with the associated GAIN register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. It is recommended to place the ADC in standby or idle mode when writing to the OFFSET registers.

Table 108. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFFSET[23:16]							
OFFSET[15:8]							
OFFSET[7:0]							

Table 109. Bit Descriptions for OFFSET Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET		ADC Offset Coefficient.	0x0	R/W

GAIN REGISTERS

Address: 0xCB (low byte of GAIN0) to 0x12D (high byte of GAIN7) in increments of 14, Reset: 0x555555

The AD4195-4 has eight gain registers, GAIN0 to GAIN7. Each GAIN register is associated with a setup, GAINn is associated with Setup n. The GAIN registers are 24-bit registers and hold the full-scale calibration coefficient for the ADC. Although the gain error is factory calibrated for all gains, the GAIN register has a default value of 0x555555. The GAIN register contains this value on power-on and after a reset. The GAIN registers are read/write registers. However, when writing to the registers, it is recommended to place the ADC in standby or idle mode. The default value is automatically overwritten if a system full-scale calibration is initiated by the user or the registers are written to.

Table 110. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GAIN[23:16]							
GAIN[15:8]							
GAIN[7:0]							

Table 111. Bit Descriptions for GAINn Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN		ADC Gain Coefficient.	0x555555	R/W

REF_CONTROL REGISTER

Address: 0x130/0x131 (low/high byte), Reset: 0x0001

The internal 2.5V reference is enabled/disabled using this register. Note that the internal reference must be enabled when the internal temperature sensor or the excitation currents are being used. The internal reference must be enabled if a channel selects the internal reference for its conversion using the REF_SELECT bits.

ON-CHIP REGISTER MAP

Table 112. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
RESERVED							REF_EN

Table 113. Bit Descriptions for REF_CONTROL Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED		Reserved.	0x0	R
0	REF_EN		Internal Reference Enable.	0x1	R/W
		0	Disable internal reference.		
		1	Enable internal reference and output to REFOUT.		

V_BIAS REGISTER

Address: 0x134/0x135 (low/high byte), Reset: 0x0000

The internal bias voltage, which is equal to (AVDD + AVSS)/2, is enabled/disabled using this register.

Table 114. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							VBIAS_IN8_EN
VBIAS_IN7_EN	VBIAS_IN6_EN	VBIAS_IN5_EN	VBIAS_IN4_EN	VBIAS_IN3_EN	VBIAS_IN2_EN	VBIAS_IN1_EN	VBIAS_IN0_EN

Table 115. Bit Descriptions for V_BIAS Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	RESERVED		Reserved.	0x0	R
8	VBIAS_IN8_EN		Enable Voltage Bias on AIN8.	0x0	R/W
7	VBIAS_IN7_EN		Enable Voltage Bias on AIN7.	0x0	R/W
6	VBIAS_IN6_EN		Enable Voltage Bias on AIN6.	0x0	R/W
5	VBIAS_IN5_EN		Enable Voltage Bias on AIN5.	0x0	R/W
4	VBIAS_IN4_EN		Enable Voltage Bias on AIN4.	0x0	R/W
3	VBIAS_IN3_EN		Enable Voltage Bias on AIN3.	0x0	R/W
2	VBIAS_IN2_EN		Enable Voltage Bias on AIN2.	0x0	R/W
1	VBIAS_IN1_EN		Enable Voltage Bias on AIN1.	0x0	R/W
0	VBIAS_IN0_EN		Enable Voltage Bias on AIN0.	0x0	R/W

I_PULLUP REGISTER

Address: 0x136/0x137 (low/high byte), Reset: 0x0000

Pull-up currents of approximately 100nA can be enabled/disabled on the analog input pins using this register.

Table 116. Bit Names

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[15:8]	RESERVED							I_PULLUP_IN8_EN
[7:0]	I_PULLUP_IN7_EN	I_PULLUP_IN6_EN	I_PULLUP_IN5_EN	I_PULLUP_IN4_EN	I_PULLUP_IN3_EN	I_PULLUP_IN2_EN	I_PULLUP_IN1_EN	I_PULLUP_IN0_EN

Table 117. Bit Descriptions for I_PULLUP Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	RESERVED		Reserved.	0x0	R

ON-CHIP REGISTER MAP

Table 117. Bit Descriptions for I_PULLUP Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
8	I_PULLUP_IN8_EN		Enable Pull-up Current on AIN8.	0x0	R/W
7	I_PULLUP_IN7_EN		Enable Pull-up Current on AIN7.	0x0	R/W
6	I_PULLUP_IN6_EN		Enable Pull-up Current on AIN6.	0x0	R/W
5	I_PULLUP_IN5_EN		Enable Pull-up Current on AIN5.	0x0	R/W
4	I_PULLUP_IN4_EN		Enable Pull-up Current on AIN4.	0x0	R/W
3	I_PULLUP_IN3_EN		Enable Pull-up Current on AIN3.	0x0	R/W
2	I_PULLUP_IN2_EN		Enable Pull-up Current on AIN2.	0x0	R/W
1	I_PULLUP_IN1_EN		Enable Pull-up Current on AIN1.	0x0	R/W
0	I_PULLUP_IN0_EN		Enable Pull-up Current on AIN0.	0x0	R/W

CURRENT_SOURCE REGISTERS

Address: 0x138 (low byte of CURRENT_SOURCE0) to 0x13E (high byte of CURRENT_SOURCE3) in increments of 2, Reset: 0x0000

The AD4195-4 has two excitation currents (IOUT0 and IOUT1), which can be programmed independently. The current source is enabled and the pin on which the current is available is selected using this register.

Table 118. Bit Names

Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[15:8]	RESERVED					I_OUT_PIN		
[7:0]	RESERVED						I_OUT_VAL	

Table 119. Bit Descriptions for CURRENT_SOURCE Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		Reserved.	0x0	R
[12:8]	I_OUT_PIN		Selects the pin on which the excitation current is available. Settings not listed are reserved.	0x0	R/W
		00000	IOUT is Available on AIN0.		
		00001	IOUT is Available on AIN1.		
		00010	IOUT is Available on AIN2.		
		00011	IOUT is Available on AIN3.		
		00100	IOUT is Available on AIN4.		
		00101	IOUT is Available on AIN5.		
		00110	IOUT is Available on AIN6.		
		00111	IOUT is Available on AIN7.		
		01000	IOUT is Available on AIN8.		
		01001	Reserved.		
		01010	Reserved.		
		01011	Reserved.		
		01100	Reserved.		
		01101	Reserved.		
		01110	Reserved.		
		01111	Reserved.		
		10000	Reserved.		
		10001	IOUT is Available on GPIO0.		
		10010	IOUT is Available on GPIO1.		
		10011	IOUT is Available on GPIO2.		
		10100	IOUT is Available on GPIO3.		
[7:3]	RESERVED		Reserved.	0x0	R
[2:0]	I_OUT_VAL		Current Source Value. The internal reference must be enabled when the excitation currents are being used. The internal reference can be enabled via the REF_CONTROL register.	0x0	R/W

ON-CHIP REGISTER MAP

Table 119. Bit Descriptions for CURRENT_SOURCE Register (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		000	0µA.		
		001	10µA.		
		010	50µA.		
		011	100µA.		
		100	250µA.		
		101	500µA.		
		110	1000µA.		
		111	1500µA.		

GPIO_MODE REGISTER

Address: 0x190/0x191 (low/high byte), Reset: 0x0000

The GPIO pins are configured as inputs or outputs using this register. Note that these pins have multiple functions – GPIOs, power switch, reference, excitation current, and CHANNEL_TO_GPIO function. The functions are prioritized, for more details, see the General-Purpose Inputs/Outputs (GPIO0 to GPIO3) section.

Table 120. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
CH3_MODE		CH2_MODE		CH1_MODE		CH0_MODE	

Table 121. Bit Descriptions for GPIO_MODE Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED		Reserved.	0x0	R
[7:6]	CH3_MODE		GPIO3 Mode.	0x0	R/W
		00	Disabled.		
		01	Configured as an input.		
		10	Configured as an output.		
		11	Reserved.		
[5:4]	CH2_MODE		GPIO2 Mode.	0x0	R/W
		00	Disabled.		
		01	Configured as an input.		
		10	Configured as an output.		
		11	Reserved.		
[3:2]	CH1_MODE		GPIO1 Mode.	0x0	R/W
		00	Disabled.		
		01	Configured as an input.		
		10	Configured as an output.		
		11	Reserved.		
[1:0]	CH0_MODE		GPIO0 Mode.	0x0	R/W
		00	Disabled.		
		01	Configured as an input.		
		10	Configured as an output.		
		11	Reserved.		

ON-CHIP REGISTER MAP

GPIO_OUTPUT_DATA REGISTER

Address: 0x192/0x193 (low/high byte), Reset: 0x0000

When the GPIO pins are configured as outputs, the value on the pin is set in this register.

Table 122. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
RESERVED				CH3_OUTPUT	CH2_OUTPUT	CH1_OUTPUT	CH0_OUTPUT

Table 123. Bit Descriptions for GPIO_OUTPUT_DATA Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	RESERVED		Reserved.	0x0	R
3	CH3_OUTPUT		Pin GPIO3 Output State.	0x0	R/W
2	CH2_OUTPUT		Pin GPIO2 Output State.	0x0	R/W
1	CH1_OUTPUT		Pin GPIO1 Output State.	0x0	R/W
0	CH0_OUTPUT		Pin GPIO0 Output State.	0x0	R/W

GPIO_INPUT_DATA REGISTER

Address: 0x194/0x195 (low/high byte), Reset: 0x0000

When the GPIO pins are configured as inputs, the value on the pin is displayed in this register.

Table 124. Bit Names

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED							
RESERVED				CH3_INPUT	CH2_INPUT	CH1_INPUT	CH0_INPUT

Table 125. Bit Descriptions for GPIO_INPUT_DATA Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	RESERVED		Reserved.	0x0	R
3	CH3_INPUT		Pin GPIO3 Input State.	0x0	R
2	CH2_INPUT		Pin GPIO2 Input State.	0x0	R
1	CH1_INPUT		Pin GPIO1 Input State.	0x0	R
0	CH0_INPUT		Pin GPIO0 Input State.	0x0	R

OUTLINE DIMENSIONS

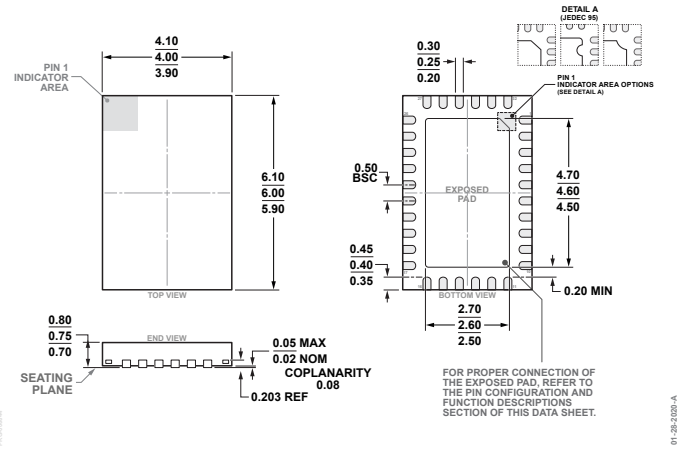

Figure 103. 32-Lead Lead Frame Chip-Scale Package [LFCSP] 4mm × 6mm Body and 0.75mm Package Height (CP-32-34)
Dimensions Shown in millimeters

Updated: January 31, 2025

ORDERING GUIDE

Table 126. Ordering Guide

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4195-4BCPZ	−40°C to +105°C	32-Lead LFCSP	Tray, 490	CP-32-34
AD4195-4BCPZ-RL7	−40°C to +105°C	32-Lead LFCSP	Reel, 1,500	CP-32-34

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Table 127. Evaluation Boards

Model[1]	Description
EVAL-AD4195-4ARDZ	Evaluation Board
EVAL-SDP-CK1Z	Evaluation Controller Board

[1] Z = RoHS-Compliant Part.