4-Channel, 16-Bit Voltage Output DAC, On-Chip Reference, SPI

FEATURES

- 16-bit resolution, ±3 LSB_{16} INL, ±1 LSB_{16} DNL
- TUE: ±0.22% of FSR maximum
- Offset error: ±1.5mV maximum
- Gain error: ±0.26% of FSR maximum
- Guaranteed sourcing current of 100 mA
- Ultra-low headroom: 12mV at 20mA load
- 2.5V internal voltage reference, 5ppm/°C, typical
- 55nV/√Hz noise spectral density (external reference)
- 96nV/√Hz noise spectral density (internal reference)
- Output voltage, current, and die temperature monitors
- 50MHz SPI write and read
- 2.7V to 5.5V power supply range
- 1.2V or 1.8V compatible digital interface
- Operating temperature range: −40°C to +125°C
- Small package: 2.1 mm × 2.2 mm, 25-ball WLCSP or 3 mm × 3 mm, 20-lead LFCSP

APPLICATIONS

- Optical transceivers
- Test and measurement
- Industrial automation
- Data acquisition systems

GENERAL DESCRIPTION

The AD3531/AD3531R are low power, 4-channel, 16-bit, buffered voltage output, digital-to-analog converters (DACs) that include software-programmable gain controls that result in full-scale output spans of 2.5V or 5V for reference voltages of 2.5V. The devices operate from single, 2.7V to 5.5V supply ranges and are guaranteed monotonic by design. The AD3531R also offers a 2.5V, 5ppm/°C internal reference that is disabled by default.

The devices include integrated multiplexers that allow monitoring of output voltages, currents, and internal die temperature. The AD3531/AD3531R are available in a 2.1 mm × 2.2 mm, 25-ball WLCSP or 3 mm × 3 mm, 20-lead LFCSP packages. The devices incorporate power-on reset (POR) circuits that ensure that the DACs output power up to and present at 16kΩ to ground until a valid write is executed. The DACs also contain power-down modes that reduce the current consumption down to 620µA, typical.

The serial peripheral interface (SPI) and MICROWIRE®-compatible, 4-wire serial interface operates on logic levels as low as 1.08V up to 1.98V and clock rates up to 50MHz.

Table 1. Device Family List

Channel Count	Interface	Reference	16-Bit
4	SPI	External	AD3531

FUNCTIONAL BLOCK DIAGRAM

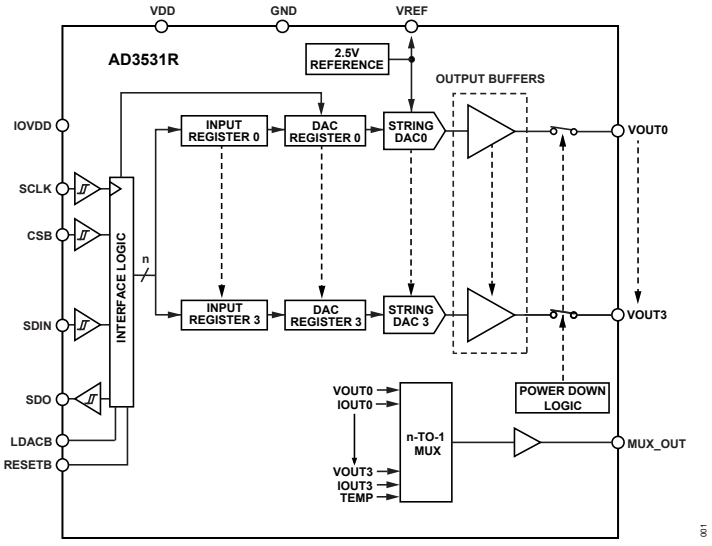


Figure 1. Functional Block Diagram

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9/2026—Rev. C to Rev. D

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Moved Headroom and Footroom Section ... 27

3/2026—Rev. B to Rev. C

Changes to Zero-Code Error Drift Parameter, Offset Error Drift Parameter, Full-Scale Error Drift Parameter, and Gain Error Drift Parameter; Table 2 ... 4
Changes to Figure 38 ... 16
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10/2025—Rev. 0 to Rev. A

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Changed Master to Controller (Throughout) 1
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Added Figure 5; Renumbered Sequentially 10
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Changes to Ordering Guide 45

4/2025—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

VDD = 2.7V to 5.5V, IOVDD = 1.08V to 1.98V, VREF = 2.5V (internal or external), load resistance (R_L) = 2kΩ, load capacitance (C_L) = 200pF. All specifications are T_J = −40°C to +125°C and typical at T_A = 25°C, unless otherwise noted.

Table 2. Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[1]					
Resolution	16			Bits	
Integral Nonlinearity Error (INL)		±3	±10	LSB	Range = 0 to VREF
		±3	±10	LSB	Range = 0 to 2 × VREF
Differential Nonlinearity Error (DNL)			±1	LSB	Range = 0 to VREF and guaranteed monotonic
			±1	LSB	Range = 0 to 2 × VREF and guaranteed monotonic
Zero-Code Error		0.22	±1	mV	Range = 0 to VREF or range = 0 to 2 × VREF
Offset Error		−0.16	±1.5	mV	Range = 0 to VREF
		−0.23	±1.6	mV	Range = 0 to 2 × VREF
Full-Scale Error		−0.05	±0.26	% of FSR	Range = 0 to VREF
		−0.06	±0.18	% of FSR	Range = 0 to 2 × VREF
Gain Error		−0.05	±0.26	% of FSR	Range = 0 to VREF
		−0.06	±0.18	% of FSR	Range = 0 to 2 × VREF
Total Unadjusted Error (TUE)		±0.04	±0.22	% of FSR	Range = 0 to VREF
		±0.04	±0.16	% of FSR	Range = 0 to 2 × VREF
Zero-Code Error Drift		±1.3		µV/°C	Range = 0 to VREF or range = 0 to 2 × VREF
Offset Error Drift		±1.3		µV/°C	Range = 0 to VREF or range = 0 to 2 × VREF
Full-Scale Error Drift		±2		ppm	Of FSR/°C, Range = 0 to VREF or range = 0 to 2 × VREF
Gain Error Drift		±2		ppm	Of FSR/°C, Range = 0 to VREF or range = 0 to 2 × VREF
DC Power Supply Rejection Ratio (PSRR)		0.03		mV/V	DAC code = midscale and supply voltage (V_{DD}) = 5V ± 10%
DC Crosstalk		±6		µV	Due to single channel, full-scale output change, internal reference, and range = 0 to VREF
		±0.6		µV/mA	Due to load current change, external reference, and range = 0 to 2 × VREF
		±11		µV	Due to powering down (per channel), internal reference, and range = 0 to VREF
OUTPUT CHARACTERISTICS					
Output Power-Up State		16		kΩ	Pull-down resistance
Output Voltage Range	0		2.5	V	Range = 0 to VREF, internal reference, and VDD > VREF
	0		5	V	Range = 0 to 2 × VREF, internal reference, and VDD > 2 × VREF
Maximum Capacitive Load		2		nF	R_L = ∞
		5		nF	R_L = 1kΩ
Load Regulation		40		µV/mA	V_{DD} = 5V ± 10%, DAC code = midscale, and −30mA ≤ output current (I_{OUT}) ≤ +30mA
		40		µV/mA	V_{DD} = 3V ± 10%, DAC code = midscale, and −20mA ≤ I_{OUT} ≤ +20mA
Short-Circuit Current [2]	100			mA	Sourcing
	80			mA	Sinking
Headroom	20	12		mV	Source current = 20mA
Footroom	45	24		mV	Sink current = 20mA
Load Impedance at Rails		0.625		Ω	VDD, sourcing
		1.25		Ω	GND, sinking
Power-Up Time		5		µs	Exiting power-down mode and V_{DD} = 5V
REFERENCE INPUT					
Reference Input Current		375		µA	V_{REF} = V_{DD}= 5.5V and range = 0 to VREF

SPECIFICATIONS

Table 2. Electrical Characteristics (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
		750		µA	V_{REF} = V_{DD} = 5.5V and range = 0 to 2 × VREF
Reference Input Range	1		V_{DD}	V	Range = 0 to VREF
	1		V_{DD}/2	V	Range = 0 to 2 × VREF
Reference Input Impedance		15.0		kΩ	Range = 0 to VREF
		7.5		kΩ	Range = 0 to 2 × VREF
REFERENCE OUTPUT					
Output voltage (V_{OUT})	2.4975		2.5025	V	WLCSP; T_J = 25°C
	2.4965		2.5035	V	LFCSP ; T_J = 25°C
Voltage Reference Temperature Coefficient (TC)[3]		5	15	ppm/°C	
		5	10	ppm/°C	T_J = 25°C to +125°C
Output Impedance		0.06		Ω	
Output Voltage Noise		25		µV p-p	0.1Hz to 10Hz
Output Voltage Noise Density		96		nV/√Hz	At T_A, f = 10kHz, C_L = 10nF, and range = 0 to VREF or 0 to 2× VREF
Maximum Capacitive Load		0.5		nF	
Load Regulation Sourcing		60		µV/mA	At ambient temperature
Output Current Load Capability		5		mA	Sourcing
		100		µA	Sinking
Line Regulation		10		µV/V	At ambient temperature
Long-Term Stability Drift		100		ppm	After 1000 hours at 25°C
Thermal Hysteresis		125		ppm	First cycle
		25		ppm	Additional cycles
INTEGRATED MULTIPLEXER					
Buffer Output Current		±10		mA	
Buffer Output Impedance		0.9		Ω	
Buffer Offset		10		mV	
Maximum Capacitive Load		470		pF	
Multiplexer (Mux) Switching Glitch[4]		0.5		mV	
LOGIC INPUTS					
Input Current			±1	µA	Per pin
Input Low Voltage (V_{IL})			0.3 × IOVDD	V	
Input High Voltage (V_{IH})	0.7 × IOVDD			V	
Input Capacitance		2		pF	
LOGIC OUTPUT (SDO)					
Output Low Voltage (V_{OL})			0.4	V	Sink current (I_{SINK}) = 200µA
Output High Voltage (V_{OH})	IOVDD − 0.4			V	Source current (I_{SOURCE}) = 200µA
Floating State Output Capacitance		2		pF	
POWER REQUIREMENTS					
IOVDD	1.08		1.98	V	
IOVDD Pin Current (I_{IOVDD})			16	µA	
VDD	2.7		5.5	V	Range = 0 to VREF
	VREF + 1.5		5.5	V	Range = 0 to 2 × VREF
VDD Current (I_{VDD})					V_{IH} = V_{DD}, V_{IL} = GND, and V_{DD} = 2.7V to 5.5V
Normal Operation[5]		2.8	3.4	mA	External reference
		3.85	4.3	mA	Internal reference
500Ω to GND, 3.85kΩ to GND, and 16kΩ to GND[6]		0.67	0.85	mA	External reference

SPECIFICATIONS

Table 2. Electrical Characteristics (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
		1.45	1.7	mA	Internal reference

1 Static performance tested with the outputs unloaded, unless otherwise noted. Linearity calculated using a reduced code range of 256 to 65279.

2 The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature may impair device reliability.

3 Voltage reference temperature coefficient is calculated as per the box method. See the Terminology section for further information.

4 The peak voltage glitch seen on the VOUTn channels when a different channel is monitored through MUX_OUT_SELECT_O (SEL).

5 Interface inactive. All channels in Operating Mode 0 with outputs unloaded.

6 Interface inactive. All channels in either Operating Mode 1, Operating Mode 2, or Operating Mode 3.

AC SPECIFICATIONS

VDD = 2.7V to 5.5V, 1.08V ≤ IOVDD ≤ 1.98V, VREF = 2.5V (external), R_L = 2kΩ to GND, C_L = 200pF, and all specifications are T_J = −40°C to +125°C, typical at T_A = 25°C, unless otherwise noted.

Table 3. AC Specifications

Parameter	Min	Typ	Max	Unit	Test Condition/Comments
OUTPUT VOLTAGE SETTLING TIME		5	7.9	µs	¼ to ¾ scale settling to ±2 LSB
SLEW RATE		1		V/µs	
DIGITAL-TO-ANALOG GLITCH IMPULSE		1		nV-sec	1 LSB change around major carry, internal reference, and range = 0 to VREF
DIGITAL FEEDTHROUGH		0.09		nV-sec	Internal reference
CROSSTALK[1]					
Digital		0.09		nV-sec	Internal reference
Analog		−0.2		nV-sec	Internal reference and range = 0 to VREF
		−0.3		nV-sec	Internal reference and range = 0 to 2 × VREF
DAC-to-DAC		−0.3		nV-sec	Internal reference and range = 0 to 2 × VREF
TOTAL HARMONIC DISTORTION (THD)[2]		−93		dB	At T_A, bandwidth = 20kHz, V_{DD} = 5V, output frequency (f_{OUT}) = 1kHz, internal reference, and range = 0 to 2 × VREF
OUTPUT NOISE SPECTRAL DENSITY		55		nV/√Hz	DAC code = midscale, 10kHz, range = 0 to 2 × VREF, and external reference
		96		nV/√Hz	DAC code = midscale, 10kHz, range = 0 to 2 × VREF, and internal reference
OUTPUT NOISE		6.6		µV p-p	0.1Hz to 10Hz and range = 0 to VREF
SIGNAL-TO-NOISE RATIO (SNR)		92		dB	At T_A = 25°C, bandwidth = 20kHz, V_{DD} = 5V, f_{OUT} = 1kHz, and internal reference
SPURIOUS-FREE DYNAMIC RANGE (SFDR)		84		dB	At T_A = 25°C, bandwidth = 20kHz, V_{DD} = 5V, f_{OUT} = 1kHz, and internal reference
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)		90		dB	At T_A = 25°C, bandwidth = 20kHz, V_{DD} = 5V, f_{OUT} = 1kHz, internal reference, and range = 0 to 2 × VREF

1 See the Terminology section. Measured using internal reference and range = 0 to VREF, unless otherwise noted.

2 Digitally generated sine wave (f_{OUT}) at 1kHz.

SPECIFICATIONS

TIMING CHARACTERISTICS

All input signals are specified with rise time (t_R) = fall time (t_F) = 1ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{INL} + V_{INH})/2. VDD = 2.7V to 5.5V, 1.08V ≤ IOVDD ≤ 1.98V, and VREF = 2.5V. All specifications are T_J = −40°C to +125°C, unless otherwise noted.

Table 4. SPI Interface Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_1	SCLK cycle time	20		80[1]	ns
t_2	SCLK high time		t_1/2		ns
t_3	SCLK low time		t_1/2		ns
t_4	SCLK rising edge to CSB falling edge	10			ns
t_5	$\overline{CS}$ falling edge to SCLK rising edge setup time	7			ns
t_6	SCLK rising edge to CSB rising edge	4			ns
t_7	$\overline{CS}$ rising edge to SCLK rising edge	6			ns
t_8	Data hold time	2			ns
t_9	Data setup time	5			ns
t_{10}	CSB high time (single, combined, or all channel update)	10			ns
t_{11}	SCLK falling edge to SDO data available			9	ns
t_{12}	SCLK falling edge to SDO data remains valid			10	ns
t_{13}	CSB rising edge to SDO disabled			9	ns
t_{14}	SCLK falling edge to SDO enabled			10	ns
t_{15}	Last SCLK rising edge to V_{OUT} transition start		3		µs
t_{16}	RESETB pulse width		2.5		µs
t_{17}	RESETB falling edge to V_{OUT} transition		3		µs
t_{18}	RESETB rising edge to SPI transaction begin		150		ns

[1] Only applicable for stream mode functionality.

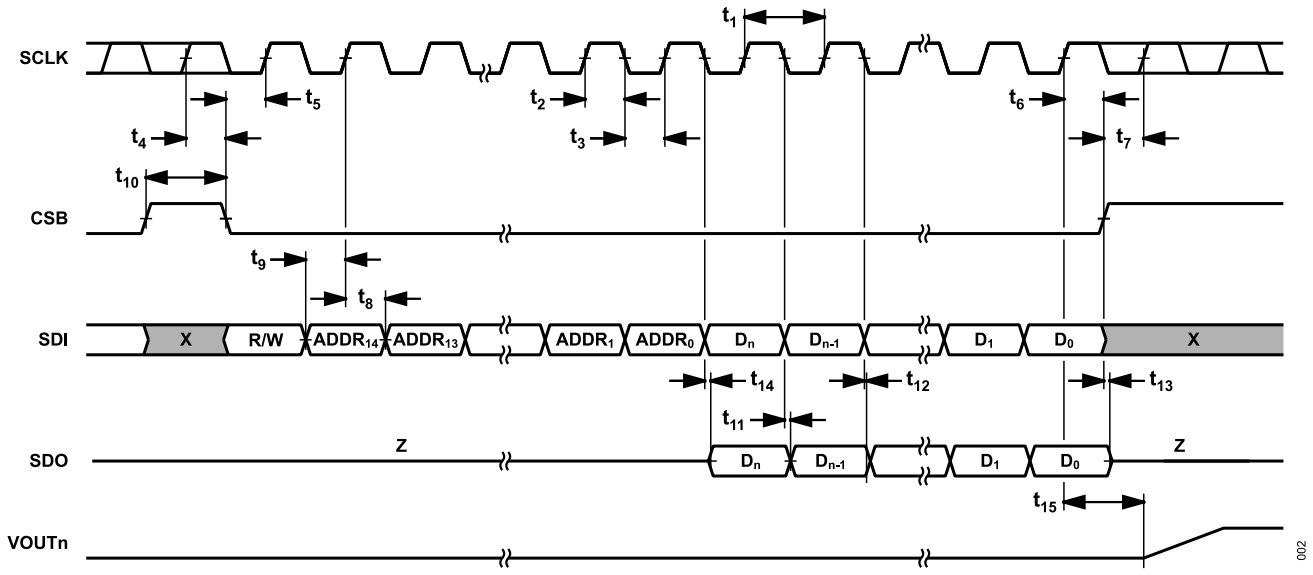


Figure 2. Serial Read and Write Operation

SPECIFICATIONS

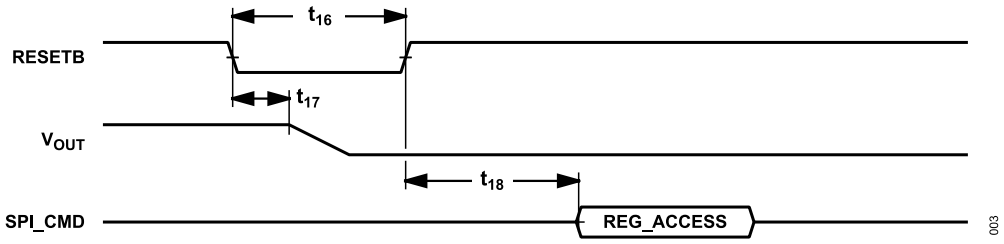


Figure 3. Reset Timing

Table 5. LDAC Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{L1}	LDACB pulse width (For both CSB==1 and CSB==0)	120			ns
t_{L2}	LDACB falling edge to SPI DAC update	640			ns
t_{L3}	SPI DAC update to LDACB negative edge.	640			ns
t_{L4}	LDACB falling edge to V_{OUT} transition		1.3		µs

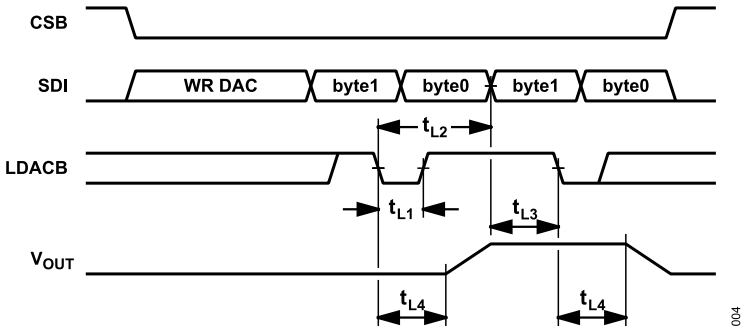


Figure 4. LDAC Timing

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
VDD to GND	−0.3V to +6.5V
IOVDD to GND	−0.3V to +2.1V
VOUTn to GND	−0.3V to VDD + 0.3V
VREF[1] to GND	−0.3V to VDD + 0.3V
Digital Input Voltage to GND	−0.3V to IOVDD + 0.3V
Temperature	
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Absolute Maximum Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb-Free (J-STD-020)	260°C

[1] Configured as the reference input pin.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot, sealed enclosure. θ_{JB} is the junction to board thermal resistance. θ_{JC} is the is the junction to case thermal resistance. Ψ_{JT} is the is the junction to top thermal characterization parameter. Ψ_{JB} is the is the junction to board thermal characterization.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
CB-25-11[1]	43.71	9.64	4.75	4.42	9.64	°C/W
CP-20-23[2]	71.11	24.67	43.58	5.36	22.51	°C/W

[1] Simulation values on JEDEC 2S2P board with 4 thermal vias, still air (0m/sec airflow).

[2] Simulation values on JEDEC 2S2P board without thermal via due to absence of exposed paddle, still air (0m/sec airflow).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

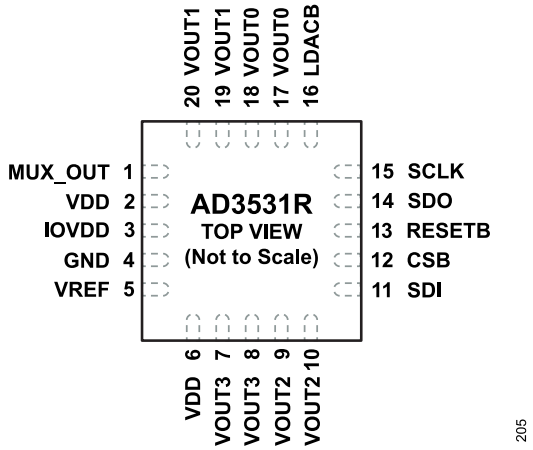


Figure 5. LFCSP Pin Configuration

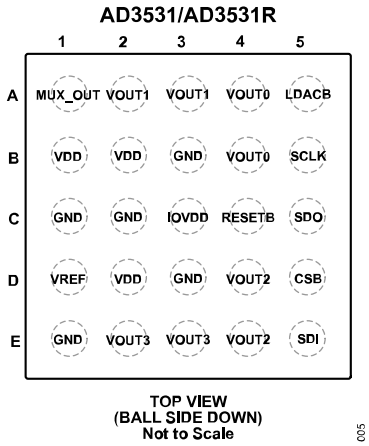


Figure 6. WLCSP Pin Configuration

Table 8. Pin Function Descriptions

LFCSP	WLCSP	Mnemonic	Type[1]	Description
1	A1	MUX_OUT	AO	Analog Multiplexer. The MUX_OUT pin is used to monitor the internal die temperature, output voltages and output current of a selected channel.
2,6	B1, B2, D2	VDD	S	Power Supply Input. The AD3531/AD3531R operates from 2.7V to 5.5V. Decouple the VDD supply with a 10µF capacitor in parallel with a 0.1µF capacitor to GND.
3	C3	IOVDD	DI	Digital Power Supply. The voltage on the IOVDD pin is specified in Table 2.
4	B3, C1, C2, D3, E1	GND	S	Ground Reference Point for All Circuitry on the Device.
5	D1	VREF	AI/O	Reference Output Voltage. When using the internal reference, this is the reference output pin. The VREF is the reference input by default.
11	E5	SDI	DI	Serial Data Input. Logic Input. Provides data to be written to the device and is clocked into the register on the rising edge of SCLK.
12	D5	CSB	DI	Active Low Control Input. This is the frame synchronization signal for the input data.
13	C4	RESETB	DI	Asynchronous Reset pin. Active-low logic input and falling edge sensitive. See the Hardware Reset section for additional information.
14	C5	SDO	DO	Serial Data Output. Logic output. A readback operation provides data on this output pin as a serial data stream. Data is clocked out on the falling edge of SCLK and is valid on the rising edge of SCLK.
15	B5	SCLK	DI	Serial Clock Input. Data transfers at rates of up to 50MHz for write operation and 25MHz for read operation.
16	A5	LDACB	DI	Asynchronous Load DAC pin. Active low logic input, falling edge sensitive. See the Hardware LDAC section for additional information.
17, 18	A4, B4	VOUT0	AO	Analog Output Voltage from DAC 0. The output amplifier has rail-to-rail operation.
19, 20	A2, A3	VOUT1	AO	Analog Output Voltage from DAC 1. The output amplifier has rail-to-rail operation.
9, 10	D4, E4	VOUT2	AO	Analog Output Voltage from DAC 2. The output amplifier has rail-to-rail operation.
7, 8	E2, E3	VOUT3	AO	Analog Output Voltage from DAC 3. The output amplifier has rail-to-rail operation.

[1] AO is analog output pin, AI/O is analog input or output pin, S is supply pin, DI is the digital input pin, and DO is the digital input pin.

TYPICAL PERFORMANCE CHARACTERISTICS

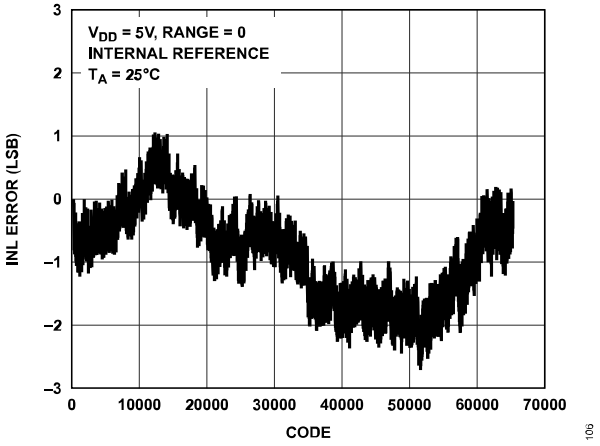


Figure 7. INL Error vs. Code

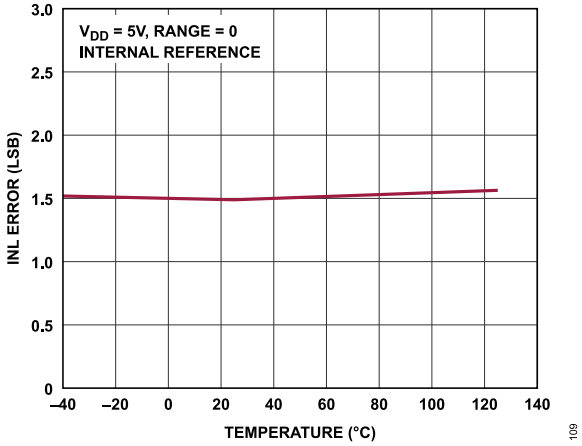


Figure 10. INL Error vs. Temperature

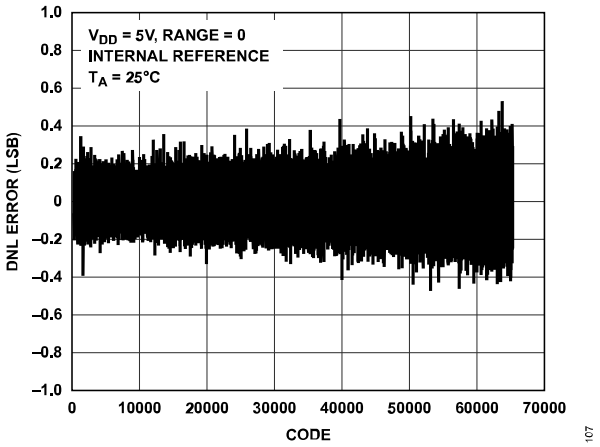


Figure 8. DNL Error vs. Code

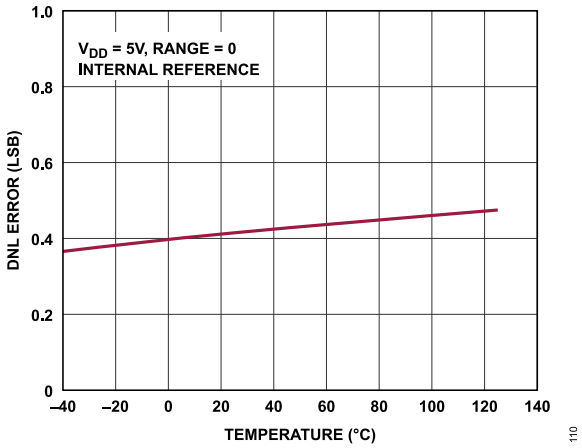


Figure 11. DNL Error vs. Temperature

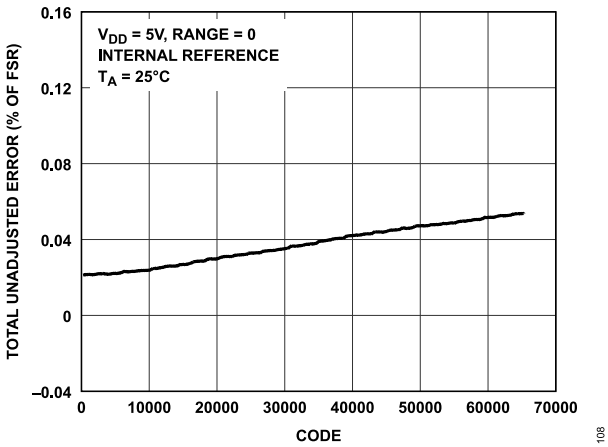


Figure 9. TUE vs. Code

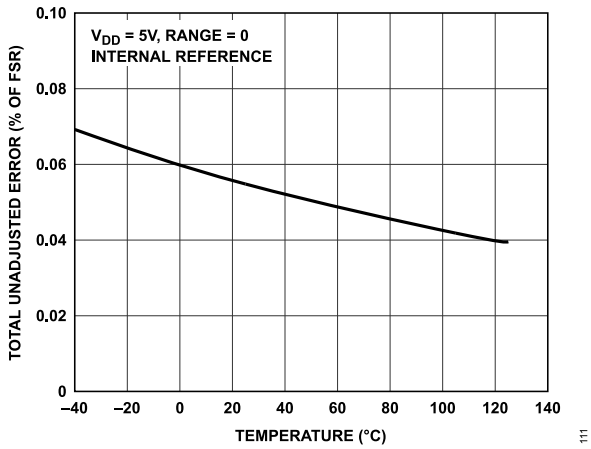


Figure 12. TUE vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

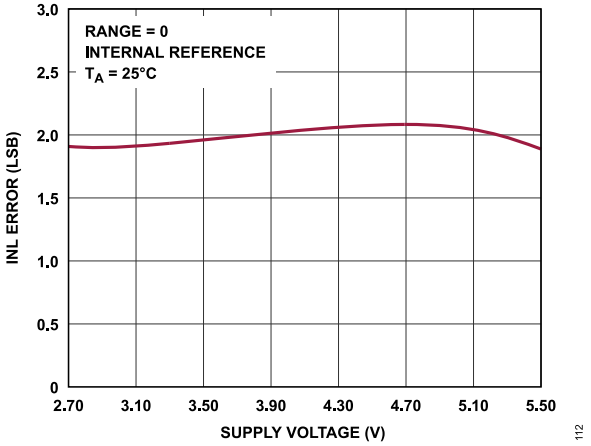


Figure 13. INL Error vs. Supply Voltage

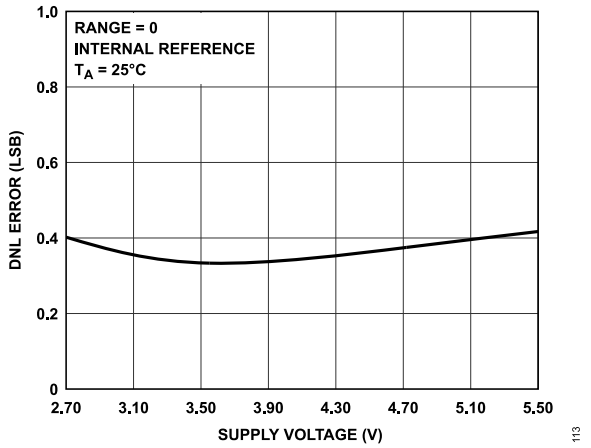


Figure 14. DNL Error vs. Supply Voltage

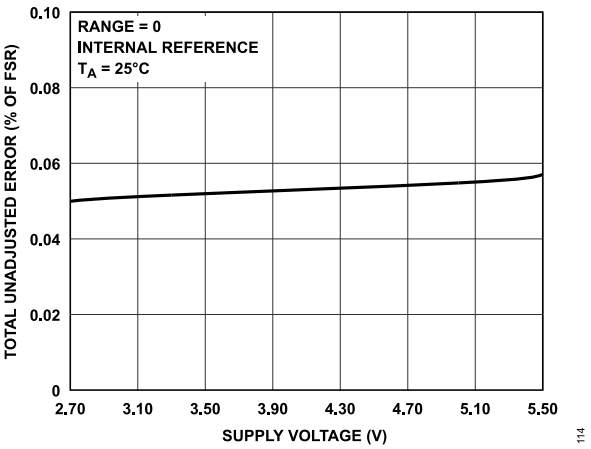


Figure 15. TUE vs. Supply Voltage

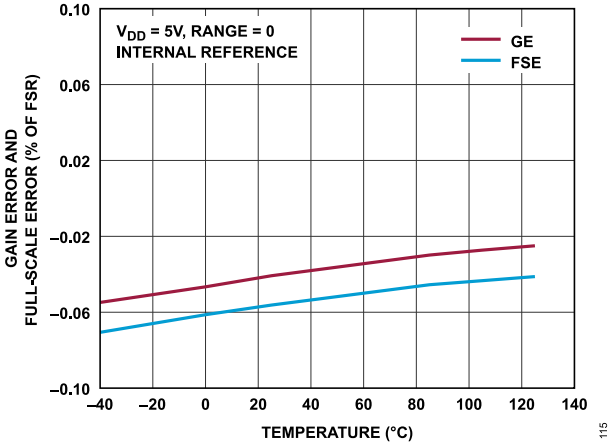


Figure 16. Gain Error and Full-Scale Error vs. Temperature

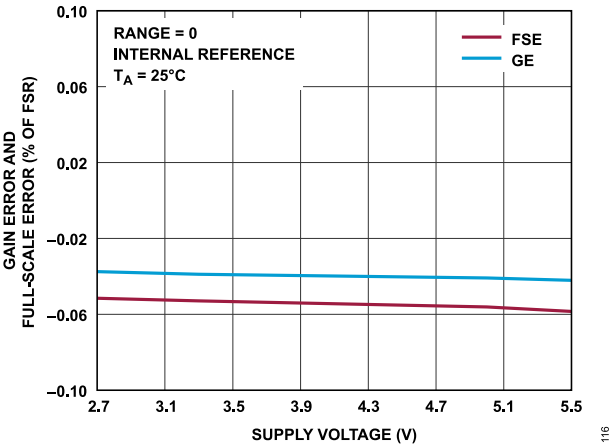


Figure 17. Gain Error and Full-Scale Error vs. Supply Voltage

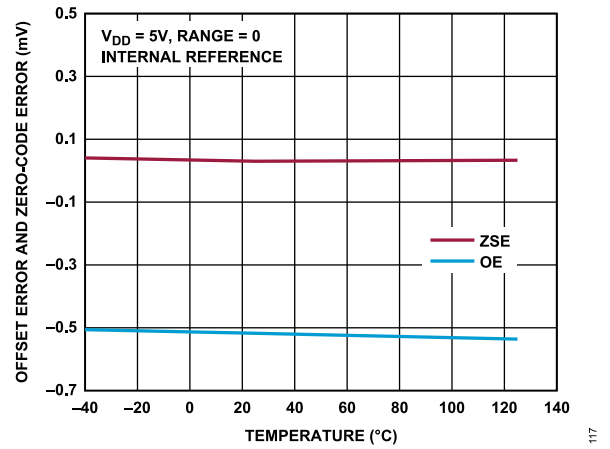


Figure 18. Offset Error and Zero-Code Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

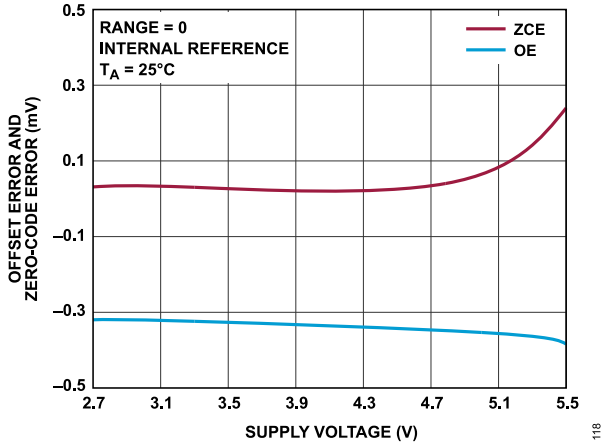


Figure 19. Offset Error and Zero-Code Error vs. Supply Voltage

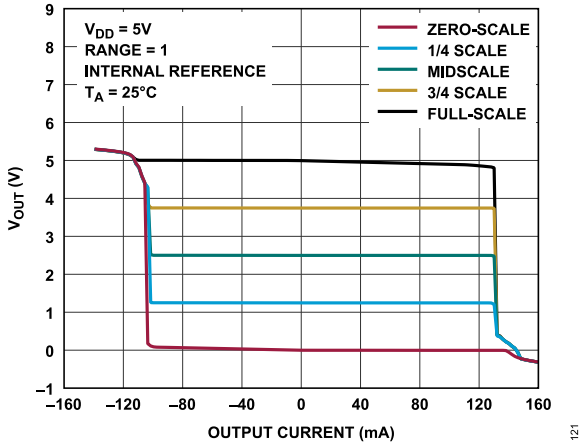


Figure 22. Source and Sink Capability at VDD = 5V

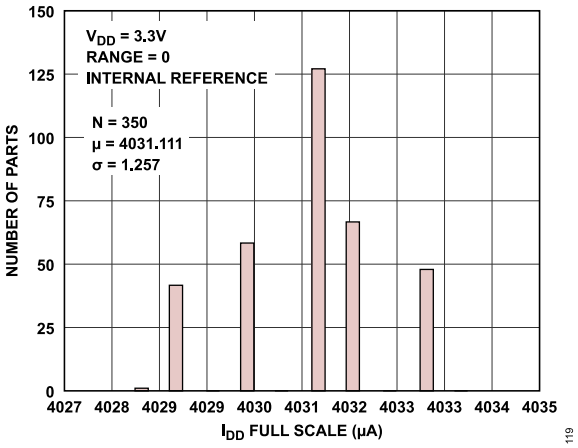


Figure 20. Supply Current (I_{DD}) Histogram with Internal Reference

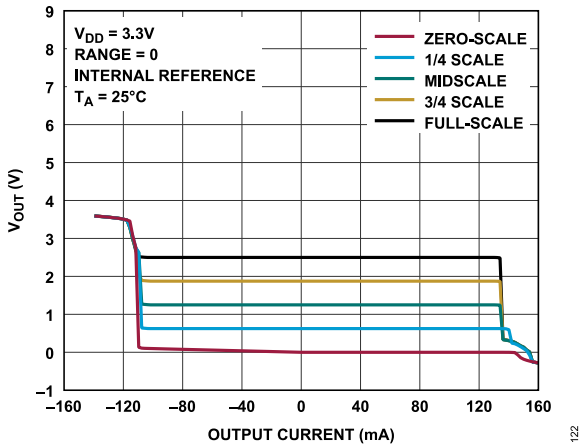


Figure 23. Source and Sink Capability at VDD = 3.3V

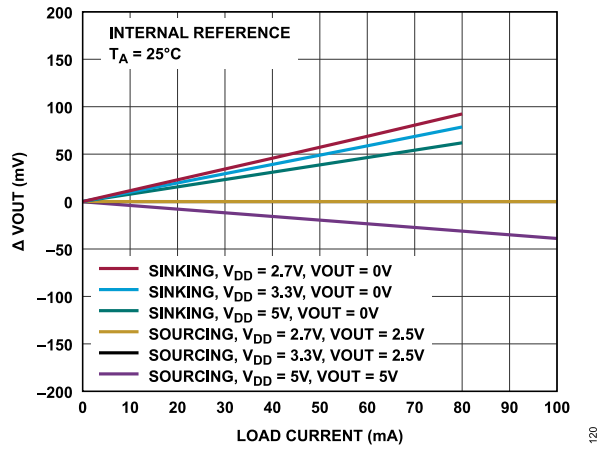


Figure 21. Headroom and Footroom (ΔVOUT) vs. Load Current

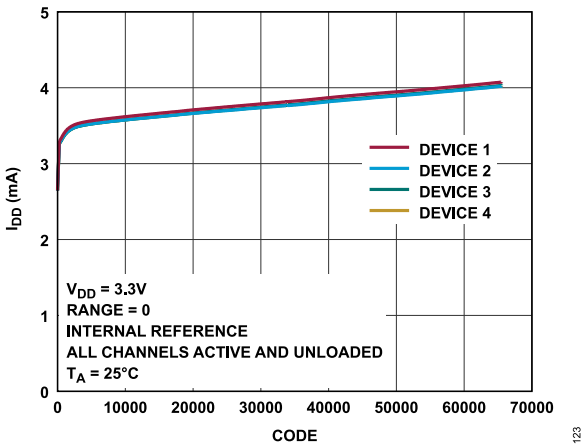


Figure 24. I_{DD} vs. Code

TYPICAL PERFORMANCE CHARACTERISTICS

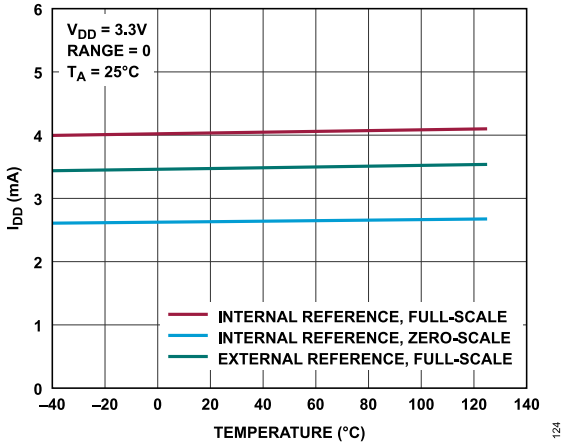


Figure 25. I_{DD} vs. Temperature

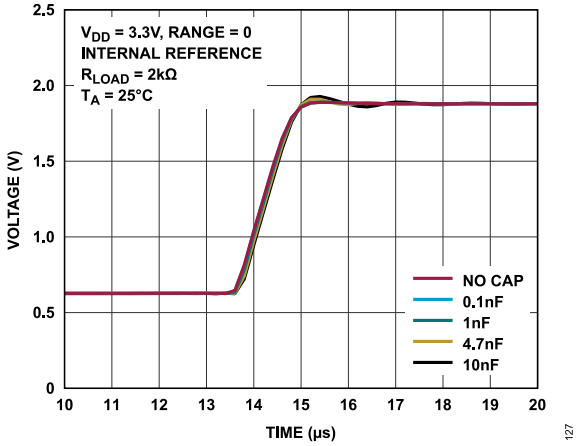


Figure 28. Settling Time at Various Capacitive Loads

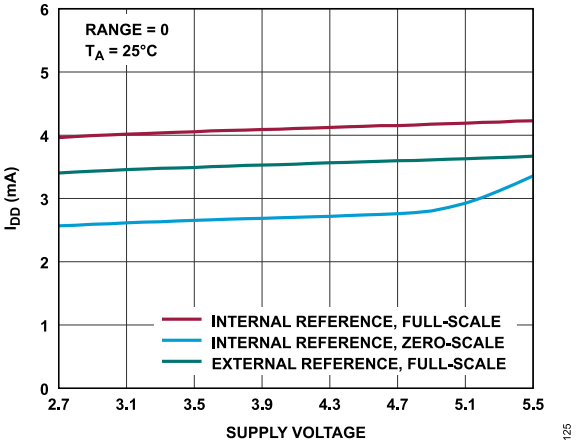


Figure 26. I_{DD} vs. Supply Voltage

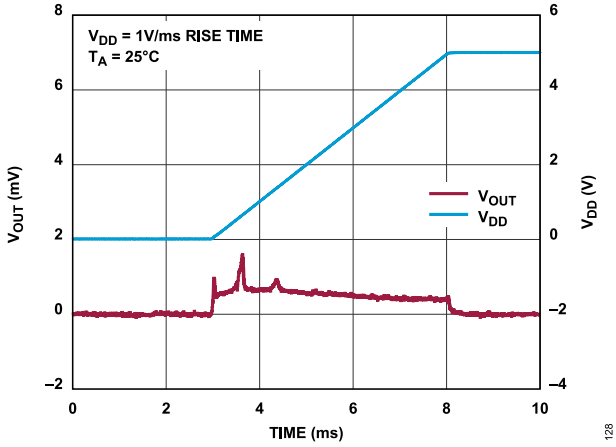


Figure 29. Power-On Reset to Tri-State Output

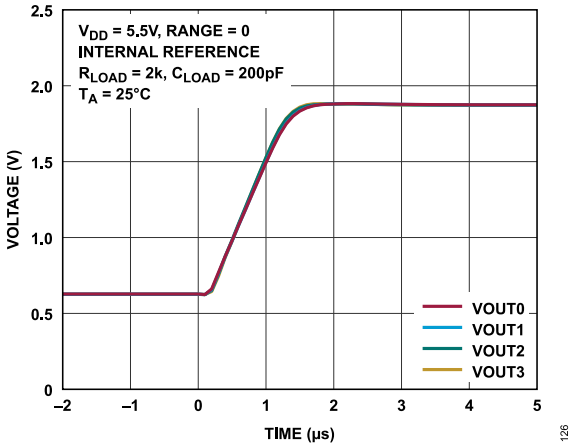


Figure 27. Settling Time

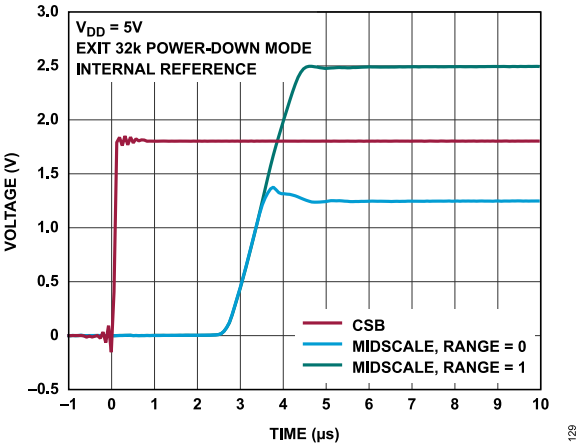


Figure 30. Exiting Power-Down to Midscale

TYPICAL PERFORMANCE CHARACTERISTICS

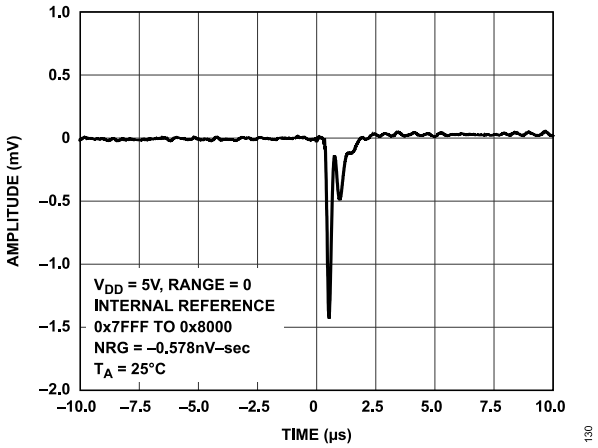


Figure 31. Digital-to-Analog Glitch Impulse 5V

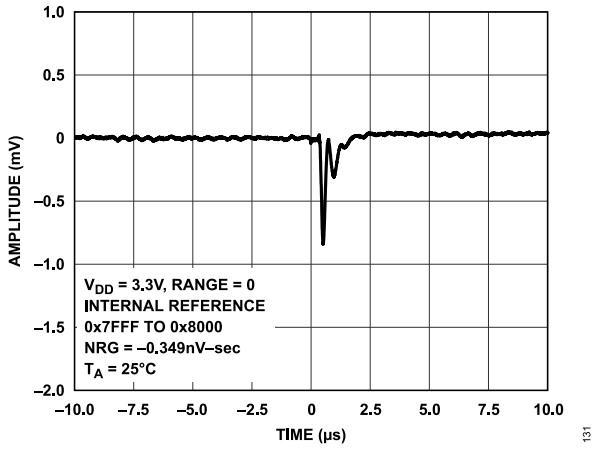


Figure 32. Digital-to-Analog Glitch Impulse 3.3V

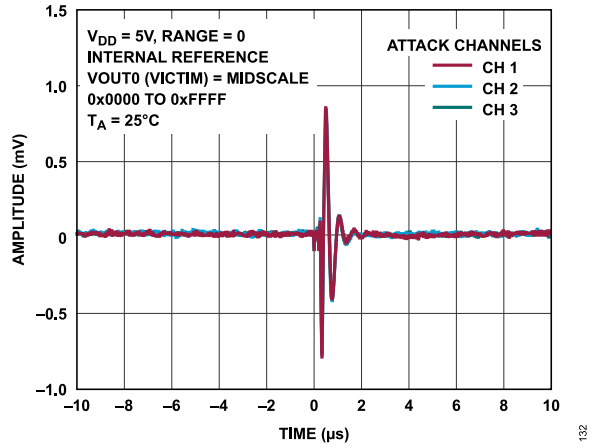


Figure 33. Analog Crosstalk 5V

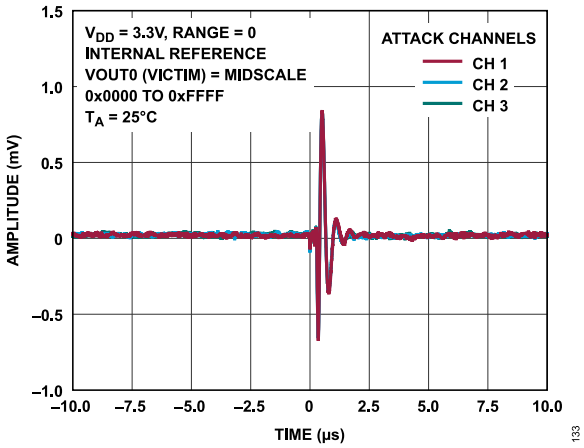


Figure 34. Analog Crosstalk 3.3V

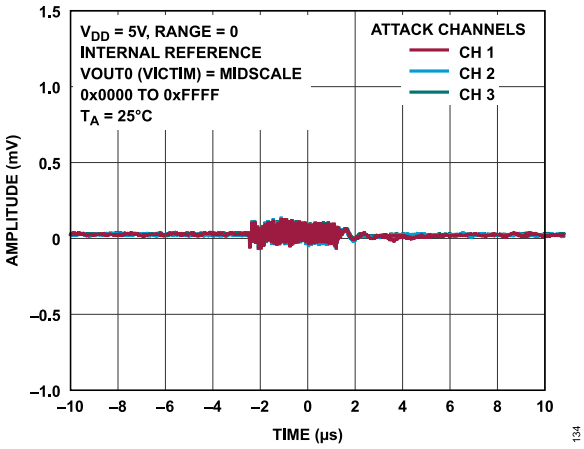


Figure 35. DAC-to-DAC Crosstalk 5V

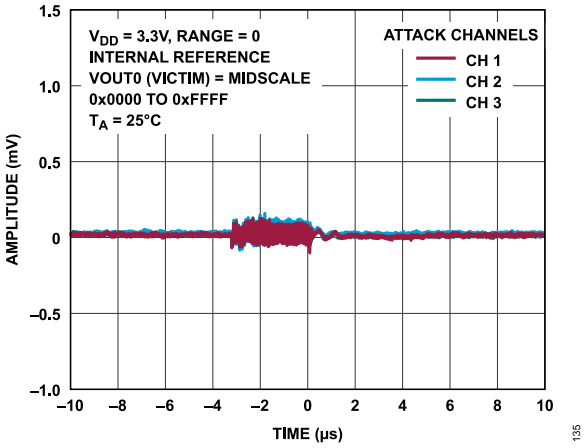


Figure 36. DAC-to-DAC Crosstalk 3.3V

TYPICAL PERFORMANCE CHARACTERISTICS

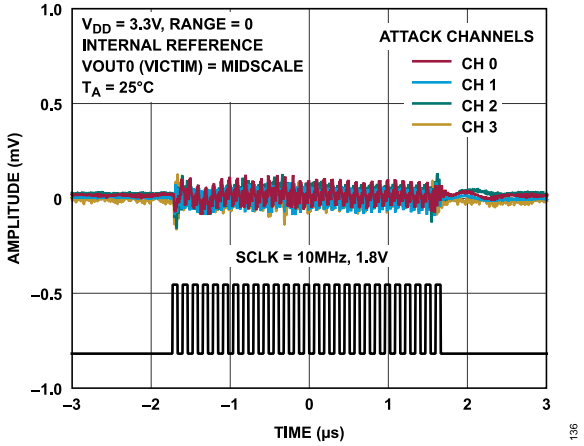


Figure 37. Digital Feedthrough

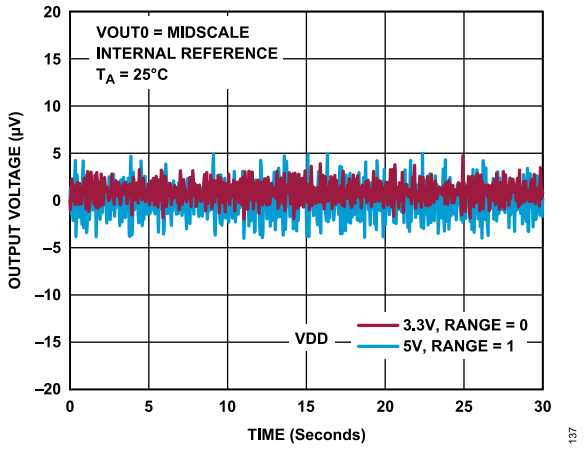


Figure 38. 0.1Hz to 10Hz Output Noise

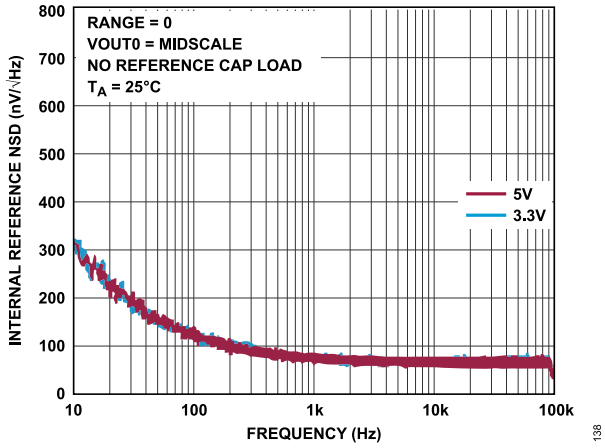


Figure 39. Noise Spectral Density (NSD)

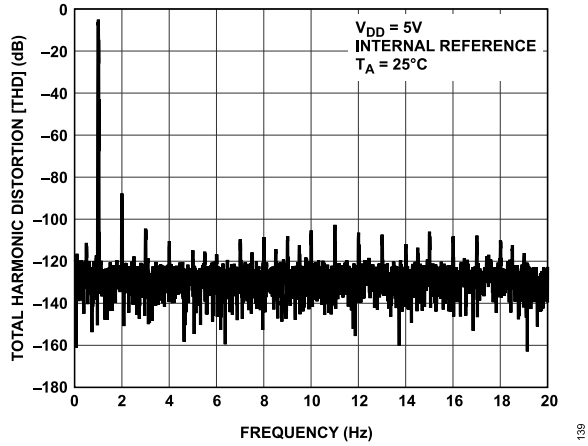


Figure 40. THD at 1kHz

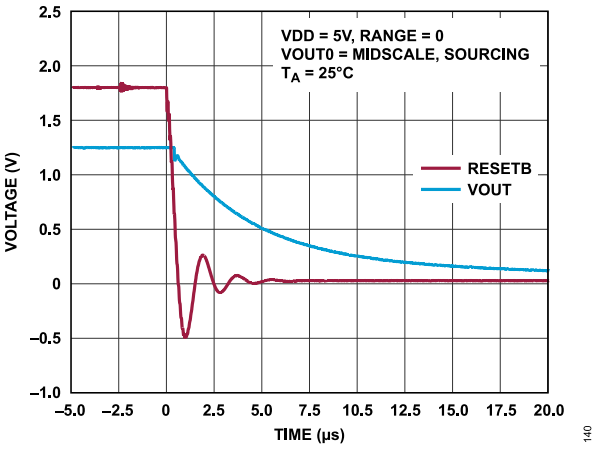


Figure 41. Hardware Reset

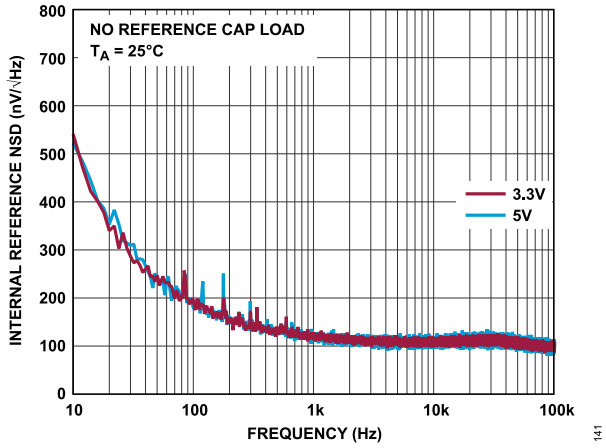


Figure 42. Internal Reference NSD vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

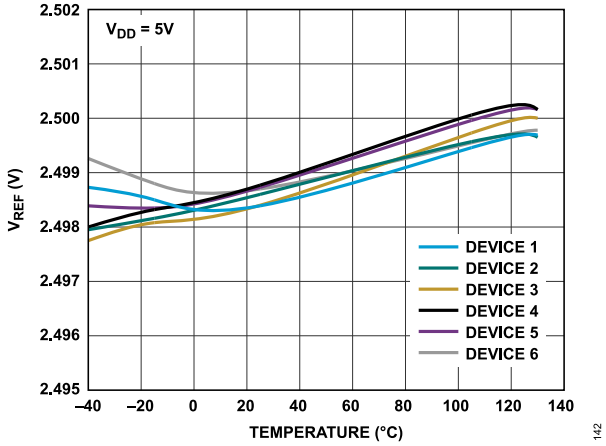


Figure 43. VREF vs. Temperature (WLCSP)

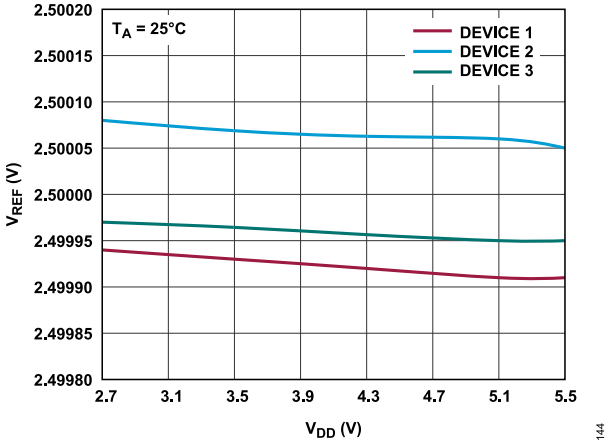


Figure 46. VREF vs. VDD

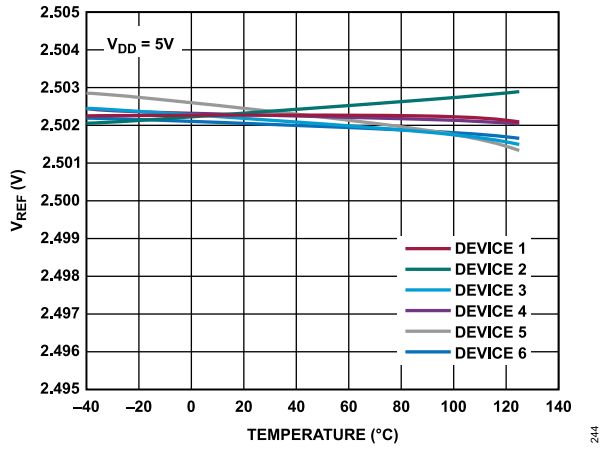


Figure 44. VREF vs. Temperature (LFCSP)

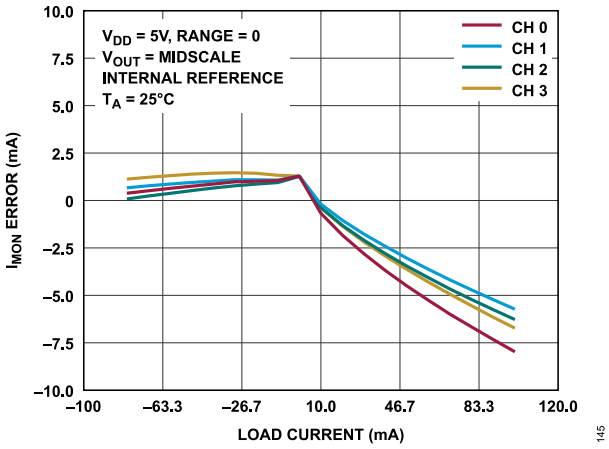


Figure 47. MUX_OUT I_{MON} Error vs. Output Current

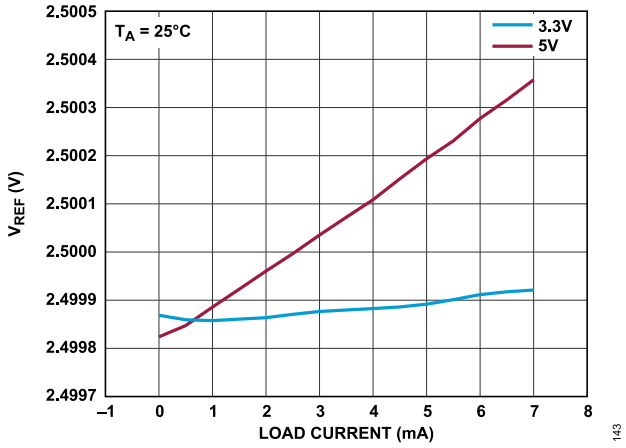


Figure 45. VREF vs. Load Current

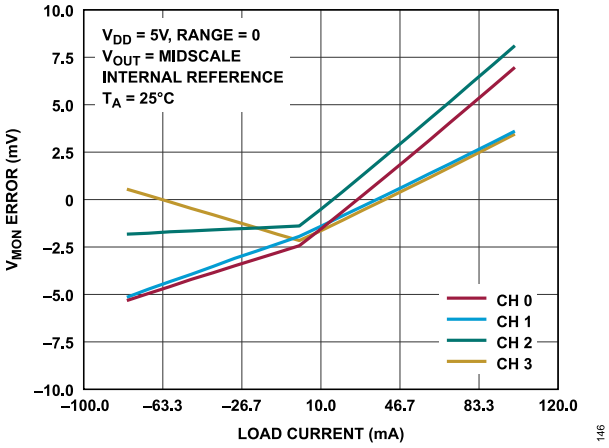


Figure 48. MUX_OUT V_{MON} Error vs. Output Current

TYPICAL PERFORMANCE CHARACTERISTICS

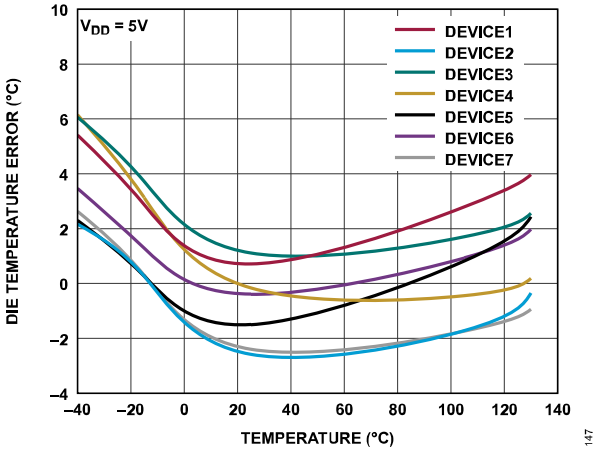


Figure 49. MUX_OUT Error vs. Internal Die Temperature

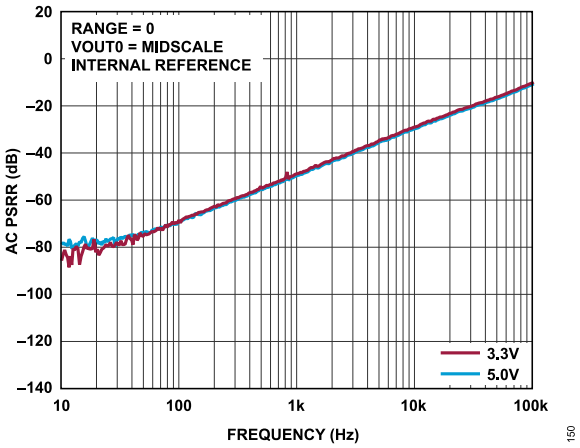


Figure 52. MUX_OUT AC PSRR vs. Frequency

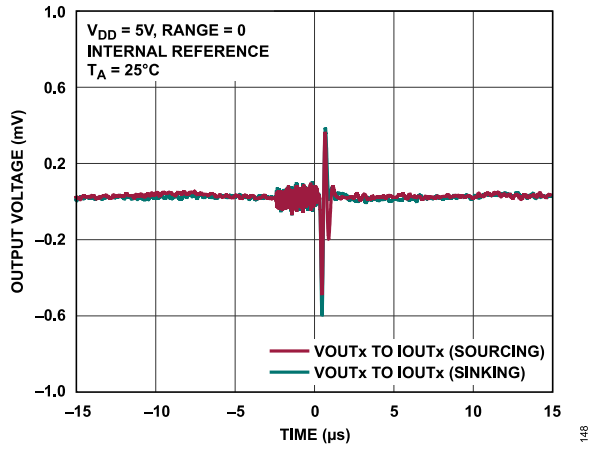


Figure 50. MUX_OUT to VOUTx Glitch

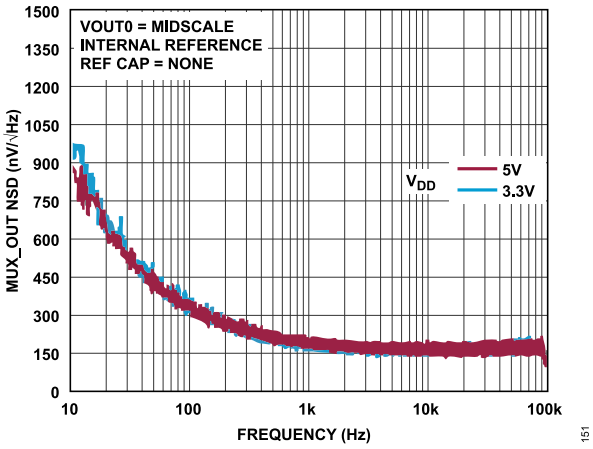


Figure 53. MUX_OUT NSD vs. Frequency

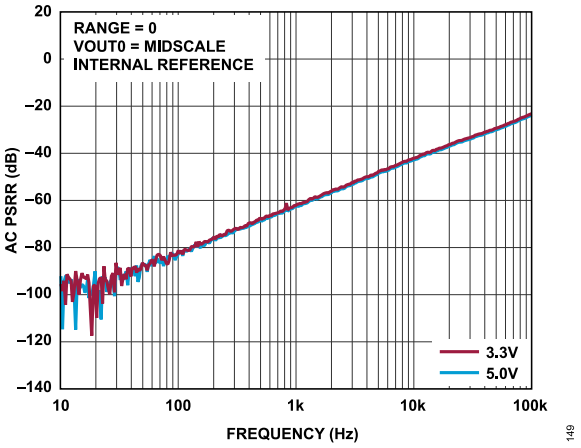


Figure 51. V_{OUT} AC PSRR vs. Frequency

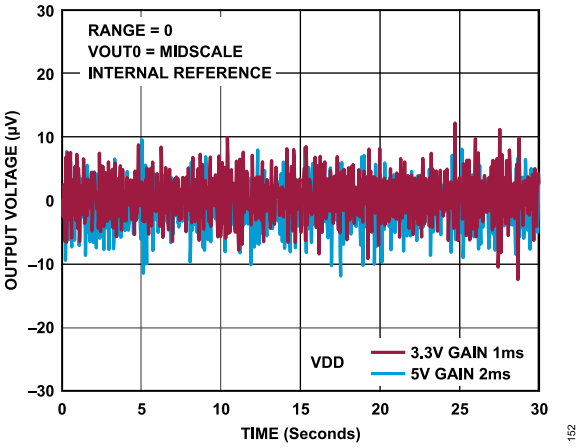


Figure 54. MUX_OUT 0.1Hz to 10Hz (1/f) Noise

TYPICAL PERFORMANCE CHARACTERISTICS

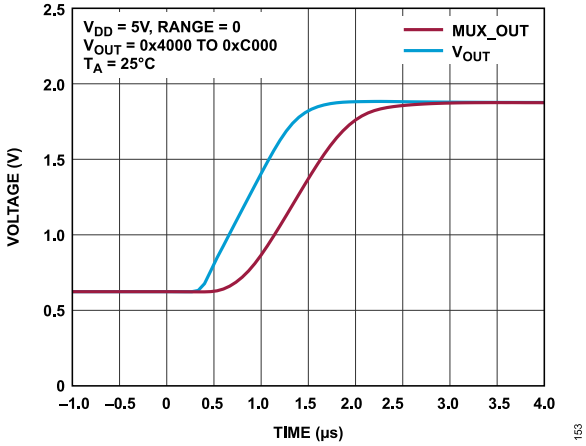


Figure 55. MUX_OUT vs. Output Voltage Transient, Rising

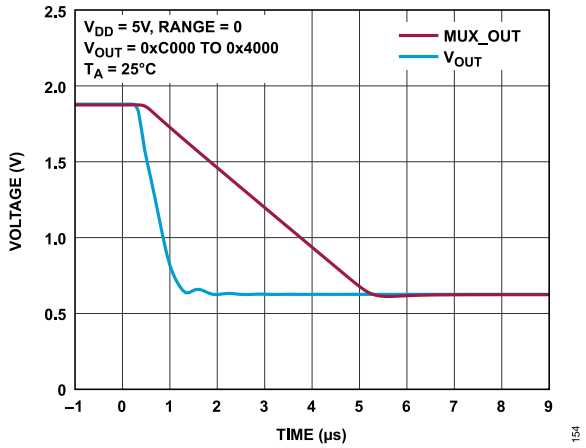


Figure 56. MUX_OUT vs. Output Voltage Transient, Falling

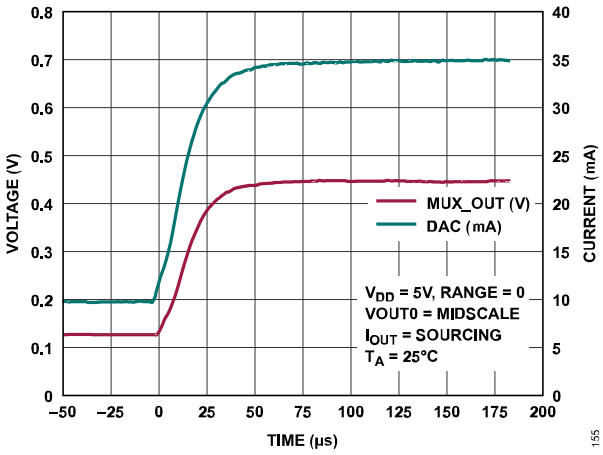


Figure 57. MUX_OUT Output Current Transient, Rising

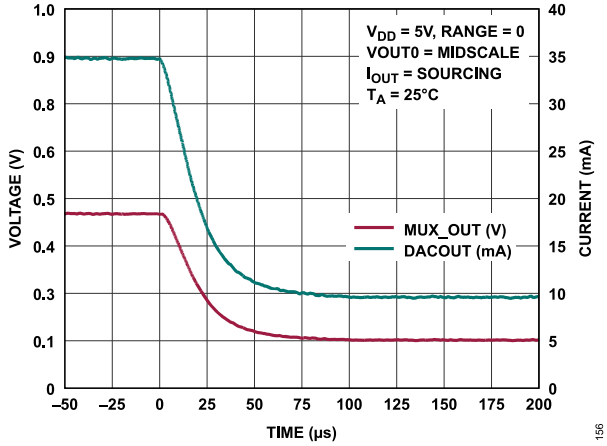


Figure 58. MUX_OUT vs. Output Current Transient, Falling

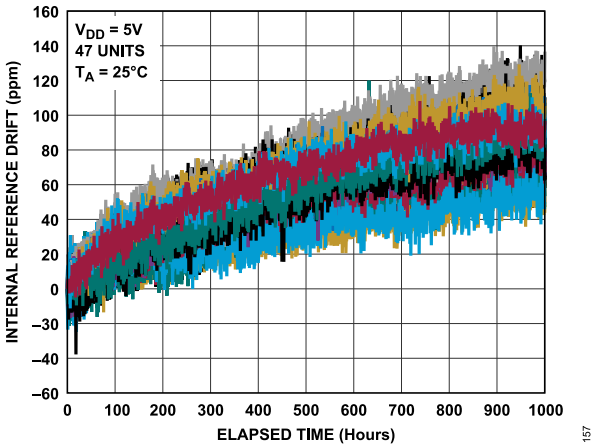


Figure 59. Reference Long Term Drift

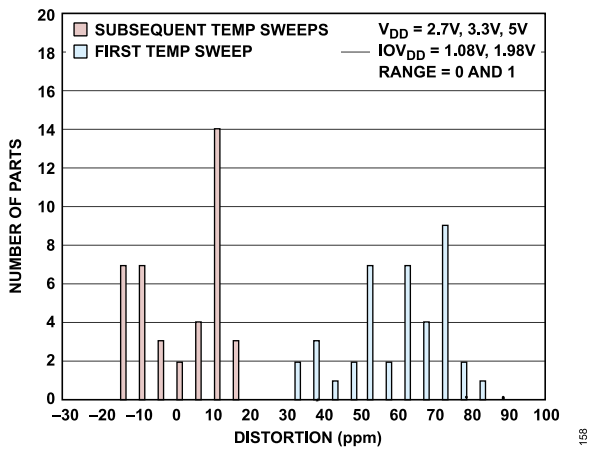


Figure 60. Reference Thermal Hysteresis

TYPICAL PERFORMANCE CHARACTERISTICS

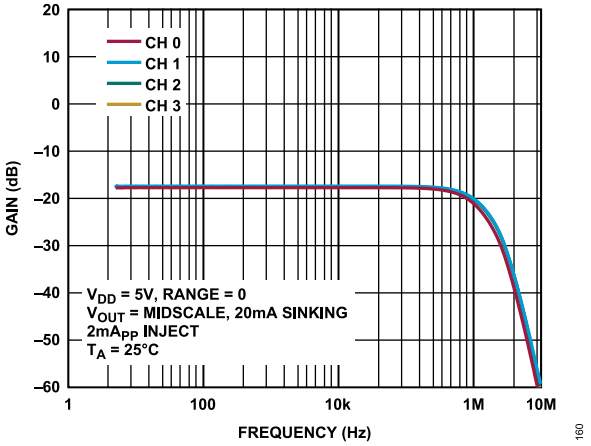


Figure 61. MUX_OUT Current Monitoring Frequency Response Across Channels

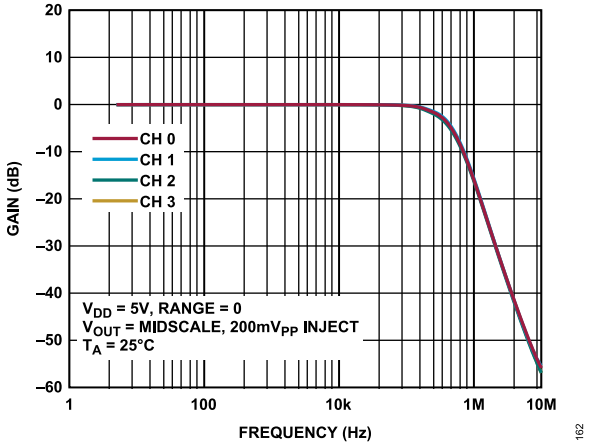


Figure 62. MUX_OUT Voltage Monitoring Frequency Response Across Channels

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured with Code 256 loaded in the DAC register. It can be negative or positive.

Offset Error Drift

The offset error drift is a measurement of the relative variation of the offset with temperature. It is expressed in ppm/°C. Total offset at a given temperature is calculated as

$$Deviation\ at\ T = Deviation\ at\ 25℃ + \frac{TC \times (T - 25) \times V_{RANGE}}{10^6} \quad (1)$$

Full-Scale and Zero-Scale Error

These errors measure the deviation from the ideal value at full scale and zero scale, at 25°C. The error is expressed as % of full-scale range (FSR).

Full-Scale and Zero-Scale Error Drift

These parameters measure the variation of the zero-scale and full-scale voltage as a function of the temperature, relative to the ideal zero-scale and full-scale voltages. They are expressed in ppm/°C. The total deviation over temperature is calculated using the same equation as offset error drift.

DC PSRR and AC PSRR

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in the supplies for midscale output of the DAC. For DC PSRR, it is measured in mV/V and VDD is varied by ±10%. While for AC PSRR, it is measured in dB and a ±200mV p-p AC sweep signal is injected on VDD.

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a given step change.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV × sec and is measured when the digital input code is changed by 1 LSB.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. Digital feedthrough is specified in nV × sec and measured with a full-scale code change on the data bus, which means from all 0s to all 1s and vice versa.

Output Noise Spectral Density

Noise spectral density is a measurement of the internally generated random noise. Noise is measured at the DAC output when it is loaded with the midscale code and center frequency set to 10kHz. It is measured in nV/$\sqrt{Hz}$.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and the attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as shown in the following equation:

$$TC = \left(\frac{V_{REF_MAX} - V_{REF_MIN}}{V_{REF_NOM} \times TEMP_RANGE}\right) \times 10^6 \quad (2)$$

where: V_{REF_MAX} is the maximum reference output measured over the total temperature range. V_{REF_MIN} is the minimum reference output measured over the total temperature range. V_{REF_NOM} is the nominal reference output voltage, 2.5V. TEMP_RANGE is the specified temperature range, −40°C to +125°C.

DC Crosstalk

DC crosstalk is the DC change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV. DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

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DIGITAL-TO-ANALOG CONVERTER

The AD3531/AD3531R are low power, 4-channel, 16-bit, voltage output DACs that operate on analog supply voltages of 2.7V to 5.5V and digital supply voltages of 1.08V to 1.98V. The AD3531/AD3531R have 5ppm/°C 2.5V on-chip references.

The AD3531/AD3531R offer versatile 4-wire serial interfaces compatible with classic SPI. See the Serial Interface section for more details.

DAC Channels

The AD3531/AD3531R contain 4 buffered voltage output DAC channels capable of sourcing 100mA and sinking 80mA of current. A simplified block diagram of a DAC channel is shown in Figure 63.

The output amplifier generates rail-to-rail voltages on its output, giving an ideal output range of 0 to VREF at OUTPUT_CONTROL_0(RANGE) = 0 (VDD > VREF), or 0 to 2 × VREF at OUTPUT_CONTROL_0(RANGE) = 1 (VDD > 2 × VREF). The headroom and footroom voltages, which are defined by the output current, should also be taken into consideration when selecting the appropriate output range and V_{DD}. The output slew rate is 1.1V/µs with a typical ¼ to ¾ settling time of 5µs while driving a load of 2kΩ in parallel with 200pF to GND.

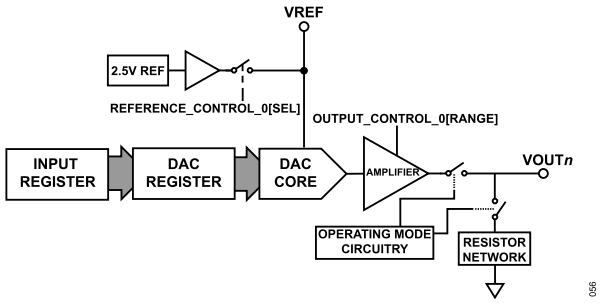


Figure 63. DAC Channel Block Diagram

Transfer Function

The conversion of the digital input code to the ideal output voltage is given by the following equation:

$$V_{OUTn} = V_{REF} \times \frac{D}{2^N} \times G \quad (3)$$

where:
V_{OUTn} is the output voltage seen at the selected DAC channel n.
V_{REF} is the voltage present on the VREF pin, which is an input by default. When the internal reference is turned on, this is equal to 2.5V.
D is the decimal equivalent of the straight binary code that is loaded into the DAC register (0 to 65535 for the AD3531/AD3531R).
N is the DAC resolution in bits.
G is the gain of the output amplifier. G = 1 if OUTPUT_CONTROL_0(RANGE) = 0 (default), and G = 2 if OUTPUT_CONTROL_0(RANGE) = 1.

Modes of Operation

There are four operating modes for each channel of the AD3531/AD3531R as listed in Table 9. These operating modes are software programmable via the MODE_CH_n[1:0] in the Output Operating Mode 0 Register and the Output Operating Mode 1 Register. Upon power-up or after a power-on reset, Operating Mode 3 is set by default, where the output amplifier is powered down and an effective resistance of 16kΩ can be seen from the VOUTn pin to GND.

Table 9. AD3531/AD3531R Operating Modes

Operating Modes	Output State	MODE_CH_n [1]	MODE_CH_n [0]
0	Normal operation	0	0
1	500Ω to GND	0	1
2	3.85kΩ to GND	1	0
3	16kΩ (default)	1	1

Entering into Mode 1, Mode 2, or Mode 3 will not affect other register settings or the read and write capability of those registers. The input or DAC registers can still be updated but will not reflect on the DAC output pins.

VOLTAGE REFERENCE

The AD3531R has an on-chip, buffered, 2.5V, 5ppm/°C reference available at the VREF pin that is capable of sourcing external loads up to +5mA.

By default, upon power-up or after a power-on reset, the VREF pin is configured as an input pin, and external reference voltage must be provided. The internal reference can be enabled by setting REFERENCE_CONTROL_0(SEL) to 1. See the the Reference Control 0 Register section for more details.

INTEGRATED MULTIPLEXER

The AD3531/AD3531R contain a 15:1 multiplexer that can output a voltage on the MUX_OUT pin representative of either the output voltage or output current of a chosen channel or the internal die temperature of the device. The monitor point can be set by configuring the SEL bits on the Multiplexer Input Select 0 Register. An invalid write MUX_OUT_SELECT_0(SEL) is ignored and the MUX_OUT_SELECT_0(SEL) value must not change.

The transfer function of the integrated multiplexer when voltage output monitor is selected is given by the equation below. A voltage output of VREF represents the full scale range of the DAC channel being monitored regardless of the OUTPUT_CONTROL_0(RANGE) value.

For OUTPUT_CONTROL_0(RANGE) = 0

$$V_{MEAS} = MUX_OUT \quad (4)$$

For OUTPUT_CONTROL_0(RANGE) = 1

$$V_{MEAS} = MUX_OUT \times 2 \quad (5)$$

where:

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V_{MEAS} is the measured voltage output of the selected channel. MUX_OUT is the voltage output on the MUX_OUT pin in volts.

The transfer function when using current output monitor:

$$I_{MEAS} = MUX_OUT \times 80\,mA/V \quad (6)$$

where:
I_{MEAS} is the measured current at the output of the selected channel.
MUX_OUT is the voltage output on the MUX_OUT pin in volts.

The internal die temperature can also be monitored through the MUX_OUT pin by setting the MUX_OUT_SELECT_0(SEL) to 0x19. The transfer function used to derive the measured temperature with internal reference enabled is given by the following equation:

$$T_{MEAS} = \frac{MUX_OUT - 0.44}{0.0016V/°C} \quad (7)$$

where:
T_{MEAS} is the measured internal die temperature in °C.
MUX_OUT is the voltage at the MUX_OUT pin in volts.

The integrated multiplexer has a buffered output capable of providing of ±5mA current. The errors of monitoring the VOUTn and IOUTn, where n is the channel number, are typically ±5mV and ±2mA, respectively.

DAC CORE FUNCTIONS

Each DAC channel has its own Input Register and DAC Register, as shown in Figure 63. Both registers are accessible through the serial interface. The DAC register stores digital code equivalent to the DAC output voltage while the input register acts as a temporary staging register before being passed on the DAC Register. With the LDAC function, one or more DAC registers could be updated in parallel with the data held in the input register.

The DAC registers can be written to directly, in which case the corresponding output updates immediately without the need for a hardware or software LDAC. Directly writing to the DAC register does not affect the data stored in the input register.

Writing to the MULTI_INPUT_CH register allows one or more input registers to be updated in a single write operation. The MULTI_INPUT_SEL_0 register determines which input register will be updated with the data written to the multiple input register. See the Multiple Input Select 0 Register section for additional information.

Similarly, writing to the MULTI_DAC_CH register allows one or more DAC registers to be updated in a single write operation. MULTI_DAC_INPUT_SEL_0 determines which DAC register will be updated with the data written to the multiple DAC register. See the Multiple DAC Select 0 Register section for more information.

To ensure that the DAC update is successful, DAC register updates should only occur once every 640ns. Refer to t_{L2} and t_{L3} from Table 5. An error flag will also be asserted when a DAC update write is unsuccessful which can be check by reading the UPDATE_ERR bit on the Status Control Register.

LDAC Function

The LDAC function is used to initiate the transfer of the contents of select input registers to the corresponding DAC registers, thereby updating one or more VOUT pins at the same time. The LDAC function can be executed by hardware through the LDACB pin or by software through SW_LDAC_TRIG_0 (Register Address 0xDD and Register Address 0xE1). Both hardware and software LDAC perform the same function.

Hardware LDAC

The AD3531/AD3531R has an active low LDACB pin that is falling edge sensitive. If the LDACB signal is brought low, the selected input register contents are transferred to corresponding DAC register. If LDACB is held low when writing to the device, the input registers appear transparent, and when an input register is written to, the DAC register is updated with the contents of the input register at the same time. When LDACB is held high, DAC codes can be written to any input registers without affecting the DAC output. Refer to Figure 4.

The Hardware LDAC Enable 0 Register is used to determine the DAC channels to be updated from the corresponding input registers when LDACB is active or asserted. By default, all DAC channels are selected and the HLD_EN_CH_n bitfields contain a 1. A 0 set on a HLD_EN_CH_n bitfield disables the hardware LDAC feature for the target DAC channel.

Software LDAC

The software LDAC function is synonymous to an LDACB falling edge. It provides a way to initiate a transfer of content between selected input registers to DAC registers through the serial interface via writing 1 to the SLD_TRIG_0 bit on either of the Software LDAC Trigger 0 Register (Register Address = 0xDD)or Software LDAC Trigger 0 Register (Register Address = 0xE1).

The Software LDAC Enable 0 Register is used to determine the DAC channels to be updated from the corresponding input registers when a software LDAC is performed. By default, all DAC channels are selected and the SW_LDAC_EN_0 bitfields contain a 1. A 0 set in a SW_LDAC_EN_0 bitfield disables the software LDAC feature for the target DAC channel.

POWER-ON RESET

On power-up the input and DAC data registers of every DAC channel are loaded with a zero code. Meanwhile, the POR circuit ensures that the DAC output amplifiers are powered down (see Mode 3 in the Modes of Operation section) until the output operating mode for the channel is changed. All registers are reset to their default values.

Hardware Reset

RESETB is an active low signal that is falling edge sensitive. Asserting RESETB sets these devices into the POR state. While

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RESETB is asserted, all SPI transactions and LDACB pulses are ignored, and the SDO output is in a high-Z state.

When RESETB is deasserted, the digital core initialization is performed and all DAC registers are reset to their default values. The digital core must finish the initialization procedure for around 150ns before any SPI transactions are performed.

Software Reset

The devices can also be reset using the serial interface by setting the SW_RESET bit and RESET_SW bit in the INTERFACE_CONFIG_A register. Both bit fields must be written at the same data phase to trigger a successful software reset. After the software reset transaction, the POR sequence and digital core initialization are performed, and all DAC registers are reset to the default values except for the INTERFACE_CONFIG_A register. Succeeding SPI transactions cannot be started until after around 150ns have passed after the last SCLK on the soft reset transaction. See the Timing Characteristics section for additional information.

SERIAL INTERFACE

The AD3531/AD3531R uses a 4-wire serial interface (CSB, SCLK, SDI, and SDO) that is compatible with classic SPI, QSPI, and MICROWIRE interface standards, as well as most digital signal processors (DSPs). See Figure 2 for a timing diagram of a typical write sequence. Data is sampled by the AD3531/AD3531R on the positive edge of the clock. This corresponds to either SPI Mode 0 or Mode 3.

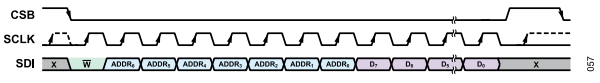


Figure 64. Classic SPI Write

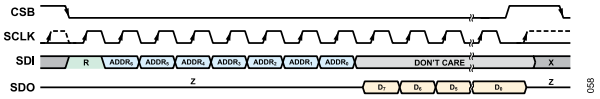


Figure 65. Classic SPI Read

SPI Frame Synchronization

The CSB pin frames data during a SPI transaction. A falling edge on the CSB enables the digital interface and initiates an SPI transaction. Each SPI transaction consists of at least one instruction phase and one data phase. For all SPI transactions, data is aligned MSB first. Deasserting the CSB during a SPI transaction terminates part or all of the data transfer and disables the digital interface. If the CSB is deasserted (returned high) after one or more registers are written, completed registers are written or read, but any partially written register is aborted. Figure 64 and Figure 65 show detailed timing diagrams for performing register reads and writes via the SPI interface.

Instruction Phase

Every SPI frame starts with the instruction phase. The instruction phase immediately follows the falling edge of the CSB that initiates the SPI transaction. The instruction phase consists of a read/write bit (R/$\overline{W}$) followed by a register address word. Setting R/$\overline{W}$ low initiates a write instruction, whereas setting R/$\overline{W}$ high initiates a read instruction.The register address word is 15 bits in length.

Data Phase

The data phase immediately follows the instruction phase (as shown in Figure 66 and Figure 67. The data phase can include the data for a single-byte register, a multibyte register, or multiple registers.

If the data phase of a SPI write transaction does not include the entire byte of data for the register being updated, the contents of the register are not updated, and INTERFACE_STATUS_A(CLOCK_COUNT_ERR) is set.

Multibyte Registers

Besides the 1-byte registers, the AD3531/AD3531R also contain registers with two bytes of data stored in adjacent addresses that are referred to as multibyte registers. When writing to a multibyte register, all bytes must be accessed in a single SPI transaction. For this reason, the INTERFACE_CONFIG_C(STRICT_REGISTER_ACCESS) is read only and set to 1. A write transaction to a multibyte register takes effect after the 16th SCLK edge of the data phase.

The address of a multibyte register always depends on INTERFACE_CONFIG_A(ADDR_ASCENSION). With addresses descending, the first byte accessed in the data phase must be the most significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next lowest address. With addresses ascending, the first byte accessed in the data phase must be the least significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next highest address.

For example, the DAC_CH0 register is two bytes long, and the addresses of its least significant byte and most significant byte are 0xD2 and 0xD3, respectively. Figure 66 and Figure 67 show read transactions of this register for address ascending and descending mode, respectively.

Address direction is selected with INTERFACE_CONFIG_A(ADDR_ASCENSION). If this bit is set to 0, the address decrements after each byte is accessed. If this bit is set to 1, the address increments after each byte is accessed. If a SPI write transaction to a multibyte register is attempted on a per byte basis, the register contents are not updated on the device, and INTERFACE_STATUS_A(REGISTER_PARTIAL_ACCESS_ERR) is set.

This device contains the following multibyte registers: DAC_CHn, Input_CHn, MULTI_DAC_CH, and MULTI_INPUT_CH.

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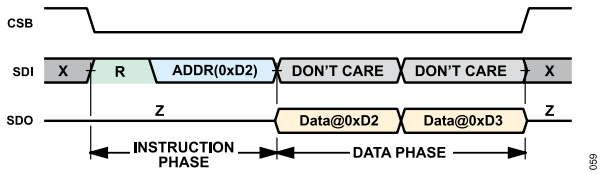


Figure 66. Multibyte Read in Ascending Mode

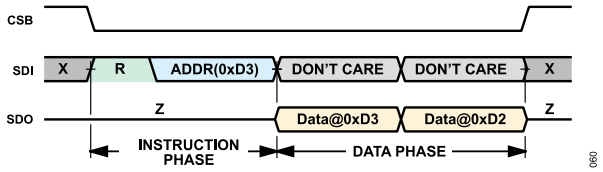


Figure 67. Multibyte Read in Descending Mode

Single Instruction Mode

When streaming mode is disabled, and single instruction mode is enabled. In single instruction mode, the data phase consists of data for a single register, and each data phase must be followed by a new instruction phase (even if CSB remains low). Single instruction mode allows the digital host to quickly read from and write to registers with nonadjacent addresses in a single SPI frame (see Figure 68), whereas streaming mode only allows either reading or writing to contiguous registers without pulsing CSB high to initiate a new instruction phase.

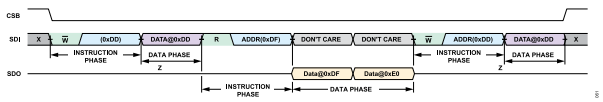


Figure 68. Single Instruction Mode

When accessing multibyte registers in single instruction mode, data phase should include all 2 bytes or 16 SCLK cycles, and the register address order is dependent on INTERFACE_CONFIG_A(ADDR_ASCENSION).

Streaming Mode

When the single instruction mode is disabled, and streaming mode is enabled. In streaming mode, multiple registers with adjacent addresses can be accessed with a single instruction phase and data phase, allowing efficient access of contiguous regions of memory (for example, during initial device configuration). The streaming mode is selected by default.

When in streaming mode, each SPI frame consists of a single instruction phase and the following data phase contains data for multiple registers with adjacent addresses. A starting register address is specified by the digital host in the instruction phase, and this address is automatically incremented or decremented (based on the address direction setting) after each byte of data is accessed. Therefore, the data phase can be multiple bytes long, and each consecutive byte of read or write data corresponds to the next highest or lowest register address (for ascending and descending address direction, respectively).

When writing to a multibyte register in streaming mode with address ascending, the LSB of the register must be addressed in the instruction phase and data must be provided starting from the LSB in the data phase. When writing to a multibyte register in streaming mode with the address descending, the user must start addressing the most significant byte of the register in the instruction phase and provide data starting from the most significant byte in the data phase.

When reading from a multibyte register in streaming mode with address descending, read back the data starting from the MSB. When reading from a multibyte register in streaming mode with address ascending, read back data starting from the LSB.

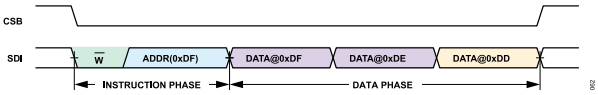


Figure 69. Streaming Mode SPI transfer

The STREAM_MODE register can be used to specify a set of consecutive registers to loop through in the data phase. Looping allows the digital host to repeatedly read from or write to a set of registers as efficiently as possible.

If the address direction is set to descending, the address decrements until it reaches Address 0x00. On the subsequent byte access, the address is set to the highest valued byte address available (0xF9).

If address direction is set to ascending, the address increments until it reaches the highest valued byte address available (0xF9). On the subsequent byte access, the address is reset to 0x00.

If STREAM_MODE is set to a value other than 0, looping is enabled, and the value in STREAM_MODE sets the number of bytes to be accessed in a single data phase before the byte address resets to the one specified in the instruction phase.

The value of the STREAM_MODE(LOOP_COUNT) register can be kept or returned to the default value of 0 when the frame transaction is completed, that is, the CSB is brought high. The STREAM_MODE register behavior is controlled by TRANSFER_CONFIG(KEEP_STREAM_LENTH_VAL).

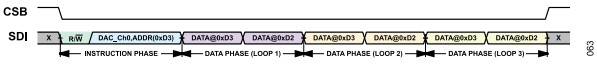


Figure 70. Looping Enabled with LOOP_COUNT = 2

When using STREAM_MODE, be aware of the DAC update timings mentioned in DAC Core Functions.

CRC ERROR DETECTION

The AD3531/AD3531R DACs feature optional cyclic redundancy checks (CRCs) to provide error detection for SPI transactions between the digital host and the DAC (target). The CRC error detection is disabled by default. The CRC error detection allows the SPI host and targets to detect bit transfer errors with significant

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reliability. The CRC algorithm involves using a seed value and polynomial division to generate a CRC code. The controller and target both calculate the CRC code independently to determine the validity of transferred data.

This DAC uses the CRC-8 standard with the following polynomial:

$$x^8 + x^2 + x + 1 \quad (8)$$

CRC error detection is enabled with the CRC_EN and CRC_EN_B bits in the INTERFACE_CONFIG_C register. The value of CRC_EN is only updated if CRC_EN_B is set to the CRC_EN inverted value in the same register write instruction. Therefore, to enable the CRC, the CRC_EN must therefore be set to 0b01 while CRC_EN_B is set to 0b10 in the same write transaction.

To disable the CRC, the CRC_EN must be set to 0b00 and the CRC_EN_B is set to 0b11 in the same write transaction.

Writing inverted values to two separate fields reduces the chances of CRC being enabled in error. The CSB must be brought high at the end of the enable/disable write. The first CRC code must be included after the register write/read data, immediately following the register write transaction enabling the CRC. A register write transaction that disables the CRC must still include the CRC code on SDI, but the following transaction does not require the CRC code.

Figure 71 and Figure 72 show how a CRC code is appended to the write or read, respectively, for the digital host or DAC to validate the data. For register writes, the digital host must generate the CRC using the calculation described in Equation 8. For register reads, the host must also send the correct CRC byte that is checked by the DAC. The first byte of data sent contributes to the CRC calculation. Therefore, a value of 0x00 is recommended. In the same read transaction, the DAC provides the CRC code for the digital host to verify.

When accessing multibyte registers with the CRC error detection enabled, the CRC code is placed after all bytes of register data. When the CRC error detection is enabled, the DAC does not update its register contents in response to a register write transaction unless it receives a valid CRC code at the end of the register data on the SDI. If the CRC code is invalid, or the digital host fails to transmit the CRC code, the AD3531/AD3531R do not update the register contents, and the CRC_ERR flag in the INTERFACE_STATUS_A register is set. The CRC_ERR flag is write-1-to-clear (W1C) and the correct CRC is required for the write to clear to take effect.

Table 14 shows the seed value used in the CRC code calculation and how it is transmitted for both single instruction mode and streaming mode. When using single instruction mode, every CRC code in a SPI frame uses 0xA5 as the seed value to prevent stuck at fault conditions for Address 0x0000.

When using the streaming mode, the first CRC code in a SPI frame also uses 0xA5 as the seed value, but subsequent CRC codes in the same frame are calculated using the LSB of the register address being accessed in the SPI transaction as the seed value.

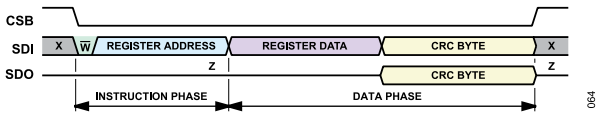


Figure 71. SPI Write with CRC Enabled

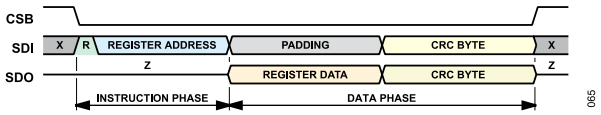


Figure 72. SPI Read with CRC Enabled

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD3531/AD3531R does not have any restrictions for power supply sequencing. The outputs are maintained at POR state with a known pull-down resistance until proper register configurations are set.

The AD3531/AD3531R must have an ample supply bypassing of 10µF in parallel with 0.1µF on each supply, located as close to the package as possible (ideally directly against the device). The VREF pin, on the other hand, has a maximum capacitive load of 0.5nF as stated in Table 2. The 10µF capacitors are the tantalum bead type. The 0.1µF and 0.5nF capacitors must have low effective series resistance (ESR) and low effective series inductance (ESL). Common ceramic capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

LAYOUT GUIDELINES

The pin configuration of the AD3531/AD3531R is arranged in a way that facilitates optimal layout, an example of which is shown in Figure 73. Most digital high speed lines are located on one side of the chip, with the analog functions of each DAC symmetrically distributed along the other three sides. This arrangement allows routing of the digital lines straight away from the analog functions.

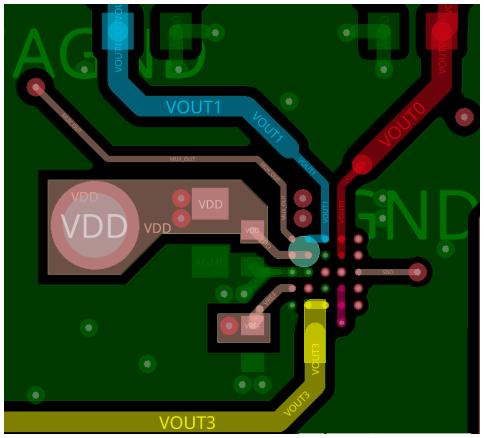


Figure 73. Evaluation Board Layout

The following are some PCB design recommendation to obtain the best performance for the AD3531/AD3531R:

- Ensure that the power supply line has as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line.
- A low impedance analog ground plane and star grounding techniques are recommended. It is advised to keep the ground layer continuous to minimize ground resistance.
- Shield clocks and other fast switching digital signals from other parts of the board by using a digital ground.
- Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at 45° or 90° angles to each other to reduce feedthrough effects through the board.
- For clock rates around the device maximum of 50MHz, it is advised to add series resistors near the source I/O pins. Values from 22Ω to 100Ω are commonly used and would help improve signal integrity by reducing ringing and reflections caused by the fast signal transitions.

HEADROOM AND FOOTROOM

Headroom and footroom refers to the voltage difference between the supply voltage and the intended output voltage of the DAC for a specified output load current. If the supply voltage headroom or footroom is insufficient, the pass element of the integrated output amplifier of the DAC acts like a resistor instead of an ideal switch. This causes the output voltage to drop as the load current increases.

The AD3531/AD3531R has a very low typical headroom requirement of 25mV/20mA and 50mV/20mA for footroom. The typical performance is shown in Figure 21. The voltage drop is generally linear in nature, hence, can be calculated by multiplying the load current by the headroom/footroom specification. For example, we have a 5V supply and a 5V setting at the output of the DAC. If the DAC starts sourcing current of 30mA to a load, the DAC output voltage would be around 4.963V.

For a footroom example, a DAC output that is sinking 30mA of current would result to an output voltage that is 75mV above ground potential.

DAC UPDATE

There are multiple ways of updating the DAC_CHn registers, hence VOUTn, Figure 74 shows a flow chart of options to update DAC_CHn registers considering several factors such as single vs. multiple channel updates, similar vs. unique data, and the mode of LDAC.

APPLICATIONS INFORMATION

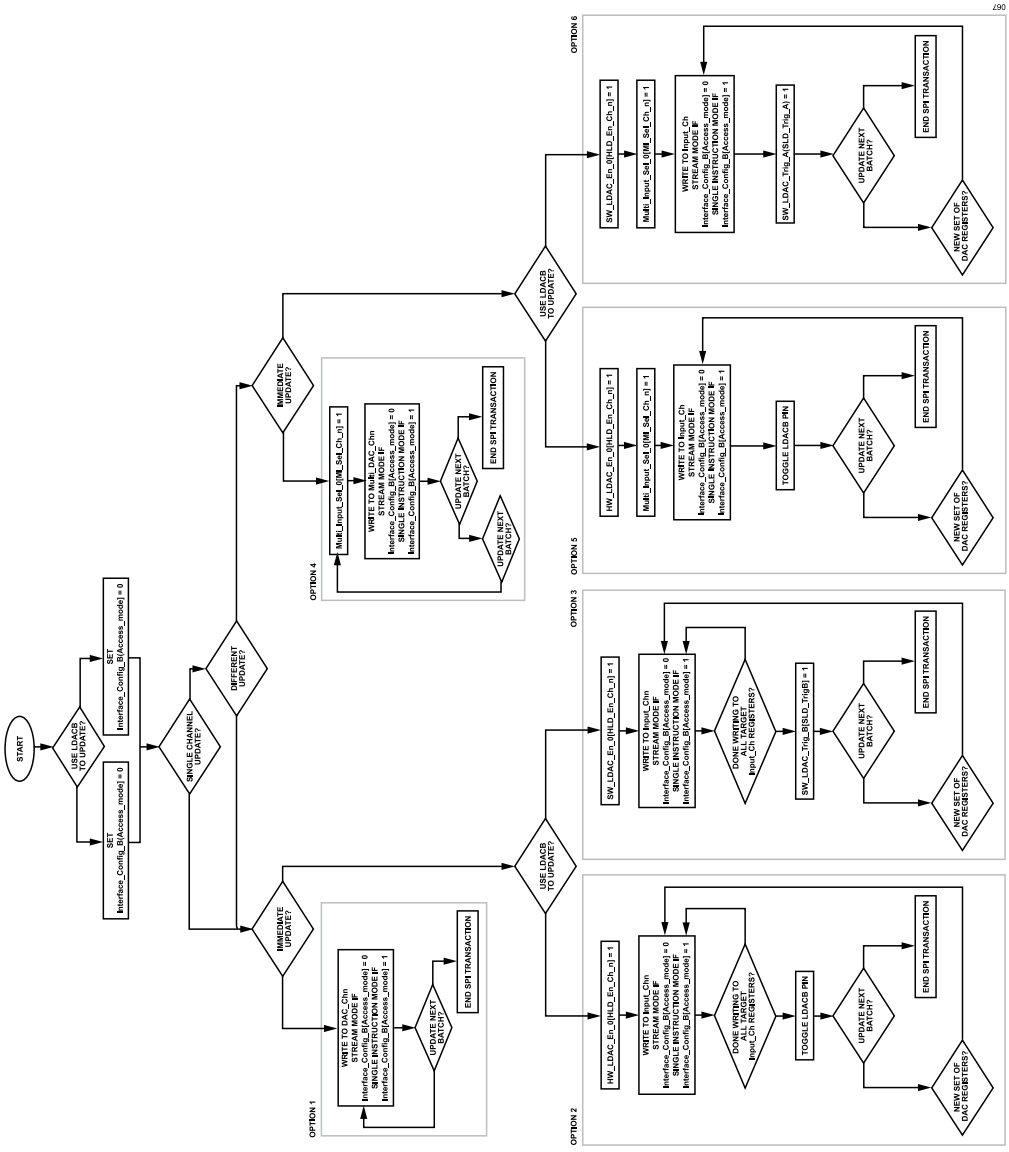


Figure 74. DAC Update Flowchart

Option 1 (Immediate Update, Unique Data, No LDAC, and Single and Multiple Channels)

Option 1 allows the immediate update of the DAC_CHn registers after writing the whole 16-bit data. An LDAC is not required.

Option 1 is applicable to both single channel and multiple channel updates in single instruction or stream modes.

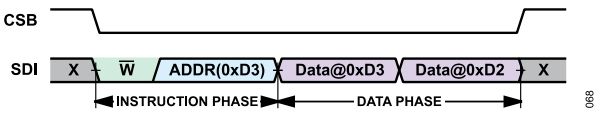


Figure 75. Option 1 Example: Write to DAC_CH0 Register; Single Instruction Mode and Address Descending

A single instruction is sent with the descending mode selected. The higher address of the multibyte register is called on the instruction phase (0xD3, DAC_CH0 register, followed by two 8-bit data) that updates the output immediately after the last SCLK.

Option 2 (Controlled Update, Unique Data, Hardware LDAC, and Single and Multiple Channels

Option 2 allows controlled update timing of the DAC_CHn registers from the INPUT_CHn registers through a hardware LDAC.

Applicable to both single channel and multiple channel updates in single instruction or stream modes.

APPLICATIONS INFORMATION

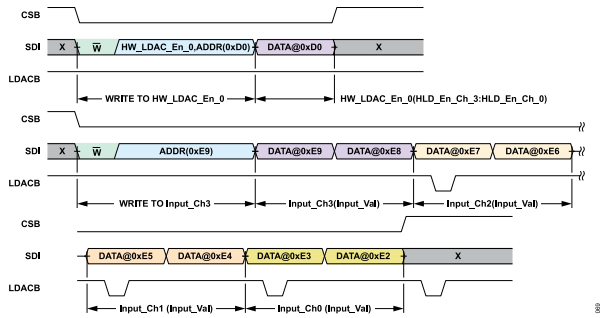


Figure 76. Option 2 Example: Write to Input_Ch3 to Input_Ch0 Registers; Hardware LDAC Enabled; Stream Mode and Address Descending

A single instruction is sent to write to the HW_LDAC_EN_0 register, enabling hardware LDAC for the selected channels. Then, a stream mode is initiated, in default descending mode, writing to the INPUT_CH3 first up to INPUT_CH0. The LDACB is asserted at the end of the stream updating the DAC registers and the DAC output (if the correct LDACB timing is observed).

Option 3 (Controlled Update, Unique Data, Software LDAC, and Single and Multiple Channels)

Option 3 allows controlled update timing of the DAC_CHn registers from the INPUT_CHn registers through the software LDAC.

This option is applicable to both single channel and multiple channel updates in single instruction and stream modes.

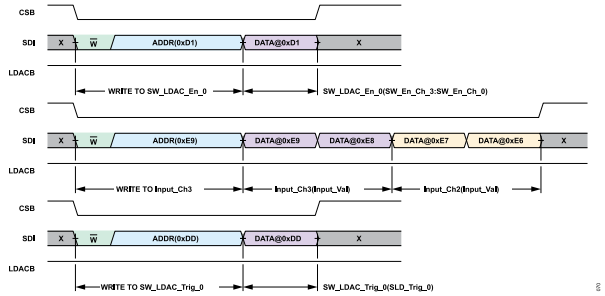


Figure 77. Option 3 Example: Write to INPUT_CH3 and INPUT_CH2 Registers, with a software LDAC, Stream Mode and Address Descending

Similar to Option 2, except, a software LDAC function is used instead of a hardware LDAC. The SW_LDAC_EN_0 register determines which channel gets affected by a software LDAC command. The DAC registers and DAC outputs are updated with the input data written after the last SCLK of the SW LDAC command.

Option 4 (Immediate Update, Same Data, No LDAC, and Multiple Channels)

Option 4 allows the immediate and simultaneous update of multiple DAC_CHn registers identified by MULTI_DAC_SEL_0(MD_SEL_CH_n) bitfields with the same data. Data is contained in MULTI_DAC_CH register and update is initiated after writing the whole 16-bit data. An LDAC is not required.

Option 4 is ideal for multiple channel updates in both single instruction and stream mode.

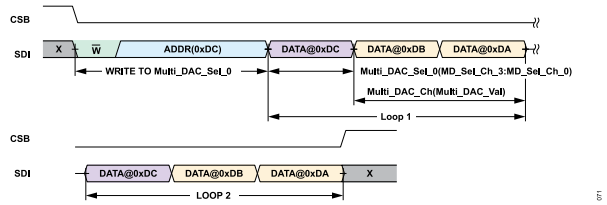


Figure 78. Option 4 Example: Write to MULTI_DAC_CHn Register, Stream Mode (Loop) and Address Descending

A write instruction is sent to Multi_DAC_Sel_0 register, enabling multi DAC function for the selected channels. With stream mode descending enabled, the next commands are the data for the adjacent multi-byte register 0xDB (and 0xDA) MULTI_DAC_CH. Assuming that STREAM_MODE(LOOP_COUNT) is set to 0x3, the succeeding data stream loops back to the start address, 0xDC, and repeats the process, until CSB is deasserted.

Option 5 (Controlled Update, Same Data, Hardware LDAC, and Multiple Channels)

Option 5 allows controlled update timing of multiple DAC_CHn registers identified by MULTI_INPUT_SEL_0(MI_SEL_CH_n) and HW_LDAC_EN_0(HLD_EN_CH_n) bitfields with the same data. Data is contained in MULTI_INPUT_CH register and update is initiated by providing a valid LDACB pulse.

Option 5 is ideal for multiple channel updates in both single instruction and stream modes.

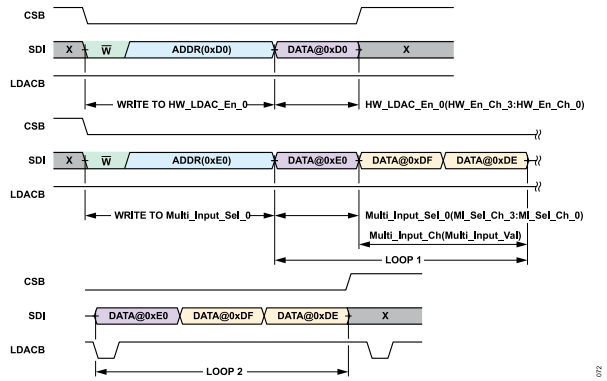


Figure 79. Option 5 Example: Write to MULTI_INPUT_CH Register with a Hardware LDAC, Stream Mode (Loop) and Address Ascending

Option 5 is similar to Option 2 except this option makes use of the MULTI_INPUT_SEL_0 and MULTI_INPUT_CH registers to select and update the input registers of multiple DAC channels. The LDACB is asserted after each loop ends, updating the DAC registers and the DAC outputs (when correct LDAC is observed).

APPLICATIONS INFORMATION

Option 6 (Controlled Update, Same Data, Software LDAC, and Multiple Channel)

Option 6 allows immediate and simultaneous update of multiple DAC_CHn registers identified by MULTI_INPUT_SEL_0(MI_SEL_CH_n) and SW_LDAC_EN_0(SLD_EN_CH_n) bitfields with the same data. Data is contained in MULTI_INPUT_CH register and is initiated through the software LDAC.

Option 6 is ideal for multiple channel updates in both single instruction and stream modes.

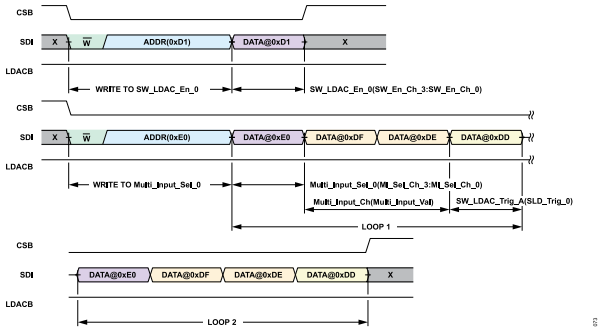


Figure 80. Option 6 Example: Write to Multi_Input_Ch Register with a Software LDAC, Stream Mode (Loop) and Address Ascending

Option 6 is the same as Option 5, except a software LDAC function is used instead of a hardware LDAC function. The SW_LDAC_EN_0 register determines which channel is affected by a software LDAC command.

REGISTER SUMMARY

Table 10. AD3531/AD3531R Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET	RESERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			RESET_SW	0x10	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	RESERVED			SHORT_INSTRUCTION	RESERVED			0x00	R/W
0x02	DEVICE_CONFIG	[7:0]	RESERVED						OPERATING_MODES		0x00	R/W
0x03	CHIP_TYPE	[7:0]	RESERVED				CHIP_TYPE				0x08	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x01	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				Device_REVISION				0x01	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		Version						0x84	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x0E	STREAM_MODE	[7:0]	LOOP_COUNT								0x00	R/W
0x0F	TRANSFER_CONFIG	[7:0]	RESERVED					KEEP_STREAM_LENGTH_VAL	RESERVED		0x00	R/W
0x10	INTERFACE_CONFIG_C	[7:0]	CRC_ENABLE		STRICT_REGISTER_ACCESS	RESERVED	ACTIVE_INTERFACE_MODE		CRC_ENABLEB		0x23	R/W
0x11	INTERFACE_STATUS_A	[7:0]	NOT_READY_ERR	RESERVED		CLOCK_COUNT_ERR	CRC_ERR	RESERVED	REGISTER_PARTIAL_ACCESS_ERR	RESERVED	0x00	R/W
0x20	OUTPUT_OPERATING_MODE_0	[7:0]	MODE_CH_3		MODE_CH_2		MODE_CH_1		MODE_CH_0		0xFF	R/W
0x2A	OUTPUT_CONTROL_0	[7:0]	RESERVED					RANGE	RESERVED		0x00	R/W
0x3C	REFERENCE_CONTROL_0	[7:0]	RESERVED							SEL	0x00	R/W
0x93	MUX_OUT_SELECT_0	[7:0]	RESERVED			SEL					0x00	R/W
0xC2	STATUS_CONTROL	[7:0]	RESERVED				UPDATE_ERR	RESET_WARNING	INTERFACE_ERR	DEVICE_NOT_READY	0x04	R/W
0xD0	HW_LDAC_EN_0	[7:0]	RESERVED				HLD_EN_CH_3	HLD_EN_CH_2	HLD_EN_CH_1	HLD_EN_CH_0	0xFF	R/W
0xD1	SW_LDAC_EN_0	[7:0]	RESERVED				SLD_EN_CH_3	SLD_EN_CH_2	SLD_EN_CH_1	SLD_EN_CH_0	0xFF	R/W
0xD3 TO 0xD9 by 2[1]	DAC_CHn	[15:8]	DAC_VAL[15:8]								0x0000	R/W
		[7:0]	DAC_VAL[7:0]									
0xDB[1]	MULTI_DAC_CH	[15:8]	MULTI_DAC_VAL[15:8]								0x0000	R/W
		[7:0]	MULTI_DAC_VAL[7:0]									
0xDC	MULTI_DAC_SEL_0	[7:0]	RESERVED				MD_SEL_CH_3	MD_SEL_CH_2	MD_SEL_CH_1	MD_SEL_CH_0	0xFF	R/W
0xDD	SW_LDAC_TRIG_0	[7:0]	SLD_TRIG_0	RESERVED							0x00	R/W
0xDF[1]	MULTI_INPUT_CH	[15:8]	MULTI_INPUT_VAL[15:8]								0x0000	R/W
		[7:0]	MULTI_INPUT_VAL[7:0]									

REGISTER SUMMARY

Table 10. AD3531/AD3531R Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0xE0	MULTI_INPUT_SEL_0	[7:0]	RESERVED				MI_SEL_CH_3	MI_SEL_CH_2	MI_SEL_CH_1	MI_SEL_CH_0	0xFF	R/W
0xE1	SW_LDAC_TRIG_0	[7:0]	SLD_TRIG_0	RESERVED							0x00	R/W
0xE3 to 0xE9 by 2[1]	INPUT_CHn	[15:8]	INPUT_VAL[15:8]								0x0000	R/W
		[7:0]	INPUT_VAL[7:0]									

[1] See for Multibyte Registers more details

REGISTER DETAILS

INTERFACE CONFIGURATION A REGISTER

Address: 0x00, Reset: 0x10, Name: INTERFACE_CONFIG_A

INTERFACE Configuration Settings

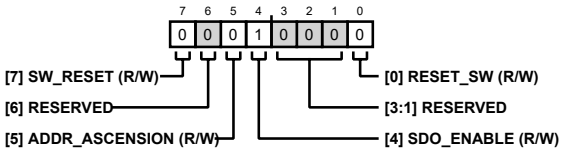


Table 11. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET	First of Two of SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written at the same time to trigger a software reset of the part. All registers except for this register are reset to their default values.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_ASCENSION	Determines Sequential Addressing Behavior. 0: Address is Decremented by One When Streaming. 1: Address is Incremented by One When Streaming.	0x0	R/W
4	SDO_ENABLE	SDO Pin Enable. 0: SDO pin disabled 1: SDO pin enabled	0x1	R/W
[3:1]	RESERVED	Reserved.	0x0	R
0	RESET_SW	Second of Two of SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written at the same time to trigger a software reset of the part. All registers except for this register are reset to their default values.	0x0	R/W

INTERFACE CONFIGURATION B REGISTER

Address: 0x01, Reset: 0x00, Name: INTERFACE_CONFIG_B

Additional INTERFACE Configuration Settings

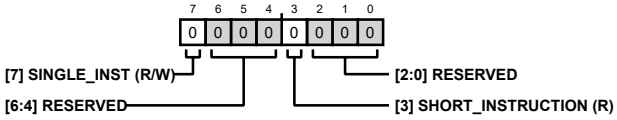
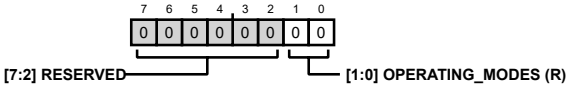


Table 12. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INST	Select Streaming or Single Instruction Mode. 0: Streaming Mode is Enabled. The address increments/decrements as successive data bytes are received. 1: Single Instruction Mode is Enabled.	0x0	R/W
[6:4]	RESERVED	Reserved.	0x0	R
3	SHORT_INSTRUCTION	Instruction Phase Address	0x0	R
[2:0]	RESERVED	Reserved.	0x0	R

DEVICE CONFIGURATION REGISTER

Address: 0x02, Reset: 0x00, Name: DEVICE_CONFIG



REGISTER DETAILS

Table 13. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	OPERATING_MODES	Operating mode. Read only. 00: Normal Operating Mode. 11: Low Power Mode.	0x0	R

CHIP TYPE REGISTER

Address: 0x03, Reset: 0x08, Name: CHIP_TYPE

The chip type is used to identify the family of ADI devices a given device belongs to. It should be used in conjunction with the product ID to uniquely identify a given product.

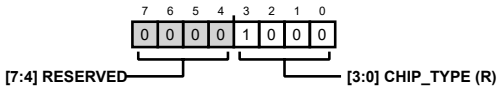


Table 14. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Precision DAC.	0x8	R

PRODUCT ID LOW REGISTER

Address: 0x04, Reset: 0x01, Name: PRODUCT_ID_L

Low byte of the product ID

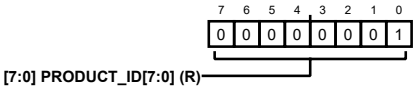


Table 15. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	This is Device Chip Type/Family. The product ID should be used in conjunction with Chip Type to identify a product.	0x1	R

PRODUCT ID HIGH REGISTER

Address: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

High byte of the product ID

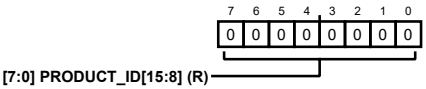


Table 16. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Device Chip Type/Family. The product ID should be used in conjunction with the chip type to identify a product.	0x0	R

REGISTER DETAILS

CHIP GRADE REGISTER

Address: 0x06, Reset: 0x01, Name: CHIP_GRADE

Identifies product variations and device revisions

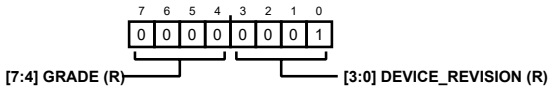


Table 17. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	Device Performance Grade.	0x0	R
[3:0]	DEVICE_REVISION	Device Hardware Revision.	0x1	R

SCRATCH PAD REGISTER

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

This may be used to test writes and reads

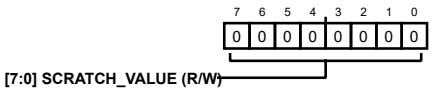


Table 18. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Software can write to and read from this location without any device side effects.	0x0	R/W

SPI REVISION REGISTER

Address: 0x0B, Reset: 0x84, Name: SPI_REVISION

Indicates the SPI interface revision

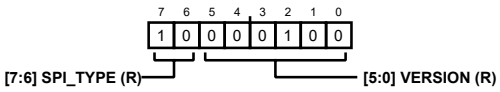


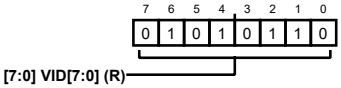
Table 19. Bit Descriptions for SPI_REVISION

Bits	Bit Name	Description	Reset	Access
[7:6]	SPI_TYPE	Always Reads as 0x2.	0x2	R
[5:0]	VERSION	SPI Version.	0x4	R

VENDOR ID LOW REGISTER

Address: 0x0C, Reset: 0x56, Name: VENDOR_L

Low byte of the vendor ID



REGISTER DETAILS

Table 20. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Analog Devices Vendor ID.	0x56	R

VENDOR ID HIGH REGISTER

Address: 0x0D, Reset: 0x04, Name: VENDOR_H

High byte of the vendor ID

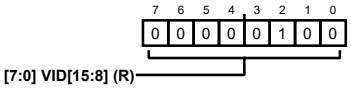


Table 21. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Analog Devices Vendor ID.	0x4	R

STREAM MODE REGISTER

Address: 0x0E, Reset: 0x00, Name: STREAM_MODE

Defines the length of the loop when streaming data

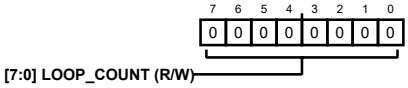


Table 22. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Sets the Data Byte Count Before Looping to Start Address. When streaming data, a non-zero value sets the number of data bytes written before the address loops back to the start address. A maximum of 255 bytes may be written using this approach. A value of 0x00, disables the loop back, so that addressing wraps around at the upper/lower limits of memory.	0x0	R/W

TRANSFER CONFIGURATION REGISTER

Address: 0x0F, Reset: 0x00, Name: TRANSFER_CONFIG

Controls how data moves between controller and target registers

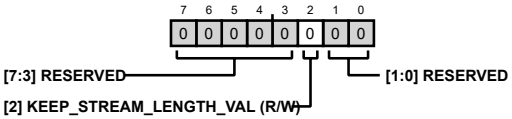


Table 23. Bit Descriptions for TRANSFER_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	KEEP_STREAM_LENGTH_VAL	Whet Set the Loop Counter Does Not Reset on CSB Rising Edge.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

INTERFACE CONFIGURATION C REGISTER

Address: 0x10, Reset: 0x23, Name: INTERFACE_CONFIG_C

REGISTER DETAILS

Additional Interface Configuration Settings

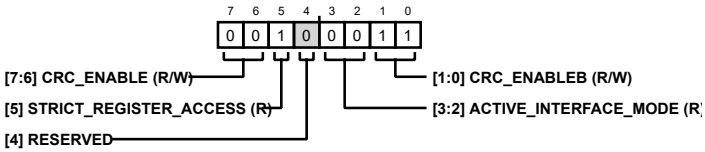


Table 24. Bit Descriptions for INTERFACE_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	CRC_ENABLE	CRC Enable. Written to enable/disable the use of CRC on the interface. The CRC_ENABLEB bit field must also be written with the inverted value of this bit field for the CRC to be enabled. 00: CRC Disabled. 01: CRC Enabled.	0x0	R/W
5	STRICT_REGISTER_ACCESS	Multibyte Registers Must Be Read/Written in Full. When this mode is enabled, all bytes of a multibyte register must be read/written in full. 0: Normal mode, no access restrictions. 1: Strict mode, multibyte registers require all bytes accessed.	0x1	R
4	RESERVED	Reserved.	0x0	R
[3:2]	ACTIVE_INTERFACE_MODE	Active Mode the SPI Interface is Operating in.	0x0	R
[1:0]	CRC_ENABLEB	Inverted CRC Enable. This must be written with the inverted value of the CRC_ENABLE. d 10: CRC Enabled 11: CRC Disable	0x3	R/W

INTERFACE STATUS A REGISTER

Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS_A

Status bits are set to 1 to indicate an active condition and may be cleared by writing a 1 to the corresponding bit location

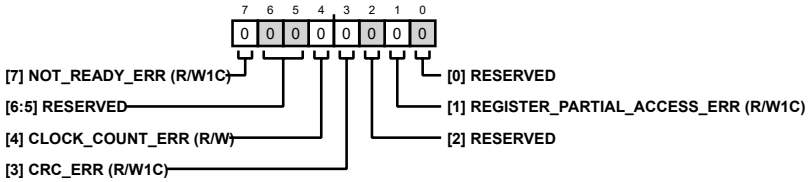


Table 25. Bit Descriptions for INTERFACE_STATUS_A

Bits	Bit Name	Description	Reset	Access
7	NOT_READY_ERR	Device Not Ready for Transaction. This error bit is set if the user attempts to execute a SPI transaction before the completion of digital initialization.	0x0	R/W1C
[6:5]	RESERVED	Reserved.	0x0	R
4	CLOCK_COUNT_ERR	Incorrect Number of Clocks Detected in a Transaction.	0x0	R/W
3	CRC_ERR	Invalid/No CRC Received. This is set when the controller fails to send a CRC or when the device calculates and checks the CRC and finds the CRC value is incorrect.	0x0	R/W1C
2	RESERVED	Reserved.	0x0	R
1	REGISTER_PARTIAL_ACCESS_ERR	Set When Fewer Than Expected Number of Bytes Read/Written. This bit is only valid when strict register access is enabled.	0x0	R/W1C
0	RESERVED	Reserved.	0x0	R

OUTPUT OPERATING MODE 0 REGISTER

Address: 0x20, Reset: 0xFF, Name: OUTPUT_OPERATING_MODE_0

Configures the operating modes for Channel 0 to Channel 3

REGISTER DETAILS

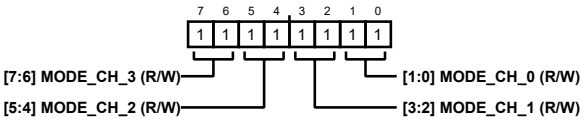


Table 26. Bit Descriptions for OUTPUT_OPERATING_MODE_0

Bits	Bit Name	Description	Reset	Access
[7:6]	MODE_CH_3	Mode Channel 3. Output operating mode for Channel 3. 00: Normal operation. 01: Powered down: 500Ω output impedance. 10: Powered down: 3.85kΩ output impedance. 11: Powered down: 16kΩ output impedance.	0x3	R/W
[5:4]	MODE_CH_2	Mode Channel 2. Output operating mode for Channel 2. 00: Normal operation. 01: Powered down: 500Ω output impedance. 10: Powered down: 3.85kΩ output impedance. 11: Powered down: 16kΩ output impedance.	0x3	R/W
[3:2]	MODE_CH_1	Mode Channel 1. Output operating mode for Channel 1. 00: Normal operation. 01: Powered down: 500Ω output impedance. 10: Powered down: 3.85kΩ output impedance. 11: Powered down: 16kΩ output impedance.	0x3	R/W
[1:0]	MODE_CH_0	Mode Channel 0. Output operating mode for Channel 0. 00: Normal operation. 01: Powered down: 500Ω output impedance. 10: Powered down: 3.85kΩ output impedance. 11: Powered down: 16kΩ output impedance.	0x3	R/W

OUTPUT CONTROL 0 REGISTER

Address: 0x2A, Reset: 0x00, Name: OUTPUT_CONTROL_0

Configures output range for all channels

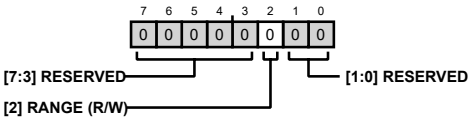


Table 27. Bit Descriptions for OUTPUT_CONTROL_0

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	RANGE	Output Range. Bitfield used to configure output range for all channels. 0: Range 0. Output will range from 0V to VREF 1: Range 1. Output will range from 0V to 2×VREF	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

REFERENCE CONTROL 0 REGISTER

Address: 0x3C, Reset: 0x00, Name: REFERENCE_CONTROL_0

Configures reference source for all channels

REGISTER DETAILS

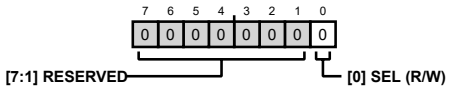


Table 28. Bit Descriptions for REFERENCE_CONTROL_0

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	SEL	Reference Select. Selects the voltage reference source for all channels. 0: Select 0. VREF pin is an input pin, an external reference should be provided through this pin. 1: Select 1. VREF pin is an output pin, internal reference is used by the part and is also available on VREF pin.	0x0	R/W

MULTIPLEXER INPUT SELECT 0 REGISTER

Address: 0x93, Reset: 0x00, Name: MUX_OUT_SELECT_0

Selects which of the multiplexer's input signals will be monitored on the MUX_OUT pin

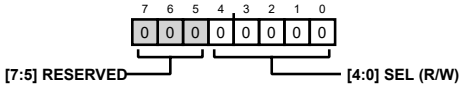


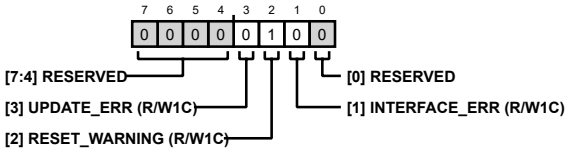
Table 29. Bit Descriptions for MUX_OUT_SELECT_0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SEL	Multiplexer Input Select. Selects which of the multiplexer's input signals will be monitored on the MUX_OUT pin. 0x0: Powered down. MUX_OUT pin is powered down. An 80 kΩ impedance can be seen at the MUX_OUT pin. 0x1: VOUT0. A voltage representation of VOUT0 can monitored on MUX_OUT pin. 0x2: IOUT0 (source mode). A voltage representation of IOUT0 (source mode) can monitored on MUX_OUT pin. 0x3: IOUT0 (sink mode). A voltage representation of IOUT0 (sink mode) can monitored on MUX_OUT pin. 0x7: VOUT1. A voltage representation of VOUT1 can monitored on MUX_OUT pin. 0x8: IOUT1 (source mode). A voltage representation of IOUT1 (source mode) can monitored on MUX_OUT pin. 0x9: IOUT1 (sink mode). A voltage representation of IOUT1 (sink mode) can monitored on MUX_OUT pin. 0xD: VOUT2. A voltage representation of VOUT2 can monitored on MUX_OUT pin. 0xE: IOUT2 (source mode). A voltage representation of IOUT2 (source mode) can monitored on MUX_OUT pin. 0xF: IOUT2 (sink mode). A voltage representation of IOUT2 (sink mode) can monitored on MUX_OUT pin. 0x13: VOUT3. A voltage representation of VOUT3 can monitored on MUX_OUT pin. 0x14: IOUT3 (source mode). A voltage representation of IOUT3 (source mode) can monitored on MUX_OUT pin. 0x15: IOUT3 (sink mode). A voltage representation of IOUT3 (sink mode) can monitored on MUX_OUT pin. 0x19: Die temperature. A voltage representation of internal die temperature can monitored on MUX_OUT pin. 0x1A: AGND. MUX_OUT pin internally tied to AGND.	0x0	R/W

STATUS CONTROL REGISTER

Address: 0xC2, Reset: 0x04, Name: STATUS_CONTROL

Event flags due to start up sequence, interface, reset, and update can be read. Write 1 to clear.



REGISTER DETAILS

Table 30. Bit Descriptions for STATUS_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	UPDATE_ERR	Update Error. Status to indicate that there was an attempt to update a DAC_Chn within 640ns since the last update. 0: Error 0. All updates successful. 1: Error 1. Overlapping updates attempted.	0x0	R/W1C
2	RESET_WARNING	Reset Warning. Status to indicate if the device went through a reset event. 0: Warning 0. Reset warning flag cleared. 1: Warning 1. Reset event occurred.	0x1	R/W1C
1	INTERFACE_ERR	Interface Error. Status to indicate an error flag is asserted in INTERFACE_STATUS_A. 0: Error 0. No interface error. 1: Error 1. Interface error.	0x0	R/W1C
0	RESERVED	Reserved.	0x0	R

HARDWARE LDAC ENABLE 0 REGISTER

Address: 0xD0, Reset: 0x0F, Name: HW_LDAC_EN_0

Enable hardware LDAC functionality for channel 0 to channel 3

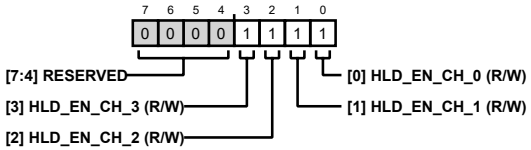


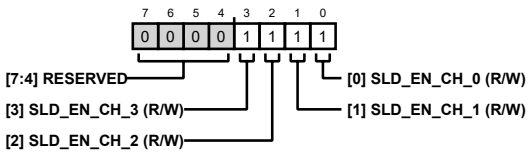
Table 31. Bit Descriptions for HW_LDAC_EN_0

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	HLD_EN_CH_3	Hardware LDAC Enable Channel 3. Enable/disable hardware LDAC functionality on Channel 3. 0: HLD En 0. Disable hardware LDAC on Channel 3. 1: HLD En 1. Enable hardware LDAC on Channel 3.	0x1	R/W
2	HLD_EN_CH_2	Hardware LDAC Enable Channel 2. Enable/disable hardware LDAC functionality on Channel 2. 0: HLD En 0. Disable hardware LDAC on Channel 2. 1: HLD En 1. Enable hardware LDAC on Channel 2.	0x1	R/W
1	HLD_EN_CH_1	Hardware LDAC Enable Channel 1. Enable/disable hardware LDAC functionality on Channel 1. 0: HLD En 0. Disable hardware LDAC on Channel 1. 1: HLD En 1. Enable hardware LDAC on Channel 1.	0x1	R/W
0	HLD_EN_CH_0	Hardware LDAC Enable Channel 0. Enable/disable hardware LDAC functionality on Channel 0. 0: HLD En 0. Disable hardware LDAC on Channel 0. 1: HLD En 1. Enable hardware LDAC on Channel 0.	0x1	R/W

SOFTWARE LDAC ENABLE 0 REGISTER

Address: 0xD1, Reset: 0x0F, Name: SW_LDAC_EN_0

Enable software LDAC functionality for Channel 0 to Channel 3



REGISTER DETAILS

Table 32. Bit Descriptions for SW_LDAC_EN_0

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	SLD_EN_CH_3	Software LDAC Enable Channel 3. Enable/disable software LDAC functionality on Channel 3. 0: SLD En 0. Disable software LDAC on Channel 3. 1: SLD En 1. Enable software LDAC on Channel 3.	0x1	R/W
2	SLD_EN_CH_2	Software LDAC Enable Channel 2. Enable/disable software LDAC functionality on Channel 2. 0: SLD En 0. Disable software LDAC on Channel 2. 1: SLD En 1. Enable software LDAC on Channel 2.	0x1	R/W
1	SLD_EN_CH_1	Software LDAC Enable Channel 1. Enable/disable software LDAC functionality on Channel 1. 0: SLD En 0. Disable software LDAC on Channel 1. 1: SLD En 1. Enable software LDAC on Channel 1.	0x1	R/W
0	SLD_EN_CH_0	Software LDAC Enable Channel 0. Enable/disable software LDAC functionality on channel 0 0: SLD En 0. Disable software LDAC on Channel 0. 1: SLD En 1. Enable software LDAC on Channel 0.	0x1	R/W

DAC REGISTER

Address: 0xD3 to 0xD9 (Increments of 2), Reset: 0x0000, Name: DAC_Chn

16-bit data defines the voltage of VOUTn pin, where n is the channel number

DAC_Ch0: 0xD2-0xD3
DAC_Ch1: 0xD4-0xD5
DAC_Ch2: 0xD6-0xD7
DAC_Ch3: 0xD8-0xD9

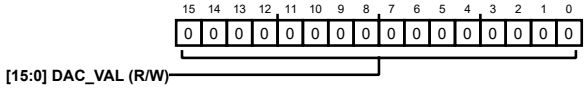


Table 33. Bit Descriptions for DAC_Chn

Bits	Bit Name	Description	Reset	Access
[15:0]	DAC_VAL	DAC Value. 16-bit data defines the voltage of VOUTn pin, where n is the channel number	0x0	R/W

MULTIPLE DAC REGISTER

Address: 0xDB, Reset: 0x0000, Name: MULTI_DAC_CH

Data written to this register also writes all DAC_CHn selected in MULTI_DAC_SEL_0

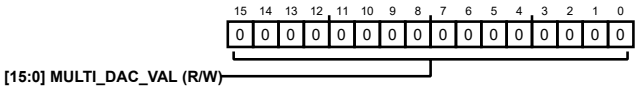


Table 34. Bit Descriptions for MULTI_DAC_CH

Bits	Bit Name	Description	Reset	Access
[15:0]	MULTI_DAC_VAL	Multiple DAC Value. Data written to all DAC_Chn selected in Multi_DAC_SEL_0. Read data will always return the latest data written.	0x0	R/W

MULTIPLE DAC SELECT 0 REGISTER

Address: 0xDC, Reset: 0x0F, Name: MULTI_DAC_SEL_0

Select which DAC_Chn will be written when a write operation is executed on Multi_DAC_Ch; only applies DAC_Ch0 to DAC_Ch3

REGISTER DETAILS

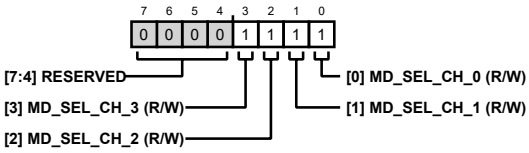


Table 35. Bit Descriptions for MULTI_DAC_SEL_0

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	MD_SEL_CH_3	Multiple DAC Select Channel 3. If selected, write operation on Multi_DAC_Ch also writes DAC_Ch3 with the same data. If deselected, write operation on Multi_DAC_Ch will have no effect on DAC_Ch3. 0: MD Sel 0. Deselect DAC_Ch3 for Multi_DAC_Ch operation. 1: MD Sel 1. Select DAC_Ch3 for Multi_DAC_Ch operation.	0x1	R/W
2	MD_SEL_CH_2	Multiple DAC Select Channel 2. If selected, write operation on Multi_DAC_Ch also writes DAC_Ch2 with the same data. If deselected, write operation on Multi_DAC_Ch will have no effect on DAC_Ch2. 0: MD Sel 0. Deselect DAC_Ch2 for Multi_DAC_Ch operation. 1: MD Sel 1. Select DAC_Ch2 for Multi_DAC_Ch operation.	0x1	R/W
1	MD_SEL_CH_1	Multiple DAC Select Channel 1. If selected, write operation on Multi_DAC_Ch also writes DAC_Ch1 with the same data. If deselected, write operation on Multi_DAC_Ch will have no effect on DAC_Ch1. 0: MD Sel 0. Deselect DAC_Ch1 for Multi_DAC_Ch operation. 1: MD Sel 1. Select DAC_Ch1 for Multi_DAC_Ch operation.	0x1	R/W
0	MD_SEL_CH_0	Multiple DAC Select Channel 0. If selected, write operation on Multi_DAC_Ch also writes DAC_Ch0 with the same data. If deselected, write operation on Multi_DAC_Ch will have no effect on DAC_Ch0. 0: MD Sel 0. Deselect DAC_Ch0 for Multi_DAC_Ch operation. 1: MD Sel 1. Select DAC_Ch0 for Multi_DAC_Ch operation.	0x1	R/W

SOFTWARE LDAC TRIGGER 0 REGISTER

Address: 0xDD, Reset: 0x00, Name: SW_LDAC_TRIG_0

Initiates transfer of Input_Chn to DAC_Chn; Only takes effect on enabled channels identified by SW_LDAC_En_0

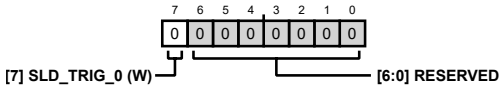


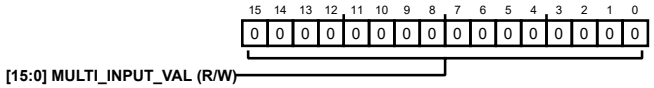
Table 36. Bit Descriptions for SW_LDAC_TRIG_0

Bits	Bit Name	Description	Reset	Access
7	SLD_TRIG_0	Software LDAC Trigger 0. When set, initiates transfer of Input_Chn to DAC_Chn, where n is the channel number as enabled by SW_LDAC_En_0. Writing 0 will have no effect.	0x0	W
[6:0]	RESERVED	Reserved.	0x0	R

MULTIPLE INPUT REGISTER

Address: 0xDF, Reset: 0x0000, Name: MULTI_INPUT_CH

Data written to this register also writes all Input_Chn selected in Multi_Input_Sel_0; read data will always return the latest data written



REGISTER DETAILS

Table 37. Bit Descriptions for MULTI_INPUT_CH

Bits	Bit Name	Description	Reset	Access
[15:0]	MULTI_INPUT_VAL	Multiple Input Value. Data to be written to all Input_Chn selected in Multi_Input_Sel_0. Read data will always return the latest data written.	0x0	R/W

MULTIPLE INPUT SELECT 0 REGISTER

Address: 0xE0, Reset: 0x0F, Name: MULTI_INPUT_SEL_0

Select which Input_Chn will be written when a write operation is executed on Multi_Input_Ch; only applies Input_Ch0 to Input_Ch3

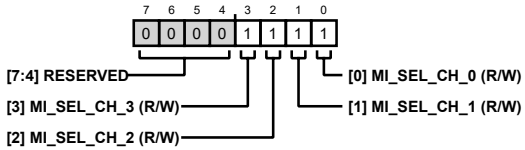


Table 38. Bit Descriptions for MULTI_INPUT_SEL_0

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	MI_SEL_CH_3	Multiple Input Select Channel 3. If selected, write operation on Multi_Input_Ch also writes Input_Ch3 with the same data. If deselected, write operation on Multi_DAC_Ch will have no effect on Input_Ch3. 0: MI Sel 0. Deselect Input_Ch3 for Multi_Input_Ch operation. 1: MI Sel 1. Select Input_Ch3 for Multi_Input_Ch operation.	0x1	R/W
2	MI_SEL_CH_2	Multiple Input Select Channel 2. If selected, write operation on Multi_Input_Ch also writes Input_Ch2 with the same data. If deselected, write operation on Multi_DAC_Ch will have no effect on Input_Ch2. 0: MI Sel 0. Deselect Input_Ch2 for Multi_Input_Ch operation. 1: MI Sel 1. Select Input_Ch2 for Multi_Input_Ch operation.	0x1	R/W
1	MI_SEL_CH_1	Multiple Input Select Channel 1. If selected, write operation on Multi_Input_Ch also writes Input_Ch1 with the same data. If deselected, write operation on Multi_DAC_Ch will have no effect on Input_Ch1. 0: MI Sel 0. Deselect Input_Ch1 for Multi_Input_Ch operation. 1: MI Sel 1. Select Input_Ch1 for Multi_Input_Ch operation.	0x1	R/W
0	MI_SEL_CH_0	Multiple Input Select Channel 0. If selected, write operation on Multi_Input_Ch also writes Input_Ch0 with the same data. If deselected, write operation on Multi_DAC_Ch will have no effect on Input_Ch0. 0: MI Sel 0. Deselect Input_Ch0 for Multi_Input_Ch operation. 1: MI Sel 1. Select Input_Ch0 for Multi_Input_Ch operation.	0x1	R/W

SOFTWARE LDAC TRIGGER 0 REGISTER

Address: 0xE1, Reset: 0x00, Name: SW_LDAC_TRIG_0

Initiates transfer of Input_Chn to DAC_Chn; only takes effect on enabled channels identified by SW_LDAC_En_0

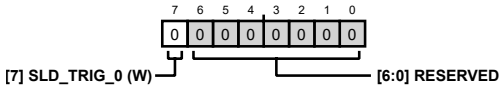


Table 39. Bit Descriptions for SW_LDAC_TRIG_0

Bits	Bit Name	Description	Reset	Access
7	SLD_TRIG_0	Software LDAC Trigger 0. When set, initiates transfer of Input_Chn to DAC_Chn, where n is the channel number as enabled by SW_LDAC_En_0. Writing 0 will have no effect.	0x0	W
[6:0]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

INPUT REGISTER

Address: 0xE3 to 0xE9 (Increments of 2), Reset: 0x0000, Name: INPUT_CHn

A write to this register does not update the output voltage of the device; hardware LDAC or software LDAC is required to push data from INPUT_CHn to DAC_Chn, which will also update the output

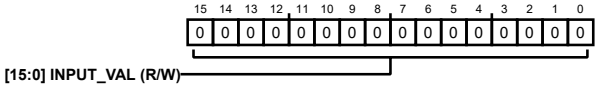


Table 40. Bit Descriptions for INPUT_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	INPUT_VAL	Input Value. 16-bit INPUT_CHn data where n is the channel number.	0x0	R/W

OUTLINE DIMENSIONS

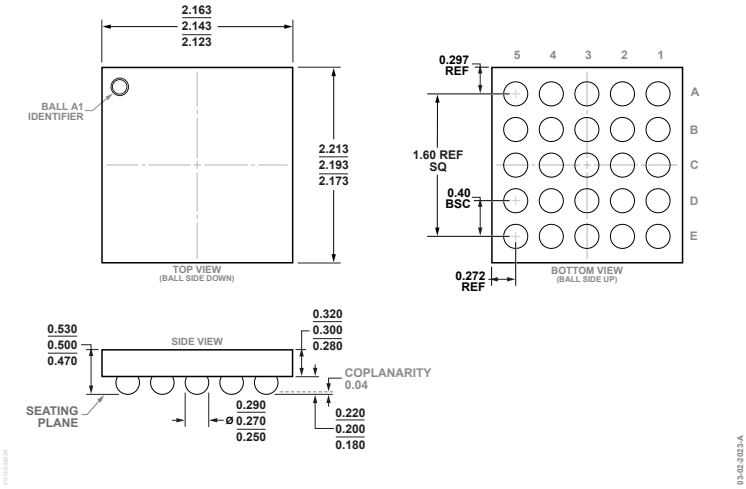


Figure 81. 25-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-25-11)
Dimensions shown in millimeters

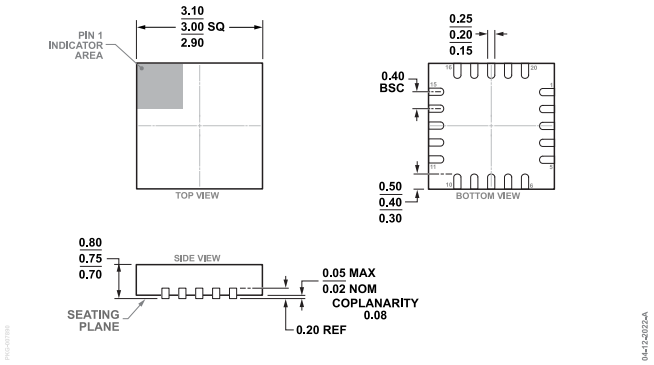


Figure 82. 20-Lead Lead Frame Chip Scale Package [LFCSP]
3 x 3 mm Body and 0.85 mm Package Height
(CP-20-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD3531RBCBZ-RL7	−40°C to +125°C	25-Ball WLCSP (2.143mm × 2.193mm × 0.500mm)	Reel, 1500	CB-25-11
AD3531BCBZ-RL7	−40°C to +125°C	25-Ball WLCSP (2.143mm × 2.193mm × 0.500mm)	Reel, 1500	CB-25-11
AD3531RBCPZ-RL7	−40°C to +125°	20-Lead LFCSP (3 mm × 3 mm × 0.75 mm)	Reel, 1500	CP-20-23
AD3531BCPZ-RL7	−40°C to +125°	20-Lead LFCSP (3 mm × 3 mm × 0.75 mm)	Reel, 1500	CP-20-23

[1] Z = RoHS Compliant Part.

OUTLINE DIMENSIONS

EVALUATION BOARD

Model[1]	Description
EVAL-AD3531RARDZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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