Data Sheet

MAX17636, MAX17638, MAX17639

3V to 36V, 6A/8A/10A, 12A Peak, High-Efficiency, Synchronous Step-Down DC-DC Converter

FEATURES

- Designed for Ultra-High Efficiency
  - 22mΩ/8mΩ $R_{DS\text{-}ON}$ Power MOSFETs
  - 94.9% Efficiency from $24V_{IN}$ to $5V_{OUT}$, 10A with 95.6% Peak Efficiency at 6A
  - External Bias Input for Improved Efficiency
  - 40µA I_Q Regulating $24V_{IN}$ to $3.3V_{OUT}$
- 10A Maximum Continuous, 12A Peak Transient Output for MAX17639
- Die Temperature Monitoring
- Designed for Low EMI
  - Symmetrical Input Voltage Pins
  - 400kHz to 2.2MHz Adjustable Switching Frequency with External Clock Synchronization
  - 4mm x 4mm 18L-FC2QFN
- Reduces External Components and Total Cost
  - No Schottky–Synchronous Operation
  - Adjustable Output Range from 0.6V to 90% of V_{IN}
  - Programmable Soft-Start and EN/UVLO Threshold
- Operates Reliably in Adverse Industrial Environments
  - Built-in Hiccup-Mode Overload Protection
  - Built-in Output-Voltage Status Monitoring and Die Temperature Monitoring with $\overline{\text{RESET}}$/TJ Pin
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature Range

SIMPLIFIED APPLICATION DIAGRAM

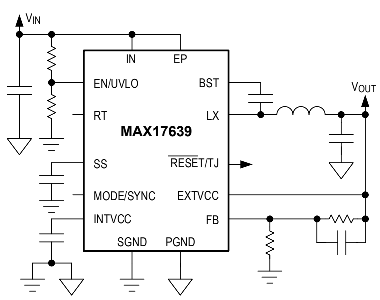

Figure 1. Typical Application Circuit

GENERAL DESCRIPTION

The MAX1763x are the high-efficiency, high-voltage, synchronous step-down DC-DC converters with integrated MOSFETs operating over an input voltage range of 3V to 36V. The MAX17636, MAX17638, MAX17639 can deliver up to 6A, 8A, and 10A continuous currents, respectively. Additionally, MAX17639 can support up to 12A peak current. These devices can generate output voltages ranging from 0.6V up to 90% of V_{IN}.

These devices feature a MODE/SYNC pin that can be used to program the device in forced pulse-width modulation (PWM) or switching frequency modulation (SFM) modes of operation and to synchronize the internal clock to an external clock. These devices offer an enable/input undervoltage lockout (EN/UVLO) pin to program the desired input voltage at which the converter turns on/off. These devices also have a soft-start (SS) pin to reduce inrush currents during startup. In addition, these devices feature a $\overline{\text{RESET}}$/TJ, pin which can be used either to monitor the status of output voltage or die temperature. The die temperature monitor allows the user to directly measure the silicon die temperature instead of relying on theoretical estimation, thus enabling robust, reliable power supply design.

APPLICATIONS

- Factory and Building Automation
- Distributed DC Power Systems
- General Purpose Power Supply

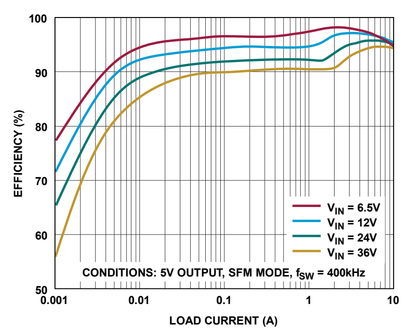

Figure 2. Efficiency vs. Load Current

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Initial Release	—
1	10/25	Updated Ordering Guide	34

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7µF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$/TJ = RT = Open, V_{BST} to V_{LX} = 1.8V, T_J = -40°C to +150°C. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. [1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input Voltage Range	V_{IN}		3		36	V
Input Shutdown Current	$I_{IN\text{-}SH}$	$V_{EN/UVLO}$ = 0V, T_A = T_J = +25°C		3.95	5.35	µA
		$V_{EN/UVLO}$ = 0V		3.95	40	µA
No Load IN Pin Current (See *Figure 54*)	I_{IN_SFM}	MODE/SYNC = Open, V_{IN} = 24V, V_{EXTVCC} = 5V		65		µA
	I_{IN_PWM}	$V_{MODE/SYNC}$ = 0V, V_{IN} = 24V, V_{EXTVCC} = 5V		23		mA
Input UVLO	$V_{IN\_UVLO\_R}$	V_{IN} rising	2.7	2.8	2.9	V
	$V_{IN\_UVLO\_F}$	V_{IN} falling	2.58	2.68	2.78	V
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.22	1.25	1.28	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.12	1.15	1.18	V
EN/UVLO Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 0V, T_A = +25°C	-50	0	+50	nA
LINEAR REGULATORS (INTVCC, EXTVCC)						
INTVCC Output Voltage	V_{INTVCC}	3 ≤ V_{IN} ≤ 36V, I_{INTVCC} = 1mA	1.74	1.8	1.86	V
		1mA ≤ I_{INTVCC} ≤ 30mA	1.72	1.8	1.87	V
		2.35 ≤ V_{EXTVCC} ≤ 12V, I_{INTVCC} = 1mA	1.74	1.8	1.86	V
		V_{EXTVCC} = 12V, 1mA ≤ I_{INTVCC} ≤ 30mA	1.72	1.8	1.87	V
INTVCC Undervoltage Threshold	V_{INTVCC_UVR}	V_{INTVCC} rising	1.61	1.64	1.69	V
	V_{INTVCC_UVF}	V_{INTVCC} falling	1.545	1.58	1.625	V
EXTVCC Voltage Range	V_{EXTVCC}		2.35		12	V
EXTVCC Switchover Threshold	V_{EXTVCC_UVR}	V_{EXTVCC} rising	2.25	2.30	2.35	V
EXTVCC Switchover Threshold	V_{EXTVCC_UVF}	V_{EXTVCC} falling	2.15	2.2	2.25	V
HIGH-SIDE AND LOW-SIDE MOSFETS						

(V_{IN} = 24V, $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7μF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$/TJ = RT = Open, V_{BST} to V_{LX} = 1.8V, T_J = -40°C to +150°C. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. [1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Side nMOS On-Resistance	$R_{DS\text{-}ONH}$	I_{LX} = 0.3A, sourcing		22.5	42	mΩ
Low-Side nMOS On-Resistance	$R_{DS\text{-}ONL}$	I_{LX} = 0.3A, sinking		8.5	16	mΩ
LX Leakage Current	I_{LX_LKG}	V_{IN} = 36V, V_{LX} = (V_{PGND}+1)V to (V_{IN} - 1)V, T_A = +25°C, $V_{EN/UVLO}$ = 0V	-2		+2	μA
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0.3V	4.4	5	5.3	μA
FEEDBACK (FB)						
FB Regulation Voltage	$V_{FB\text{-}REG}$		0.593	0.6	0.607	V
FB Input-Bias Current	I_{FB}	V_{FB} = 1V, T_A = +25°C	-50		+50	nA
MODE SELECTION AND EXTERNAL CLOCK SYNCHRONIZATION (MODE/SYNC)						
MODE Threshold	$V_{M\text{-}SFM}$	SFM Mode	1.3			V
	$V_{M\text{-}PWM}$	PWM Mode			0.5	V
SYNC Frequency Capture Range	f_{SYNC}	f_{SW} set by R_{RT} [2]	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC High Pulse Width	t_{SYNC_H}		100			ns
SYNC Low Pulse Width	t_{SYNC_L}		100			ns
SYNC Threshold	V_{IH}		1.3			V
	V_{IL}				0.5	V
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK\text{-}LIMIT}$	MAX17639	15.1	17.8	20.5	A
		MAX17638	11.3	13.3	15.3	A
		MAX17636	8.3	9.8	11.3	A
Valley Current-Limit Threshold	$I_{VALLEY\text{-}LIMIT}$	PWM Mode, MAX17639		-8		A
		PWM Mode, MAX17638		-7		A
		PWM Mode, MAX17636		-6		A
		SFM Mode	-0.10	0.13	+0.36	A
SWITCHING FREQUENCY (RT)						
Switching Frequency	f_{SW}	R_{RT} = 75kΩ	375	400	440	kHz

(V_{IN} = 24V, $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7µF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$/TJ = RT = Open, V_{BST} to V_{LX} = 1.8V, T_J = -40°C to +150°C. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. [1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		R_{RT} = 9.96kΩ	1980	2200	2420	kHz
		R_{RT} = Open	450	500	540	kHz
V_{FB} Hiccup Threshold	$V_{FB\text{-}HICF}$	V_{FB} falling	0.345	0.36	0.375	V
Hiccup Timeout		See Note[3]		130		ms
Minimum On-Time	$t_{ON\text{-}MIN}$			80	110	ns
Minimum Off-Time	$t_{OFF\text{-}MIN}$			120	150	ns
LX Dead Time	LX_{DT}			5		ns
OUTPUT VOLTAGE STATUS AND DIE TEMPERATURE MONITOR ($\overline{RESET}$ /TJ)						
$\overline{RESET}$ Output Level Low	$V_{\overline{RESET}L}$	$I_{\overline{RESET}}$ = 10mA			0.6	V
$\overline{RESET}$ Output Leakage Current	$I_{\overline{RESET}LKG}$	T_A = T_J = +25°C, $V_{\overline{RESET}}$ = 5.5V	-50		+50	nA
FB Threshold for $\overline{RESET}$ De-assertion	$V_{FB\text{-}OKR}$	V_{FB} Rising	93	95	97	%
FB Threshold for $\overline{RESET}$ Assertion	$V_{FB\text{-}OKF}$	V_{FB} Falling	90	91.7	93.7	%
$\overline{RESET}$ Delay after FB Reaches $V_{FB\text{-}OKR}$				2		ms
$\overline{RESET}$/TJ Pin Voltage	V_{T25}	T_A = +25°C, $\overline{RESET}$ /TJ = 20kΩ connected to SGND	580	595	610	mV
$\overline{RESET}$/TJ Pin Voltage Variation with respect to Die Temperature	dV_{TJ}/dT			2		mV/°C
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		175		°C
Thermal Shutdown Hysteresis				10		°C

1 Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.

2 The maximum allowable external clock frequency is 2.2MHz.

3 See the *Overcurrent Protection (OCP)/Hiccup Mode* section for more details.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
IN to PGND	-0.3V to +40V
EN/UVLO to SGND	-0.3V to (V_{IN} + 0.3V)
LX to PGND	-0.3V to (V_{IN} + 0.3V)
EXTVCC to SGND	-14V to +14V
BST to PGND	-0.3V to +42V
BST to LX	-0.3V to +2.2V
BST to INTVCC	-0.3V to +40V
FB, SS, RT, INTVCC to SGND	-0.3V to +2.2V
$\overline{\text{RESET}}$/TJ, MODE/SYNC to SGND	-0.3V to +6V
PGND to SGND	-0.3V to +0.3V
LX total RMS Current	15A
Output Short-Circuit Duration	Continuous
Continuous Power Dissipation (Multilayer Board), T_A = +70°C, derate 52.6mW/°C above +70°C	4210mW
Operating Temperature Range[1]	-40°C to +150°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature, Soldering, 10s	+300°C
Soldering Temperature (reflow)	+260°C

[1] Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

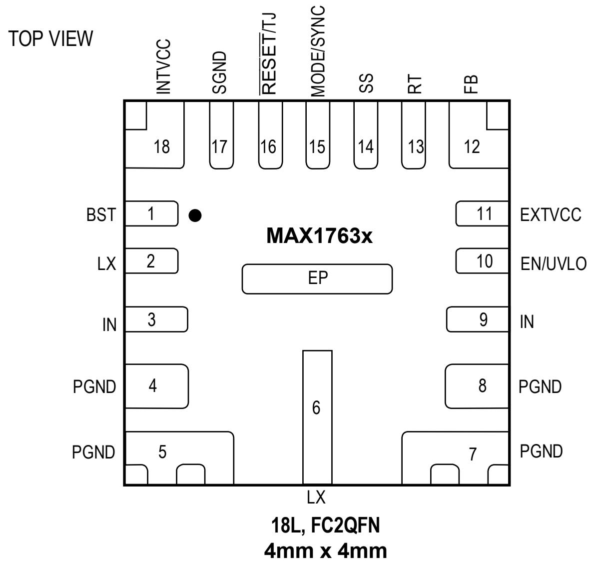


Figure 3. MAX1763x Pin Configuration

Pin Descriptions

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	BST	Bootstrap Capacitor Pin. Connect a 0.1µF ceramic capacitor between BST and LX (Pin 2).
2, 6	LX	Switching Node Pins. Connect LX (Pin 2) to the one end of the bootstrap capacitor. Connect LX (Pin 6) to the switching side of the inductor.
3, 9	IN	Power Supply Input Pins. The MAX1763x require two 0.1µF input bypass capacitors. One 0.1µF capacitor should be placed between IN (Pin 3) and PGND (Pin 4). A second 0.1µF capacitor should be placed between IN (Pin 9) and PGND (Pin 8). These capacitors must be placed as close as possible to the MAX1763x. The additional input capacitors (2 x 4.7µF or more) should be placed close to the MAX1763x across the input power traces. Connect the IN pins (3, 9) to EP using a plane. Refer to the MAX17639 evaluation board user guide for a layout example.
4, 5, 7, 8	PGND	Power Ground Pins. Connect PGND pins to the power ground plane. Refer to the MAX17639 evaluation kit data sheet for a layout example.
10	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the device. Connect to the center of the resistor-divider between IN and SGND to set the input voltage at which the part turns on. Pull low for disabling the device

PIN	NAME	DESCRIPTION
11	EXTVCC	External Bias Input for EXT-LDO. Connect the pin to the converter output voltage node for output voltages ranging from 2.5V to 12V for improved efficiency. Connect the pin to SGND when EXTVCC feature is not used. See the *Linear Regulator (INTVCC and EXTVCC)* section for more details.
12	FB	Feedback Input Pin. Connect the FB pin to the center node of a resistor divider connected between the output voltage node and the SGND pin to set the output voltage. See the *Adjusting Output Voltage* section for more details
13	RT	Switching Frequency Programming Input Pin. Connect a resistor from RT to SGND to set the converter switching frequency between 400kHz and 2.2MHz. Leave the RT pin open for the default 500kHz switching frequency. See the *Setting the Switching Frequency (RT)* section for more details.
14	SS	Soft-Start Input Pin. Connect a capacitor from SS to SGND to set the soft-start time.
15	MODE/SYNC	Mode Selection Input/External Clock Synchronization Input Pin. MODE/SYNC pin configures the device to operate in PWM or SFM modes of operation. Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. Leave the MODE/SYNC pin open for SFM operation at light loads. The MODE/SYNC pin can also be used to synchronize the converter to an external clock. See the *Mode Selection and External Clock Synchronization (MODE/SYNC)* section for more details.
16	$\overline{\text{RESET}}$/TJ	Open-Drain Status Output/Die Temperature Monitor Output Pin. This pin can be used to monitor either the status of the output voltage or the die temperature. The two functions cannot be used at the same time. Output voltage status can be monitored by connecting the $\overline{\text{RESET}}$/TJ pin to a power supply through a pull-up resistor. The $\overline{\text{RESET}}$/TJ output is driven low if FB node voltage drops below 91.7%(typ) of its set value. $\overline{\text{RESET}}$/TJ goes high 2ms after FB rises above 95%(typ) of its set value. The $\overline{\text{RESET}}$/TJ pin can also be used to monitor the die temperature of the device by connecting a 20kΩ resistor from the $\overline{\text{RESET}}$/TJ pin to SGND. See the *Output-Voltage Status and Die Temperature Monitor ($\overline{/}$TJ)* section for more details.
17	SGND	Signal Ground.
18	INTVCC	1.8V Linear Regulator Output Pin. Connect a minimum of 4.7µF ceramic capacitor between INTVCC and SGND. Linear regulator does not support the external loading on the INTVCC pin.
—	EP	Exposed Pad. Always connect EP to the IN pins (3, 9) using a plane. Refer to the MAX17639 evaluation kit data sheet for a layout example.

FUNCTIONAL DIAGRAM

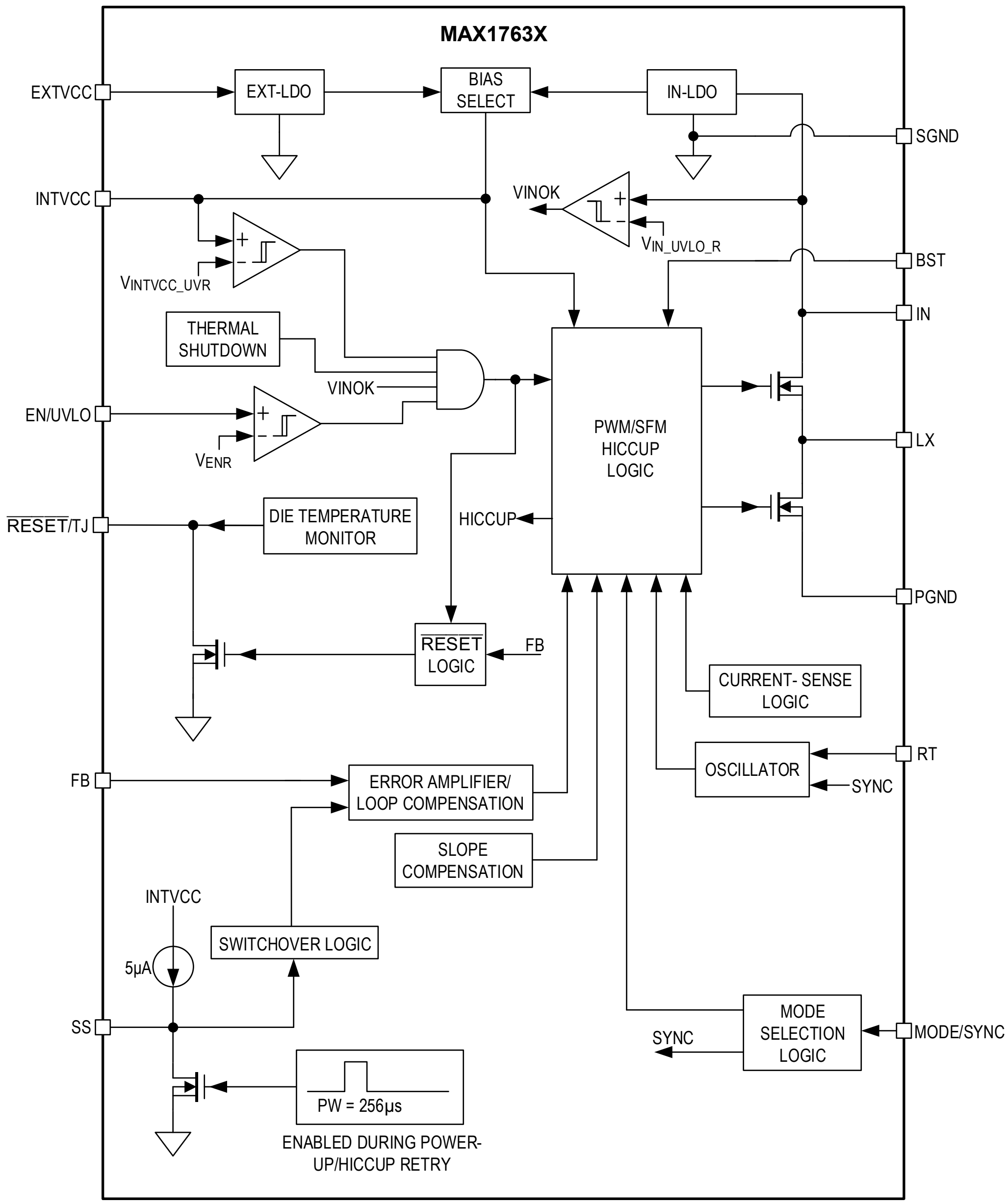


Figure 4. MAX1763x Functional Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8200pF, T_A = +25°C, unless otherwise noted.)

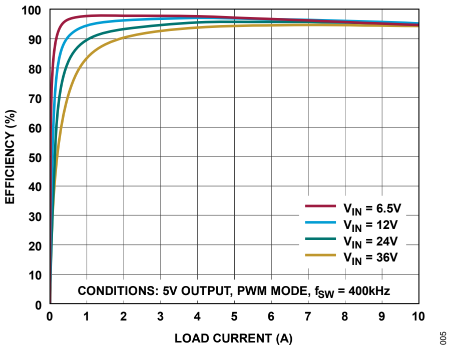


Figure 5. Efficiency vs. Load Current (Figure 54 Circuit)

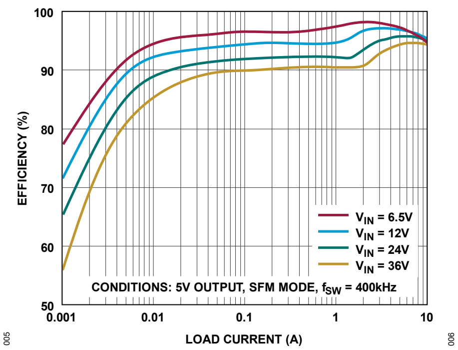


Figure 6. Efficiency vs. Load Current (Figure 54 Circuit)

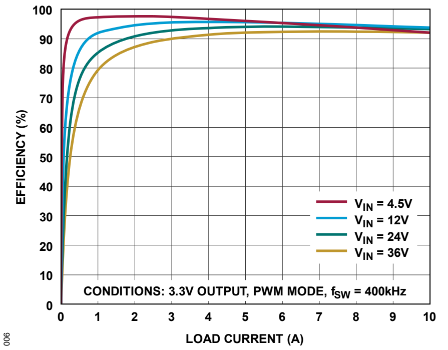


Figure 7. Efficiency vs. Load Current (Figure 55 Circuit)

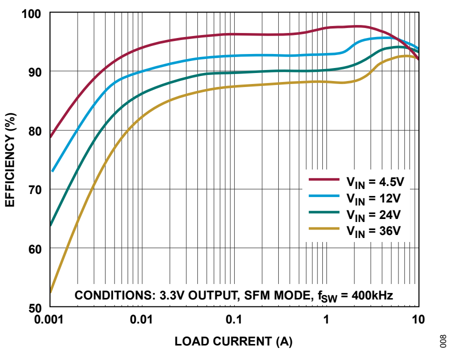


Figure 8. Efficiency vs. Load Current (Figure 55 Circuit)

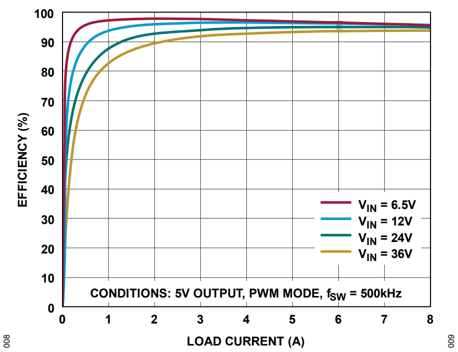


Figure 9. Efficiency vs. Load Current (Figure 56 Circuit)

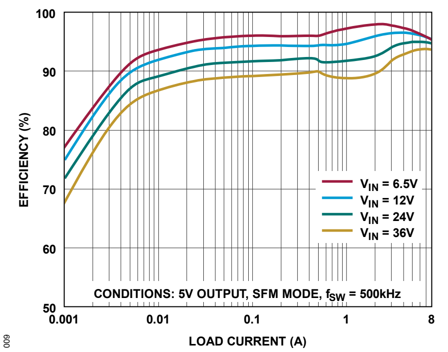


Figure 10. Efficiency vs. Load Current (Figure 56 Circuit)

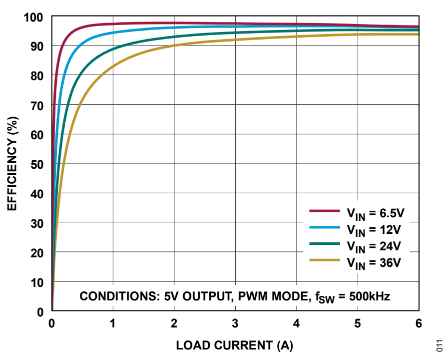


Figure 11. Efficiency vs. Load Current (Figure 57 Circuit)

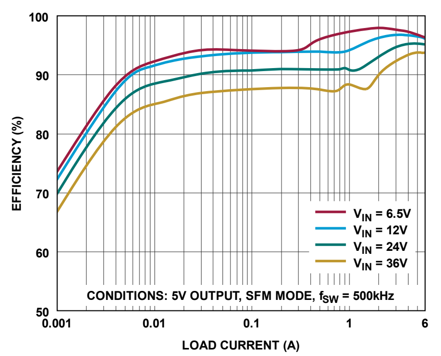


Figure 12. Efficiency vs. Load Current (Figure 57 Circuit)

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7μF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1μF, C_{SS} = 8200pF, T_A = +25°C, unless otherwise noted.)

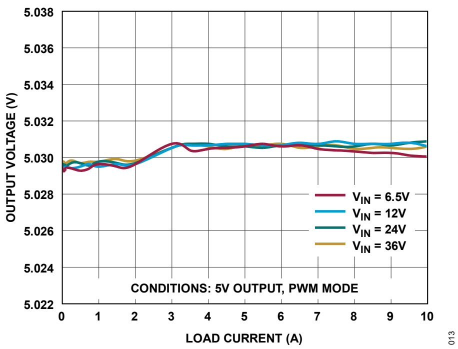


Figure 13. Output Voltage vs. Load Current (Figure 54 Circuit)

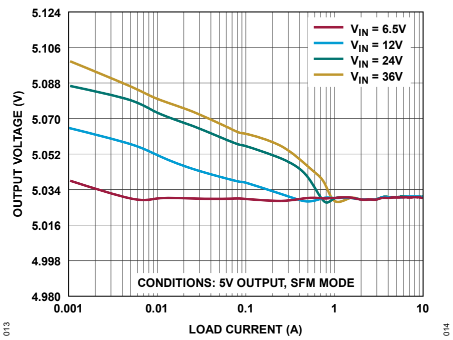


Figure 14. Output Voltage vs. Load Current (Figure 54 Circuit)

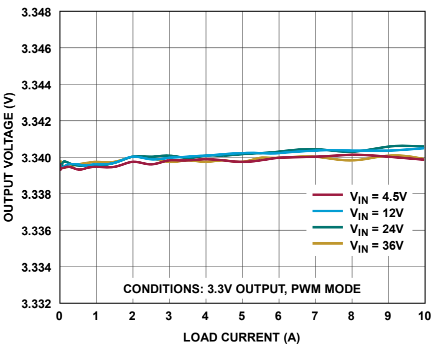


Figure 15. Output Voltage vs. Load Current (Figure 55 Circuit)

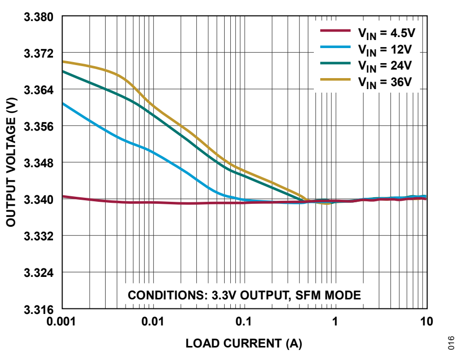


Figure 16. Output Voltage vs. Load Current (Figure 55 Circuit)

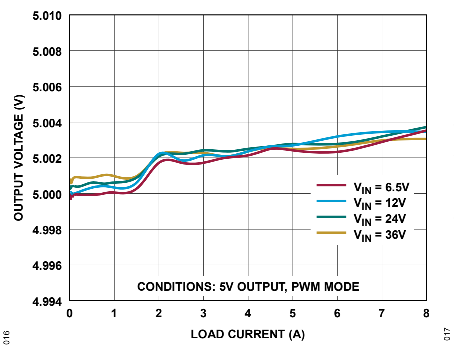


Figure 17. Output Voltage vs. Load Current (Figure 56 Circuit)

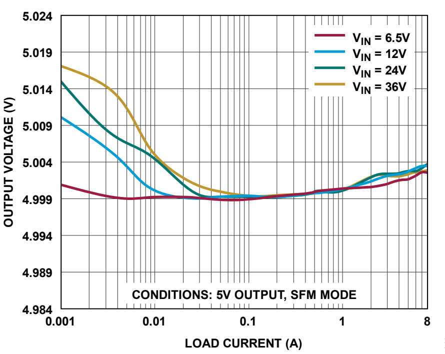


Figure 18. Output Voltage vs. Load Current (Figure 56 Circuit)

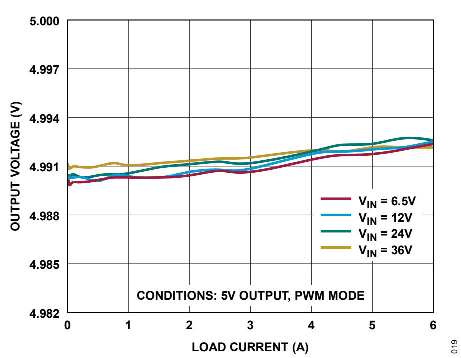


Figure 19. Output Voltage vs. Load Current (Figure 57 Circuit)

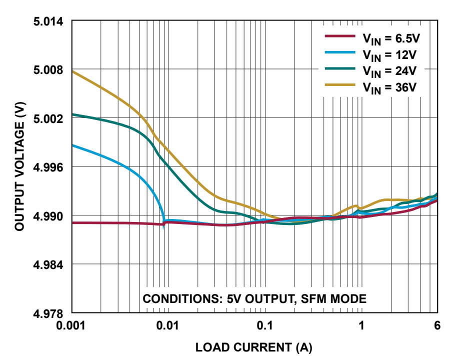


Figure 20. Output Voltage vs. Load Current (Figure 57 Circuit)

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8200pF, T_A = +25°C, unless otherwise noted.)

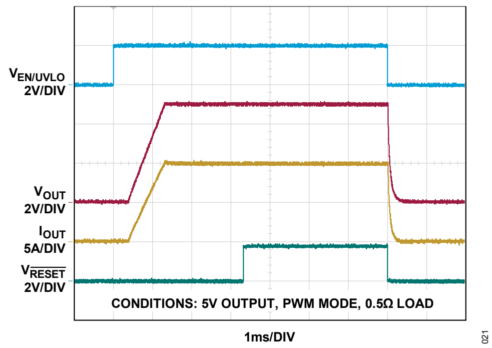


Figure 21. Soft-Start/Shutdown Through EN/UVLO (Figure 54 Circuit)

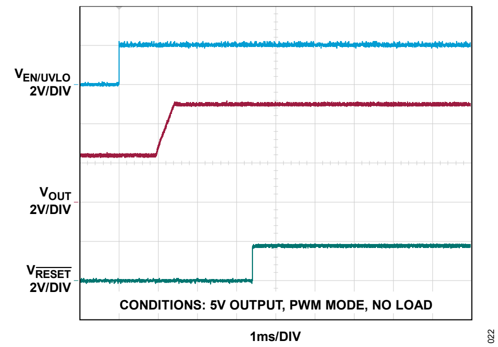


Figure 22. Soft-Start With Prebias Voltage of 2.5V (Figure 54 Circuit)

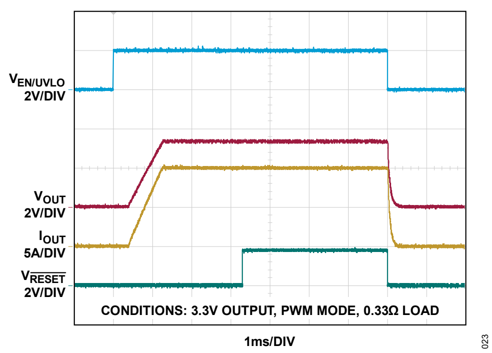


Figure 23. Soft-Start/Shutdown Through EN/UVLO (Figure 55 Circuit)

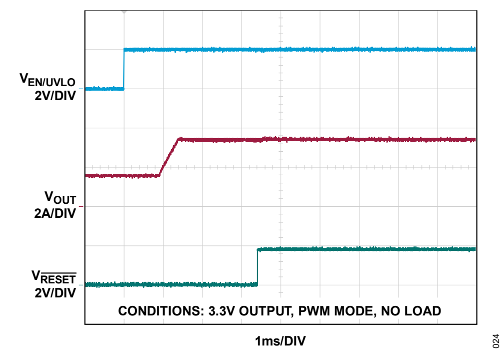


Figure 24. Soft-Start With Prebias Voltage of 1.65V (Figure 55 Circuit)

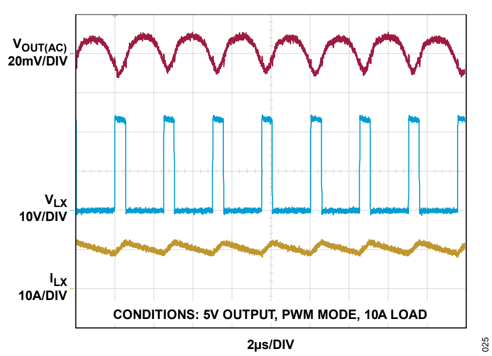


Figure 25. Steady-State Performance (Figure 54 Circuit)

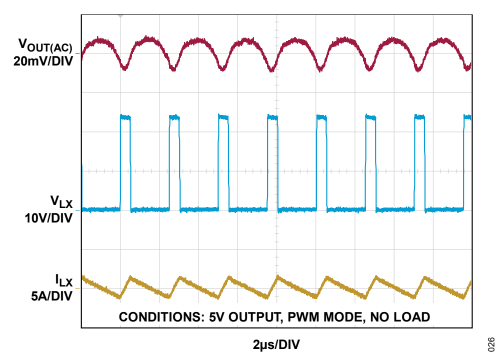


Figure 26. Steady-State Performance (Figure 54 Circuit)

($V_{IN} = V_{EN/UVLO} = 24V$, $C_{INTVCC} = 4.7\mu F$, $V_{SGND} = V_{PGND} = 0V$, $V_{EXTVCC} = V_{OUT}$, $C_{BST} = 0.1\mu F$, $C_{SS} = 8200pF$, $T_A = +25°C$, unless otherwise noted.)

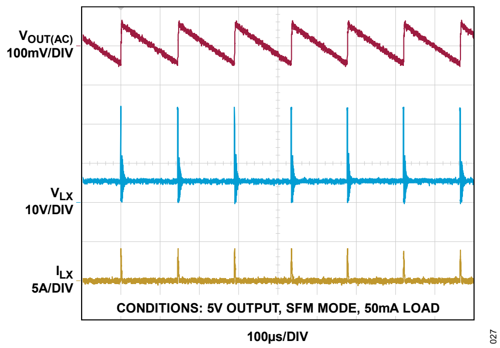


Figure 27. Steady-State Performance (Figure 54 Circuit)

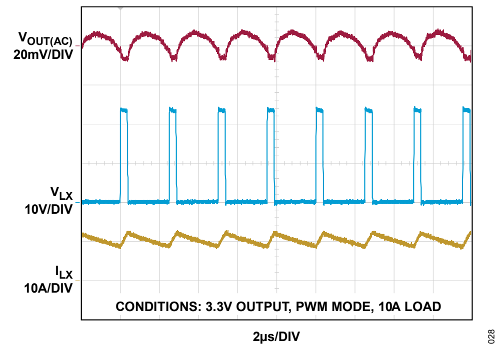


Figure 28. Steady-State Performance (Figure 55 Circuit)

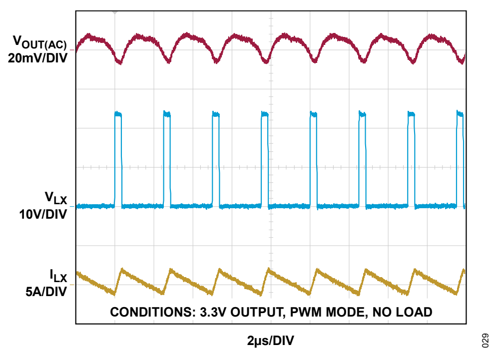


Figure 29. Steady-State Performance (Figure 55 Circuit)

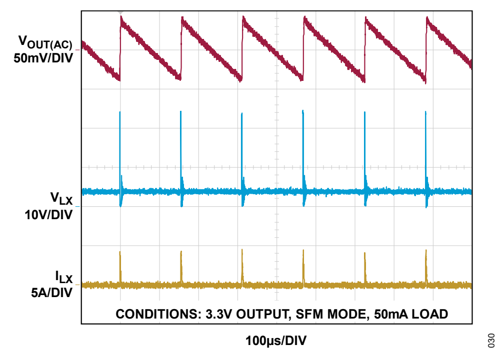


Figure 30. Steady-State Performance (Figure 55 Circuit)

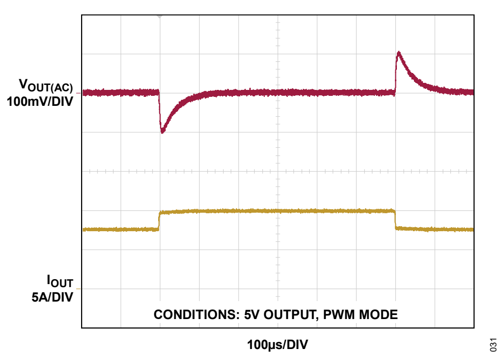


Figure 31. Load Transient Between 7.5A and 10A (Figure 54 Circuit)

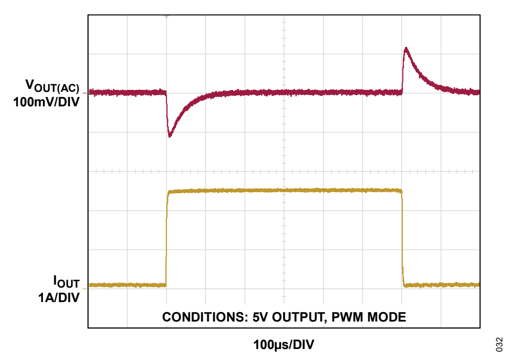


Figure 32. Load Transient Between 10mA and 2.5A (Figure 54 Circuit)

($V_{IN} = V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7µF, $V_{SGND} = V_{PGND}$ = 0V, $V_{EXTVCC} = V_{OUT}$, C_{BST} = 0.1µF, C_{SS} = 8200pF, T_A = +25°C, unless otherwise noted.)

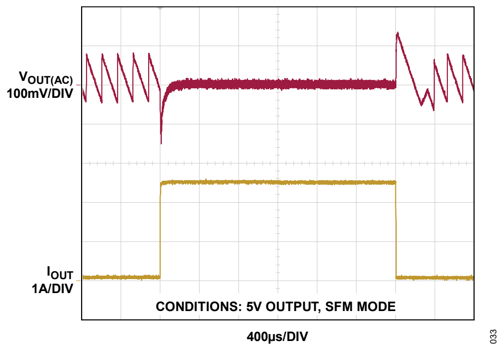


Figure 33. Load Transient Between 50mA and 2.5A (Figure 54 Circuit)

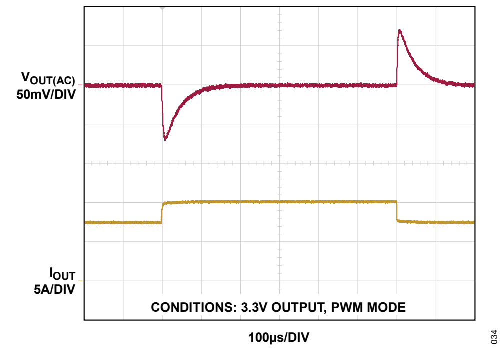


Figure 34. Load Transient Between 7.5A and 10A (Figure 55 Circuit)

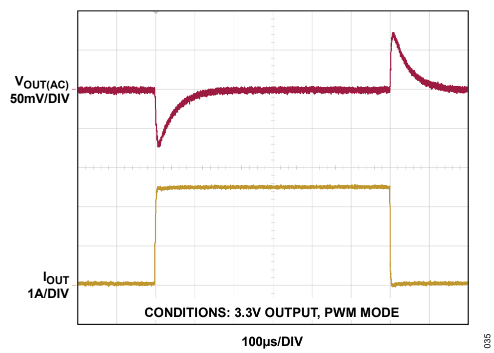


Figure 35. Load Transient Between 10mA and 2.5A (Figure 55 Circuit)

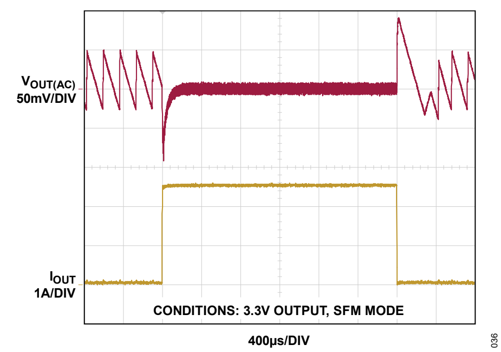


Figure 36. Load Transient Between 50mA and 2.5A (Figure 55 Circuit)

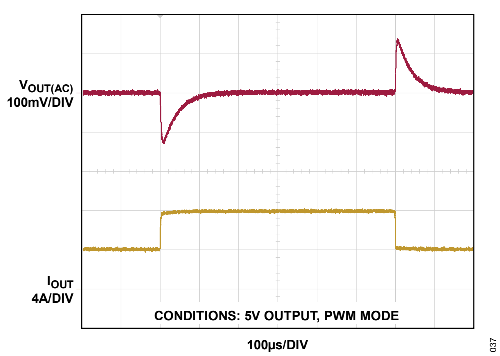


Figure 37. Load Transient Between 4A and 8A (Figure 56 Circuit)

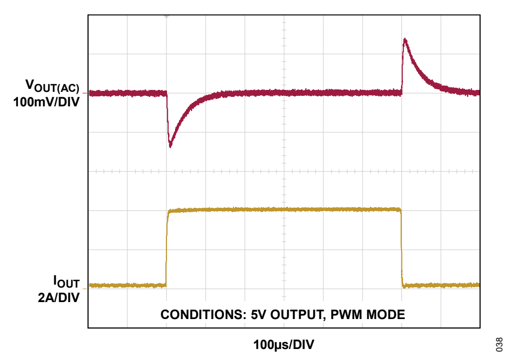


Figure 38. Load Transient Between 10mA and 4A (Figure 56 Circuit)

($V_{IN} = V_{EN/UVLO} = 24V$, $C_{INTVCC} = 4.7\mu F$, $V_{SGND} = V_{PGND} = 0V$, $V_{EXTVCC} = V_{OUT}$, $C_{BST} = 0.1\mu F$, $C_{SS} = 8200pF$, $T_A = +25°C$, unless otherwise noted.)

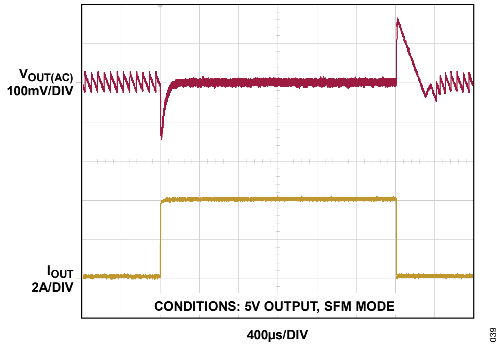


Figure 39. Load Transient Between 50mA and 4A (Figure 56 Circuit)

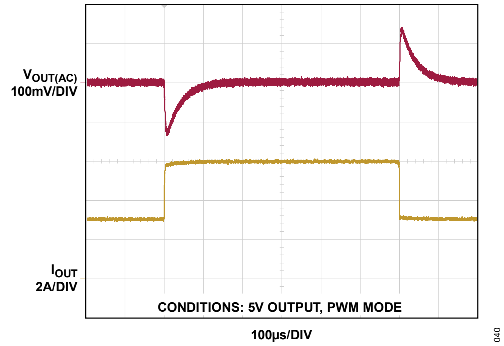


Figure 40. Load Transient Between 3A and 6A (Figure 57 Circuit)

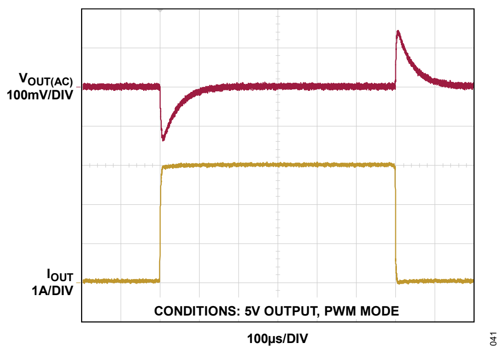


Figure 41. Load Transient Between 10mA and 3A (Figure 57 Circuit)

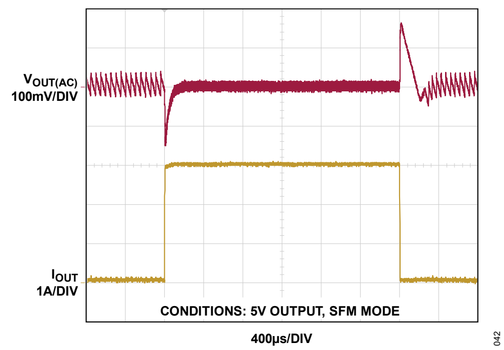


Figure 42. Load Transient Between 50mA and 3A (Figure 57 Circuit)

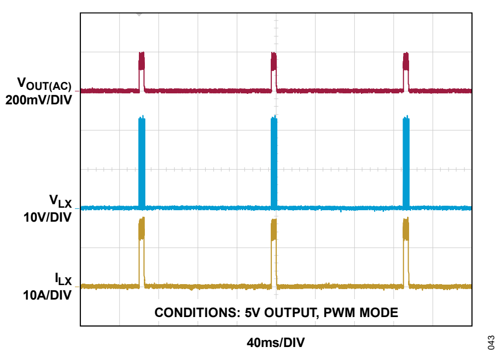


Figure 43. Overload Protection (Figure 54 Circuit)

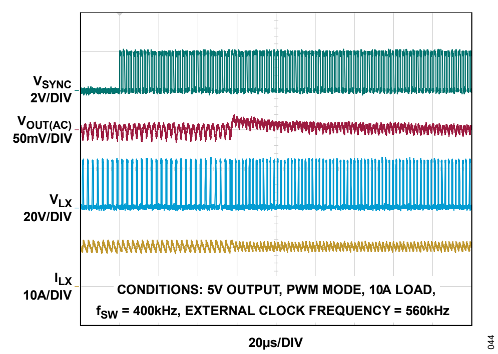


Figure 44. External Clock Synchronization (Figure 54 Circuit)

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8200pF, T_A = +25°C, unless otherwise noted.)

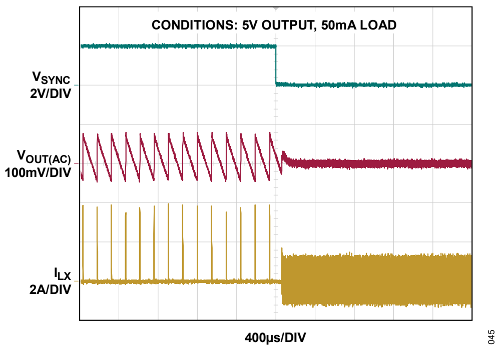


Figure 45. Dynamic Mode Change (Figure 54 Circuit)

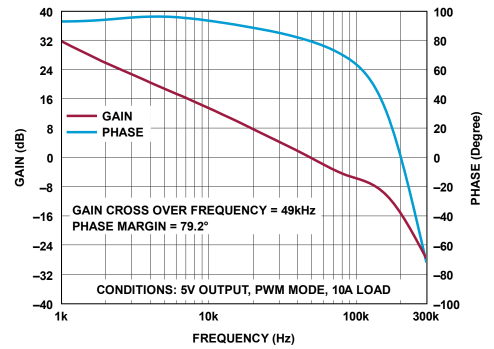


Figure 46. Gain/Phase vs. Frequency (Figure 54 Circuit)

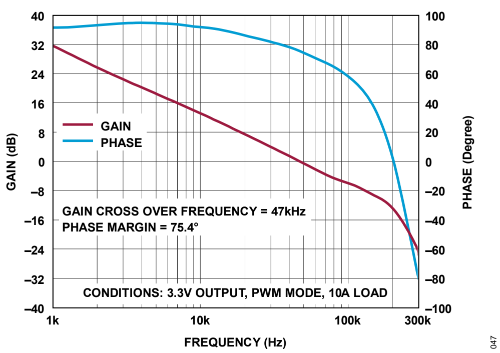


Figure 47. Gain/Phase vs. Frequency (Figure 55 Circuit)

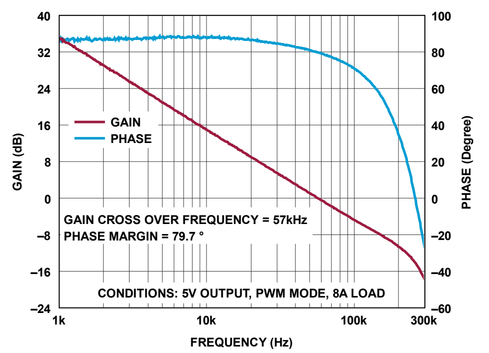


Figure 48. Gain/Phase vs. Frequency (Figure 56 Circuit)

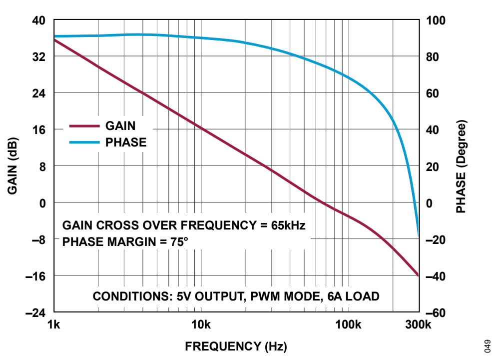


Figure 49. Gain/Phase vs. Frequency (Figure 57 Circuit)

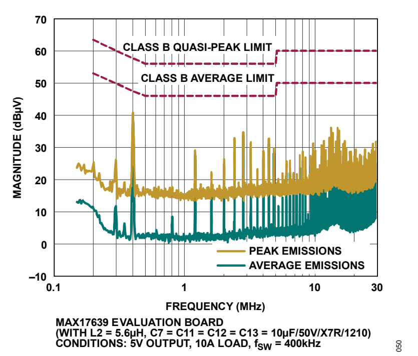


Figure 50. CISPR 32 Conducted Emission Test With Class B Limits

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{INTVCC} = 4.7µF, V_{SGND} = V_{PGND} = 0V, V_{EXTVCC} = V_{OUT} , C_{BST} = 0.1µF, C_{SS} = 8200pF, T_A = +25°C, unless otherwise noted.)

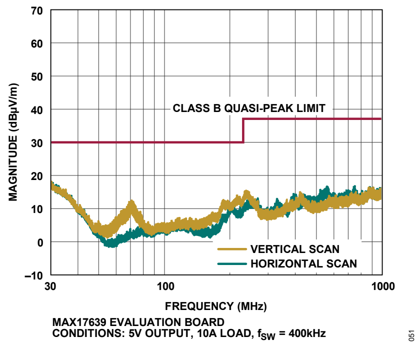


Figure 51. CISPR 32 Radiated Emission Test With Class B Limits

DETAILED DESCRIPTION

The MAX1763x are the high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operating over an input voltage range of 3V to 36V. The MAX17636, MAX17638, MAX17639 can deliver up to 6A, 8A, and 10A continuous current, respectively. Additionally, the MAX17639 can support up to 12A peak current. These devices can generate output voltages ranging from 0.6V up to 90% of V_{IN}. Built-in compensation across the output-voltage range eliminates the need for external compensation components. The feedback-voltage regulation accuracy is ±1.2% over -40°C to +150°C temperature range.

The MAX1763x feature a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node, which sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until the appropriate or maximum duty cycle is reached or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up and stores energy in the inductor, and also provides current to the output. During the rest of the switching cycle, the high-side MOSFET turns off, and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

These devices feature a MODE/SYNC pin that can be used to program the device in forced pulse-width modulation (PWM) or switching frequency modulation (SFM) modes of operation and to synchronize internal clock to an external clock. These devices offer an enable/input undervoltage lockout (EN/UVLO) pin to program the desired input voltage at which the converter turns on/off. These devices also have a soft-start (SS) pin to reduce inrush currents during startup. In addition, these devices feature a $\overline{\text{RESET}}$/TJ pin, which can be used either to monitor the status of output voltage or die temperature. The die temperature monitor allows the user to directly measure the silicon die temperature instead of relying on theoretical estimation, thus enabling robust, reliable power supply design. These devices offer low minimum on-time and low minimum off-time, allowing the converter to operate with a wider input voltage range for a given switching frequency.

Mode Selection and External Clock Synchronization (MODE/SYNC)

The MAX1763x support PWM and SFM modes of operation. The devices enter the programmed mode of operation based on the setting of the MODE/SYNC pin. If the MODE/SYNC pin is low (< $V_{M\text{-}PWM}$), the device operates in a constant-frequency PWM mode at all loads. If the MODE/SYNC pin is left open (> $V_{M\text{-}SFM}$), the device operates in SFM mode at light loads. The device also supports on-the-fly mode change between PWM and SFM modes. When there is a state transition on the MODE/SYNC pin, the device waits for a period of 40μs (typ) and transitions into the mode based on the MODE/SYNC pin voltage at the end of 40μs period.

The MODE/SYNC pin can be used to synchronize the internal oscillator of the device to an external clock in both modes of operation. The external clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the programmed switching frequency. When an external clock is applied to the MODE/SYNC pin, if eight or more external clock rising edges are detected in a period of 40μs (typ), the device operates in PWM mode only and the internal oscillator frequency changes to the external clock frequency at the end of the 40μs period. When the external clock is removed, the device continues to operate in PWM mode for a period of 40μs with the frequency set by RT and enters a mode based on the MODE/SYNC pin status. The external clock logic high and low pulse widths should be more than 100ns.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to the SFM mode of operation.

SFM Mode Operation

In SFM mode, the inductor current is discontinuous at light loads. SFM mode provides reduced frequency operation at light loads and allows the device to hibernate, enabling higher efficiency.

At light loads, the inductor peak current is forced to the SFM peak current ($I_{PK\text{-}SFM}$) by turning on the high-side MOSFET. After the inductor current reaches $I_{PK\text{-}SFM}$, the high-side MOSFET is turned off, and the low-side MOSFET is turned on.

The low-side MOSFET is turned off when the inductor current reaches zero, and the device enters high impedance state. Consequently, the output voltage rises above the set voltage. The next switching cycle is initiated when the output voltage falls to the set voltage. As a result, the switching frequency decreases linearly as the load current reduces.

The device enters SFM mode when the inductor peak current demanded by the load is less than $I_{PK\text{-}SFM}$, and the inductor valley current reaches zero for 32 consecutive switching cycles. The device exits SFM mode when the inductor peak current demanded by the load exceeds $I_{PK\text{-}SFM}$.

In SFM mode, when the device stays in high impedance state in each switching cycle for more than 7.5µs, in eight consecutive switching cycles, the device enters hibernate mode from the subsequent switching cycle. In hibernate mode, whenever the device enters high impedance state between two MOSFET switching cycles, most of the internal blocks are turned off to minimize quiescent current. When the hibernate period reduces below 6.5µs, the device exits hibernate mode.

SFM mode offers better efficiency compared to PWM mode at light load conditions. However, the output-voltage ripple is higher than PWM mode due to reduced switching frequency at light loads. The output capacitance may be adjusted to achieve a desired steady state output voltage ripple.

Linear Regulator (INTVCC and EXTVCC)

The MAX1763x have two internal low-dropout linear regulators, IN-LDO and EXT-LDO, that power INTVCC. IN-LDO is powered from the IN pin and EXT-LDO is powered from the EXTVCC pin. IN-LDO is enabled during V_{IN} power-up or EN/UVLO power-up. Only one of these two linear regulators operates depending on the voltage at the EXTVCC pin. During power-up, the switchover from IN-LDO to EXT-LDO occurs at the end of the programmed soft-start time if the EXTVCC pin voltage is greater than 2.3V (V_{EXTVCC_UVR}). Powering INTVCC from EXT-LDO reduces on-chip dissipation and increases efficiency at higher input voltages. Connect the EXTVCC pin to the converter output voltage node for output voltages ranging from 2.5V to 12V for improved efficiency. The typical INTVCC output voltage is 1.8V. Bypass INTVCC to SGND with a 4.7µF low-ESR ceramic capacitor. INTVCC powers the internal blocks, the low-side MOSFET driver and recharges the external bootstrap capacitor.

The MAX1763x start switching only when the voltage at INTVCC is greater than 1.64V (V_{INTVCC_UVR}). The devices employ an undervoltage lockout circuit that forces the converter off when the INTVCC voltage falls below 1.58V (V_{INTVCC_UVF}). The hysteresis of 65mV prevents chattering on power-up/power-down.

In applications where the converter output is connected to the EXTVCC pin, if the output is shorted to ground, the transfer from EXT-LDO to IN-LDO happens seamlessly without impacting on the normal functionality. Connect EXTVCC pin to SGND when not in use.

Setting the Switching Frequency (RT)

The switching frequency of the device can be programmed from 400kHz to 2.2MHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor (R_{RT}) connected at the RT pin by the following equation:

$$R_{RT} = \frac{31914000}{f_{SW}} - 4.85$$

Where R_{RT} is in kΩ and f_{SW} is in Hz. Leave the RT pin open for a default f_{SW} of 500kHz. See *Table 4* for R_{RT} resistor values for a few common switching frequencies.

Table 4. Switching Frequency vs. R_{RT} Resistor

Switching Frequency (kHz)	R_{RT} Resistor (kΩ)
500	Open
400	75
500	59
2200	9.96

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage setting should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)}\right)}{1 - f_{SW(MAX)} \times t_{OFF\text{-}MIN(MAX)}} + I_{OUT(MAX)} \times \left(R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)}\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\text{-}MIN(MAX)}}$$

where,

V_{OUT} = Output voltage (V),

$I_{OUT(MAX)}$ = Maximum load current (A),

$R_{DCR(MAX)}$ = Worst-case DC resistance (Ω) of the inductor,

$f_{SW(MAX)}$ = Worst-case switching frequency (Hz),

$t_{OFF\text{-}MIN(MAX)}$ = Worst-case minimum switch off-time (s),

$t_{ON\text{-}MIN(MAX)}$ = Worst-case minimum switch on-time (s),

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Worst-case on-state resistances (Ω) of low-side and high-side internal MOSFETs, respectively.

Overcurrent Protection (OCP)/Hiccup Mode

The MAX1763x provide a robust overcurrent protection (OCP) scheme that protects the device under overload and output short-circuit conditions. The OCP scheme protects the device by using a hysteretic control of the inductor current that avoids the inductor current run-away condition. In hysteretic control, whenever the inductor peak current exceeds the specified peak current-limit threshold ($I_{PEAK\text{-}LIMIT}$), the high-side MOSFET is turned off, and the low-side MOSFET is turned on. When the inductor current crosses the lower current-limit threshold, the low-side MOSFET is turned off, and the high-side MOSFET is turned on. In addition, if the FB node voltage drops below 0.36V ($V_{FB\text{-}HICF}$) due to a fault condition any time after soft-start is completed, hiccup mode is activated.

In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 130ms. Once the hiccup timeout period expires, a soft-start is attempted again. Note that when a soft-start is attempted under overload conditions if the FB node voltage does not exceed 0.41V, the device continues in hysteretic control for the total time duration of the programmed soft start time and 2ms. The hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

The device provides a valley current protection scheme that protects itself in PWM mode from large negative currents. Under strong external output bias conditions, when the inductor current falls below the specified valley current-limit threshold ($I_{VALLEY\text{-}LIMIT}$), the device enters high impedance state where both the MOSFETs are turned off and the inductor current reaches 0A. The device recovers from a high impedance state and starts switching when the output voltage falls below the regulation point when the external output bias is removed.

Output-Voltage Status and Die Temperature Monitor ($\overline{\text{RESET}}$/TJ)

The MAX1763x offer a $\overline{\text{RESET}}$/TJ pin that can be used to monitor either the status of the output voltage or the die temperature. The two functions cannot be used at the same time.

To monitor the status of the converter output voltage, the open-drain $\overline{\text{RESET}}$/TJ output requires an external pullup resistor to a bias supply voltage. During startup, $\overline{\text{RESET}}$/TJ goes high (high impedance) with a delay of 2ms after the feedback voltage (V_{FB}) increases above 95% ($V_{FB\text{-}OKR}$). $\overline{\text{RESET}}$/TJ is pulled low when V_{FB} drops below 91.7% ($V_{FB\text{-}OKF}$). $\overline{\text{RESET}}$/TJ is also pulled low during thermal shutdown or when EN/UVLO pin goes below 1.15V (V_{ENF}).

To monitor the die temperature, connect a 20kΩ resistor from $\overline{\text{RESET}}$/TJ to SGND. The die temperature monitor feature is functional only when the output voltage is above 95% ($V_{FB\text{-}OKR}$) of its set point. During fault conditions like thermal shutdown, VIN UVLO, and VCC UVLO, this pin is pulled low and die temperature monitoring is not supported. Die temperature monitoring is also not supported during hibernation in SFM mode.

The die temperature (T_J) in °C is calculated as follows:

$$T_J = \frac{(V_{TJ} - V_{T25})}{(2 \times 10^{-3})} + 25$$

where,

V_{TJ} is the $\overline{\text{RESET}}$/TJ pin voltage in V when the converter is loaded.

Prebiased Output

When the MAX1763x start into a prebiased output, the high-side and the low-side switches remain turned off so that the converter does not sink current from the output. The switching of the MOSFETs commences only after the voltage at the SS pin (V_{SS}) crosses the voltage at the feedback pin (V_{FB}). V_{FB} then smoothly ramps up to $V_{FB\text{-}REG}$ in alignment with the V_{SS}, and the output voltage reaches its target value.

Thermal-Shutdown Protection

The MAX1763x offer internal thermal shutdown protection to limit the junction temperature. When the junction temperature of the device exceeds +175°C, an on-chip thermal sensor shuts down the device, allowing the device to cool down. The device turns on with soft-start after the junction temperature cools down by 10°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown in normal operation.

APPLICATIONS INFORMATION

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source, reducing noise and voltage ripple on the input caused by the circuit's switching. The following equation defines the input capacitor RMS current requirement (I_{RMS}):

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{(V_{IN}\text{-}V_{OUT}) \times V_{OUT}}}{V_{IN}}$$

where,

$I_{OUT(MAX)}$ is the maximum load current.

I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1\text{-}D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where,

D = V_{OUT}/V_{IN} is the duty ratio of the converter,

f_{SW} = the switching frequency,

ΔV_{IN} = the allowable input voltage ripple,

η = the efficiency.

Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the input capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{V_{OUT}}{K \times f_{SW}}$$

Where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. See Table 5 for the value of K for the respective devices. Select an inductor whose value is nearest to the value calculated by the previous formula. Select a low-loss inductor with acceptable dimensions and the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above $I_{PEAK\text{-}LIMIT}$.

Table 5. Part Number vs. Value of K

Part Number	Value of K
MAX17639	4.8
MAX17638	4.7
MAX17636	3.5

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 25% of the maximum output current in the application, so the output-voltage deviation is contained to 3% of the output voltage. The minimum required output capacitance can be calculated as follows:

$$C_{OUT1} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

where,

I_{STEP} = Load current step,

$t_{RESPONSE}$ = Response time of the controller,

ΔV_{OUT} = Allowable output-voltage deviation,

f_C = Target closed-loop crossover frequency,

f_{SW} = Switching frequency.

Select f_C to be 1/8th of f_{SW} for the switching frequencies less than or equal to 640 kHz. If the switching frequency is more than 640 kHz, select f_C to be 80kHz.

The minimum required output capacitance required to meet the output voltage ripple specification ($\Delta V_{OUT\text{-}RIPPLE}$) in SFM mode at a particular load (I_O) is calculated as follows:

$$C_{OUT2} = \frac{1}{2} \times \frac{L_{SEL} \times (I_{PK\text{-}SFM} - I_O)^2}{\Delta V_{OUT\text{-}RIPPLE}} \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)$$

where I_O is less than or equal to half of $I_{PK\text{-}SFM}$.

Select the output capacitance to be the higher of C_{OUT1} and C_{OUT2}. Actual derating of ceramic capacitors with DC bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Soft-Start capacitor selection

The MAX1763x implement an adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{OUT_SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 14 \times 10^{-6} \times C_{OUT\_SEL} \times V_{OUT}$$

where C_{OUT_SEL} and C_{SS} are in Farad.

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{8.33 \times 10^{-6}}$$

where C_{SS} is in Farad and t_{SS} is in seconds. For example, to program a 1ms soft-start time, an 8200pF capacitor should be connected from the SS pin to SGND. The MAX1763x offer a minimum programmable soft-start time of 1ms. Note that, during start-up, device operates at a variable switching frequency until the output voltage reaches 95% of set output voltage.

Setting the Input Undervoltage-Lockout Level

The MAX1763x offer an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to SGND (see *Figure 52*). Connect the center node of the divider to EN/UVLO pin. Choose R_{UVL_TOP} to be 3.32MΩ and then calculate R_{UVL_BOT} as follows:

$$R_{UVL\_BOT} = \frac{R_{UVL\_TOP} \times V_{ENR}}{(V_{INU} - V_{ENR})}$$

where V_{INU} is the voltage at which the device is required to turn on. It is recommended that V_{INU} is higher than 0.8 x V_{OUT} to avoid hiccup during slow power up (slower than soft start)/power down. If the EN/UVLO pin is driven from an external signal source, a series resistance of a minimum 1kΩ is recommended to be placed between the output pin of signal source and the EN/UVLO pin to reduce voltage ringing on the line.

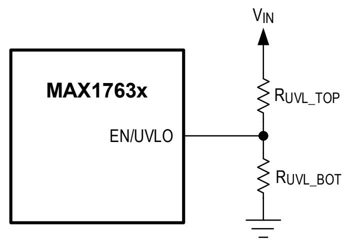


Figure 52. Setting the Input Undervoltage Lockout

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the output-voltage node (V_{OUT}) to SGND (see *Figure 53*). Connect the center node of the resistive divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_{FB_TOP} (kΩ) from the output-voltage node (V_{OUT}) to the FB pin as follows:

$$R_{FB\_TOP} = \frac{578}{f_C \times C_{OUT\_SEL}}$$

where,

f_C = Crossover frequency (Hz),

C_{OUT_SEL}= Actual capacitance (F) of selected output capacitor at DC-bias voltage.

Calculate resistor R_{FB_BOT} (kΩ) connected from the FB pin to SGND as follows:

$$R_{FB\_BOT} = \frac{R_{FB\_TOP} \times 0.6}{V_{OUT} - 0.6}$$

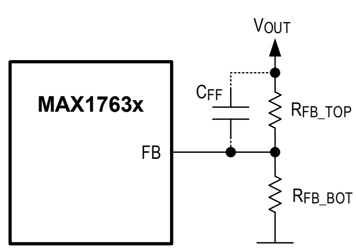


Figure 53. Setting the Output Voltage

Add a capacitor (C_{FF}) across R_{FB_TOP} when the part is used in SFM mode or when dynamic mode change is used in an application. C_{FF} is not needed when the part is used in PWM mode alone.

Calculate the capacitance (C_{FF}) value using the following equation:

$$\frac{330}{R_{FB\_TOP}} < C_{FF} < \frac{500}{R_{FB\_TOP}}$$

where,

R_{FB_TOP} = Top side feedback resistance (kΩ),

C_{FF} = Feedforward capacitance (pF). C_{FF} must be chosen to withstand output voltage.

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = P_{OUT} \times \left(\frac{1}{\eta}\text{-}1\right) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where,

P_{OUT} is the output power (W),

η is the efficiency of the converter,

R_{DCR} is the DC resistance (Ω) of the inductor (see the *Typical Performance Characteristics* for more information on efficiency at typical operating conditions).

The die temperature (T_J) of the device may also be estimated at any given maximum ambient temperature (T_A) from the following equation, when the die temperature monitor ($\overline{\text{RESET}}$/TJ) feature is not used.

$$T_J = T_A + \left(\theta_{JA} \times P_{LOSS}\right)$$

Note: Junction temperatures greater than +125°C degrade operating lifetimes.

Printed Circuit Board (PCB) Layout Guidelines

All traces carrying pulsed currents must be very short and as wide as possible. The inductance of these traces must be kept to an absolute minimum due to the high di/dt of the currents. Since the inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI. When routing the circuitry around the IC, the signal ground (SGND), and the power ground (PGND) for switching currents must be kept separate. PCB layout also affects the thermal performance of the design.

- Place the input capacitors as close as possible to the IN and PGND pins.
- Connect the INTVCC capacitor close to the INTVCC pin and connect the other terminal to the SGND plane.
- Place the BST capacitor close to the BST and LX pins.
- Place the inductor as close as possible to the LX pin. Minimize the length and area of the trace connection from the LX pin to the inductor.
- Place the output capacitors as close as possible to non-switching side of the inductor.
- Place the PGND terminals of the input capacitor and output capacitor as close as possible to the PGND pins and connect them to the PGND plane.
- Place the RT resistor, SS capacitor and FB resistors as close as possible to their respective pins. Connect their other terminals to the SGND plane.
- Keep all the power and load connections short to keep inductances at minimum levels.

- Connect the PGND and SGND nodes at a point where the switching activity is at its minimum, at the negative terminal of the INTVCC bypass capacitor.
- Several thermal throughputs (vias) that connect to a large plane should be provided under IN, PGND and LX pins for efficient heat dissipation.

Refer to the MAX17639 evaluation board user guide for recommended PCB layout and routing.

TYPICAL APPLICATION CIRCUITS

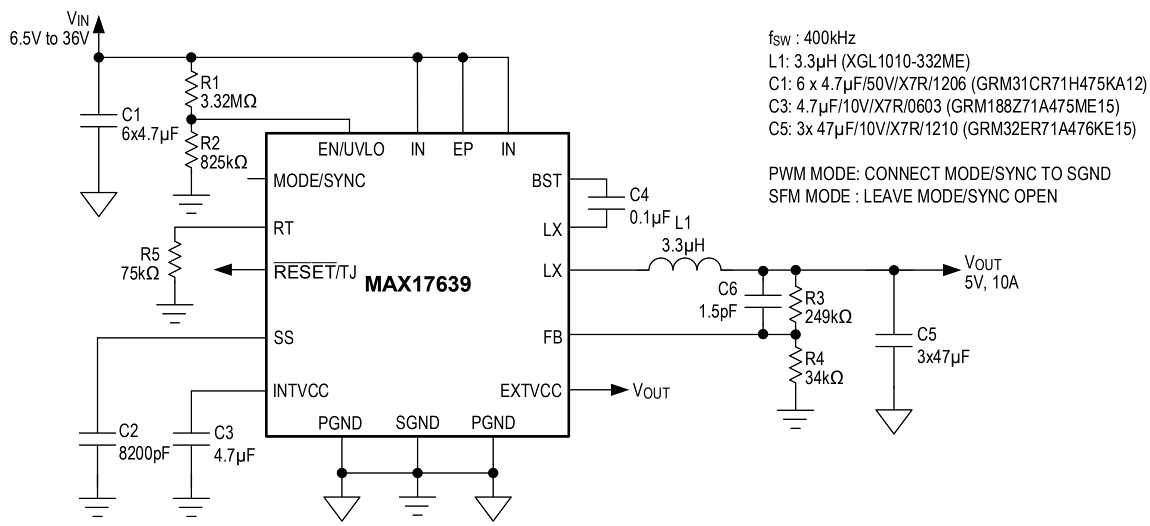


Figure 54. 5V Output with 400kHz Switching Frequency

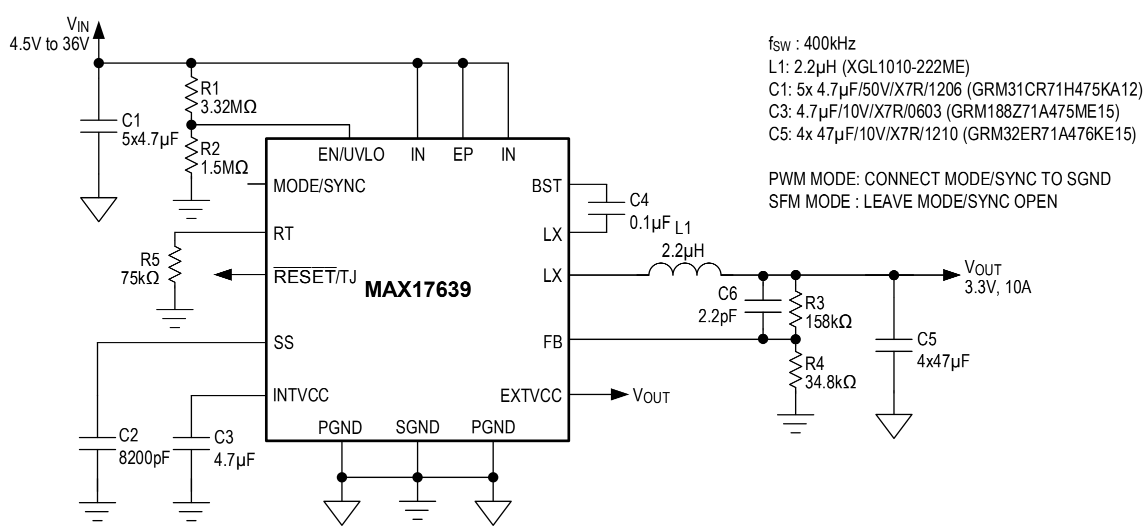


Figure 55. 3.3V Output with 400kHz Switching Frequency

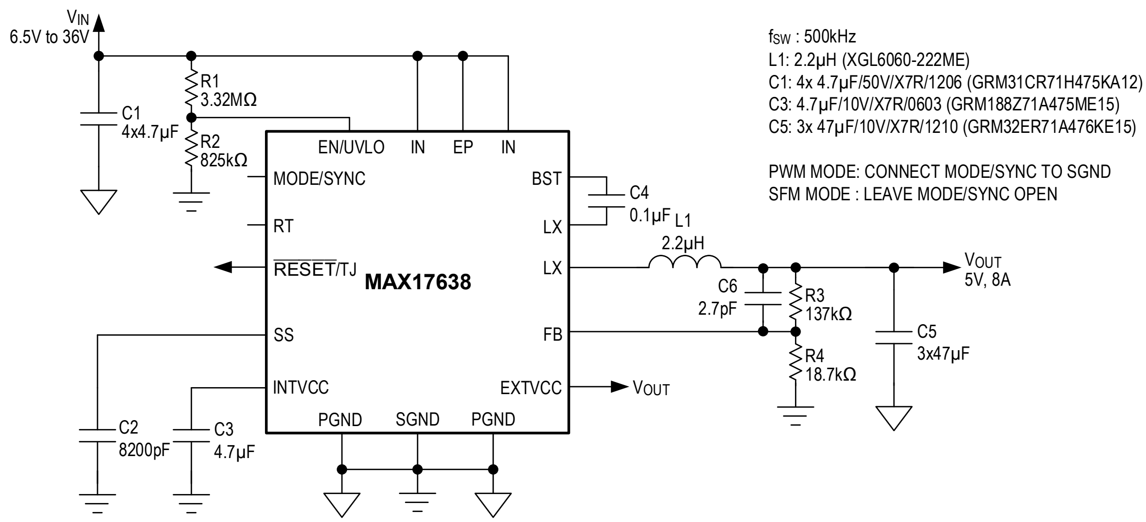


Figure 56. 5V Output with 500kHz Switching Frequency

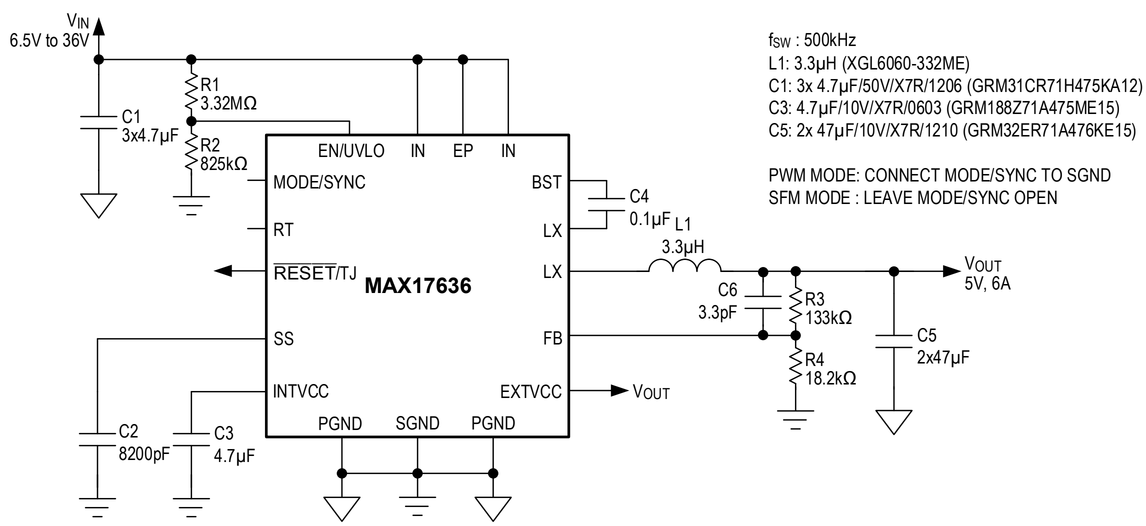


Figure 57. 5V Output with 500kHz Switching Frequency

OUTLINE DIMENSIONS

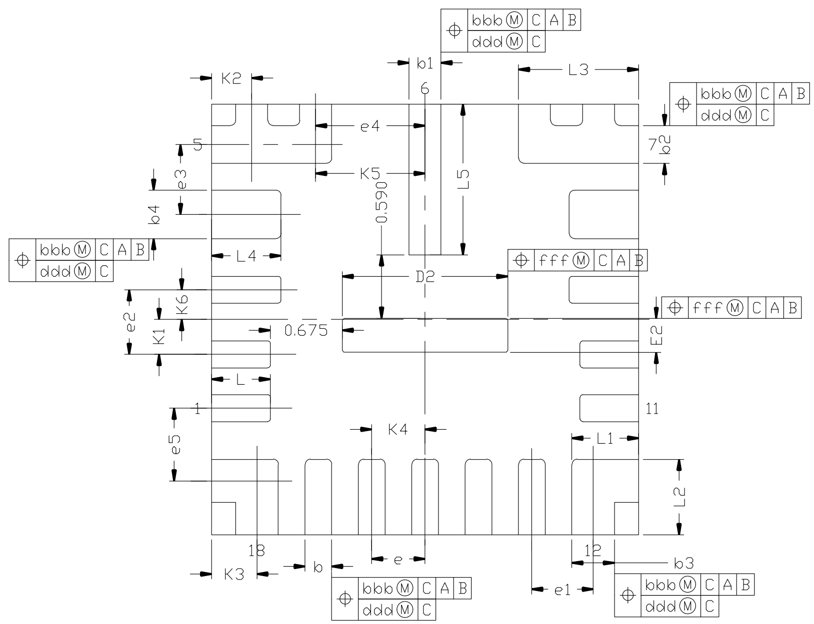
Table 6. Thermal Resistance of 18L FC2QFN

Thermal Resistance, Four-Layer Board (Note 1)	
Junction to Ambient (θ_{JA})	19°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2.02°C/W

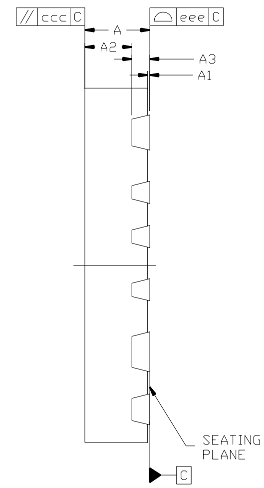
Note 1: Package thermal resistances were obtained using the MAX17639 evaluation kit with no airflow.

For the latest package outline information and land patterns (footprints), refer to *package index* at www.analog.com. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

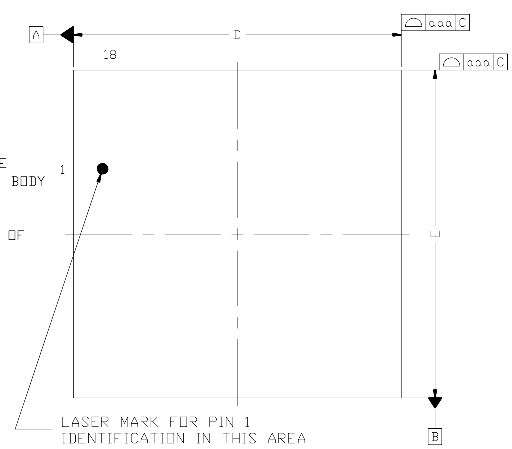
PACKAGE OUTLINE, 18L FC2QFN
4x4x0.75 MM



BOTTOM VIEW



SIDE VIEW



TOP VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	—	0.050	0.000	—	0.002
A2	—	0.530	0.580	—	0.021	0.023
A3		0.203	REF.		0.008	REF.
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.250	0.300	0.350	0.010	0.012	0.014
b2	0.300	0.350	0.400	0.012	0.014	0.016
b3	0.350	0.400	0.450	0.014	0.016	0.018
b4	0.400	0.450	0.500	0.016	0.018	0.020
D		4	BSC		0.157	BSC
D2	1.450	1.550	1.650	0.057	0.061	0.065
E		4	BSC		0.157	BSC
E2	0.215	0.315	0.415	0.008	0.012	0.016
L	0.450	0.550	0.650	0.018	0.022	0.026
L1	0.525	0.625	0.725	0.021	0.025	0.029
L2	0.600	0.700	0.800	0.024	0.028	0.031
L3	1.025	1.125	1.225	0.040	0.044	0.048
L4	0.550	0.650	0.750	0.022	0.026	0.030
L5	1.300	1.400	1.500	0.051	0.055	0.059
e		0.500	BSC		0.020	BSC
e1		0.575	BSC		0.023	BSC
e2		0.600	BSC		0.024	BSC
e3		0.650	BSC		0.026	BSC
e4		1.025	BSC		0.040	BSC
e5		0.675	BSC		0.027	BSC
K1		0.325	BSC		0.013	BSC
K2		0.375	BSC		0.015	BSC
K3		0.425	BSC		0.017	BSC
K4		0.500	BSC		0.020	BSC
K5		1.025	BSC		0.040	BSC
K6		0.275	BSC		0.011	BSC
TOLERANCES OF FORM AND POSITION						
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.050			0.002	
eee		0.080			0.003	
fff		0.100			0.004	

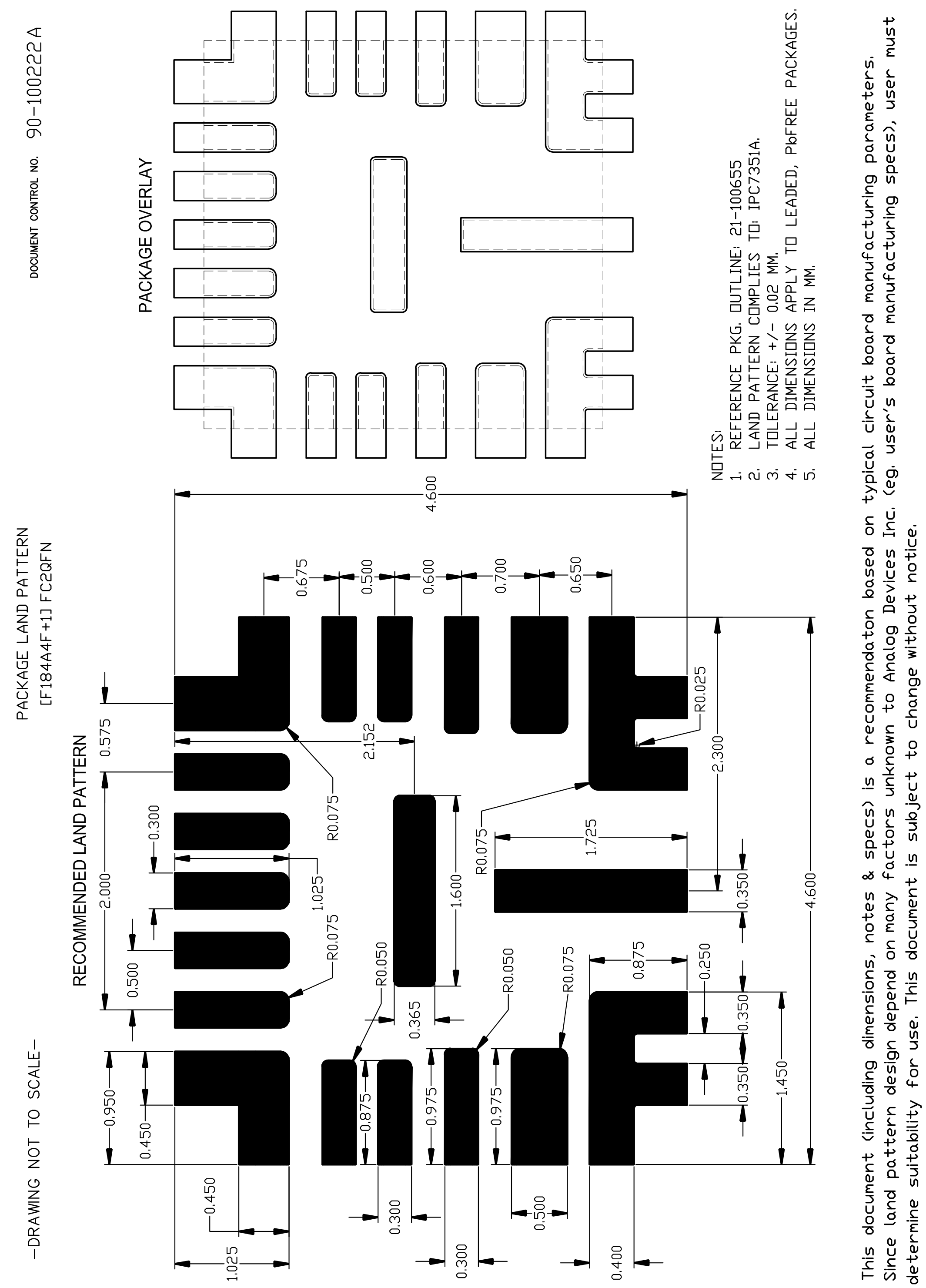
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. PACKAGE WARPAGE MAX 0.08 mm.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. APPLIED ONLY TO TERMINALS.
8. PKG CODE is F184A4F+1.

-DRAWING NOT TO SCALE-

DOCUMENT CONTROL NO. 21-100655A

Land Pattern



ORDERING GUIDE

Table 7. Ordering Guide

Part Number	Temperature Range	Pin Package
MAX17639AFN+	-40°C to +150°C	18-FC2QFN (4mm x 4mm)
MAX17639AFN+T	-40°C to +150°C	18-FC2QFN (4mm x 4mm)
MAX17638AFN+*	-40°C to +150°C	18-FC2QFN (4mm x 4mm)
MAX17638AFN+T*	-40°C to +150°C	18-FC2QFN (4mm x 4mm)
MAX17636AFN+*	-40°C to +150°C	18-FC2QFN (4mm x 4mm)
MAX17636AFN+T*	-40°C to +150°C	18-FC2QFN (4mm x 4mm)

+Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

*Potential future product.