65V, 7A/8A Peak Synchronous Step-Down Silent Switcher with 2.5µA Quiescent Current

FEATURES

- **Silent Switcher®** Architecture
  - Ultralow EMI Emissions
  - Optional Spread Spectrum Modulation
- High Efficiency at High Frequency
  - Up to 95% Efficiency at 1MHz, $12V_{IN}$ to $5V_{OUT}$
  - Up to 94% Efficiency at 2MHz, $12V_{IN}$ to $5V_{OUT}$
- Wide Input Voltage Range: 3.4V to 65V
- 7A Maximum Continuous Output, 8A Peak Transient Output
- Ultralow Quiescent Current Burst Mode® Operation
  - 2.5µA I_Q Regulating $12V_{IN}$ to $3.3V_{OUT}$
  - Output Ripple < $10mV_{P-P}$
- Fast Minimum Switch On-Time: 40ns
- Low Dropout Under All Conditions: 60mV at 1A
- Adjustable and Synchronizable: 200kHz to 2.2MHz
- Peak Current Mode Operation
- Output Soft-Start and Tracking
- Small 27-Lead 6mm × 3mm Flip chip 2 quad flat no-lead (FC2QFN) Package

GENERAL DESCRIPTION

The **LT®8647** synchronous step-down regulator features Silent Switcher architecture designed to minimize Electromagnetic interference (EMI) emissions while delivering high efficiency at high switching frequencies. This performance makes the LT8647 ideal for noise-sensitive applications and environments.

The fast, clean, low-overshoot switching edges enable high-efficiency operation even at high-switching frequencies, leading to a small overall solution size. Peak current mode control with a 40ns minimum on-time allows high step-down ratios even at high switching frequencies.

Burst Mode operation enables ultralow standby current consumption, pulse-skipping mode allows full switching frequency at lower output loads, and spread spectrum operation can further reduce EMI emissions.

APPLICATIONS

- Industrial Supplies
- General Purpose Step-Down

TYPICAL APPLICATION

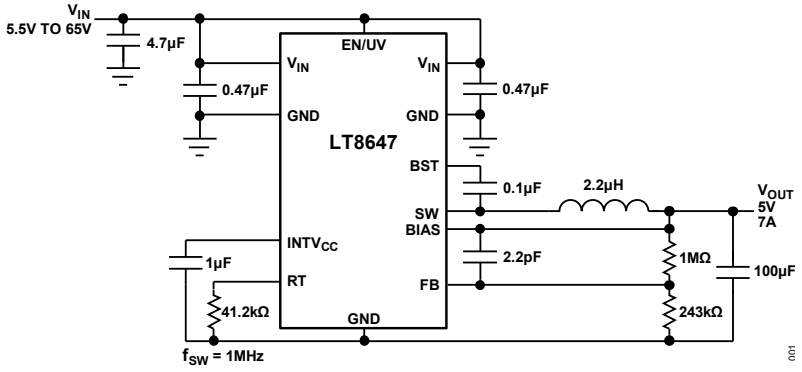

Figure 1. 5V, 7A Step-Down Converter

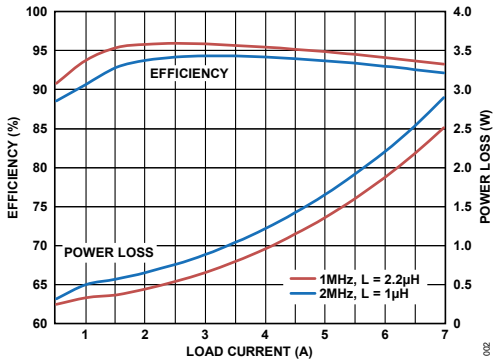

Figure 2. $12V_{IN}$ TO $5V_{OUT}$ Efficiency vs. Frequency

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	7/25	Initial release	—
A	8/25	Updated Figure 23 and Figure 24 in the *Typical Performance Characteristics* section.	16
B	12/25	Updated V_{IN}, SW, EN/UV value from 65V to 70V in *Table 2. Absolute Maximum Ratings* section.	6

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_J = –40°C to +150°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Input Voltage			3.0	3.4	V
V_{IN} Quiescent Current in Shutdown	$V_{EN/UV}$ = 0V, T_A = +25°C		0.9	3	µA
	$V_{EN/UV}$ = 0V		0.9	20	µA
V_{IN} Quiescent Current in Sleep	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 0V, T_A = +25°C		1.7	4	µA
	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 0V		1.7	20	µA
V_{IN} Quiescent Current when Active	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 2V, R_T = 60.4kΩ, V_{BIAS} = 0V, T_A = +25°C		0.4	0.6	mA
V_{IN} Current in Regulation	V_{OUT} = 0.97V, V_{IN} = 6V, I_{LOAD} = 1mA, V_{SYNC} = 0V, T_A = +25°C		200	300	µA
Feedback Reference Voltage	V_{IN} = 6V, T_A = +25°C	0.964	0.970	0.976	V
	V_{IN} = 6V	0.956	0.970	0.982	V
Feedback Voltage Line Regulation	V_{IN} = 4V to 42V		0.004	0.025	%/V
Feedback Pin Input Current	V_{FB} = 1V, T_A = +25°C	-20		20	nA
BIAS Pin Current Consumption	V_{BIAS} = 3.3V, f_{SW} = 2MHz, T_A = +25°C		22		mA
Minimum On-Time[2]	I_{LOAD} = 3A, SYNC = 0V		40	65	ns
	I_{LOAD} = 3A, SYNC = 2V		35	65	ns
Minimum Off-Time	T_A = +25°C		80	110	ns
Oscillator Frequency	R_T = 221kΩ	180	210	240	kHz
	R_T = 60.4kΩ	665	700	735	kHz
	R_T = 18.2kΩ	1.8	1.95	2.1	MHz
Top Power N-Channel Metal-Oxide-Semiconductor (NMOS) On-Resistance	I_{SW} = 1A, T_A = +25°C		36		mΩ
Top Power NMOS Current Limit		10.5	14	17.5	A
Bottom Power NMOS On-Resistance	V_{INTVCC} = 3.4V, I_{SW} = 1A, T_A = +25°C		25		mΩ
Bottom Power NMOS Current Limit	V_{INTVCC} = 3.4V, T_A = +25°C	7.5	11	14	A
SW Leakage Current	V_{IN} = 42V, V_{SW} = 0V, 42V, T_A = +25°C	-1.5		1.5	µA
EN/UV Pin Threshold	EN/UV Rising	0.95	1.01	1.07	V
EN/UV Pin Hysteresis	T_A = +25°C		45		mV

(T_J = –40°C to +150°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EN/UV Pin Current	$V_{EN/UV}$ = 2V, T_A = +25°C	-20		20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Falling	5	7.5	10	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Rising	-10.5	-8	-5.5	%
PG Hysteresis	T_A = +25°C		0.4		%
PG Leakage Current	V_{PG} = 3.3V, T_A = +25°C	-40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.1V		750	2000	Ω
SYNC/MODE Threshold	SYNC/MODE DC and Clock Low-Level Voltage	0.7	0.9		V
	SYNC/MODE Clock High-Level Voltage		1.2	1.4	V
	SYNC/MODE DC High-Level Voltage	2.2	2.55	2.9	V
Spread Spectrum Modulation Frequency Range	R_T = 60.4kΩ, V_{SYNC} = 3.3V, T_A = +25°C		24		%
Spread Spectrum Modulation Frequency	V_{SYNC} = 3.3V, T_A = +25°C		2.5		kHz
TR/SS Source Current		1.2	2	2.8	µA
TR/SS Pull-Down Resistance	Fault Condition, TR/SS = 0.1V, T_A = +25°C		220		Ω

1 Specifications over the –40°C and 150°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls.

2 Guaranteed by design and characterization, not production tested.

3 High junction temperatures degrade operating lifetimes. The Operating lifetime is derated at junction temperatures exceeding 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (PD, in Watts) according to the formula:

$$T_J = T_A + PD \times \theta_{JA}$$

Where θ_{JA} (in °C /W) is the package thermal resistance.

4 This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, SW, EN/UV	70V
PG	42V
BIAS	25V
FB, TR/SS	4V
BST-SW	7V
RT, SYNC/MODE	6V
LT8647R	-40°C to 150°C
Storage Temperature Range	-65°C to 150°C
Maximum Reflow (Package Body) Temperature	260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Electrostatic Discharge (ESD)

The following ESD information is provided for the handling of ESD-sensitive devices in an ESD-protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 and Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 3. LT8647 ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)
HBM	±2500
CDM	±1250

ESD Caution

Electrostatic discharge (ESD) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

Table 4. Thermal Resistance on EVAL-LT8647-AZ

Thermal Resistance, Four-Layer Board	
Junction-to-Ambient (θ_{JA})	26°C/W
Junction-to-Case (θ_{JCtop})	20.2°C/W
Junction-to-Case Thermal Resistance (Ψ_{JT})	0.3°C/W

Table 5. Thermal Resistance on JEDEC Board

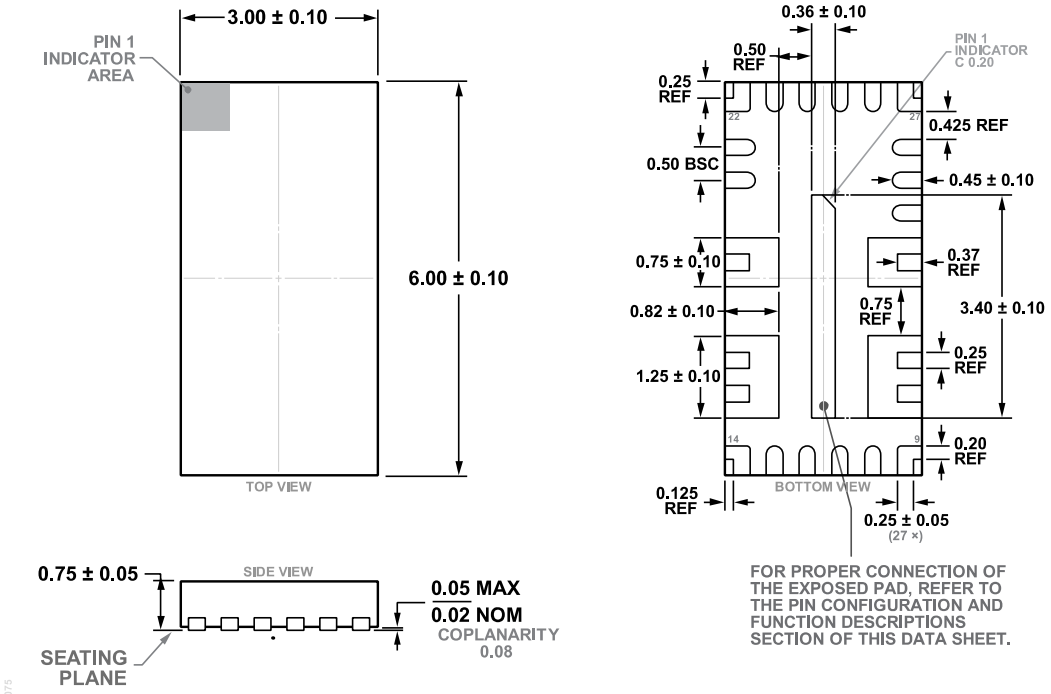
Thermal Resistance, Four-Layer Board[1]	
Junction-to-Ambient (θ_{JA})	30.6°C/W
Junction-to-Case (θ_{JCtop})	20.2°C/W
Junction-to-Case Thermal Resistance (Ψ_{JT})	0.2°C/W

[1] Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

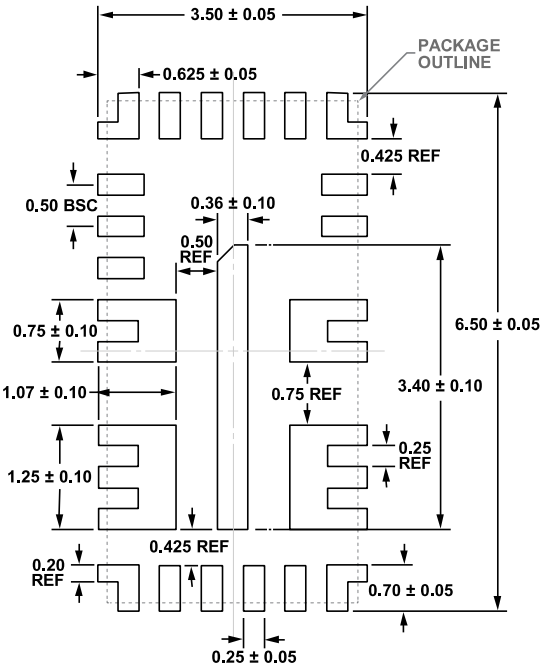
For the latest package outline information and land patterns (footprints), refer to the **Packaging Index**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may display a different suffix character, but the drawing still pertains to the package, regardless of its RoHS status.

Package thermal resistances were obtained using the evaluation kit, a four-layer board. For detailed information on package thermal considerations, refer to **Thermal Characterization of IC Packages**.

FC2QFN PACKAGE (CP-27-1)
27-LEAD (3mm × 6mm × 0.75mm)



RECOMMENDED SOLDER PAD LAYOUT
(TOP VIEW)



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

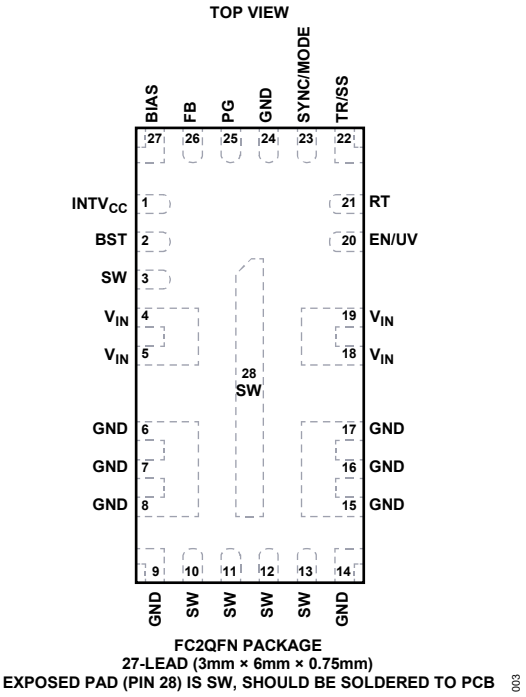


Figure 3. Pin Configuration

Pin Descriptions

Table 6. Pin Descriptions

PIN	NAME	FUNCTION	TYPE
1	$INTV_{CC}$	Internal 3.4V Regulator Bypass Pin. This voltage powers the internal power drivers and control circuits. The $INTV_{CC}$'s maximum output current is 25mA. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ current will be supplied from BIAS if BIAS > 3.1V; otherwise, current will be drawn from V_{IN}. The voltage on $INTV_{CC}$ will vary between 2.8V and 3.4V when BIAS is between 3.0V and 3.6V. Place a low ESR ceramic capacitor of at least 1µF from this pin to ground, close to the IC.	Analog Output Internal supply
2	BST	This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 0.1µF boost capacitor as close as possible to the IC.	Analog Output
3	SW	The SW pins are the outputs of the internal power switches. Use this pin to tie the boost capacitor from BST to SW.	Analog Output
4, 5, 18, 19	V_{IN}	The V_{IN} pins supply current to the LT8647 internal circuitry and the internal topside power switch. The LT8647 requires the use of multiple V_{IN} bypass capacitors. Two small 0.47µF capacitors should be placed as close as possible to the LT8647, one capacitor on each side of the device (C_{IN1}, and C_{IN2}). A third	Analog Input

PIN	NAME	FUNCTION	TYPE
		capacitor with a large value, 4.7µF or higher, should be placed near C_{IN1} or C_{IN2}. See the *Applications Information* section for a sample layout.	
—	NC	Half-Etched.	
6, 7, 8, 9, 14, 15, 16, 17	GND	Ground. Place the negative terminal of the input capacitor as close as possible to the GND pins. See the *Applications Information* section for a sample layout.	Analog Input
10, 11, 12, 13, Exposed Pad (Pin 28)	SW	The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor. This node should be kept small on the Printed circuit board (PCB) for good performance and low EMI. The exposed pad should be connected and soldered to the SW trace for good thermal performance. If necessary, due to manufacturing limitations, exposed pad may be left disconnected. However, thermal performance will be degraded.	Analog Output
20	EN/UV	The LT8647 is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.01V going up and 0.965V going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8647 will shut down.	Analog Input
21	RT	A resistor is tied between the RT pin and ground to set the switching frequency.	Digital Input
22	TR/SS	Output Tracking and Soft-Start Pin. This pin allows the user to control the output voltage ramp rate during startup. A TR/SS voltage below 0.97V forces it to regulate the FB pin to equal the TR/SS pin voltage. When TR/SS exceeds 0.97V, the tracking function is disabled, and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed.	Analog Input
23	SYNC/MODE	This pin programs four different operating modes: 1) Burst Mode: Tie this pin to ground for Burst Mode operation at low output loads—this will result in an ultralow quiescent current. 2) Pulse-skipping mode: This mode offers full-frequency operation down to low output loads before pulse skipping occurs. Float this pin for pulse-skipping mode. When floating, pin leakage currents should be <1µA.	Digital Input

PIN	NAME	FUNCTION	TYPE
		3) Spread spectrum mode: Tie this pin high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V for pulse-skipping mode with spread-spectrum modulation. 4) Synchronization mode: Drive this pin with a clock source to synchronize to an external frequency. During synchronization, the part will operate in pulse-skipping mode.	
24	GND	Ground. Connect this pin to the system ground and to the ground plane.	
25	PG	The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±8% of the final regulation voltage, and there are no fault conditions. PG is pulled low when EN/UV is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown. PG is valid when V_{IN} is above 3.4V.	Digital Output
26	FB	The LT8647 regulates the FB pin to 0.97V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor ranges from 1pF to 10pF.	Analog Input
27	BIAS	The internal regulator will draw current from BIAS instead of V_{IN} when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V to 25V, this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT}, use a 1µF local bypass capacitor on this pin. If no supply is available, tie to GND. However, especially for high-input or high-frequency applications, BIAS should be tied to output or an external supply of 3.3V or above.	Analog Input Internal supply

BLOCK DIAGRAM

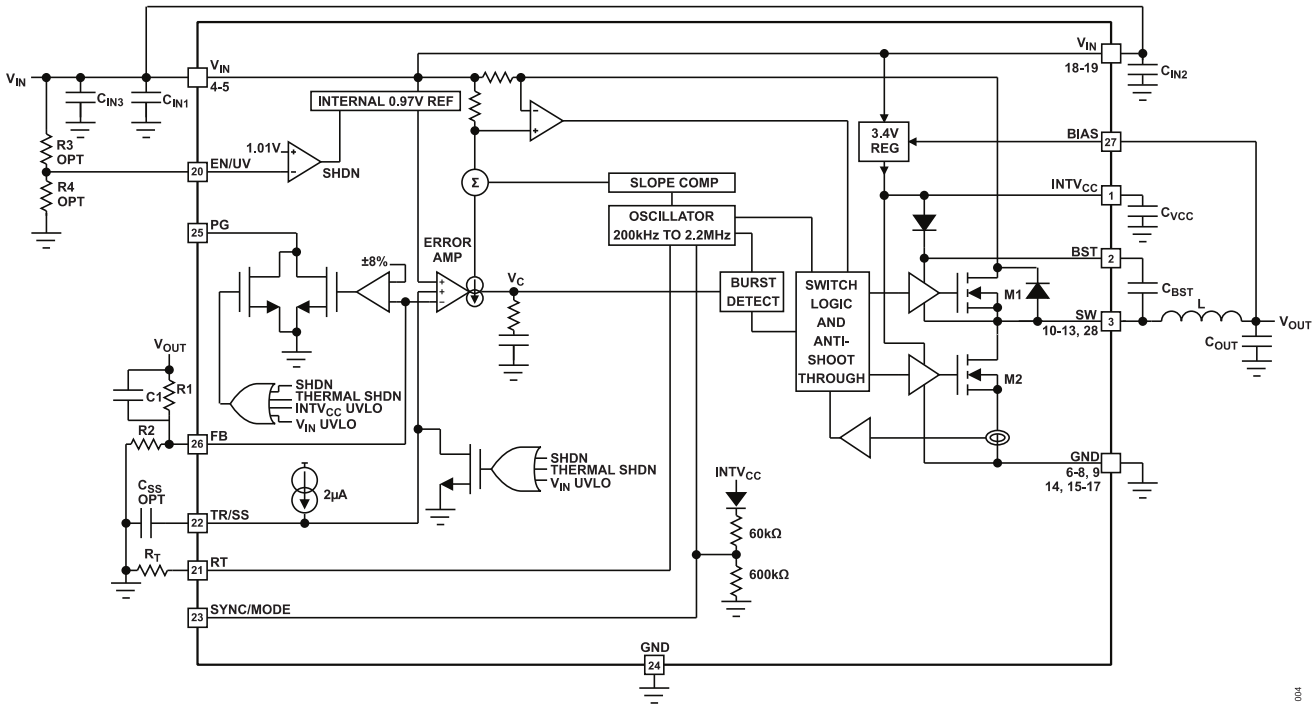


Figure 4. LT8647 Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise specified.

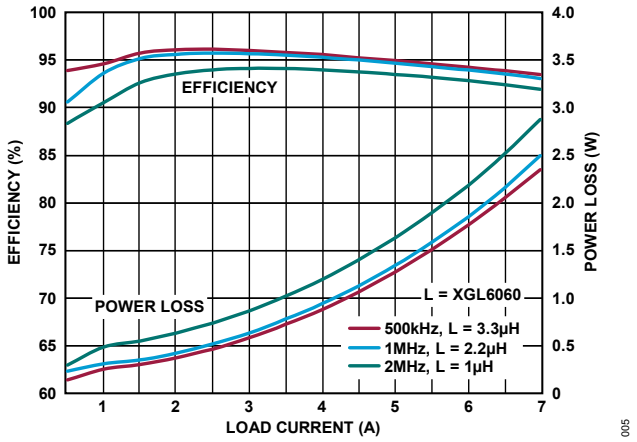


Figure 5. $12V_{IN}$ to $5V_{OUT}$ Efficiency vs. Frequency

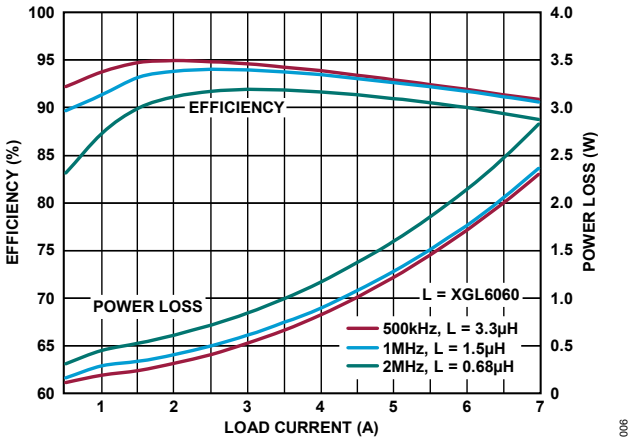


Figure 6. $12V_{IN}$ to $3.3V_{OUT}$ Efficiency vs. Frequency

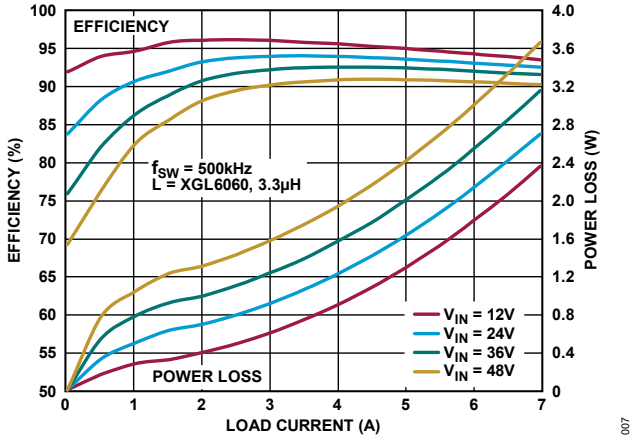


Figure 7. Efficiency at $5V_{OUT}$

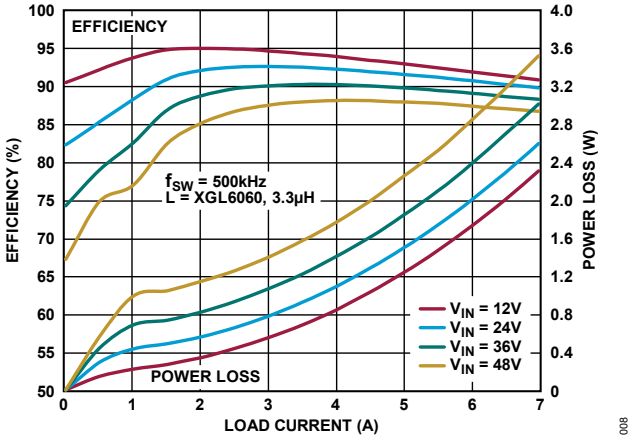


Figure 8. Efficiency at $3.3V_{OUT}$

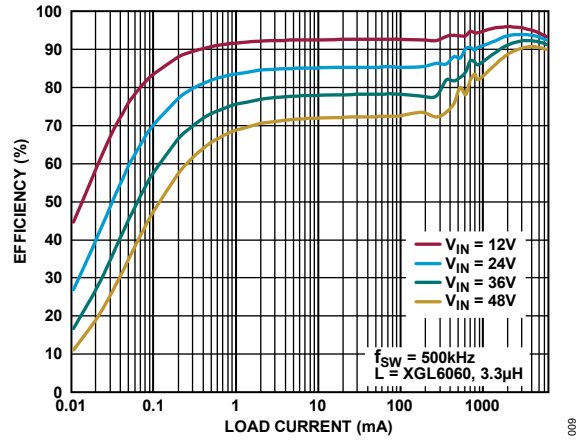


Figure 9. Low-Load Efficiency at $5V_{OUT}$

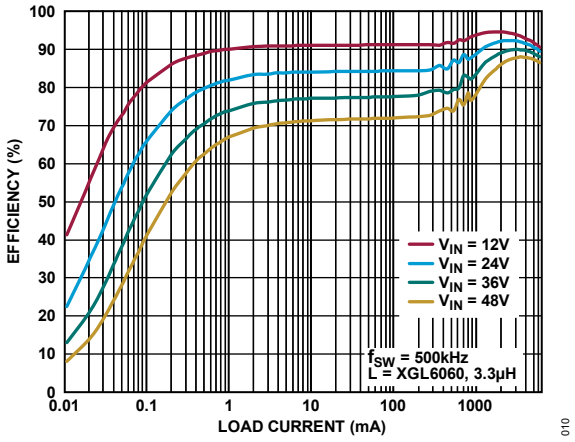


Figure 10. Low-Load Efficiency at $3.3V_{OUT}$

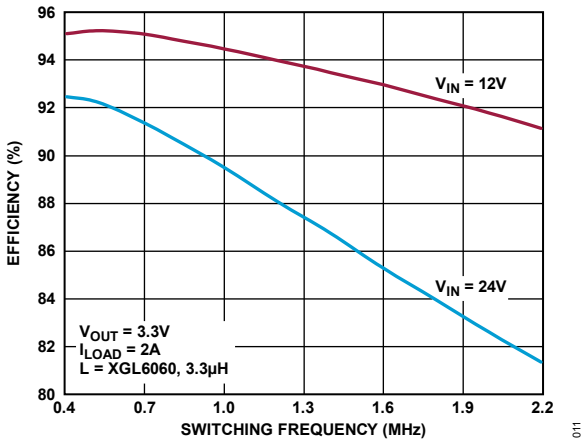


Figure 11. Efficiency vs. Frequency

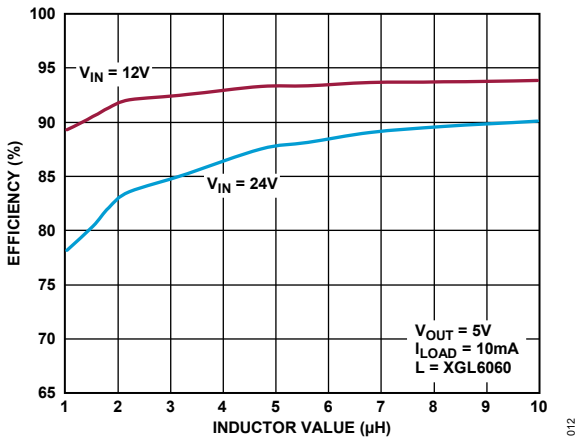


Figure 12. Burst Mode Operation Efficiency vs. Inductor Value

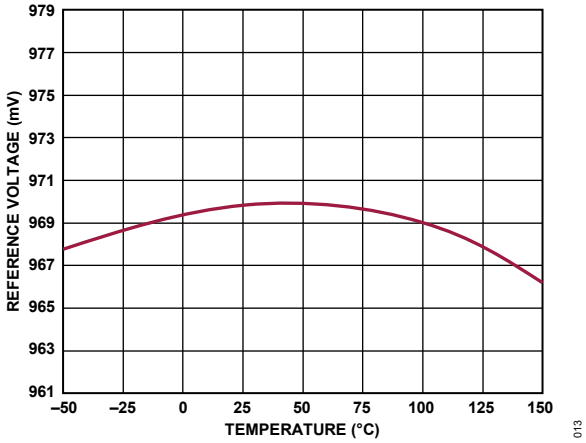


Figure 13. Reference Voltage

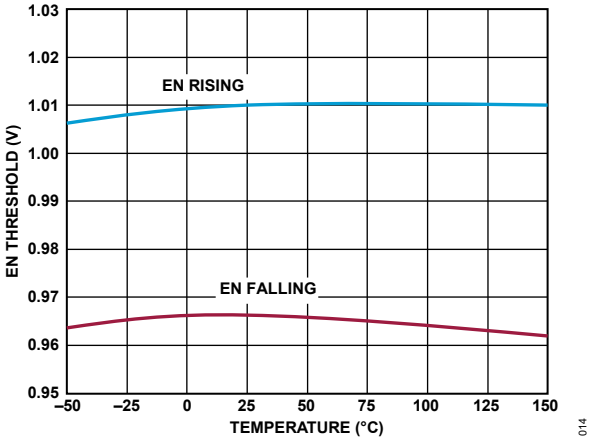


Figure 14. EN Pin Thresholds

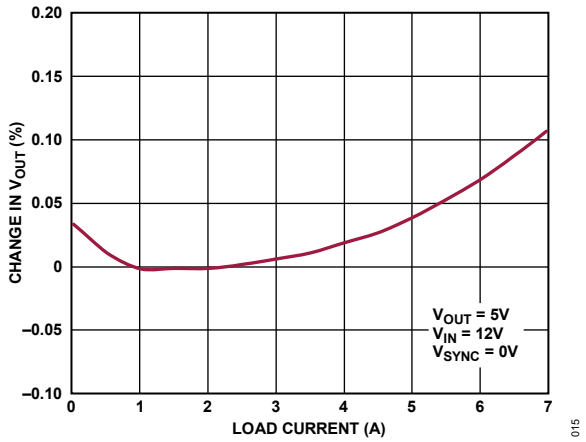


Figure 15. Load Regulation

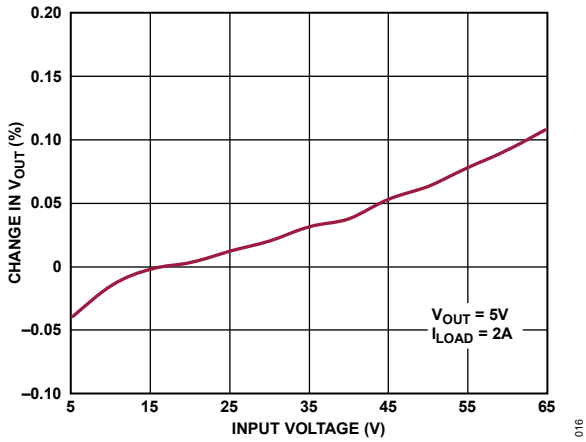


Figure 16. Line Regulation

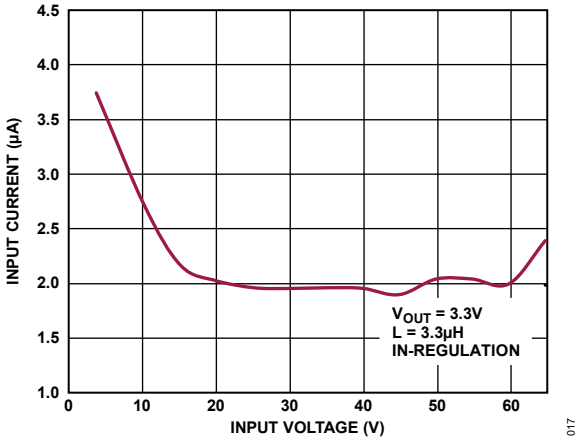


Figure 17. No-Load Supply Current

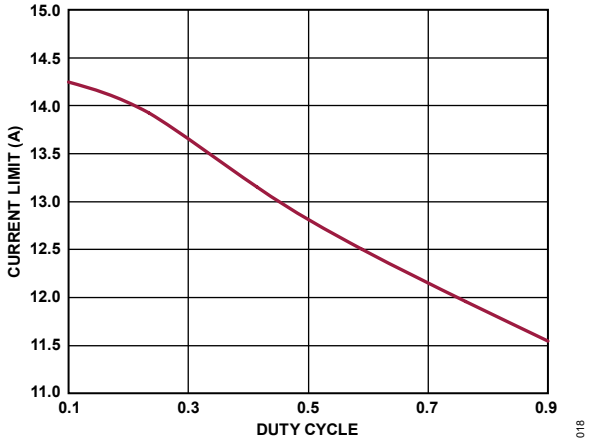


Figure 18. Top FET Current Limit vs. Duty Cycle

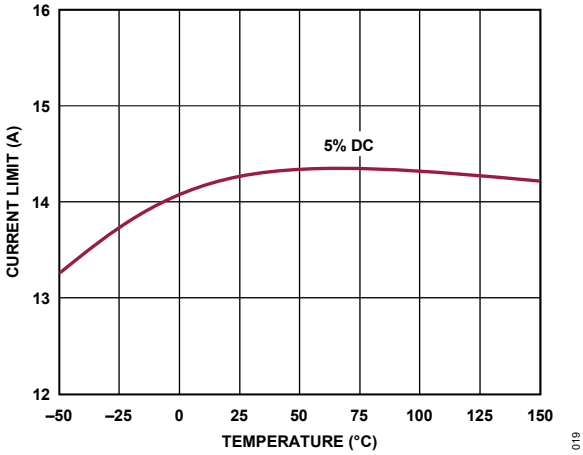


Figure 19. Top FET Current Limit

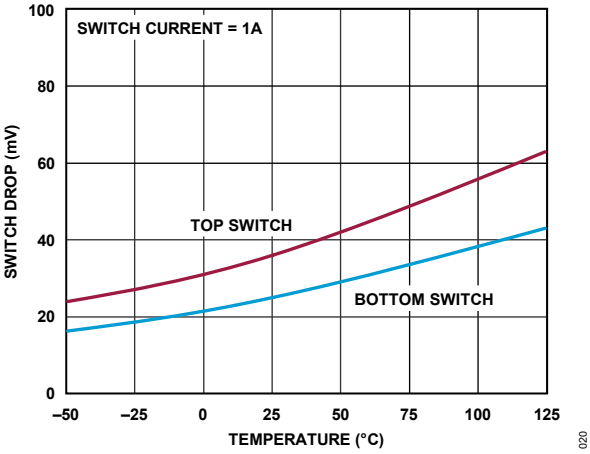


Figure 20. Switch Drop vs. Temperature

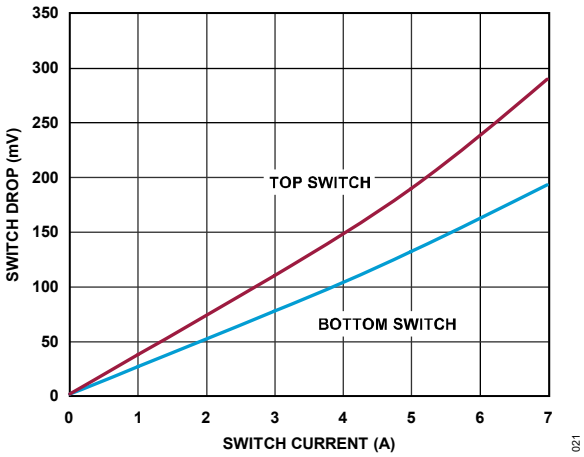


Figure 21. Switch Drop vs. Switch Current

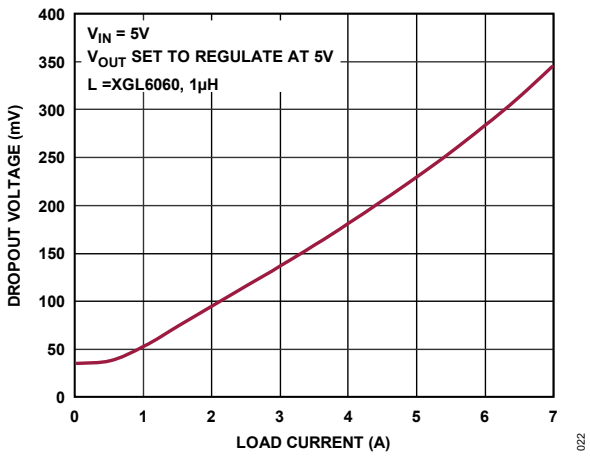


Figure 22. Dropout Voltage

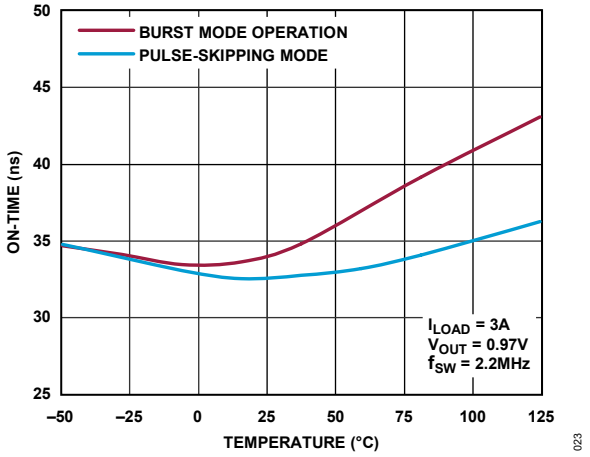


Figure 23. Minimum On-Time

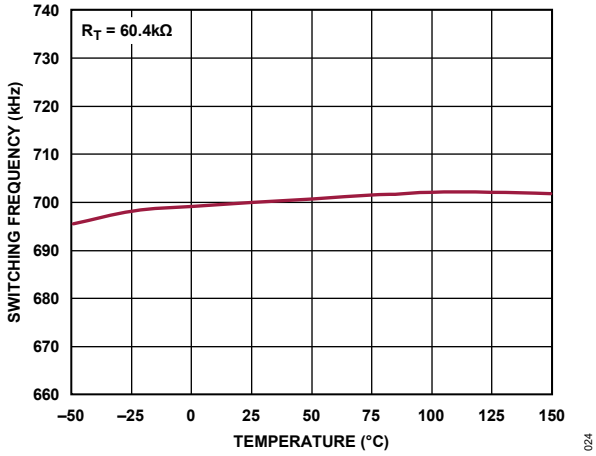


Figure 24. Switching Frequency

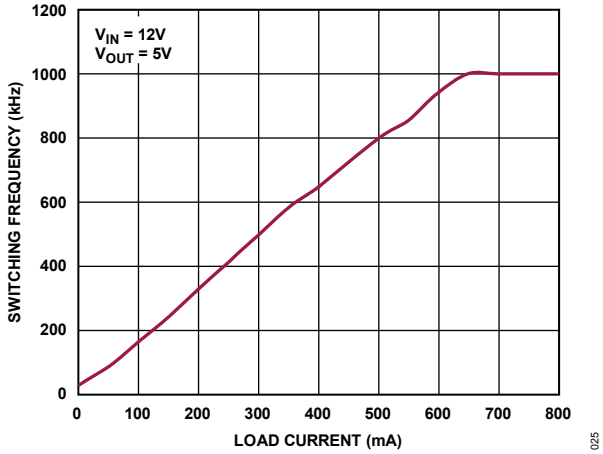


Figure 25. Burst Frequency, See Typical Application

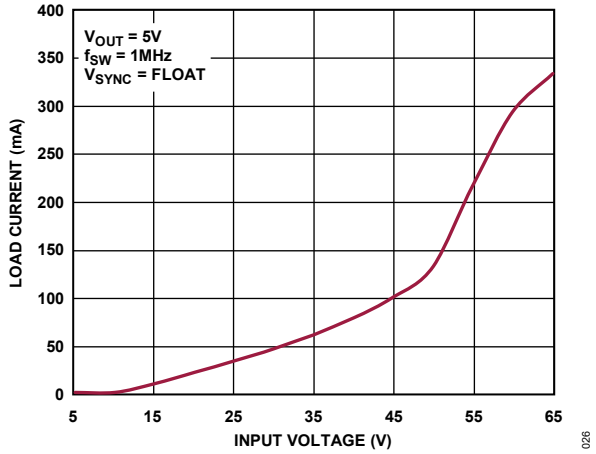


Figure 26. Minimum Load to Full-Frequency (Pulse-Skipping Mode), See Typical Application

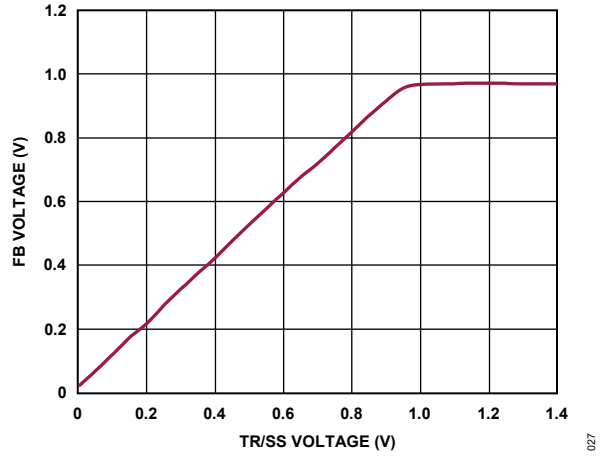


Figure 27. Soft-Start Tracking

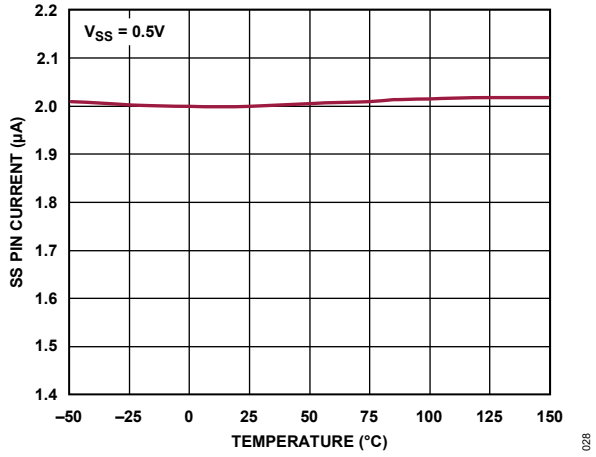


Figure 28. Soft-Start Current

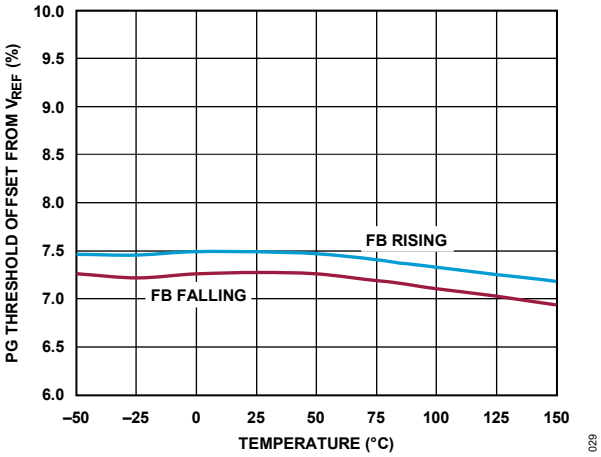


Figure 29. PG High Thresholds

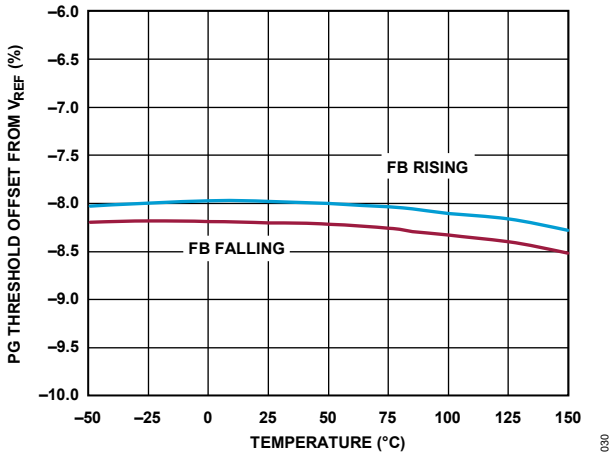


Figure 30. PG Low Thresholds

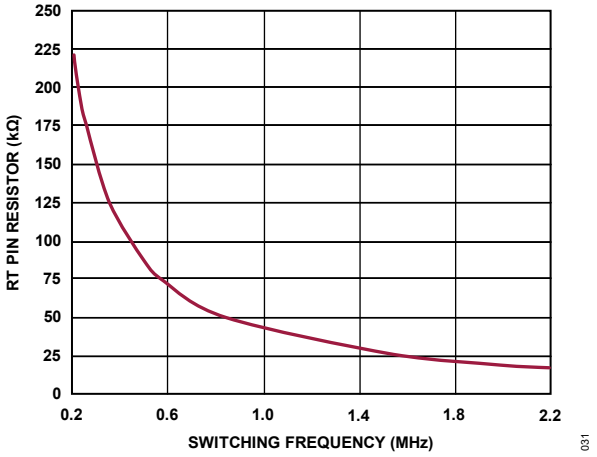


Figure 31. RT Programmed Switching Frequency

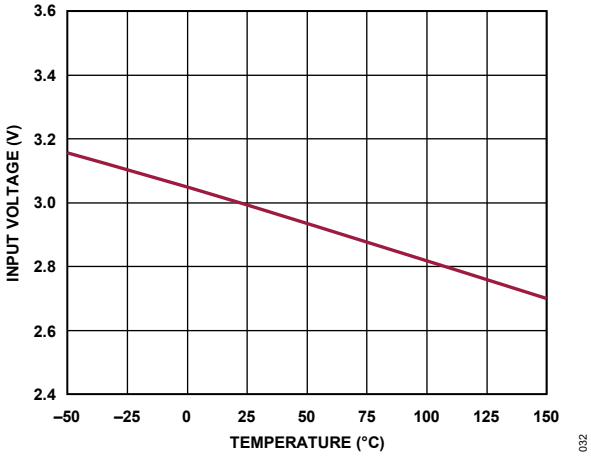


Figure 32. Minimum Input Voltage

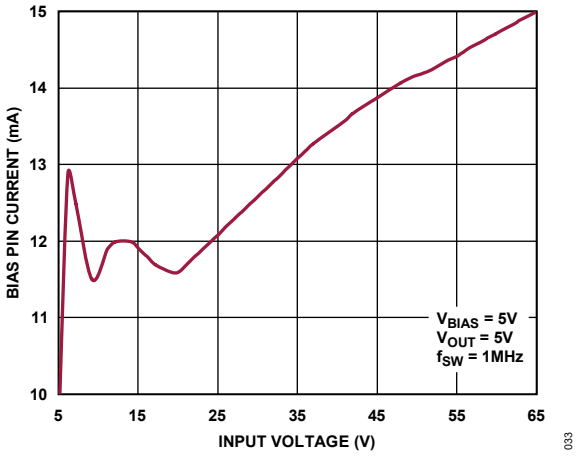


Figure 33. Bias Pin Current

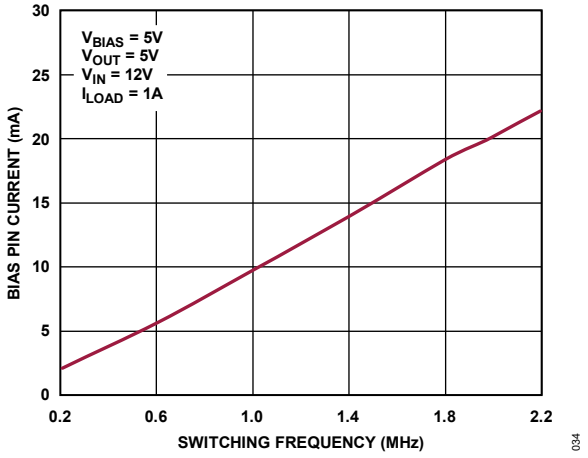


Figure 34. Bias Pin Current

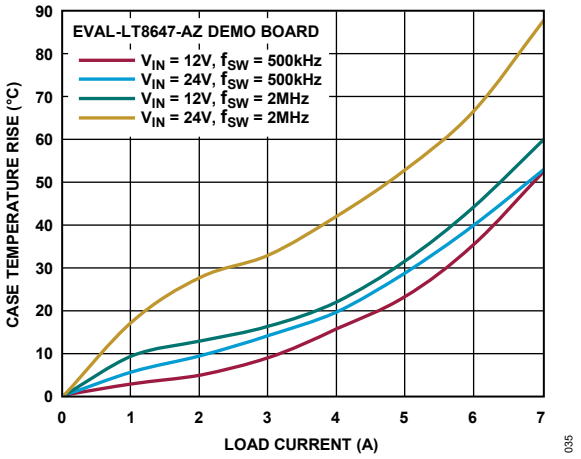


Figure 35. Case Temperature Rise (Refer to the EVAL-LT8647-AZ demo board)

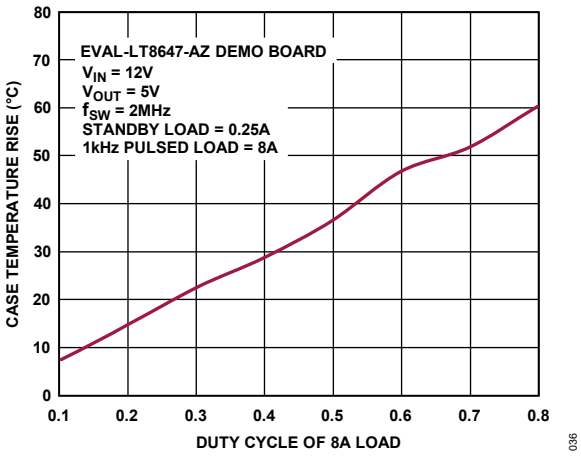


Figure 36. Case Temperature Rise vs. 8A Pulsed Load (Refer to the EVAL-LT8647-AZ demo board)

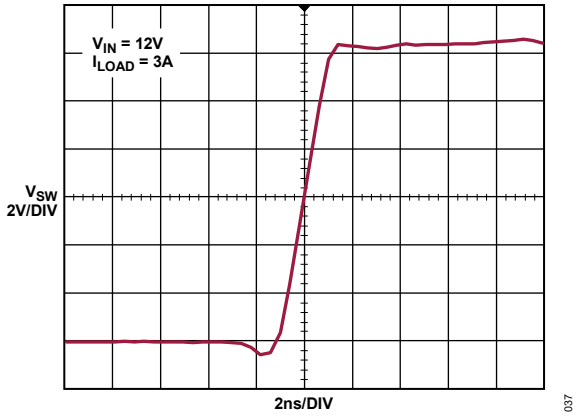


Figure 37. Switch Rising Edge

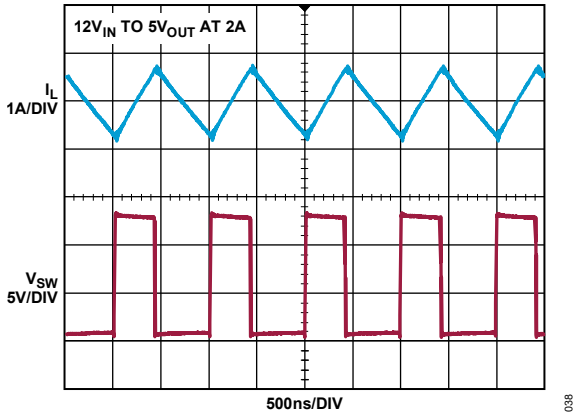


Figure 38. Switching Waveforms, Full-Frequency Continuous Operation (See Typical Application)

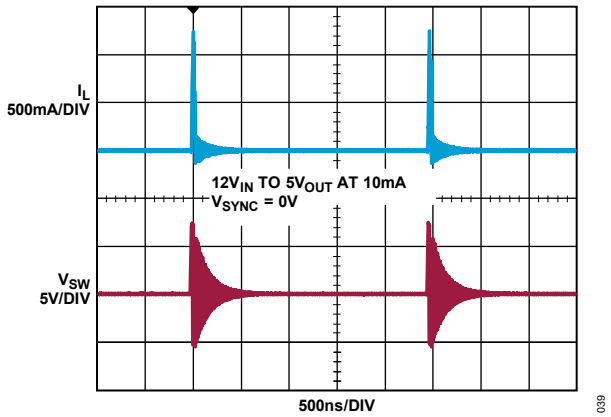


Figure 39. Switching Waveforms, Burst Mode Operation (See Typical Application)

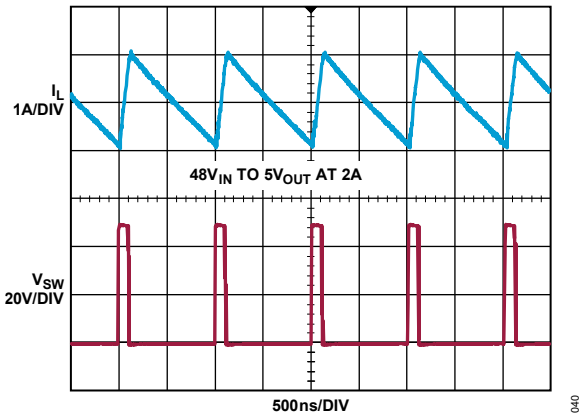


Figure 40. Switching Waveforms (See Typical Application)

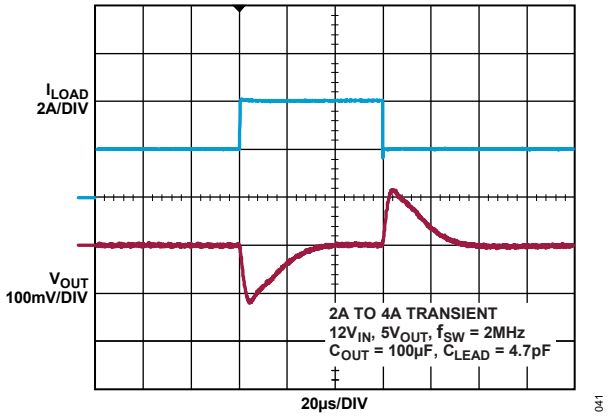


Figure 41. Transient Response; Internal Compensation

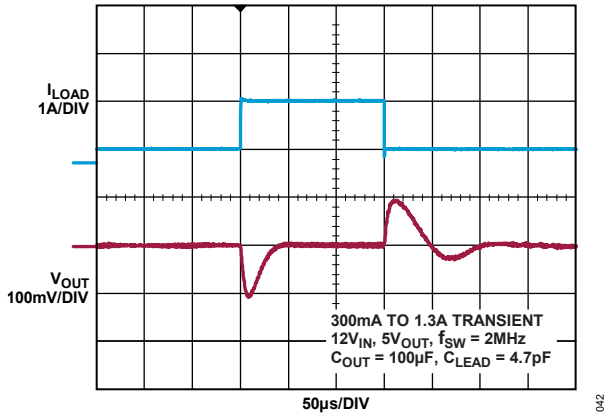


Figure 42. Transient Response: 300mA (Burst Mode Operation) to 1.3A Transient

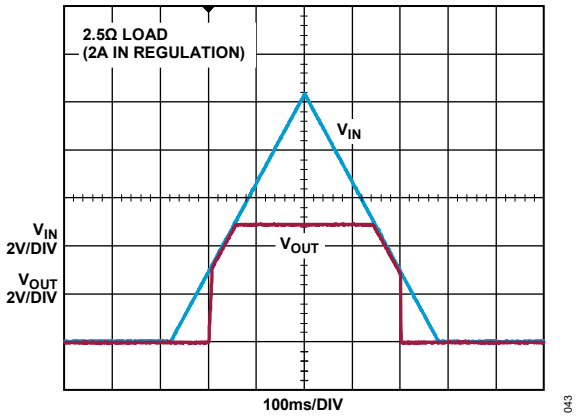


Figure 43. Start-Up Dropout Performance

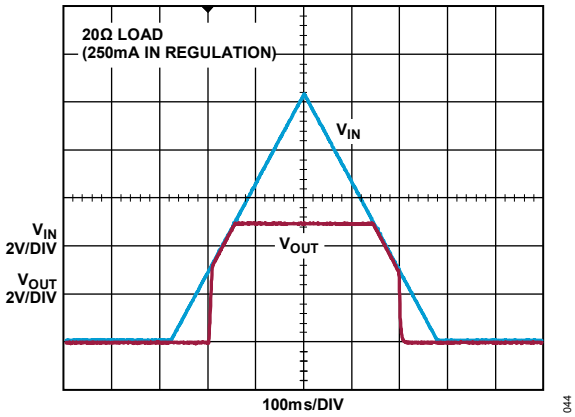


Figure 44. Start-Up Dropout Performance

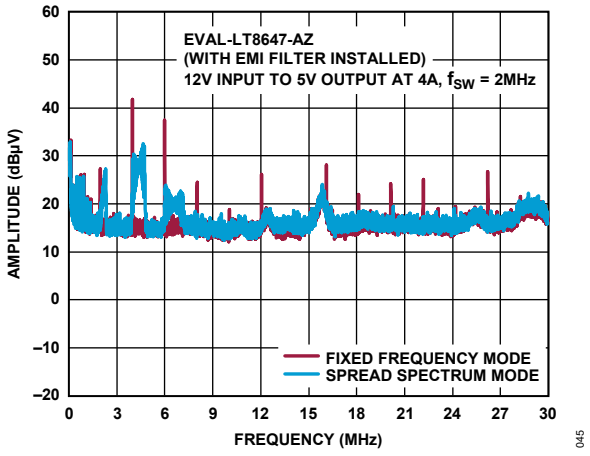


Figure 45. Conducted EMI Performance (Refer to the EVAL-LT8647-AZ demo board)

Radiated EMI Performance
(CISPR32 Radiated Emission Test with Class B Limits)
(Refer to the EVAL-LT8647-AZ demo board)

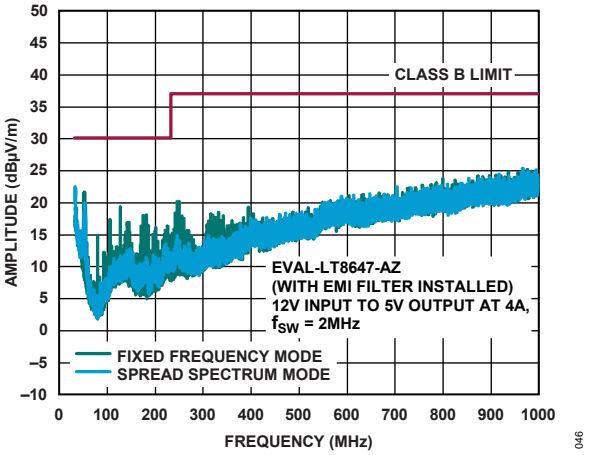


Figure 46. Radiated EMI Performance with EMI Filter

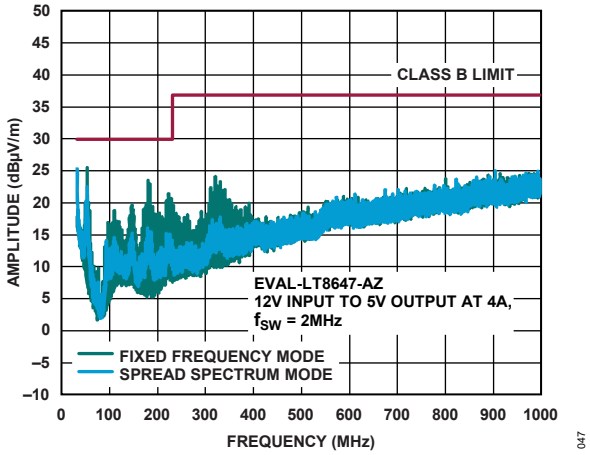


Figure 47. Radiated EMI Performance without EMI Filter

THEORY OF OPERATION

The LT8647 is a monolithic, constant-frequency, current-mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The voltage on the internal V_C node controls the peak inductor current at which the top switch turns off. The error amplifier servos the V_C node by comparing the voltage on the FB pin with an internal 0.97V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference, leading the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or the inductor current falls to zero. If overload conditions result in more than 11A flowing through the bottom switch, the next clock cycle will be delayed until the switch current returns to a safe level.

If the EN/UV pin is low, the LT8647 is shut down and draws approximately 1µA from the input. When the EN/UV pin is above 1.01V, the switching regulator becomes active.

To optimize efficiency at light loads, the LT8647 operates in Burst Mode when operating under light load conditions. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7µA. In a typical application, 2.5µA will be consumed from the input supply when regulating with no load. The SYNC/MODE pin is tied low to enable Burst Mode operation and can be left floating to use pulse-skipping mode. If a clock is applied to the SYNC/MODE pin, the part will synchronize to an external clock frequency and operate in pulse-skipping mode. While in pulse-skipping mode, the oscillator operates continuously, and positive SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output, resulting in a quiescent current of several hundred µA.

To improve EMI, the LT8647 can operate in spread spectrum mode. This feature varies the clock with a triangular frequency modulation of +20%. For example, if the LT8647's frequency is programmed to switch at 2MHz, spread spectrum mode will modulate the oscillator between 2MHz and 2.4MHz. The SYNC/MODE pin should be tied high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V to enable spread spectrum modulation in pulse-skipping mode.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased at 3.3V or above. Otherwise, the internal circuitry will draw current from V_{IN}. The BIAS pin should be connected to V_{OUT} if the LT8647 output is programmed at 3.3V to 25V.

Comparators monitoring the FB pin voltage will pull the PG pin low if the output voltage varies more than ±8% (typical) from the set point or if a fault condition is present.

The oscillator reduces the LT8647's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value, which occurs during start-up or overcurrent conditions. When a clock is applied to the SYNC/MODE pin, the SYNC/MODE pin is floated or held DC high, the frequency foldback is disabled, and the switching frequency will slow down only during overcurrent conditions.

APPLICATIONS INFORMATION

Low EMI Printed Circuit Board (PCB) Layout

The LT8647 is specifically designed to minimize EMI emissions and also to maximize efficiency when switching at high frequencies. For optimal performance, the LT8647 should use multiple V_{IN} bypass capacitors.

Two small 0.47µF capacitors can be placed as close as possible to the LT8647, one on each side of the device (C_{IN1} and C_{IN2}). A third capacitor with a larger value, 4.7µF or higher, should be placed near C_{IN1} or C_{IN2}.

See *Figure 48* for the recommended PCB layouts.

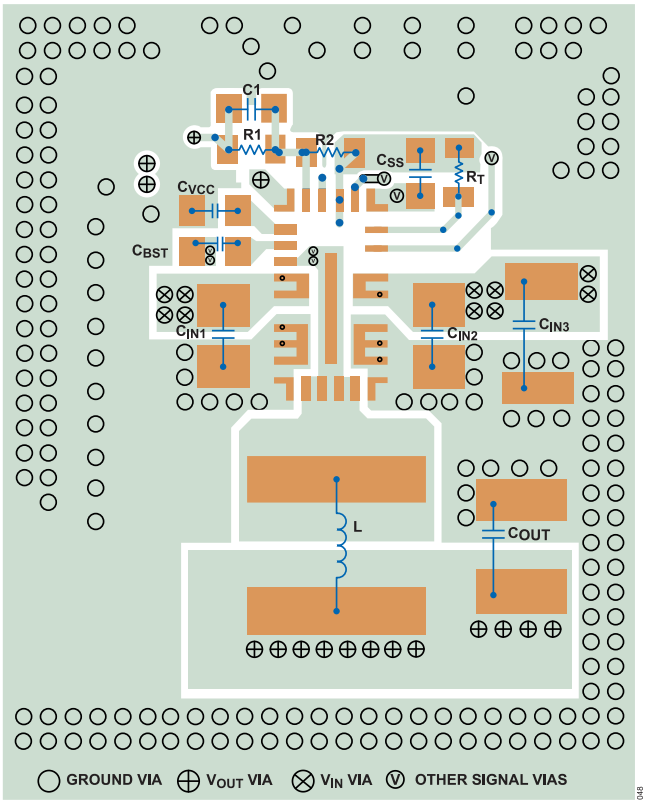


Figure 48. Recommended PCB Layouts for the LT8647

For more details and PCB design files, refer to the **EVAL-LT8647-AZ**.

Note: Large, switched currents flow in the LT8647 V_{IN} and GND pins and the input capacitors. The loops formed by the input capacitors should be minimized by placing the capacitors adjacent to the V_{IN} and GND pins. Capacitors with small case sizes, such as 0603 or 0805, are optimal due to the lowest parasitic inductance.

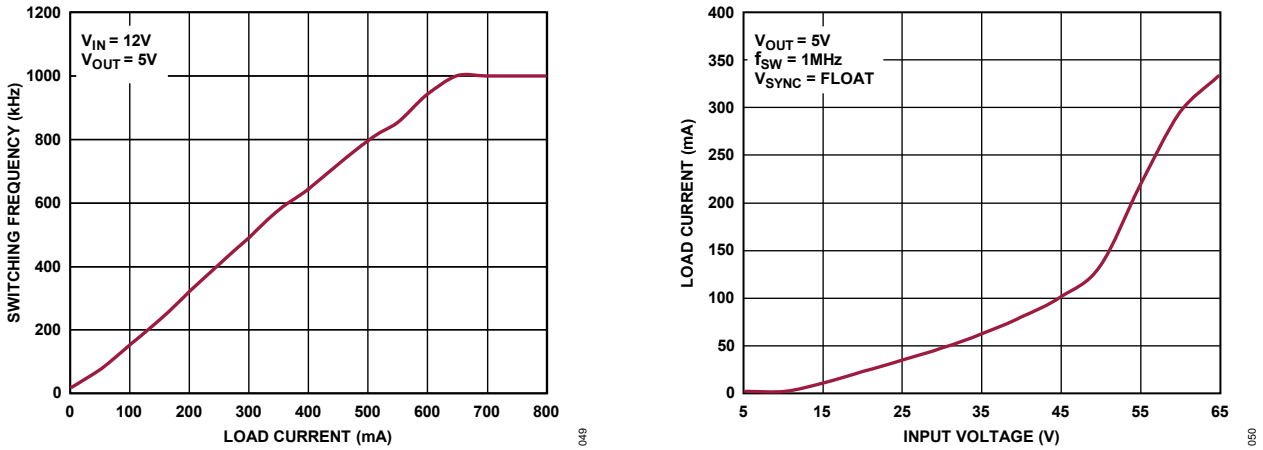
The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes.

The exposed pad at the bottom of the package should be soldered to the PCB to reduce thermal resistance. To keep thermal resistance low, extend the ground plane from the GND pins as much as possible and add thermal vias to additional ground planes within the circuit board and on the bottom side.

Burst Mode Operation

To enhance efficiency at light loads, the LT8647 operates in low-ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. In Burst Mode operation, the LT8647 delivers single small pulses of current to the output capacitor, followed by sleep periods during which the output power is supplied by the output capacitor. While in sleep mode, the LT8647 consumes 1.7µA.

As the output load decreases, the frequency of single current pulses decreases, see *Figure 49 (a)*, and the percentage of time the LT8647 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the LT8647's quiescent current approaches 2.5µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.



(a) Burst Frequency

(b) Minimum Load to Full-Frequency (Pulse-Skipping Mode)

Figure 49. SW Frequency vs Load Information in Burst Mode Operation (2a) and Pulse-Skipping Mode (2b). See Typical Application for more details.

To achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in the Burst mode operation, such that the LT8647 can stay in sleep mode for a longer period between each pulse. This can be achieved by using a larger inductor value and should be considered independent of the switching frequency when choosing an inductor. For example, a lower inductor value would typically be used for a high-switching frequency application. If high light load efficiency is desired, a higher inductor value should be chosen. See *Figure 12* in the *Typical Performance Characteristics* section.

While in Burst Mode operation, the current limit of the top switch is approximately 1.25A (see *Figure 50*), resulting in a low output voltage ripple. Increasing the output capacitance will decrease the output ripple proportionally. As the load ramps upward from zero, the switching frequency will increase, but only up to the switching frequency programmed by the resistor at the RT pin as shown in *Figure 49 (a)*.

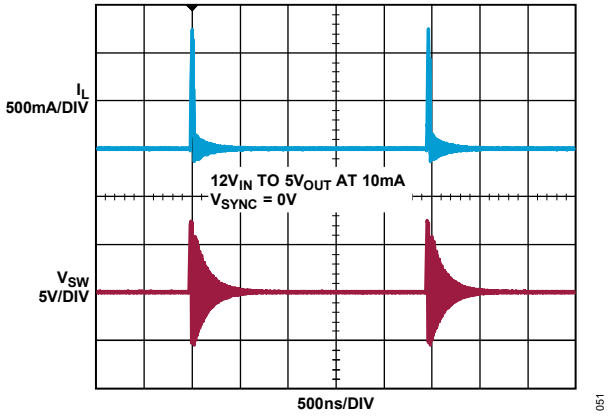


Figure 50. Burst Mode Operation, (See Typical Application for more details)

The output load at which the LT8647 reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice. To select low-ripple Burst Mode operation, tie the SYNC/MODE pin to a voltage below 0.4V (this can be ground or a logic low output).

Pulse-Skipping Mode

For certain applications, it is desirable for the LT8647 to operate in pulse-skipping mode, which offers two major differences from the Burst Mode operation. First, the clock remains active at all times, and all switching cycles are synchronized to the clock. In this mode, much of the internal circuitry is awake at all times, increasing quiescent current to several hundred µA. Second, the full switching frequency is reached at a lower output load than in the Burst Mode operation, as shown in *Figure 49 (b)*. To enable pulse-skipping mode, float the SYNC/MODE pin. The leakage current in this pin should be <1µA. See *Figure 4* (Block Diagram) for more details on internal pull-up and pull-down resistance.

Spread Spectrum Mode

The LT8647 features spread spectrum operation to further reduce EMI emissions. To enable spread spectrum operation, the SYNC/MODE pin should be tied high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by RT to approximately 20% higher than that value. The modulation frequency is approximately 3kHz. For example, when the LT8647 is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 3kHz rate. When Spread-Spectrum operation is selected, the Burst Mode operation is disabled, and the part will run in Pulse-Skipping mode.

Synchronization

To synchronize the LT8647 oscillator to an external frequency, connect a square wave to the SYNC/MODE pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

The LT8647 will not enter the Burst Mode operation at low output loads, while synchronized to an external clock, but instead will pulse-skip to maintain regulation. The LT8647 may be synchronized over a 200kHz to 2.2MHz range. The RT resistor should be chosen to set the LT8647 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal is 500kHz or higher, the RT should be selected for 500kHz. The slope compensation is set by the RT value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency does not change the slopes of the inductor current waveform, if the inductor is large enough to prevent subharmonic oscillations at the frequency set by RT, then the slope compensation will be sufficient for all synchronization frequencies.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to the following equation:

$$R1 = R2\left(\frac{V_{OUT}}{0.97V} - 1\right) \quad (1)$$

See *Figure 4* (Block Diagram) for the Reference designators. 1% resistors are recommended to maintain output voltage accuracy.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no-load input current to the converter, which is approximately:

$$I_Q = 1.7\mu A + \left(\frac{V_{OUT}}{R1+R2}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{n}\right) \quad (2)$$

where 1.7µA is the quiescent current of the LT8647, and the second term is the current in the feedback divider reflected to the input of the buck operating at its light load efficiency n. For a 3.3V application with R1 = 1MΩ and R2 = 412kΩ, the feedback divider draws 2.3µA. With V_{IN} = 12V and n = 80%, this adds 0.8µA to the 1.7µA quiescent current, resulting in 2.5µA no-load current from the 12V supply. Note that this equation implies that the no-load current is a function of V_{IN}. See *Figure 17* in the *Typical Performance Characteristics* section.

When using large FB resistors, a 1pF to 10pF phase-lead capacitor should be connected from V_{OUT} to FB.

High V_{OUT} Considerations

In applications where the output voltage is higher than 10V, refer to the *Reverse Current Considerations* section in **Application Note AN-2582**. For more details.

Setting the Switching Frequency

The LT8647 employs a constant-frequency PWM architecture that can be programmed to switch between 200kHz and 2.2MHz by using a resistor tied from the RT pin to ground. *Table 7* shows the required R_T value for the desired switching frequency.

Table 7. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	71.5
0.7	60.4
0.8	52.3
1.0	41.2
1.2	33.2
1.4	28.0
1.6	23.7

f_{SW} (MHz)	R_T (kΩ)
1.8	20.5
2.0	17.8
2.2	15.8

The R_T resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{46.5}{f_{SW}} - 5.2 \quad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

Operating Frequency Selection and Trade-Offs

The selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high-frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated using the following equation:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)})} \quad (4)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.2V, respectively, at maximum load), and $t_{ON(MIN)}$ is the minimum top switch on-time as shown in the *Table 1* (Electrical Characteristics table). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may reach the absolute maximum rating of 65V regardless of the R_T value. However, the LT8647 will reduce the switching frequency, as needed, to maintain control of the inductor current and ensure safe operation.

The LT8647 is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode, the LT8647 skips switch cycles, resulting in a lower switching frequency than programmed by the RT pin.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios, use the following formula to set the switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \times t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (5)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.2V, respectively at maximum load), f_{SW} is the switching frequency (set by RT), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that a higher switching frequency will increase the minimum input voltage, below which cycles will be dropped to achieve a higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8647 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions, the LT8647 safely tolerates operation with a saturated inductor using a high-speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L = \left(\frac{V_{OUT}+V_{SW(BOT)}}{f_{SW}}\right)\times 0.4 \quad (6)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.2V), and L is the inductor value in µH.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus half of the inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (7)$$

where ΔI_L is the inductor ripple current as calculated as shown in *Equation 9*, and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 2A output should use an inductor with an RMS rating of greater than 2A and an I_{SAT} of greater than 3A. During long-duration overload or short-circuit conditions, the inductor's RMS rating requirement is greater to avoid overheating of the inductor. To maintain high efficiency, the series resistance (DCR) should be less than 0.02Ω, and the core material should be suitable for high-frequency applications.

The LT8647 limits the peak switch current to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 14A at low-duty cycles and decreases linearly to 11.5A at DC = 0.9. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (8)$$

The peak-to-peak ripple current in the inductor can be calculated using the following equation:

$$\Delta I_L = \frac{V_{OUT}}{L\times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (9)$$

where f_{SW} is the switching frequency of the LT8647, and L is the value of the inductor. Therefore, the maximum output current that the LT8647 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may need to be increased if the ripple current limits the maximum output current ($I_{OUT(MAX)}$), given the switching frequency and maximum input voltage used in the desired application.

When operating at high V_{IN} (greater than 40V), a frequency and duty cycle that require a switch on-time of less than 100ns, select an inductor such that the ΔI_L is greater than 1.5A to prevent duty cycle jitter.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the inductor value may be lowered, allowing the LT8647 to operate with a higher ripple current. This allows the use of a physically smaller inductor, or one with a lower DCR, resulting in higher efficiency.

Be aware that low inductance may result in discontinuous mode operation, which further reduces the maximum load current.

For more information about maximum output current and discontinuous operation, refer to **Analog Devices' Application Note 44** for more details.

For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillation (See Equation 10). Refer to **Analog Devices' Application Note 19** for more details.

$$L_{MIN} = \frac{V_{IN}(2 \times DC\text{-}1)}{3 \times f_{SW}} \quad (10)$$

where DC is the duty cycle ratio (V_{OUT}/V_{IN}), and f_{SW} is the switching frequency.

Input Capacitor

The V_{IN} of the LT8647 should be bypassed with at least three ceramic capacitors for best performance. Two small ceramic capacitors, each with a value of 0.47µF, should be placed close to the part, one on each side of the device (CIN1 and CIN2). These capacitors should be 0603 or 0805 in size. For automotive applications requiring two series input capacitors, two small 0603 or 0805 capacitors may be placed on each side of the LT8647.

A third, larger ceramic capacitor of 4.7µF or larger should be placed close to C_{IN1} or C_{IN2}. See the *Low EMI Printed Circuit Board (PCB) Layout* for more details. X7R or X5R capacitors are recommended for best performance across a wide range of temperature and input voltage.

Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low-performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high-quality (underdamped) tank circuit. If the LT8647 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8647's voltage rating. This situation is easily avoided (refer to **Analog Devices Application Note 88** for more details).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8647 to produce the DC output. In this role, it determines the output ripple; thus, low impedance at the switching frequency is important. The second function is to store energy to satisfy transient loads and stabilize the LT8647's control loop. Ceramic capacitors have very low Equivalent series resistance (ESR) and provide the best ripple performance. See the *Typical Application Circuits* section for recommended starting values.

Use X5R or X7R types. This choice will provide a low output ripple and good transient response. Transient performance can be improved by using a higher value output capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of the output capacitor can be used to save space and cost, but transient performance will suffer, potentially causing loop instability. See the *Typical Application Circuits* section for recommended capacitor values.

When selecting a capacitor, special attention should be given to the datasheet to calculate the effective capacitance under the relevant operating conditions, including voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

The ceramic capacitors are small, robust, and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8647 due to their piezoelectric nature. In a Burst Mode operation, the LT8647's switching frequency depends on the load current. At very light loads, the LT8647 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8647 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high-performance tantalum or electrolytic capacitor at the output. Low-noise ceramic capacitors are also available.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8647. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high-quality (underdamped) tank circuit. If the LT8647 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8647's rating. This situation is easily avoided (Refer to **Analog Devices' Application Note 88** for more details).

Enable Pin

The LT8647 is in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 1.01V, with 45mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN programs the LT8647 to regulate the output only when V_{IN} is above a desired voltage. See *Figure 4* (Block Diagram) for more details. Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws constant power from the source, so the source current increases as the source voltage drops. This appears to be a negative resistance load to the source, which can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = \left(\frac{R3}{R4} + 1\right) \times 1.01V \quad (11)$$

where the LT8647 will remain off until the V_{IN} exceeds $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below the $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily exceed the supply current consumed by the LT8647. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low-dropout (LDO) regulator generates the 3.4V supply from V_{IN}, which powers the drivers and the internal bias circuitry and must be bypassed to ground with a minimum of 1µF ceramic capacitor. The $INTV_{CC}$ can supply enough current for the LT8647's circuitry. To improve efficiency, the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically, the BIAS pin can be tied to the output of the LT8647 or can be tied to an external supply of 3.3V or above. If BIAS is connected to a supply other than V_{OUT}, ensure that it is bypassed with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN}. Applications with high input voltage and high switching frequency, where the internal LDO pulls current from V_{IN}, will increase die temperature due to higher power dissipation across the LDO. Note: Do not connect an external load to the $INTV_{CC}$ pin.

Output Voltage Tracking and Soft-Start

The LT8647 allows the user to program its output voltage ramp rate via the TR/SS pin. An internal 2µA pulls up the TR/SS pin to $INTV_{CC}$. Placing an external capacitor on TR/SS allows soft starting the output, preventing a current surge on the input supply. During the soft-start ramp, the output voltage will proportionally track the TR/SS pin voltage.

For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.97V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier. Thus, regulating the FB pin voltage to that of the TR/SS pin. When TR/SS exceeds 0.97V, tracking is disabled, and the feedback voltage is regulated to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TR/SS pin, which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor include the EN/UV pin transitioning low, the V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8647's output voltage is within the ±8% window of the regulation point, the output voltage is considered good, and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching, both the upper and lower thresholds include a 0.4% hysteresis. PG is valid when V_{IN} is above 3.4V.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown.

Shorted and Reversed Input Protection

The LT8647 will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. First, the switching frequency is folded back when the output is lower than the set point, maintaining inductor current control. Second, the bottom switch current is monitored, such that if the inductor current exceeds safe levels, the switching of the top switch is delayed until the inductor current falls to safe levels.

Frequency foldback behavior depends on the state of the SYNC pin: If the SYNC pin is low, the switching frequency will slow while the output voltage is lower than the programmed level. If the SYNC pin is connected to a clock source, floated, or tied high, the LT8647 will stay at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

There is another situation to consider in systems where the output remains high when the input to the LT8647 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode-ORed with the LT8647's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8647's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN pin is grounded, the SW pin current will drop to approximately 1µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of the EN pin, parasitic body diodes inside the LT8647 can pull current from the output through the SW pin and the V_{IN} pin. *Figure 51* illustrates the connection of the V_{IN} and EN/UV pins, which enables the LT8647 to run only when the input voltage is present and protects against a shorted or reversed input.

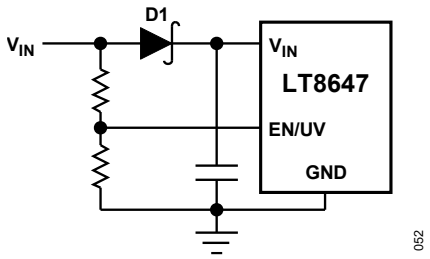


Figure 51. Reverse V_{IN} Protection

Thermal Considerations and Peak Output Current

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8647. The ground pins on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will dissipate heat from the LT8647. Placing additional vias can further reduce thermal resistance. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8647 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8647 power dissipation by the thermal resistance from junction to ambient.

The internal overtemperature protection monitors the junction temperature of the LT8647. If the junction temperature reaches approximately 180°C, the LT8647 will stop switching and indicate a fault condition until the temperature drops about 10°C cooler.

The temperature rise of the LT8647 is worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level. *Figure 52* shows examples of how case temperature rise can be managed by reducing V_{IN}, switching frequency, or load.

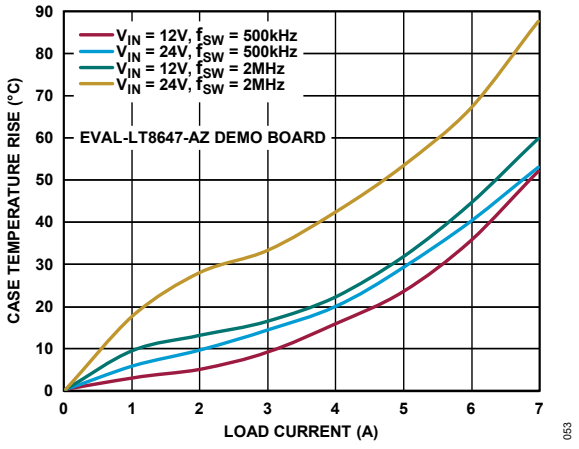


Figure 52. Case Temperature Rise (Refer to the EVAL-LT8647-AZ demo board)

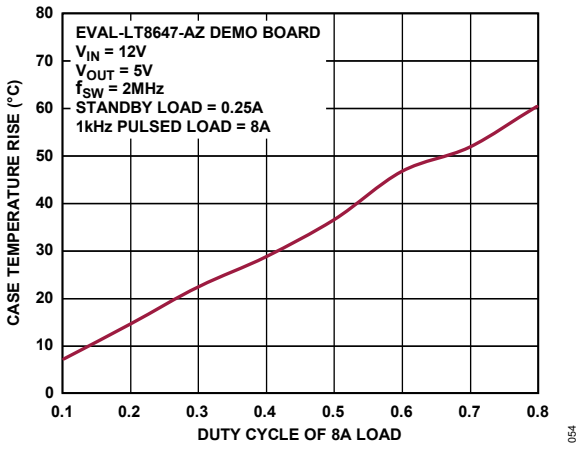


Figure 53. Case Temperature Rise vs. 8A Pulsed Load (Refer to the EVAL-LT8647-AZ demo board)

The LT8647's internal power switches are capable of safely delivering up to 8A of peak output current. However, due to thermal limitations, the package can only handle 8A loads for short periods. This time is determined by how quickly the case temperature approaches the maximum junction rating. *Figure 53* illustrates an example of how the case temperature rise varies with the duty cycle of a 1kHz pulsed 8A load.

The LT8647's top switch current limit decreases with higher duty cycle operation for slope compensation. This also limits the output current the LT8647 can deliver for a given application. See *Figure 18* in the *Typical Performance Characteristics* section.

TYPICAL APPLICATION CIRCUITS

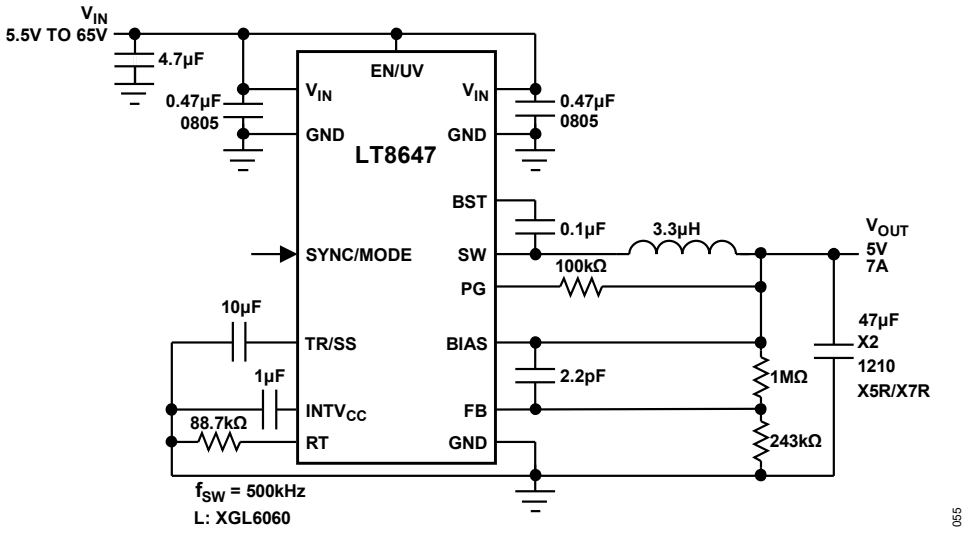


Figure 54. 5V, 7A Step-Down Converter with Soft-Start and Power Good

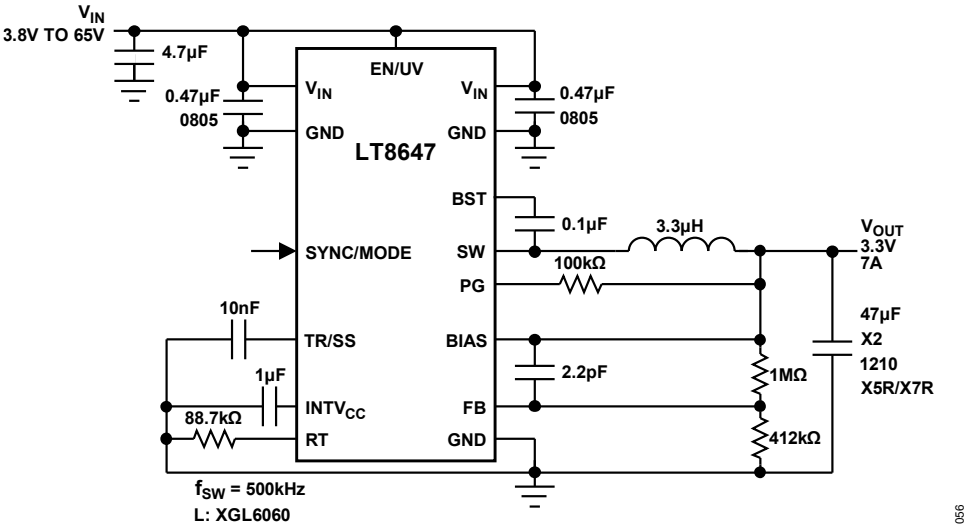


Figure 55. 3.3V, 7A Step-Down Converter with Soft-Start and Power Good

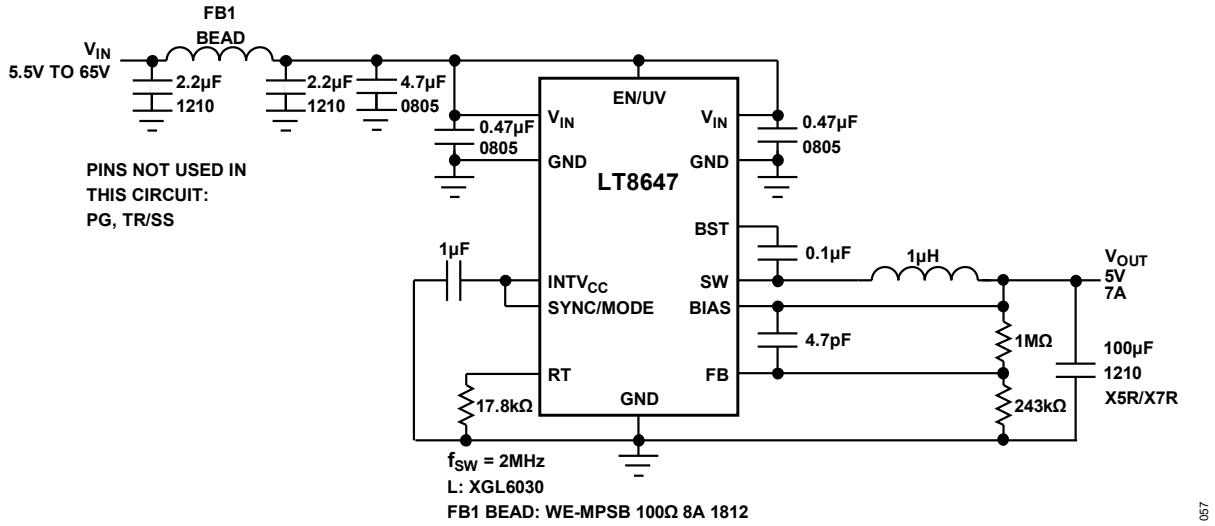


Figure 56. Ultralow EMI 5V, 7A Step-Down Converter with Spread Spectrum

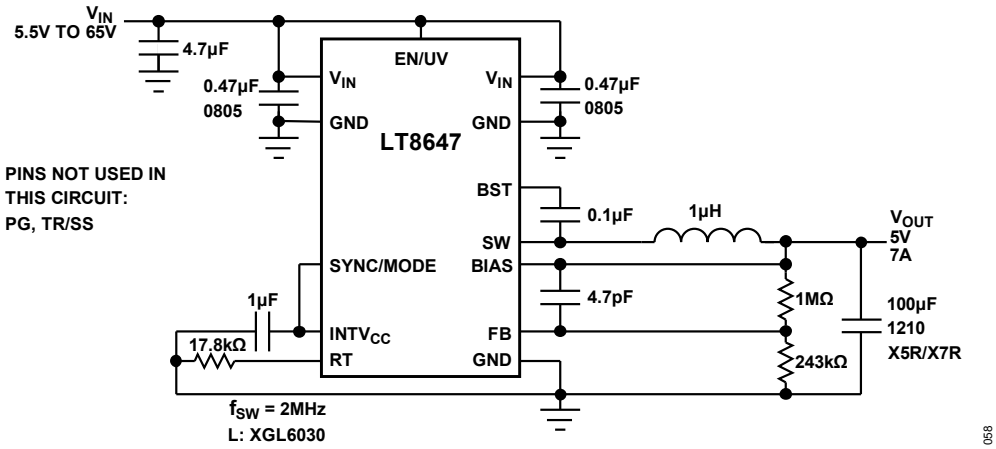


Figure 57. 2MHz, 5V, 7A Step-Down Converter with Spread Spectrum

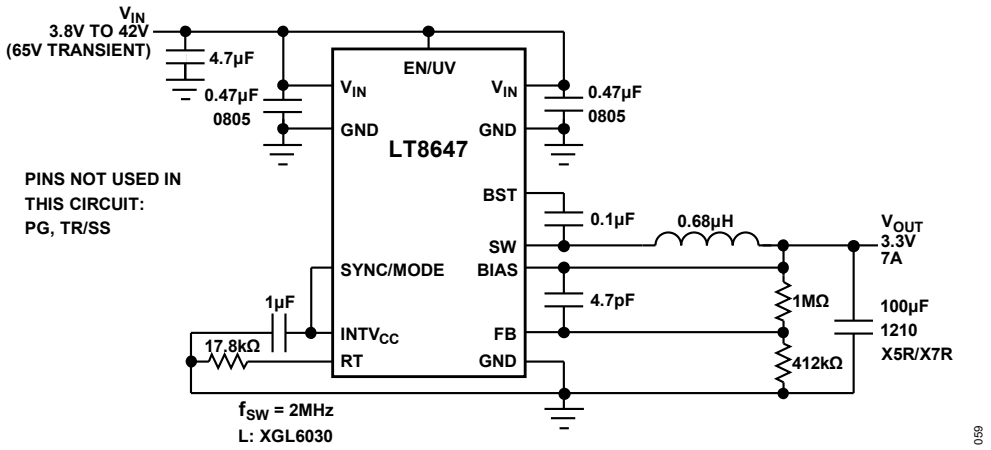


Figure 58. 2MHz, 3.3V, 7A Step-Down Converter with Spread Spectrum

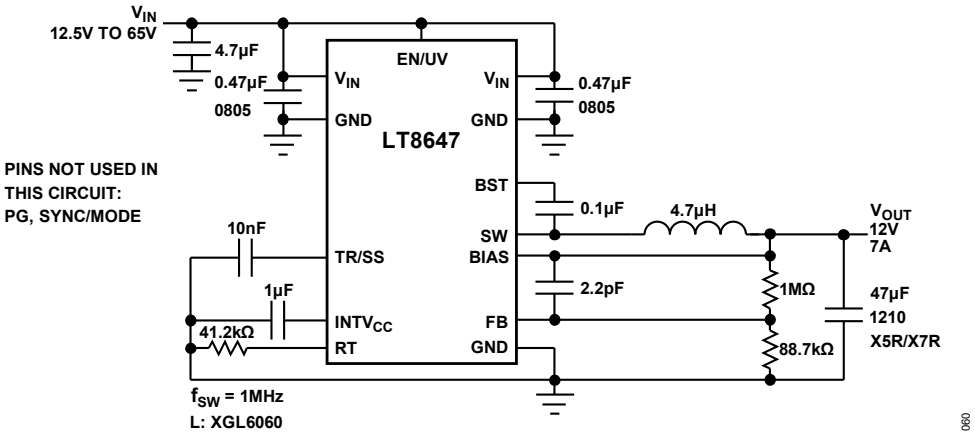


Figure 59. 12V, 7A Step-Down Converter

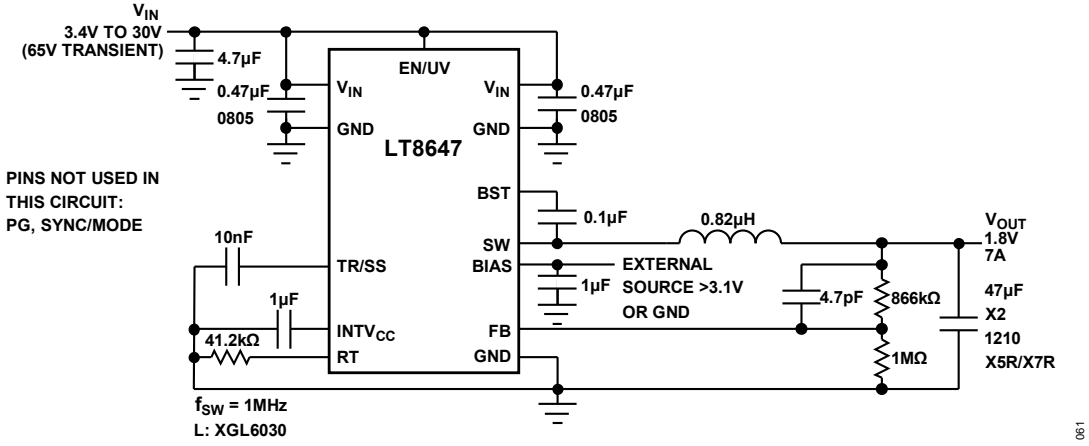


Figure 60. 1.8V, 7A Step-Down Converter

ORDERING GUIDE

Table 8. Ordering Guide

PART NUMBER	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8647RCPZ-RL	8647	27-Lead (3mm x 6mm) FC2QFN Package	-40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges.

*The temperature grade is identified by a label on the shipping container.