Data Sheet

ADRF5702

Silicon Digital Attenuator, 0.125dB LSB, 8-Bit, 50MHz to 20GHz

FEATURES

- Frequency range: 50MHz to 20GHz
- Attenuation range: 31.875dB with 0.125dB step size
- Low insertion loss
  - 1.4dB typical up to 6GHz (5V supply)
  - 1.8dB typical up to 12GHz (5V supply)
  - 2.6dB typical up to 20GHz (5V supply)
- Attenuation accuracy: −(0.1 + 2.0% of attenuation state) typical up to 20GHz
- Step error: −0.30dB typical up to 20GHz (5V supply)
- High linearity
  - Input P0.1dB
    - Attenuation state < 8dB: 32dBm typical (5V supply)
    - Attenuation state ≥ 8dB: 29dBm typical (5V supply)
  - Input IP3
    - Attenuation state < 16dB): 55dBm typical (5V supply)
    - Attenuation state ≥ 16dB): 50dBm typical (5V supply)
- High RF power handling
  - 27dBm average (ATTIN)
  - 32dBm peak (5V supply, attenuation state < 8dB)
  - 29dBm peak (5V supply, attenuation state ≥ 8dB)
  - 27dBm hot switching
- RF amplitude settling time (50% triggered control to 0.05dB of final RF output): 140ns
- Consistent return loss at all attenuation states
- Single-supply operation: 5V or 3.3V
- No low frequency spurs, and no internal voltage generation
- Serial and parallel mode control, CMOS/LVTTL compatible
- 24-terminal, 4.0mm × 4.0mm, land grid array (LGA) package

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G millimeter wave
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

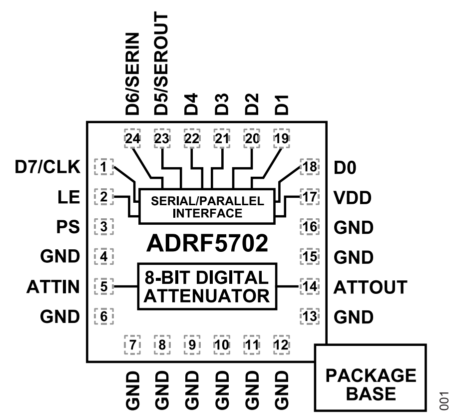

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5702 is a 8-bit digital attenuator with a 31.875dB attenuation range and 0.125dB step size manufactured in a silicon on insulator (SOI) process.

This device operates from 50MHz to 20GHz with an insertion loss lower than 2.6dB and excellent attenuation accuracy. The ADRF5702 has RF input power handling capabilities of 27dBm average and 29dBm peak for all states from the ATTIN pin.

The ADRF5702 requires a single-supply voltage of 5V or 3.3V. The device does not support supply intermediate supply voltage levels except values given in the Electrical Specifications section.

The device features serial or parallel mode control and complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5702 RF ports are designed to match a characteristic impedance of 50Ω.

The ADRF5702 comes in a 24-terminal, 4.0mm × 4.0mm, land grid array (LGA) package and can operate from −40°C to +105°C.

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

7/2025—Rev. 0 to Rev. A

6/2025—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 5V or 3.3V, control voltage (V_{CTRL}) = 0V or 3.3V, case temperature (T_{CASE}) = 25°C, and a 50Ω system, unless otherwise noted. V_{CTRL} is the voltages of the digital control input pins.

Table 1. 5V Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.05		20	GHz
INSERTION LOSS						
		50MHz to 6GHz		1.4		dB
		6GHz to 12GHz		1.8		dB
		12GHz to 20GHz		2.6		dB
RETURN LOSS		All attenuation states				
ATTIN						
		50MHz to 6GHz		19		dB
		6GHz to 12GHz		18		dB
		12GHz to 20GHz		16		dB
ATTOUT						
		50MHz to 6GHz		20		dB
		6GHz to 12GHz		20		dB
		12GHz to 20GHz		18		dB
ATTENUATION						
Range		Between minimum and maximum attenuation states		31.875		dB
Step Size		Between any successive attenuation states		0.125		dB
Accuracy		Referenced to insertion loss				
		50MHz to 20GHz		−(0.1 + 2.0% of state) or +(0.5% of state)		dB
Step Error		Between any successive state				
		50MHz to 6GHz		−0.20 or +0.05		dB
		6GHz to 12GHz		−0.30 or +0.05		dB
		12GHz to 20GHz		−0.30 or +0.10		dB
RELATIVE PHASE		Max attenuation state referenced to insertion loss				
		6GHz		20		Degrees
		12GHz		41		Degrees
		20GHz		70		Degrees

SPECIFICATIONS

Table 1. 5V Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS		All attenuation states at input power (P_{IN}) = 10dBm, f = 1GHz				
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		60		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% triggered control to 90% of RF output		100		ns
RF Amplitude Settling Time						
0.1dB		50% triggered control to 0.1dB of final RF output		120		ns
0.05dB		50% triggered control to 0.05dB of final RF output		140		ns
Overshoot		Worst-case transition		1.8		dB
Undershoot		Worst-case transition		2.5		dB
RF Phase Settling Time		f = 20GHz				
5°		50% triggered control to 5° of final RF output, f = 18GHz		92		ns
1°		50% triggered control to 1° of final RF output, f = 18GHz		100		ns
INPUT LINEARITY[1]		50MHz to 18GHz				
0.1dB Power Compression	P0.1dB					
		Attenuation state < 8dB		32		dBm
		Attenuation state ≥ 8dB		29		dBm
Third-Order Intercept	IP3	Two-tone P_{IN} = 14dBm per tone, Δf = 1MHz				
		Attenuation state < 16dB		55		dBm
		Attenuation state ≥ 16dB		50		dBm
Second-Order Intercept	IP2	Two-tone P_{IN} = 10dBm per tone, Δf = 1MHz				
		Attenuation state < 16dB		98		dBm
		Attenuation state ≥ 16dB		88		dBm
VIDEO FEEDTHROUGH[2]				2		mV p-p
DIGITAL CONTROL INPUTS		LE, PS, and D0 to D7				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		μA
High	I_{INH}			<1		μA
SUPPLY CURRENT						
Positive Supply Current	I_{DD}	VDD = 5V		3.50		mA
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage[3]	V_{DD}		4.75		5.25	V
Digital Control Voltage	V_{CTRL}		0		3.3	V
RF Power Handling[4]		f = 50MHz to 18GHz, T_{CASE} = 85°C[5], all attenuation states				
Input at ATTIN						
Average		All attenuation states			27	dBm
Peak[6]		Attenuation state < 8dB			32	dBm
		Attenuation state ≥ 8dB			29	dBm
Hot Switching		All attenuation states			27	dBm

SPECIFICATIONS

Table 1. 5V Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input at ATTOUT						
Average		Attenuation state < 8dB			27	dBm
		Attenuation state ≥ 8dB			24	dBm
Peak		Attenuation state < 8dB			32	dBm
		Attenuation state ≥ 8dB			29	dBm
Hot Switching		All attenuation states			24	dBm
Case Temperature	T_{CASE}		−40		105	°C

[1] For input linearity performance over frequency, see Figure 48 to Figure 49.

[2] Video feedthrough is peak transient measured at the RF ports in a 50Ω test setup, without an RF signal present while switching the control voltage.

[3] Device does not support intermediate supply voltage levels except those levels detailed in the Table 1.

[4] For RF power handling derating over the extended frequency range, see Figure 2.

[5] For T_{CASE} = 105°C operation, the RF power handling derates from the T_{CASE} = 85°C specifications by 3 dB.

[6] Peak: (≤100ns pulse duration, 5% duty cycle).

SPECIFICATIONS

Table 2. 3.3V Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.05		20	GHz
INSERTION LOSS						
		50MHz to 6GHz		1.5		dB
		6GHz to 12GHz		1.9		dB
		12GHz to 20GHz		2.7		dB
RETURN LOSS		All attenuation states				
ATTIN						
		50MHz to 6GHz		19		dB
		6GHz to 12GHz		18		dB
		12GHz to 20GHz		16		dB
ATTOUT						
		50MHz to 6GHz		20		dB
		6GHz to 12GHz		20		dB
		12GHz to 20GHz		18		dB
ATTENUATION						
Range		Between minimum and maximum attenuation states		31.875		dB
Step Size		Between any successive attenuation states		0.125		dB
Accuracy		Referenced to insertion loss				
		50MHz to 20GHz		−(0.1 + 1.0% of state) or +(0.5% of state)		dB
Step Error		Between any successive state				
		50MHz to 6GHz		−0.15 or +0.05		dB
		6GHz to 12GHz		−0.25 or +0.05		dB
		12GHz to 20GHz		−0.25 or +0.12		dB
RELATIVE PHASE		Referenced to insertion loss				
		6GHz		28		Degrees
		12GHz		46		Degrees
		20GHz		65		Degrees

SPECIFICATIONS

Table 2. 3.3V Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS		All attenuation states at input power (P_{IN}) = 10dBm, f = 1GHz				
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		65		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% triggered control to 90% of RF output		120		ns
RF Amplitude Settling Time						
0.1dB		50% triggered control to 0.1dB of final RF output		140		ns
0.05dB		50% triggered control to 0.05dB of final RF output		180		ns
Overshoot		Worst-case transition		1.8		dB
Undershoot		Worst-case transition		2.5		dB
RF Phase Settling Time		f = 20GHz				
5°		50% triggered control to 5° of final RF output		112		ns
1°		50% triggered control to 1° of final RF output		120		ns
INPUT LINEARITY[1]		50MHz to 18GHz				
0.1dB Power Compression	P0.1dB					
		Attenuation state < 8dB		30		dBm
		Attenuation state ≥ 8dB		27		dBm
Third-Order Intercept	IP3	Two-tone P_{IN} = 14dBm per tone, Δf = 1MHz				
		All attenuation states		50		dBm
Second-Order Intercept	IP2	Two-tone P_{IN} = 10dBm per tone, Δf = 1MHz				
		Attenuation state < 16dB		95		dBm
		Attenuation state ≥ 16dB		85		dBm
VIDEO FEEDTHROUGH[2]				2		mV p-p
DIGITAL CONTROL INPUTS		LE, PS, and D0 to D7				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		μA
High	I_{INH}			<1		μA
SUPPLY CURRENT						
Positive Supply Current	I_{DD}	VDD = 3.3V		1.75		mA
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage[3]	V_{DD}	Low power mode	3.15		3.45	V
Digital Control Voltage	V_{CTRL}		0		3.3	V
RF Power Handling[4]		f = 50MHz to 18GHz, T_{CASE} = 85°C[5], all attenuation states				
Input at ATTIN						
Average		All attenuation states			27	dBm
Peak[6]		Attenuation state < 8dB			30	dBm
		Attenuation state ≥ 8dB			27	dBm
Hot Switching		All attenuation states			27	dBm

SPECIFICATIONS

Table 2. 3.3V Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input at ATTOUT						
Average		Attenuation state < 8dB			27	dBm
		Attenuation state ≥ 8dB			24	dBm
Peak		Attenuation state < 8dB			30	dBm
		Attenuation state ≥ 8dB			27	dBm
Hot Switching		All attenuation states			24	dBm
Case Temperature	T_{CASE}		−40		105	°C

[1] For input linearity performance over frequency, see Figure 50 to Figure 51.

[2] Video feedthrough is peak transient measured at the RF ports in a 50Ω test setup, without an RF signal present while switching the control voltage.

[3] Device does not support intermediate supply voltage levels except for those listed in Table 2.

[4] For RF power handling derating over the extended frequency range, see Figure 2.

[5] For T_{CASE} = 105°C operation, the RF power handling derates from the T_{CASE} = 85°C specifications by 3 dB.

[6] Peak: (≤100ns pulse duration, 5% duty cycle).

TIMING SPECIFICATIONS

See Figure 53, Figure 54, and Figure 55 for the timing diagrams.

Table 3. Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Serial period, see the Serial Mode Interface section	20			ns
t_{CS}	Control setup time, see the Serial Mode Interface section	3			ns
t_{CH}	Control hold time, see the Serial Mode Interface section	3			ns
t_{LN}	LE setup time, see the Serial Mode Interface section	3			ns
t_{LEW}	LE pulse width, see the Serial Mode Interface section and the Latched Parallel Mode section	5			ns
t_{LES}	LE pulse spacing, see the Serial Mode Interface section	150			ns
t_{CKN}	Serial clock hold time from LE, see the Serial Mode Interface section	3			ns
t_{PH}	Hold time, see the Latched Parallel Mode section	3			ns
t_{PS}	Setup time, see the Latched Parallel Mode section	5			ns
t_{CO}	Clock to output (SEROUT) time, see the Serial Mode Interface section			20	ns

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.5V to +5.5V
Digital Control Inputs	
Voltage	−0.3V to +3.6V
Current	3mA
RF Power[1] (f = 50MHz to 18GHz, T_{CASE} = 85°C[2])	
Input at ATTIN	
Average (5V or 3.3V, All Attenuation States)	27.5dBm
Peak	
5V, Attenuation State < 8dB	32.5dBm
5V, Attenuation State ≥ 8dB	29.5dBm
3.3V, Attenuation State < 8dB	30.5dBm
3.3V, Attenuation State ≥ 8dB	27.5dBm
Hot Switching (5V or 3.3V, All Attenuation States)	27.5dBm
Input at ATTOUT	
Average	
5V or 3.3V, Attenuation State < 8dB	27.5dBm
5V or 3.3V, Attenuation State ≥ 8dB	24.5dBm
Peak	
5V, Attenuation State < 8dB	32.5dBm
5V, Attenuation State ≥ 8dB	29.5dBm
3.3V, Attenuation State < 8dB	30.5dBm
3.3V, Attenuation State ≥ 8dB	27.5dBm
Hot Switching (5V or 3.3V, All Attenuation States)	24.5dBm
Unbiased (VDD = 0V, Input at ATTIN and ATTOUT)	27dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to 150°C
Reflow	260°C

[1] For RF power handling derating over extended frequency range, see Figure 2.

[2] For T_{CASE} = 105°C operation, the RF power handling derates from the T_{CASE} = 85°C specifications by 3 dB.

Stresses at or above those listed under absolute maximum ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to carrier bottom) thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-24-20	100	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

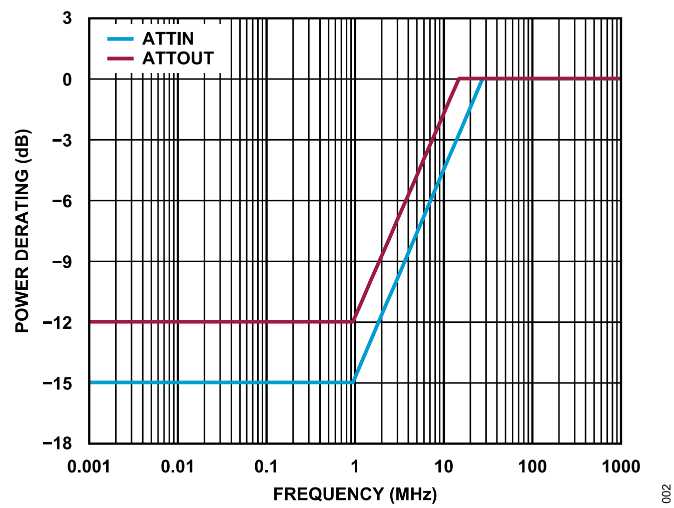

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5702

Table 6. ADRF5702, 24-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM		
RFx and RFC Pins	2000	2
Supply and Control Pins	2000	2
CDM	500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

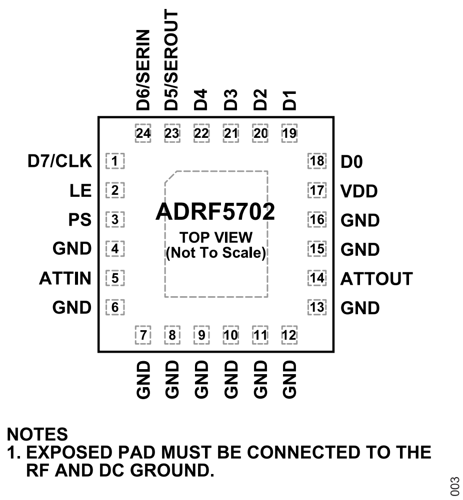

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D7/CLK	Parallel Control Input for 16dB Attenuator Bit (D7). Serial Clock Input (CLK). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
2	LE	Latch Enable Input. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
3	PS	Parallel or Serial Control Interface Selection Input. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
4, 6 to 13, 15, 16	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
5	ATTIN	Attenuator Input. See Figure 4 for the interface schematic. This pin is DC coupled and matched to 50Ω. A DC blocking capacitor is necessary.
14	ATTOUT	Attenuator Output. See Figure 4 for the interface schematic. This pin is DC coupled and matched to 50Ω. A DC blocking capacitor is necessary.
17	VDD	Positive Supply Input. See Figure 7 for the interface schematic.
18	D0	Parallel Control Input for 0.125dB Attenuator Bit (D0). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
19	D1	Parallel Control Input for 0.25dB Attenuator Bit (D1). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
20	D2	Parallel Control Input for 0.5dB Attenuator Bit (D2). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
21	D3	Parallel Control Input for 1dB Attenuator Bit (D3). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
22	D4	Parallel Control Input for 2dB Attenuator Bit (D4). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
23	D5/SEROUT	Parallel Control Input for 4dB Attenuator Bit (D5). Serial Data Output (SEROUT). See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
24	D6/SERIN	Parallel Control Input for 8dB Attenuator Bit (D6). Serial Data Input (SERIN). See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
	EPAD	Exposed pad must be connected to the RF and DC ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

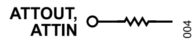

Figure 4. ATTIN and ATTOUT Interface Schematic

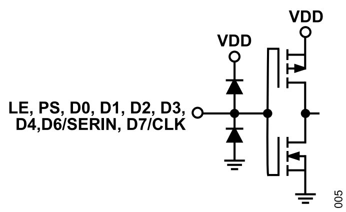

Figure 5. Digital Input Interface Schematic (LE, PS, D0, D1, D2, D3, D4, D6/SERIN, and D7/CLK)

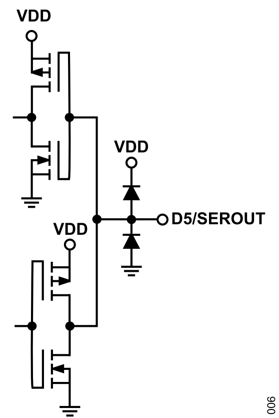

Figure 6. Digital Input Interface Schematic (D5/SEROUT)

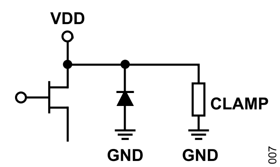

Figure 7. VDD Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION AND RETURN LOSS, ATTENUATION, STEP AND STATE ERROR, AND RELATIVE PHASE

VDD = 5V, V_{CTRL} = 0V or 3.3V, T_{CASE} = 25°C, and a 50Ω system, unless otherwise noted.

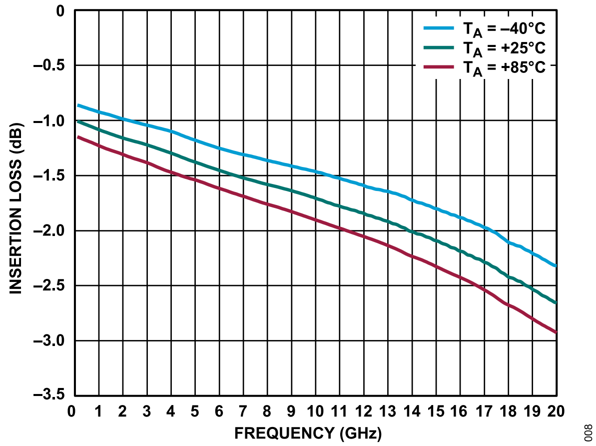

Figure 8. Insertion Loss vs. Frequency over Temperature

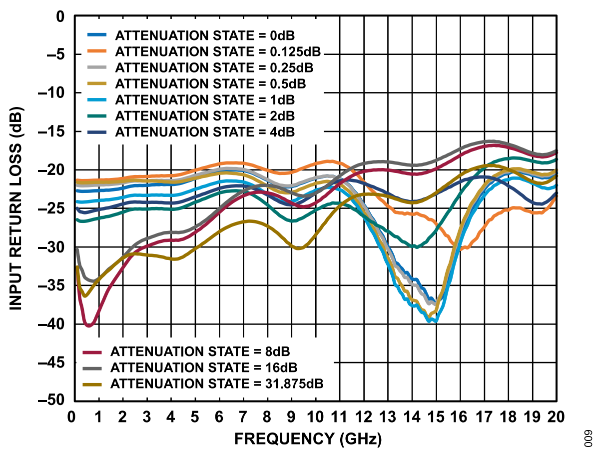

Figure 9. Input Return Loss vs. Frequency

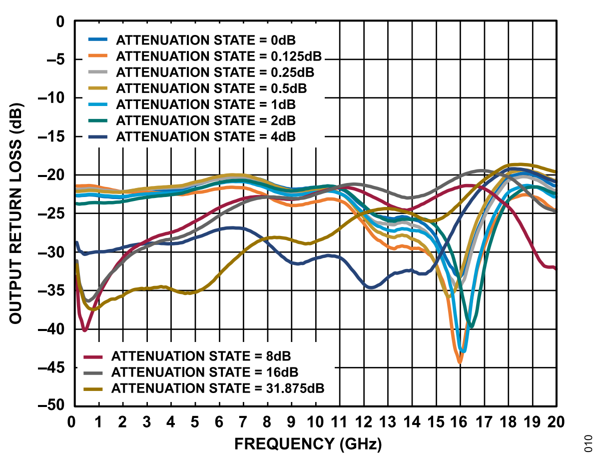

Figure 10. Output Return Loss vs. Frequency

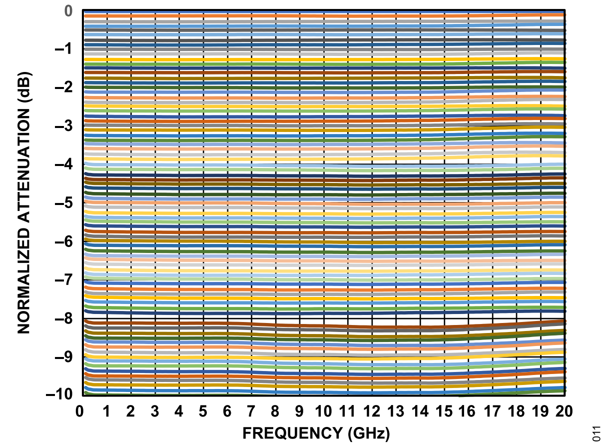

Figure 11. Normalized Attenuation vs. Frequency for States up to −10dB

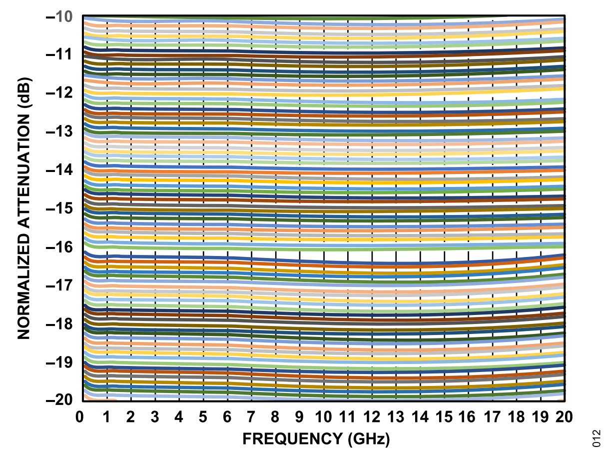

Figure 12. Normalized Attenuation vs. Frequency for States from −10dB to −20dB

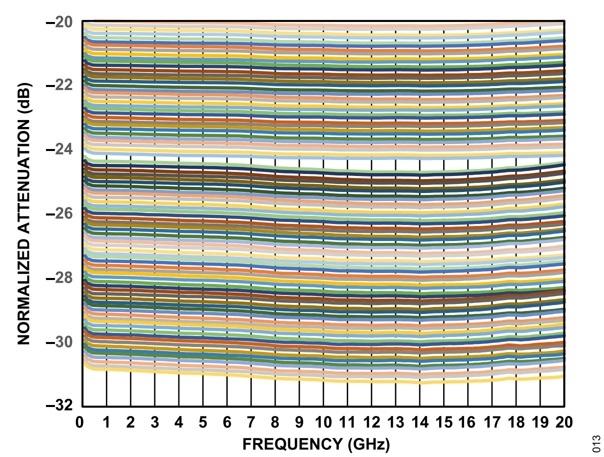

Figure 13. Normalized Attenuation vs. Frequency for States from −20dB to −32dB

TYPICAL PERFORMANCE CHARACTERISTICS

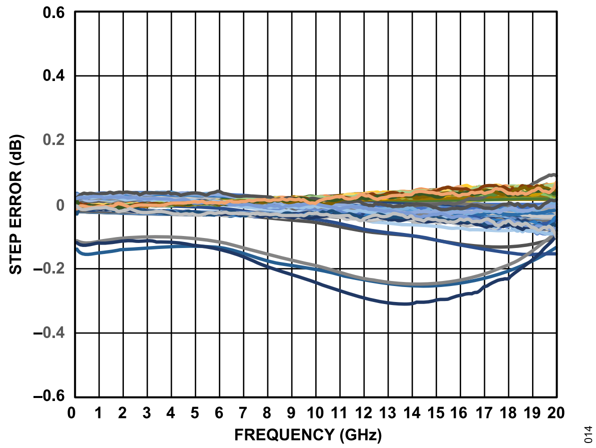

Figure 14. Step Error vs. Frequency at 25°C for 256 Attenuation States

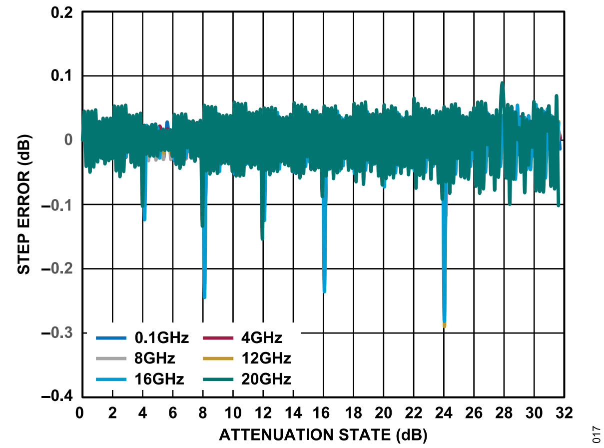

Figure 17. Step Error vs. Attenuation State at 25°C

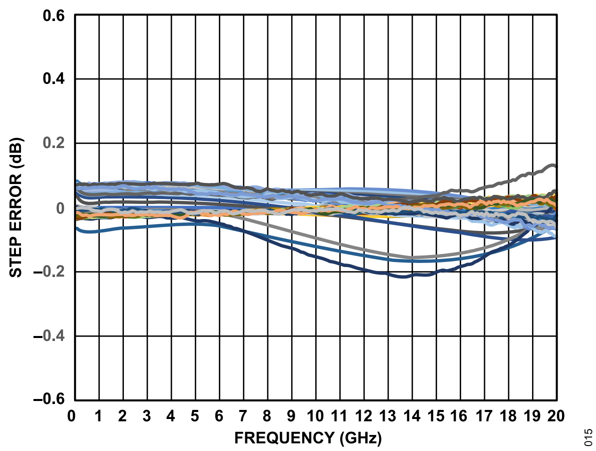

Figure 15. Step Error vs. Frequency at 85°C for 256 Attenuation States

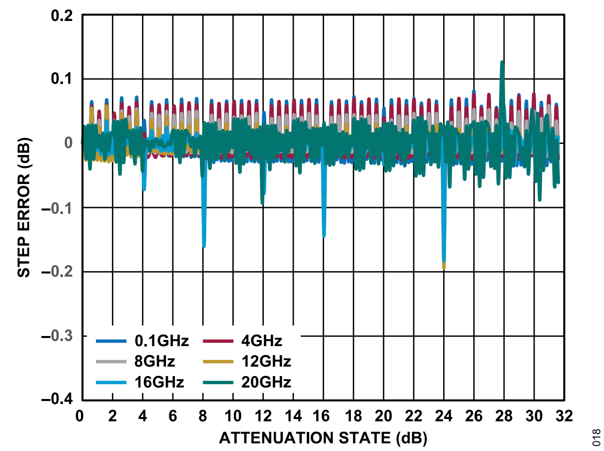

Figure 18. Step Error vs. Attenuation State at 85°C

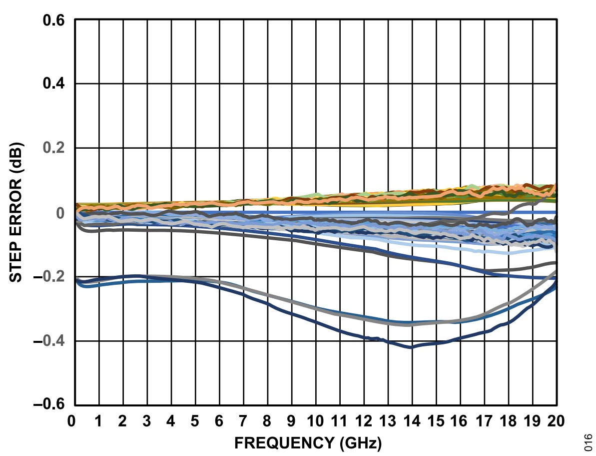

Figure 16. Step Error vs. Frequency at −40°C for 256 Attenuation States

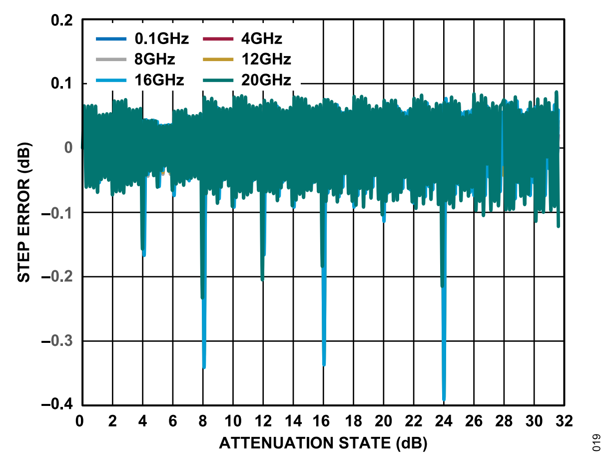

Figure 19. Step Error vs. Attenuation State at −40°C

TYPICAL PERFORMANCE CHARACTERISTICS

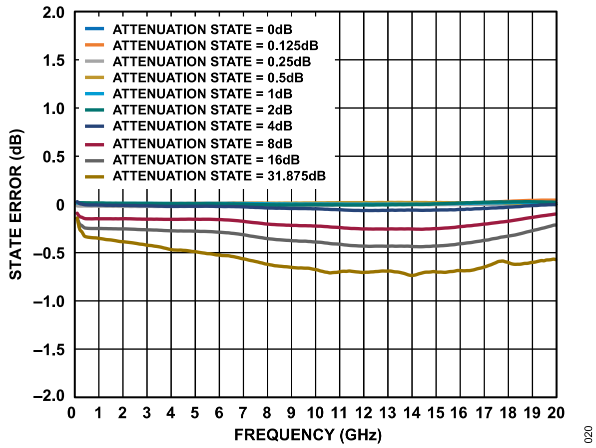

Figure 20. State Error vs. Frequency at 25°C

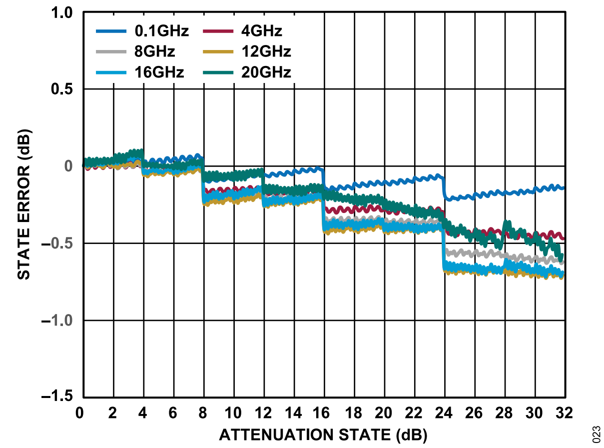

Figure 23. State Error vs. Attenuation State at 25°C

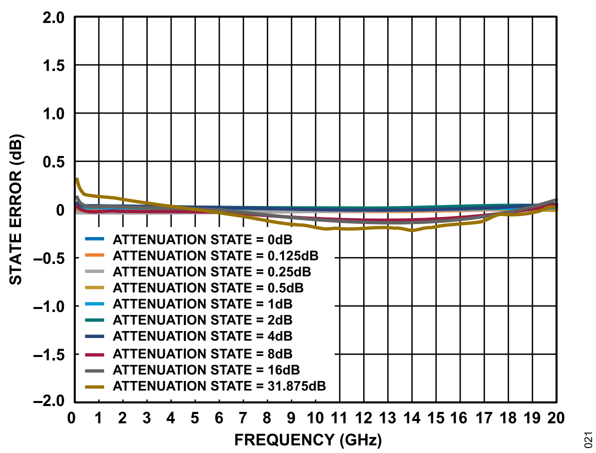

Figure 21. State Error vs. Frequency at 85°C

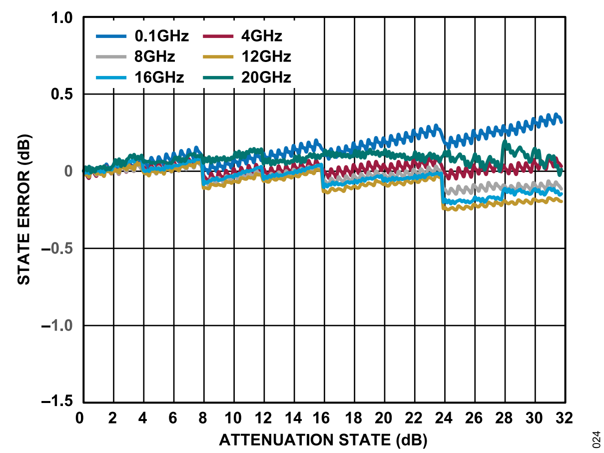

Figure 24. State Error vs. Attenuation State at 85°C

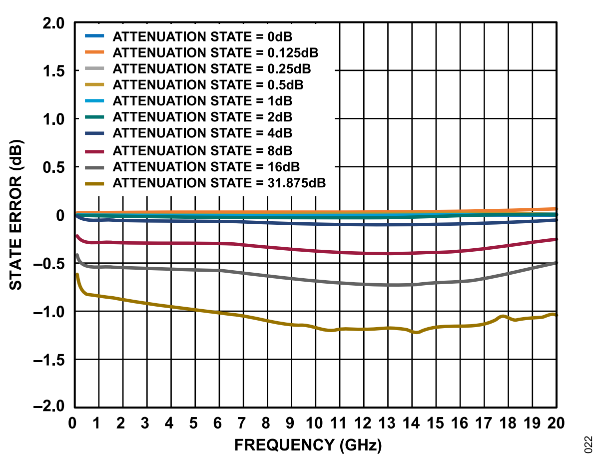

Figure 22. State Error vs. Frequency at −40°C

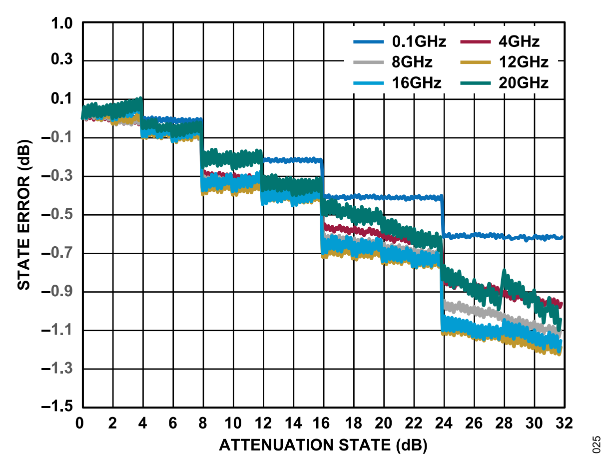

Figure 25. State Error vs. Attenuation State at −40°C

TYPICAL PERFORMANCE CHARACTERISTICS

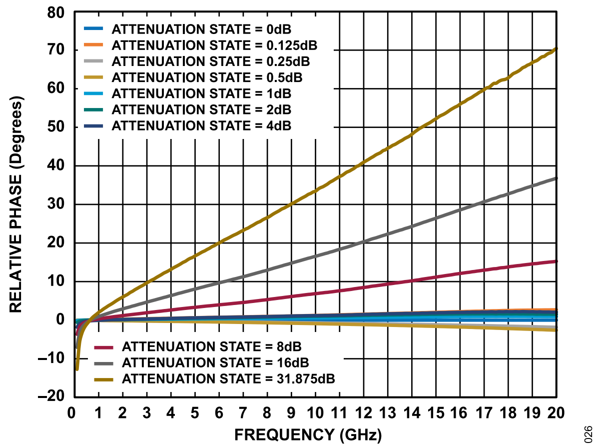

Figure 26. Relative Phase vs. Frequency

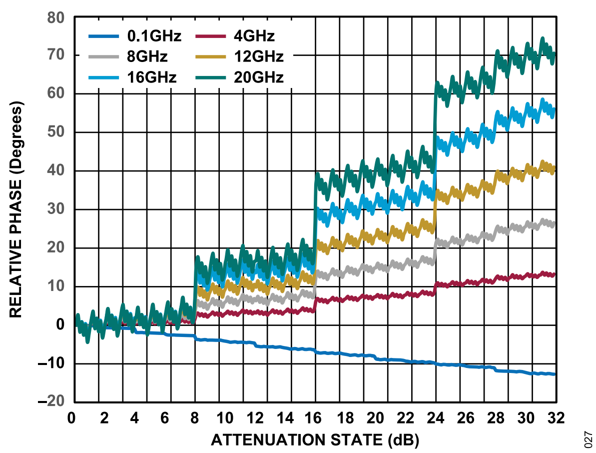

Figure 27. Relative Phase vs. Attenuation State over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 3.3V, V_{CTRL} = 0V or 3.3V, T_{CASE} = 25°C, and a 50Ω system, unless otherwise noted.

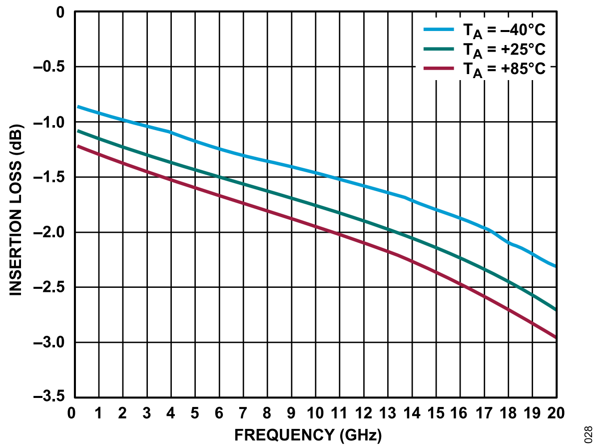

Figure 28. Insertion Loss vs. Frequency over Temperature

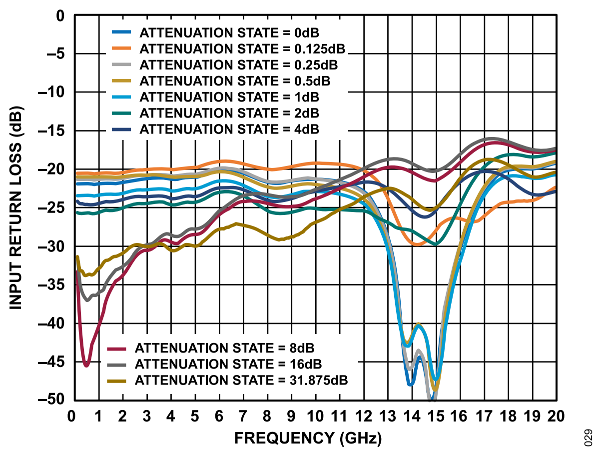

Figure 29. Input Return Loss vs. Frequency

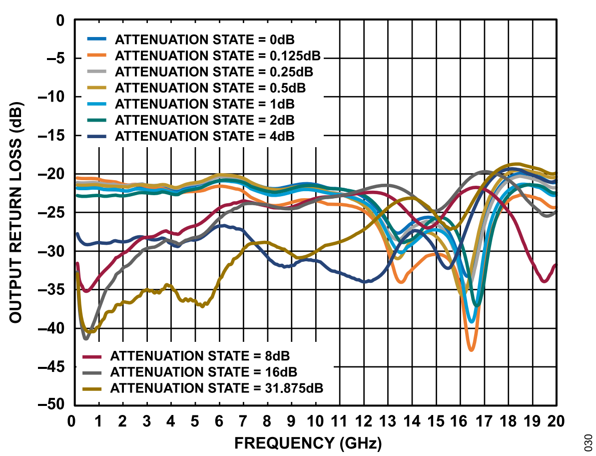

Figure 30. Output Return Loss vs. Frequency

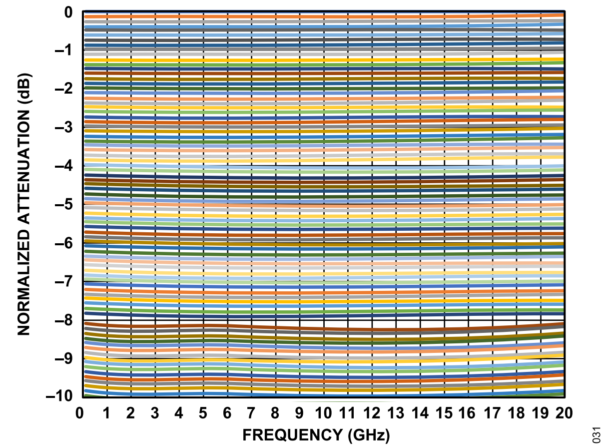

Figure 31. Normalized Attenuation vs. Frequency for States up to −10dB

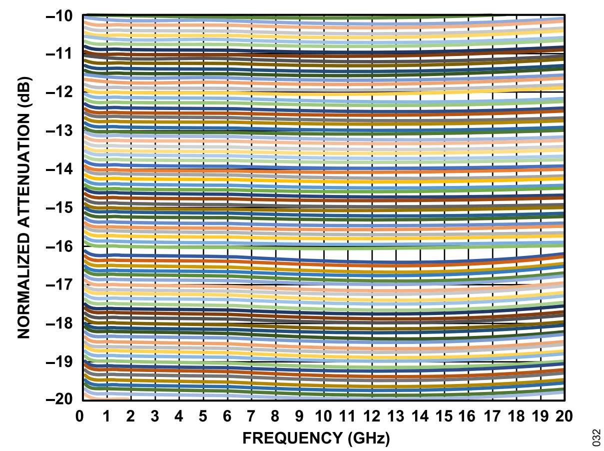

Figure 32. Normalized Attenuation vs. Frequency for States from −10dB to −20dB

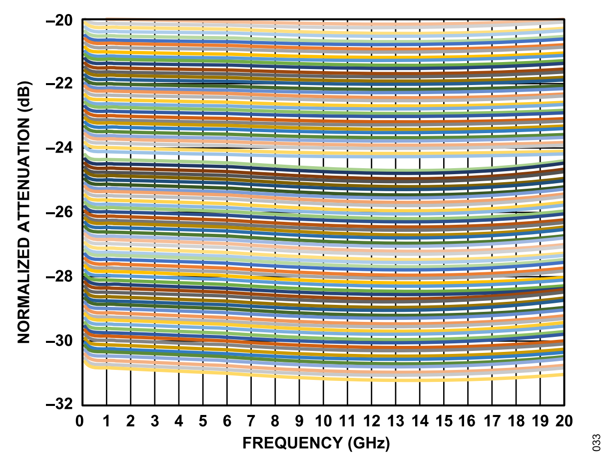

Figure 33. Normalized Attenuation vs. Frequency for States from −20dB to −32dB

TYPICAL PERFORMANCE CHARACTERISTICS

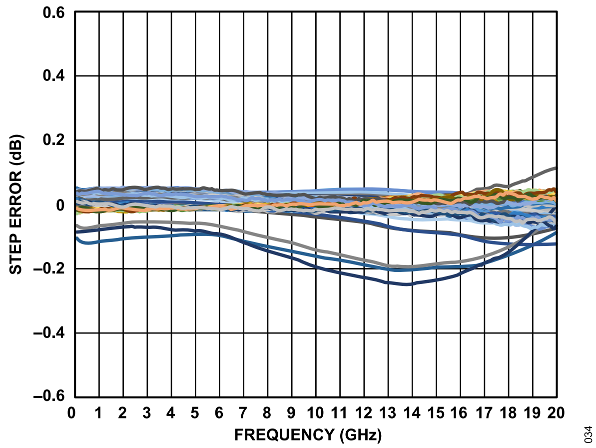

Figure 34. Step Error vs. Frequency at 25°C for 256 Attenuation States

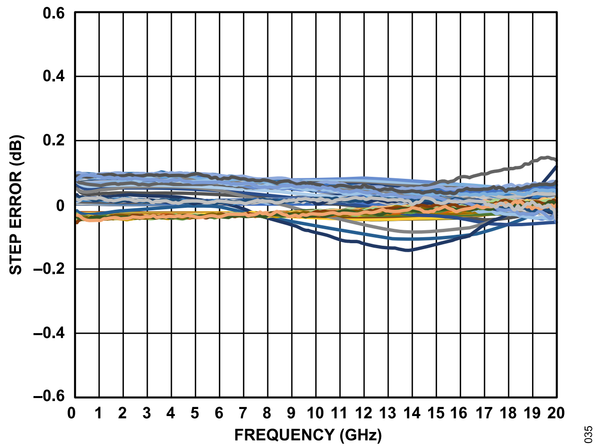

Figure 35. Step Error vs. Frequency at 85°C for 256 Attenuation States

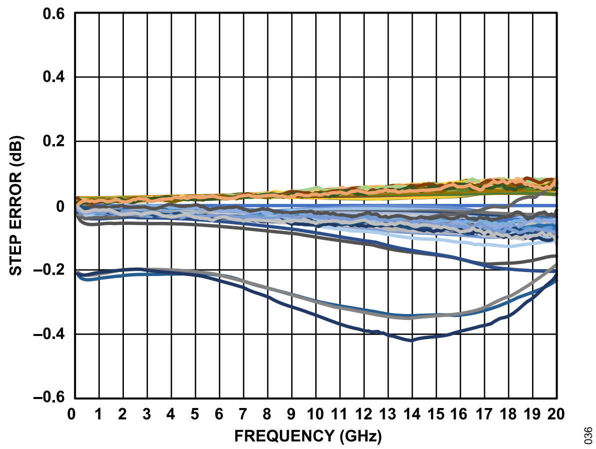

Figure 36. Step Error vs. Frequency at −40°C for 256 Attenuation States

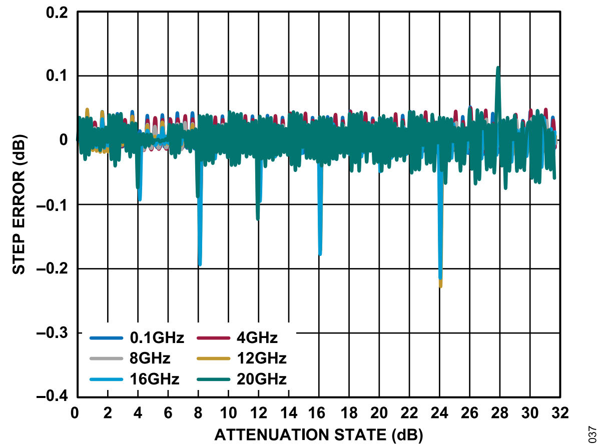

Figure 37. Step Error vs. Attenuation State at 25°C

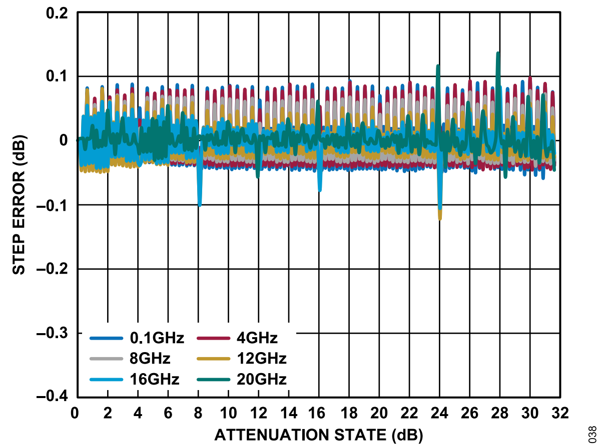

Figure 38. Step Error vs. Attenuation State at 85°C

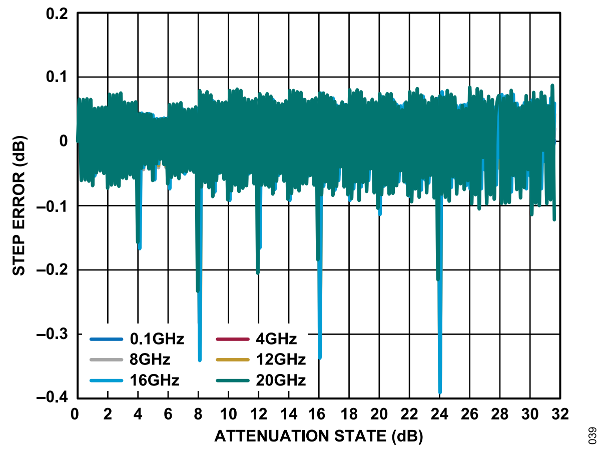

Figure 39. Step Error vs. Attenuation State at −40°C

TYPICAL PERFORMANCE CHARACTERISTICS

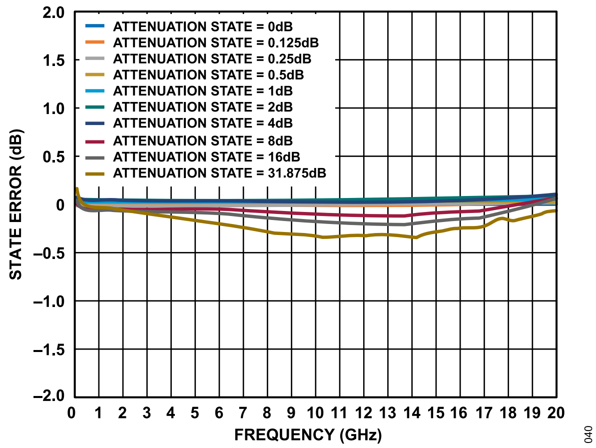

Figure 40. State Error vs. Frequency at 25°C

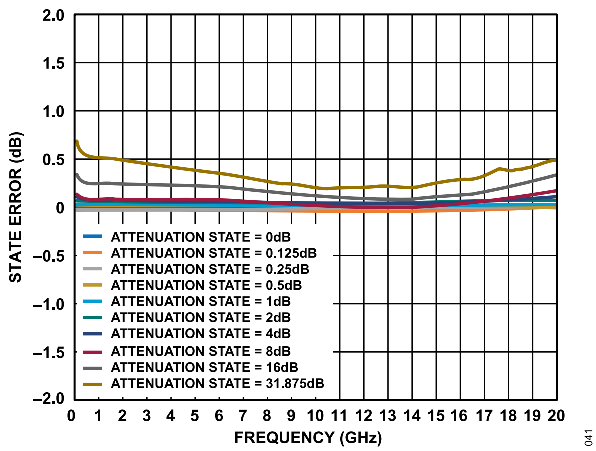

Figure 41. State Error vs. Frequency at 85°C

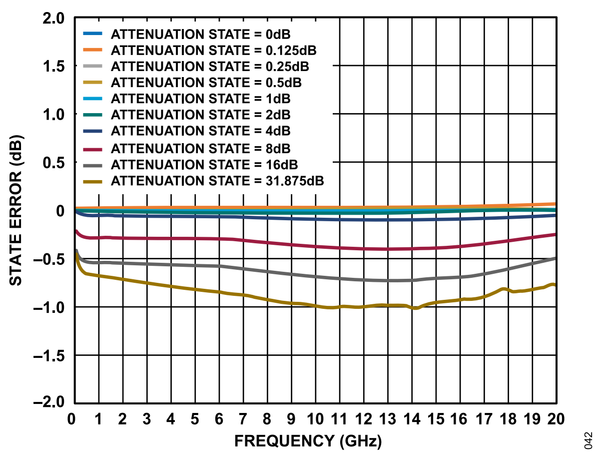

Figure 42. State Error vs. Frequency at −40°C

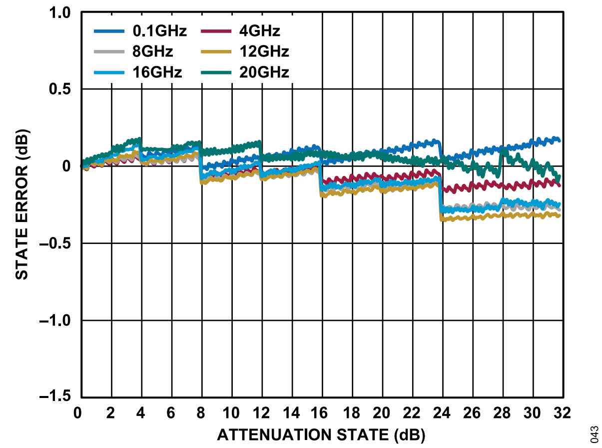

Figure 43. State Error vs. Attenuation State at 25°C

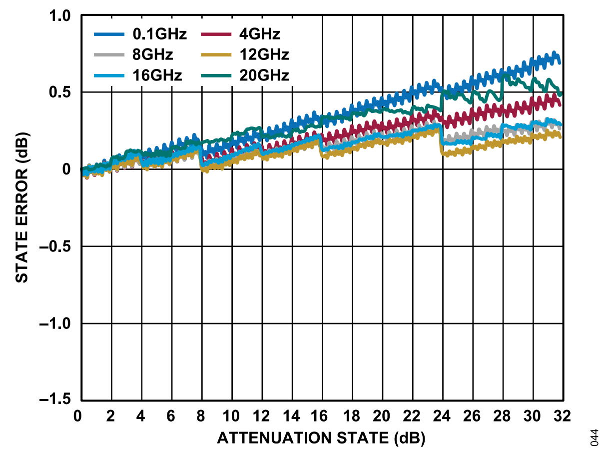

Figure 44. State Error vs. Attenuation State at 85°C

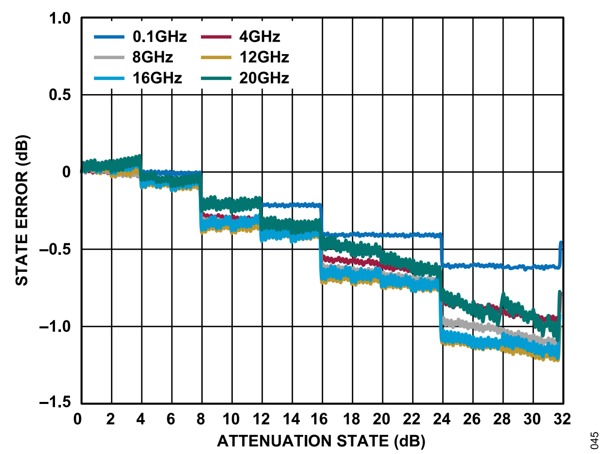

Figure 45. State Error vs. Attenuation State at −40°C

TYPICAL PERFORMANCE CHARACTERISTICS

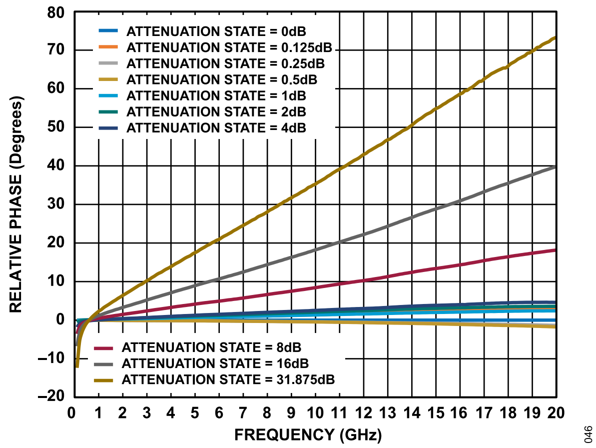

Figure 46. Relative Phase vs. Frequency

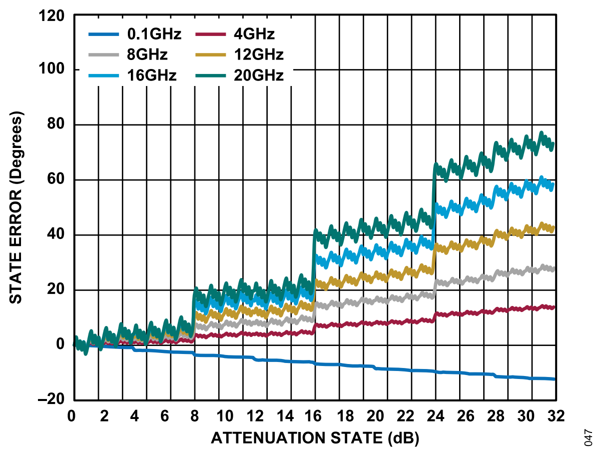

Figure 47. Relative Phase vs. Attenuation State over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 5V, V_{CTRL} = 0V or 3.3V, T_{CASE} = 25°C, and a 50Ω system, unless otherwise noted.

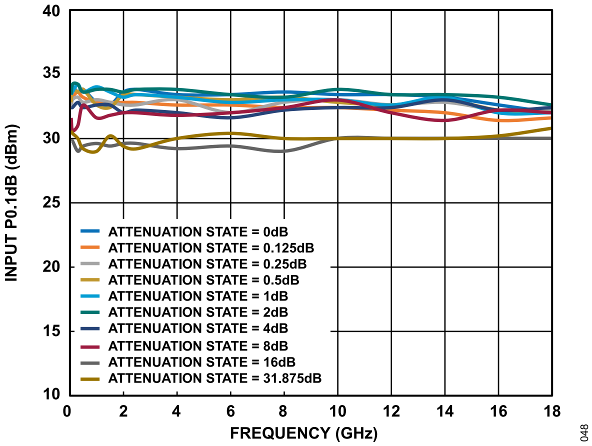

Figure 48. Input P0.1dB vs. Frequency

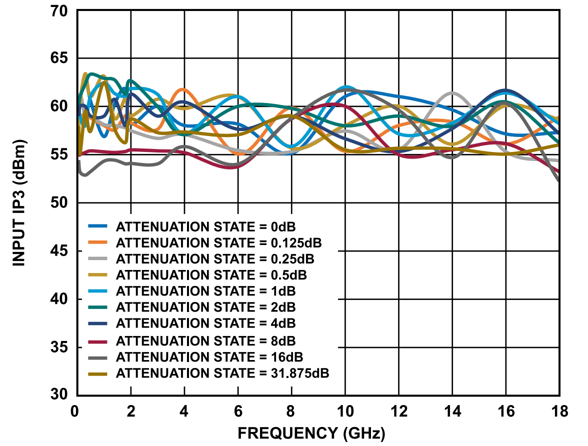

Figure 49. Input IP3 vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 3.3V, V_{CTRL} = 0V or 3.3V, T_{CASE} = 25°C, and a 50Ω system, unless otherwise noted.

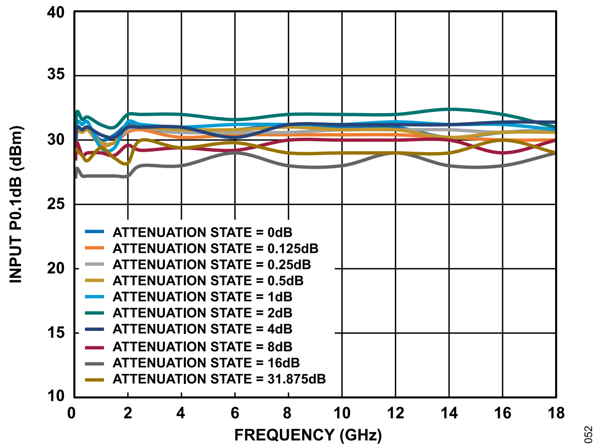

Figure 50. Input P0.1dB vs. Frequency

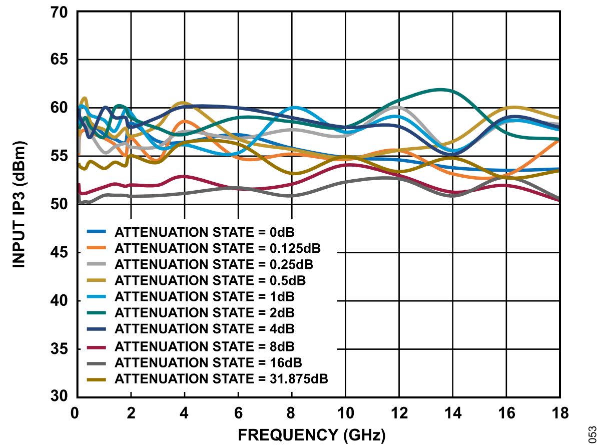

Figure 51. Input IP3 vs. Frequency

THEORY OF OPERATION

The ADRF5702 incorporates a 8-bit fixed attenuator array that offers an attenuation range of 31.875 dB with a 0.125 dB step size. An integrated driver provides serial or parallel mode control of the attenuator array.

The ADRF5702 has ten digital control inputs, D0 (LSB) to D7 (MSB), LE, and PS. To select the desired attenuation state in serial or parallel mode, refer to Table 8 and Table 9. For timing diagrams, see Figure 53, Figure 54, and Figure 55.

POWER SUPPLY

The ADRF5702 requires a positive supply voltage applied to the VDD pin. The device does not support supply intermediate supply voltage levels except the values listed in the Electrical Specifications section. Bypassing capacitors are recommended on the supply line to filter high frequency noise.

The power-up sequence follows:

1. Connect GND to ground.
2. Power up the V_{DD} voltage.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the V_{DD} voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1kΩ resistor to limit the current flowing into the control pins in such cases.
4. Apply an RF input signal.

The power-down sequence is the reverse order of the power-up sequence.

Power-Up State

The ADRF5702 has internal power-on reset circuitry that sets the attenuator to the maximum attenuation state (31.875 dB) when the V_{DD} voltage is applied.

RF INPUT AND OUTPUT

The power handling is defined by the ATTIN port. Refer to the RF input power specifications in Table 1.

Table 8. Truth Table

Digital Control Input[1]								
D7	D6	D5	D4	D3	D2	D1	D0	Attenuation State (dB)
Low	Low	Low	Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	Low	Low	Low	High	0.125
Low	Low	Low	Low	Low	Low	High	Low	0.25
Low	Low	Low	Low	Low	High	Low	Low	0.5
Low	Low	Low	Low	High	Low	Low	Low	1.0
Low	Low	Low	High	Low	Low	Low	Low	2.0
Low	Low	High	Low	Low	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	High	High	31.875

1 Any combination of the states within this table provides an attenuation equal to the sum of the bits selected.

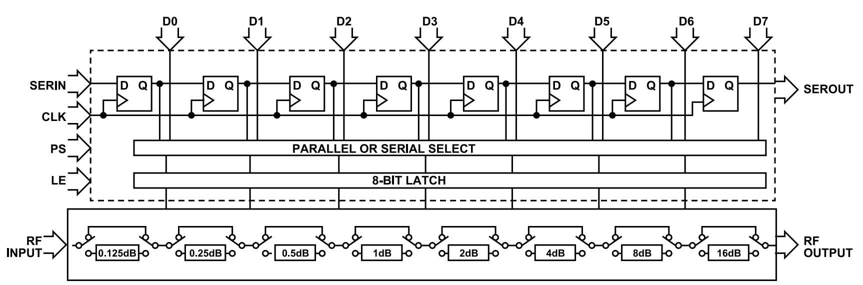

Figure 52. Simplified Circuit Diagram

THEORY OF OPERATION

SERIAL OR PARALLEL MODE SELECTION

The ADRF5702 can be controlled in either serial or parallel mode by setting the PS pin to high or low, respectively (see Table 9).

Table 9. Mode Selection

PS	Control Mode
Low	Parallel
High	Serial

SERIAL MODE INTERFACE

The ADRF5702 supports a 4-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), serial data output (SEROUT), and latch enable (LE). The serial control interface is activated when the PS pin is set to high.

The ADRF5702 attenuation states can be controlled using the 8-bit SERIN data.

In serial mode, the SERIN data is clocked MSB first on the rising CLK edges into the shift register. Then, LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock the new SERIN data into the shift register as CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 53, Figure 54, the Timing Specifications section, and the RF Input and Output section for additional information.

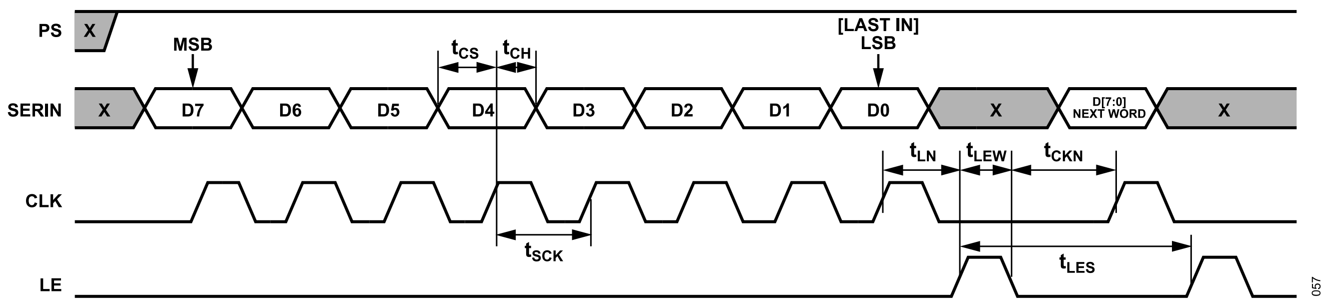

Figure 53. Serial Control Timing Diagram

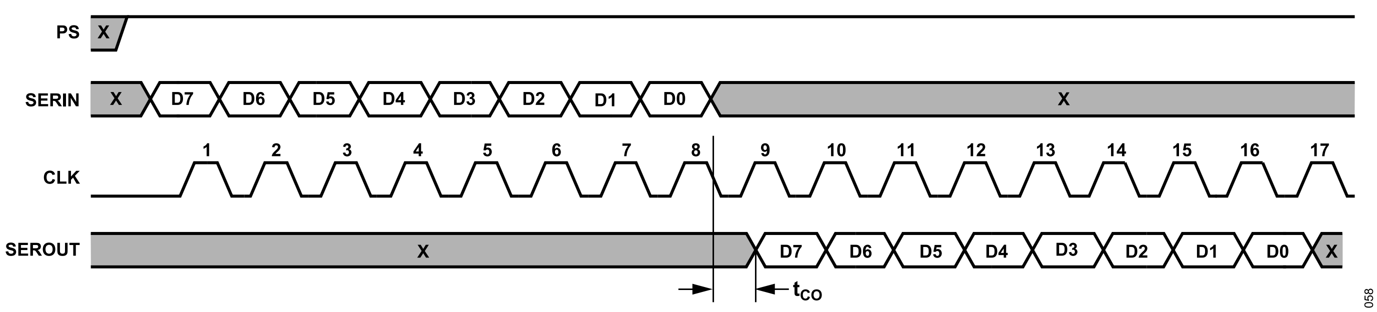

Figure 54. Serial Output Timing Diagram

THEORY OF OPERATION

PARALLEL MODE INTERFACE

The ADRF5702 has eight digital control inputs, D0 (LSB) to D7 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 8.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode, keep the LE pin high. To change the attenuation state, use the control voltage inputs (D0 to D7) directly. Direct parallel mode is for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, the LE pin must be kept low when changing the control voltage inputs (D0 to D7) to set the attenuation state. When the desired state is set, toggle LE high to transfer the 8-bit data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change (see Figure 55 and Table 3 for additional information).

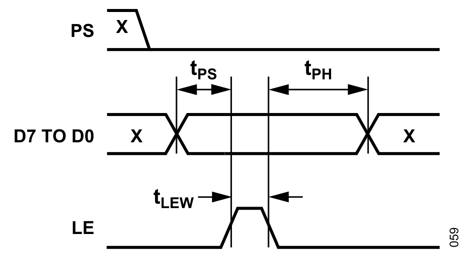

Figure 55. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

The ADRF5702 has one power supply pin (VDD) and ten control pins (PS, LE, and D0 to D7). Figure 56 shows the external components and connections for the supply and control pins. The supply pin (VDD) is decoupled with 100pF multilayer ceramic capacitor. Place the decoupling capacitor as close as possible to the ADRF5702. Because the RF lines are biased at a nonzero voltage, DC blocking capacitors are required. The device pinout allows the placement of the decoupling capacitors close to the ADRF5702. Refer to the Pin Configuration and Function Descriptions section for additional information.

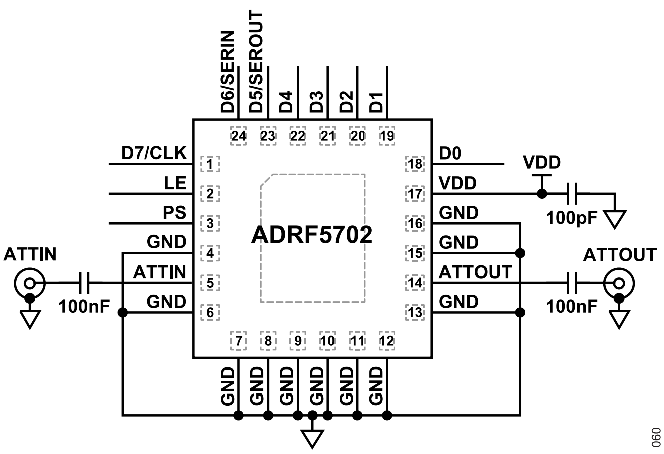

Figure 56. Simplified Application Circuit

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50Ω characteristic impedance on the PCB. Figure 57 shows the referenced CPWG RF trace design for an RF substrate with 8mil thick Rogers RO4003 dielectric material. The RF trace with a 14mil width and a 7mil clearance is recommended for 1.5mil finished copper thickness.

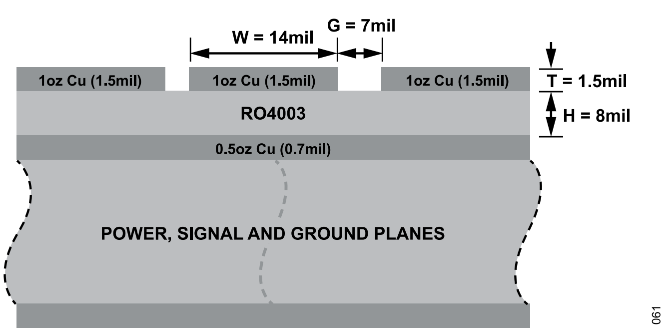

Figure 57. Example PCB Stack-Up

Figure 58 shows the routing of the RF traces, supply, and control signals from the ADRF5702. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

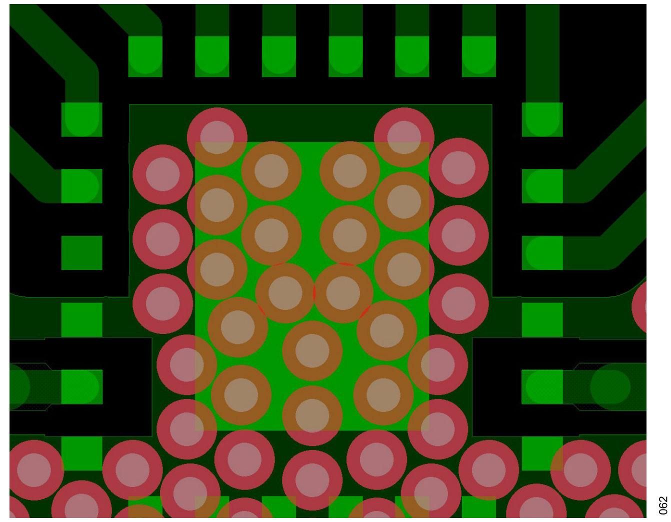

Figure 58. PCB Routings

Figure 59 shows the recommended layout from the device RF pins to the 50Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to the device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended to the device edge and tapered to the RF trace with a 45° angle. The paste mask is designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

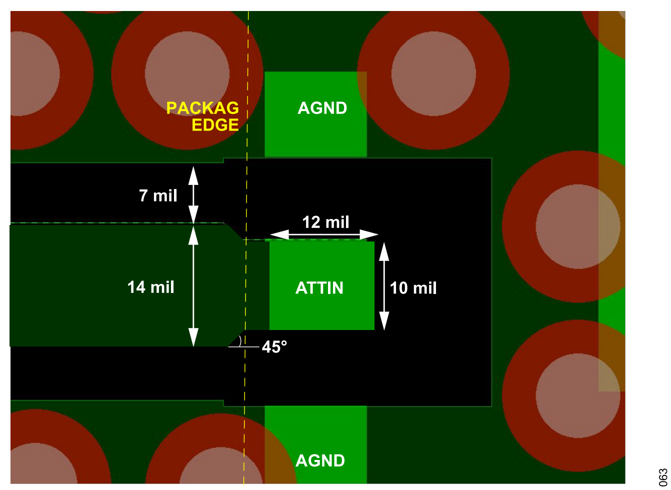

Figure 59. Recommended ATTIN Pin and ATTOUT Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support for further recommendations.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CC-24-20	LGA	24-Terminal Land Grid Array Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5702BCCZN	−40°C to +105°C	24-Terminal Land Grid Array [LGA]	Tape, 500	CC-24-20
ADRF5702BCCZN-R7	−40°C to +105°C	24-Terminal Land Grid Array [LGA]	Reel, 500	CC-24-20

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADRF5702-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.