ANALOG DEVICES

Data Sheet

ADRF5476

Flip-Chip, Silicon Digital Step Attenuator, 1GHz to 72GHz

FEATURES

- Frequency range: 1GHz to 72GHz
- Attenuation range: 12dB with a 4dB step size
- Bidirectional operation
- Low insertion loss
  - 0.9dB up to 18GHz
  - 1.3dB up to 40GHz
  - 2.1dB up to 67GHz
  - 3.0dB up to 72GHz
- Typical step error
  - ±0.50dB up to 55GHz
  - ±0.75dB up to 72GHz
- High input linearity
  - P0.1dB: >24dBm typical
  - IP3: >45dBm typical
- High RF input power handling
  - Steady state: 24dBm
  - Hot switching: 24dBm
- No low frequency spurious signals
- Parallel mode control, CMOS- and LVTTL-compatible
- RF amplitude settling time (50% triggered control to 0.1dB of final RF output): 55ns
- 14-ball, 1.940mm × 1.160mm, bumped bare die sales

APPLICATIONS

- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

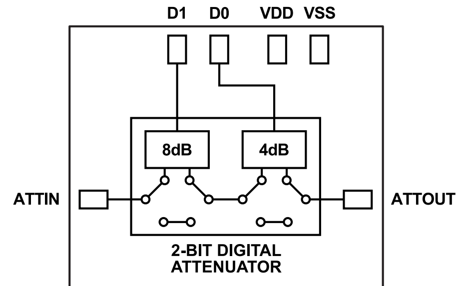

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5476 is a silicon, 2-bit digital attenuator with a 12dB attenuation range with a 4dB step size.

The ADRF5476 is specified from 1GHz to 72GHz with less than 3.0dB of insertion loss and with ±0.75dB step error at 72GHz. The device can operate bidirectionally, the ATTIN and ATTOUT ports of the ADRF5476 have an RF power handling capability of 24dBm average and 24dBm peak for all states.

The ADRF5476 draws a current of +124μA on the positive supply of +3.3V and −528μA on negative supply of −3.3V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5476 RF ports are designed to match a characteristic impedance of 50Ω.

The ADRF5476 is a 14-ball, 1.940mm × 1.160mm, bumped bare die sales and can operate between −40°C to +105°C.

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REVISION HISTORY

1/2026—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = +3.3V, VSS = −3.3V, D0 = 0V or VDD, D1 = 0V or VDD, and case temperature (T_{CASE}) = 25°C for 50Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		1		72	GHz
INSERTION LOSS	10MHz to 18GHz		0.9		dB
	18GHz to 40GHz		1.3		dB
	40GHz to 55GHz		1.6		dB
	55GHz to 67GHz		2.1		dB
	6 GHz to 7 GHz		3.0		dB
RETURN LOSS	ATTIN and ATTOUT, all attenuation states				
	10MHz to 18GHz		17		dB
	18GHz to 40GHz		16		dB
	40GHz to 55GHz		16		dB
	55GHz to 67GHz		15		dB
	67GHz to 72GHz		15		dB
ATTENUATION					
Range	Between minimum and maximum attenuation states		12		dB
Step Size	Between any successive attenuation states		4		dB
Accuracy	Referenced to insertion loss state				
	10MHz to 18GHz		±(0.3 + 3% of state)		dB
	18GHz to 40GHz		±(0.5 + 5% of state)		dB
	40GHz to 55GHz		±(0.5 + 5% of state)		dB
	55GHz to 67GHz		±(0.5 + 5% of state)		dB
	67GHz to 72GHz		±(0.5 + 5% of state)		dB
Step Error	Between any successive state				
	10MHz to 18GHz		±0.20		dB
	18GHz to 40GHz		±0.40		dB
	40GHz to 55GHz		±0.50		dB
	55GHz to 67GHz		±0.50		dB
	67GHz to 72GHz		±0.75		dB
RELATIVE PHASE	Referenced to insertion loss state				
	10MHz to 18GHz		14		Degrees
	18GHz to 40GHz		34		Degrees
	40GHz to 55GHz		48		Degrees
	55GHz to 67GHz		56		Degrees
	67GHz to 72GHz		57		Degrees
SWITCHING CHARACTERISTICS	All attenuation states at an input power (P_{IN}) = 10dBm				
Rise Time and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output		5		ns
On Time and Off Time (t_{ON} and t_{OFF})	50% triggered control to 90% of RF output		10		ns
RF Amplitude Settling Time					
0.1dB	50% triggered control to 0.1dB of final RF output		55		ns
0.05dB	50% triggered control to 0.05dB of final RF output		70		ns
RF Phase Settling Time	f = 40 GHz				
5°	50% triggered control to 5° of final RF output		34		ns
1°	50% triggered control to 1° of final RF output		40		ns

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT LINEARITY[1]	1GHz to 72GHz				
0.1dB Power Compression (P0.1dB)			>24		dBm
1dB Power Compression (P1dB)			>24		dBm
Third-Order Intercept (IP3)	Two-tone input power = 10dBm per tone, Δf = 1MHz, all attenuation states		>45		dBm
DIGITAL CONTROL INPUTS	D1 and D0				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Current					
Low (I_{INL})			−10		μA
High (I_{INH})			<1		μA
SUPPLY CURRENT					
Positive Supply Current (I_{DD})	VDD pin				
Bias Low	D1 and D0 = 0V		124		μA
Bias High	D1 and D0 = 3.3V		104		μA
Negative Supply Current (I_{SS})	VSS pin		−528		μA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage					
VDD		3.15		3.45	V
VSS		−3.45		−3.15	V
Digital Control Voltage		0		VDD	V
RF Power[2]	Frequency (f) = 3GHz to 72GHz, T_{CASE} = 85°C,[3] all attenuation states				
Input at ATTIN and ATTOUT	Steady state, average			24	dBm
	Steady state, peak			24	dBm
	Hot switching, average			24	dBm
	Hot switching, peak			24	dBm
T_{CASE}		−40		+105	°C

[1] Input linearity performance degrades over frequency.

[2] For power derating over frequency, see Figure 2. Power derating is applicable for all ATTIN and ATTOUT power specifications.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.3V to +3.6V
Negative Supply Voltage	−3.6V to +0.3V
Digital Control Input[1]	
Voltage	−0.3V to VDD + 0.3V
Current	3mA
RF Input Power[2] (f = 3GHz to 72GHz, T_{CASE} = 85°C[3])	
Input at ATTIN and ATTOUT	
Steady State, Average	27dBm
Steady State, Peak	27dBm
Hot Switching, Average	27dBm
Hot Switching, Peak	27dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C
Continuous Power Dissipation (P_{DISS})	0.125W

[1] Overvoltages at the digital control input are clamped by internal diodes. Current must be limited to the maximum rating given.

[2] For power derating vs. frequency, see Figure 2.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CD-14-1	200	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVE

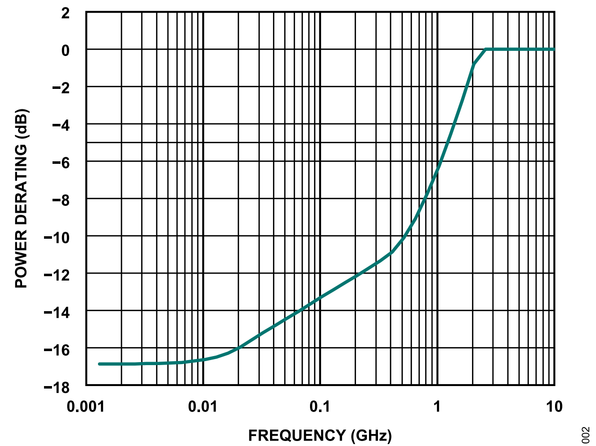


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

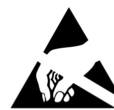
Human body model (HBM) per ESDA/JEDEC JS-001.

ESD Ratings for ADRF5476

Table 4. ADRF5476, 14-Ball BUMPED_CHIP

ESD Model	Withstand Threshold (V)
HBM	±750 for ATTIN and ATTOUT pins ±2000 for supply and digital control pins

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

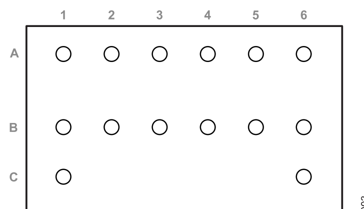


Figure 3. Pin Configuration (Top View—Ball Side Down)

Table 5. Pin Function Descriptions

Ball No.	Mnemonic	X Coordinate (mm)	Y Coordinate (mm)	Description
A1	GND	−0.750	+0.400	Ground.
A2	D1	−0.450	+0.400	Parallel Control Input for the 8dB Attenuator. The D1 pin is internally pulled up with 330kΩ. See Figure 4 for the interface schematic.
A3	D0	−0.150	+0.400	Parallel Control Input for the 4dB Attenuator. This D0 pin is internally pulled up with 330kΩ. See Figure 4 for the interface schematic.
A4	VDD	+0.150	+0.400	Positive Supply Voltage. See Figure 5 for the interface schematic.
A5	VSS	+0.450	+0.400	Negative Supply Voltage. See Figure 6 for the interface schematic.
A6	GND	+0.750	+0.400	Ground.
B1	GND	−0.750	−0.050	Ground.
B2	GND	−0.450	−0.050	Ground.
B3	GND	−0.150	−0.050	Ground.
B4	GND	+0.150	−0.050	Ground.
B5	GND	+0.450	−0.050	Ground.
B6	GND	+0.750	−0.050	Ground.
C1	ATTIN	−0.750	−0.350	Attenuator Input. The ATTIN pin is DC-coupled and biased to 0V and AC matched to 50Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0V DC. See Figure 7 for the interface schematic.
C6	ATTOUT	+0.750	−0.350	Attenuator Output. The ATTOUT pin is DC-coupled and biased to 0V and AC matched to 50Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0V DC. See Figure 7 for the interface schematic.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

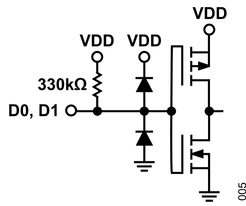


Figure 4. D0, D1 Interface Schematic

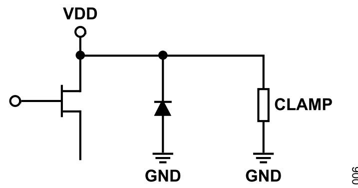


Figure 5. VDD Pin Interface Schematic

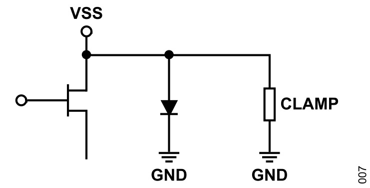


Figure 6. VSS Pin Interface Schematic

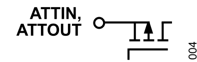


Figure 7. ATTIN, ATTOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, ATTENUATION, STEP ERROR, AND RELATIVE PHASE

VDD = +3.3V, VSS = −3.3V, D0 = 0V or VDD, D1 = 0V or VDD, and T_{CASE} = 25°C on a 50Ω system, unless otherwise noted. Insertion loss, return loss, and isolation are measured on a probe board using ground-signal (GS) probes close to the ATTIN and ATTOUT pins.

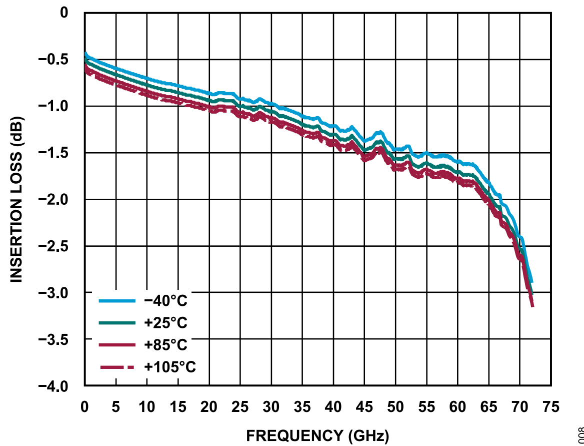


Figure 8. Insertion Loss vs. Frequency for Various Temperatures

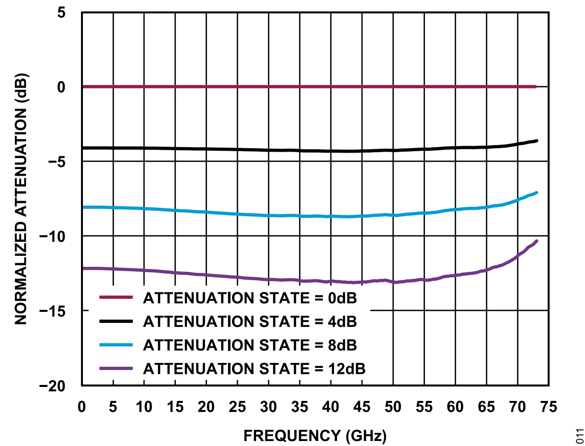


Figure 11. Normalized Attenuation vs. Frequency for All States

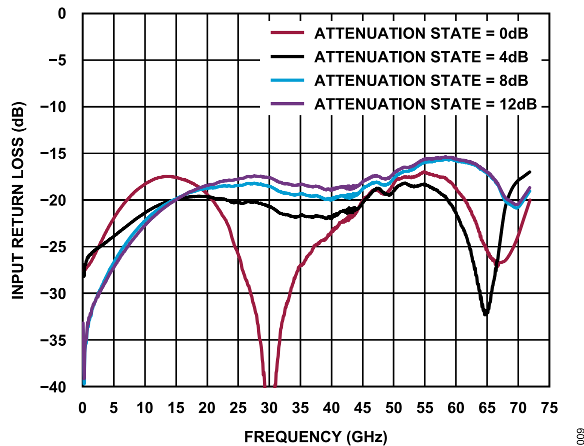


Figure 9. Input Return Loss vs. Frequency for All States

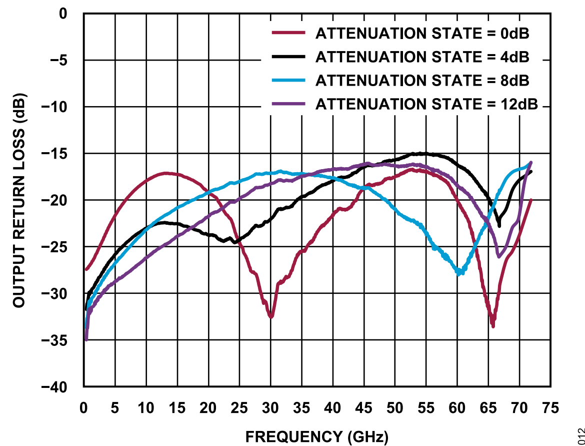


Figure 12. Output Return Loss vs. Frequency for All States

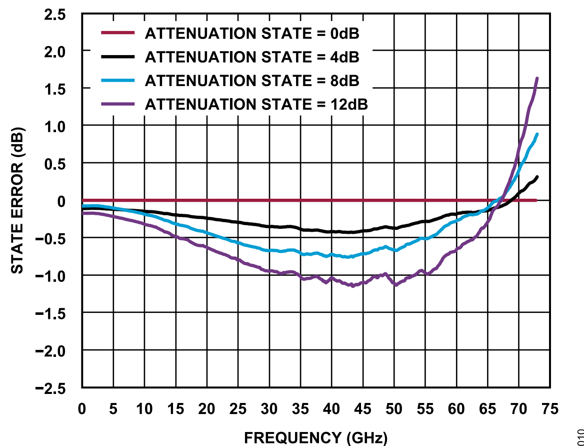


Figure 10. State Error vs. Frequency for All States

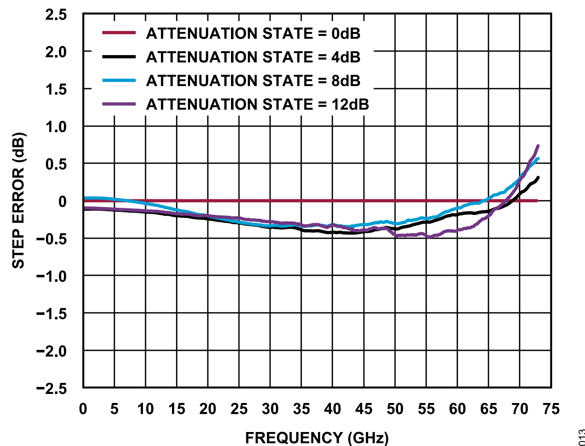


Figure 13. Step Error vs. Frequency for All States

TYPICAL PERFORMANCE CHARACTERISTICS

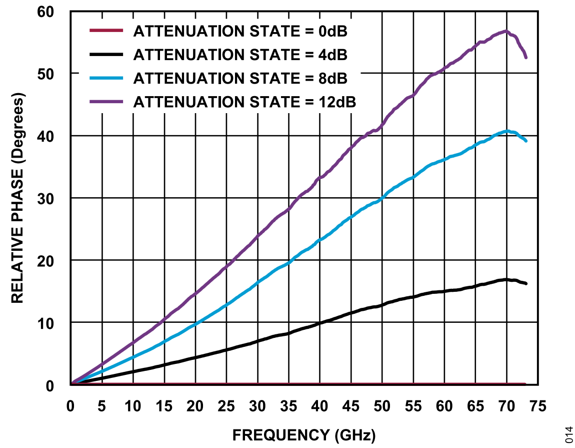


Figure 14. Relative Phase vs. Frequency for All States

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = +3.3V, VSS = −3.3V, D0 = 0V or VDD, D1 = 0V or VDD, and T_{CASE} = 25°C on a 50Ω system, unless otherwise noted. The large signal performance parameters are measured on a connectorized board.

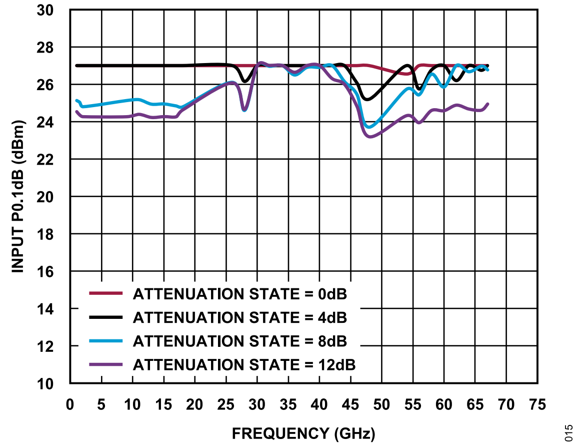


Figure 15. Input P0.1dB vs. Frequency for All States

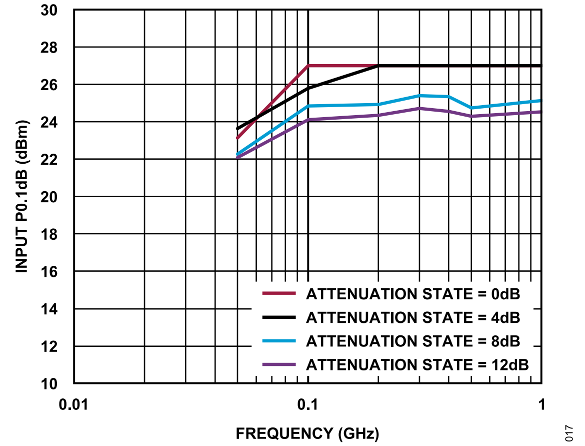


Figure 17. Input P0.1dB vs. Frequency (Low Frequency Detail) for All States

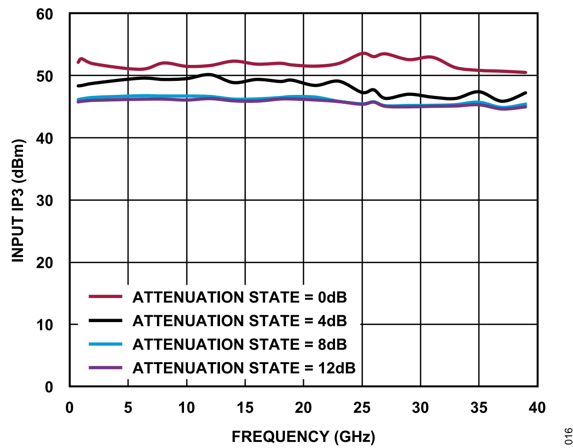


Figure 16. Input IP3 vs. Frequency for All States

THEORY OF OPERATION

The ADRF5476 incorporates a 2-bit fixed attenuator array that offers an attenuation range of 12dB with a 4dB step size. An integrated driver provides parallel mode control of the attenuator array.

The ADRF5476 has two digital control inputs, D0 and D1, to select the desired attenuation state in parallel mode. Internally, there are two 4dB stages, and these stages can be controlled by the D0 and D1 pins.

POWER SUPPLY

The ADRF5476 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Power up the digital control inputs. The relative order of the digital control inputs is not important. However, powering the digital control inputs before the VDD supply may inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1kΩ resistor to limit the current flowing into the control pin.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are DC-coupled to 0V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0V. The RF ports are internally matched to 50Ω.

The ADRF5476 supports bidirectional operation. The power handling of the ATTIN and ATTOUT ports are the same. Refer to the RF power input specifications in Table 1.

Table 6. Recommended Truth Table

Digital Control Input		
D1	D0	Attenuation State (dB)
Low	Low	0 (reference)
Low	High	4
High	Low	8
High	High	12

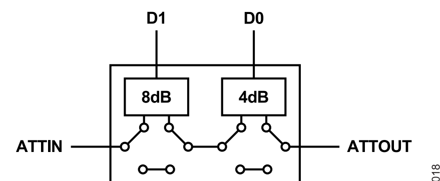


Figure 18. Simplified Circuit Diagram

APPLICATIONS INFORMATION

The ADRF5476 has two power supply pins (VDD and VSS) and two control pins (D1 and D2). Figure 19 shows the external components and connections for the supply pins. The VDD, VSS, D1, and D2 pins are decoupled with 100pF multilayer ceramic capacitors. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the ATTIN and ATTOUT pins when the RF lines are biased at a voltage other than 0V. Refer to the Pin Configuration and Function Descriptions section for further details.

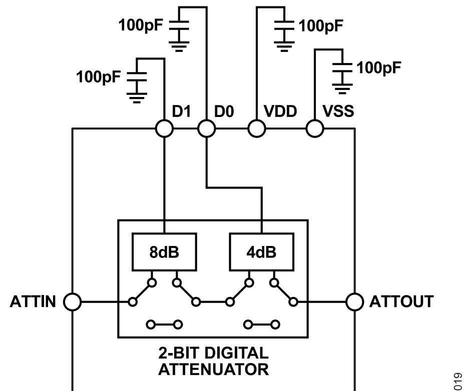


Figure 19. Recommended Schematic

APPLICATIONS INFORMATION

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with 50Ω characteristic impedance on the PCB. Figure 20 shows the referenced CPWG design for a 150μm thick Megtron6 2×1080 R-5775G dielectric material. The RF trace with 300μm width and 300μm gap is used for 42μm finished copper thickness.

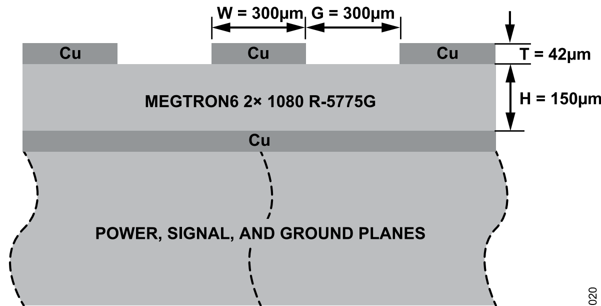


Figure 20. Probe Board Stackup

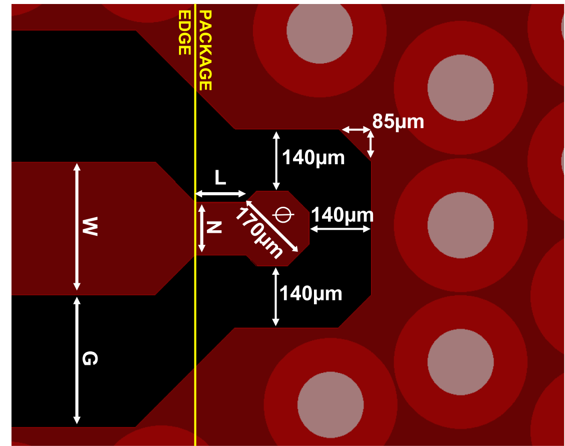


Figure 21. Recommended ATTIN Pin and ATTOUT Pin Transitions

Figure 21 shows the recommended layout from the ATTIN and ATTOUT pins of the device to the 50Ω CPWG. Signal pads have a 170μm diameter extended with a neck for broadband tuning and tapered to an RF trace with a 45° angle. The optimized ATTIN pin and ATTOUT pin transitions for broadband performance are given for different stackups in Table 7. For further recommendations on alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Analog Devices Support.

Table 7. Recommended ATTIN Pin and ATTOUT Pin Transitions for Different Stackups

RF Stackup Height and Dielectric		RF Trace Dimensions		ADRF5476	Transition Dimensions	
H (μm)	Er	W (μm)	G (μm)	Mnemonic	N (μm)	L (μm)
85	3.02	180	250	All	120	250
100	3.34	200	225	All	120	200
115	3.40	225	250	All	120	170
125	3.00	250	225	All	170	170
150[1].	3.40	300	300	All	170	170
175	3.16	360	245	All	170	170
190	3.00	425	225	All	170	170
200	3.55	425	275	All	170	170

[1] Design reference and generic footprint

APPLICATIONS INFORMATION

DIE ASSEMBLY

The ADRF5476 complies with standard RoHS-reflow assembly process and its temperature profiles. The device can be assembled with other surface-mounted technology (SMT) components in the same reflow cycle. However, the PCB must be designed according to the pick and place process.

The top copper layer of the PCB is designed for optimum RF performance where the solder mask and paste mask layers are designed for optimum assembly yield. The ground pads are drawn as solder mask defined. The signal pads are drawn as pad defined. The same solder mask and paste mask design can be used for both pads.

The ADRF5476 can also be assembled without applying a solder paste on the PCB. If no solder paste is applied, the ADRF5476 must be dipped into flux prior to placement on the PCB.

Reflow Assembly with Solder Paste

Solder mask openings of 175µm in a square shape are recommended for the signal and ATTIN and ATTOUT pins, and solder mask openings of 150µm in a square shape are recommended for the GND pins. Solder mask thickness must not exceed 50µm. Paste mask is drawn circular with a 150µm diameter. Using a stencil with 2mil thickness and no aperture reduction yields the optimum paste mask print. The device does not need any flux dipping during the pick and place process.

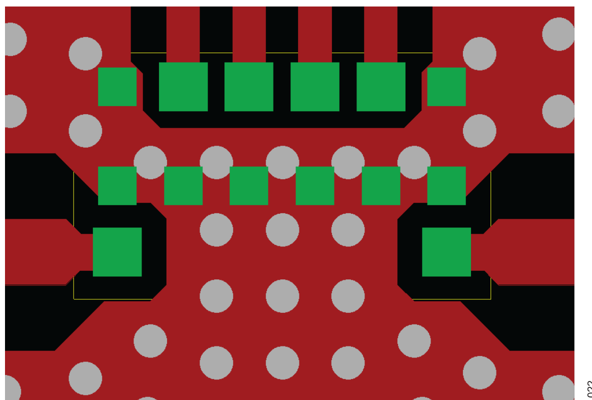


Figure 22. Recommended Footprint for Solder Paste

Reflow Assembly with Flux Dipping

Solder mask openings in a circular shape and 130µm in diameter are recommended. Solder mask thickness must not exceed 50µm. Solder paste is not applied. The device is dipped into flux prior to placement on the board.

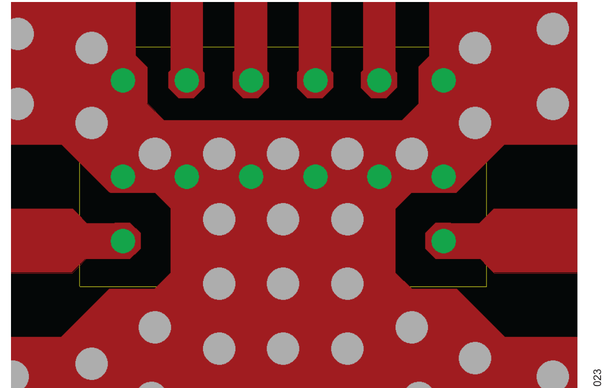


Figure 23. Recommended Footprint for Flux Dip Assembly

Assembly Durability

The device is a bumped die. The bump composition has a copper (Cu) pillar with a plated tin (Sn) and silver (Ag) solder-cap, which forms the device interconnect to the PCB when it is attached with reflow. The integrity of the interconnect structures and solder joints are compromised by the accumulated stress over temperature due to a mismatch of the thermomechanical properties of the different materials in the complete assembly of the user hardware. The ADRF5476 fulfills the JEDEC JED47L requirements under the JESD22-A104 Condition J (0-100C) for 2300 temperature cycles while mounted on a 0.75mm thick laminate PCB, which is assembled using solder paste reflow and without any underfill material applied. Users must qualify their hardware for the environmental conditions aligned with their end-use requirements because differences in PCB properties and design, varied number of temperature cycles, soak time, and dwell time, and changes in temperature range can affect thermomechanical results. Note that using a proper underfill adhesive significantly improves the integrity of the device assembly by reducing the stress exposed to the interconnect structures and solder joints.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CD-14-1	BUMPED_CHIP	14-Ball Bumped Bare Die Sales

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packaging Quantity	Package Option
ADRF5476BCDZ	−40°C to +105°C	14-Ball Bumped Bare Die Sales [BUMPED_CHIP]	Cut-Tape, 1 to 500	CD-14-1
ADRF5476BCDZ-R7	−40°C to +105°C	14-Ball Bumped Bare Die Sales [BUMPED_CHIP]	Reel, 500	CD-14-1

[1] Z = RoHS-Compliant Part.

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