Data Sheet

ADPL74101

100V Synchronous Step-Down Controller with Internal Bootstrap Switch

FEATURES

- Wide V_{IN} Range: 4V to 100V
- Wide output voltage range: 0.8V ≤ V_{OUT} ≤ 60V
- Internal Bootstrap Switch for the High-Side Gate Driver Stage
- Accurate Adjustable Driver Voltage with UVLO Protection
- Selectable Continuous, Pulse-Skipping, or Burst Mode Operation at Light Loads
- Programmable Output Voltage with VPRG Pin (5V or 12V)
- Current Limit Foldback during Short Fault
- Low Operating I_Q: 5µA (48V_{IN} to 5V_{OUT})
- Programmable Frequency (100kHz to 1MHz)
- Synchronizable Frequency (100kHz to 1MHz)
- Spread Spectrum Frequency Modulation
- 28-Lead (4mm × 5mm), QFN Package

APPLICATIONS

- Industrial Power Systems
- Military Avionics and Medical Systems
- Telecommunications Power Systems

GENERAL DESCRIPTION

The *ADPL®74101* is a high-performance step-down DC-to-DC controller that drives all N-channel synchronous metal-oxide-semiconductor field-effect transistor (MOSFET) power stages from input voltages up to 100V.

The ADPL74101 features an adjustable gate-drive voltage from 4V to 5.5V, ideal for driving logic-level MOSFETs.

The internal smart bootstrap switch avoids the need for an external diode. The very low no-load quiescent current extends operating runtime in battery-powered systems. The MODE pin selects among Burst Mode operation, pulse-skipping mode, or continuous inductor current mode at light loads.

The ADPL74101 additionally features spread spectrum operation, which significantly reduces the peak radiated and conducted noise on both the input and output supplies, making it easier to comply with electromagnetic interference (EMI) standards.

TYPICAL APPLICATION

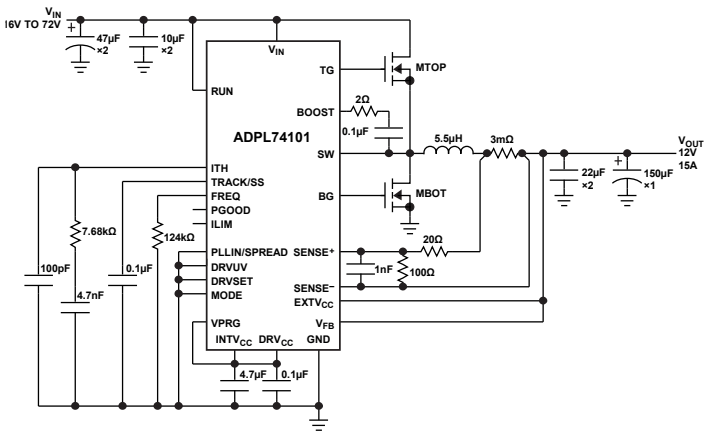


Figure 1. High Efficiency, 12V Output Buck Regulator

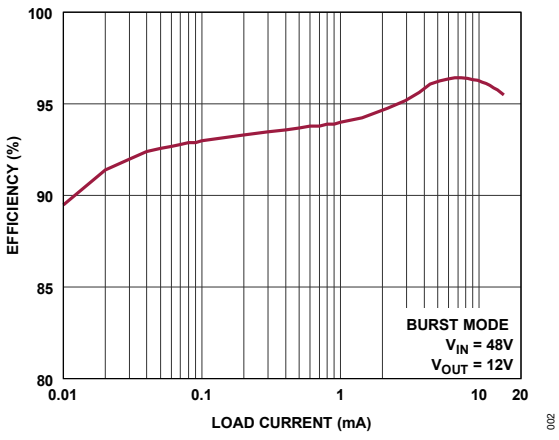


Figure 2. Efficiency for Figure 1

TABLE OF CONTENTS

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/25	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_J = -40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12V, RUN = 12V, VPRG = Floating, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Supply						
Input Supply Operating Range	V_{IN}		4		100	V
Total Input Supply Current in Regulation	I_{IN}	48V to 5V, No Load[1] 14V to 3.3V, No Load[1]		5 14		µA µA
Controller Operation						
Regulated Output Voltage Set Point	V_{OUT}		0.8		60	V
Regulated Feedback Voltage[2]	V_{FB}	V_{IN} = 4V to 100V, ITH Voltage = 0.6V to 1.2V VPRG = Floating, T_A = 25°C VPRG = Floating VPRG = 0V VPRG = $INTV_{CC}$	 0.792 0.788 4.925 11.82	 0.8 0.8 5.0 12	 0.808 0.812 5.075 12.18	 V V V V
Feedback Current[2]		VPRG = Floating, T_A = 25°C VPRG = 0V or $INTV_{CC}$, T_A = 25°C	-50	0 1	+50 2	nA µA
Feedback Overvoltage Threshold		Relative to V_{FB}, T_A = 25°C	7	10	13	%
Transconductance Amplifier[2]	g_m	ITH = 1.2V, Sink and Source Current = 5µA		1.8		mMho
Maximum Current Sense Threshold	$V_{SENSE(MAX)}$	V_{FB} = 0.7V, $SENSE^-$ = 3.3V ILIM = 0V ILIM = Floating ILIM = $INTV_{CC}$	 21 45 67	 26 50 75	 31 55 83	 mV mV mV
$SENSE^+$ Pin Current	I_{SENSE^+}	$SENSE^+$ = 3.3V, T_A = 25°C	-1		+1	µA
$SENSE^-$ Pin Current	I_{SENSE^-}	$SENSE^-$ < 3V 3.2V ≤ $SENSE^-$ < $INTV_{CC}$ – 0.5V $SENSE^-$ > $INTV_{CC}$ + 0.5V		1 75 725		µA µA µA
Soft-Start Charge Current		TRACK/SS = 0V	9.5	12	14.5	µA
RUN Pin ON Threshold		RUN Rising	1.15	1.20	1.25	V

(Specifications are at T_J = -40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12V, RUN = 12V, VPRG = Floating, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
RUN Pin Hysteresis				120		mV
DC Supply Current						
V_{IN} Shutdown Current		RUN = 0V		1		µA
V_{IN} Sleep Mode Current		$SENSE^-$ < 3.2V, $EXTV_{CC}$ = 0V		15		µA
Sleep Mode Current[3] V_{IN} Current V_{IN} Current $EXTV_{CC}$ Current $SENSE^-$ Current		 $SENSE^-$ ≥ 3.2V, $EXTV_{CC}$ = 0V $SENSE^-$ ≥ 3.2V, $EXTV_{CC}$ ≥ 4.8V $SENSE^-$ ≥ 3.2V, $EXTV_{CC}$ ≥ 4.8V $SENSE^-$ ≥ 3.2V		 5 1 6 10		 µA µA µA µA
Pulse-Skipping (PS) or Forced Continuous Mode (FCM), V_{IN} or $EXTV_{CC}$ Current[3]				2		mA
Gate Drivers						
TG or BG On-Resistance		DRVSET = $INTV_{CC}$ Pull-Up Pull-Down		 2.0 1.0		 Ω Ω
BOOST to DRV_{CC} Switch On-Resistance		DRVSET = $INTV_{CC}$		7		Ω
TG or BG Transition Time[4]		Rise Time, C_{LOAD} = 3300pF Fall Time, C_{LOAD} = 3300pF		25 15		ns ns
TG Off to BG On Delay Time[4] Synchronous Switch On-Delay Time				 20		 ns
BG Off to TG On-Delay Time[4] Top Switch On-Delay Time				 20		 ns
TG Minimum On-Time[5]	$t_{ON(MIN)}$			40		ns

(Specifications are at T_J = -40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12V, RUN = 12V, VPRG = Floating, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Maximum Duty Factor for TG		Output in dropout, V_{FREQ} = 0V		99		%
$INTV_{CC}$ Low-Dropout (LDO) Linear Regulators						
$INTV_{CC}$ Voltage for V_{IN} and $EXTV_{CC}$ LDOs		$EXTV_{CC}$ = 0V for V_{IN} LDO, $EXTV_{CC}$ = 12V for $EXTV_{CC}$ LDO DRVSET = $INTV_{CC}$ DRVSET = 0V DRVSET = 64.9kΩ	 5.2 4.8 4.5	 5.5 5.0 4.75	 5.7 5.2 5.0	 V V V
DRV_{CC} Load Regulation		DRV_{CC} load current (I_{CC}) = 0mA to 100mA, T_A = 25°C		1	3	%
Undervoltage Lockout	UVLO	DRV_{CC} Rising DRVUV = $INTV_{CC}$ DRVUV = 0V DRVUV = Floating DRV_{CC} Falling DRVUV = $INTV_{CC}$ DRVUV = 0V DRVUV = floating	 4.8 3.6 4.2 4.55 3.4 4.0	 5.0 3.8 4.4 4.75 3.6 4.18	 5.2 4.0 4.6 4.95 3.8 4.4	 V V V V V V
$EXTV_{CC}$ LDO Switchover Voltage $EXTV_{CC}$ Rising		DRVUV = $INTV_{CC}$ or Floating, T_A = 25°C DRVUV = 0V, T_A = 25°C	5.75 4.6	5.95 4.76	6.15 4.9	V V
$EXTV_{CC}$ LDO Switchover Hysteresis $EXTV_{CC}$ Falling		DRVUV = $INTV_{CC}$ or Floating DRVUV = 0V		390 220		mV mV
Spread Spectrum Oscillator and Phase-Locked Loop						
Fixed Frequencies	f_{OSC}	PLLIN/SPREAD = 0V FREQ Voltage (V_{FREQ})= 0V, T_A = 25°C FREQ = 374kΩ FREQ = 75kΩ, T_A = 25°C	 320 450	 370 100 500	 420 550	 kHz kHz kHz
Synchronizable Frequency Range	f_{SYNC}	PLLIN/SPREAD = External Clock	0.1		1	MHz
PLLIN Input High Level			2.2			V
PLLIN Input Low Level					0.5	V

(Specifications are at T_J = -40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12V, RUN = 12V, VPRG = Floating, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Spread Spectrum Frequency Range (Relative to f_{OSC})		PLLIN/SPREAD = $INTV_{CC}$ Minimum Frequency Maximum Frequency		 0 20		 % %
PGOOD Outputs						
PGOOD Voltage Low		PGOOD = 2mA, T_A = 25°C		0.2	0.4	V
PGOOD Leakage Current		PGOOD = 5V, T_A = 25°C	-1	0	+1	µA
PGOOD Trip Level (V_{FB} with Respect to Set Regulated Voltage)		T_A = 25°C V_{FB} Rising Hysteresis V_{FB} Falling Hysteresis	 7 -13 	 10 1.6 -10 1.6	 13 -7 	 % % % %
PGOOD Delay for Reporting a Fault				25		µs

1 This specification is not tested in production.

2 The ADPL74101 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

3 $SENSE^-$ bias current is reflected to the input supply by the formula $I_{VIN} = I_{SENSE^-} \times V_{OUT}/(V_{IN} \times \eta)$, where η is the efficiency.

4 Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

5 The minimum on-time condition specified for inductor peak-to-peak ripple current is >40% of the maximum load current (I_{MAX}). See the *Minimum On-Time Considerations* section for more details.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Input Supply (V_{IN})	-0.3V to 100V
RUN	-0.3V to 100V
BOOST	-0.3V to 106V
SW	-5V to 100V
BOOST to SW	-0.3V to 6V
TG[1]	Not applicable
BG[1]	Not applicable
$EXTV_{CC}$	-0.3V to 30V
DRV_{CC}, $INTV_{CC,}$ $BSTV_{CC}$	-0.3V to 6V
V_{FB}	-0.3V to 15V
PLLIN/SPREAD, FREQ	-0.3V to 6V
TRACK/SS	-0.3V to 6V
ITH	-0.3V to 6V
DRVSET, DRVUV	-0.3V to 6V
MODE, ILIM, VPRG	-0.3V to 6V
PGOOD	-0.3V to 6V
$SENSE^+$, $SENSE^-$	-0.3V to 65V
$SENSE^+$ to $SENSE^-$ Continuous	-0.3V to +0.3V
$SENSE^+$ to $SENSE^-$ <1ms	-100mA to 100mA
Operating Junction Temperature Range[2]	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

[1] Do not apply a voltage or current source to these pins. They must be connected only to capacitive loads. Otherwise, permanent damage may occur.

[2] The ADPL74101 is specified over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Electrostatic Discharge (ESD)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD Caution

	**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

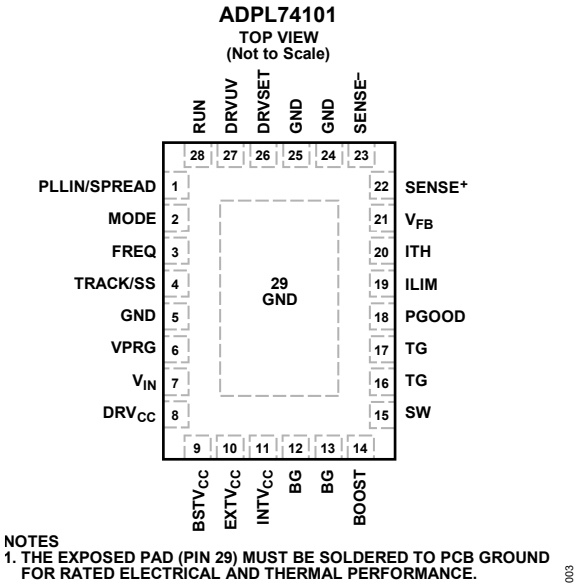


Figure 3. Pin Configuration

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	PLLIN/ SPREAD	External Synchronization Input to Phase Detector/Spread Spectrum Enable. When an external clock is applied to PLLIN/SPREAD, the phase-locked loop forces the rising TG signal to synchronize with the rising edge of the external clock. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator, or to GND to disable spread spectrum dithering.
2	MODE	Mode Select Input. This input determines how the ADPL74101 operates at light loads. Connect the MODE to GND to select the Burst Mode operation. An internal 100kΩ resistor to GND also invokes Burst Mode operation when MODE is floating. Connect MODE to $INTV_{CC}$ to force continuous inductor current operation. Tying MODE to $INTV_{CC}$ through a 100kΩ resistor selects the pulse skipping operation.
3	FREQ	Frequency Control Pin for the Internal Voltage-Controlled Oscillator (VCO). Connect FREQ to GND for a fixed frequency of 370kHz. Program frequencies between 100kHz and 1MHz by using a resistor between FREQ and GND. Minimize the capacitance on FREQ.
4	TRACK/SS	External Tracking/Soft Start Input. TRACK/SS regulates the V_{FB} voltage to the lesser of 0.8V or the voltage on the TRACK/SS pin. An internal 12µA pull-up current source is connected to TRACK/SS. A capacitor to GND at TRACK/SS sets the ramp time to the final regulated output voltage. The ramp time is equal to 1ms for every 12.5nF of capacitance. Alternatively, a resistor divider on another voltage supply connected to TRACK/SS allows the output to track the other supply during startup.
5	GND	Ground. This pin must be soldered to the printed circuit board (PCB) GND.

6	VPRG	Output Voltage Control Pin. VPRG sets the adjustable output mode using external feedback resistors or the fixed 12V or 5V output mode. Floating VPRG programs the output from 0.8V to 60V with an external resistor divider, regulating V_{FB} to 0.8V. Connect VPRG to $INTV_{CC}$ or GND to program the output to 12V or 5V, respectively, through an internal resistor divider on V_{FB}.
7	V_{IN}	Main Supply Pin. A bypass capacitor must be tied between V_{IN} and GND.
8	DRV_{CC}	Gate Driver Power Supply Pin. The gate drivers are powered from DRV_{CC}. Connect DRV_{CC} to $INTV_{CC}$ by a separate trace to the $INTV_{CC}$ bypass capacitor.
9	$BSTV_{CC}$	Bootstrap Diode Anode Connection Pin. Place an optional external Schottky diode between the $BSTV_{CC}$ and BOOST pins to bypass most of the 7Ω switch resistance between DRV_{CC} and BOOST.
10	$EXTV_{CC}$	External Power Input to an Internal LDO Regulator Connected to DRVCC. This LDO regulator supplies $INTV_{CC}$ power, bypassing the internal V_{IN} LDO regulator whenever $EXTV_{CC}$ exceeds the $EXTV_{CC}$ switchover voltage. See the $EXTV_{CC}$ connection in the *Power and Bias Supplies (VIN, EXTVCC, DRVCC, and INTVCC)* section and *INTVCC Regulators (OPTI-DRIVE)* section. Do not exceed 30 V on $EXTV_{CC}$. Connect $EXTV_{CC}$ to GND if the $EXTV_{CC}$ LDO regulator is not used.
11	$INTV_{CC}$	Output of the Internal LDO Regulator. The $INTV_{CC}$ voltage regulation point is set by the DRVSET pin. $INTV_{CC}$ must be decoupled to GND with a 4.7µF to 10µF ceramic or other low equivalent series resistance (ESR) capacitor.
12, 13	BG	High Current Gate Driver for Bottom field-effect transistor (FET). BG pulls up to DRV_{CC} and pulls down to GND. Tie the BG directly to the bottom FET gate for maximum gate drive transition speed. Tie a resistor between BG and the bottom FET gate to adjust the gate slew rate. Tie the BG pins together as close as possible.
14	BOOST	Bootstrapped Supply to the Top Side Floating Driver. Connect a capacitor between the BOOST and SW pins. An internal switch provides power to the BOOST pin from DRV_{CC} when the bottom FET turns on. The voltage swing at the BOOST pin is from DRV_{CC} to (V_{IN} + DRV_{CC}).
15	SW	Switch Node Connection to Inductor.
16, 17	TG	High Current Gate Driver for Top FET. TG pulls up to BOOST and pulls down to SW. Tie TG directly to the top FET gate for maximum gate drive transition speed. Tie a resistor between TG and the top FET gate to adjust the gate slew rate. Tie the TG pins together as close as possible.
18	PGOOD	Power Good Open-Drain Logic Output. PGOOD is pulled to GND when the voltage on V_{FB} is not within ±10% of its set point.
19	ILIM	Current Comparator Sense Voltage Range Input. Tying ILIM to GND or $INTV_{CC}$ or floating ILIM sets the maximum current sense threshold to one of three different levels (25mV, 75mV, and 50mV, respectively).
20	ITH	Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.

21	V_{FB}	Error Amplifier Feedback Input. If VPRG is floating, V_{FB} receives the remotely sensed feedback voltage from an external resistive divider across the output. If VPRG is tied to GND or $INTV_{CC}$, V_{FB} receives the remotely sensed output voltage directly.
22	$SENSE^+$	The Positive Input to the Differential Current Comparator. The ITH pin voltage and controlled offset between the $SENSE^-$ and $SENSE^+$ pins, in conjunction with the current sense resistor (R_{SENSE}), set the current trip threshold.
23	$SENSE^-$	The Negative Input to the Differential Current Comparator. The $SENSE^-$ pin supplies current to the current comparator when $SENSE^-$ is greater than $INTV_{CC}$. When the $SENSE^-$ is 3.2V or greater, the pin supplies the majority of the sleep mode quiescent current instead of V_{IN}, further reducing the input-referred quiescent current.
24, 25	GND	Ground. Connect this pin to the PCB GND.
26	DRVSET	$INTV_{CC}$ Regulation Program Pin. DRVSET sets the regulation point for the $INTV_{CC}$ LDO linear regulators. Connect DRVSET to GND to set $INTV_{CC}$ to 5V. Connect DRVSET to $INTV_{CC}$ to set $INTV_{CC}$ to 5.5V. Program voltages between 4V and 5.5V by placing a resistor (50kΩ to 110kΩ) between DRVSET and GND. The resistor and an internal 20µA source current create a voltage used by the $INTV_{CC}$ LDO regulator to set the regulation point.
27	DRVUV	DRV_{CC} UVLO and $EXTV_{CC}$ Switchover Program Pin. DRVUV determines the $INTV_{CC}$ UVLO and $EXTV_{CC}$ switchover rising and falling thresholds, as listed in *Table 1* (Electrical Characteristics table).
28	RUN	Run Control Input for the Controller. Forcing RUN below 1.08V disables controller switching. Forcing RUN below 0.7V shuts down the ADPL74101, reducing quiescent current to approximately 1µA. Tie the RUN pin to V_{IN} for always-on operation.
29	GND (EPAD)	Ground (Exposed Pad). The exposed pad must be soldered to PCB GND for rated electrical and thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

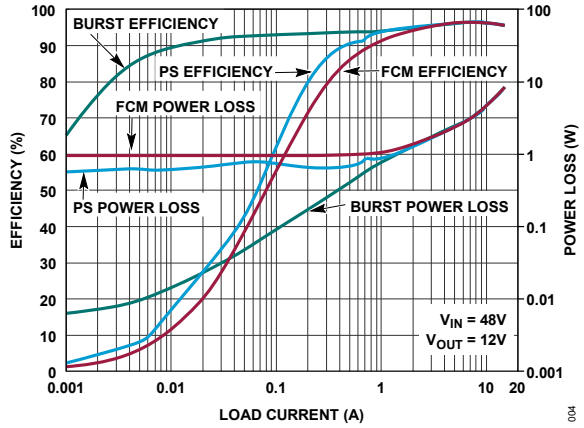


Figure 4. Efficiency and Power Loss vs. Load Current, See Figure 46 (Typical Applications) for more details

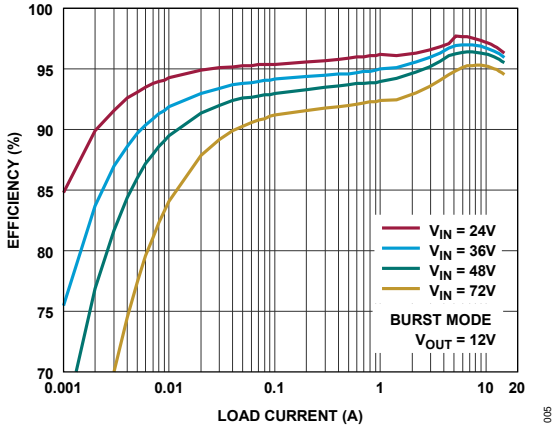


Figure 5. Efficiency vs. Load Current, See Figure 46 (Typical Applications) for more details

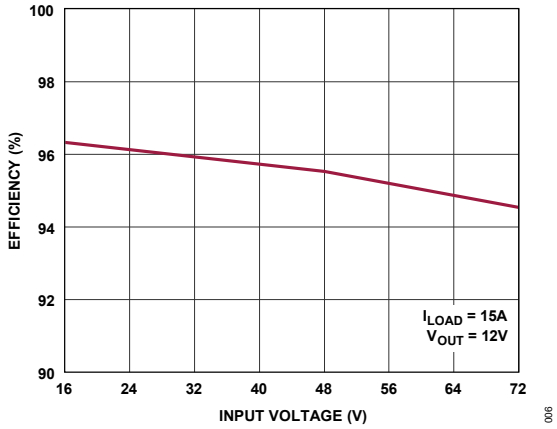


Figure 6. Efficiency vs. Input Voltage, See Figure 46 (Typical Applications) for more details

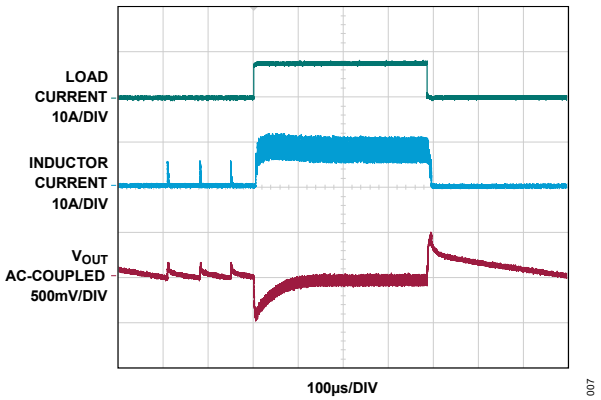


Figure 7. Load Step Burst Mode Operation, See Figure 46 (Typical Applications) for more details

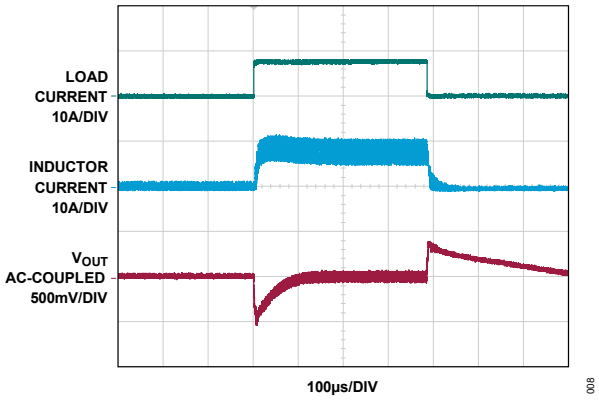


Figure 8. Load Step Pulse-Skipping Mode, See Figure 46 (Typical Applications) for more details

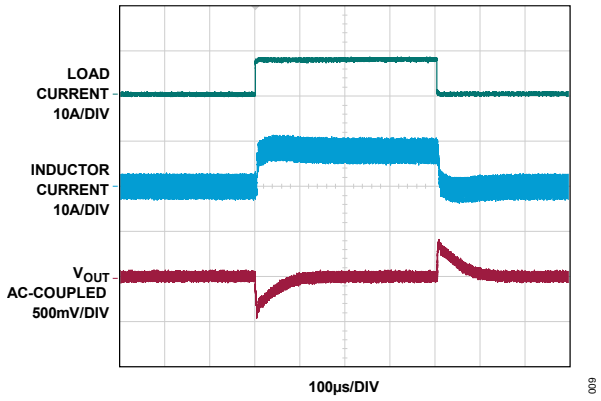


Figure 9.Load Step Forced Continuous Mode, See Figure 46 (Typical Applications) for more details

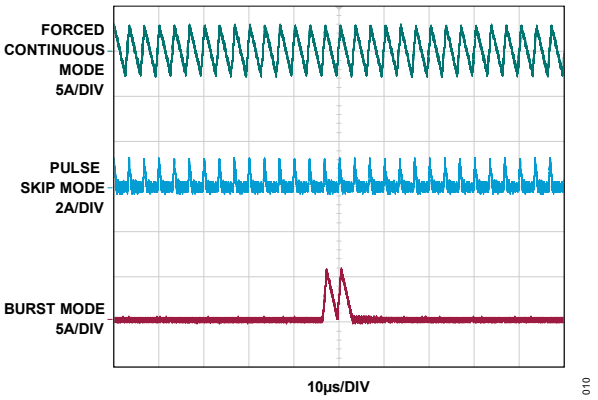


Figure 10. Inductor Current at Light Load, See Figure 46 (Typical Applications) for more details

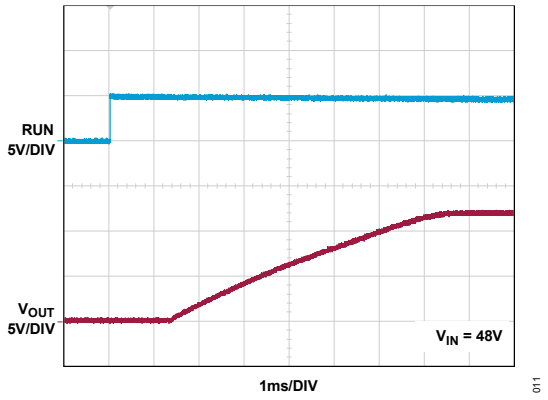


Figure 11. Soft Startup, See Figure 46 (Typical Applications) for more details

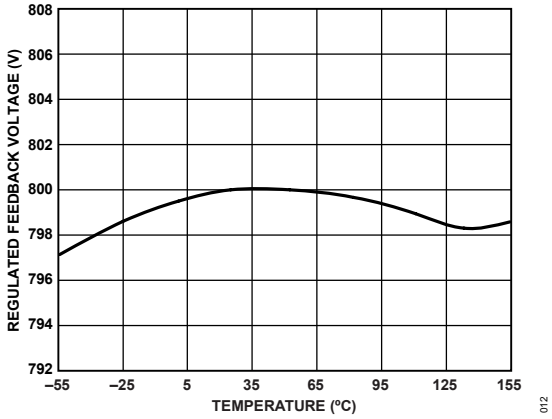


Figure 12. Regulated Feedback Voltage vs. Temperature

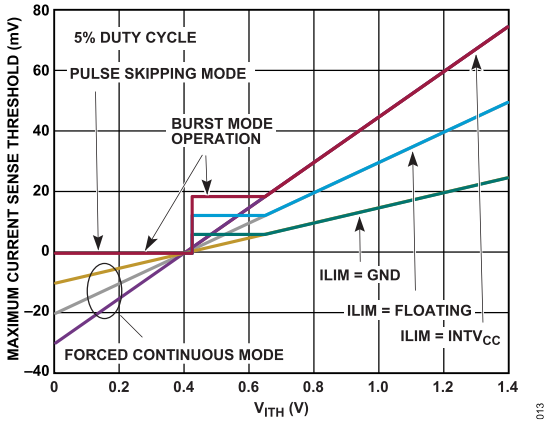


Figure 13. Maximum Current Sense Threshold vs. V_{ITH}

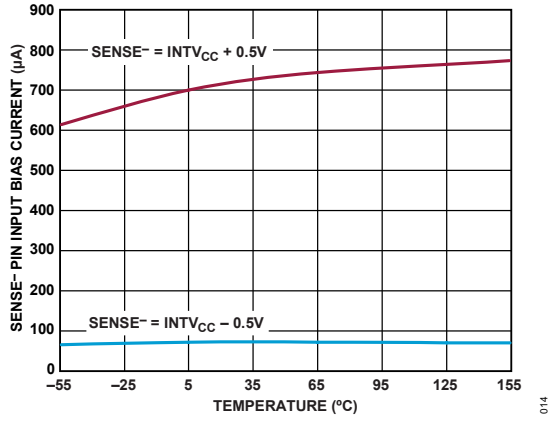


Figure 14. $SENSE^-$ Pin Input Bias Current vs. Temperature

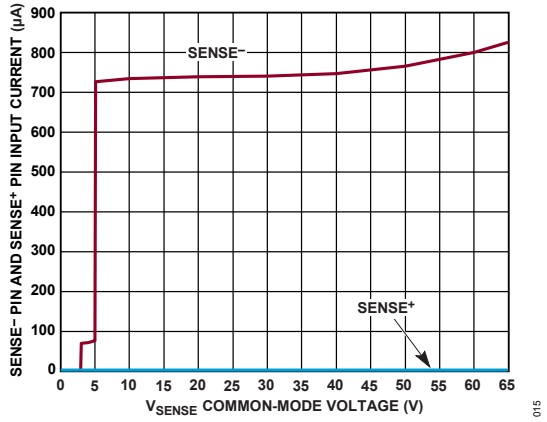


Figure 15. $SENSE^-$ Pin and $SENSE^+$ Pin Input Current vs. V_{SENSE} Common Mode Voltage

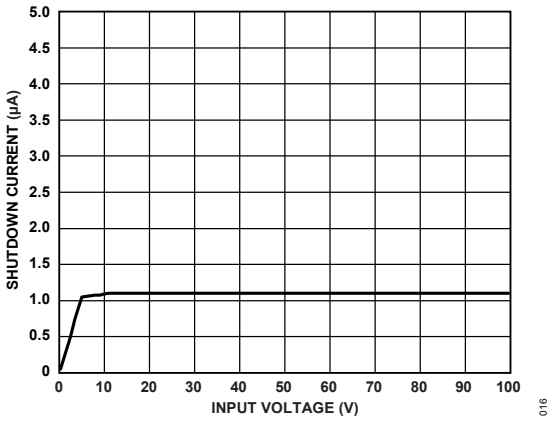


Figure 16. Shutdown Current vs. Input Voltage

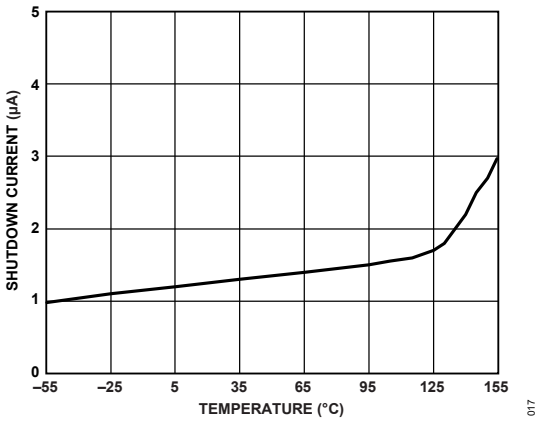


Figure 17. Shutdown Current vs. Temperature

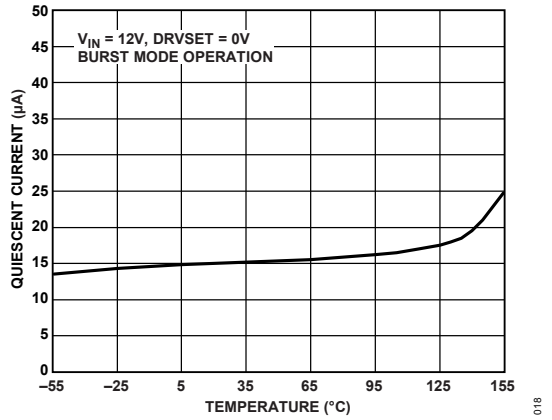


Figure 18. Quiescent Current vs. Temperature

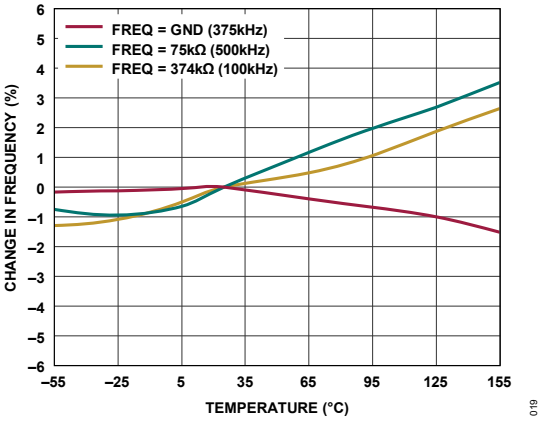


Figure 19. Oscillator Frequency vs. Temperature

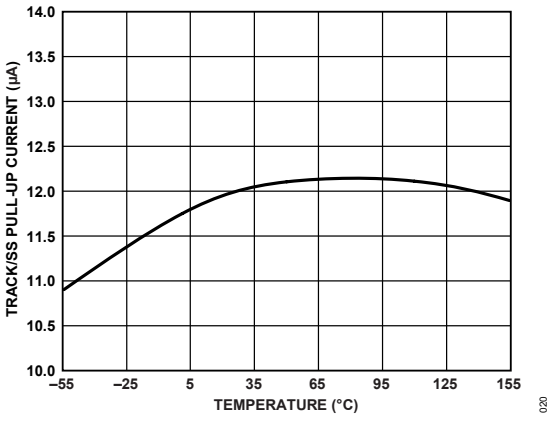


Figure 20. TRACK/SS Pull-Up Current vs. Temperature

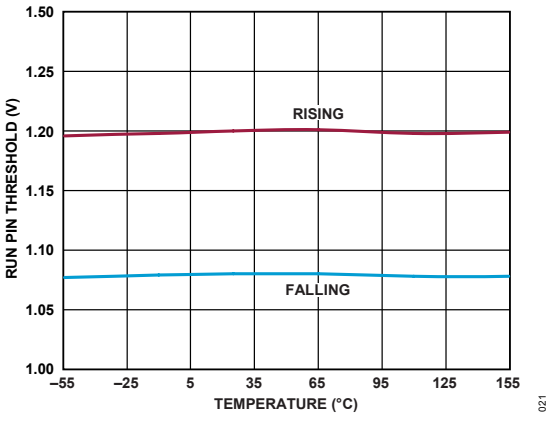


Figure 21. RUN Pin Threshold vs. Temperature

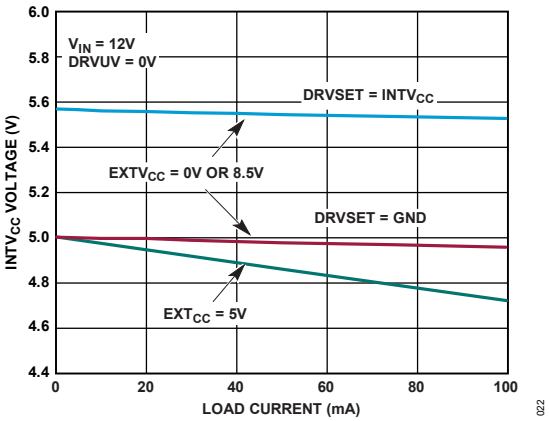


Figure 22. $INTV_{CC}$ Voltage vs. Load Current

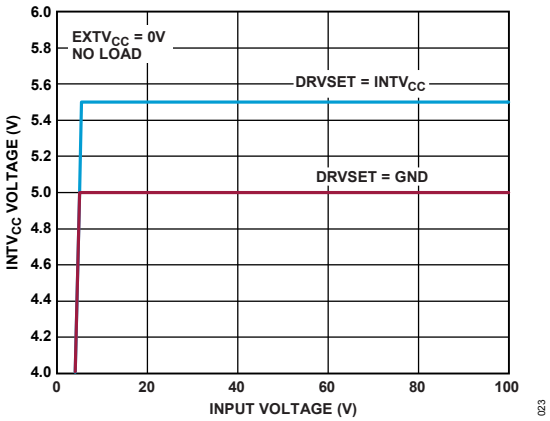


Figure 23. $INTV_{CC}$ Voltage vs. Input Voltage

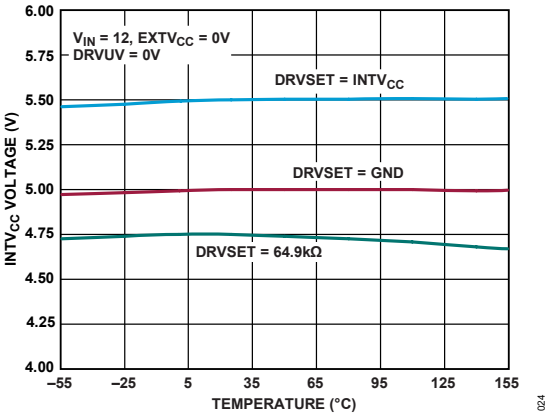


Figure 24. $INTV_{CC}$ Voltage vs. Temperature

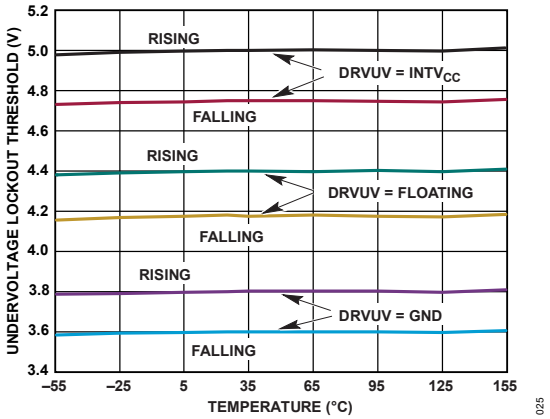


Figure 25. Undervoltage Lockout Threshold vs. Temperature

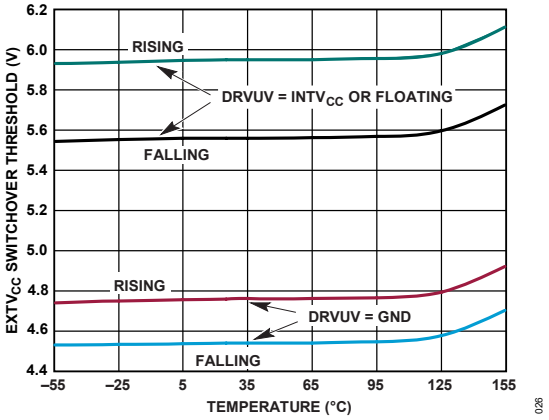


Figure 26. $EXTV_{CC}$ Switchover Threshold vs. Temperature

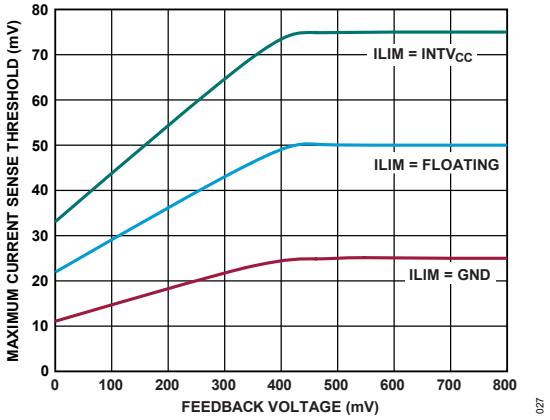
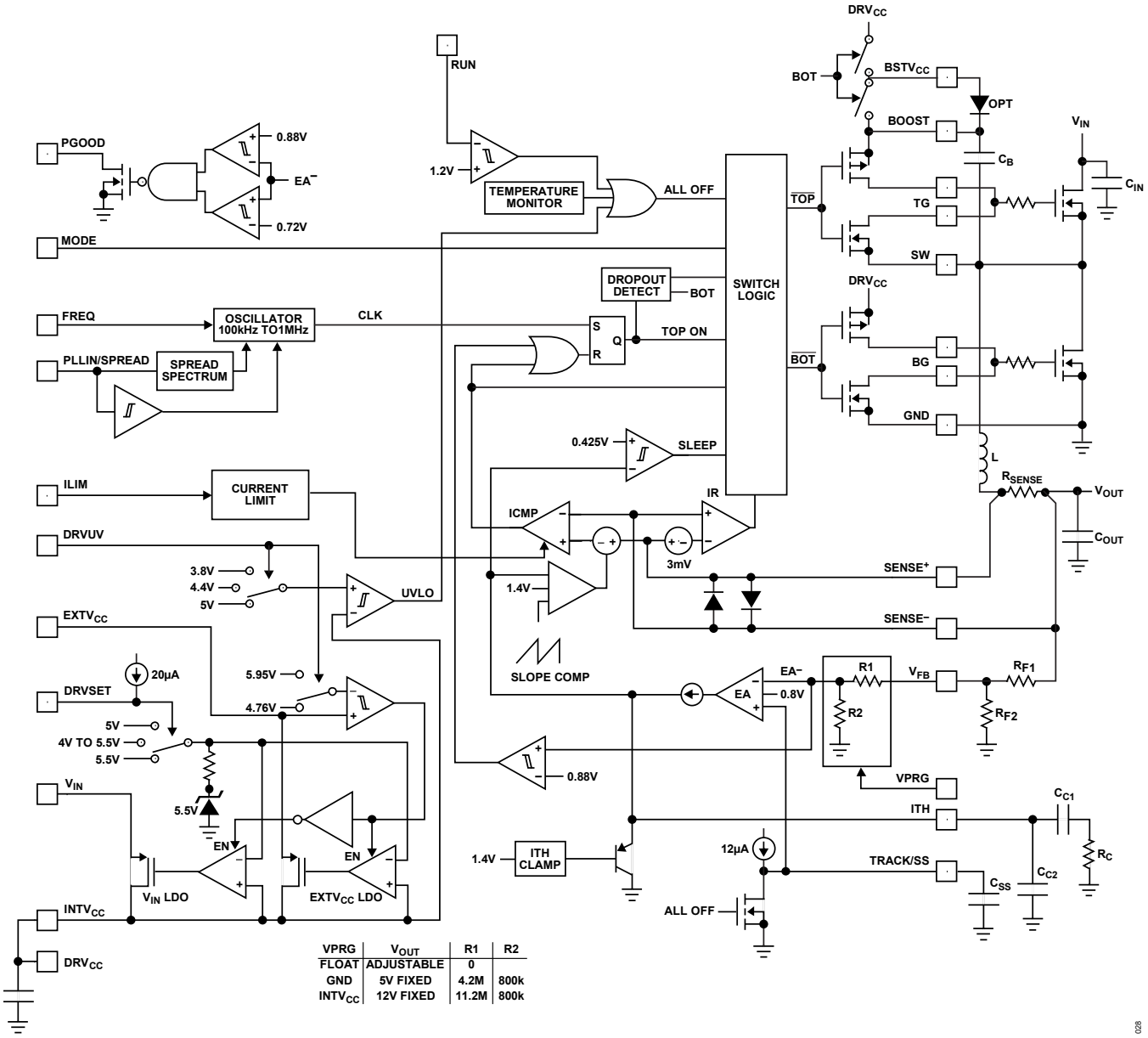


Figure 27. Maximum Current Sense Threshold vs. Feedback

FUNCTIONAL DIAGRAM



VPRG	V_{OUT}	R1	R2
FLOAT	ADJUSTABLE	0	
GND	5V FIXED	4.2M	800k
$INTV_{CC}$	12V FIXED	11.2M	800k

Figure 28. Functional Diagram

THEORY OF OPERATION

Main Control Loop

The ADPL74101 is a synchronous controller using a constant-frequency, peak-current mode architecture. During normal operation, the external top FET turns on when the clock sets the set/reset (SR) latch, causing the inductor current to increase. The main switch turns off when the main current comparator, ICMP, resets the SR latch. After the top FET is turned off each cycle, the bottom FET turns on, which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator (IR), or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the error amplifier (EA) output. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to GND) to the internal 0.8V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

Power and Bias Supplies (V_{IN}, $EXTV_{CC}$, DRV_{CC}, and $INTV_{CC}$)

The $INTV_{CC}$ pin supplies power for the top and bottom FET drivers and most of the internal circuitry. The supply for the FET drivers is derived from the DRV_{CC} pin, which must be tied to the $INTV_{CC}$ pin to supply power to the gate drivers. LDO linear regulators are available from both the V_{IN} pin and $EXTV_{CC}$ pin to provide power to $INTV_{CC}$, which can be programmed from 4V to 5.5V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage, the V_{IN} LDO regulator supplies power to $INTV_{CC}$. If $EXTV_{CC}$ is taken above its switchover voltage, the V_{IN} LDO regulator turns off, and the $EXTV_{CC}$ LDO regulator turns on. When enabled, the $EXTV_{CC}$ LDO regulator supplies power to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high-efficiency external source, such as the ADPL74101 switching regulator output.

High-Side Bootstrap Capacitor

The top FET driver is biased from the floating bootstrap capacitor (C_B), which normally recharges through an internal switch between BOOST and DRV_{CC} whenever the bottom FET turns on. The internal switch is high impedance when the bottom FET is off, preventing the bootstrap capacitor from overcharging when SW rings below GND during the dead times.

If the input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top FET continuously. The dropout detector detects this event and forces the top FET off and the bottom FET on for a short time every tenth cycle to allow C_B to recharge, resulting in a 99% duty cycle at 370kHz operation and approximately 99% duty cycle at 1MHz operation. If the bootstrap capacitor voltage falls below approximately 75% of the $INTV_{CC}$ voltage, the boost refresh pulses increase to every fourth cycle to deliver more charge to C_B, resulting in slightly lower duty cycles in dropout.

Dead Time Control

The ADPL74101 provides dead-time control, meaning the driver logic waits for the bottom FET to turn off before turning on the top FET, and vice versa. Dead-time control results in a fixed dead-time of 20ns.

Startup and Shutdown (RUN and TRACK/SS Pins)

Use the RUN pin to shut down the ADPL74101. Pulling the RUN pin below 1.08V shuts down the main control loop. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDO regulators. In this shutdown state, the ADPL74101 draws only 1µA of quiescent current.

The RUN pin needs to be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 100V (absolute maximum). Therefore, the pin can be tied to V_{IN} in always-on applications where the controller is enabled continuously and never shuts down. Additionally, a resistive divider from V_{IN} to the RUN pin can be used to set a precise input undervoltage lockout so that the power supply does not operate below a user-adjustable level.

The startup of V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than 0.8V internal reference voltage, the ADPL74101 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 0.8V reference voltage. This method allows the TRACK/SS pin to be used as a soft-start, which smoothly ramps the output voltage on startup, limiting the input supply inrush current. An external capacitor from the TRACK/SS pin to GND is charged by an internal 12µA pull-up current, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond), V_{OUT} rises smoothly from 0V to its final value.

Alternatively, the TRACK/SS pin can be used to make the startup of V_{OUT} track that of another supply. Typically, this requires connecting to the TRACK/SS pin through an external resistor divider from the other supply to GND. See the *RUN Pin and Undervoltage Lockout* section and *Soft-Start and Tracking (TRACK/SS Pin)* section for more details.

Light Load Operation: Burst Mode Operation, Pulse-Skipping, or Forced Continuous Mode (MODE Pin)

The ADPL74101 can be set to enter high-efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode at light-load currents.

To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V. An internal 100kΩ resistor to GND invokes Burst Mode operation when the MODE pin is floating, and pulse-skipping mode when the MODE pin is tied to $INTV_{CC}$ through an external 100kΩ resistor.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of its maximum value, even though the voltage on the ITH pin may indicate a lower value. If the average inductor current is higher than the load current, the EA decreases the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode), and both external FETs turn off. The ITH pin is then disconnected from the EA output, and parked at 0.45V.

In sleep mode, much of the internal circuitry turns off, reducing the quiescent current drawn by the ADPL74101 to 15µA. When V_{OUT} is 3.2V or higher, the majority of this quiescent current is supplied by the $SENSE^-$ pin, which further reduces the input-referred quiescent current by the ratio of V_{IN}/V_{OUT} multiplied by the efficiency.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, EA's output rises. When the output voltage drops enough, the ITH pin is reconnected to the EA output, the sleep signal goes low, and the controller resumes normal operation by turning on the top FET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The IR turns off the bottom FET just before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

When the MODE pin is connected for pulse skipping mode, the ADPL74101 operates in pulse-width modulation (PWM) pulse skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At light loads, ICMP can remain tripped for several cycles and force the top FET to stay off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference, as compared to Burst Mode operation. Pulse skipping mode provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Unlike forced continuous mode and pulse-skipping mode, Burst Mode operation cannot be synchronized to an external clock. Therefore, if Burst Mode operation is selected and the switching frequency is synchronized to an external clock applied to the PLLIN/SPREAD pin, the ADPL74101 switches from Burst Mode operation to forced continuous mode.

Frequency Selection, Spread Spectrum, and Phase-Locked Loop (FREQ and PLLIN/SPREAD Pins)

The free-running switching frequency of the ADPL74101 controller is selected using the FREQ pin. Tying FREQ to GND selects 370 kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 100kHz and 1MHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the ADPL74101 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency within the typical boundaries of the frequency set by the FREQ pin, and +20%.

A phase-locked loop (PLL) is available on the ADPL74101 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The PLL of the ADPL74101 aligns the turn-on of the external top FET to the rising edge of the synchronizing signal.

The PLL frequency is prebiased to the free-running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes to synchronize the rising edge of the external clock to the rising edge of TG. For faster lock-in to the external clock, use the FREQ pin to set the internal oscillator to approximately the external clock's frequency. The PLL of the ADPL74101 is guaranteed to lock to an external clock source with a frequency between 100kHz and 1MHz.

The PLLIN/SPREAD pin is transistor-transistor logic (TTL)-compatible with thresholds of 1.6V (rising) and 1.1V (falling), and is guaranteed to operate with a clock signal swing of 0.5V to 2.2V.

Output Overvoltage Protection

The ADPL74101 has an overvoltage comparator that guards against transient overshoots and other more serious conditions that can cause output overvoltage. When the V_{FB} pin rises by more than 10% above its regulation point of 0.8V, the top FET turns off, and the inductor current cannot reverse.

Foldback Current

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft start interval (as long as the V_{FB} voltage is keeping up with the TRACK/SS voltage).

Power Good

The ADPL74101 has a PGOOD pin that is connected to the open-drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} voltage is not within ±10% of the 0.8V reference. The PGOOD pin is also pulled low when the RUN pin is low (shutdown). When the V_{FB} voltage is within the ±10% requirement, the MOSFET turns off, and the pin can be pulled up by an external resistor to a source no greater than 6V, such as $INTV_{CC}$.

APPLICATIONS INFORMATION

Use Cases

Figure 1 is a simplified ADPL74101 application circuit. External component selection is largely driven by the load requirements and begins with selecting the inductor, current-sense components, operating frequency, and light-load operating mode. The remaining power stage components, consisting of the input and output capacitors and power FETs, can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, inluding soft start, biasing, and loop compensation.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of FET switching and gate charge losses. In addition to this trade-off, the effect of the inductor value on ripple current and low-current operation must also be considered. The inductor value directly affects the ripple current.

The maximum average inductor current ($I_{L(MAX)}$) is equal to the maximum output current. The peak current is equal to the average inductor current plus half of the inductor ripple current (ΔI_L), which decreases with higher inductance (L) or higher frequency (f) and increases with higher V_{IN}, as shown in Equation 1:

$$\Delta I_L = \frac{1}{f \times L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output-voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \times I_{L(MAX)}$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) cause this transition to occur at lower load currents, which can cause a dip in efficiency in the upper range of low-current operation. In Burst Mode operation, lower inductance values cause the burst frequency to decrease.

Inductor Core Selection

When the value for higher inductance (L) is known, select the type of inductor. High-efficiency regulators generally cannot afford the core loss found in low-cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is dependent on the inductance value selected. As inductance increases, core losses decrease. However, because increased inductance requires more turns of wire, copper losses increase.

Ferrite designs have low core loss and are preferred for high switching frequencies. Therefore, design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, meaning inductance collapses abruptly when the peak design current is exceeded. This collapse results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

Current Sense Selection

The ADPL74101 can be configured to use either inductor DC resistance (DCR) sensing or low-value resistor sensing. The choice between the two current-sensing schemes is a design trade-off between cost, power consumption, and accuracy. DCR sensing is popular because it saves expensive current-sensing resistors and is more power-efficient, particularly in high-current applications. However, current sensing resistors provide the most accurate current limits for the controller. The selection of other external components is driven by the load requirement and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and the inductor value.

The SENSE+ and SENSE− pins are the inputs to the current comparator. The common-mode voltage range on these pins is 0V to 65V (See the *Absolute Maximum Ratings* for more details), enabling the ADPL74101 to regulate output voltages up to a maximum of 60V. The SENSE+ pin is high impedance, drawing less than ≈1µA. This high impedance allows the current comparator to be used in inductor DCR sensing. The impedance of the SENSE− pin changes depending on the common-mode voltage. When less than $INTV_{CC}$ – 0.5 V, the SENSE− pin is at a relatively high impedance, drawing ≈1µA. When the SENSE− pin is above $INTV_{CC}$ + 0.5 V, a higher current (≈700µA) flows into the pin. Between $INTV_{CC}$ – 0.5 V and $INTV_{CC}$ + 0.5 V, the current transitions from the smaller current to the higher current. The SENSE− pin has an additional ≈70µA current when its voltage is above 3.2V to bias internal circuitry from V_{OUT} instead of V_{IN}, which reduces the input-referred supply current.

Filter components mutual to the sense lines must be placed close to the ADPL74101, and the sense lines must run close together to a Kelvin connection underneath the current sense element, as shown in *Figure 29*. Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current-sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used, as shown in *Figure 31*. The R1 resistor must be placed close to the switching node to prevent noise from coupling into sensitive small signal nodes.

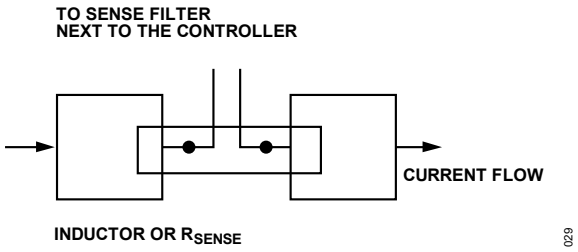


Figure 29. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

Figure 30 shows a typical sensing circuit using a discrete resistor. R_{SENSE} is chosen based on the required output current. The current comparator of the controller has a $V_{SENSE(MAX)}$ of 50mV, 25mV, or 75mV, depending on the state of the ILIM pin. The current comparator threshold voltage sets the peak inductor current.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current (ΔI_L) (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 2, as follows:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application delivers the full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ as shown in *Table 1* (Electrical Characteristics table).

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal for lower inductor values (<3µH) or higher current (>5A) applications. This error is proportional to the input voltage and can degrade line regulation or cause loop instability. Placing an RC filter (RF) into the sense pins, as shown in *Figure 30*, can be used to compensate for this error. For optimal cancellation of the ESL, set the RC filter time constant to $R_F \times C_F = ESL/R_{SENSE}$ (C_F is the filter capacitor). In general, select C_F to be in the range of 1 nF to 10 nF and calculate the corresponding R_F. Surface-mount sense resistors in low ESL, wide footprint geometries are recommended to minimize this error. If not specified in the data sheet of the manufacturer, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint, and 0.2nH for a resistor with a 1225 footprint.

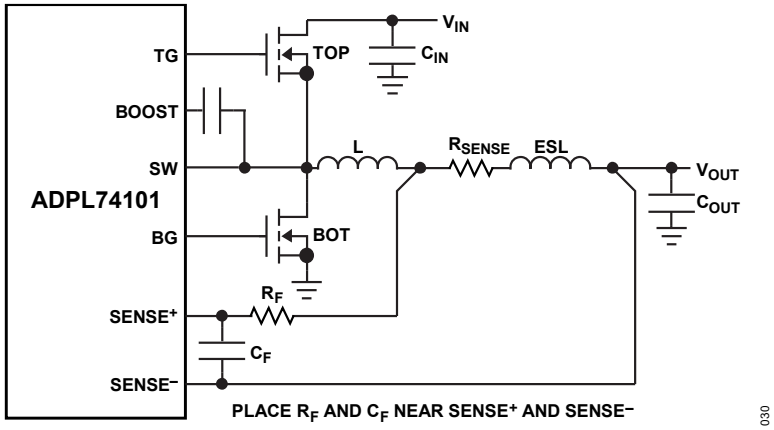


Figure 30. Using a Resistor to Sense Current

Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the ADPL74101 is capable of sensing the voltage drop across the inductor DCR, as shown in *Figure 31*. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for low-value, high-current inductors. In a high-current application requiring such an inductor, power loss through a sense resistor costs several points of efficiency compared to inductor DCR sensing.

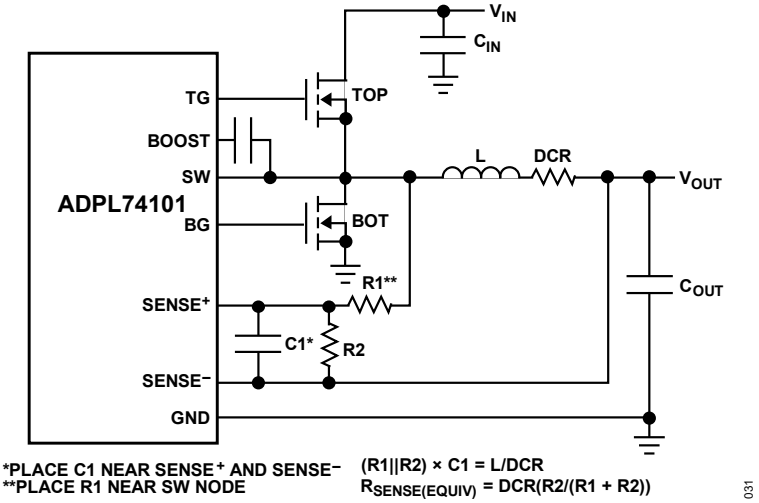


Figure 31. Using the Inductor DCR to Sense Current ($R_{SENSE(EQUIV)}$ is the Equivalent Sensed Resistance)

If the external (R1||R2) × C1 time constant is chosen to be equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1+R2). R2 scales the voltage across the sense terminals for applications where the DCR exceeds the target sense resistor value. To properly dimension the external filter components, the inductor's DCR must be known. The DCR can be measured using an inductance, capacitance, and resistance (LCR) meter. However, the DCR tolerance is not always the same and varies with temperature. Refer to the manufacturer's data sheet for detailed information.

Using $I_{L(MAX)}$ and ΔI_L (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 3, as follows:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (3)$$

To ensure that the application delivers the full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in *Table 1* (Electrical Characteristics table).

Next, determine the DCR of the inductor. When provided, use the maximum value noted by the manufacturer, typically given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C. To scale the maximum inductor DCR (DCR_{MAX}) to the desired sense resistor (R_D) value, use the divider ratio given by Equation 4, as follows:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}} \quad (4)$$

C1 is typically selected to be in the range of 0.1 µF to 0.47 µF. This range forces the equivalent resistance (R1||R2) to around 2 kΩ, reducing the error that can result from the ≈1µA current of the $SENSE^+$ pin.

R1||R2 is scaled to the room temperature inductance and maximum DCR given by Equation 5, as follows:

$$R1 \parallel R2 = \frac{L}{(DCR \text{ at } 20°C) \times C1} \quad (5)$$

The sense resistor values are given by Equation 6 and Equation 7, as follows:

$$R1 = \frac{R1 \parallel R2}{R_D} \quad (6)$$

$$R2 = \frac{R1 \times R_D}{1 - R_D} \quad (7)$$

The maximum power loss (P_{LOSS}) in R1 is related to duty cycle and occurs in continuous mode at the maximum input voltage ($V_{IN(MAX)}$) given by Equation 8, as follows:

$$P_{LOSS} \text{ in } R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{R1} \quad (8)$$

Ensure that R1 has a power rating higher than P_{LOSS} in R1. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light-load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates the need for a sense resistor, reduces conduction losses, and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Setting the Operating Frequency

Selecting the operating frequency is a trade-off between efficiency and component size. High-frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses, but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In higher voltage applications, transition losses contribute more significantly to power loss, and a proper balance between size and efficiency is achieved with a switching frequency between 300kHz and 900kHz. Lower-voltage applications benefit from lower switching losses, and can operate at switching frequencies up to 1MHz, if desired. The switching frequency is set using the FREQ and PLLIN/SPREAD pins, as shown in *Table 4*.

Table 4. Setting the Switching Frequency Using FREQ and PLLIN/SPREAD

FREQ PIN	PLLIN/SPREAD PIN	FREQUENCY
0V	0V	370kHz
Resistor to GND	0V	100kHz to 1MHz
Any of the Above	External Clock, 100kHz to 1MHz	Phase-locked to external clock
Any of the Above	$INTV_{CC}$	Spread spectrum f_{OSC} modulated 0% to +20%

Tying the FREQ pin to ground selects 370kHz. Placing a resistor between FREQ and ground allows the frequency to be programmed anywhere between 100kHz and 1MHz. Choose a FREQ pin resistor (R_{FREQ}) from *Figure 32* or Equation 9, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{f_{osc}} \quad (9)$$

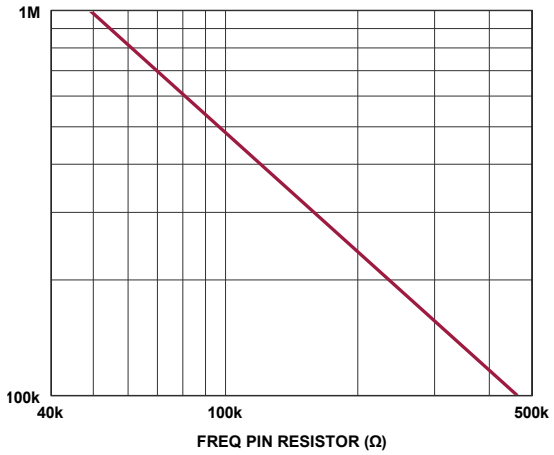


Figure 32. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

To improve EMI performance, the spread-spectrum mode can be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum mode is enabled, the switching frequency modulates around the frequency selected by the FREQ pin, and +20%. Spread-spectrum mode can be used in any operating mode selected by the MODE pin (Burst Mode, pulse-skipping, or forced continuous mode).

A PLL is also available on the ADPL74101 to synchronize the internal oscillator to an external clock source connected to the PLLIN/ SPREAD pin. After the PLL locks, TG is synchronized to the rising edge of the external clock signal. See the *Phase-Locked Loop and Frequency Synchronization* section for more details.

Selecting the Light-Load Operating Mode

The ADPL74101 can be set to enter high-efficiency Burst Mode operation, constant-frequency pulse skipping mode, or forced continuous conduction mode at light load currents. To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse skipping mode, tie the MODE pin to INTVCC through a 100kΩ resistor. An internal 100kΩ resistor from the MODE pin to GND selects Burst Mode if the pin is floating. When synchronized to an external clock via the PLLIN/SPREAD pin, the ADPL74101 operates in pulse-skipping mode when selected. Otherwise, the ADPL74101 operates in forced continuous mode.

Table 5 summarizes the use of the MODE pin to select the light load operating mode.

Table 5. Using the MODE Pin to Select Light Load Operating Mode

MODE PIN	LIGHT-LOAD OPERATING MODE	MODE WHEN SYNCHRONIZED
0V or Floating	Burst Mode	Forced Continuous
100kΩ to $INTV_{CC}$	Pulse-Skipping	Pulse-Skipping
$INTV_{CC}$	Forced Continuous	Forced Continuous

The requirements of each application dictate the appropriate choice for the light-load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom FET before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the regulator operates in discontinuous operation. In addition, when the load current is light, the inductor current begins bursting at frequencies lower than the switching frequency and enters a low current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light loads.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of the load. In this mode, the efficiency at light loads is considerably lower than in Burst Mode operation. However, continuous operation has the advantage of lower output-voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

In pulse-skipping mode, constant-frequency operation is maintained down to approximately 1% of the designed maximum output current. At very light loads, the PWM comparator can remain tripped for several cycles and force the top FET to remain off for the same number of cycles (skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple, low audio noise, and reduced RF interference compared to Burst Mode operation. Pulse skipping mode provides higher light-load efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. Consequently, pulse-skipping mode represents a compromise between light-load efficiency, output ripple, and EMI.

In some applications, it may be desirable to change the light load operating mode based on the conditions present in the system. For example, if a system is inactive, the user can select high-efficiency Burst Mode operation by keeping the MODE pin set to 0V. When the system wakes, the user can send an external clock to PLLIN/ SPREAD, or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. These on-the-fly mode changes can allow an individual application to benefit from the advantages of each light load operating mode.

Dead Time Control

The ADPL74101 uses dead time control. The dead time is measured between one FET turning off and the other FET turning on. The delay between BG and TG transitions is fixed to approximately 20 ns.

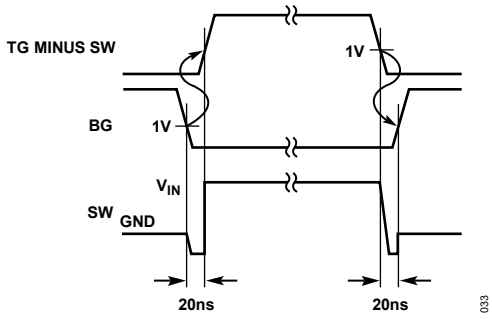


Figure 33. Dead Time Control

Power FET Selection

Two external power FETs must be selected for the ADPL74101: one N-channel FET for the top (main) switch and one N-channel FET for the bottom (synchronous) switch. The peak-to-peak gate drive levels are set by the $INTV_{CC}$ regulation point (4V to 5.5V). For silicon MOSFETs, logic-level threshold MOSFETs are required in most applications. Pay close attention to the breakdown voltage (BVD_{SS}) specification for the FETs as well.

Selection criteria for the power FETs include the on resistance ($R_{DS(ON)}$), Miller capacitance (C_{MILLER}), input voltage, and maximum output current. C_{MILLER} can be approximated from the gate-charge curve typically provided in the data sheet of the FET manufacturer. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat, divided by the specified change in the voltage difference between the drain and source terminals of the MOSFET (V_{DS}). This result is then multiplied by the ratio of the application applied V_{DS} to the gate-charge-curve specified V_{DS}. When the device is operating in continuous mode, the duty cycles for the top and bottom FETs are given by Equation 10 and Equation 11, as follows:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}} \tag{10}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}-V_{OUT}}{V_{IN}} \tag{11}$$

The FET power dissipation at maximum output current is given by Equation 12 and Equation 13, as follows:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2 \times (1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right) \times (R_{DR})(C_{MILLER}) \times \left(\frac{1}{V_{INTVCC}-V_{THMIN}} + \frac{1}{V_{THMIN}}\right)(f) \tag{12}$$

$$P_{SYNC} = \frac{V_{IN}-V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} \tag{13}$$

where:

P_{MAIN} is the power dissipation from the main switch.
δ is the temperature dependency of $R_{DS(ON)}$ ($\delta \approx 0.005$/°C).
R_{DR} is the effective driver resistance at the FET's Miller threshold voltage ($R_{DR} \approx 2\Omega$).
V_{INTVCC} is the $INTV_{CC}$ voltage.
V_{THMIN} is the typical FET minimum threshold voltage.
P_{SYNC} is the power dissipation from the synchronous switch.

Both FETs have I^2R losses (I^2R is the power loss equation of the FETs), whereas the main N-channel equations include an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20 V, the high-current efficiency generally improves with larger FETs. However, for V_{IN} > 20 V, the transition losses rapidly increase, so that using a higher $R_{DS(ON)}$ device with lower C_{MILLER} provides higher efficiency. The synchronous FET losses are greatest at high input voltage when the top switch duty factor is low, or during a short circuit when the synchronous switch is on close to 100% of the period.

C_{IN} and C_{OUT} Selection

The selection of the input capacitance (CIN) is usually based on the worst-case rms current drawn through the input network (battery, fuse, or capacitor). The highest $V_{OUT} \times I_{OUT}$ product needs to be used in Equation 14 to determine the maximum rms capacitor current requirement.

In continuous mode, the source current of the top FET is a square wave with a duty cycle of V_{OUT}/V_{IN}. To prevent large voltage transients, use a low effective series resistance (ESR) capacitor sized for the maximum rms current (I_{RMS}). At IMAX, the maximum rms capacitor current is given by Equation 14, as follows:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}((V_{OUT})(V_{IN} - V_{OUT}))^{1/2} \quad (14)$$

Equation 14 has a maximum at V_{IN} = 2 V_{OUT}, where $I_{RMS} = I_{OUT/2}$ (I_{OUT} is the output current). This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the ripple current ratings of capacitor manufacturers are often based on only 2000 hours of life. This basis makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors can be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the ADPL74101, ceramic capacitors can also be used for C_{IN}. Consult the manufacturer if there are any questions.

Placing a small (0.1µF to 1µF) bypass capacitor between the ADPL74101 V_{IN} pin and GND, close to the ADPL74101, is also recommended. An optional 1Ω to 10Ω resistor placed between CIN and the V_{IN} pin provides further isolation from a noisy input supply.

The selection of the output capacitance (C_{OUT}) is driven by the ESR. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by Equation 15, as follows:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8fC_{OUT}}\right) \quad (15)$$

where:
f is the operating frequency.
ΔI_L is the ripple current in the inductor.

The output ripple is highest at the maximum input voltage because ΔI_L increases with the input voltage.

Setting the Output Voltage

The ADPL74101 output voltages are set by an external feedback resistor divider carefully placed across the output, as shown in *Figure 34* and *Figure 35*. The regulated output voltage is determined by Equation 16, as follows:

$$V_{OUT} = 0.8V(1 + \frac{R_B}{R_A}) \quad (16)$$

Place the R_A and R_B resistors close to the V_{FB} pin to minimize PCB trace length and noise on the sensitive V_{FB} node. Take care to route the V_{FB} trace away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feedforward capacitor (C_{FF}) can be used.

The ADPL74101 can be programmed to a fixed 12V or 5V output via the VPRG pin. *Figure 35* shows how the V_{FB} pin is used to sense the output voltage in fixed output mode. Tying VPRG to $INTV_{CC}$ or GND programs, V_{OUT} to 12V or 5V, respectively. Floating VPRG sets V_{OUT} to an adjustable output mode using external resistors.

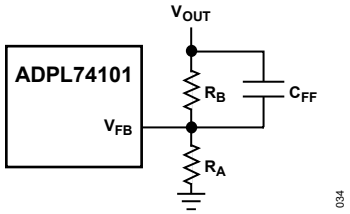


Figure 34. Setting Adjustable Output Voltage

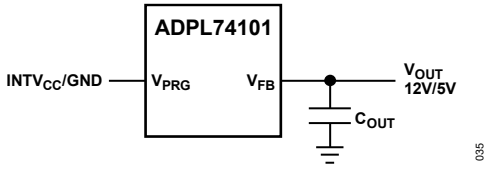


Figure 35. Setting Fixed 12V or 5V Output Voltage

RUN Pin and Undervoltage Lockout

The ADPL74101 is enabled using the RUN pin. The RUN pin has a rising threshold of 1.2V with 100mV of hysteresis. Pulling the RUN pin below 1.08V shuts down the main control loop and resets the soft-start. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDO regulators. In this state, the ADPL74101 draws only ≈1µA of quiescent current.

The RUN pin is high impedance; it must be externally pulled up or pulled down, and is driven directly by logic. The RUN pin can tolerate up to 100V (the absolute maximum). Therefore, the pin can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shuts down. Do not float the RUN pin.

The RUN pin can also be configured as a precise UVLO on the input supply with a resistor divider from V_{IN} to GND, as shown in *Figure 36*.

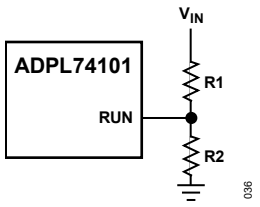


Figure 36. Using the Run Pin as UVLO

The V_{IN} UVLO thresholds can be computed by Equation 17 and Equation 18, as follows:

$$\text{UVLO RISING} = 1.2\text{V}(1 + \frac{\text{R1}}{\text{R2}}) \quad (17)$$

$$\text{UVLO FALLING} = 1.08\text{V}(1 + \frac{\text{R1}}{\text{R2}}) \quad (18)$$

The current that flows through the R1 and R2 divider adds to the shutdown, sleep, and active current of the ADPL74101. Ensure to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range can be required to keep the impact on quiescent shutdown and sleep currents low.

Soft-Start and Tracking (TRACK/SS Pin)

The startup of V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 0.8 V reference, the ADPL74101 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin instead of the internal reference. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during startup.

Soft start is enabled by connecting a capacitor from the TRACK/SS pin to GND. An internal 12µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The ADPL74101 regulates its feedback voltage (and therefore V_{OUT}) based on the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. For a desired soft start time (t_{SS}), select a soft start capacitor (C_{SS}) = t_{SS} × 15nF/ms.

Alternatively, the TRACK/SS pin can be used to track another supply during startup, as shown qualitatively in *Figure 37* and *Figure 38*. To track another supply, connect a resistor divider from the leader supply (V_X) to the TRACK/SS pin of the follower supply (V_{OUT}), as shown in *Figure 39*. During startup, V_{OUT} tracks V_X, according to the ratio set by the resistor divider in Equation 19:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \times \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B} \quad (19)$$

Set $R_{TRACKA} = R_A$ and $R_{TRACKB} = R_B$ for coincident tracking ($V_{OUT} = V_X$ during startup).

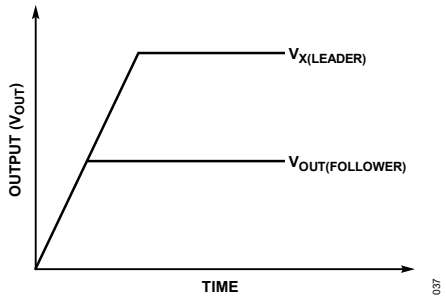


Figure 37. Coincident Tracking

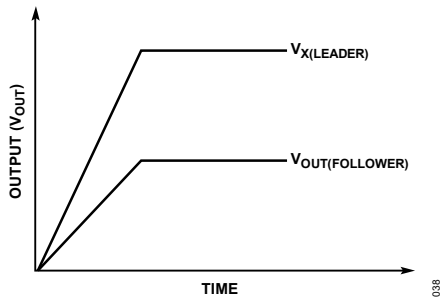


Figure 38. Ratiometric Tracking

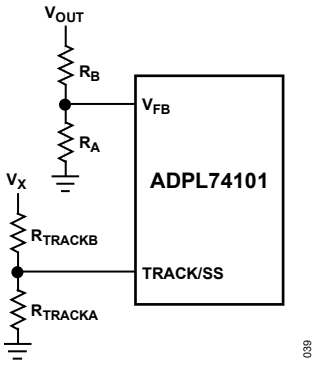


Figure 39. Using the TRACK/SS Pin for Tracking

INTVCC Regulators (OPTI-DRIVE)

The ADPL74101 features two separate internal LDO linear regulators that supply power at the $INTV_{CC}$ pin from either the V_{IN} pin or the $EXTV_{CC}$ pin, depending on the $EXTV_{CC}$ pin voltage and connections to the DRVSET and DRVUV pins. The DRV_{CC} pin is the supply pin for the FET gate drivers and must be connected to the $INTV_{CC}$ pin. The V_{IN} LDO regulator and the $EXTV_{CC}$ LDO regulator regulate $INTV_{CC}$ between 4 V and 5.5 V, depending on how the DRVSET pin is set. Each LDO regulator can provide a peak current of at least 100mA.

Bypass the $INTV_{CC}$ pin to GND with a minimum of 4.7µF ceramic capacitor, and place it as close as possible to the pin. It is recommended to place an additional 1µF ceramic capacitor between the DRV_{CC} pin and the GND pin to supply the high-frequency transient currents required by the FET gate drivers.

The DRVSET pin programs the $INTV_{CC}$ supply voltage, and the DRVUV pin selects the different $INTV_{CC}$ UVLO and $EXTV_{CC}$ switchover threshold voltages. *Table 6* summarizes the different DRVSET pin configurations and the corresponding voltage settings for each configuration. *Table 7* summarizes the different DRVUV pin configurations and voltage settings. Tying the DRVSET pin to $INTV_{CC}$ programs $INTV_{CC}$ to 5.5V. Tying the DRVSET pin to GND programs $INTV_{CC}$ to 5.0V. Place a 43kΩ to 100kΩ resistor between DRVSET and GND to program the $INTV_{CC}$ voltage between 4V to 5.5V, as shown in *Figure 40*.

Table 6. *DRVSET Pin Configurations and Voltage Settings*

DRVSET PIN	$INTV_{CC}$ VOLTAGE (V)
GND	5.0
$INTV_{CC}$	5.5
Resistor to GND 43kΩ to 100kΩ	4 to 5.5

Table 7. DRVUV Pin Configurations and Voltage Settings

DRVUV PIN	$INTV_{CC}$ UVLO RISING and FALLING THRESHOLDS (V)	$EXTV_{CC}$ SWITCHOVER RISING and FALLING THRESHOLDS (V)
GND	3.8 and 3.6	4.76 and 4.54
Floating	4.4 and 4.18	5.95 and 5.56
$INTV_{CC}$	5 and 4.75	5.95 and 5.56

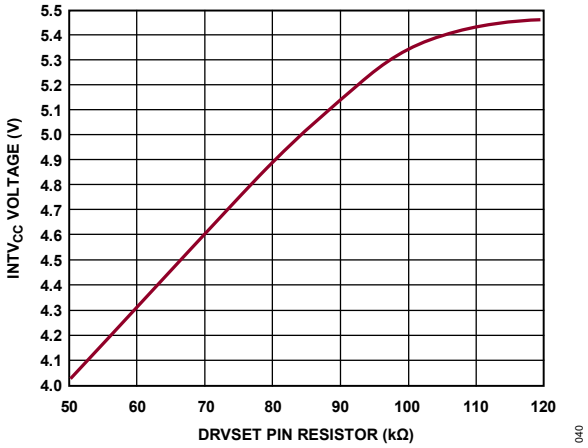


Figure 40. Relationship Between $INTV_{CC}$ Voltage and Resistor Value at the DRVSET Pin

High-input-voltage applications in which large FETs are driven at high frequencies can exceed the maximum junction temperature rating for the ADPL74101. The $INTV_{CC}$ current, which is dominated by the gate charge current, can be supplied by either the V_{IN} LDO regulator or the $EXTV_{CC}$ LDO regulator. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.76V or 5.95V, as determined by the DRVUV pin), the V_{IN} LDO regulator is enabled. In this case, power dissipation for the IC is equal to V_{IN} × $INTV_{CC}$ current (I_{INTVCC}). The gate charge current is dependent on the operating frequency, as discussed in the *Efficiency Considerations* section. To estimate the junction temperature, use the equation detailed in *Table 2*. For example, the ADPL74101 $INTV_{CC}$ current is limited to less than 36mA from a 36V supply when not using the $EXTV_{CC}$ supply at an ambient temperature of 70°C, as shown in Equation 20:

$$T_J = 70°C + (36mA)(36V)(43°C/W) = 125°C \quad (20)$$

To prevent the maximum junction temperature from exceeding, check the input supply current while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ exceeds its rising switchover threshold, the V_{IN} LDO regulator turns off, and the $EXTV_{CC}$ LDO regulator enables. The $EXTV_{CC}$ LDO regulator remains on as long as the voltage applied to $EXTV_{CC}$ remains above its falling switchover threshold. The $EXTV_{CC}$ LDO regulator attempts to regulate the $INTV_{CC}$ voltage to the voltage as programmed by the DRVSET pin. Therefore, while $EXTV_{CC}$ is less than 5V, the LDO regulator is in dropout, and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ exceeds the programmed voltage (up to an absolute maximum of 30V), $INTV_{CC}$ is regulated to the programmed voltage. Using the $EXTV_{CC}$ LDO regulator allows the FET driver and control power to be derived from the switching regulator output of the ADPL74101 ($4.7V \le V_{OUT} \le 30V$) during normal operation, and from the V_{IN} LDO regulator when the output is out of regulation (for example, during startup or short-circuit). If more current is required through the $EXTV_{CC}$ LDO regulator than is specified, add an external Schottky diode between the $EXTV_{CC}$ and $INTV_{CC}$ pins. In this case, do not apply more than 6V to the $EXTV_{CC}$ pin.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from an output, because the V_{IN} current resulting from the driver and control currents is scaled by a factor of $V_{OUT}/(V_{IN}$ × efficiency). For 5V to 30V regulator outputs, connect the $EXTV_{CC}$ pin to V_{OUT}. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature as shown in Equation 20 from 125°C to the results given by Equation 21, as follows:

$$T_J = 70°C + (36mA)(8.5V)(43°C/W) = 83°C \quad (21)$$

However, for 3.3V and other low-voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This connection causes the internal V_{IN} LDO regulator to power $INTV_{CC}$, resulting in an efficiency penalty of up to 10% or more at high input voltages.
2. $EXTV_{CC}$ is connected directly to the regulator output. This connection is the normal connection for an application with an output range of 5V to 30V and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available, it can be used to power $EXTV_{CC}$, provided that it is compatible with the FET gate drive requirements. This supply can be higher or lower than V_{IN}. However, a lower $EXTV_{CC}$ voltage results in higher efficiency.
4. $EXTV_{CC}$ connected to an output-derived boost or charge pump. For regulators with outputs below 5V, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that is boosted above the $EXTV_{CC}$ switchover threshold.

Topside FET Driver Supply (C_B)

An external bootstrap capacitor (C_B) connected to the BOOST pin supplies the gate drive voltage for the topside FET. C_B in *Figure 28* (Functional Diagram) is charged via an internal switch from DRV_{CC} when the SW pin is low, and the bottom FET is turned on. The on-resistance of the internal switch is approximately 7Ω. To deliver more charge current to C_B under certain operating conditions, place an external Schottky diode between $BSTV_{CC}$ and BOOST to bypass most of the internal switch resistance between DRV_{CC} and BOOST.

When the topside FET turns on, the driver places the C_B voltage across the gate source of the desired FET, which enhances the FET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN}, and the BOOST pin follows. With the topside FET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of C_B must be 100 times the total input capacitance of the topside FETs. For a typical application, a value of $C_B = 0.1\mu F$ is sufficient.

Minimum On-Time Considerations

The minimum on time ($t_{ON(MIN)}$) is the smallest time duration that the ADPL74101 is capable of turning on the top FET. $t_{ON(MIN)}$ is determined by internal timing delays and the gate charge required to turn on the FET. Low-duty-cycle applications can approach this minimum on time limit. Take care to ensure the results in Equation 22, as follows:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \times f} \quad (22)$$

If the duty cycle falls below the minimum on-time requirement, the controller begins to skip cycles. The output voltage continues to be regulated, but the ripple voltage and current increases. The minimum on-time for the ADPL74101 is approximately 40ns. However, as the peak sense voltage decreases, the minimum on time gradually increases to about 60ns. This change is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, significant cycle skipping can occur with correspondingly larger current and voltage ripple.

Fault Conditions: Current Limit and Foldback

The ADPL74101 includes current foldback to reduce the load current when the output is shorted to GND. If the output voltage falls below 70% of its regulation point, the maximum sense voltage is progressively lowered from 100% to 40% of its maximum value. Under short-circuit conditions with low duty cycles, the ADPL74101 begins cycle skipping to limit the short-circuit current. In this situation, the bottom FET dissipates most of the power, but less than in normal operation. The short-circuit ripple current ($\Delta I_{L(SC)}$) is determined by $t_{ON(MIN)} \approx 40ns$, the input voltage, and the inductor value given by Equation 23, as follows:

$$\Delta I_L = t_{ON(MIN)} \times \frac{V_{IN}}{L} \quad (23)$$

The resulting average short-circuit current (I_{SC}) is given by Equation 24, as follows:

$$I_{SC} = 40\% \times I_{LIM(MAX)} - \frac{\Delta I_{L(SC)}}{2} \quad (24)$$

where $I_{LIM(MAX)}$ is the maximum peak inductor current.

Fault Conditions: Overvoltage Protection

If the output voltage rises 10% above the set regulation point, the top FET turns off, and the inductor current is not allowed to reverse until the overvoltage condition clears.

Fault Conditions: Overtemperature Protection

At higher temperatures or when the internal power dissipation causes excessive self-heating (for example: a short from $INTV_{CC}$ to GND), the internal overtemperature shutdown circuitry shuts down the ADPL74101. When the internal die temperature exceeds 180°C, the $INTV_{CC}$ LDO regulator and gate drivers disable. When the die cools to 160°C, the ADPL74101 enables the $INTV_{CC}$ LDO regulator and resumes operation, starting with a soft-start startup. Avoid long-term overstress ($T_J > 125°C$) because it can degrade the device performance or shorten the device life.

Phase-Locked Loop and Frequency Synchronization

The ADPL74101 has an internal PLL that allows the turn-on of the top FET to be synchronized to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase lock and synchronization. Although it is not required, placing the free-running frequency near the external clock frequency prevents the oscillator from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the ADPL74101 operates in pulse-skipping mode when the MODE pin is selected, or in forced continuous mode otherwise. The ADPL74101 is guaranteed to synchronize to an external clock applied to the PLLIN/SPREAD pin that swings up to at least 2.2V and down to 0.5V or less. Note that the ADPL74101 can only be synchronized to an external clock frequency between 100kHz to 1MHz.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Analyzing individual losses is useful for determining what is limiting the efficiency and which change produces the most improvement. The percent efficiency can be expressed by Equation 25, as follows:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + \ldots) \quad (25)$$

where L1, L2, L3, and so on, are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in ADPL74101 circuits: IC V_{IN} current, $INTV_{CC}$ regulator current, I^2R losses, and topside FET transition losses.

The V_{IN} current is the DC supply current given in *Table 1* (Electrical Characteristics table), excluding the FET driver and control currents. Other than at light loads in Burst Mode operation, V_{IN} current typically results in a small (<0.1%) loss.

The $INTV_{CC}$ current is the sum of the FET driver and control currents. The FET driver current results from switching the gate capacitance of the power FETs. Each time a FET gate switches from low to high and back to low again, a packet of charge (dQ) moves from $INTV_{CC}$ to GND. The resulting dQ/time duration (dt) is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, gate charge current ($I_{GATECHG}$) = SW frequency (f_{SW})(Q_T + Q_B), where Q_T and Q_B are the gate charges of the top and bottom FETs.

Supplying $INTV_{CC}$ from an output-derived source through $EXTV_{CC}$ scales the V_{IN} current required for the driver and control circuits by a factor of $V_{OUT}/(V_{IN} \times \text{efficiency})$. For example, in a 20V to 5V application, 10 mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This result reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

I^2R losses are predicted from the DC resistances of the input fuse (if used), FET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode, the average output current flows through L and R_{SENSE}, but is chopped between the top and bottom FETs. If the two FETs have approximately the same $R_{DS(ON)}$, the resistance of one FET can be summed with the resistances of L, R_{SENSE}, and ESR to obtain the I^2R losses.

For example, if each $R_{DS(ON)}$ = 30mΩ, R_L = 50mΩ, R_{SENSE} = 10mΩ, and ESR = 40mΩ (the sum of both input and output capacitance losses), the total resistance is 130mΩ. The resulting losses range from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high-performance digital systems are not doubling, but quadrupling the importance of loss terms in the switching regulator system.

Transition losses apply only to the top FETs and become significant only when operating at higher input voltages (typically 15V or greater). Transition losses can be estimated using Equation 26, as follows:

$$\text{TRANSITION LOSS} = (1.7)(V_{IN})^2 \times I_{L(MAX)} \times C_{RSS} \times f_{SW} \quad (26)$$

where C_{RSS} is the reverse transfer capacitance.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional 5% to 10% efficiency degradation in portable systems. It is important to include these system-level losses during the design phase. The internal battery and fuse resistance losses can be minimized by ensuring that C_{IN} has adequate charge storage and a low ESR at the switching frequency. A 25W supply typically requires a minimum of 20µF to 40µF of capacitance with a maximum ESR of 20mΩ to 50mΩ. Other losses, including inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

To check the regulator loop response, examine the load current transient response. Switching regulators take several cycles to respond to a step in the DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charging or discharging C_{OUT}, generating a feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which indicates a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The dc step, rise time, and settling at this test point reflect the closed-loop response. Assuming a predominantly second-order system, the phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components that are shown in *Figure 1*, *Figure 42*, *Figure 44*, and *Figure 46* provide an adequate starting point for most applications.

The ITH series compensation resistor (R_C) to compensation capacitor (C_C) filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 times to 2 times their initial values) to optimize the transient response when the final PCB layout is done, and the particular output capacitor type and value are determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of the full load current, with a rise time of 1µs to 10µs, produces output voltage and ITH pin waveforms that give a sense of the overall loop stability without breaking the feedback loop.

Placing a power FET directly across from the output capacitor, and driving the gate with an appropriate signal generator, is a practical way to produce a realistic load-step condition. The initial output-voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop. Therefore, this signal cannot be used to determine phase margin. For this reason, it is better to look at the ITH pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop increases by increasing R_C, and the bandwidth of the loop increases by decreasing C_C. If R_C increases by the same factor as C_C decreases, the zero frequency remains unchanged, keeping the phase shift the same in the most critical frequency range of the feedback loop. The output-voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage, if the load switch resistance is low and it is driven quickly.

If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time must be controlled so that the load rise time is limited to approximately $C_{LOAD} \times 25\mu s/\mu F$. Therefore, a 10µF capacitor requires a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume the nominal input voltage ($V_{IN(NOMINAL)}$) = 12V, $V_{IN(MAX)}$ = 22V, V_{OUT} = 3.3V, I_{OUT} = 20A, and f_{SW} = 1MHz.

Use the following steps to design an application circuit:

1. Set the operating frequency. The frequency is not one of the internal preset values. Therefore, a resistor from the FREQ pin to GND is required, with a value given by Equation 27, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{1\text{MHz}} = 37\text{k}\Omega \quad (27)$$

2. Determine the inductor value. Initially, select a value based on an inductor ripple current of 30%. To calculate the inductor value, use Equation 28, as follows:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN(NOMINAL)}}\right) = 0.4\mu\text{H} \quad (28)$$

   The highest value of the ripple current occurs at the maximum input voltage. In this case, the ripple at V_{IN} = 22V is 35%.

3. Verify that the minimum on-time of 40ns is not violated. The minimum on-time occurs at $V_{IN(MAX)}$, as shown in Equation 29:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \times f_{SW}} = 150\text{ns} \quad (29)$$

   This time is sufficient to satisfy the minimum on-time requirement. If the minimum on-time is violated, the ADPL74101 skips pulses at high input voltage, resulting in lower frequency operation and higher inductor current ripple than desired. If undesirable, this behavior can be avoided by decreasing the frequency (with the inductor value adjusted accordingly) to avoid operation near the minimum on time.

4. Select the R_{SENSE} resistor value. The peak inductor current is the maximum DC output current plus half of the inductor ripple current, or 20A × (1 + 0.30/2) = 23A in this case. The R_{SENSE} resistor value can then be calculated based on the minimum value for the maximum current sense threshold (45mV for ILIM = float), given by Equation 30, as follows:

$$R_{SENSE} \leq \frac{45\text{mV}}{23\text{A}} \cong 2\text{m}\Omega \quad (30)$$

   To allow for additional margin, a lower value R_{SENSE} can be used (for example, 1.8mΩ). However, ensure that the inductor saturation current has sufficient margin above $V_{SENSE(MAX)}/R_{SENSE}$, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.

5. Select the feedback resistors. If light-load efficiency is required, high-value feedback resistors can be used to minimize the current due to the feedback divider. However, in most applications, a feedback divider current in the range of 10µA to 100µA or more is acceptable. For a 50µA feedback divider current, R_A = 0.8V/50µA = 16kΩ. R_B can then be calculated as $R_B = R_A(3.3V/0.8V - 1)$ = 50kΩ.

6. Select the FETs. The best way to evaluate FET performance in a particular application is to build and test the circuit on the bench, facilitated by an ADPL74101 evaluation board. However, an educated guess about the application is helpful to initially select FETs. Because this is a high-current, low-voltage application, I^2R losses are likely to dominate over transition losses for the top FET. Therefore, choose a FET with lower $R_{DS(ON)}$ rather than lower gate charge to minimize the combined loss terms. The bottom FET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the bottom FET is typically chosen to be of lower $R_{DS(ON)}$ and higher gate charge than the top FET.

Due to the high current in this application, two FETs may be needed in parallel to more evenly balance the dissipated power and to lower the $R_{DS(ON)}$. Be sure to select logic-level threshold MOSFETs, because the gate drive voltage is limited to 5.5V ($INTV_{CC}$).

7. Select the input and output capacitors. C_{IN} is chosen for an RMS current rating of at least 10A ($I_{OUT}/2$, with margin) at the temperature. C_{OUT} is chosen with an ESR of 3mΩ for low output ripple. Multiple capacitors connected in parallel may be required to reduce the ESR to this level. The output ripple in continuous mode is highest at the maximum input voltage. The output voltage ripple ($V_{ORIPPLE}$) due to ESR is approximately given by Equation 31, as follows:

$$V_{ORIPPLE} = ESR \times \Delta I_L = 3m\Omega \times 6A = 18mV_{P-P} \quad (31)$$

On the 3.3V output, $18mV_{P-P}$ is equal to 0.55% of the peak-to-peak voltage ripple.

8. Determine the bias supply components. Because the regulated output is not greater than the $EXTV_{CC}$ switchover threshold, it cannot be used to bias $INTV_{CC}$. However, if another 5V supply is available, connect that supply to $EXTV_{CC}$ to improve efficiency. For a 6.7ms soft start, select a 0.1µF capacitor for the TRACK/SS pin. As a first pass estimate for the bias components, select the $INTV_{CC}$ capacitance (C_{INTVCC}) = 4.7µF and C_B = 0.1µF.
9. Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light-load efficiency and constant-frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread-spectrum, or phase-locked frequency is desired. The RUN pin can be used to control the minimum input voltage for regulator operation, or it can be tied to V_{IN} for always-on operation. Use ITH compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

PCB Board Layout Checklist

Figure 41 shows the current waveforms present in the various branches of the synchronous regulators operating in the continuous mode.

When laying out the PCB, use the following checklist to ensure the device operates properly.

1. Route the BG traces together and connect them as close as possible to the bottom FET gate. If using gate resistors, connect the resistor connections to the FET gate as close as possible to the FET. Connecting the BG farther from the bottom FET gate can cause inaccuracies in the dead-time control circuit of the ADPL74101. Route the TG traces together and connect them as close as possible to the top FET gate.
2. The combined IC GND pin and the GND return of C_{INTVCC} must return to the combined C_{OUT} negative terminals. The path formed by the top N-channel FET and the C_{IN} capacitor must have short leads and PCB trace lengths. Connect the output capacitor's negative terminals as close as possible to the negative terminals of the input capacitor by placing the capacitors next to each other and away from the loop.
3. Connect the ADPL74101 V_{FB} pin resistive dividers to the positive terminals of C_{OUT} and the signal GND. Place the divider close to the V_{FB} pin to minimize noise coupling into the sensitive V_{FB} node. The feedback resistor connections must not be along the high-current input feeds from the input capacitors.
4. Route the $SENSE^-$ and $SENSE^+$ leads together with minimum PCB trace spacing. Route these traces away from the high-frequency switching nodes on an inner layer, if possible. The filter capacitor between $SENSE^+$ and $SENSE^-$ must be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.

5. Connect the $INTV_{CC}$ decoupling capacitor close to the IC, between the $INTV_{CC}$ and the power GND pin. This capacitor carries the current peaks of the FET drivers. Place an additional 1µF ceramic capacitor between the DRV_{CC} and GND pins to improve noise performance.
6. Keep the switching node (SW), top gate nodes (TG), and boost node (BOOST) away from sensitive small signal nodes, especially from the voltage and current sensing feedback pins. All of these nodes exhibit large, and fast-moving signals. Therefore, keep the nodes on the output side of the ADPL74101 and ensure they occupy the minimum PCB trace area.
7. Use a modified star ground technique: a low-impedance, large-copper-area central grounding point on the same side of the PCB as the input and output capacitors, with tie-ins to the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider, and the GND pin of the IC.

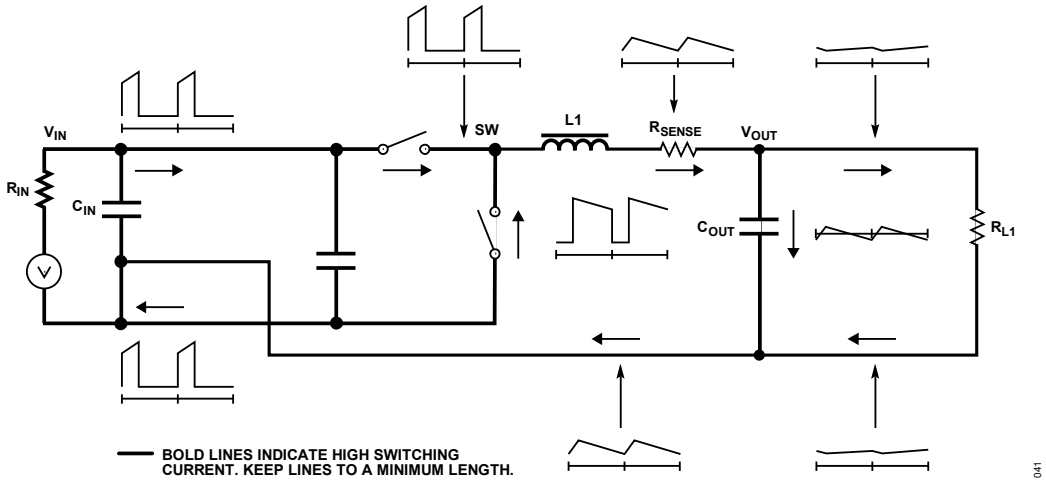


Figure 41. Branch Current Waveforms

PCB Layout Debugging

Use a DC to 50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (the SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation is maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold, typically 25% of the maximum designed current level in Burst Mode operation.

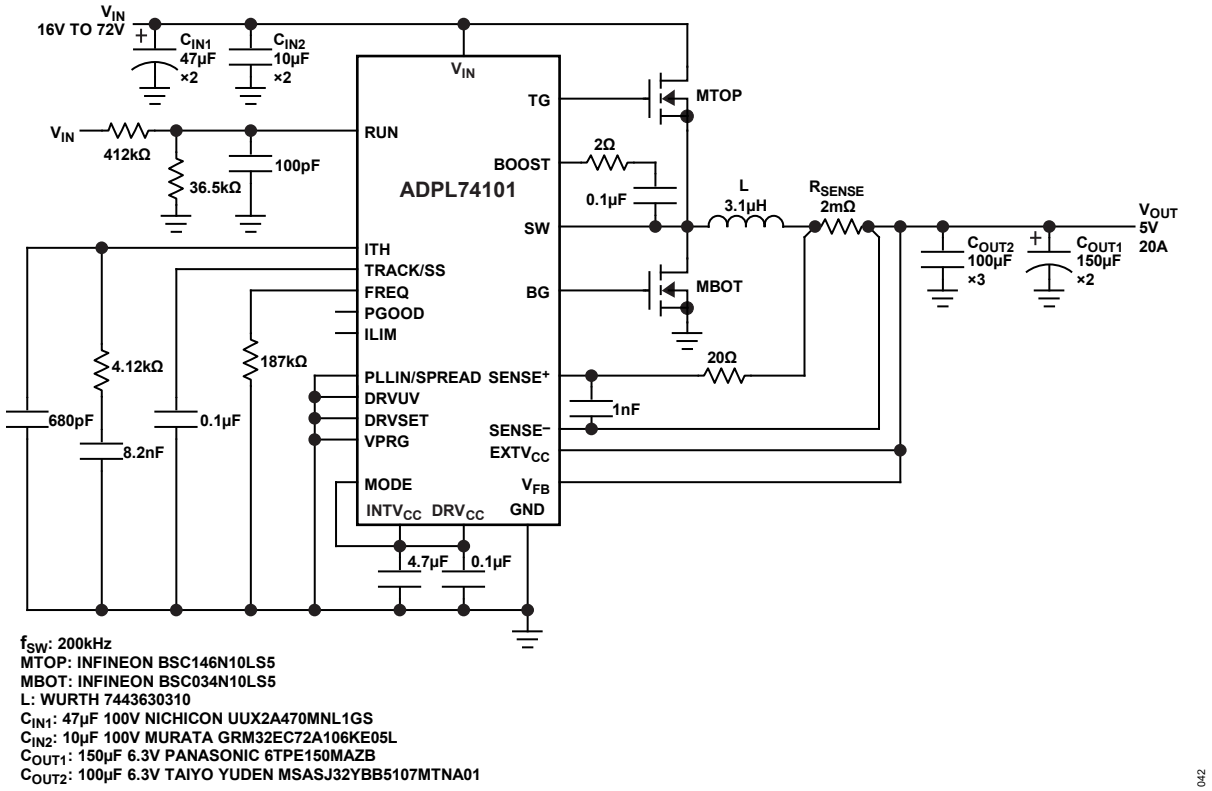
The duty cycle percentage is maintained from cycle to cycle in a well-designed, low-noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage-sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame an improper PCB layout if regulator bandwidth optimization is not required.

Reduce the V_{IN} from its nominal level to verify the operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation. Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, check for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. Place the capacitor across the current-sensing pins next to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high-frequency capacitive coupling. If problems are encountered with high-current output loading at lower input voltages, look for inductive coupling between CIN, the top FET, and the bottom FET components to the sensitive current and voltage

sensing traces. In addition, investigate the common GND path voltage pickup between these components and the device's GND pin.

A problem that can be missed in an otherwise properly working switching regulator, results when the current-sensing leads are hooked up backwards. The output voltage under this improper hookup is maintained, but the advantages of current-mode control are not realized. Compensation of the voltage loop is more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor. The regulator maintains control of the output voltage.

TYPICAL APPLICATIONS



f_{SW}: 200kHz
MTOP: INFINEON BSC146N10LS5
MBOT: INFINEON BSC034N10LS5
L: WURTH 7443630310
C_{IN1}: 47µF 100V NICHICON UUX2A470MNL1GS
C_{IN2}: 10µF 100V MURATA GRM32EC72A106KE05L
C_{OUT1}: 150µF 6.3V PANASONIC 6TPE150MAZB
C_{OUT2}: 100µF 6.3V TAIYO YUDEN MSASJ32YBB5107MTNA01

Figure 42. High-Efficiency, 5V_{OUT} 20A, Buck Regulator

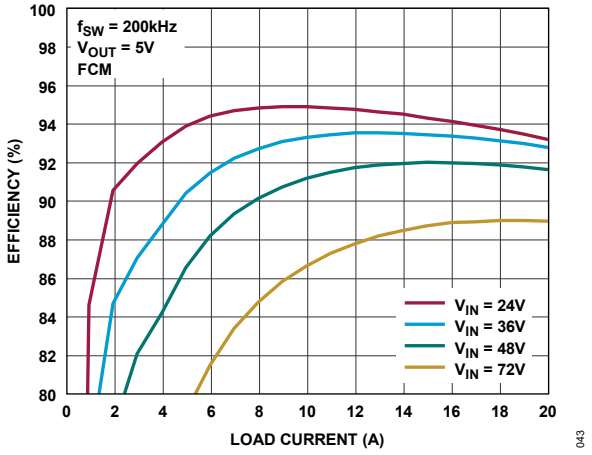


Figure 43. V_{OUT} Efficiency vs. Load Current for Figure 42

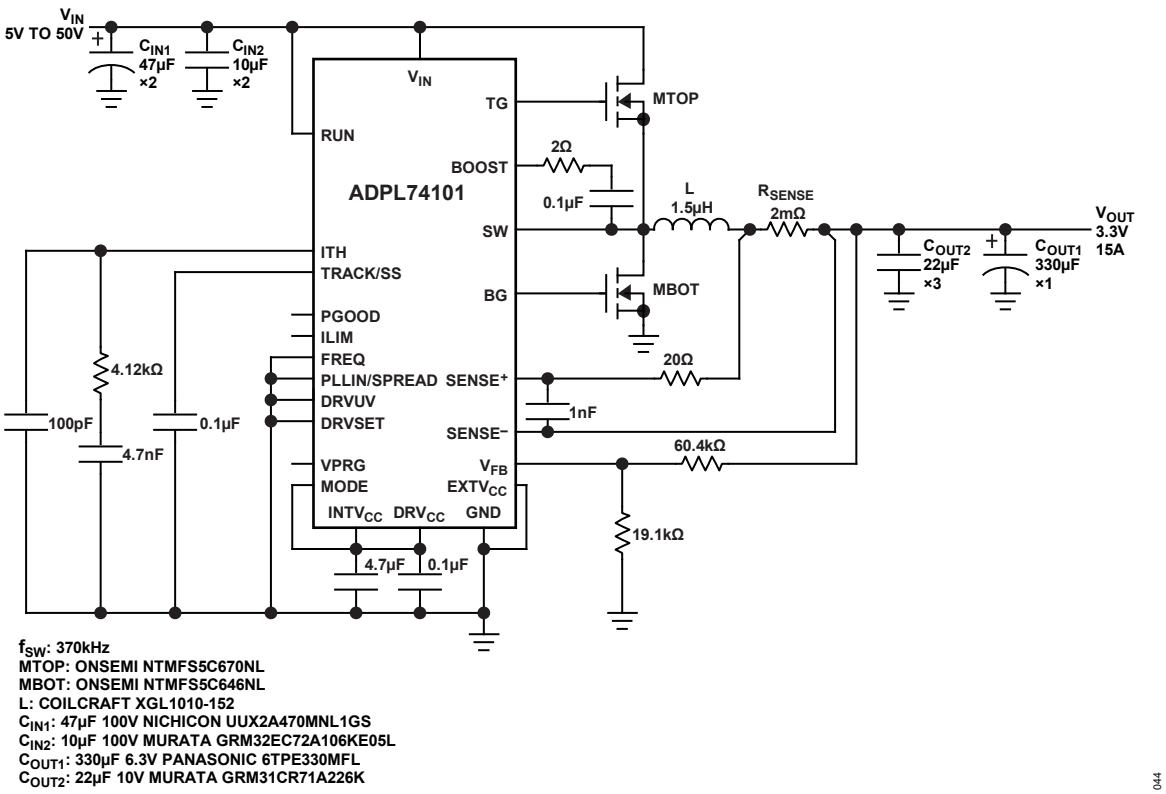


Figure 44. High-Efficiency, 3.3V_{OUT}, Buck Regulator

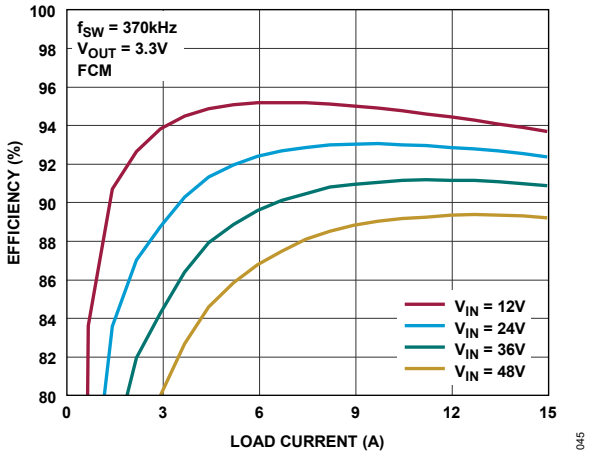
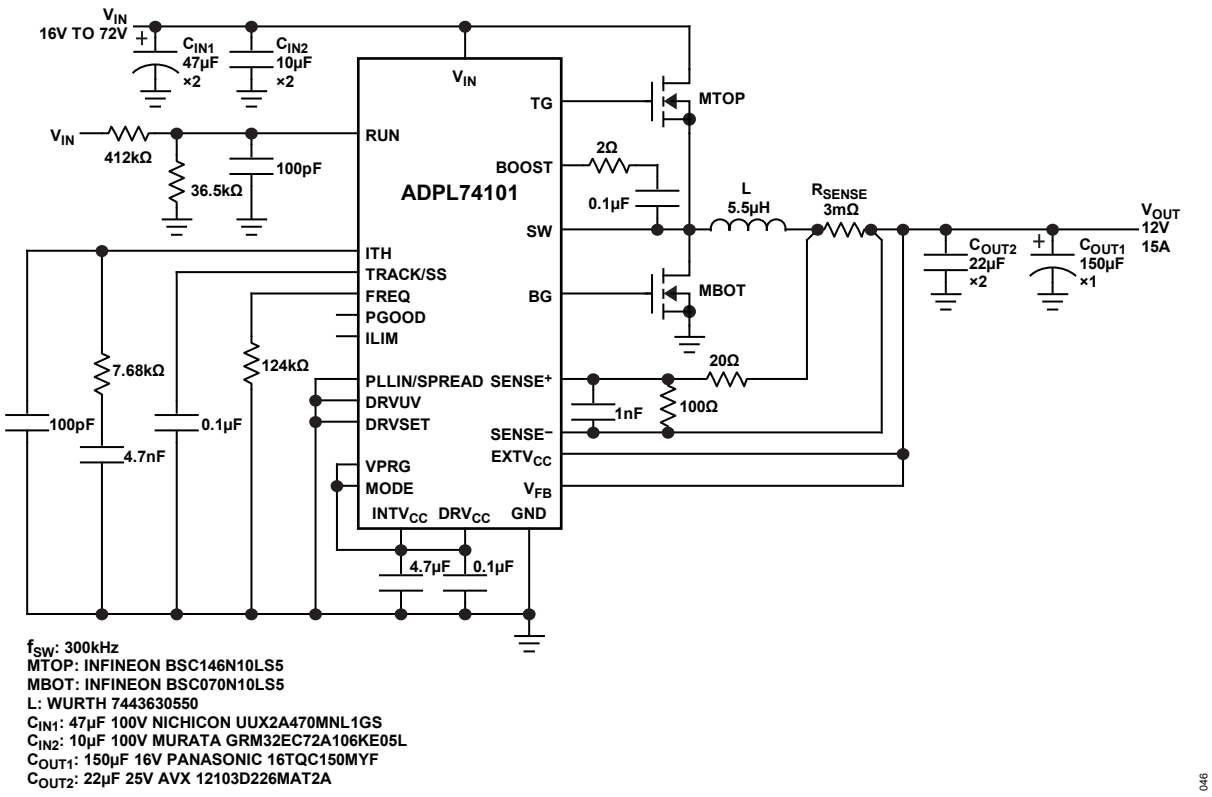


Figure 45. V_{OUT} Efficiency vs. Load Current for Figure 44



f_{SW}: 300kHz
MTOP: INFINEON BSC146N10LS5
MBOT: INFINEON BSC070N10LS5
L: WURTH 7443630550
C_{IN1}: 47µF 100V NICHICON UUX2A470MNL1GS
C_{IN2}: 10µF 100V MURATA GRM32EC72A106KE05L
C_{OUT1}: 150µF 16V PANASONIC 16TQC150MYF
C_{OUT2}: 22µF 25V AVX 12103D226MAT2A

Figure 46. High-Efficiency, 12V_{OUT}, Buck Regulator

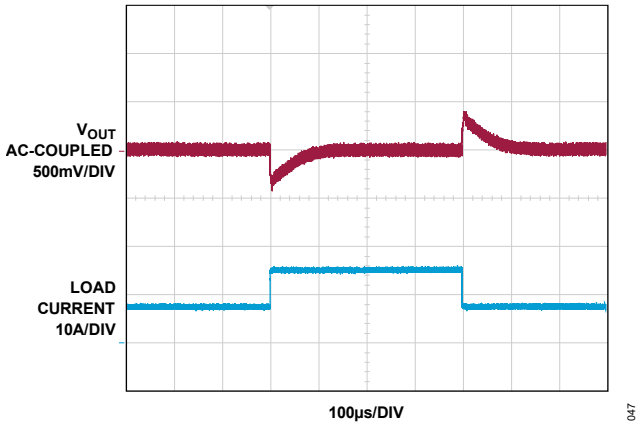


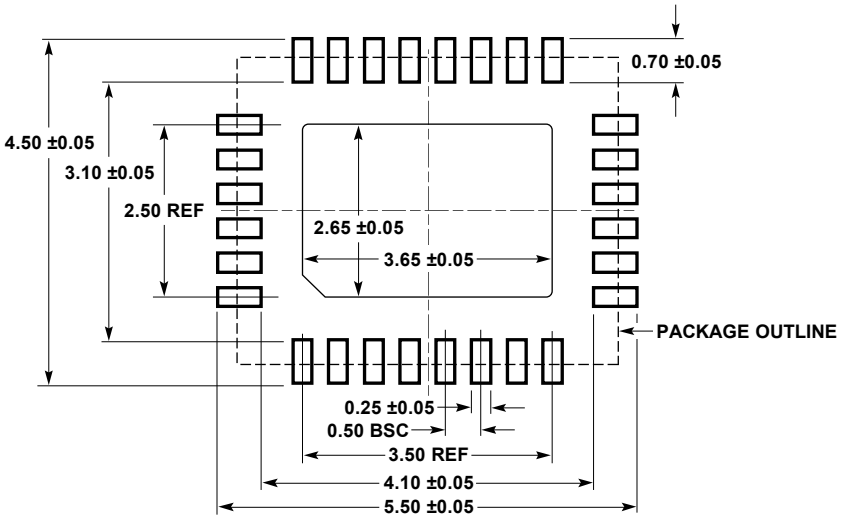
Figure 47. Load-Step Response for Figure 46

RELATED PARTS

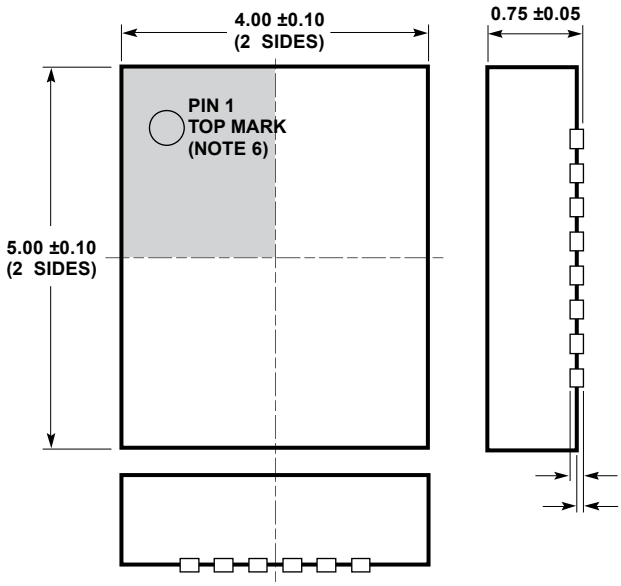
PART NUMBER	DESCRIPTION	COMMENTS
LTC7897	140V, Low I_Q, Synchronous Buck Controller with Programmable 5V to 10V Gate Drive	4.5V ≤ V_{IN} ≤ 140V, V_{OUT} Up to 135V, 100kHz to 3MHz Fixed Operating Frequency, 4mm × 5mm, 28-Lead Quad Flat No Lead (QFN)
LTC7810	150V, Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with 100% Duty Cycle, 10V Gate Drive	4.5V ≤ V_{IN} ≤ 140V, 1V ≤ V_{OUT} ≤ 60V, I_Q = 110µA, PLL Fixed Frequency 50kHz to 750kHz, 48-Lead, 7mm × 7mm, eLQFP Package
LTC7803	40V, Low I_Q, 3MHz Synchronous Step-Down Controller with Spread Spectrum	PLL Fixed Frequency of 100kHz to 3MHz, 4.5V ≤ V_{IN} ≤ 40V, I_Q = 12µA, 0.8V ≤ V_{OUT} ≤ 40V, 3mm × 3mm, 16-QFN Package, 16-Lead Mini Small Outline Package (MSOP)
LTC7805	40V, Low I_Q, Dual, 2-Phase, 100% Duty Cycle Synchronous Step-Down Controller	PLL Fixed Frequency of 100kHz to 3MHz, 4.5V ≤ V_{IN} ≤ 40V, I_Q = 14µA, V_{OUT} Up to 40V, 4mm × 5mm, 28-Lead QFN Package
LTC7802	40V, Low I_Q, 3MHz Dual, 2-Phase, Synchronous Step-Down Controller with Spread Spectrum	4.5V ≤ V_{IN} ≤ 40V, V_{OUT} Up to 40V, I_Q = 12µA, PLL Fixed Frequency of 100kHz to 3MHz, 4mm × 5mm, 28-Lead QFN Package
LTC7800	60V, Low I_Q, High Frequency, Synchronous Step-Down Controller	4.5V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA, PLL Fixed Frequency of 320kHz to 2.25MHz, 3mm × 4mm, 20-Lead QFN Package
LTC7804	40V, Low I_Q, 3MHz Synchronous Boost Controller with Spread Spectrum	4.5V ≤ V_{IN} ≤ 40V, V_{OUT} Up to 40V, 100kHz to 3MHz Fixed Operating Frequency, 3mm × 3mm, QFN-16
LTC3866	38V, Synchronous Step-Down Controller with Sub-mΩ DCR Sensing and Differential Output Sense	4.5V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 3.5V, PLL Fixed Frequency of 250kHz to 770kHz, 4mm × 4mm, 24-Lead QFN Package, 24-Lead Thin Shrink Small Outline Package (TSSOP)
LTC3833	38V, Synchronous Step-Down Controller with Differential Output Voltage Sensing	4.5V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 5.5V, PLL Fixed Frequency of 200kHz to 2MHz, 3mm × 4mm, 20-Lead QFN package, 20-Lead TSSOP
LTC7801	150V, Low I_Q, Synchronous Step-Down DC/DC Controller	4.5V ≤ V_{IN} ≤ 140V, 150V_{PK}, 0.8V ≤ V_{OUT} ≤ 60V, I_Q = 40µA, PLL Fixed Frequency of 50kHz to 900kHz, 4mm × 5mm, 24-Lead QFN Package, 24-Lead TSSOP

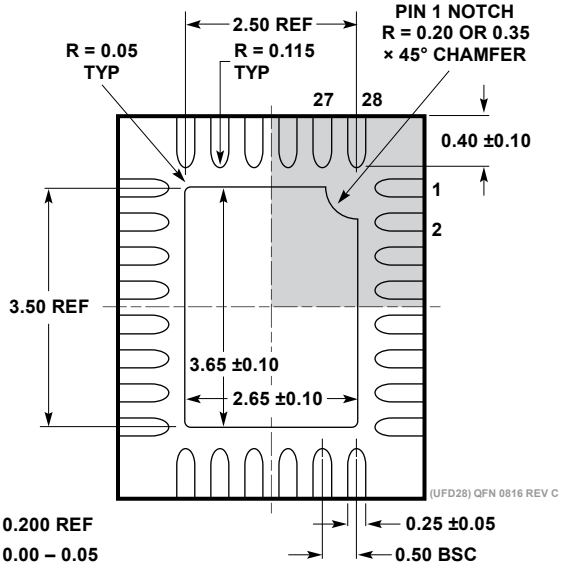
OUTLINE DIMENSIONS

UFD Package
28-Lead Plastic QFN (4mm x 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

ORDERING GUIDE

Table 8. Ordering Guide

MODEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
ADPL74101ACPZ-RL	–40°C to +125°C	28-Lead (4mm x 5mm) Plastic Quad Flat No-lead (QFN) package	05-08-1712