Functionality and Features of the ADE9000 High Performance, Multiphase Energy and Power Quality Monitoring IC

SCOPE

This reference manual provides a detailed description of the ADE9000 functionality and features. This document must be used in conjunction with the ADE9000 data sheet.

FUNCTIONAL BLOCK DIAGRAM

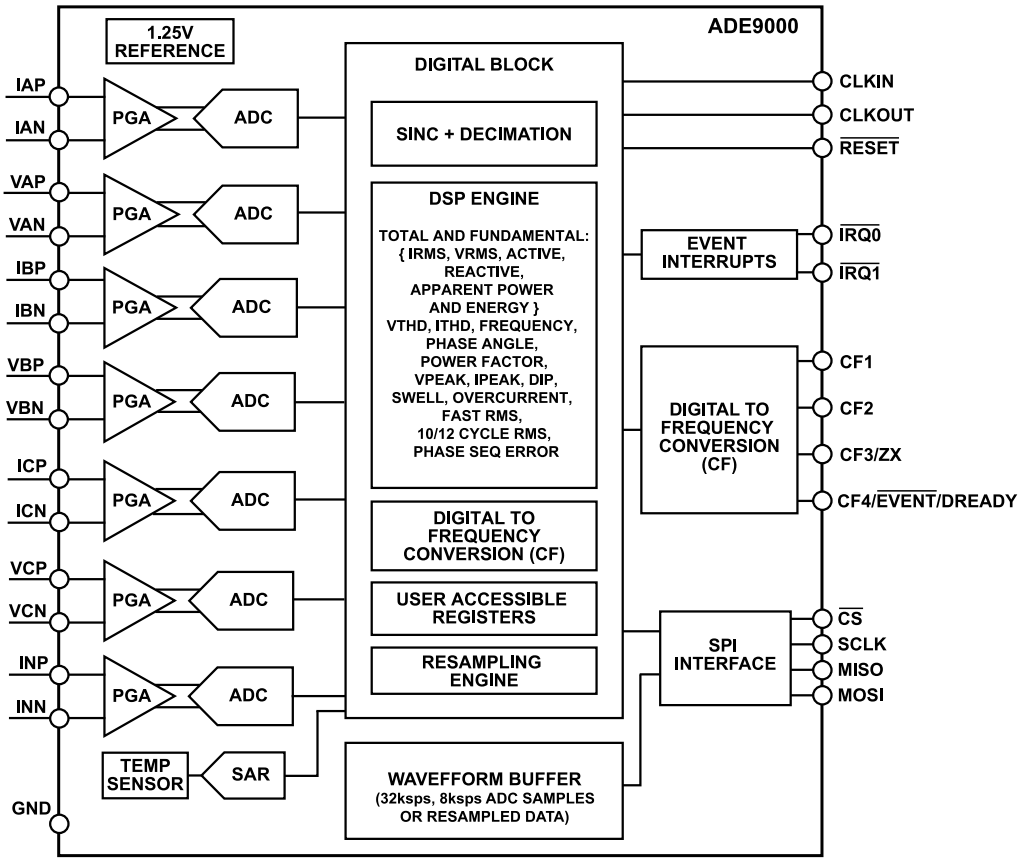

Figure 1. Functional Block Diagram

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REVISION HISTORY

7/2025—Rev. 0 to Rev. A

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3/2017—Revision 0: Initial Version

ANALOG-TO-DIGITAL CONVERTER (ADC)

OVERVIEW

The ADE9000 incorporates seven independent, second-order, Σ-Δ ADCs that sample simultaneously. Each ADC is 24 bits and supports fully differential and pseudo differential inputs, which can go above and below ground. The ADE9000 includes a low noise, low drift, internal band gap reference. Set the EXT_REF bit in the CONFIG1 register if using an external voltage reference. Each ADC contains a programmable gain amplifier which allows a gain of 1, 2, or 4.

ANALOG INPUT CONFIGURATION

There is no internal buffering; the impedance of the ADE9000 depends on the programmable gain selected.

Fully Differential Inputs

The input signals on the IAP, IAN, IBP, IBN, ICP, ICN, VAP, VAN, VBP, VBN, VCP, and VCN pins must not exceed 0.6 V. The differential full-scale input range of the ADCs is ±1 V peak (0.707 V rms).

Figure 2 and Figure 3 show two common types of input signals for an energy monitoring application. Figure 2 shows the maximum input allowed with differential antiphase signals. A current transformer with center tapped burden resistor generates differential, antiphase signals. Figure 3 shows the maximum input signal with pseudo differential signals, similar to those obtained when sensing the mains voltage signal through a resistive divider or using a Rogowski coil current sensor.

The following conditions must be met for the input signals with gain = 1:

- |IAP, IAN, IBP, IBN, ICP,ICN, VAP, VAN, VBP, VBN, VCP, and VCN| ≤ +0.6 V peak
- |IxP − IxN| ≤ +1 V peak, |VxP − VxN| ≤ +1 V peak

Each ADC contains a programmable gain amplifier which allows a gain of 1, 2, or 4. The ADC produces full-scale output codes with an input of ±1 V. With a gain of 1, this full-scale output corresponds to a differential antiphase input of 0.707 V rms, as shown in Figure 2. At a gain of 2, full-scale output codes are produced with an input of 0.353 V rms, as shown in Figure 3. At gain of 4, full-scale output codes are generated with a 0.1765 V rms input signal. Note that the voltages on the xP and xN pins must be within ±0.6 V, as specified in the data sheet.

Write the x_GAIN bits in the PGA_GAIN register to configure the gain for each channel.

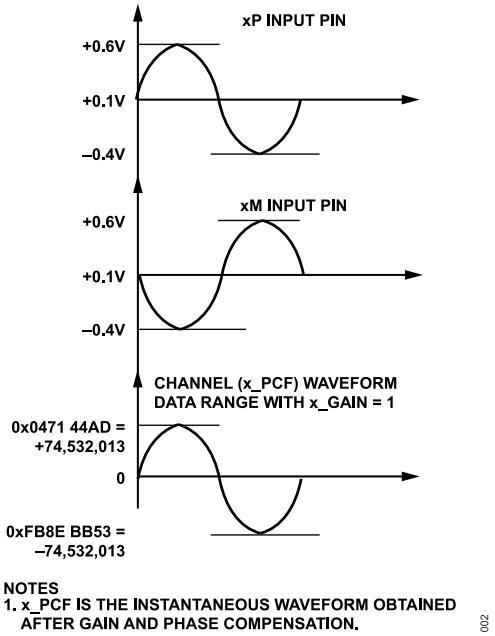

Figure 2. Maximum Input Signal with Differential Antiphase Input with Common Mode Voltage = 0.1 V, Gain = 1

ANALOG-TO-DIGITAL CONVERTER (ADC)

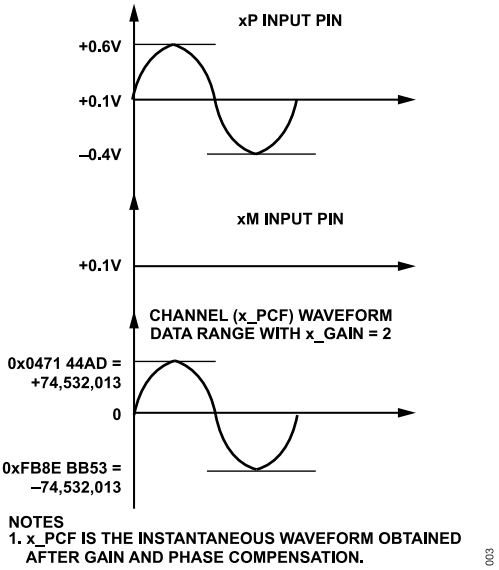

Figure 3. Maximum Input Signal with Pseudo Differential Input with Common Mode Voltage = 0.1 V, Gain = 2

Interfacing to Current and Voltage Sensors

Figure 4 and Figure 6 show the recommended circuits to connect to current transformer sand Rogowski coil current sensors. Figure 5 shows the interface circuit to measure the mains voltage.

The antialiasing filter corner is chosen around 7 kHz to provide sufficient attenuation of out of band signals near the modulator clock frequency. The same RC filter corner is used on voltage channels as well, to avoid phase errors between current and voltage signals. Note that the Rogowski coil input network has a second-order antialias filter to further reduce out of band noise because the Rogowski sensor has a 1/f response.

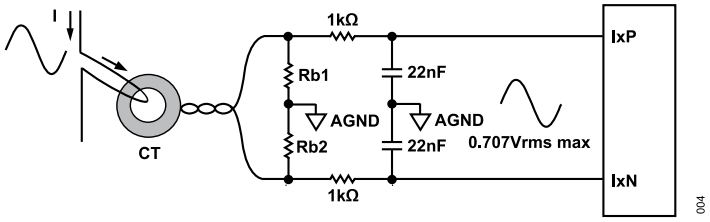

Figure 4. Application Circuit with Current Transformer Current Sensor

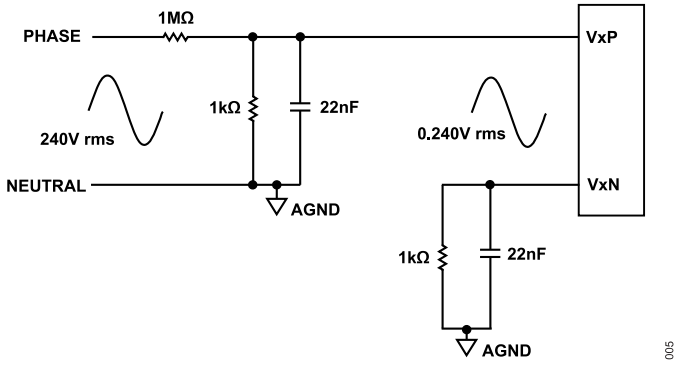

Figure 5. Application Circuit with Voltage Sensed Through Resistor Divider

ANALOG-TO-DIGITAL CONVERTER (ADC)

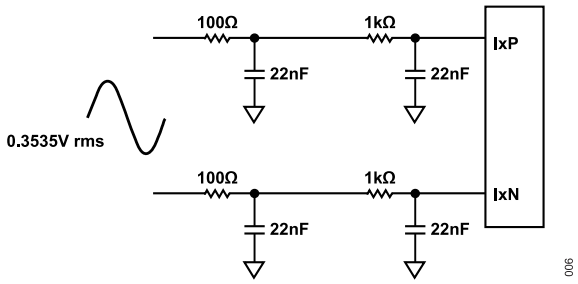

Figure 6. Application Circuit with Rogowski Coil Current Sensor

INTERNAL RF IMMUNITY FILTER

Energy metering applications require the meter to be immune to external radio frequency fields of 30 V/m, from 80 MHz up to 10 GHz, according to IEC 61000-4-3. The ADE9000 has internal antialiasing filters to improve performance in this testing because it is difficult to filter these signals externally. The second-order, internal low-pass filter (LPF) has a corner frequency of 10 MHz. Note that external antialias filters are required to attenuate frequencies above 7 kHz, as shown in the Interfacing to Current and Voltage Sensors section.

MODES OF OPERATION

Each ADC has two modes of operation: normal mode and disabled mode.

In the normal mode of operation, ADCs are turned on and sample continuously. The CHNL_DIS register can be used to disable the ADCs individually.

There are 2 different power modes available in the ADE9000 (see the Power Modes section). All ADCs are turned on in PSM0 power mode. In PSM3 mode, all ADCs are disabled and cannot be turned on.

Table 1. ADC Operation in PSMx Power Modes

PSMx Power Mode	ADC Mode of Operation
PSM0	Normal (on)
PSM3	Disabled (always off)

OUTPUT DATA RATES AND FORMAT

When a conversion has been completed, the DREADY bit of the STATUS0 register is set to 1. If the CF4_CFG[3:2] bits in the CONFIG1 register are equal to 11, the CF4/EVENT/DREADY pin corresponds to DREADY and pulses high to indicate when seven new ADC results are ready.

In the ADE9000, the modulator sampling rate (MODCLK) is fixed at 2.048 MHz (CLKIN/12 = 24.576/12). The output data rate of the sinc filter is MODCLK/64, whereas the low-pass filter/decimator stage yields an output rate 4 times slower than the sinc filter output rate. Figure 7 shows the digital filtering that takes the 2.048 MHz ADC samples and creates waveform information at a decimated rate of 32 kHz or 8 kHz.

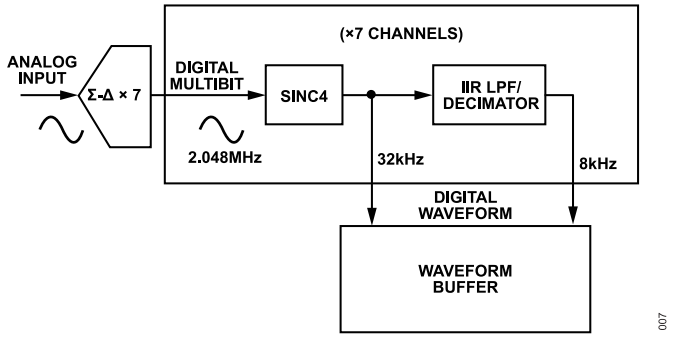

Figure 7. Datapath Following ADC Stage

The output data rates are summarized in Table 2.

ANALOG-TO-DIGITAL CONVERTER (ADC)

Table 2. Output Data Rates

Parameter	Output Data Rate
CLKIN Frequency	24.576 MHz
ADC Modulator Clock, MODCLK	2.048 MHz
SINC Output Data Rate, SINC_ODR	32 kHz
Low-Pass Filter Output Data Rate	8 kHz
3 dB Bandwidth	3.2 kHz

The ADC data in the waveform buffer is stored as 32-bit data by shifting left by 4 bits and sign extending, as shown in Table 3.

Table 3. 32-Bit ADC Data Format

Bits[31:28]	Bits[27:4]	Bits[3:0]
SE	ADC_DATA[23:0]	0000

The expected output code in the waveform buffer from the sinc filter when input is at 1 V peak is 67,107,786 (decimal). The expected output code in the waveform buffer from the decimator filter when input is at 1 V peak is 74,518,668. See the Waveform Buffer section for more information.

VOLTAGE REFERENCE

The ADE9000 supports a 1.25 V internal reference. An external reference can be connected between the REFIN and REFGND pins. When using an external voltage reference, set the EXT_REF bit of the CONFIG1 register, which disables the internal reference buffer.

CRYSTAL OSCILLATOR/EXTERNAL CLOCK

The ADE9000 contains a crystal oscillator. Alternatively, a digital clock signal can be applied at the CLKIN pin of the ADE9000.

When a crystal is used as the clock source for the ADE9000, attach the crystal and the ceramic capacitors, with capacitances of CL1 and CL2, as shown in Figure 8. It is not recommended to attach an external feedback resistor in parallel to the crystal.

When a digital clock signal is applied at the CLKIN pin, the inverted output is available at the CLKOUT pin. This output is not buffered internally and cannot be used to drive any other external devices directly. Note that CLKOUT is available in PSM0 operating mode only.

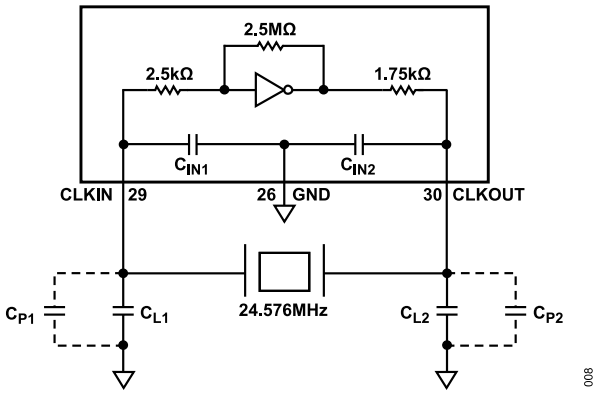

Figure 8. Crystal Application Circuit

CRYSTAL SELECTION

The transconductance of the crystal oscillator circuit in the ADE9000, gm, is provided in the data sheet. It is recommended to have 3 to 5 times more gm than the calculated $gm_{CRITICAL}$ for the crystal.

The following equation shows how to calculate the $gm_{CRITICAL}$ for the crystal from information given in the crystal data sheet:

$$gm_{CRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2 \times \pi \times f_{CLK(Hz)})^2 \times (C_0 + C_L)^2 \quad (1)$$

where:
$gm_{CRITICAL}$ is the minimum gain required to start the crystal, expressed in mA/V.
ESR_{MAX} is the maximum ESR, expressed in ohms.
f_{CLK} is 24.576 MHz, expressed in Hz as 24.576×10^6. C_0 is the maximum shunt capacitance, expressed in farads.
C_L is the load capacitance, expressed in farads.

Crystals with low ESR and smaller load capacitance have a lower $gm_{CRITICAL}$ and are easier to drive.

The ADE9000 evaluation board uses a crystal manufactured by Abracon (Part Number ABLS-24.576MHZ-8-L4Q-F-T), which has a maximum ESR of 40 Ω, load capacitance of 8 pF, and maximum shunt capacitance of 7 pF, which results in a $gm_{CRITICAL}$ of 0.86 mA/V:

$$gm_{CRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2 \times \pi \times f_{CLK(Hz)})^2 \times (C_0 + C_L)^2$$

$$gm_{CRITICAL} = 4 \times 40 \times 1000 \times (2 \times \pi \times 24.576 \times 10^6)^2 \times (7 \times 10^{-12} + 8 \times 10^{-12})^2 = 0.86$$

The gain of the crystal oscillator circuit in the ADE9000, gm, provided in the data sheet is more than 5 times $gm_{CRITICAL}$; therefore, there is sufficient margin to start up this crystal.

LOAD CAPACITOR CALCULATION

Crystal manufacturers specify the combined load capacitance across the crystal, CL. The capacitances in Figure 8 can be described as follows:

- CP_1 and CP_2: parasitic capacitances on the clock pins formed due to printed circuit board (PCB) traces.
- Cin_1 and Cin_2: internal capacitances of the CLKIN and CLKOUT pins respectively.
- CL_1 and CL_2: selected load capacitors to get the correct combined CL for the crystal.

The internal pin capacitances, C_{in1} and C_{in2}, are 4 pF each, as shown in the data sheet. To find the values of CP_1 and CP_2, measure the capacitance on each of the clock pins of the PCB, CLKIN and CLKOUT, respectively, with respect to the AGND pin. If the measurement is done

CRYSTAL OSCILLATOR/EXTERNAL CLOCK

after soldering the IC to the PCB, subtract out the 4 pF internal capacitance of the clock pins to find the actual value of parasitic capacitance on each of the crystal pins.

To select the appropriate capacitance value for the ceramic capacitors, calculate CL_1 and CL_2 from the following equation:

$$CL = [(CL_1 + CP_1 + C_{IN1}) \times (CL_2 + CP_2 + C_{IN2})]/(CL_1 + CP_1 + C_{IN1} + CL_2 + CP_2 + C_{IN2}) \quad (2)$$

Select CL_1 and CL_2 such that the total capacitance on each clock pins is

$$CL_1 + CP_1 + C_{IN1} = CL_2 + CP_2 + C_{IN2} \quad (3)$$

Using Equation 2 and Equation 3, the values of CL_1 and CL_2 can be calculated.

LOAD CAPACITOR CALCULATION EXAMPLE

If a crystal with load capacitance specification of 8 pF is selected and the measured parasitic capacitances from the PCB traces are CP1 = CP2 = 2 pF, Equation 2 implies that

$$CL = [(CL_1 + CP_1 + C_{IN1}) \times (CL_2 + CP_2 + C_{IN2})]/(CL_1 + CP_1 + C_{IN1} + CL_2 + CP_2 + C_{IN2})$$

$$8\text{ pF} = [(CL_1 + 2\text{ pF} + 4\text{ pF}) \times (CL_2 + 2\text{ pF} + 4\text{ pF})]/(CL_1 + 2\text{ pF} + 4\text{ pF} + CL_2 + 2\text{ pF} + 4\text{ pF})$$

Assuming that $CL_1 = CL_2$, to satisfy Equation 3,

$$8\text{ pF} = [(CL_1 + 6\text{ pF}) \times (CL_1 + 6\text{ pF})]/(CL_1 + 6\text{ pF} + CL_1 + 6\text{ pF})$$

$$8\text{ pF} = [(CL_1 + 6\text{ pF}) \times (CL_1 + 6\text{ pF})]/[2 \times (CL_1 + 6\text{ pF})]$$

$$8\text{ pF} = (CL_1 + 6\text{ pF})/2$$

Therefore, $CL_1 = CL_2 = 10$ pF.

Based on this example, 10 pF ceramic capacitors are selected for CL_1 and CL_2.

POWER MANAGEMENT

POWER MODES

The ADE9000 offers two operating modes, PSM0 and PSM3. The entry into the power modes is controlled by the PM1 and PM0 pins. These pins are checked continuously to determine which operating mode to enter. If it is desired to place the ADE9000 into a low power reset state, PSM3 can be used.

POWER-ON SEQUENCE

After power is applied to the VDD pin of the ADE9000 IC, the device checks the state of the PM0 and PM1 pins to check the power supply mode (see the Power Modes section for more information). If in PSM0 mode (PM1 and PM0 = 00 or 01) and the $\overline{\text{RESET}}$ pin is high, the AVDD and DVDD low dropout regulators (LDOs) are turned on when VDD reaches 2.4 V to 2.6 V. If the $\overline{\text{RESET}}$ pin is low, the AVDD and DVDD LDOs are not turned on. Note that there is a clamp that limits the current used to charge the AVDD and DVDD LDOs to 17 mA per LDO.

When AVDD and DVDD are both above 1.3 V to 1.5 V and VDD is above 2.4 V to 2.6 V, a 20 ms timer is started to allow additional time for the supplies to come to their normal potentials (VDD between 2.97 V and 3.6 V, AVDD at 1.9 V, and DVDD at 1.7 V). After this timer has elapsed, the crystal oscillator is started.

The RSTDONE interrupt is triggered 26 ms later, bringing the $\overline{\text{IRQ1}}$ pin low and setting the RSTDONE bit in the STATUS1 register. The RSTDONE bit being set indicates to the user that the ADE9000 has finished its power-up sequence. The user can now configure the IC via the serial peripheral interface (SPI). After configuring the device, write the RUN register to start the DSP so that it starts making measurements. Note that registers from Address 0x000 through Address 0x0FF and Address 0x400 through Address 0x5FF are restored to their default values during power-on. Registers from Address 0x200 through Address 0x3FF are cleared within 500 µs from when the RUN register value changes from 0x0000 to 0x0001. Also note that the waveform buffer, Address 0x800 through Address 0xFFF, is not cleared after reset.

In PSM3 mode, the AVDD and DVDD LDOs are not turned on. The RSTDONE interrupt does not occur, and the SPI port is not available

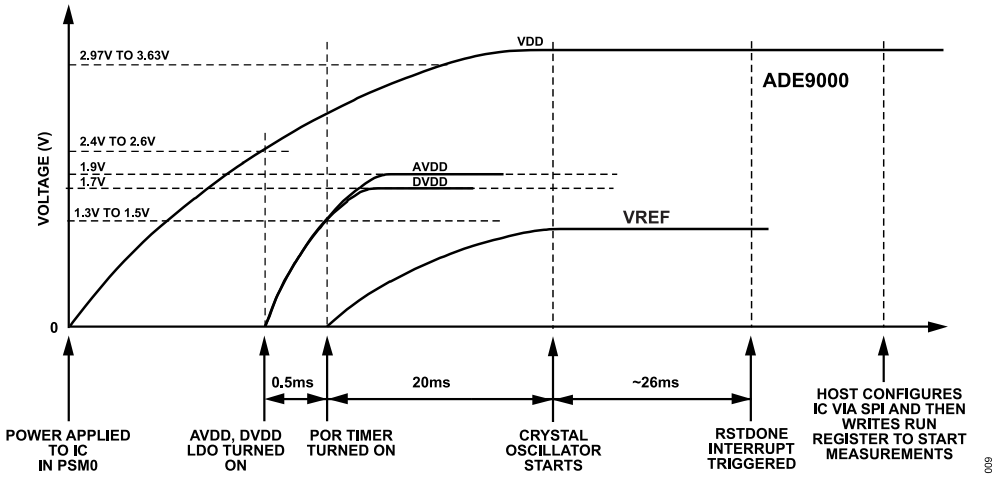

Figure 9. ADE9000 Power-On Sequence for PSM0

Table 4. Power Modes (PSM0 and PSM3)

PSMx Power Mode	Description	PM1 Pin	PM0 Pin	Functions Available	SPI Available?
PSM0	Normal mode	0	0 or 1	All functions	Yes
PSM3	Idle	1	1	None	No

BROWNOUT DETECTION

Power-on reset (POR) circuits monitor the VDD, AVDD, and DVDD supplies. If AVDD or DVDD drops below 1.3 V to 1.5 V, or VDD drops below 2.4 V to 2.6 V, the IC is held in reset and the power-on sequence begins again, waiting until AVDD and DVDD are above 1.3 V to 1.5 V and VDD is above 2.4 V to 2.6 V before starting the 20 ms POR timer. A RSTDONE interrupt on $\overline{\text{IRQ1}}$ indicates when the ADE9000 can be reinitialized via the SPI.

POWER MANAGEMENT

RESET

If the $\overline{\text{RESET}}$ pin goes low for 1 µs or the SWRST bit is set in the CONFIG1 register to initiate a software reset, the AVDD and DVDD LDOs are turned off. The power-on sequence resumes from the point where the AVDD and DVDD LDOs are turned on (see the Power-On Sequence section for details). For applications that require putting the ADE9000 into a low power reset state, it is recommended to use PSM3, which consumes roughly 2 µA, instead of holding the IC in reset with the $\overline{\text{RESET}}$ pin low, which consumes 100 µA (see the data sheet for the exact current consumption).

CHANGING POWER MODES

The state of the PM1 and PM0 pins is continuously monitored. If the power mode changes from PSM0 to PSM3 (PM1 and PM0 = 11) for 1 µs, the AVDD and DVDD LDOs are turned off. When the power mode switches back to PSM0, the power-on sequence resumes from the point where the AVDD and DVDD LDOs are turned on.

MEASUREMENTS

CURRENT CHANNEL MEASUREMENT UPDATE RATES

Table 5 indicates the registers that hold current channel measurements and the rate at which they update.

Table 5. Current Channel Measurement Update Rates

Register Name	Description	UpdateRate
AI_SINC_DAT	IA sinc4 filter output	32 ksps
BI_SINC_DAT	IB sinc4 filter output	32 ksps
CI_SINC_DAT	IC sinc4 filter output	32 ksps
NI_SINC_DAT	IN sinc4 filter output	32 ksps
AI_LPF_DAT	IA sinc4 + IIR LPF filter output	f_{DSP} = 8 ksps
BI_LPF_DAT	IB sinc4 + IIR LPF filter output	f_{DSP} = 8 ksps
CI_LPF_DAT	IC sinc4 + IIR LPF filter output	f_{DSP} = 8 ksps
NI_LPF_DAT	IN sinc4 + IIR LPF filter output	f_{DSP} = 8 ksps
AI_PCF	Instantaneous current on IA	f_{DSP} = 8 ksps
BI_PCF	Instantaneous current on IB	f_{DSP} = 8 ksps
CI_PCF	Instantaneous current on IC	f_{DSP} = 8 ksps
NI_PCF	Instantaneous current on IN	f_{DSP} = 8 ksps
AIRMS	Filtered-based total rms of IA	f_{DSP} = 8 ksps
BIRMS	Filtered-based total rms of IB	f_{DSP} = 8 ksps
CIRMS	Filtered-based total rms of IC	f_{DSP} = 8 ksps
NIRMS	Filtered-based total rms of IN	f_{DSP} = 8 ksps
ISUMRMS	Filtered rms of vector sum (AI_PCF + BI_PCF + CI_PCF ± NI_PCF); see the Neutral Current RMS, Vector Current Sum section	f_{DSP} = 8 ksps
IPEAK	Peak current channel sample; see the Peak Detection section	f_{DSP} = 8 ksps
ANGLx_xxx	Voltage to current or current to current phase angle; see the Angle Measurement section	CLKIN/24 = 1024 ksps

ADC_REDIRECT Multiplexer

The ADE9000 provides a multiplexer that allows any ADC output to be redirected to any digital processing datapath.

By default, each modulator is mapped to its corresponding datapath. For example, the IAP and IAN pins go into the IA modulator, which is mapped to the IA digital processing datapath. Write to the ADC_REDIRECT register to change the ADC to digital channel mapping.

The redirection can be useful to simplify layout, depending on if the ADE9000 is on the top or bottom of the PCB, by redirecting the IA ADC output to the IC digital datapath and the IC ADC output to the IA digital datapath. To redirect the IA and IC ADC outputs, write IA_DIN = 010 and IC_DIN = 000 in the ADC_REDIRECT register.

Alternatively, the VA voltage channel output can be used for all three datapaths by writing VB_DIN = 100 and VC_DIN = 100 in the ADC_REDIRECT register.

The neutral current channel does not offer a zero-crossing output or angle measurements. To calibrate the phase of the neutral current NI_PCF signal, direct the neutral current ADC output to, for example, the Phase B digital current channel and check how its angles correspond to Phase A by writing IB_DIN = 011.

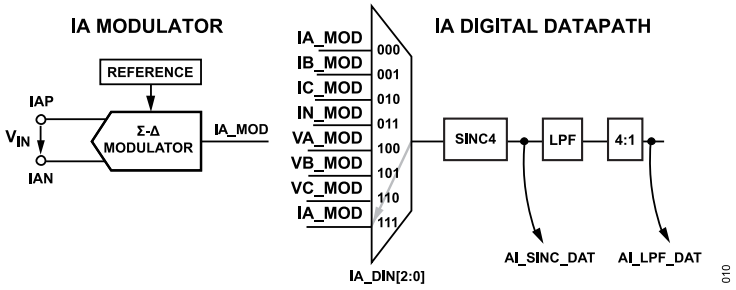

Figure 10. ADC_REDIRECT Modulator to Digital Datapath Multiplexing

MEASUREMENTS

Current Channel Gain, XIGAIN

There are many sources of gain error in an energy metering system. The current sensor, including current transformer burden resistors, may have some error. There is part to part gain error in the ADE9000 device itself, and the voltage reference may have some variation (see the data sheet for the device specifications).

The ADE9000 provides a current gain calibration register so that each metering device has the same current channel scaling.

The current channel gain varies with xIGAIN as shown in the following equation:

$$Current \quad Channel \quad Gain = \left(1 + \frac{xIGAIN}{2^{27}}\right) \tag{4}$$

Use Equation 4 to calculate the xIGAIN value for a given current channel gain:

xIGAIN = ROUND((*Current Channel Gain* − 1) × 2^{27}

The current channel gain can be positive or negative.

For example, to gain the current channel up by 10% to 1.1,

xIGAIN = ROUND((1.1 − 1) × 2^{27} = 13421773 = 0x00CC_CCCD

To gain it down by 10% to 0.9,

xIGAIN = ROUND((0.9 − 1) × 2^{27} = −1 × 10^{7} = 0xFF33_3333

It is also possible to use the current channel gain register to change the sign of the current channel, which can be useful if the current sensor was installed backwards. To compensate for this, use current channel gain = −1.

xIGAIN = ROUND((−1 − 1) × 2^{27} = −268435456 = 0xF000_0000

If the multipoint phase and gain feature is used, it is recommended to use the xIGAIN for the main correction, done at the nominal current for the meter (see the Multipoint Phase/Gain Calibration section for more information).

Note that for a given phase,

|*Current Channel Gain* × *Voltage Channel Gain* × *Power Gain*| ≤ 3.75 (5)

IB Calculation Using ICONSEL

Write the ICONSEL bit in ACCMODE to calculate IB = −IA − IC. This setting can help save the cost of a current transformer in some 3-wire delta configurations. See the Applying the ADE9000 to a 3-Wire Delta Service section for more information.

High-Pass Filter

A high-pass filter is provided to remove dc offsets for accurate rms and energy measurements.

The ADE9000 high-pass filter on the current and voltage channels is enabled by default. It can be disabled by writing the DISPHPF bit in the CONFIG0 register equal to 1.

It is recommended to leave the high-pass filter enabled to achieve the metering performance listed in the specifications in the data sheet.

For some applications, it is desirable to increase the high-pass filter corner, such as to improve performance when a Rogowski coil current sensor is used.

The high-pass filter corner is selectable using the HPF_CRN bits in the CONFIG2 register (see Table 6).

Table 6. HPF Corner Gain with 50 Hz Input Signal

HPF_CRN	$f_{-3\ dB}$ (Hz)	HPF_GAIN	Settling Time to 1% for DC Step (sec)	Settling Time to 0.1% for DC Step (sec)
0	77.4	0.537	0.009	0.013
1	39.3	0.790	0.018	0.027
2	19.8	0.935	0.037	0.055
3	9.9	0.984	0.073	0.110

MEASUREMENTS

Table 6. HPF Corner Gain with 50 Hz Input Signal (Continued)

HPF_CRN	$f_{-3\ dB}$ (Hz)	HPF_GAIN	Settling Time to 1% for DC Step (sec)	Settling Time to 0.1% for DC Step (sec)
4	5.0	0.997	0.147	0.221
5	2.5	0.999	0.294	0.442
6 (default)	1.25	1.001	0.589	0.883
7	0.625	1.001	1.179	1.768

Digital Integrator

A digital integrator is included to allow easy interfacing to di/dt current sensors, also known as Rogowski coils. The di/dt sensor output increases by 20 dB/decade over the frequency range. To compensate for this increase, the digital integrator applies −20 dB/decade gain with a phase shift of approximately −90°.

A second-order antialiasing filter is required to avoid noise aliasing back in the band of interest when the ADC is sampling.

To enable the digital integrator on the IA, IB, and IC channels, set the INTEN bit in the CONFIG0 register. To enable the digital integrator on the neutral current, IN channel, set the ININTEN bit in the CONFIG0 register.

Figure 11 and Figure 12 show the magnitude and phase response of the ADE9000 digital integrator with the default DICOEFF = 0xFFFFE000.

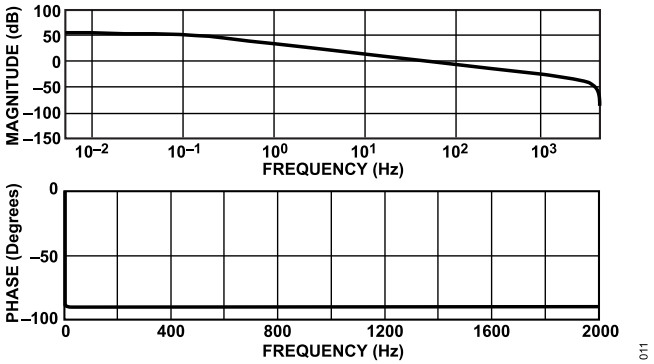

Figure 11. Digital Integrator Magnitude and Phase Response with DICOEFF = 0xFFFFE000

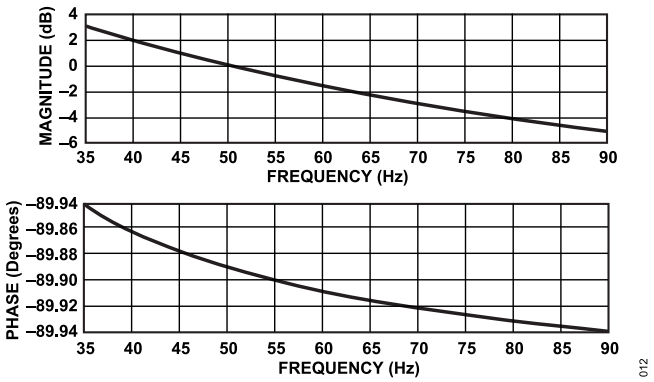

Figure 12. Digital Integrator Magnitude and Phase Response from 40 Hz to 80 Hz with DICOEFF = 0xFFFFE000

If the integrator is enabled, set DICOEFF = 0xFFFFE000.

MEASUREMENTS

Phase Compensation

The ADE9000 phase compensation uses a digital filter to achieve a phase adjustment of ±0.001°. This high resolution improves the total active energy and reactive energy performance at low power factors.

The phase calibration range is −15° to +2.25° at 50 Hz.

To achieve this calibration range, the voltage channel is delayed by one 8 ksps sample, 2.25° at 50 Hz:

$$Voltage\ \ Channel\ \ Delay° = \left(\frac{f_{LINE}}{f_{DSP}} \times 360°\right) \quad (6)$$

$$Voltage\ \ Channel\ \ Delay° = \left(\frac{50}{8000} \times 360°\right) = 2.25°$$

The current channel is then delayed by a digital filter, according to the value programmed into the xPHCALx register. The resulting phase correction depends on the value in the xPHCALx register. The following equation provides the phase correction between the input current and voltage after the combined voltage and current delays. In this formula, PhaseCorrection° is positive to correct a current that lags the voltage, and PhaseCorrection° is negative to correct a situation where the current leads the voltage, such as occurs with a current transformer:

$$Phase\ \ Correction° = arctan\left(\frac{-\sin\omega}{xPHCALx \times 2^{-27} + \cos\omega}\right) - arctan\left(\frac{-xPHCALx \times 2^{-27} \times \sin\omega}{1 + xPHCALx \times 2^{-27} \times \cos\omega}\right) + \omega \quad (7)$$

where $\omega = 2 \times \pi \times f_{LINE}/f_{DSP}$.

The xPHCALx register value can be calculated from the desired phase correction according to this equation:

$$xPHCALx = \left(\frac{\sin(\varphi - \omega) + \sin\omega}{\sin(2 \times \omega - \varphi)}\right) \times 2^{27} \quad (8)$$

For example, if f_{LINE} = 50 Hz, f_{DSP} = 8 kHz, and the current leads the voltage by 0.1 degrees, Phase Correction° = −0.1°. Write xPHCALx = 0xFFD3_7760 to correct for this.

$\omega = 2 \times \pi \times 50/8000 = 0.03927$

$$xPHCALx = \left(\frac{\sin(RADIANS(-0.1) - 0.03927) + \sin 0.03927}{\sin(2\ \ 0.03927 - RADIANS(-0.1))}\right) \times 2^{27} = -2918553 = 0xFFD3\_7767$$

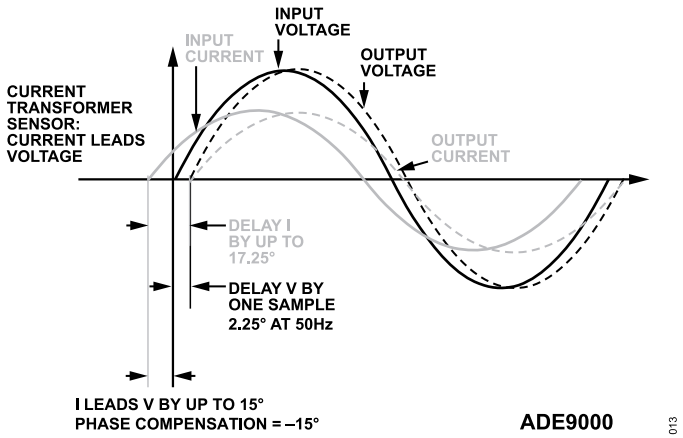

Figure 13. Phase Compensation Example for Current Transformer, where the Current Leads the Voltage

MEASUREMENTS

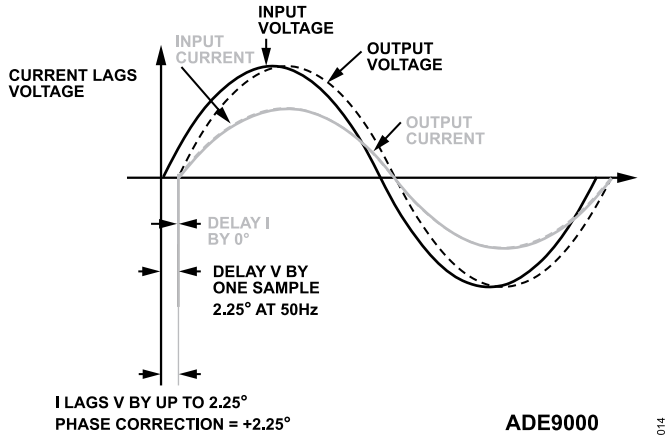

Figure 14. Phase Compensation Example where Current Lags Voltage

Using the previous equations, it can be seen that at 60 Hz, the voltage channel delay is 2.7°:

$$Voltage\ \ Channel\ \ Delay° = \left(\frac{60}{8000} \times 360°\right) = 2.7°$$ (9)

This leads to a phase calibration range of −15° to +2.7° at 60 Hz.

Multipoint Phase/Gain Calibration

The ADE9000 allows the current channel gain and phase compensation to vary as a function of the calculated input current rms amplitude in xIRMS. This feature corrects for the nonlinearities of current transformer sensors to achieve very high meter accuracy, for example in Class 0.2 meters.

Multipoint Gain and Phase

There is a current channel gain, xIGAIN, that is applied regardless of the xIRMS input signal level. This gain compensates for the nominal gain error of the current channel, including the current transformer and burden resistors. If multipoint phase and gain compensation is enabled, an additional current gain value is applied in based on the xIRMS value to compensate for the current transformer gain shift over input signal amplitude.

If multipoint gain and phase compensation is enabled, with MTEN = 1, an additional gain factor, xIGAIN0 through xIGAIN4, is applied based on the xIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values, as shown in Figure 15.

Similarly, for the phase compensation, if multipoint phase and gain compensation is enabled, the applied current channel phase compensation varies based on the xIRMS input signal level.

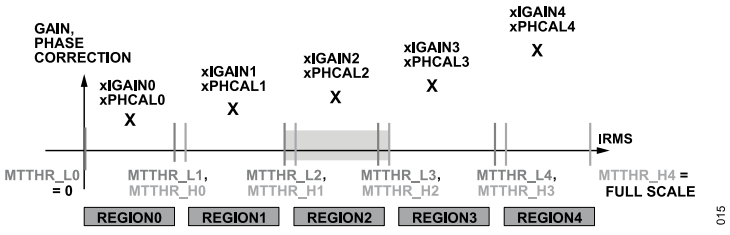

Figure 15. Multipoint Phase and Gain Calibration

The MTTHR_Lx and MTTHR_Hx registers set up the ranges in which to apply each set of corrections, allowing hysteresis.

The decision of which coefficients to apply is done according to the following rules:

```
If xIRMS >MTTHR_H[current_region]
  If current_region <=3
    Current_region++;
```

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```
Else If xIRMS >MTTHR_L[current_region]
  If current_region >=1
    current_region--;
xIGAIN = xIGAIN[current_region];
xPHCAL = xPHCAL[current_region];
```

For example, if AIRMS goes above MTTHR_H2, the phase and gain correction is set to AIGAIN3 and APHCAL3, respectively. Then, if AIRMS goes below MTTHR_L3, the phase and gain correction is set to AIGAIN2 and APHCAL2, respectively.

For proper operation, the value of the registers must be MTTHR_L[0] < MTTHR_L[1] < MTTHR_H[0] < MTTHR_L[2] < MTTHR_H[1] < MTTHR_L[3] < MTTHR_H[2] < MTTHR_L[4] < MTTHR_H[3] < MTTHR_H[4].

Multipoint phase and gain calibration is disabled by default. To enable it, set the MTEN bit in the CONFIG0 register.

Single Point Gain and Phase

When multipoint phase and gain calibration is disabled, single-point phase and gain calibration is allowed.

In this case, the xIGAIN register is applied. No additional current channel gain is applied based on xIRMS amplitude.

When multipoint phase and gain calibration is disabled, the xPHCAL0 phase compensation is always applied regardless of the xIRMS value.

Voltage Channel Gain

The xVGAIN registers can be used to calibrate the voltage channel of each phase. The xVGAIN register has the same scaling as the xIGAIN register. See the Current Channel Gain, XIGAIN section for the equation.

FULL-SCALE CODES

Table 7 gives the expected codes when the ADC inputs are at full scale with PGA gain set to 1.

Table 7. Full-Scale ADC Codes

Parameter	Output Code
Sinc4 Output at 32 ksps	67,107,786
Dec Output at 8 ksps	74,518,668
xPCF at 8 ksps	74,532,013
Total IRMS and VRMS	52,702,092
Fundamental IRMS and VRMS	52,702,092
Total WATT, VAR, and VA	20,694,066
Fundamental WATT, VAR, and VA	20,694,066
Fast RMS½	52,702,092
10 Cycle RMS/12 Cycle RMS	52,702,092
Resampled Data	18,196

POWER AND FILTER-BASED RMS MEASUREMENT ALGORITHMS

Filter-Based Total RMS

The ADE9000 offers current and voltage rms measurements that are calculated by squaring the input signal, low-pass filtering, and then taking the square root of the result.

The low-pass filter, LPF2, extracts the rms value, attenuating harmonics of a 50 Hz or 60 Hz fundamental by at least 64 dB so that, at full scale, the variation in the calculated rms value is very small, ±0.064% error. Note that the rms reading variation increases as the input signal gets smaller because the noise in the measurement increases.

Note that the xRMS register does not read 0 with the xP and xN inputs shorted together.

The filter based rms has a bandwidth of 3.2 kHz

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The rms calculations, one for each channel, AIRMS, BIRMS, CIRMS, NIRMS, AVRMS, BVRMS, and CVRMS, are updated every 8 ksps. The ISUMRMS calculation uses the same method to calculate ISUMRMS, where ISUM = IA + IB + IC ± IN, and also updates at 8 ksps (see the Neutral Current RMS, Vector Current Sum section for more information).

The xRMS value at full scale is 52,702,092 (decimal). The full scale is a function of PGA gain.

$$full\ \ scale = \frac{full\ \ scale\ \ input\ \ at\ \ PGA\ \ GAIN1}{PGA\ \ GAIN} \quad (10)$$

For high performance at small input signals, below 1000:1, it is recommended to calibrate the offset of this measurement using the xRMSOS register. It is recommended to calibrate the offset at the smallest input signal that requires good performance; do not calibrate this measurement with zero input signal.

The following equation indicates how the xRMSOS register value modifies the result in the xRMS register.

$$xxRMS = \sqrt{xxRMS_0{}^2 + \ \ 2^{15} \times xxRMSOS} \quad (11)$$

where $xxRMS_0$ is the initial xRMS register value before offset calibration.

For example, if the expected the AIRMS at 1000:1 is 52,702,092/1000 = 52,702 (decimal) and the AIRMS register reading is 53280 (decimal), the offset calibration register is

$$AIRMSOS = \frac{52702^2 - 53280^2}{2^{15}} = -1869d = 0\text{xFFFF8B8}$$

Table 8 shows the rms settling time to 99% of full scale for a 50 Hz signal.

Table 8. RMS Settling Time

Configuration	RMS Settling Time, FS = 99% (sec)
Integrator On, HPF On, and LPF2 On	0.54
Integrator Off, HPF On, and LPF2 On	0.48

Neutral Current RMS, Vector Current Sum

The ADE9000 calculates the neutral current rms from a neutral current sensor input into the INP and INN pins, and stores the result in the NIRMS register. A NIRMSOS register allows offset calibration of this measurement. The scaling is the same as for the other xIRMS and xIRMSOS registers (see the Filter-Based Total RMS section for more information).

The ADE9000 also calculates the rms of the sum of IA + IB + IC ± IN and stores the result in the ISUMRMS register. The ISUMRMSOS register allows offset calibration of this measurement. The scaling is the same as for the other xIRMS and xIRMSOS registers (see the Filter-Based Total RMS section for more information).

If a neutral current sensor is not used, write the ISUM_CFG[1:0] bits in the CONFIG0 register equal to 0, and then ISUMRMS approximates the neutral current from the sum of IA, IB, and IC.

If the measured neutral current, NI_PCF, deviates from the sum of AI_PCF + BI_PCF + CI_PCF current channel waveforms, there may be a fault in the system.

To determine how large the mismatch is between the measured neutral current and the measured A, B, and C currents, select ISUM_CFG[1:0] to 01 or 10 based on the direction of the neutral current with respect to the other current channel waveforms.

Table 9. ISUM Configuration Options

CONFIG0.ISUM_CFG[1:0]	ISUM calculation
00, 11	ISUM = AI_PCF + BI_PCF + CI_PCF
01	ISUM = AI_PCF + BI_PCF + CI_PCF + NI_PCF
10	ISUM = AI_PCF + BI_PCF + CI_PCF − NI_PCF

ISUMRMS has the same scaling as xIRMS. Note that if AI_PCF, BI_PCF, and CI_PCF are all at full scale and in phase with each other, with the ISUM_CFG[1:0] equal to 00 or 11, ISUMRMS is 3 × 52,702,092 = 158,106,276 (decimal). If AI_PCF, BI_PCF, CI_PCF, and NI_PCF are all at full scale and in phase with each other, with the ISUM_CFG[1:0] equal to 01, ISUMRMS is 4 × 52,702,092 = 210,808,368 (decimal).

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To obtain an indication if ISUMRMS exceeds a threshold, configure ISUMLVL. Then the MISMTCH bit in STATUS0 and associated interrupt indicate if there is a change in the relationship between ISUMRMS and ISUMLVL.

Calculate the desired value of ISUMLVL according to the following equation:

$$ISUMLVL = \left(\frac{xIRMS\_FULL\_SCALE}{X}\right) \quad (12)$$

where:
xIRMS_Full_Scale is the nominal xIRMS value with full-scale inputs, 52,702,092.
X is the desired current level to indicate a MISMTCH error.

For example, to set ISUMLVL to warn about a vector current sum greater than 10,000:1 from full scale, X = 10,000 in the previous equation.

Total Active Power

Total active power is commonly used for billing purposes. It includes power on the fundamental and on the harmonics.

The total active power on each phase is calculated by first multiplying the xI_PCF and xV_PCF waveforms. Then the result is low-pass filtered, unless the DISAPLPF bit in the CONFIG0 register is equal to 1. Finally, the xPGAIN is applied to perform a gain correction and the xWATTOS value is applied to correct the watt offset.

Figure 16 shows the relationship between the I and V input signals and the instantaneous active power and low-pass filtered active power, assuming that I and V are at full scale with only the fundamental is present and a power factor of 1.

If the DISAPLPF bit in the CONFIG0 is equal to 1, xWATT reflects the instantaneous active power; and if it is equal to 0, xWATT reflects the low-pass filtered active power, in Figure 16, assuming xPGAIN = 0 and xWATTOS = 0.

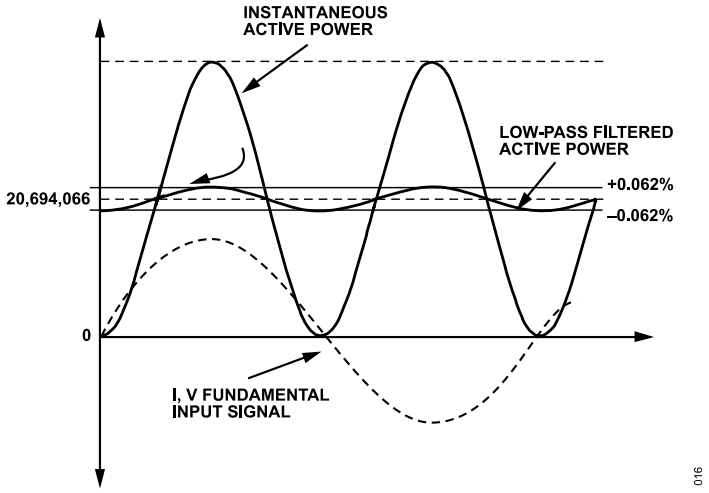

Figure 16. Instantaneous Active Power and Low-Pass Filtered Active Power at a Power Factor of 1

The low-pass filter, LPF2, extracts the total active power, attenuating harmonics of a 50 Hz or 60 Hz fundamental by 64 dB so that, at full scale, the variation in the low-pass filtered active power is very small, ±0.062%.

The resulting xWATT signal has an update rate of 8 ksps and a bandwidth of 3.2 kHz.

The xPGAIN register has the same scaling as the xIGAIN register. xWATTOS has the same scaling as xWATT. xWATT can be calibrated using the energy or power registers. When using the power registers, xWATTOS is calculated using the following equation:

$$xWATTOS = xWATT_{EXPECTED} - xWATT_{MEASURED} \quad (13)$$

The xWATT value with full-scale inputs and no gain is 20,694,066. Note that xVAR and VA have the same scaling; therefore, the same equation can be used for all three offsets.

The variable X is the smallest power level to calibrate. For example, to calibrate the energy at 10,000 from full scale, X = 10,000 in the previous equation.

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$$xWATTOS = \frac{1}{\frac{20694066}{10,000}} = 0.05\,\%$$

Then each bit in the xWATTOS register can correct an error of 0.05% at 10,000:1. Note that in most applications, the total active power performance with small inputs is sufficient with xWATTOS at zero.

Table 10 shows the settling times for total active power for a 50 Hz signal.

Table 10. Total Active Power Settling Time

	Total Active Power Settling Time (sec)	
Configuration	**FS = 99%**	**FS = 99.90%**
Integrator On, HPF On, and LPF2 On	0.43	0.66
Integrator Off, HPF On, and LPF2 On	0.43	0.66
Integrator Off, HPF On, and LPF2 Off	0.01	0.06

Total Reactive Power

Total reactive power includes reactive power on the fundamental and on the harmonics. The current channel, xI_PCF, is shifted by 90° at the fundamental and at all harmonics. This signal is then multiplied by the voltage waveform, xV_PCF. The result is then low-pass filtered, unless the DISRPLPF bit in the CONFIG0 register 1. Finally, the xPGAIN value is applied to perform a gain correction, and the xVAROS value is applied to correct the VAR offset. Note that in most applications, the total reactive power performance with small inputs is sufficient with xVAROS at zero.

The total reactive power at a power factor of 0 has a similar ripple to the total active power at a power factor of 1 (see Figure 16).

The resulting AVAR signal has an update rate of 8 ksps and a bandwidth of 3.2 kHz.

It is possible to disable the reactive power calculation by setting the VARDIS bit in the VAR_DIS register. This bit must be set before writing the RUN bit for proper operation.

The total reactive power offset can be calibrated for even better performance over a wide dynamic range using the xVAROS register. xVAROS has the same scaling as xVAR; see the Total Active Power section to understand how to calculate this register value. Table 11 shows the settling times for total reactive power for a 50 Hz signal.

Table 11. Total Reactive Power Settling Time

	Total Reactive Power Settling Time (sec)	
Configuration	**FS = 99%**	**FS = 99.90%**
Integrator On, HPF On, and LPF2 On	0.43	0.59
Integrator Off, HPF On, and LPF2 On	0.43	0.59
Integrator Off, HPF On, and LPF2 Off	0.02	0.05

Total Apparent Power

Apparent power is generated by multiplying the current rms measurement, xIRMS, by the corresponding voltage rms, xVRMS, and then applying a gain correction, xPGAIN. The result is stored in the xVA register. Note that the offset of the total apparent power calculation is performed by calibrating the xIRMS and xVRMS measurements, using the xIRMSOS and xVRMSOS registers; see the Filter-Based Total RMS section for more information on the rms calculation.

The resulting xVA signal has an update rate of 8 ksps and a bandwidth of 3.2 kHz.

In some applications, if there is a tamper detected on the voltage channel inputs, it is desirable to accumulate the apparent energy assuming that the voltage were at a nominal level. The ADE9000 offers a register, VNOM, which can be set to a value to correspond to, for example, 240 V rms. If the VNOMx_EN bits in the CONFIG0 register are set, VNOM is multiplied by xIRMS when calculating xVA.

Table 12 shows the settling times for total apparent power for a 50 Hz signal.

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Table 12. Total Apparent Power Settling Time

Configuration	Total Apparent Power Settling Time, FS = 99% (sec)
Integrator On, HPF On, and LPF2 On	0.54

Fundamental Measurements

The ADE9000 uses a proprietary algorithm to extract the fundamental from the total measured signal to make measurements including fundamental IRMS, VRMS, WATT, VAR, VA, ITHD, and VTHD. This algorithm requires initialization of the network frequency and of the nominal voltage measured in the voltage channel. The SELFREQ bit in the ACCMODE register selects whether the system is 50 Hz or 60 Hz. For a 50 Hz system, clear the SELFREQ bit; for a 60 Hz system, set the SELFREQ bit to 1. The SELFREQ selection must be made prior to writing the RUN register to 1.

The VLEVEL register indicates the nominal value of the voltage channel. Calculate VLEVEL according to this equation:

$$VLEVEL = X \times 1{,}144{,}084 \quad (14)$$

where X is the dynamic range that nominal input signal is at with respect to full scale.

It is recommended to set the voltage channel input so that the nominal voltage (for example, 240 V rms) corresponds to one half of the analog input signal range of the ADE9000. The ADE9000 can support ±1 V peak, 0.707 V rms inputs; therefore, it is recommended to scale the voltage channel inputs to 0.353 V rms. Then, with a nominal 240 V, the input signal is at half of full scale and X is equal to 2. Write 2,288,168 (decimal) to the VLEVEL register to configure this feature:

$$VLEVEL = 2 \times 1{,}144{,}084 = 2{,}288{,}168$$

After configuring these two parameters, SELFREQ and VLEVEL, the ADE9000 tracks the fundamental line frequency within ±5 Hz of the 50 Hz or 60 Hz frequency selected in SELFREQ. If a larger frequency range than ±5 Hz is required in the application, monitor the line period, xPERIOD, and change the SELFREQ selection accordingly. Note that the RUN register must be set to zero before changing the SELFREQ setting and then be set to one again.

Fundamental RMS

The ADE9000 offers fundamental current and voltage rms measurements using the proprietary fundamental estimation technique described in the Fundamental Measurements section. The xIFRMSOS and xVFRMSOS registers allow the offset to be calibrated for even better performance at low input signal levels.

Note that the xFRMS register does not read 0 with the xP and xN inputs shorted together.

The fundamental rms calculations, one for each channel, AIFRMS, BIFRMS, CIFRMS, AVFRMS, BVRMS, and CVRMS, are updated every 8 ksps. Note that there the neutral current channel does not have a fundamental rms measurement.

The xFRMS value at full scale is 52,702,092 (decimal).

For high performance at small input signals, below 1000:1, it is recommended to calibrate the offset of this measurement using the xFRMSOS register. It is recommended to calibrate the offset at the smallest input signal which requires good performance; do not calibrate this measurement with zero input signal.

The following equation indicates how the xFRMSOS register value modifies the result in the xFRMS register.

$$xxFRMS = \sqrt{xxFRMS_0{}^2 + 2^{15} \times xxFRMSOS} \quad (15)$$

where $xxFRMS_0$ is the initial xFRMS register value before offset calibration.

Fundamental Active Power

The ADE9000 offers fundamental active power measurements using the proprietary fundamental estimation technique. The fundamental active power is then gained by xPGAIN and offset correction is applied according to the xFWATTOS register.

The xFWATTOS register allows offset calibration to provide even better performance with low input signal levels. Figure 17 shows the signal chain for the AFWATT measurement.

MEASUREMENTS

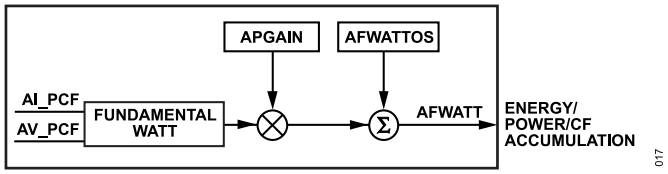

Figure 17. Fundamental WATT, AFWATT Calculation

xFWATTOS has the same scaling as xFWATT; see the Total Active Power section to understand how to calculate this register value.

Fundamental Reactive Power

The ADE9000 offers fundamental reactive power measurements using the proprietary fundamental estimation technique. This is then gained by xPGAIN and offset correction is applied according to the xFVAROS register. Figure 18 shows the signal chain for the AFVAR measurement.

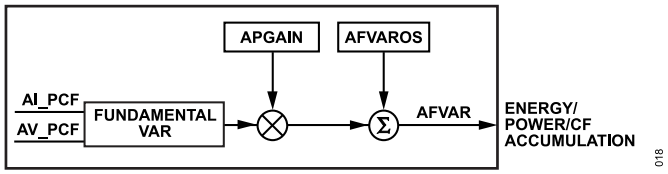

Figure 18. Fundamental Reactive Power, AFVAR

The fundamental reactive power at a power factor of 0 has a similar ripple to the total active power at a power factor of 1 (see Figure 16).

xFVAROS has the same scaling as xFVAR; see the Total Active Power section to understand how to calculate this register value.

Fundamental Apparent Power

The ADE9000 offers fundamental rms measurements using the proprietary fundamental estimation technique described in the Fundamental Measurements and Fundamental RMS sections. The fundamental rms measurements, xIFRMS and xVFRMS, are multiplied together to obtain fundamental apparent power. This is then gained by xPGAIN and stored in the xFVA register. Figure 19 shows the signal chain for the AFVA measurement.

Note that offset correction can be performed by calibrating the AIFRMS and AVFRMS measurements.

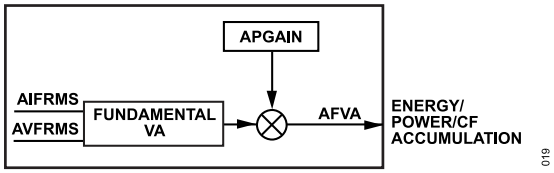

Figure 19. Fundamental Apparent Power, AFVA

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ENERGY MEASUREMENTS OVERVIEW

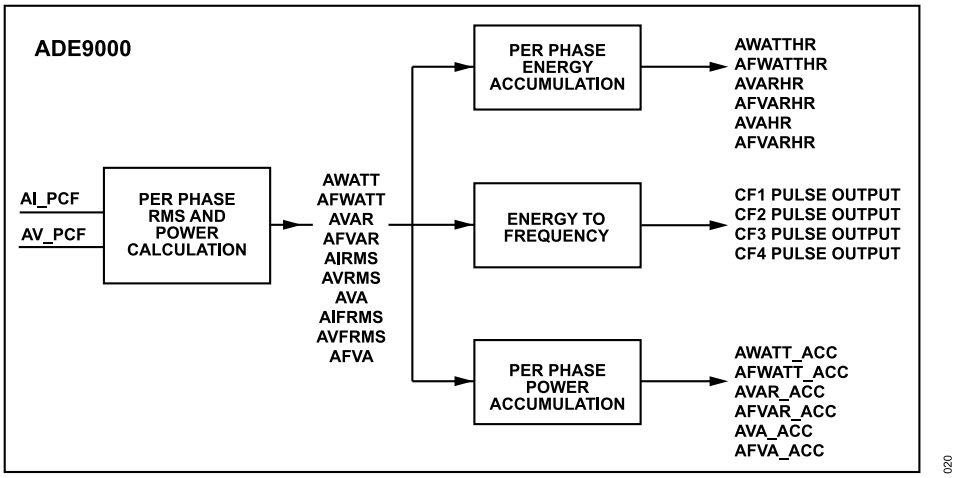

Figure 20. Per Phase Power and Energy Calculations from xI_PCF and xV_PCF Waveforms

Figure 20 shows how AI_PCF and AV_PCF are used to calculate per phase rms and power calculations and how these are accumulated into the AWATTHR and AWATT_ACC registers, as well as the CFx pulse outputs.

Per Phase Energy Measurements Update Rate

Instantaneous power measurements, including as xWATT, xVAR, xVA, and xFVAR, update at a rate of f_{DSP} = 8 ksps.

These measurements are accumulated into power measurements in the xWATT_ACC register, which updates at a user defined interval of up to 1 sec, depending on the selection in the PWR_TIME register.

Energy measurements update every f_{DSP} = 8 ksps by default and can store up to 106 sec of accumulation at full scale. Alternatively, these registers can be set into a different accumulation mode where they update after a user defined number of line cycles or samples.

Power factor, ITHD, and VTHD measurements update every 4096/8 ksps = 1.024 sec.

RMS½ measurements update every ½ line cycle (10 ms at 50 Hz).

10 cycle rms/12 cycle rms measurements update every 10 cycles on a 50 Hz network, or 12 cycles on a 60 Hz network. The SELFREQ bit in the ACCMODE register defines which network is being used.

Table 13. Watt Related Register Update Rates

Register Name	Description	Update Rate
AWATT	Low-pass filtered total active power on Phase A	8 ksps
BWATT	Low-pass filtered total active power on Phase B	8 ksps
CWATT	Low-pass filtered total active power on Phase C	8 ksps
AWATT_ACC	Accumulated total active power on Phase A	After the PWR_TIME 8 ksps samples, from 250 µs to 1.024 sec
BWATT_ACC	Accumulated total active power on Phase B	After the PWR_TIME 8 ksps samples, from 250 µs to 1.024 sec
CWATT_ACC	Accumulated total active power on Phase C	After the PWR_TIME 8 ksps samples, from 250 µs to 1.024 sec
AWATTHR	Accumulated total active energy on Phase A	According to the settings in EP_CFG and EP_TIME; holds up to 106 sec of energy at full scale.
BWATTHR	Accumulated total active energy on Phase B	According to the settings in EP_CFG and EP_TIME; holds up to 106 sec of energy at full scale.
CWATTHR	Accumulated total active energy on Phase C	According to the settings in EP_CFG and EP_TIME; holds up to 106 sec of energy at full scale.
APF	Phase A power factor[1]	Every 1.024 sec
BPF	Phase B power factor [1]	Every 1.024 sec

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Table 13. Watt Related Register Update Rates (Continued)

Register Name	Description	Update Rate
CPF	Phase C power factor [1]	Every 1.024 sec

[1] See the Power Factor section.

ENERGY ACCUMULATION

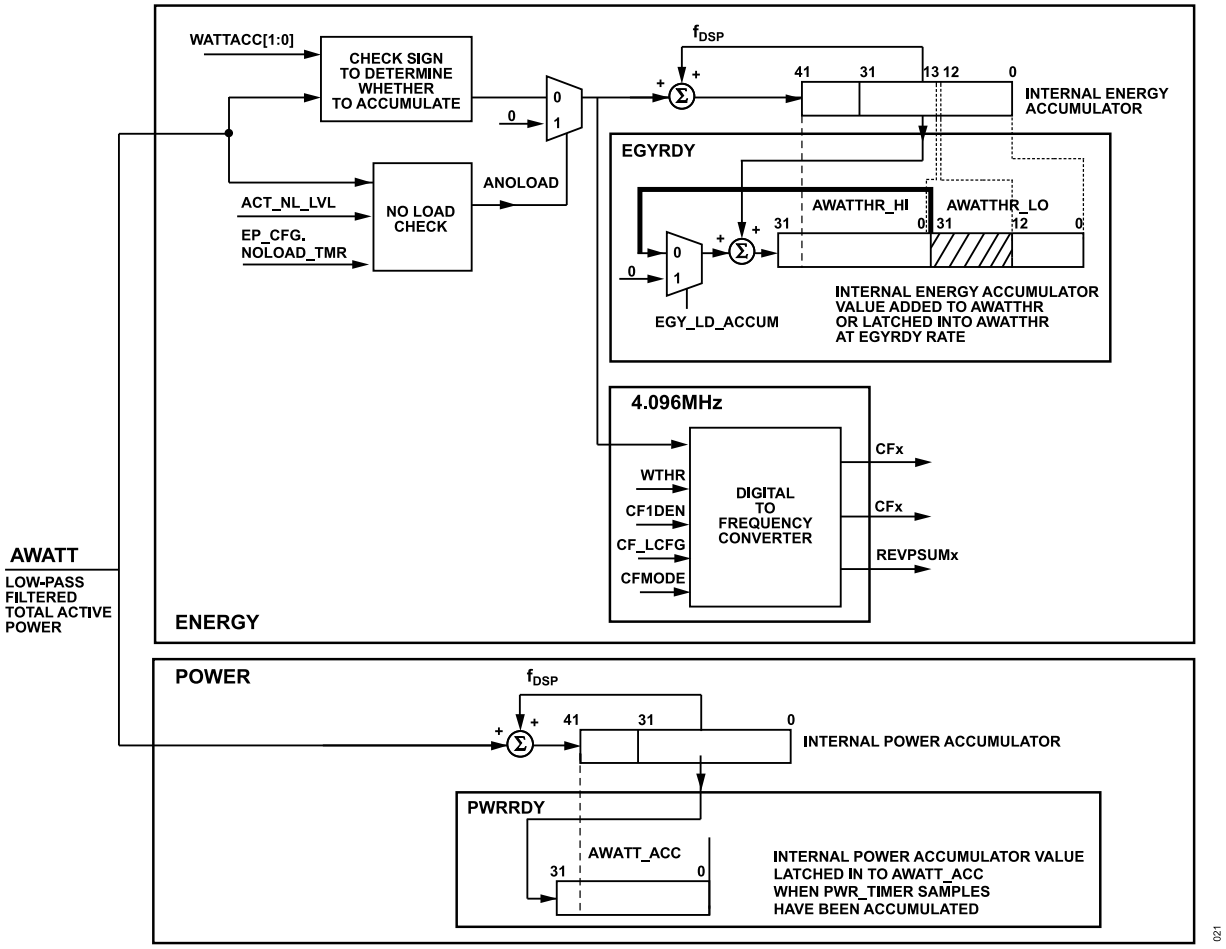

Figure 21. AWATT Accumulation into Energy and Power, Using No-load Threshold and Signed Accumulation Mode

Figure 21 shows how AWATT is accumulated into the AWATTHR and AWATT_ACC registers. A no-load threshold is applied and the energy is checked to determine whether to accumulate the AWATT sample into the internal energy accumulator. The internal energy accumulator is either added to the AWATTHR register or overwrites it at a EGYRDY rate. Set the EGY_PWR_EN bit in EP_CFG register to run the energy and power accumulator.

Signed Energy Accumulation Modes

Total Active Energy Accumulation Modes

In some installations, it is desirable to bill for only positive total active energy. The ADE9000 offers a way to do this using the WATTACC[1:0] bits in the ACCMODE register. To set the total and fundamental active energy accumulation and any corresponding CF pulse output for positive energy only, write WATTACC[1:0] to 10.

If WATTACC[1:0] is equal to zero, the energy accumulation is signed. The MSB of the AWATTHR_HI and AFWATTHR_HI registers indicates whether the accumulated energy is negative or positive.

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Other accumulation modes include absolute accumulation mode with WATTACC[1:0] equal to 01 (where the absolute value of AWATT is accumulated), and negative only accumulation mode with WATTACC[1:0] equal to 11 (where only negative active energy is accumulated).

Reactive Energy Accumulation Modes

In some installations, because reactive energy can change frequently between positive and negative values with inductive and capacitive loads, it is desirable to bill for the absolute value of reactive energy. The ADE9000 offers a way to do this using the VARACC[1:0] bits in the ACCMODE register. To set the total and fundamental reactive energy register and any corresponding CF pulse output to accumulate the absolute value of reactive energy, write VARACC[1:0] to 01.

If VARACC[1:0] is equal to zero, the total and fundamental reactive energy accumulation is signed. The MSB of the AVARHR_HI and AFVARHR_HI registers indicates whether the energy is negative or positive.

Other accumulation modes offered include positive only accumulation mode with VARACC[1:0] equal to 10, and negative only accumulation mode (where only negative reactive energy is accumulated) with VARACC[1:0] equal to 11.

No-Load Detection

No-load detection prevents energy accumulation due to noise, when the input currents are below a given meter start current.

To determine if a no-load condition is present, the ADE9000 evaluates if the accumulated energy is below a user defined threshold over a user defined time period, which is done on a per phase and per energy basis.

The NOLOAD_TMR[2:0] bits in the EP_CFG register determine whether to evaluate the no-load condition over 64 samples to 4096 samples, 64/8 ksps = 8 ms to 512 ms, by writing to the bits in the EP_CFG register, as described in Table 14. No-load detection is enabled by default, over the minimum time of 64/8 ksps = 8 ms. No-load detection is disabled when the NOLOAD_TMR[2:0] bits in the EP_CFG are equal to 111 (binary).

Table 14. No-Load Condition Evaluation Time

NOLOAD_TMR[2:0]	Samples to Evaluate No Load Over (Y)	Time that No-Load Detection is Evaluated Over
0	64	8 ms
1	128	16 ms
2	256	32 ms
3	512	64 ms
4	1024	128 ms
5	2048	256 ms
6	4096	512 ms
7	No-load disabled	No-load disabled

The user defined no-load thresholds are written into the ACT_NL_LVL, REACT_NL_LVL, and APP_NL_LVL registers. The ACT_NL_LVL register sets the no-load threshold for total and fundamental active energy. Correspondingly, the REACT_NL_LVL register sets the no-load threshold for total and fundamental reactive energy while the APP_NL_LVL sets the no-load threshold for total and fundamental apparent energy.

The no load thresholds are calculated according to the following equation:

$$xNL\_LVL = \left(\frac{xWATT\_Full\_Scale \times Y}{X}\right) \quad (16)$$

where:

xWATT_Full_Scale is the nominal xWATT value with full-scale inputs, 20,694,066. Note that xVAR and VA have the same scaling; therefore, the same value can be used for all three thresholds.

Y is the samples to Evaluate no-load over see Table 14.

X is the desired no-load input power level. For example, to set the no-load threshold to zero out energy below 50,000 from full scale, X = 50,000 in the previous equation.

Then, for a 50,000:1 no-load threshold level, xNL_LVL is 0x6804:

$$xNL\_LVL = \left(\frac{20,694,066 \times 64}{50000}\right) = 26,488 = 0x6778$$

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When a phase is in no-load, every f_{DSP} = 8 ksps, zero energy is accumulated into the energy registers and CF accumulation.

Note that the x_ACC registers are not affected by no-load detection. Even when in no-load, any power calculated in the respective xWATT, xVAR, and xVA registers is accumulated into the corresponding x_ACC register every f_{DSP} = 8 ksps.

No-Load Indications

The PHNOLOAD register indicates whether each phase of energy is in no-load. For example, the PHATNL[2:0] bits in the PHNOLOAD register indicate whether the Phase A total apparent energy, reactive energy, and active energy are in phase on Bit 2 through Bit 0, respectively. If a bit is set, it indicates that the phase energy is in no-load; if it is clear, the phase is not in no-load.

The user can enable an interrupt to occur when one of the per phase energy no-load status changes, either going into or out of no-load. There is an interrupt enable bit for each type of energy. Set the VAFNOLOAD, RFNOLOAD, AFNOLOAD, VANLOAD, RNLOAD, and ANLOAD bits in the STATUS1 register to enable an interrupt on $\overline{IRQ1}$ when one or more phases of fundamental VA, fundamental VAR, fundamental watt, total VA, total VAR, and total watt no-load changes status.

There is also an option to indicate the no-load status on the $\overline{EVENT}$ pin; see the Interrupts/EVENT section for more information.

Figure 22 shows what happens when the xWATT, low-pass filtered watt, value goes above the user configured no-load threshold and then back down below it again. The same concept applies to all of the energy values (total and fundamental VAR, total VA) with the corresponding REACT_NL_LNL and APP_NL_LVL no-load thresholds.

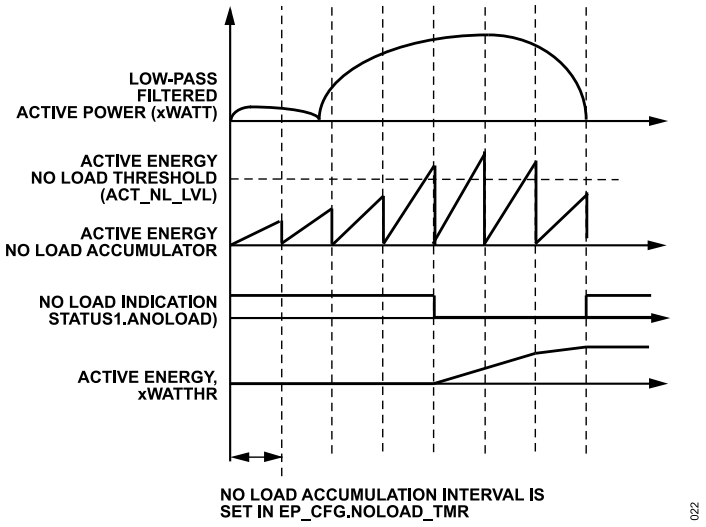

Figure 22. No-Load Detection and Indication

Energy Accumulation Details

Internal Energy Register Overflow Rate

There are 42-bit internal signed energy accumulators for each phase of each energy accumulation, as shown in Figure 21. These accumulators update at a rate of f_{DSP} = 8 ksps. The following equation shows how to calculate the time until the internal accumulator overflows with full-scale inputs and all digital gain and offset factors at zero, where AWATT_AT_FULL_SCALE refers to the nominal AWATT value with full scale inputs.

$$Maximum\ \ Internal\ \ Energy\ \ Accumulator\ \ Time\ \ (\text{sec}) = \left(\frac{2^{41}}{AWATT\_AT\_FULL\_SCALE \times f_{DSP}}\right) \quad (17)$$

For example, with CONFIG0.MTEN equal to zero, for single-point gain compensation and AIGAIN, AVGAIN, APGAIN, and AWATTOS all equal to zero, the Phase A total active energy has a digital gain of 1. Then, the Phase A total active energy accumulated in the internal accumulator overflows in 13.3 sec with the nominal full-scale AWATT value of 20,694,066.

$$Maximum\ \ Internal\ \ Energy\ \ Accumulator\ \ Time\ \ (\text{sec}) = \left(\frac{2^{41}}{20,694,066 \times 8000}\right) = 13.3\ \ \text{sec}$$

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User Energy Register Update Rate, EGYRDY

As shown in Figure 21, the internal energy accumulator is latched into a user accessible energy register or added to user accessible register at a rate of EGYRDY. Figure 23 further describes how the EGYRDY update rate is generated.

The EGYRDY update rate occurs after EGY_TIME + 1 f_{DSP} samples or EGY_TIME + 1 half line cycles, according to the EGY_TMR_MODE bit in the EP_CFG register.

If EGY_TMR_MODE is zero, the internal energy register accumulates for EGY_TIME + 1 samples at 8 ksps. This mode is called sample-based accumulation.

$$Internal\ \ Energy\ \ Accumulation\ \ Time\ \ (\text{sec}) = \left(\frac{EGY\_TIME + 1}{f_{DSP}}\right) \quad (18)$$

The EGY_TIME[12:0] register allows up to (8191 + 1) = 8192 samples to be accumulated, which corresponds to 8192/8000 = 1.024 sec if EGY_TMR_MODE is equal to zero.

$$Internal\ \ Energy\ \ Accumulation\ \ Time\ \ (\text{sec}) = \left(\frac{8191 + 1}{8000}\right) = 1.024\ \ \text{sec}$$

If EGY_TMR_MODE is 1, the internal energy register accumulates for EGY_TIME + 1 half line cycles at 8 ksps. This mode is called half line cycle-based accumulation. In this mode, the zero-crossing source to monitor is set by ZX_SEL bits in the ZX_LP_SEL register, as shown in Figure 23.

$$Internal\ \ Energy\ \ Accumulation\ \ Time\ \ (\text{sec}) = \frac{EGY\_TIME + 1}{ZX\ \ Rate} \quad (19)$$

With a 50 Hz line frequency, the ZX interrupt rate is 100 Hz, then the maximum accumulation time is 81.92 sec with EGY_TIME equal to 0x1FFF, 8191 (decimal):

$$Internal\ \ Energy\ \ Accumulation\ \ Time\ \ (\text{sec}) = \frac{8191 + 1}{100\ \ \text{Hz}} = 81.92\ \ sec$$

Note that the internal energy register overflows in 13.3 sec with full-scale inputs; therefore, EGY_TIME must be set lower than 1329 (decimal) to prevent overflow when EGY_TMR_MODE is 1.

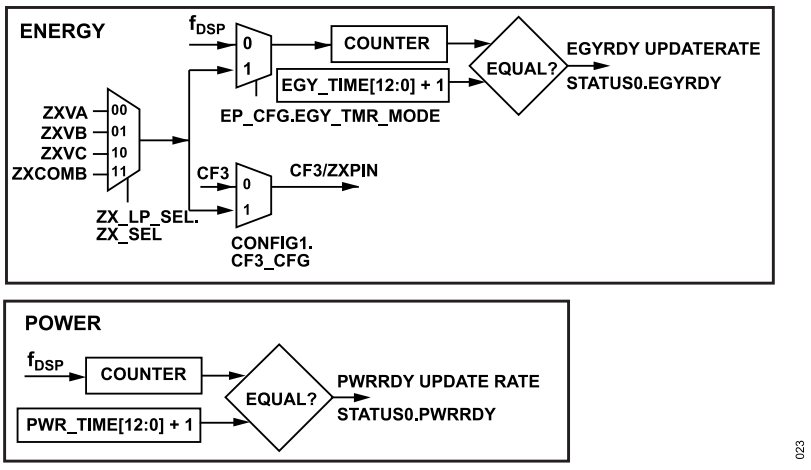

Figure 23. EGYRDY and PWRRDY Update Rate

Reloading or Accumulating User Energy Register

When the EGYRDY event happens, the internal energy accumulation is either directly loaded into the xWATTHR register or added to the existing accumulation based on the state of the EGY_LD_ACCUM bit in the EP_CFG register. The internal energy register is reset and starts counting again from zero.

If EGY_LD_ACCUM is equal to zero, the internal energy register is added to the user accessible energy register. If EGY_LD_ACCUM is equal to one, the internal energy register overwrites the user accessible energy register.

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User Energy Register Overflow Rate

The energy registers in the ADE9000 are signed and 45 bits wide, split between two 32-bit registers, as shown in Figure 24. These accumulators update at a rate according to EGYRDY, as described in the User Energy Register Update Rate, EGYRDY section. The following equation shows how to calculate the time until the user accessible accumulator overflows with full-scale inputs and all digital gain and offset factors at zero, where AWATT_AT_FULL_SCALE refers to the nominal AWATT value with full-scale inputs. For this example, assume that the internal energy register is updating at every f_{DSP} = 8 ksps sample.

$$Maximum\ \ Internal\ \ Energy\ \ Accumulator\ \ Time\ \ (\text{sec}) = \left(\frac{2^{44}}{AWATT\_AT\_FULL\_SCALE \times f_{DSP}}\right) \quad (20)$$

For example, with the MTEN bit in the CONFIG0 register equal to zero, for single-point gain compensation and AIGAIN, AVGAIN, APGAIN, and AWATTOS all equal to zero, the Phase A total active energy has a digital gain of 1. Then, the Phase A total active energy accumulated in the user accessible accumulator overflows in 106.4 sec with the nominal full-scale AWATT value of 20,694,066.

$$Maximum\ \ Internal\ \ Energy\ \ Accumulator\ \ Time\ \ (\text{sec}) = \left(\frac{2^{44}}{20,694,066 \times 8000}\right) = \ \ 106.3\ \ \text{sec}$$

Accessing the User Energy Registers

Each 45-bit user accessible signed energy accumulator is divided into two registers: a register containing the 32 most significant bits, xHR_HI, and a register containing the 13 least significant bits, xHR_LO, as shown in Figure 24.

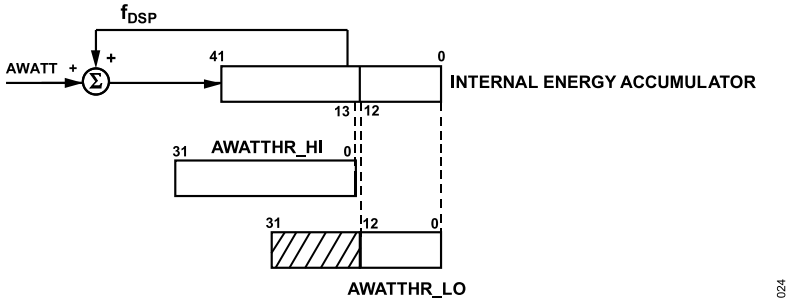

Figure 24. Internal Energy Register to AWATTHR_HI and AWATTHR_LO

The expected user energy accumulation can be calculated according to this formula based on the average AWATT value.

USER_ENERGY_ACCUMULATION = *AWATT* × (*EGY_TIME* + 1) (21)

Then, AWATTHR_HI contains the 32 most significant bits, which can be calculated by rounding the following equation down to the nearest whole number:

AWATTHR_HI = ROUNDDOWN (*USER_ENERGY_ACCUMULATION* × 2^{-13}) (22)

The 13 LSBs of USER_ENERGY_ACCUMULATION are stored in the AWATTHR_LO register.

Read User Energy Register With Reset

If the RD_RST_EN (do not use, see Errata section for more details) bit is set in the EP_CFG register, its contents are reset when a user accessible energy register is read.

For example, if AWATTHR_HI is read, the AWATTHR_HI register value goes to zero. The AWATTHR_LO register contents are not modified.

User Energy Register Use Models

There are two main use models for energy accumulation:

- Accumulate energy over a defined number of line cycles
- Accumulate energy over a defined number of samples

To accumulate energy over a defined number of half line cycles, use the following settings:

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- Configuration register settings:
  - EP_CFG register, EGY_LD_ACCUM bit = 1.
  - EP_CFG register, EGY_TMR_MODE bit = 1.
  - EP_CFG register, RD_RST_EN bit = 0.
  - EP_CFG register, EGY_PWR_EN bit = 1.
  - EGY_TIME register = desired number of half line cycles.
- Output:
  - The xHR_HI register has enough resolution for most applications.
  - To maintain perfect synchronization with CF pulse output, the xHR_LO register must be read as well, because it is cleared at every EGYRDY cycle.
- Maximum time before reading xHR_HI to prevent overflow with full-scale inputs: 13.3 sec.

To accumulate energy over a defined number of samples, use the following settings:

- Configuration register settings:
  - EP_CFG register, EGY_LD_ACCUM bit = 1
  - EP_CFG register, EGY_TMR_MODE bit = 0
  - EP_CFG register, RD_RST_EN bit = 0
  - EP_CFG register, EGY_PWR_EN bit = 1
  - EGY_TIME register = desired number of samples
- Output:
  - The xHR_HI register has enough resolution for most applications.
  - To maintain perfect synchronization with CF pulse output, the xHR_LO register must be read as well, because it is cleared at every EGYRDY cycle.
- Maximum time before reading xHR_HI to prevent overflow with full-scale inputs: 13.3 sec.

Digital to Frequency Conversion—CF Output

Many electricity meters are required to provide a pulse output that is proportional to the energy being accumulated, with a given pulse per kWh meter constant.

The ADE9000 includes four pulse outputs that are proportional to the energy accumulation, in the CF1 through CF4 output pins.

Energy and Phase Selection

The CFxSEL[2:0] bits in the CFMODE register select which type of energy to output on the CFx pin, including total or fundamental watt, VAR, and VA. Then, the TERMSELx bits in the COMPMODE register select which phase energies to include in the CF output.

For example, with the CFMODE register, CF1SEL[2:0] bits = 000 and the COMPMODE register, TERMSEL1[2:0] bits = 111, CF1 indicates the total watt output of Phase A, Phase B, and Phase C.

To calibrate the Phase A, Phase B, and Phase C total watt accumulation at the same time, using CF1 for total AWATT, CF2 for total BWATT, and CF3 for total CWATT, configure the CFMODE register, the CF1SEL, CF2SEL, and CF3SEL bits = 000; the COMPMODE register, TERMSEL0[2:0] bits = 001; the COMPMODE register, TERMSEL1[2:0] bits = 010; and the COMPMODE register, TERMSEL2[2:0] bits = 100

Configuring the Maximum CF Pulse Output Frequency

It is recommended to write xTHR = 0x0010_0000. CFxDEN can range from 2 to 65535. Configure CFxDEN to tune the CF frequency output. The relationship between the xTHR, CFxDEN, and AWATT values is given in the following equation:

$$CF \quad (\text{Hz}) = \left(\frac{f_{DTOF} \times AWATT}{xTHR \times 512 \times CFxDEN}\right) \tag{23}$$

Then, the maximum recommended CF pulse output frequency is 78.862 kHz.

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$$MAXIMUM\_CF(\text{Hz}) = \left(\frac{4.096 \times 10^6 \times 20,694,066}{0x0010\_0000 \times 512 \times 2}\right) = 78.9 \quad \text{kHz}$$

where:
f_{DTOF} is 4.096MHz.
AWATT is the value at full scale, 20,694,066.
xTHR is 0x0010_0000. *CFDEN* is 2.

The default CF pulse output using power-on reset values of xTHR and CFxDEN with full-scale inputs is

$$MAXIMUM\_CF(\text{Hz}) = \left(\frac{4.096 \times 10^6 \times 20,694,066}{0x0000\_FFFF \times 512 \times 0xFFFF}\right) = 38.5 \quad \text{Hz}$$

Configuring the CF Pulse Width

The pulse width is determined by the CFx_LT bit in the CF_LCFG register and the CF_LTMR register value.

With CFx_LT equal to zero, the active low pulse width is set at 80 ms for frequencies lower than 1/(2 × 80 ms) = 6.25 Hz. For higher frequencies, the duty cycle is 50% if CFxDEN is even, or (1 + 1/CFxDEN) × 50% if CFxDEN is odd.

If CFx_LT is set to 1, the CF active low pulse width is CF_LTMR × 6/CLKIN. The maximum CF_LTMR is 327680 = 0x0005_0000, which results in a 327680/(6/CLKIN) = 80 ms pulse. CF_LTMR must be greater than zero.

Table 15. CF Active Low Pulse Width and Duty Cycle based on CFx_LT and CF_LTMR

CFx_LT	Active Low Pulse Width for Low Frequencies (ms)	Active Low Pulse Width for High Frequencies when CFxDEN is Even	Active Low Pulse Width for High Frequencies when CFxDEN is Odd	Behavior when Entering No-Load
0	80	50%	(1 + 1/CFxDEN) × 50%	If CFx is low, finish current pulse, then return high.
1	CF_LTMR × 6/CLKIN × 1000	50%	(1 + 1/CFxDEN) × 50%	If CFx is low, keep CFx low until no-load state is finished.

CF Pulse Sign

Some applications must record positive and negative energy usage separately. To facilitate this, the SUMxSIGN bits in the PHSIGN register indicate whether the sum of the energy that went into the last CFx pulse was positive or negative. SUMxSIGN is zero if the sum of the energy that went into the CFx pulse is positive, and equal to one if the sum of the energy was negative.

Furthermore, the REVPSUMx bits in the STATUS0 register and EVENT_STATUS register indicate if the CF polarity changed sign. For example, if the last CF2 pulse represents positive reactive energy and the next CF2 pulse represents negative reactive energy, the REVPSUM2 bit in the STATUS0 and EVENT_STATUS registers is set. This event can be enabled to generate an interrupt on $\overline{\text{IRQ0}}$.

Clearing the CF Accumulator

It can be desirable to clear out a partial CF accumulation, for example, during the power-up and initialization process. To clear the accumulation in the digital to frequency converter and CFDEN counter, write the CF_ACC_CLR bit in the CONFIG1 register to 1. The CF_ACC_CLR bit automatically clears itself.

Disabling the CF Pulse Output and CFx Interrupt

To disable the CFx pulse output and keep the CFx output high, write a 1 to the CFx_DIS bit in the CFMODE register. If the CFx output is disabled, the CFx bit in STATUS0 is not set when a new CF pulse is ready. Note that the REVPSUMx bits, which indicate if CF pulses were positive or negative, are not affected by the CFx_DIS setting.

POWER ACCUMULATION

Figure 21 shows how AWATT low-pass filtered active power samples are accumulated to provide an accurate active power value in the AWATT_ACC register. The sign of the Phase A total active power accumulation is monitored in the REVAPA status bit, and interrupts can be enabled if the power changes sign. There are corresponding x_ACC accumulations for each power on each phase and REVx status bits in STATUS0 to indicate if the power changes sign.

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Power Accumulation Details

Figure 21 shows how AWATT values are accumulated into an internal power accumulator and then are latched into the xWATT_ACC register at a rate of PWRRDY.

PWRRDY is set after PWR_TIME + 1 samples at 8 ksps have been accumulated. The power accumulation time can be calculated according to the following equation:

$$Internal\ \ Power\ \ Accumulation\ \ Time\ \ (\text{sec}) = \left(\frac{PWR\_TIME + 1}{8000}\right)$$

The PWR_TIME[12:0] register allows up to (8191 + 1) = 8192 samples to be accumulated, which corresponds to 8192/8000 = 1.024 sec:

$$Internal\ \ Power\ \ Accumulation\ \ Time\ \ (\text{sec}) = \left(\frac{8091 + 1}{8000}\right) = 1.024\ \ \text{sec}$$

The internal power accumulator overflows at the same rate as the internal energy accumulator (see the Internal Energy Register Overflow Rate section).

Accessing the User Power Registers

Each 42-bit user accessible signed power accumulator is divided into a register containing the 32 most significant bits, x_ACC, as shown in Figure 24.

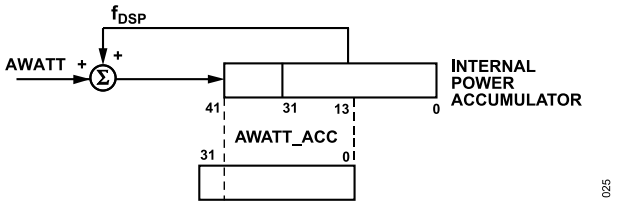

Figure 25. Internal Power Register to AWATT_ACC

The expected user power accumulation can be calculated according to this formula based on the average AWATT value.

USER_POWER_ACCUMULATION = *AWATT* × (*PWR_TIME* + 1) (24)

Then, expected data in the 32-bit power accumulation registers (xWATT_ACC, xVAR_ACC, and xVA_ACC) can be calculated as follows:

Power accumulation register = ROUNDDOWN(*USER_POWER_ACCUMULATION* × 2^{-13}) (25)

For example, if 4000 samples of AWATT are accumulated, at 8 ksps with full-scale inputs, the expected value of AWATT_ACC is 0x009B_0003:

USER_POWER_ACCUMULATION = 20,694,066 × (3999 + 1) = 82776264000

AWATT_ACC = ROUNDDOWN (82776264000 × 2^{-13}) = 10104524 = 0x009A_2ECC

To determine the consumption in watts, multiply xWATT_ACC by the W/LSB constant: xWATT_ACC × W/LSB.

Note that W/LSB varies with PWR_TIME accumulation time.

Power Sign Detection

The REVRPC, REVRPB, REVRPA, REVAPC, REVAPB, and REVAPA bits in the STATUS0 register allow the user to monitor if the active or reactive power on any phase has changed sign.

The PWR_SIGN_SEL[1:0] bits allow the user to select whether the power sign change follows the total or fundamental energies. To have the REVAPx power sign status bits track total watt, PWR_SIGN_SEL[0] = 0. To track fundamental VAR on REVRPx bits, write PWR_SIGN_SEL[1] = 1.

The CVARSIGN, CWSIGN, BVARSIGN, BWSIGN, AVARSIGN, and AWSIGN bits in the PHSIGN register indicate whether the total or fundamental VAR and WATT selected in the PWR_SIGN_SEL[1:0] bits are positive or negative.

The power signs are updated at the same time as the xWATT_ACC, xFWATT_ACC, xVAR_ACC, and xFVAR_ACC registers and correspond to the sign of these registers. Note that the power registers and signs are updated after the number of f_{DSP} = 8 ksps samples configured in the

MEASUREMENTS

PWR_TIME register have elapsed, from 250 µs to 1.024 sec. The power sign change indication in the REVxPx bits are updated at the same time; see the Power Accumulation Details section for more information.

The ADE9000 allows the user to accumulate total watt and VAR powers into separate positive and negative registers: PWATT_ACC and NWATT_ACC, PVAR_ACC and NVAR_ACC. This is done by evaluating the AWATT, low-pass filtered active power every 8 ksps. If the AWATT is positive, it is added to the PWATT_ACC accumulation. If the AWATT is negative, the absolute value is added to the NWATT_ACC accumulation. A new accumulation from zero begins when the power update interval set in PWR_TIMER has elapsed. The positive and negative total watt and total VAR from all three phases are added into the positive/negative watt and VAR accumulations.

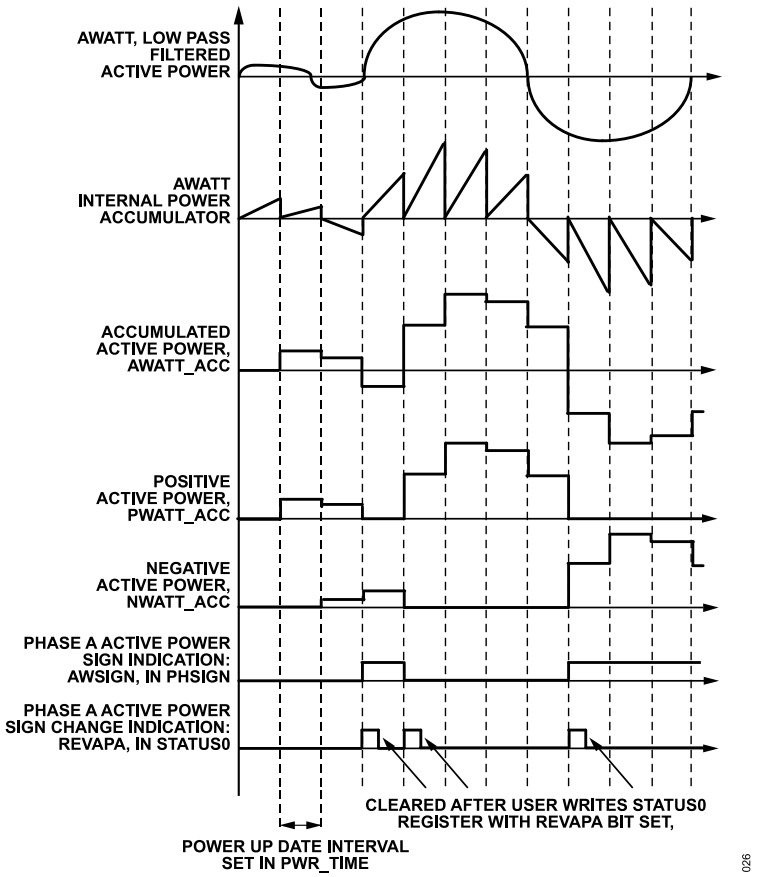

Figure 26. Power Accumulation and Power Sign

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE9000 offers zero-crossing detection on the VA, VB, VC, IA, IB, and IC input signals. The neutral current channel, IN, does not contain a zero-crossing detection circuit. The zero-crossing circuit is used as the time base for resampling, line period, angle measurements, and energy accumulation using line cycle accumulation mode. The xV_PCF and xI_PCF are the voltage and current channel waveforms processed by the DSP, and which can be stored into the waveform buffer at a 8 ksps data rate (see the Waveform Buffer section for more information).

The ZX_SRC_SEL bit in the CONFIG0 register sets whether data going into the zero-crossing detection circuit comes before or after the high-pass filter, integrator, and phase compensation. By default, the data after phase compensation is used. Note that the high-pass filter has 500 ms settling time with a step change in the input; therefore, for a fast response, it is recommended to set ZX_SRC_SEL to look for a zero-crossing before the high-pass filter. If a high-pass filter is disabled with the HPFDIS bit in the CONFIG0 register equal to 1, or if the ZX_SRC_SEL bit in the CONFIG0 register is equal to 1, note that a dc offset on the input may cause the time between negative to positive and positive to negative zero-crossings and positive to negative to negative to positive zero-crossings to change, indicating that the ZX detection does not have a 50% duty cycle.

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The current and voltage signals are low-pass filtered to remove harmonics. The low-pass filter, LPF1, has a corner of 82 Hz and the equation is as follows:

$$H(z) = \frac{2^{-4}}{1-\left(1-2^{-4}\right)z^{-1}}$$

The low-pass filter settling time is 71 samples, 71/8 ksps, which equals 8.875 ms.

Figure 27 shows the delay between the detected zero-crossing signal and the input. Note that there is a 4.3 ms delay between the input signal zero-crossing and the ZX zero-crossing indication, with a 50Hz input signal. Zero-crossings are generated on both negative to positive and positive to negative transitions.

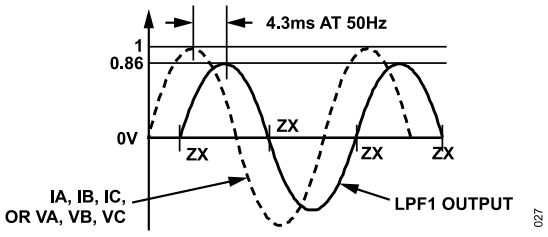

Figure 27. Zero-Crossing Detection on Voltage and Current Channels

To provide protection from noise, the voltage channel zero-crossing events (ZXVA, ZXVB, and ZXVC) are not generated if the absolute value of the LPF1 output voltage is smaller than the threshold, ZXTHRSH. The current channel ZX detection outputs (ZXIA, ZXIB, and ZXIC) are active for all input signals levels.

The zero-crossing threshold, ZXTHRSH, can be calculated from the following equation:

$$ZXTHRSH = \frac{(V\_PCF \quad at \quad Full \quad Scale) \times (LPF1\_ATTENUATION)}{X \times 32 \times 2^8} \tag{26}$$

where:
V_PCF at full scale is ±74,532,013 (decimal).
X is the dynamic range that the zero-crossing must be blocked below.
LPF1_ATTENUATION is 0.86 at 50 Hz and 0.81 at 60 Hz, the gain attenuation of the LPF1 filter.

For example, to prevent signals 100 times lower than full scale from generating a ZX output, set ZXTHRSH to 78 (decimal):

$$ZXTHRSH = \frac{(74,532,013) \times (0.86)}{100 \times 32 \times 2^8} = 78\text{d}$$

Additionally, to prevent false zero-crossings, after a ZX is generated, 1 ms must elapse before the next ZX can be output.

Combined Voltage Zero-Crossing

Phase A, Phase B, and Phase C voltage channel signals are combined to generate one zero-crossing signal, ZX_COMB, that is stable even if one or more phases drops out.

The input to the zero-crossing detection is (VA + VB − VC)/2 with the signal chain corresponding to Figure 28. As described in the Applying the ADE9000 to Different Metering Configurations section, the ADE9000 can be used to meter different polyphase configurations. The VCONSEL[2:0] bits in the ACCMODE register are used to indicate this selection. If VCONSEL[2:0] is not equal to 0, the VB component in the combined zero-crossing circuit is set to zero.

The same precautions are used to prevent noise from generating zero-crossing interrupts on this output. As described in the Zero-Crossing Detection section, signals below the ZXTHRSH threshold do not generate ZXCOMB outputs, and a minimum of 1 ms is required between ZXCOMB generation.

MEASUREMENTS

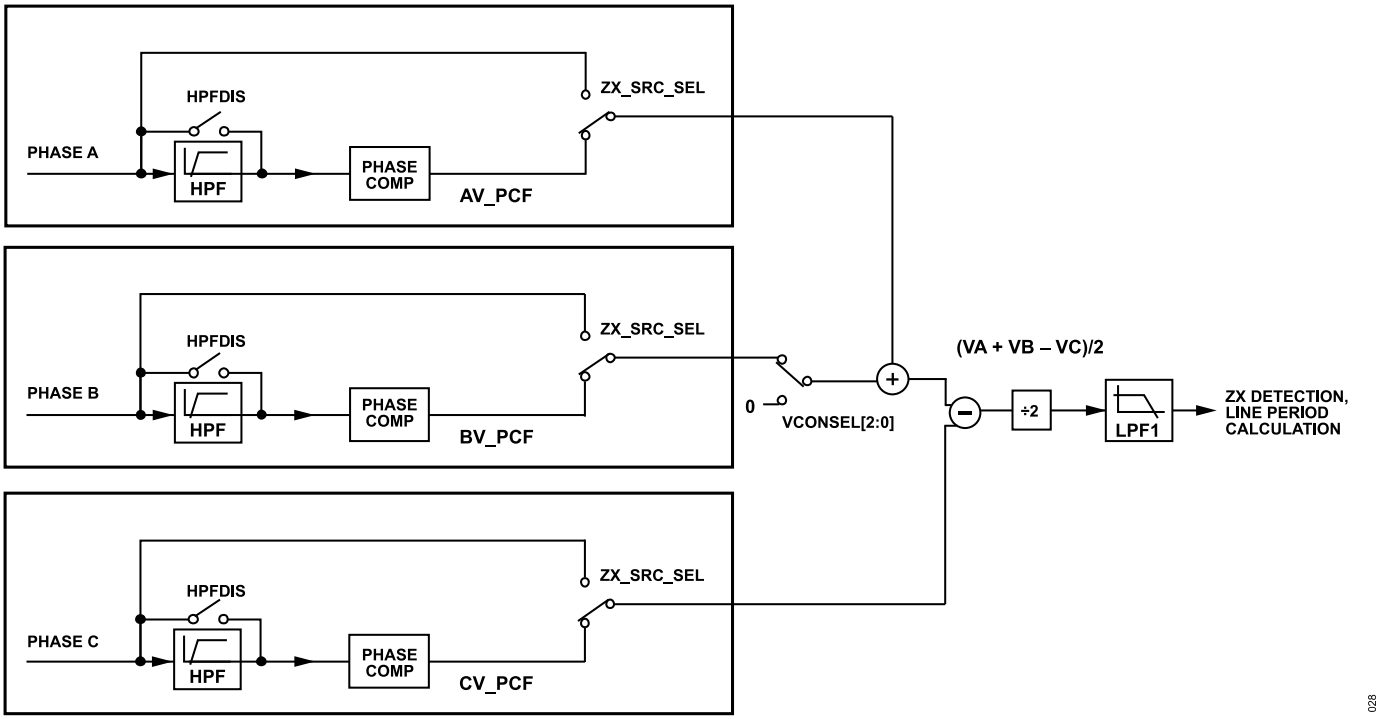

Figure 28. Combined Zero-Crossing Detection

Zero-Crossing Output Rates

There are seven zero-crossing detection circuits that monitor IA, IB, IC, VA, VB, VC, and the combined (VA + VB − VC)/2 signal. The zero-crossing detection circuits have two different output rates: 8 ksps and 1024 ksps. The 8 ksps zero-crossing signal is used to calculate the line period, sent to the ZXx bits in the STATUS1 register, and is monitored by the zero-crossing timeout, phase sequence error detection, resampling and energy accumulation functions. The 1024 ksps signal is used for angle measurements and is output on the CF3/ZX pin if the CF3_CFG bit in the CONFIG1 register is equal to 1.

Table 16 indicates which zero-crossing edges (negative to positive and positive to negative) are used for each function and indicates what happens if a zero-crossing is blocked because the input signal is below the user configured ZXTHRSH.

The CF3/ZX output pin goes from low to high when a negative to positive transition is detected and from high to low when a positive to negative transition occurs. The ZX_SEL[1:0] bits in the ZX_LP_SEL register select the zero-crossing output used for line cycle energy accumulation and the ZX output pin.

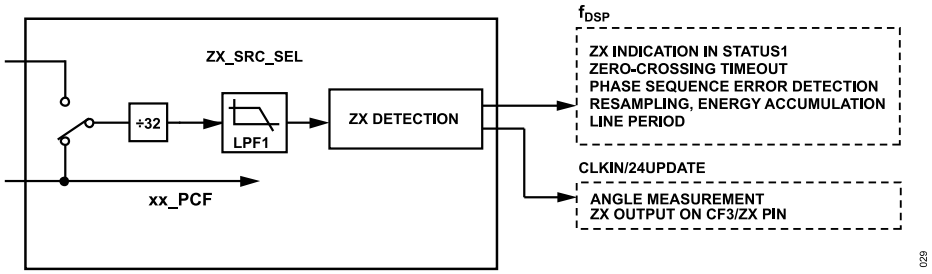

Figure 29. Zero-Crossing Output Rates

MEASUREMENTS

Table 16. Zero-Crossing Use in Other Functions

Functions Using Zero-Crossing	ZX Transitions Used	Corresponding STATUS1 Register Bits	Selecting which Phase to Use for Measurement	Effect if ZX Does Not Occur
ZX Indication in STATUS1 Register	Negative to positive, and positive to negative	ZXIA, ZXIB, ZXIC, ZXVA, ZXVB, ZXVC, ZXCOMB	Not applicable	ZXx bit is latched in STATUS1. If cleared, it is not set again. ZXx interrupt does not occur.
Zero-Crossing Timeout	Negative to positive, and positive to negative	ZXTOVA, ZXTOVB, ZXTOVC	Not applicable	Zero-crossing timeout is indicated by the ZXTOUT bit in the STATUS1 register and an interrupt can be enabled to occur.
Phase Sequence Error Detection	Depends on VCONSEL[2:0] setting	SEQERR	Not applicable	If one to two ZX events are missing, SEQERR is generated. If all ZX are missing then SEQERR bit is note set.
Energy Accumulation	Negative to positive, and positive to negative	Not applicable	ZX_LP_SEL.ZX_SEL[1:0] selects the zero-crossing output used for line cycle energy accumulation and ZX output pin.	Line cycle accumulation does not update.
Line Period Measurement	Negative to positive	Not applicable	Not applicable	Coerced to default value: 0x00A0_0000 if ACCMODE.SELFREQ = 0, for a 50 Hz network; 0x0085_5554 if ACCMODE.SELFREQ = 1, for a 60 Hz network.
Resampling, RMS½, 10 Cycle RMS/12 Cycle RMS	None	Not applicable	ZX_LP_SEL.LP_SEL[1:0] selects the phase voltage line period used as the basis for for these calculations.	If the selected line period is invalid because zero-crossings are not detected or the calculation results in something outside a 40 Hz to 70 Hz range, the line period used for the calculation is coerced to the default line period: 0x00A0_0000 if ACCMODE.SELFREQ = 0, for a 50 Hz network; 0x0085_5554 if ACCMODE.SELFREQ = 1, for a 60 Hz network.
Angle Measurements	Negative to positive	Not applicable	Not applicable	Does not update; keeps last value.
ZX Output on CF3/ZX Pin	Negative to positive, and positive to negative	Not applicable	ZX_LP_SEL.ZX_SEL[1:0] selects the zero-crossing output used for line cycle energy accumulation and ZX output pin.	Remains at current state; high or low.

Zero-Crossing Timeout

The zero-crossing timeout feature alerts the user if a zero-crossing event is not generated after a user configured amount of time. If a zero-crossing on is not received after ZXTOUT 8 ksps clocks, the corresponding ZXTOx bit in the STATUS1 register is set. For example, if ZXTOUT is equal to 8000, if a zero-crossing is not then received on Phase A for 8000/8 ksps = 1 sec, the ZXTOA bit is set in the STATUS1 register. The maximum value that can be written to the ZXTOUT register is 0xFFFF/8000 = 8.19 sec.

Line Period Calculation

The ADE9000 line period measurement is done by taking the values low-pass filtered by LPF1, as described in the Zero-Crossing Detection section, and then using the two values near the positive to negative zero-crossing to calculate the exact zero-crossing point using linear interpolation. This information is used to precisely calculate the line period, which is stored in the xPERIOD register.

MEASUREMENTS

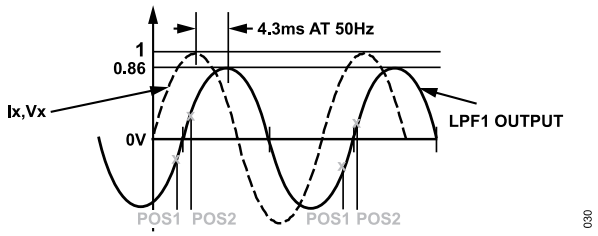

Figure 30. Line Period Calculation using Zero-Crossing Detection and Linear Interpolation

The line period, T_L, can be calculated from the xPERIOD register according to the following equation:

$$T_L = \frac{xPERIOD + 1}{8000 \times 2^{16}}(\text{sec}) \quad (27)$$

Similarly, the line frequency can be calculated from the xPERIOD register, using the following equation:

$$f_L = \frac{8000 \times 2^{16}}{xPERIOD + 1}(\text{Hz})$$

With a 50 Hz input, the xPERIOD register is 0x00A0_0000, 10485760 (decimal), and with 60 Hz, it is 0x0085_5554, 8738132 (decimal).

If the calculated period value is outside the range of 40 Hz to 70 Hz, or if the negative to positive zero-crossings for that phase are not detected, the xPERIOD register be coerced to correspond to 50 Hz or 60 Hz, according to the setting of the SELFREQ bit in the ACCMODE register. With SELFREQ equal to 0 for a 50 Hz network, the xPERIOD register is coerced to 0x00A0_0000. If SELFREQ is 1, indicating a 60 Hz network, the xPERIOD register is coerced to 0x0085_5554.

The line period is calculated for the Phase A, Phase B, and Phase C voltages and the combined voltage signal, as described in the Combined Voltage Zero-Crossing section, and stored in the APERIOD, BPERIOD, CPERIOD, and COM_PERIOD registers, respectively.

The line period calculation is used for the resampling measurement. Select which phase voltage line period is used as the basis for resampling calculation using the LP_SEL[1:0] bits in the ZX_LP_SEL register, or select a user configured value written in USER_PERIOD using the UPERIOD_SEL bit in the CONFIG2 register.

The user period selection can help in applications where the user has another algorithm to determine the line frequency, or if it is preferred to always assume a certain line frequency when resampling or calculating a fast rms measurement. USER_PERIOD[31:0] has the same scaling as the xPERIOD registers. Write USER_PERIOD[31:0] to 0x00A0_0000 for 50 Hz and 0x0085_5554 for 60 Hz.

Angle Measurement

The ADE9000 measures the time between zero-crossings on each phase. This measurement helps to determine if the system is balanced properly or to figure out if there was an installation error. The user can check if the phase angles correspond to the ones in the phasor diagrams in the Applying the ADE9000 to Different Metering Configurations section.

The times between one positive transition to the next are measured using a CLKIN/24 = 24.576/24 = 1024 kHz clock. Positive transition is defined as when the ADC samples go from a negative value to a positive value. The time between the zero-crossing on Phase A and Phase B is stored in the ANGL_VA_VB register. The resolution of the ANGLx_x2x register is (1/(1024 × 1000))/20 ms × 360° = 0.017578125° at 50 Hz.

The time between the zero-crossing on Phase B and C is stored in the ANGL_VB_VC register, and the time in between the zero-crossings on Phase A and C is stored in the ANGL_VA_VC register, as shown in Figure 31.

MEASUREMENTS

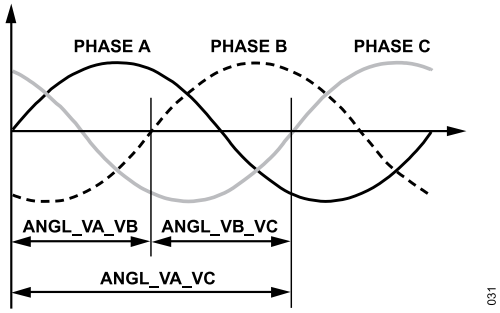

Figure 31. Voltage to Voltage Phase Angle

The angle in degrees can be calculated from the following equation with a 50 Hz line period:

Angle (degrees) = *ANGL_VA_VB* × 0.017578125/LSB (28)

For a 4-wire wye configuration, the expected ANGL_VA_VB and ANGL_VB_VC is 120°/0.017578125 = 3413 (decimal). Note that the expected ANGL_VA_VC from the Phase A voltage to Phase C voltage is 240°/0.017578125 = 13653 (decimal), which corresponds to a 120° angle between Phase C and Phase A.

The current to current zero-crossings are also measured. This measurement is done similarly to the voltage to voltage phase angle described previously, except the current channel zero-crossings are used as the reference. The time between the zero-crossing on Phase A and Phase B is stored in the ANGL_IA_IB register. The time between the zero-crossing on Phase B and Phase C is stored in the ANGL_IB_IC register, and the time in between the zero-crossings on Phase A and Phase C is stored in the ANGL_IA_IC register.

The voltage to current phase angles are measured as well. These angles can be used to determine the power factor at the fundamental. ANGL_VA_IA reflects the phase angle between the Phase A voltage and current, as shown in Figure 32. ANGL_VB_IB holds the Phase B voltage to current phase angle, and ANGL_VC_IC holds the Phase C voltage to current phase angle.

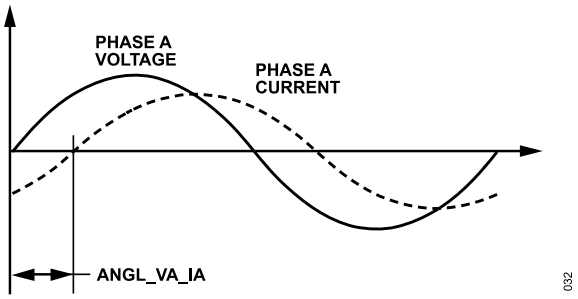

Figure 32. Voltage to Current Phase Angles

Note that if the magnitude of the voltage channel is below the user configured zero-crossing threshold, the zero-crossing output for that phase is not generated. In this event, the corresponding ANGLx_x2x measurements are not updated; the last value remains in the register. The current channel does not have these thresholds. With a low input signal level, spurious zero-crossing events may be generated on the current channel, which results in ANGLx_I2I and ANGLx_V2I readings that are not meaningful.

MEASUREMENTS

Phase Sequence Error Detection

4-Wire Wye and 4-Wire Delta

For 4-wire wye and 4-wire delta meters, the normal phase sequence is shown in Figure 33.

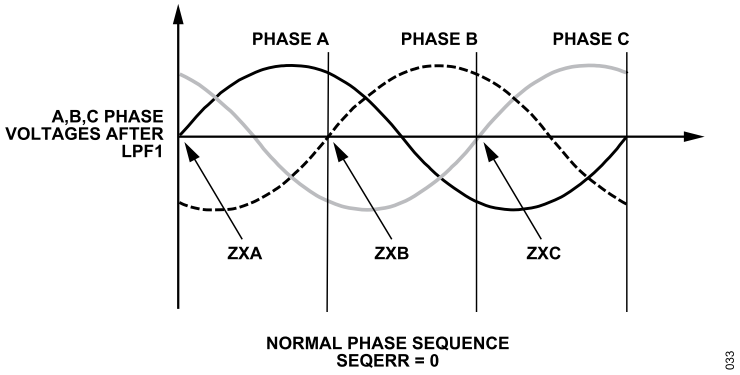

Figure 33. 4-Wire Wye and 4-Wire Delta Normal Phase Sequence

For a 4-wire wye or 4-wire delta system, VCONSEL[2:0] is 000, 010, or 011, as described in the Applying the ADE9000 to Different Metering Configurations section. In these 4-wire systems, the negative to positive transitions on ZXVA, ZXVB, and ZXVC are monitored to determine if there is a phase sequence error, as shown in Figure 35. To detect a phase sequence error, set how many sequences to observe in the SEQ_CYC register. It is recommended to set SEQ_CYC to 1. Figure 34 shows a phase sequence error for a 4-wire wye or 4-wire delta due to a wiring or installation error.

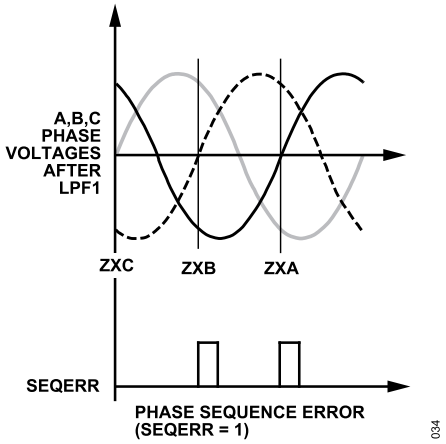

Figure 34. 4-Wire Wye and 4-Wire Delta Phase Sequence Error (Wiring Error)

Figure 35 shows that in an installation with the normal phase sequence, a phase sequence error is generated if a phase voltage drops below the ZXTHRSH.

MEASUREMENTS

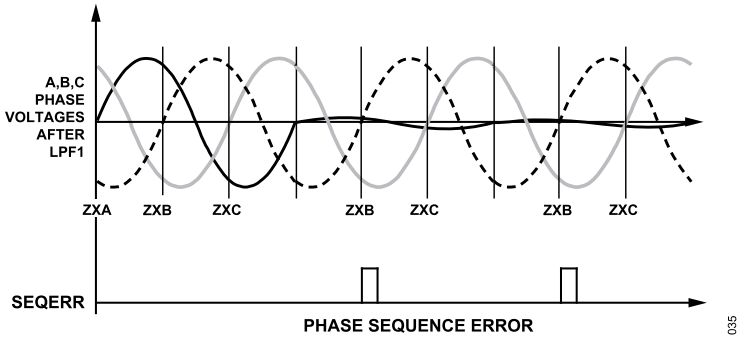

Figure 35. 4-Wire Wye, 4-Wire Delta Phase Sequence Error from a Phase Voltage Dropping Below ZXTHRSH with SEQ_CYC = 1

MEASUREMENTS

3-Wire Delta

For a 3-wire delta system, VCONSEL[2:0] is 001 or 100, as described in the Applying the ADE9000 to Different Metering Configurations section. In a 3-wire delta system, the ZXVC and ZXVA positive to negative and negative to positive transitions are monitored to detect a phase sequence error. Figure 36 shows the normal phase sequence for a 3-wire delta with VCONSEL[2:0] = 001.

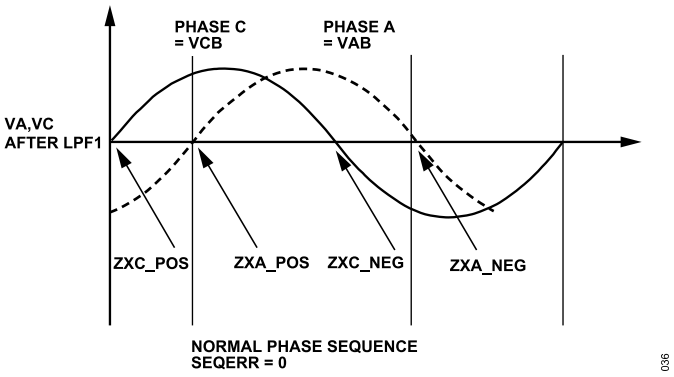

Figure 36. 3-Wire Delta Normal Phase Sequence

Write SEQ_CYC to indicate how many consecutive incorrect transitions must be observed before raising the SEQ_ERR interrupt. It is recommended to set SEQ_CYC to 1. Figure 37 shows an installation error for 3-wire delta that results in a detected phase sequence error.

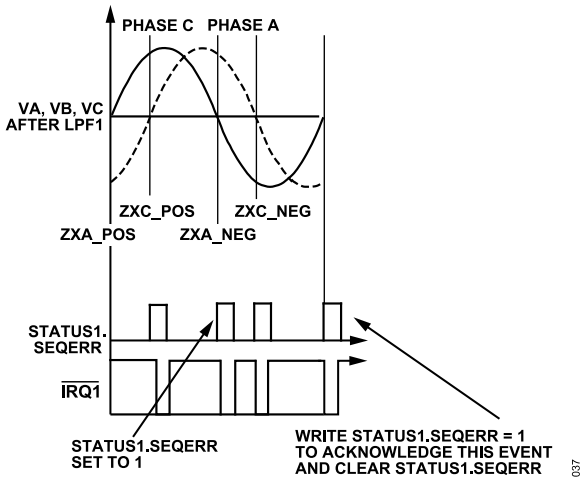

Figure 37. 3-wire Delta Phase Sequence Error (Wiring Error)

Figure 38 shows that in an installation with the normal phase sequence, a phase sequence error is generated if one of the phase voltage drops below the ZXTHRSH.

MEASUREMENTS

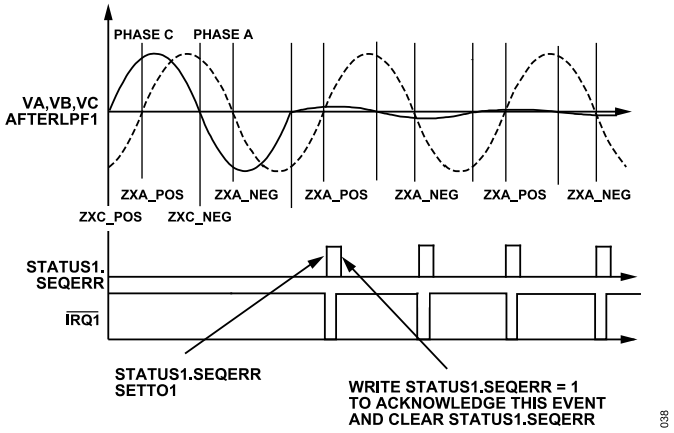

Figure 38. 3-Wire Delta Phase Sequence Error from a Phase Voltage Dropping Below ZXTHRSH with SEQ_CYC = 1

Fast RMS½ and 10/12 RMS Measurements

RMS½ is an rms measurement done over one line cycle, updated every half cycle.

This measurement is provided for voltage and current on all phases plus the neutral current. All the half cycle rms measurements are done over the same time interval and update at the same time, as indicated by the RMSONERDY bit in the STATUS0 register. The results are stored in the AIRMSONE, BIRMSONE, CIRMSONE, NIRMSONE, AVRMSONE, BVRMSONE, and CVRMSONE registers.

By default, the number of samples used in the calculation varies with measured line frequency. The LP_SEL bits in the ZX_LP_SEL register select which line period measurement is used to set the number of samples used in the RMS½ measurement.

Alternatively, the user can set the number of samples used in the calculation by setting the UPERIOD_SEL bit in CONFIG2, where the user configured USER_PERIOD register is used instead of the selected line period measurement. For more information about USER_PERIOD and the line period measurements, see the Line Period Calculation section.

The samples used for the RMS½ calculation can come from before the high-pass filter or after the integrator, as selected in the RMS_SRC_SEL bit in the CONFIG0 register.

Because the high-pass filter has a significant settling time associated with it, it is recommended to use the data from before the high-pass filter for the fastest response time.

An offset correction register is provided for even better performance with small input signal levels, xRMSONEOS.

The xRMSONE register reading with full-scale inputs is 52,702,092 (decimal).

The 10 cycle rms/12 cycle rms measurement is done over 10 cycles on a 50 Hz network, or 12 cycles on a 60 Hz network.

An offset correction register is provided for even better performance with small input signal levels, xRMS1012OS.

The xRMS1012 register reading with full scale inputs is 52,702,092 (decimal).

Table 17 shows the ½ cycle rms settling times for a 50 Hz signal. Table 18 shows the 10 cycle rms/12 cycle rms settling times for a 50 Hz signal.

Table 17. ½ RMS Settling Time

Configuration	½ RMS Settling Time, FS = 99% (sec)
Integrator On, HPF On, and LPF2 On	0.26
Integrator Off, HPF On, and LPF2 On	0.06

Table 18. 10 Cycle RMS/12 Cycle RMS Settling Time

Configuration	10/12 RMS Settling Time, FS = 99% (sec)
Integrator On, HPF On, and LPF2 On	0.6
Integrator Off, HPF On, and LPF2 On	0.2

MEASUREMENTS

Dip/Swell Indication

Dip indicates if the voltage went below a specified threshold for a user configured number of cycles. Conversely, swell indicates if the voltage went above a threshold for a specified number of cycles.

Set the DIP_LVL register to correspond to the RMS½ value to trigger the dip event, according to this equation:

$$DIP\_LVL = xVRMSONE \times 2^{-5} \quad (29)$$

Configure the number of cycles to observe the RMS½ value over in the DIP_CYC register.

The RMS½ voltages on Phase A, Phase B, and Phase C is compared to the DIP_LVL over the specified DIP_CYC. If the RMS½ voltage is low for the specified number of DIP_CYC, the dip event has occurred on that phase and the corresponding DIPA, DIPB, and DIPC bits are set in the STATUS1 register. The dip event can be configured to generate an interrupt on the $\overline{IRQ1}$ pin

The dip event can be configured to generate an event on the CF4/$\overline{EVENT}$/DREADY pin, if the corresponding bits are set in the EVENT_MASK register. This allows the user to precisely time the duration of a dip or swell, using the CF4/$\overline{EVENT}$/DREADY pin in combination with a timer on an external microcontroller.

The minimum RMS½ value measured during the dip is stored in the corresponding DIPA, DIPB, and DIPC registers.

Similarly, the swell indication has a SWELL_LVL register to set the swell threshold, according to this equation:

$$SWELL\_LVL = xVRMSONE \times 2^{-5} \quad (30)$$

There is also a SWELL_CYC register. The maximum RMS½ voltage value measured during the swell is stored in the corresponding SWELLA, SWELLB, and SWELLC registers. If the DIP_SWELL_IRQ_MODE bit is set to 0 in the CONFIG1 register, an interrupt is generated every DIP_CYC/ SWELL_CYC cycles. If DIP_SWELL_IRQ_MODE is set to 1, one interrupt is generated when dip/swell mode is entered and another interrupt is generated on exit. The mode is changed after DIP_CYC cycles. Note that if DIP_CYC/SWELL_CYC = 1, an extra interrupt is generated on exit of the dip/swell condition, and the dip/swell value, DIPx/SWELLx, is updated at that time, which exceeds the DIP_LVL/SWELL_LVL value.

Overcurrent Indication

Overcurrent indication monitors the RMS½ current measurements. If a RMS½ current is greater than the user configured OILVL, the overcurrent threshold, this is indicated in the OI bit in the STATUS1 register.

$$OILVL = xIRMSONE \times 2^{-5} \quad (31)$$

The OC_EN[3:0] bits in the CONFIG3 register select which phases to monitor for overcurrent events.

The OIPHASE[3:0] bits in the OISTATUS register indicate which current channels had RMS½ measurements greater than the threshold.

If a phase is enabled, with the corresponding OC_EN bit set and RMS½ current greater than the threshold, the OI status is set and the RMS½ value is stored in the corresponding OIx register. If a phase is disabled, or an overcurrent event does not occur on that phase, the OIx register keeps the last value.

Peak Detection

The ADE9000 records the peak value measured on the current and voltage channels, from the xI_PCF and xV_PCF waveforms. The PEAKSEL[2:0] bits in the CONFIG3 register allow the user to select which phases to monitor. Set PEAKSEL[2] to monitor Phase C, PEAKSEL[1] for Phase B, and PEAKSEL[0] for Phase A. Set PEAKSEL[2:0] = 111 (binary) to monitor all three phases.

The IPEAK register stores the peak current value in IPEAKVAL[23:0] and indicates which phase(s) currents reached the value in the IPPHASE[2:0] bits. IPEAKVAL is equal to xI_PCF/2^5.

IPPHASE[2] indicates that Phase C had the peak value, IPPHASE[1] indicates Phase B, and IPPHASE[0] indicates Phase A.

Similarly, VPEAK stores the peak voltage value in VPEAKVAL[23:0]. VPEAKVAL is equal to xV_PCF/2^5.

VPPHASE[2] indicates if Phase C had the peak voltage value, VPPHASE[1] indicates Phase B, and VPPHASE[0] indicates Phase A.

When the user reads the IPEAK register, its value is reset. The same is true for reading VPEAK.

MEASUREMENTS

Power Factor

The total active power and total apparent power are accumulated over 1.024 sec. Then, the power factor is calculated on each phase according to this equation:

$$APF = \frac{AWATT \ \ accumulated \ \ over \ \ 1.024 \ \ \text{sec}}{AVA \ \ accumulated \ \ over \ \ 1.024 \ \ \text{sec}} \quad (32)$$

The sign of the APF calculation follows the sign of AWATT.

To figure out what quadrant the energy is in, look at the sign of the total or fundamental reactive energy in that phase along with the sign of the xPF or xWATT value, as indicated in the data sheet. Quadrant I and Quadrant III have capacitive power factors, and Quadrant II and Quadrant IV have inductive power factors. Note that for most applications, the watts are received (imported) from the grid, and therefore the watt and VAR stay within Quadrant I and Quadrant IV.

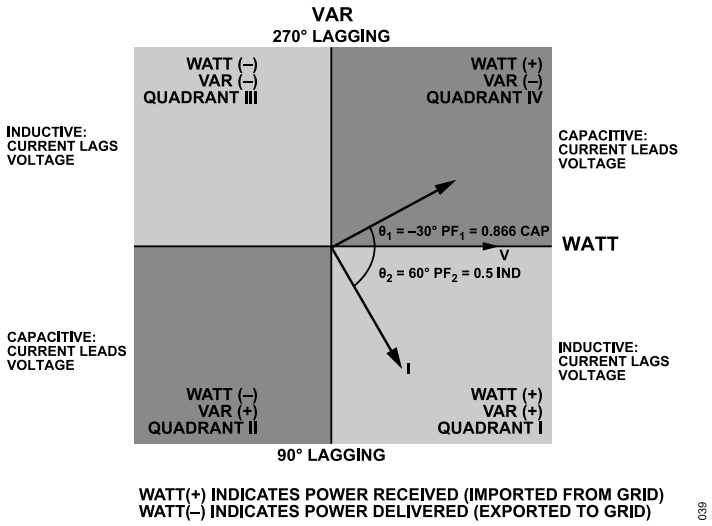

Figure 39. Watt and VAR Sign for Capacitive and Inductive Loads

The power factor results is stored in 5.27 format. The highest power factor value is 0x07FF_FFFF, which corresponds to a power factor of 1. A power factor of −1 is stored as 0xF800_0000. To determine the power factor from the xPF register value, use this equation:

$$\textit{Power Factor} = APF \times 2^{-27} \quad (33)$$

Total Harmonic Distortion

Total harmonic distortion (THD) is calculated once per second using total and fundamental rms values, as shown in this equation:

$$AITHD = \sqrt{\frac{AIRMS^2 - AIFRMS^2}{AIFRMS^2}} \quad (34)$$

The THD calculation is stored in signed 5.27 format. The highest THD value is 0x2000_0000, which corresponds to a THD of 400%. To obtain the THD value as a percentage, use this equation:

$$\%THD \text{ on Current Channel } A = AITHD \times 2^{-27} \times 100\% \quad (35)$$

A THD calculation is available on the IA, IB, IC, VA, VB, and VC channels in the AITHD, BITHD, CITHD, AVTHD, BVTHD, and CVTHD registers, respectively. Note that a THD measurement is not available on the IN channel.

MEASUREMENTS

TEMPERATURE

The ADE9000 includes a temperature measurement unit that uses a temperature sensor in conjunction with a 12-bit successive approximation register (SAR) ADC.

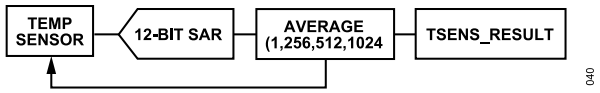

Figure 40. Temperature Measurement Block Diagram

Enable the temperature sensor by setting the TEMP_EN bit in the TEMP_CFG register. TEMP_TIME[1:0] allows 1, 256, 512, or 1024 temperature readings to be averaged, producing a result after 1.25 ms to 1.3 sec. A temperature acquisition cycle is started by setting the TEMP_START bit in the TEMP_CFG register. The result is available in the TEMP_RSLT register. The TEMP_START bit is self clearing. Set the TEMP_START bit to obtain a new reading. Set the TEMP_RDY bit in the MASK0 register to receive an interrupt when a new temperature measurement is available.

The temperature reading offset and gain is measured during production test and stored in the TEMP_TRIM register. To convert the temperature readings in TEMP_RSLT into a temperature in degrees Celsius, use this equation:

$$Temperature\ (°C) = TEMP\_RSLT \times (-TEMP\_GAIN/65536) + (TEMP\_OFFSET/32) \quad (36)$$

ACCESSING ON-CHIP DATA

SPI PROTOCOL OVERVIEW

The ADE9000 has a SPI-compatible interface, consisting of four pins: SCLK, MOSI, MISO, and $\overline{SS}$. The ADE9000 is always a SPI subordinate; it never initiates SPI communication. The SPI interface is compatible with 16-bit and 32-bit read/write operations. See the Register Information section for information about the length of each register.

Figure 41 shows the connection between the ADE9000 SPI and a main device that contains a SPI interface.

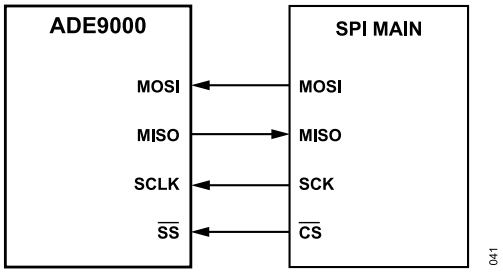

Figure 41. Connecting the ADE9000 Subordinate SPI Port to a Main SPI Device

The $\overline{SS}$ pin is the chip select input. It is used to start the SPI communication with the ADE9000.

There are three parts to the ADE9000 SPI protocol: first a 16-bit command is sent, which indicates whether a read or write operation is to be performed and which register to access. This command is followed by the 16-bit or 32-bit data to be written, in the case of a SPI write, or the data read from the register, in the case of a SPI read operation. Finally, in the case of a SPI read operation, a cyclic redundancy check (CRC) of the register data follows, unless the address is in a region that supports burst reading, in which case the data from the next register follows (see the SPI Burst Read section for more information).

The $\overline{SS}$ input must stay low for the whole SPI transaction. Bringing $\overline{SS}$ high during a data transfer operation aborts the transfer. A new transfer can be initiated by returning the $\overline{SS}$ logic input low. It is not recommended to tie $\overline{SS}$ to ground because the high to low transition on $\overline{SS}$ starts the ADE9000 SPI transaction.

Data shifts into the device at the MOSI logic input on the falling edge of SCLK, and the device samples the input data on the rising edge of SCLK. Data shifts out of the ADE9000 at the MISO logic output on the falling edge of SCLK and must be sampled by the main device on the rising edge of SCLK. The most significant bit of the word is shifted in and out first.

MISO has an internal weak pull-up of 100 kΩ, making the default state of the MISO pin high. It is possible to share the SPI bus with multiple devices, including multiple ADE9000 devices, if desired.

The ADE9000 is compatible with the following microcontroller SPI port clock polarity and phase settings: CPOL = 0 and CPHA = 0 (typically Mode 0), or CPOL = 1 and CPHA = 1 (typically Mode 3).

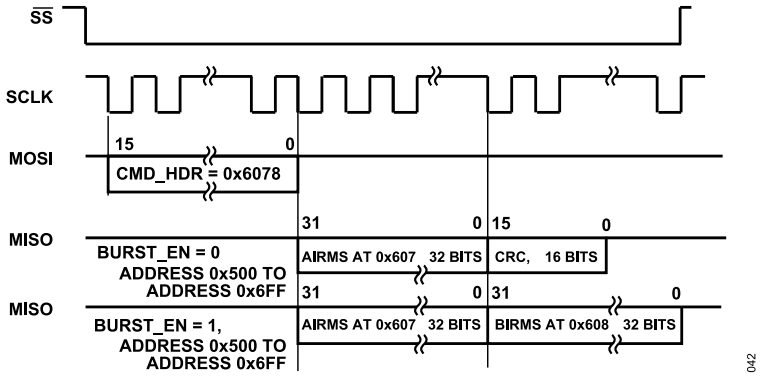

Figure 42. SPI Read Protocol Example—CRC or Next Data can Follow

The default state of the MOSI pin depends on the main SPI device. Here, it is assumed to be high (Logic 1).

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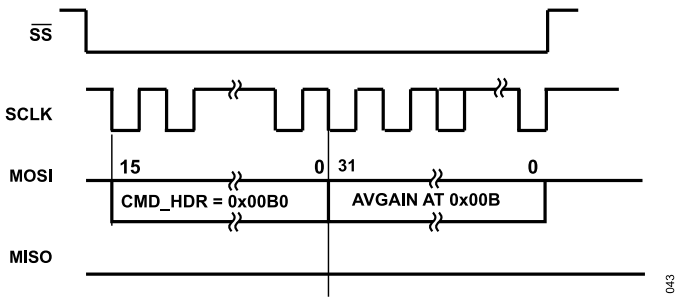

Figure 43. SPI Write Protocol Example

The maximum serial clock frequency supported by this interface is 20 MHz.

The SPI read/write operation starts with a 16-bit command (CMD_HDR), which contains the following information:

- CMD_HDR[15:4], the 12 most significant bits of the command header, contains the address of the register (ADDR[11:0]) to be read or written.
- CMD_HDR[3] is the bit that specifies if the current operation is read/write. Set this bit to 1 for read and 0 for write.
- CMD_HDR[2:0] are bits that are required for internal chip timing and can be 1s or 0s. Note that these bits are read back as 000 in the LAST_CMD register.

Figure 44 shows the information contained in the command header.

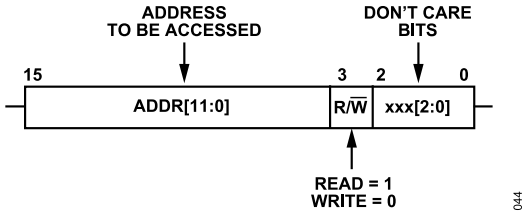

Figure 44. Command Header, CMD_HDR [15:0]

SPI WRITE

A write operation using the SPI interface of the ADE9000 is initiated when the $\overline{SS}$ pin goes low and the ADE9000 receives a 16-bit command header (CMD_HDR) with CMD_HDR[3] equal to 0.

The 16-bit or 32-bit data to be written follows the command header, with the most significant bit first.

After the last bit of data has been clocked out, the main must bring the $\overline{SS}$ line high to release the SPI bus. It is recommended to have the SCLK line idle high.

SPI READ

A read operation using the SPI interface of the ADE9000 is initiated when the $\overline{SS}$ pin goes low and the ADE9000 receives a 16-bit command header (CMD_HDR) with CMD_HDR[3] equal to 1.

The 16-bit or 32-bit data from the register follows the command header, with the most significant bit first.

The CRC of the register data is appended if

- BURST_EN = 0 and the address is within the range of 0x000 to 0x6FF.
- BURST_EN = 0 and the address is in the waveform buffer, 0x800 to 0xFFF, and BURST_CHAN is equal to 1111 (binary).

The ADE9000 provides a SPI burst read functionality: instead of sending the CRC, the following data is from the next address if the following conditions apply (see the SPI Burst Read section for more information):

- BURST_EN = 1, and the address is within the range of 0x500 to 0x63C or 0x680 to 0x6BC.
- The address is within the range of 0x800 to 0xFFF, and BURST_CHAN is not equal to 1111 (binary).

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If none of these cases apply, and extra clocks are sent, the original read data is resent.

Table 19 summarizes which data is sent after the data from the register addressed in the CMD_HDR; it varies based on the address being accessed and the BURST_EN selection.

Table 19. Data Clocked Out After Addressed Data, in SPI Read Operation

Address	BURST_EN = 0	BURST_EN = 1
0x000 to 0x4FF	CRC	Same data is resent
0x500 to 0x6FF	CRC	Next address
0x800 to 0xFFF (Waveform Buffer)	If BURST_CHAN = 1111, CRC; otherwise, next address	If BURST_CHAN = 1111, same data is resent; otherwise, next address

The $\overline{SS}$ line can be brought high before clocking out the CRC if this information is not needed in the application.

After the last bit of data, or CRC, has been clocked out, the main must bring the $\overline{SS}$ line high to release the SPI bus. Then the ADE9000 stops driving MISO and enables a 100 kΩ weak pull-up. It is recommended to have the SCLK line idle high.

An example of what happens when reading the AVGAIN register, Address 0x00B, when BURST_EN = 0 and 1 is shown in Figure 45.

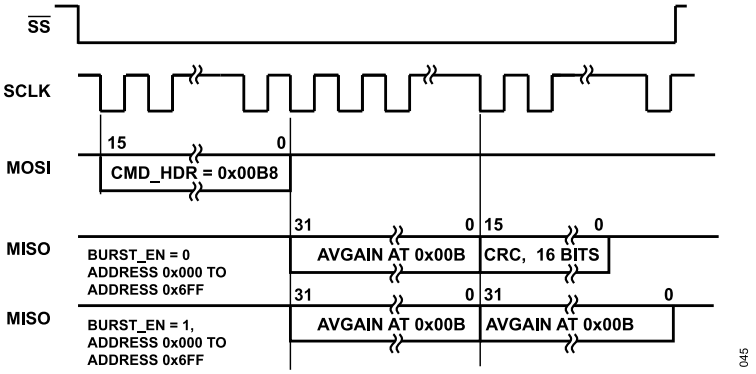

Figure 45. SPI Read Protocol Example where the Following Data is the CRC or the Initial Data is Repeated

SPI BURST READ

SPI burst read allows multiple registers to be read after sending one CMD_HDR. After the register data has been clocked out, the ADE9000 auto-increments the address and starts clocking out the data from the next register address.

SPI burst read access is available on registers with addresses ranging from 0x500 0x6FF and in the waveform buffer, with Address 0x800 to Address 0xFFF. SPI burst read is not available on other register addresses. A SPI burst read operation occurs for the options in Table 19 where next address is shown.

To enable burst read functionality on the registers from 0x500 to 0x6FF, set the BURST_EN bit in the CONFIG1 register to 1.

The waveform buffer burst read functionality is enabled by default and is managed by the BURST_CHAN[3:0] bits of the WFB_CFG register. If these bits are set to 1111 (binary), the burst read functionality of the waveform buffer is disabled. For further details on burst read operation of waveform buffer contents, see the Burst Read Waveform Buffer Samples From SPI section.

A burst read operation using the SPI interface of the ADE9000 is initiated when the $\overline{SS}$ pin goes low and the ADE9000 receives a 16-bit command header (CMD_HDR) with CMD_HDR[3] equal to 1, which meets the criteria in Table 19 where next address is shown.

Following the command header, ADE9000 sends the register data for the register addressed in the command. After the last bit of the first register value is received, the ADE9000 auto-increments the address and starts clocking out the data from the next register address. If the starting address is in the range of Address 0x500 to Address 0x516 and the SPI is clocked beyond Address 0x516, the address is auto-incremented until it reaches Address 0x5FF and then wraps back to the initial address. If the initial address is in the Address 0x600 to Address 0x63C or Address 0x680 to Address 0x6BC range and the SPI is clocked beyond Address 0x63C or Address 0x6BC, the address wraps back to the initial address. This process continues until the main sets the $\overline{SS}$ line high. Then, the ADE9000 stops driving MISO and enables a 100 kΩ weak pull-up. It is recommended to have the SCLK line idle high. An example of a SPI burst read operation is shown in Figure 42, when BURST_EN = 1. For other examples, see the Burst Read Waveform Buffer Samples From SPI section.

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SPI PROTOCOL CRC

The ADE9000 SPI port calculates a CRC of the data sent out on its MOSI pin so that the integrity of the data received by the main can be checked. The CRC of the data sent out on the MOSI pin during the last register read is offered in a 16-bit register, CRC_SPI, and can be appended to the SPI read data as part of the SPI transaction.

The CRC_SPI register value is appended to the 16-/32-bit data read from the register addressed in the CMD_HDR for the cases in Table 19 where CRC is written (see the SPI Read section for more information).

The CRC result can always be read from the CRC_SPI register directly.

There is no CRC checking as part of the SPI write register protocol. To ensure the data integrity of the SPI write operation, read the register back to verify that the value has been written to the ADE9000 correctly.

ADE9000 CRC Algorithm

The CRC algorithm implemented within the ADE9000 is based on the CRC-16-CCITT algorithm. The data output on MISO is introduced into a linear feedback shift register (LFSR)-based generator one byte at a time, most significant byte first without bit reversal, as shown in Figure 46 and Figure 47. The 16-bit result is written in the CRC_SPI register.

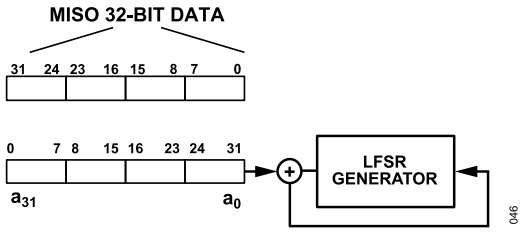

Figure 46. CRC Calculation of 32-Bit SPI Data

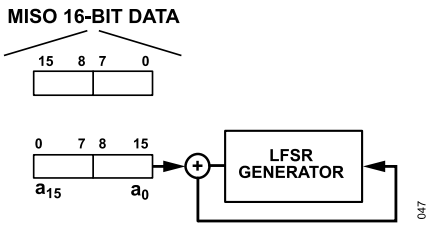

Figure 47. CRC Calculation of 16-Bit SPI Data

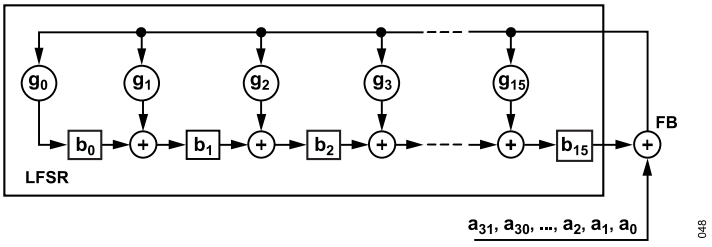

Figure 48. LFSR Generator Used for CRC_SPI Calculation

Figure 48 shows how the LFSR works. The MISO 32-bit data forms the [a_{31}, a_{30},..., a_0] bits used by the LFSR. Bit a_0 is Bit 24 of the first MISO 32-bit data to enter the LFSR, and the last data to enter the LFSR, Bit a_{31}, corresponds to Bit 7 transmitted on MISO. The formulas that govern the LFSR are as follows.

$b_i(0)$ = 1, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant bit.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm as follows:

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$$G(x) = x^{16} + x^{12} + x^5 + 1 \quad (37)$$

$$g_0 = g_5 = g_{12} = 1 \quad (38)$$

All other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (39)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (40)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots, 15 \quad (41)$$

Equation 39, Equation 40, and Equation 41 must be repeated for j = 1, 2, …, 32. The value written into the CRC_SPI register contains Bit $b_i(32)$, i = 0, 1, …, 15.

A similar process is followed for 16-bit data; see Figure 47 for information about how the bits are ordered into the LFSR.

ADDITIONAL COMMUNICATION VERIFICATION REGISTERS

The ADE9000 includes three registers that allow SPI operations to be verified. The LAST_CMD (Address 0x4A3), LAST_DATA_16 (Address 0x4AC), and LAST_DATA_32 (Address 0x423) registers record the received CMD_HDR and last read/transmitted data. The LAST_DATA_16 register contains the last data read or written during the last 16-bit transaction, and the LAST_DATA_32 register holds the data read or written during the last 32-bit transaction.

The LAST_CMD register is updated after the CMD_HDR is received. If a command to read the LAST_CMD, LAST_DATA_16, or LAST_DATA_32 registers is received, these three registers are not updated. Note that LAST_CMD[2:0] always reads back as 000.

During a SPI read operation, the LAST_DATA_16 and LAST_DATA_32 registers are updated within two main clocks after the CMD_HDR has been received. If a command to read the LAST_CMD, LAST_DATA_16, or LAST_DATA_32 registers is received, these three registers are not updated.

Note that the LAST_DATA_16 and LAST_DATA_32 registers are not updated after a SPI burst read operation; these are the cases in Table 19 where next address is written.

On a write operation, LAST_DATA_16 and LAST_DATA_32 are not updated until all 16 bits or 32 bits of the write data have been received. Note that on a write register operation, the addressed register is not written until all 16 bits or 32 bits are received, depending on the length of the register.

Note that when the LAST_CMD, LAST_DATA_16, and LAST_ DATA_32 registers are read, their values remain unchanged.

CRC OF CONFIGURATION REGISTERS

The configuration register CRC feature in the ADE9000 monitors many register values. It also optionally includes 15 registers that are individually selectable in the CRC_OPTEN register.

This feature runs as a background task; it takes 10.8 ms to calculate the configuration register CRC. The result is stored in the CRC_RSLT register. If any of the monitored registers change value, the CRC_RSLT changes as well, and the CRC_CHG bit in the STATUS 1 register is set; this can also be configured to generate an interrupt on $\overline{\text{IRQ1}}$.

After configuring the ADE9000 and writing the required registers to calibrate the measurements (such as xIGAIN or xVGAIN, for example), the configuration register CRC calculation can be started by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register. When the calculation is complete, the CRC_DONE bit is set in the STATUS1 register.

The method used for calculating the configuration register CRC is also based on the CRC-16-CCITT algorithm. The most significant byte of each register is introduced into the LFSR first, without bit reversal.

The order in which the registers are calculated is given in Table 20, with the lowest register introduced first. Note that 32-byte registers have four bytes introduced into the LFSR, and 16-byte registers have two bytes introduced into the LFSR.

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Table 20. Order of Registers Included in Configuration Register CRC

Register Addresses	Register Length (Bits)
0x01 to 0x18	32
0x21 to 0x38	32
0x41 to 0x58	32
0x60 to 0x73	32
0x409	32
0x40F	32
0x420 to 0x422	32
0x424	32
0x470 to 0x475	32
0x480 to 0x481	16
0x490 to 0x497	16
0x499	16
0x4AF to 0x4B2	16
0x425	32
0x4B8 to 0x4B9	16
0x47D	32
0x478 to 0x479	32
0x4EF	16
0x4BA	16
0x47E	32
0x00	32
0x20	32
0x40	32
0x4B6	16
0x4BF	16
0x4B5	16

WAVEFORM BUFFER

The ADE9000 has a waveform buffer comprised of 2048, 32-bit memory locations with addresses from 0x800 to 0xFFF. This memory can be filled with samples from the sinc4 or sinc4 + IIR LPF, current and voltage waveform samples processed by the digital signal processor or resampled waveforms.

Resampled waveforms make it easy to perform harmonic analysis in an external processor, which can use the 16-bit, 128 points per line cycle samples directly in a FFT, without having to perform any windowing functions or changing the FFT coefficients function of line period.

The data in the waveform buffer can come from four locations in the signal chain:

- Sinc4 outputs, xI_SINC_DAT, xV_SINC_DAT provided at 32 ksps update rate
- Sinc4 + IIR LPF output, xI_LPF_DAT, xV_LPF_DAT provided at 8 ksps update rate
- Current and voltage channel waveforms processed by the DSP (xI_PCF, xV_PCF) provided at 8 ksps update rate
- Resampled waveforms with 128 points per line cycle processed by the DSP; data rate varies with line period

Filling and accessing of the waveform buffer depends on which type of data is being filled in the buffer. The waveforms with a fixed data rate, 32 ksps or 8 ksps, are referred to as fixed data rate waveforms. Refer to the corresponding section to understand what modes and access are available for resampled waveforms vs. fixed data rate waveforms.

The waveform buffer samples can be accessed using the SPI burst read functionality so that multiple samples can be read using only one SPI command header (see the Burst Read Waveform Buffer Samples From SPI section).

FIXED DATA RATE WAVEFORMS

Fixed data rate waveforms from the signal chain can be stored into the waveform buffer from the places shown in Table 21.

Table 21. Fixed Data Rate Waveform Sources

Source	WFB_CFG.WF_SRC	Data Rate	32-Bit Data Format
Sinc4 Outputs	0	32 ksps	24 bits, shifted left by 4 bits and sign extended to 32 bits
Sinc4 + IIR LPF Output	2	8 ksps	24 bits, shifted left by 4 bits and sign extended to 32 bits
Waveforms Processed by the DSP (xI_PCF, xV_PCF)	3	8 ksps	32 bits, 2's compliment, integer

The 24-bit sinc4 and sinc4 + IIR LPF data is stored as 32-bit in the waveform buffer by shifting by left by 4 bits and sign extending, as shown in Table 22.

Table 22. 24-Bit Sinc4 and Sinc4 + IIR LPF Data

Bits[31:28]	Bits[27:4]	Bits[3:0]
SE	ADC_DATA[23:0]	0000

Table 21 indicates the WFB_SRC selection for each fixed data rate waveform source. Each fixed data rate sample is 32-bits; however, the data format varies between the three sources, as shown in Table 21. When the waveform buffer is enabled, the data from all seven channels is stored into the buffer. One sample set consists of one sample per channel, seven samples total, which are taken at the same point in time.

Figure 49 shows how the fixed data rate samples are stored into the buffer. Every sample set is separated in the memory from the adjacent one by the use of spare cells, which do not contain any sample data, as shown in Figure 49. In this way, every eighth 32-bit memory location in the buffer is reserved as a spare cell. If the seventh channel is disabled, with the WF_IN_EN bit in the WFB_CFG register equal to 0, the IN sample locations are treated as spare cells as well.

WAVEFORM BUFFER

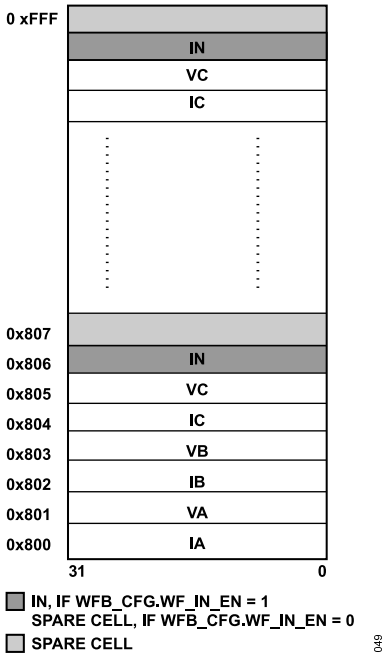

Figure 49. Fixed Data Rate Waveform Sample Storage

There are 256 (2048/8) sample sets that can be stored in the buffer. In the ADE9000, the sinc4 outputs at 32 ksps, so the buffer can contain (256/32000) = 8 ms of data from the sinc4. The sinc4 + IIR LPF samples and DSP processed xI_PCF and xV_PCF waveform samples are filled at 8 kHz, and the buffer can contain 32 ms (256/8000) of this data.

When used with fixed data rate samples, the waveform buffer is divided into 16 pages, Page 0 to Page 15. Each page contains 128, 32-bit memory locations. Figure 50 illustrates this arrangement.

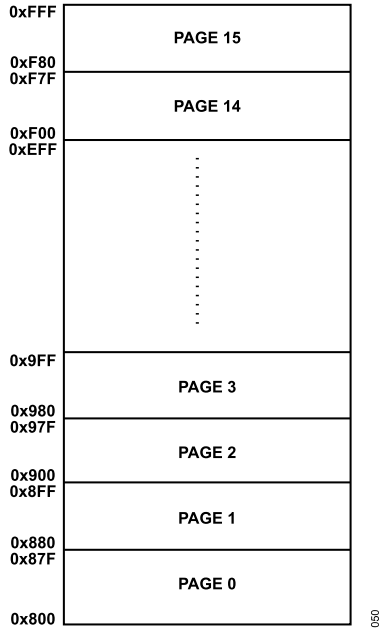

Figure 50. Waveform Buffer Page Arrangement—for Fixed Data Rate Samples Only

WAVEFORM BUFFER

Waveform Buffer Filling Indication—Fixed Data Rate Samples

The WFB_PG_IRQEN register allows the user to monitor if specific pages have been filled, with one bit managing a page of the buffer: Bit 0 manages Page 0, Bit 1 manages Page 1, and so on. For example, if Bit 0 and Bit 3 of WFB_PQ_IRQEN are set, the user receives an indication when the last address of Page 0, 0x87F, has been written (meaning that Page 0 is full), and when the last address of Page 3, 0x9FF, has been written (meaning that Page 3 is full). The PAGE_FULL bit of the STATUS0 register is set to 1 when a page enabled in the WFB_PG_IRQEN register has been filled. The user can enable an interrupt to occur on $\overline{\text{IRQ0}}$ when the PAGE_FULL bit is set by setting the PAGE_FULL bit in the STATUS0 register.

The WFB_LAST_PAGE bits in the WFB_TRG_STAT register indicate which page was filled last when filling with fixed data rate samples.

FIXED DATA RATE WAVEFORMS FILLING AND TRIGGER-BASED MODES

The waveform buffer offers different filling modes to be used with fixed data rate samples:

- Stop when buffer is full
- Continuous filling

The ADE9000 allows a selection of events to trigger waveform buffer captures, and there is an option to store the current waveform buffer address during an event, to allow the user to synchronize the event with the waveform samples.

The following are the waveform buffer actions that can be associated with an event when the buffer is filling continuously:

- Stop filling on trigger
- Center capture around trigger
- Save event address and keep filling

Stop When Buffer Is Full Mode

Stop when buffer is full mode is enabled when WF_CAP_SEL = 1 and the WF_MODE[1:0] bits are equal to 00 in the WFB_CFG register. Set the WF_CAP_EN bit in the WFB_CFG register to start filling the buffer from Address 0x800.

When the Address Location 0xFFF in Page 15 is written, the filling operation stops. To receive an indication when the buffer is full, which corresponds to Page 15 being full, set Bit 15 of the WFB_PG_IRQEN register prior to starting the capture. Then, the PAGE_FULL bit in STATUS0 is set when the buffer is full. This PAGE_FULL status change can be enabled to generate an interrupt on $\overline{\text{IRQ0}}$ as well.

To perform the next filling operation, disable the waveform buffer by clearing the WF_CAP_EN bit of the WFB_CFG register to 0, and enable it again by setting the same bit to 1.

Continuous Fill Mode

Continuous fill mode is enabled when WF_CAP_SEL = 1 and WF_MODE[1:0] in the WFB_CONFIG register is equal to 1, 2, or 3. Write the WF_CAP_EN bit in the WFB_CONFIG register to start filling the buffer from Address 0x800.

In this mode, the waveform buffer is filled continuously. When the entire buffer is filled up to Address Location 0xFFF, the filling continues from Address Location 0x800 in a circular fashion.

In this mode, it is important to monitor the filling status of the buffer using the WFB_PG_IRQEN register in conjunction with the PAGE_FULL bit in the STATUS0 register and the WFB_LAST_PAGE bits in the WFB_TRG_STAT register, as described in the Waveform Buffer Filling Indication—Fixed Data Rate Samples section. If the data is not read out of the buffer soon enough, it is overwritten.

To stop the waveform buffer capture, read the WFB_LAST_ PAGE register, so that the page that contains the most recent valid data is known, and then clear the WF_CAP_EN bit in the WFB_CONFIG register to 0.

To restart the filling operation, disable the waveform buffer by clearing the WF_CAP_EN bit of the WFB_CONFIG register if not already cleared, and then enable it again by setting this bit to 1.

There are two variations on the continuous fill mode that stop filling the waveform buffer based on a trigger event: stop filling on trigger mode, and center capture around trigger mode. These modes are selected when WF_MODE[1:0] = 1 and 2, respectively (see the Stop Filling on Trigger section and the Center Capture Around Trigger section for more information).

WAVEFORM BUFFER

Stop Filling on Trigger

When WF_CAP_SEL = 1 and WF_MODE[1:0] is equal to 1, stop filling on trigger mode is selected. Use this mode to analyze the ADC samples leading up to an event of interest.

In this mode, the waveform buffer is filled continuously. When the entire buffer is filled up to Address Location 0xFFF, the filling continues from Address Location 0x800 in a circular fashion. The events listed in Table 23 are classified as trigger events. Upon receiving an enabled trigger event, the ADE9000 stops filling the waveform buffer.

The events listed in Table 23 can be enabled as waveform buffer triggers, in the WFB_TRG_CFG register.

Table 23. Waveform Buffer Trigger Events in the WFB_TRG_CFG Register

Bit No.	Bit Name	Description
10	TRIG_FORCE	Set this bit to trigger an event to stop the waveform buffer filling
9	ZXCOMB	ZXCOMB event
8	ZXVC	ZX event in Phase C voltage
7	ZXVB	ZX event in Phase B voltage
6	ZXVA	ZX event in Phase A voltage
5	ZXIC	ZX event in Phase C current
4	ZXIB	ZX event in Phase B current
3	ZXIA	ZX event in Phase A current
2	OI	Overcurrent event
1	SWELL	Swell event
0	DIP	Dip event

The trigger events in WFB_TRG_CFG[10:0] correspond to interrupt events within the ADE9000, with the exception of the TRIG_FORCE bit. The user can set the TRIG_FORCE bit, WFB_TRG_CFG[10], to stop the filling the waveform buffer in this mode.

When one of the events configured in WFB_TRG_CFG occurs, the filling of the buffer stops and the WFB_TRIG bit is set in the STATUS0 register, which can be configured to generate an interrupt on the $\overline{\text{IRQ0}}$ pin. The address of the IN waveform of the last sample set is stored in the WFB_TRIG_ADDR bits of the WFB_TRG_STAT register. Because the filling stops when the event occurs, any sample sets with addresses greater than the WFB_TRIG_ADDR value contain old data.

To ensure that a buffer's worth of samples has been captured before the event, follow this sequence:

1. Select stop capture on trigger mode: WF_CAP_SEL = 1, WF_MODE = 1.
2. Disable all trigger events by writing WFB_TRG_CFG = 0.
3. Make sure that the buffer has been filled one time by enabling an interrupt to occur on $\overline{\text{IRQ0}}$ when the last page is filled, by setting only Bit 15 in the WFB_PQ_IRQEN register and enabling the PAGE_FULL bit in the STATUS0 register. Alternatively, the LAST_PAGE register can be read instead of using the interrupt.
4. Start the capture by writing WF_CAP_EN = 1.
5. Wait for the buffer to be filled (indicated by when the PAGE_FULL interrupt occurs or LAST_PAGE = 15).
6. When the buffer is filled, enable the desired waveform buffer events in the WFB_TRG_CFG register and set the WFB_TRIG_IRQ bit in the STATUS0 to generate an interrupt when the event has occurred and the waveform buffer has stopped filling.
7. When WFB_TRIG_IRQ occurs, read the WFB_TRIG_ADDR register to obtain the address of the trigger event, which is within a sample or two of when the event occurred and is the last filled address.

Waveform buffer values are retained when the waveform buffer is disabled by clearing the WF_CAP_EN bit in the WFB_CFG register; however, LAST_PAGE and WFB_TRIG_ADDR are reset when that bit is cleared. Read the LAST_PAGE and WFB_TRIG_ADDR registers prior to writing WF_CAP_EN = 0.

The trigger events given in Table 23 must be enabled or disabled prior to enabling the waveform buffer by writing to the WFB_TRG_CFG register.

Then, to perform the next filling operation in the stop filling on trigger mode, disable the waveform buffer by clearing the WF_CAP_EN bit of the WFB_CFG register, and then enable it again by setting the same bit to 1. Note that if the TRIG_FORCE bit was set to force a trigger, it must be cleared in the WFB_TRG_CFG register prior to starting the next capture (before writing WF_CAP_EN = 1).

WAVEFORM BUFFER

Center Capture Around Trigger

The center capture around trigger mode is enabled when WF_CAP_SEL = 1 and WF_MODE[1:0] = 2, and is similar to the stop on trigger mode, except that the waveform buffer does not stop filling after the trigger event. Even after the occurrence of the trigger event, the filling of the buffer continues to take place for the next 1024, 32-bit memory locations before stopping. It is recommended to use this mode to analyze samples before and after an event. See the Stop Filling on Trigger section for more information about trigger events.

Note that in center trigger mode, the WFB_TRIG bit in the STATUS0 register is set when the enabled trigger event occurs, and the WFB_TRG_IRQ bit in the STATUS0 register is set when the 1024 additional memory locations have been filled and the waveform buffer filling stops. Both of these status bits can be configured to generate an interrupt on the $\overline{\text{IRQ0}}$ pin. Calculate the last filled address using WFB_TRIG_ADDR:

```
If (WFB_TRIG_ADDR+1024>0xFFF,
Last Filled Address = WFB_TRIG_ADDR-1024;
Else
Last Filled Address = WFB_TRIG_ADDR+1024;
```

To ensure that a buffer's worth of samples has been captured before the event, follow this sequence:

1. Select center capture on trigger mode: WF_CAP_SEL = 1, WF_MODE = 2.
2. Disable all trigger events by writing WFB_TRG_CFG = 0.
3. Make sure that at least half of the buffer has been filled by enabling an interrupt to occur on $\overline{\text{IRQ0}}$ when Page 7 is filled, by setting only Bit 7 in the WFB_PQ_IRQEN register and enabling the PAGE_FULL bit in the STATUS0 register. Alternatively, the LAST_PAGE register can be read instead of using the interrupt.
4. Start the capture by writing WF_CAP_EN = 1.
5. Wait for the buffer to be filled (indicated by when the PAGE_FULL interrupt occurs or LAST_PAGE = 15).
6. When the buffer is filled, enable the desired waveform buffer events in the WFB_TRG_CFG register and set the WFB_TRIG_IRQ bit in the STATUS0 register to generate an interrupt when the event has occurred and the waveform buffer has stopped filling.
7. When WFB_TRIG_IRQ occurs, read the WFB_TRIG_ADDR register to obtain the address of the trigger event, which is within a sample or two of when the event occurred. The last filled address is 1024 samples later.

Save Event Address and Keep Filling

To record the waveform buffer address when a trigger event occurs, while still filling the buffer, select WF_MODE = 3 for continuous filling. When a trigger event that is enabled in the WFB_TRG_CFG register occurs, the WFB_TRIG bit in the STATUS0 register is set, which can be configured to generate an interrupt on the $\overline{\text{IRQ0}}$ pin. Read the WFB_TRIG_ADDR bits in the WFB_TRIG_STAT register to obtain the waveform buffer address for the event. Only the first enabled trigger address is stored; any later trigger events are ignored.

RESAMPLED WAVEFORMS

When resampling is enabled, the data from all seven channels is calculated and stored into the buffer. One sample set consists of one sample per channel, seven samples total, which are from the same point in time. Each resampled waveforms sample is 16-bits wide.

Figure 51 shows how the resampled waveforms are stored into the buffer.

WAVEFORM BUFFER

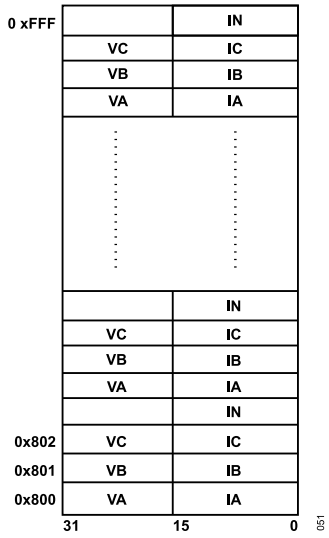

Figure 51. Resampled Waveform Sample Storage

The waveform buffer contains 2048, 32-bit memory locations and can hold 512 (2048/4) sets of samples in coherent fill mode. In the ADE9000, the buffer is filled with 128 resampled points per line cycle, which implies that the buffer can hold four line cycles' worth of data at any instant in time(128 × 4 = 512). With a 50 Hz line frequency, the buffer contains 80 ms worth of resampled data.

The resampler supports line frequency of up to 62.5 Hz this is because the internal DSP that calculates the resample data runs at 8 kHz.

$$Resampling \quad rate_{max} = 8 \quad \text{kHz}/128 = 62.5 \quad \text{Hz} \tag{42}$$

To start filling the waveform buffer with resampled waveforms, first clear the WF_CAP_EN bit to disable the waveform buffer. Then clear the WF_CAP_SEL bit in the WFB_CFG register to select the resampled data to be stored in the waveform buffer. Finally, set the WF_CAP_EN bit to start the resampling process. The waveform buffer starts filling from its first address location, 0x800. When the waveform buffer is full, the COH_WFB_FULL bit of STATUS 0 goes high, which can be enabled to generate an interrupt on $\overline{\text{IRQ0}}$. Note that this is the only status bit available for the resampled waveforms. The filling of the waveform buffer stops.

To obtain a new set of resampled data, first clear the WF_CAP_EN bit in the WFB_CFG register to 0 and then set the bit back to 1.

The time taken to fill the buffer depends on the line frequency. The waveform buffer values are retained even when the waveform buffer is disabled by clearing the WF_CAP_EN bit in the WFB_CFG register.

CONFIGURING THE WAVEFORM BUFFER

The waveform source (sinc4, sinc4 + IIR, xI_PCF/xV_PCF, or resampled), type of capture (continuous, single capture, or stop on trigger), and fill mode (continuous, one time, or based on trigger) must be configured in the WFB_CFG register. To perform this configuration, first disabled the waveform buffer by writing WF_CAP_EN = 0. Then write the WF_SRC, WF_CAP_SEL, and WF_MODE bits in the WFB_CFG register.

When the WF_CAP_EN bit is set, the capture is initiated based on whichever mode is selected by the WF_CAP_SEL and WF_MODE bits in the WFB_CFG register.

For example, if WF_CAP_SEL = 0, resampled waveforms are stored into the buffer. If WF_CAP_SEL = 1, fixed data rate samples are stored into the buffer, and the WF_MODE bits indicate whether the buffer is filled continuously or only one time, and if trigger events affect the buffer filling. All of these bits must be configured before writing the WF_CAP_EN bit in the WFB_CFG register.

When the waveform buffer is disabled by clearing the WF_CAP_EN bit, the waveform buffer data remains valid; however, the LAST_ADDR and WFB_TRIG_ADDR registers are reset.

To start a new waveform capture, disable the waveform buffer by writing WF_CAP_EN = 0. Then configure the WF_CAP_SEL and WF_MODE bits as desired by writing to the WFB_CFG register. Finally, set the WF_CAP_EN bit in the WFB_CFG register to start the capture. Do not change the WF_CAP_SEL or WF_MODE bits while the WF_CAP_EN bit is set.

WAVEFORM BUFFER

BURST READ WAVEFORM BUFFER SAMPLES FROM SPI

The waveform buffer contents can be read using SPI burst read mode. SPI burst read mode allows samples of data to be read while only sending one SPI command header. The transfer of data continues as long as the $\overline{SS}$ line is kept low and SCLK clocks arrive at the ADE9000 SCLK pin.

To make it easier to read out the desired data using the SPI burst read functionality, the user can indicate which channels of data to read out of the waveform buffer by using the BURST_CHAN bits in the WFB_CFG register, as shown in Table 24.

Table 24. Waveform Buffer Burst Read

BURST_CHAN[3:0]	Channels to Burst
0000 (default)	All channels
0001	IA and VA
0010	IB and VB
0011	IC and VC
1000	IA
1001	VA
1010	IB
1011	VB
1100	IC
1101	VC
1110	IN if WF_IN_EN = 1 in the WFB_CFG register
1111	Single address read (SPI burst mode is disabled)

The same BURST_CHAN options are available for both fixed data rate samples and resampled data.

The waveform buffer sample that is read out depends on the selection in BURST_CHAN and on whether the stored data is fixed data rate data or resampled data.

If BURST_CHAN is not equal to 1111 and fixed data rate data is stored in the waveform buffer, when WF_CAP_SEL = 1, the three least significant bits of the address are masked out when determining which sample set to read out.

If BURST_CHAN is not equal to 1111 and resampled data is stored in the waveform buffer, when WF_CAP_SEL = 0, the two least significant bits of the address are masked out when determining which sample set to read out.

If BURST_CHAN is equal to 1111, whichever address was written in the CMD_HDR is read out.

These cases are summarized in Table 25.

Table 25. SPI Address Interpretation when Reading from Waveform Buffer

Capture Type	Address of Sample Set (BURST_CHAN ≠ 1111)	Address of Sample Set (BURST_CHAN = 1111)
Fixed Data Rate Samples (WF_CAP_SEL = 1)	ADDR[11:3]	ADDR[11:0]
Resampled Data (WF_CAP_SEL = 0)	ADDR[11:2]	ADDR[11:0]

Example 1: Fixed Data Rate Data, Seven Channel Samples

WFB_CAP_SEL = 1, WF_IN_EN = 1, and BURST_CHAN = 0000 in the WFB_CFG register indicates that there is fixed data rate data in the waveform buffer and the user wants to read out samples from all seven channels. A command is sent to read Address 0x801, which is interpreted as a read to the sample set starting at Address 0x800. The first 32 SPI clocks return IA from Address 0x800, followed by VA from Address 0x801, and so on, until IN from Address 0x806. Then the sample set auto-increments and the next data is IA from Address 0x808, followed by VA. This example is shown in Figure 52. The default state of the MOSI pin depends on the main SPI device; in Figure 52, it is assumed to be high (Logic 1).

Example 2: Resampled Data, Phase C (I and V Samples)

WFB_CAP_SEL = 0 and BURST_CHAN = 0011 in the WFB_CFG register indicates that there is resampled data in the waveform buffer and the user wants to read out IC and VC samples. A command is sent to read Address 0x801, which is interpreted as a read to the sample set starting at Address 0x800. VC waveform from Address 0x802 is first transferred, followed by IC from Address 0x802. Then the sample set

WAVEFORM BUFFER

auto-increments and the next data is VC from Address 0x806, followed by IC from the same address, then VC from Address 0x80A and IC from Address 0x80A, and so on (see Figure 53). The default state of the MOSI pin depends on the main SPI device; in Figure 53, it is assumed to be high (Logic 1).

Example 3: Fixed Data Rate Data, Single Address Read Mode

WFB_CAP_SEL = 1 and BURST_CHAN = 1111 in the WFB_CFG register indicates that there is fixed data rate data in the waveform buffer and the user wants to read out one single address. A command is sent to read Address 0x801, which is interpreted as a read to Address 0x801. VA waveform from Address 0x801 is transferred, followed by the CRC if BURST_EN = 0. If BURST_EN = 1, the VA waveform data from Address 0x801 is repeated again. This example is shown in Figure 54. The default state of the MOSI pin depends on the main SPI device; in Figure 54, it is assumed to be high (Logic 1). The transfer of data continues as long as the CS line is kept low and SCLK clocks arrive at the ADE9000 SCLK pin.

Example 4: Resampled Data, Single Address Read Mode

WFB_CAP_SEL = 0 and BURST_CHAN = 1111 in the WFB_CFG register indicates that there is resampled data in the waveform buffer and the user wants to read out one single address. A command is sent to read Address 0x801, which is interpreted as a read to Address 0x801. The first 16 SPI clocks return the VA waveform from Address 0x801, followed by the IA waveform from Address 0x801, and finally the CRC if BURST_EN = 0. If BURST_EN = 1, the VA and IA waveform data from Address 0x801 is repeated again (see Figure 55).

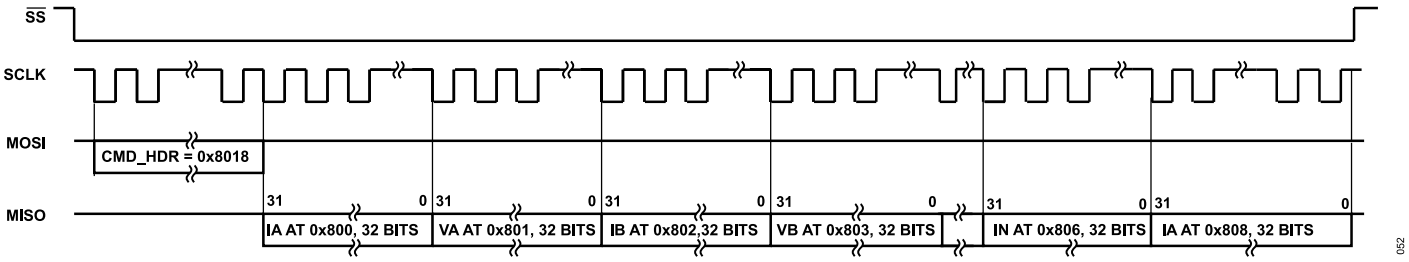

Figure 52. Waveform Buffer SPI Burst Read of Fixed Data Rate Samples, with BURST_CHAN = 0, to Read Out All Channels

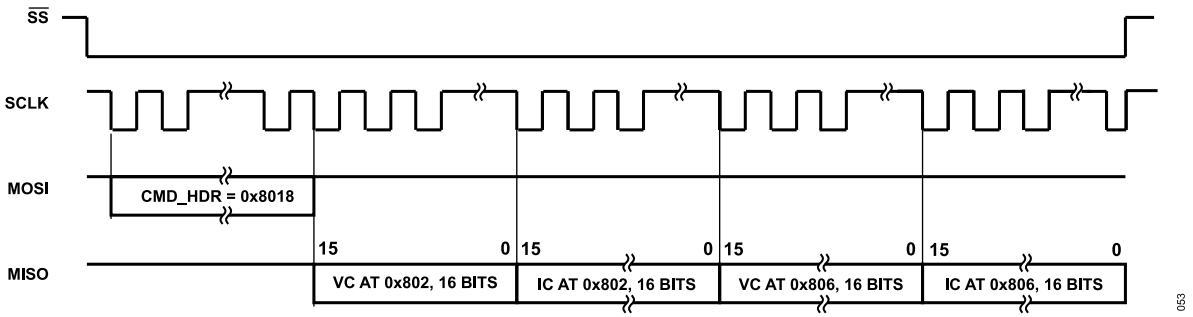

Figure 53. Waveform Buffer SPI Burst Read of Resampled Data, with BURST_CHAN = 0011, to Read out IC and VC Data

WAVEFORM BUFFER

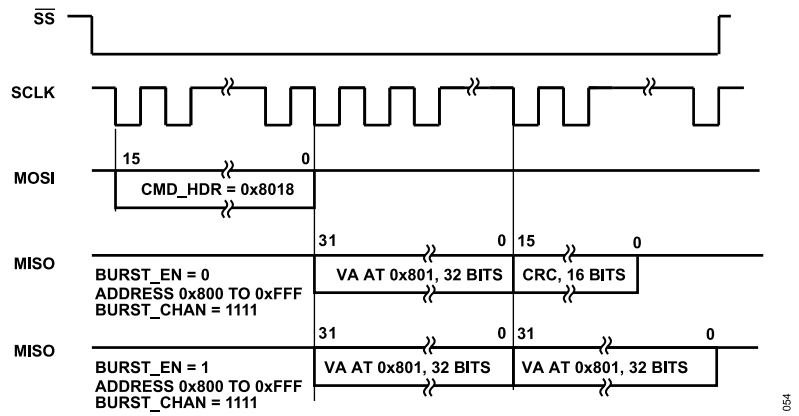

Figure 54. Waveform Buffer SPI Single Address Read of Fixed Rate Data with BURST_CHAN = 1111

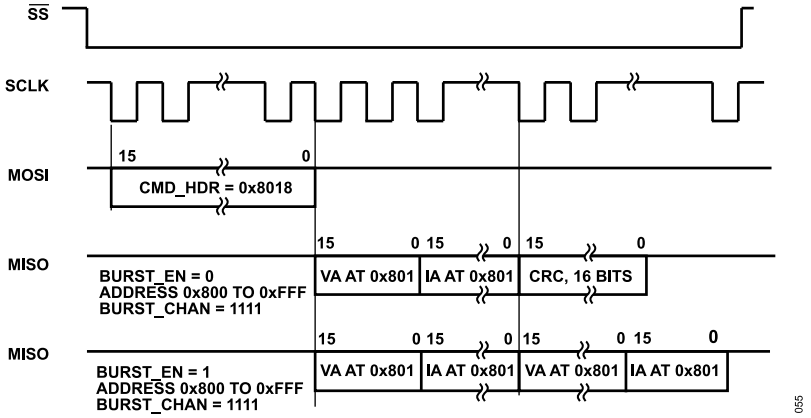

Figure 55. Waveform Buffer SPI Single Address Read of Resampled Data with BURST_CHAN = 1111

SPI CRC When Reading Waveform Buffer

When reading fixed data rate samples, with WF_CAP_SEL = 1, data read out of the waveform buffer has a CRC calculated, which is stored into the CRC_SPI register and can be read back after the waveform buffer burst read.

When reading a single address of waveform buffer data, the CRC_SPI is calculated and appended after the 32-bit data, as shown in Figure 54.

Note that when reading resampled data out of the waveform buffer, when WF_CAP_SEL = 0, the SPI_CRC _RSLT register is not updated. Read the waveform buffer a second time to check the integrity of the SPI read data.

SPI Last Data Register When Reading Waveform Buffer

If BURST_CHAN = 1111, the LAST_DATA_32 register is updated after reading a sample in the waveform buffer with the value of that 32-bit waveform buffer location.

Note that the LAST_DATA_32 register is not updated when reading the waveform buffer samples if BURST_CHAN is not equal to 1111.

INTERRUPTS/$\overline{\text{EVENT}}$

The ADE9000 has three pins, $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and CF4/$\overline{\text{EVENT}}$/DREADY, which can be used as interrupts to the host processor. The $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins go low when an enabled interrupt occurs and stay low until the event is acknowledged by setting the corresponding status bit in the STATUS0 and STATUS1 registers, respectively. The $\overline{\text{EVENT}}$ function, which is multiplexed with the CF4 and DREADY options on the CF4/$\overline{\text{EVENT}}$/DREADY pin, tracks the state of the enabled signals and goes low and high with these internal signals. The $\overline{\text{EVENT}}$ function is useful for measuring the duration of events, such as dips or swells, externally.

INTERRUPTS ($\overline{\text{IRQ0}}$ AND $\overline{\text{IRQ1}}$)

The $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins are managed by 32-bit interrupt mask registers, MASK0 and MASK1, respectively. Every event that can generate an interrupt has a corresponding bit in the MASK0 or MASK1 register and the STATUS0 or STATUS1 register.

To enable an interrupt, set the corresponding bit in the MASK0 or MASK1 register to 1. To disable an interrupt, the corresponding bit in the MASK0 or MASK1 register must be cleared to 0.

The STATUS0 and STATUS1 registers indicate if an event that can generate an interrupt has occurred. If the corresponding bit in the MASK0 or MASK1 register is set, an interrupt is generated on the corresponding $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin, and the pin goes low.

To determine the source of the interrupt, read the corresponding STATUS0 or STATUS1 register and identify which enabled bits are set to 1. To acknowledge the event and clear bits in the STATUSx register, write to the STATUSx register with the desired bit positions set to 1. Then the corresponding $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin goes high.

For example, if a zero-crossing occurs on the Phase A voltage input and the ZXVA bit is set in the MASK1 register, the $\overline{\text{IRQ1}}$ pin goes low, indicating that an enabled event has occurred. To acknowledge the event, write a 1 to the ZXVA bit in the STATUS1 register, and then the $\overline{\text{IRQ1}}$ pin goes low. The ZXVA STATUS1 bit is set regardless of whether the ZXVA bit is enabled in MASK1.

There are a few interrupts that are nonmaskable, meaning that they are generated even if the corresponding bit in the MASKx register is 0. These nonmaskable interrupts include RSTDONE and ERROR0.

There is an option to combine all the interrupts onto a single interrupt pin, $\overline{\text{IRQ1}}$, instead of using two pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$. To activate this option, set the IRQ0_ON_IRQ1 bit in the CONFIG1 register. Note that the $\overline{\text{IRQ0}}$ pin still indicates the enabled $\overline{\text{IRQ0}}$ events while in this mode, and $\overline{\text{IRQ1}}$ indicates both $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ0}}$ events.

The meaning of each individual interrupt source is provided in the related data sheet section; refer to these sections in the ADE9000 data sheet for more information.

$\overline{\text{EVENT}}$

The $\overline{\text{EVENT}}$ function is multiplexed with CF4 and DREADY on the CF4/$\overline{\text{EVENT}}$/DREADY pin. To enable the $\overline{\text{EVENT}}$ function to be output on this pin, write CF4_CFG = 10 in the CONFIG1 register.

There are 16 signals that can be incorporated into the $\overline{\text{EVENT}}$ pin and are selected in the EVENT_MASK register. All of these events sources are maskable and disabled by default.

The logic level of the $\overline{\text{EVENT}}$ output is solely dependent on the enabled events; it cannot be changed by the user. If any of the 16 events are enabled by setting their corresponding mask bit to 1 in the EVENT_MASK register, the $\overline{\text{EVENT}}$) pin goes low whenever one of the enabled events occurs and stays low until all the enabled signals have gone high. Then, the $\overline{\text{EVENT}}$ pin goes high. Note that the status sources used to generate the $\overline{\text{EVENT}}$ are not latched; if one event source is selected, the $\overline{\text{EVENT}}$ pin tracks the status of that source.

STATUS BITS IN ADDITIONAL REGISTERS

Several interrupts are used in conjunction with other status registers.

Overcurrent

The OI bit in the MASK1 register works in conjunction with the OIPHASE status bits in the OISTATUS register.

No Load

The VAFNOLOAD, RFNOLOAD, AFNOLOAD, VANLOAD, RNLOAD, and ANLOAD bits in the MASK1 register work in conjunction with additional status bits in the PHNOLOAD register.

INTERRUPTS/$\overline{\text{EVENT}}$

The following bits in the MASK0 register work with the status bits in the PHSIGN register: REVAPx, REVRPx, and REVPSUMx.

Read the additional registers to obtain more information when the corresponding bits are set in the STATUSx register.

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

The voltage and current waveforms of a polyphase system are defined in the following equations:

$$v_a(t) = \sqrt{2}\sin(\omega t) \quad (43)$$

$$v_b(t) = \sqrt{2}\sin(\omega t - 120°) \quad (44)$$

$$v_c(t) = \sqrt{2}\sin(\omega t + 120°) \quad (45)$$

$$i_a(t) = \sqrt{2}\sin(\omega t - \theta) \quad (46)$$

$$i_b(t) = \sqrt{2}\sin(\omega t - \theta - 120°) \quad (47)$$

$$i_c(t) = \sqrt{2}\sin(\omega t - \theta + 120°) \quad (48)$$

To understand how these signals relate to each other, create a phasor diagram following a convention using lagging phase angles. Figure 56 shows a common polyphase metering configuration, the 4-wire wye, with v_a, v_b, and v_c defined in the previous equations. Phase B lags Phase A by 120°, and Phase C lags Phase A by 240°. Currents are shown at a power factor of 1, PF = 1, where θ = 0 in the i_a, i_b, and i_c expressions (shown previously), and the current is in phase with the voltage.

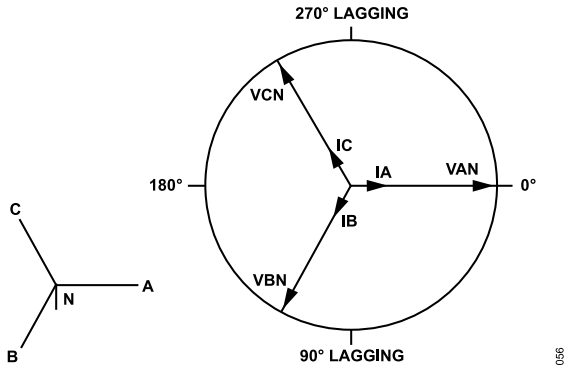

Figure 56. 4-Wire Wye Service Vector Diagram

The following figures show common metering configurations: 3-wire delta, 4-wire delta, and 3-wire residential and network. The ADE9000 can also measure multiple single-phase circuits.

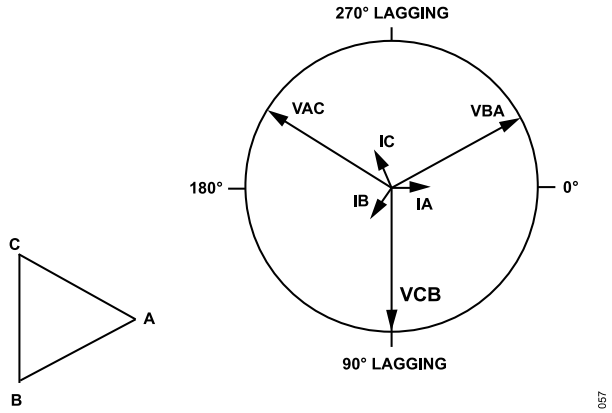

Figure 57. 3-Wire Delta Service Vector Diagram

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

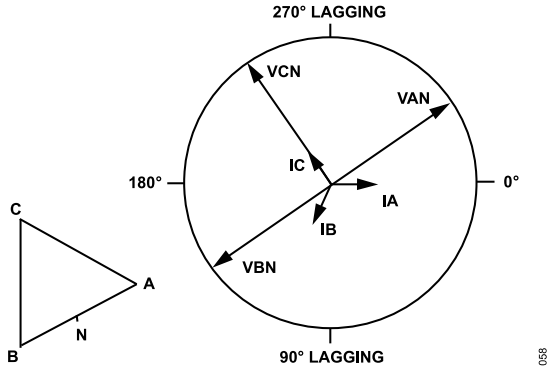

Figure 58. 4-Wire Delta Service Vector Diagram

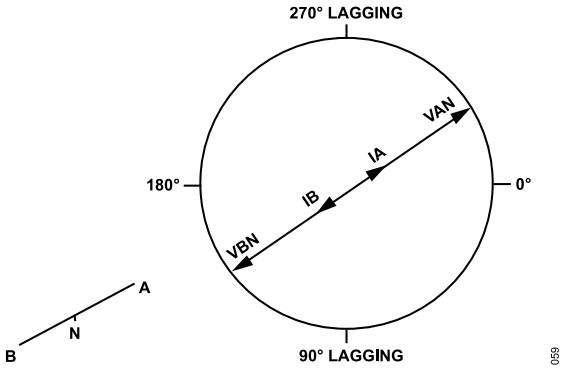

Figure 59. 3-Wire Residential 1PH Service Vector Diagram

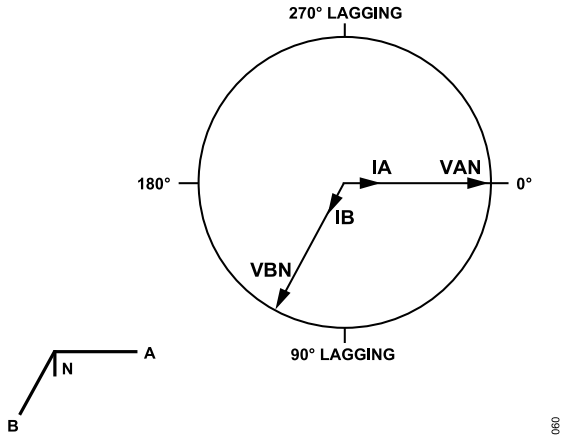

Figure 60. 3-Wire Network Meter Vector Diagram

The phasor diagrams help to understand how the voltages and currents are related in time. Figure 61 shows the 4-wire wye voltage phase sequence in time, corresponding to the Figure 56 phasor diagram and the equations for v_a, v_b, and v_c provided previously.

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

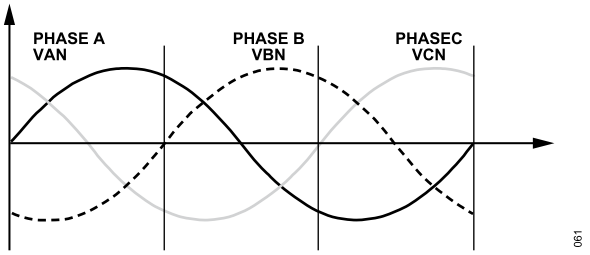

Figure 61. 4-Wire Wye, Voltage Phase Sequence in Time

NON-BLONDEL COMPLIANT METERS

Blondel's theorem states that there must be n − 1 measuring elements in a meter, where n is the number of the wires of the electric system. In this way, a Blondel compliant 4-wire wye or 4-wire delta measures three voltages and three currents. In a 3-wire delta service, at least two voltages and two currents must be measured to be Blondel compliant.

IEC meter forms are all Blondel compliant. ANSI has some meter forms that are not Blondel compliant, meaning that there are fewer than n − 1 elements, so that in a 4-wire wye or 4-wire delta, two voltage and three currents are measured. The ADE9000 has provisions to deal with non-Blondel compliant meter forms. Use the VCONSEL[2:0] bits in the ACCMODE register to select what calculation to use for VB based on the VA and VC signals.

Table 26. Non-Blondel Compliant Meter Forms

Service Type	Non-Blondel Compliant ANSI Meter Form	VCONSEL[2:0]	VB Calculation
4-Wire Wye, 2 Voltages, 3 Currents	6S, 7S, 14S, 29S, 36S, 46S, 76S	010	VB = −VA − VC
4-Wire Delta, 2 Voltages, 3 Currents	8S, 15S, 24S	011	VB = −VA

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

APPLYING THE ADE9000 TO A 4-WIRE WYE SERVICE

For the highest level of performance when measuring a 4-wire wye service, connect the neutral to ground, as shown in Figure 62. For this configuration, VCONSEL[2:0] = 000.

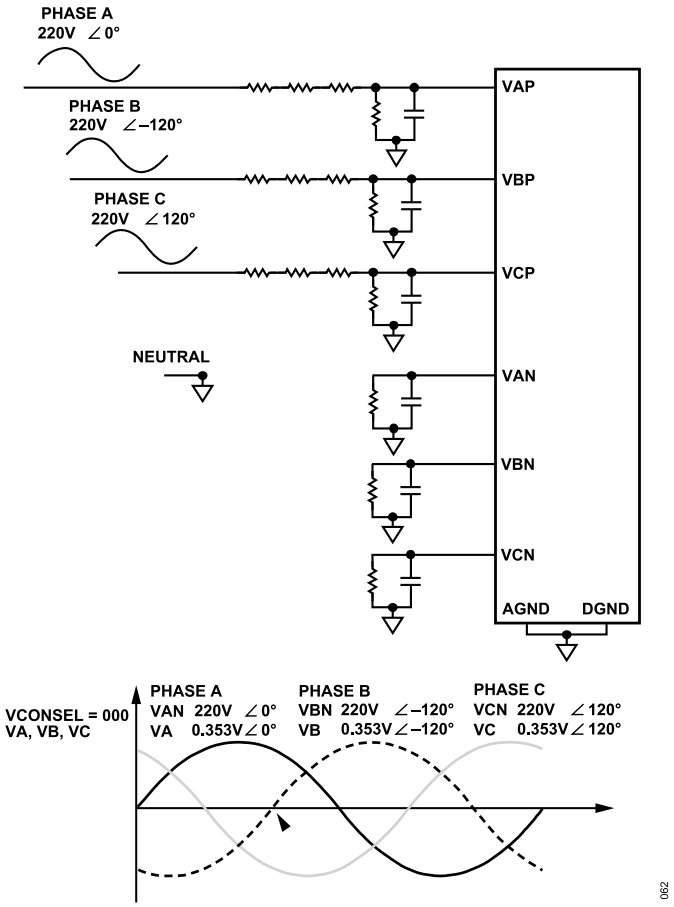

Figure 62. 4-Wire Wye, Neutral Connected to Ground

Alternatively, a series impedance can be used on the neutral, as shown in Figure 63, which can be advantageous if an isolated power supply is used. Note that this configuration has poor performance if the phase voltages are not balanced. For more information, refer to the AN-1334. For this configuration, VCONSEL[2:0] = 000.

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

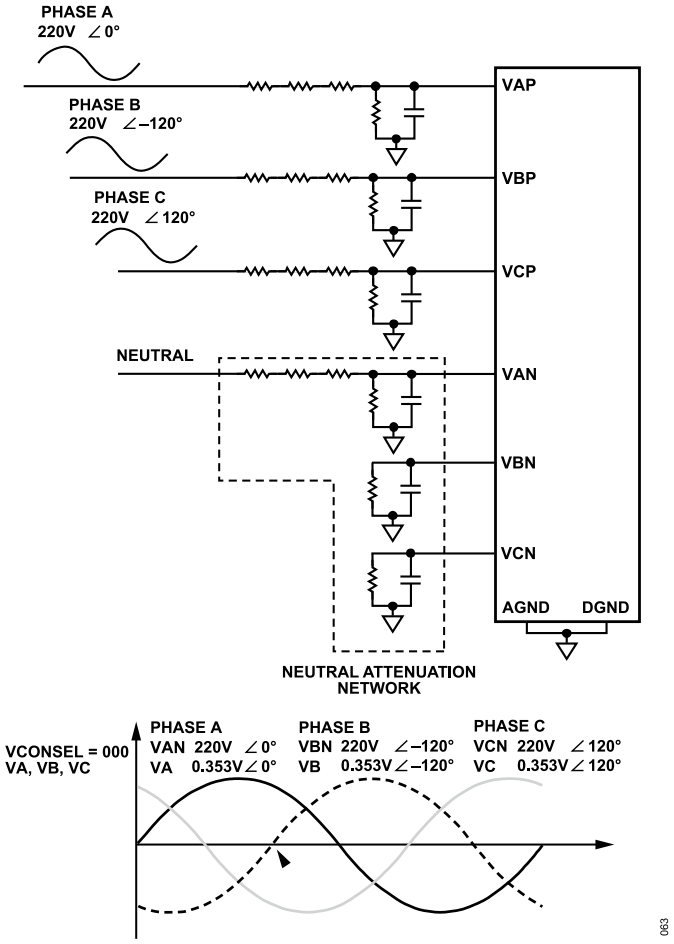

Figure 63. 4-Wire Wye, Series Impedance on the Neutral

Phase sequence error detection is performed based on the expected ABC sequence; see the Phase Sequence Error Detection section for more information.

To obtain the overall power consumed by the system (active, reactive, and apparent), add the contribution from the Phase A, Phase B, and Phase C accumulations.

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

APPLYING THE ADE9000 TO A 3-WIRE DELTA SERVICE

For the highest level of performance when measuring a 3-wire delta service, connect Phase B to ground, as shown in Figure 64. For this configuration, write VCONSEL[2:0] = 001 or 100. Then VB = VA − VC, and the ADE9000 calculates the VAC potential in the BVRMS register. To calculate the current flowing through IB from the IA and IC measurements, set ICONSEL = 1 so that IB = −IA − IC.

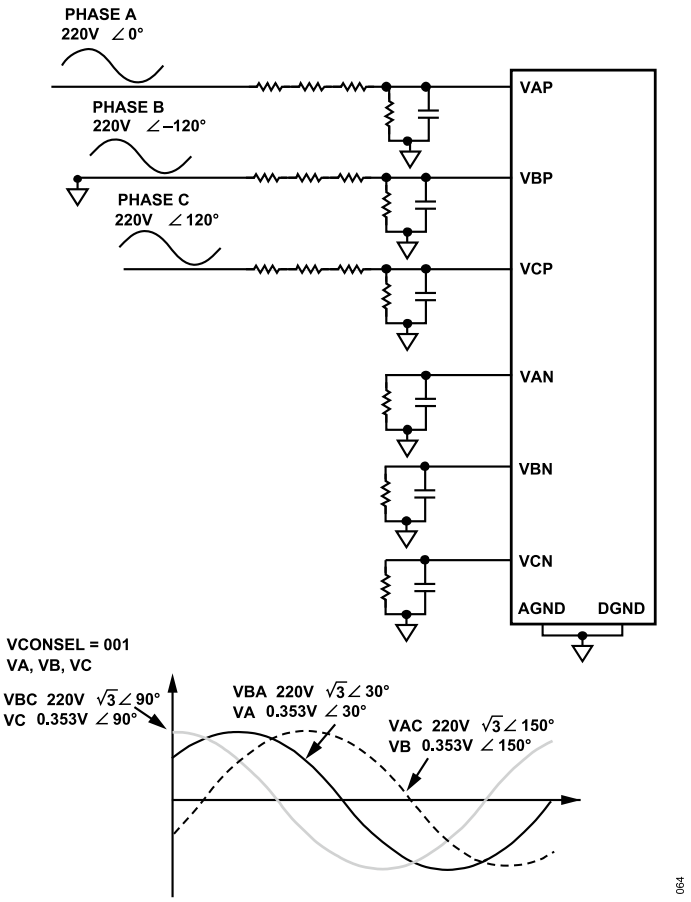

Figure 64. 3-Wire Delta, Phase B Connected to Ground

Note that for this 3-wire delta, Phase B connected to ground configuration, the phasor diagram of the VA, VC, and VB waveforms inside the ADE9000 IC, shown in Figure 65, is shifted compared to the service diagram shown in Figure 57.

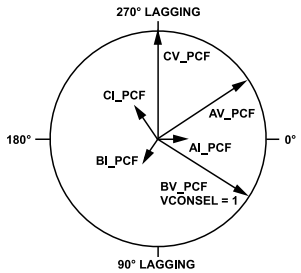

Figure 65. Phasor Diagram of xV_PCF and xI_PCF Waveforms Inside the IC with 3-Wire Delta with Phase B as Ground and VCONSEL = 001

To use the same PCB for both 4-wire wye and 3-wire delta circuits, another option is to wire Phase B to the neutral terminal of the meter, keeping the same circuit as used in Figure 62 or Figure 63. Note that VCONSEL[2:0] must be set to 001 if it is desired to obtain the VAC rms value, which is calculated in the BVRMS register, and to use the correct phase sequence detection method for the 3-wire delta configuration. To calculate the current flowing through IB from the IA and IC measurements, set ICONSEL = 1 so that IB = −IA − IC.

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

Alternatively, a series impedance can be used on Phase B, as shown in Figure 66. This configuration can be advantageous if an isolated power supply is used; however, the readings are inaccurate in this configuration if the phase voltages are not balanced. Use VCONSEL[2:0] = 100 with this configuration so that VA = VA − VB, VB = VA − VC, and VC = VC − VB. To calculate the current flowing through IB from the IA and IC measurements, set ICONSEL = 1 so that IB = −IA − IC.

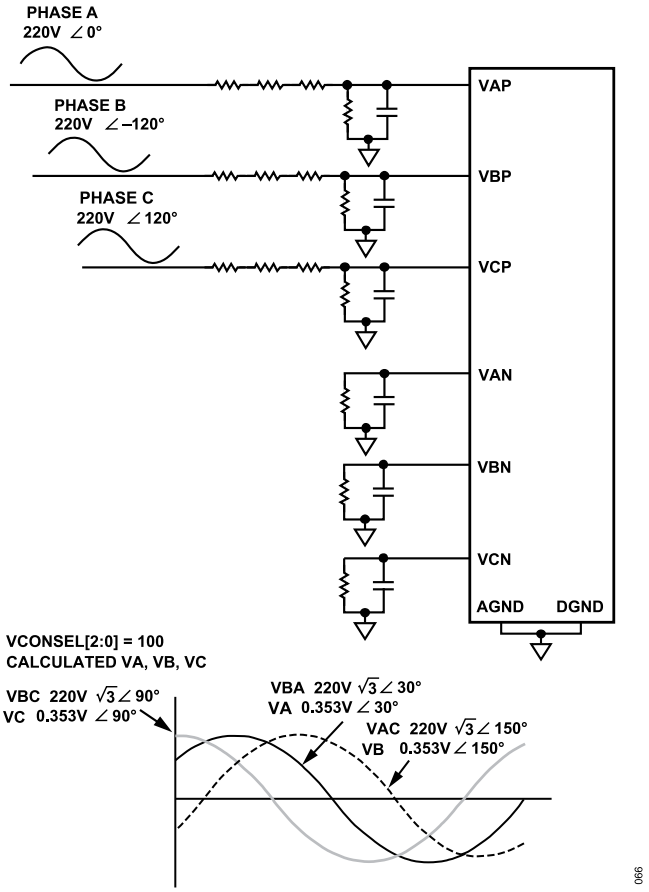

Figure 66. 3-Wire Delta, Series Impedance on Phase B and VCONSEL = 100

The phasor diagram of the VA, VB, and VC waveforms computed inside the ADE9000 for the 3-wire delta with series impedance on Phase B and VCONSEL = 100 matches the one shown in Figure 65.

Phase sequence error detection is performed with the expectation that the VC waveform leads VA; see the Phase Sequence Error Detection section for more information.

In a Blondel compliant 3-wire delta meter, only the overall power consumed by the system is meaningful; the individual phase powers are not meaningful because a line current is multiplied by a line to line voltage. To obtain the overall power consumed by the system (active, reactive, and apparent), add the contribution from Phase A and Phase C.

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

APPLYING THE ADE9000 TO A NON-BLONDEL COMPLIANT 4-WIRE WYE SERVICE

To use the ADE9000 in a non-Blondel compliant 4-wire wye service (such as for ANSI meter forms 6S, 7S, 14S, 29S, 36S, 46S, and 76S), the Phase A and Phase C voltages are measured and the Phase B voltage is calculated, VB = −VA − VC. All three phase currents are measured. For this configuration, write VCONSEL[2:0] = 010 and connect as shown in Figure 67.

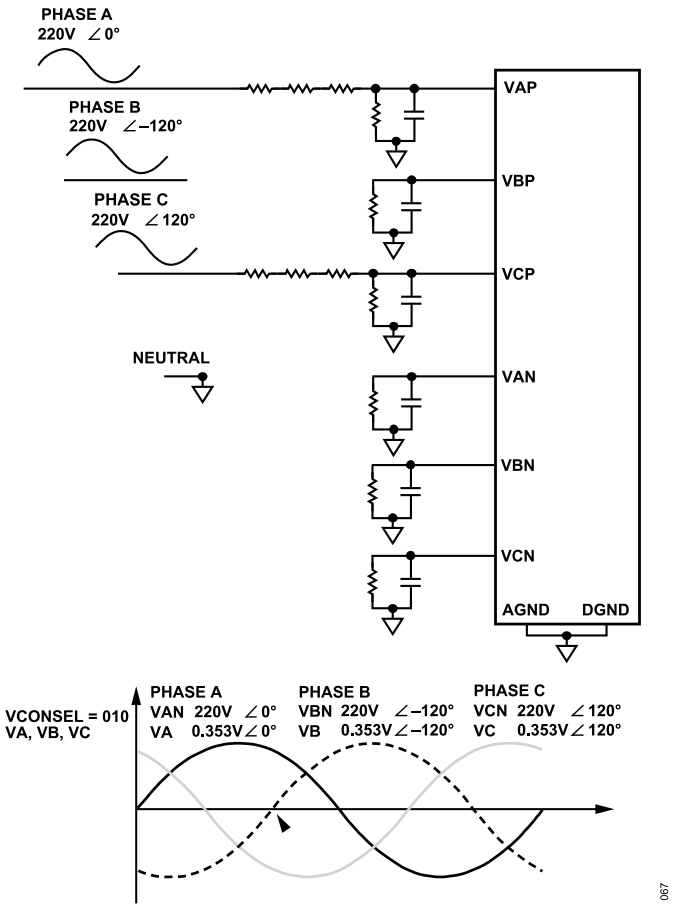

Figure 67. Non-Blondel Compliant 4-Wire Wye

The phasor diagram follows Figure 56. Phase sequence error detection is performed based on the expected ABC sequence; see the Phase Sequence Error Detection section for more information.

To obtain the total power (active, reactive, and apparent), add the contribution from Phase A, Phase B, and Phase C.

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

APPLYING THE ADE9000 TO A NON-BLONDEL COMPLIANT 4-WIRE DELTA SERVICE

To use the ADE9000 in a non-Blondel compliant 4-wire delta service (such as for ANSI meter forms 8S, 15S, and 24S), the Phase A and Phase C voltages are measured and the Phase B voltage is calculated, VB = −VA. All three phase currents are measured. For this configuration, write VCONSEL[2:0] = 011 and connect as shown in Figure 68 .

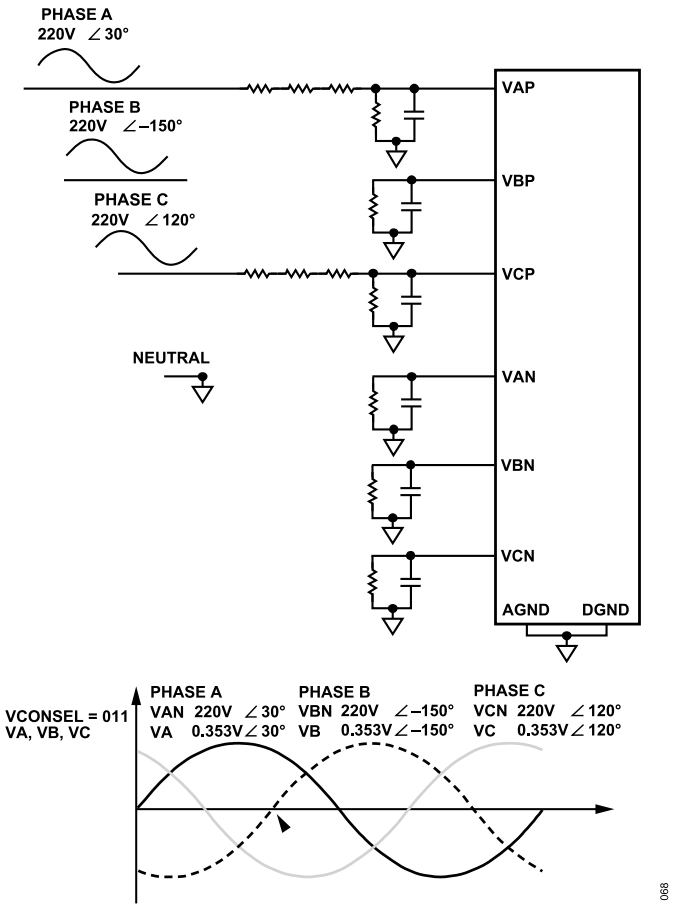

Figure 68. Non-Blondel Compliant 4-Wire Delta

The phasor diagram follows Figure 58. Phase sequence error detection is performed based on the expected ABC sequence; see the Phase Sequence Error Detection section for more information.

To obtain the total power (active, reactive, and apparent), add the contribution from Phase A, Phase B, and Phase C.

APPLYING THE ADE9000 TO DIFFERENT METERING CONFIGURATIONS

ADE9000 SERVICE TYPE SUMMARY

To summarize, the ADE9000 can be used in many different configurations to measure 4-wire wye, 4-wire delta, and 3-wire delta installations. Table 27 summarizes which VCONSEL[2:0] and ICONSEL settings to use for each configuration.

Table 27. Service Type and VCONSEL, ICONSEL Setting Summary

Service Type	ADE9000 Ground Reference	Figure for Reference	Number of Voltage Sensors Required	VCONSEL[2:0]	Number of Current Sensors Required	ICONSEL
4-Wire Wye	Neutral	Figure 62	3	000	3	0
4-Wire Wye	Isolated	Figure 63	3	000	3	0
3-Wire Delta	Phase B	Figure 64; Figure 62 with Phase B tied to neutral	2	001; VB = VA − VC	2	0: IB has current sensor1: IB = IA − IC
3-Wire Delta	Isolated	Figure 63 with Phase B tied to neutral	2	001; VB = VA − VC	2	0: IB has current sensor1: IB = −IA − IC
3-Wire Delta	Isolated	Figure 66	2	100; VA = VA − VB; VB = VA − VC; VC = VC − VB	2	0: IB has current sensor1: IB = −IA − IC
4-Wire Delta	Neutral	Figure 62 (note that VA and VB phasor diagram follows Figure 58)	3	000	3	0
4-Wire Wye, Non-Blondel Compliant	Neutral	Figure 67	2	010; VB = −VA − VC	3	0
4-Wire Delta, Non-Blondel Compliant	Neutral	Figure 68	2	011; VB = −VA	2	0: IB has current sensor1: IB = −IA − IC
3-Wire 1PH	Neutral	Not applicable	1 to 2	000	1 to 2	0
3-Wire Network	Neutral	Not applicable	2	000	2	0
Multiple 1PH Circuits	Neutral	Not applicable	3	000	3	0

QUICK START

This section describes how to set up the ADE9000 for a 3-phase, 4-wire wye measurement. Figure 62 shows the typical hardware connection for a 3-phase, 4-wire wye configuration.

1. Wait for the RSTDONE interrupt, indicated by the $\overline{\text{IRQ}}$ pin going low.
2. Configure PSM0 normal power mode by setting the PM1 pin and the PM0 pin to low.
3. Configure PGA gain on current and voltage channels using the PGA_GAIN gain register. The default gain on all channels is 1.
4. Configure the HPFDIS bits in the CONFIG0 register to enable/disable the high-pass filter. The high-pass filter is enabled by default. It is recommended to keep the high-pass filter enabled. Set the desired corner frequency for HPF using the HPF_CRN bits in the CONFIG2 register. The default value for HPF_CRN is 6 (1.25 Hz).
5. If Rogowski coils are used as current sensors, enable the digital integrator using the INTEN and INITEN bits in the CONFIG0 register. Disable the integrator when using current transformers. The digital integrators are disabled by default.
   a. If an integrator is enabled, set the DICOEFF register to 0xFFFFE000.
6. Configure the expected fundamental frequency using the SELFREQ bit (50 Hz: SELFREQ = 0, 60 Hz: SELFREQ = 1) in the ACCMODE register, and program the nominal voltage in the VLEVEL register for fundamental calculations. VLEVEL = X × 1,144,084, where X is the dynamic range that the nominal signal is at with respect to full scale.
7. Configure the zero-crossing source for ZX detection. If ZX_SRC_SEL = 1 in the CONFIG0 register, data before the HPF, integrator, and phase compensation is used. If ZX_SRC_SEL = 0, data after the HPF, integrator, and phase compensation is used. It is recommended to have ZX_SRC_SEL = 0.
8. Set VCONSEL = 000 in the ACCMODE register for a 3-phase, 4-wire wye configuration.
9. If energy is monitored using the CF outputs, configure the following registers. Skip this section if the CF outputs are not used.
   a. Configure the CFxSEL bits in the CFMODE register to select the energy type to monitor.
   b. Configure the TERMSELx bits in the COMPMODE register to select the phases to include in the CF calculation.
   c. Program xTHR to 0x00100000.
   d. Compute and program the corresponding CFxDEN register based on the desired impulses per kilowatt-hour.
   e. Configure the CF pulse width using the CF_LCFG register.
10. If energy is monitored using energy registers, configure the following registers:
    a. Configure the WATTACC and VARACC bits in the ACCMODE register to select amongst available accumulation modes (for example: signed, absolute, positive, or negative accumulation mode). The default accumulation mode is signed.
    b. Configure the NOLOAD_TMR bits in the EP_CFG register and set the ACT_NL_LVL, REACT_NL_LVL, and APP_NL_LVL level registers to detect no load and prevent energy accumulation of noise.
    c. Configure the EGY_TMR_MODE bit in the EP_CFG register to select sample (EGY_TMR_MODE = 0) or line cycle (EGY_TMR_MODE = 1) accumulation. Set the desired samples or half line cycles in the EGY_TIME register.
    d. Configure the EGY_LD_ACCUM bit in the EP_CFG register to add the internal energy register to user energy register on EGYRDY (EGY_LD_ACCUM = 0), or to overwrite the user energy register with the internal energy register value (EGY_LD_ACCUM = 1).
    e. Configure the RD_RST_EN bit in the EP_CFG register to enable reset of user energy registers on read (RD_RST_EN = 1), or to disable reset of user energy registers on read (RD_RST_EN = 0).
11. The ADE9000 can provide interrupts for a variety of events on the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins. The MASK0 or MASK1 and STATUS0 or STATUS1 registers manage the respective interrupt pins.
12. See the Power Quality Measurements section to configure the power quality parameters.
13. See the Waveform Buffer section to configure and use the waveform buffer.
14. Enable the DSP by setting the RUN register = 1, and enable energy accumulation by setting the EGY_PWR_EN bit in the EP_CFG register = 1.
15. Note that calibration is performed once at typical operating conditions. When the calibration values are computed, write the constants to registers before enabling the DSP.
16. To prevent any changes to the ADE9000 configuration, enable write protection by writing 0x3C64 to the WR_LOCK register.

CALIBRATION

The following section describes calibrating the ADE9000 using register readings. The expected register values at full scale are used as the reference.

Table 28. Full-Scale ADC Codes

Parameter	Full-Scale Codes (Decimal)
Total and Fundamental IRMS and VRMS	52,702,092
Total and Fundamental WATT, VAR, and VA	20,694,066
Fast RMS½	52,702,092
10 Cycle RMS/12 Cycle RMS	52,702,092
Resampled Data	18,196

SYSTEM PARAMETERS

The system is calibrated at nominal operating voltage and current using an accurate source. The accuracy of the calibration is less than or equal to the accuracy of the source. The example shows the calibration for Channel A. The calculations are similar for Channel B and Channel C.

- $V_{NOMINAL}$ = 220 V rms
- $I_{NOMINAL}$ = 10 A rms
- Line frequency = 50 Hz
- Current transformer ratio = 3000:1
- Burden resistor = 20 Ω
- Voltage Divider R1 = 990 kΩ
- R2 = 1 kΩ

The current transfer function is 20/3000 = 0.0067 V rms/A rms.

The voltage transfer function is 1/(900 + 1) = 0.001 V rms/A rms.

The input at the current ADC pins is 0.0067 × 10 = 0.067 V rms.

The input at the voltage ADC pins is 0.001 × 220 = 0.22 V rms.

The ADC full-scale voltage at gain = 1 is 0.707 V rms.

The nominal current as a percentage of full scale is I_{FSP} = 0.067/0.707 = 9.47%.

The nominal voltage as a percentage of full scale is V_{FSP} = 0.220/0.707 = 31.1%.

RMS CALIBRATION

AIGAIN and AVGAIN are the respective current and voltage calibration registers for Channel A.

With the nominal voltage and current inputs, read the AIRMS and AVRMS registers. It is recommended to read the rms values at zero-crossings for 1 sec and average them for better accuracy.

For this example, the AIRMS register reading is 5,294,441.

The expected AIRMS register reading is

I_{FSP} × *full-scale rms codes* = 0.0947 × 52,702,092 = 4,801,488 (49)

Therefore, the following gain must be applied to reach the expected value:

$$GAIN = \frac{AIRMS_{EXPECTED}}{AIRMS_{MEASURED}} = \frac{4,801,488}{5,294,441} = 0.907 \quad (50)$$

The AIGAIN register is calculated as follows:

$AIGAIN = (GAIN - 1) \times 2^{27} = -12,482,248 = 0xFF418938$ (51)

CALIBRATION

To calibrate AIRMSOS offset register, apply a small current typically at 5000:1 or less dynamic range. In this example, the offset calibration current is 20 mA.

After applying offset calibration current, the AIRMS register reading is 70,431.

The expected AIRMS register reading is

$$Icalibration_{FSP} \times Full\text{-}Scale\ RMS\ Codes = 0.0002 \times 52{,}702{,}092 = 10{,}540. \quad (52)$$

The AIRMSOS register is calculated as

$$AIRMSOS = \frac{AIRMS_{EXPECTED}{}^2 - AIRMS_{MEASURED}{}^2}{2^{15}}$$
$$= \frac{10{,}540^2 - 70{,}431^2}{2^{15}} \quad (53)$$
$$= -147{,}992 \quad = \quad 0x\text{FFFDBDE8}$$

Follow similar steps to obtain the AVGAIN and AVRMSOS calibration constants.

PHASE CALIBRATION

APHCAL0 is the phase calibration register for Channel A.

To calculate APHCAL0, apply a nominal current and voltage at a lagging 0.5 power factor such that the active and reactive energy registers are positive. In this example, the energy registers are configured such that EP_CFG = 0x0011 and EGY_TIME = 7999 (1 sec accumulation).

Read the AWATTHR_HI and AVARHR_HI registers.

$$Phase\ \ Error\ \ (\varphi)$$
$$= -\tan^{-1}\left(\frac{AWATTHR\_HI \times \sin(60) - AVARHR\_HI \times \cos(60)}{AWATTHR\_HI \times \cos(60) - AVARHR\_HI \times \sin(60)}\right) \quad (54)$$
$$= -\tan^{-1}\left(\frac{10356 \times \sin(60) - 17585 \times \cos(60)}{10356 \times \cos(60) - 17585 \times \sin(60)}\right)$$
$$= -0.49°$$

Therefore, the phase calibration register is

$$APHCAL0 = \left(\frac{\sin(\varphi - \omega) + \sin\omega}{\sin(2 \times \omega - \varphi)}\right) \times 2^{27}$$
$$= \left(\frac{\sin(RADIAN(-0.49) - 0.039) + \sin(0.039)}{\sin(2 \times 0.039 - RADIAN(-0.49))}\right) \times 2^{27} \quad (55)$$
$$= -13265997 = 0x\text{FF3593}B3$$

APHCAL0 = 0xFF3593B3

Follow similar steps to obtain the BPHCAL0 and CPHCAL0 calibration constants.

POWER CALIBRATION

APGAIN is the gain calibration register for Phase A. The active, reactive, and apparent powers in each phase have a common gain register and individual offset calibration registers.

1. Apply the nominal voltage and current at power factor = 1.
2. EP_CFG = 0x0011 and EGY_TIME = 7999 (1 sec accumulation).
3. Read the AWATTHR_HI register.
4. The APGAIN register value is obtained as follows:

$$APGAIN = \frac{AWATTHR\_HI_{EXPECTED} - AWATTHR\_HI_{MEASURED}}{AWATTHR\_HI_{MEASURED}} \times 2^{27} \quad (56)$$

AWATTHR_HI$_{EXPECTED}$ = I_{FSP} × V_{FSP} × *Full-Scale Power Codes* × *Accumulation Time* × 8000 × 2^{-13} = 0.0947 × 0.311 × 20,694,066 × 1 sec × 8000 × 2^{-13} = 595,191

CALIBRATION

Let AWATTHR_HI$_{MEASURED}$ = 580,000:

$$APGAIN = \frac{595,191 - 580,000}{580,000} \times 2^{27} = 3515347 = 0x35A3D3$$

Like the rms offset calibration, the power offset calibration is performed with a small current at 5000:1 or less dynamic range. In this example, the offset calibration current is 20 mA and the voltage is 220 V.

1. Apply a nominal voltage and offset calibration current at power factor = 1.
2. EP_CFG = 0x0013 and EGY_TIME = 1000 (10 sec accumulation).
3. Read the AWATTHR_HI register.
4. AWATTOS is calculated as

$$AWATTOS = \frac{AWATTHR\_HI_{EXPECTED} - AWATTHR\_HI_{MEASURED}}{Accumulation\ \ Time \times f_{DSP} \times 2^{-13}} \quad (57)$$

AWATTHR_HI$_{EXPECTED}$ = *Icalibration$_{FSP}$* × *V$_{FSP}$* × *Full-Scale Power Codes* × *Accumulation Time* × 8000 × 2^{-13} = 0.0002 × 0.311 × 20,694,066 × 10 sec × 8000 × 2^{-13} = 12570

$$AWATTOS = \frac{12,570 - 11,000}{10 \times 8000 \times 2^{-13}} = 161 = 0xA1$$

5. To compute AVAROS, apply a nominal voltage and offset calibration current at power factor = 0.

Follow similar steps to obtain BPGAIN, BWATTOS, BVAROS, CPGAIN, CWATTOS, and CVAROS.

CONVERSION CONSTANTS

Conversion constants are used to convert ADE9000 register readings into physical parameters. When the device is calibrated to the full-scale ADC codes given in Table 28, the conversion constants for the example system are calculated as follows:

$$Current\ \ Conversion\ \ Constant\ \left(\frac{\mu Arms}{LSB}\right)$$
$$= \frac{Inominal \times 10^6}{I_{FSP} \times Full-scale\ \ RMS\ \ codes} \quad (58)$$
$$= \frac{10 \times 10^6}{0.0947 \times 52,702,092}$$
$$= 2.0036\ \ \mu Arms/LSB$$

$$Voltage\ \ Conversion\ \ Constant\ \left(\frac{\mu Vrms}{LSB}\right)$$
$$= \frac{Vnominal \times 10^6}{V_{FSP} \times Full-scale\ \ RMS\ \ codes} \quad (59)$$
$$= \frac{220 \times 10^6}{0.311 \times 52,702,092}$$
$$= 13.4225\ \ \ \mu Vrms/LSB$$

$$Power\ \ Conversion\ \ Constant\ \left(\frac{mWATT/mVAR/mVA}{LSB}\right)$$
$$= \frac{Inominal \times Vnominal \times 10^3}{I_{FSP} \times V_{FSP} \times Full-scale\ \ Power\ \ codes} \quad (60)$$
$$= \frac{10 \times 220 \times 10^3}{0.0947 \times 0.311 \times 20,694,066}$$
$$= 3.6097\ \ \left(mWATT/mVAR/mVA\right)/LSB$$

CALIBRATION

$$Energy\ \ Conversion\ \ Constant\ \left(\frac{\mu WATTHr/\mu VARHr/\mu VAHr}{LSB}\right)$$
$$= \frac{Inominal \times Vnominal \times 10^6}{I_{FSP} \times V_{FSP} \times Full-scale\ \ Power\ \ codes \times 2^{-13} \times 3600 \times 8000} \quad (61)$$
$$= \frac{10 \times 220 \times 10^6}{0.0947 \times 0.311 \times 20,694,066 \times 2^{-13} \times 3600 \times 8000}$$
$$= 1.0268\ \left(\mu WATTHr/\mu VARHr/\mu VAHr\right)/LSB$$

The physical parameters are obtained by multiplying the register readings with the respective conversion constants.

For example, if the AIRMS register reading is 10,540,400 decimal codes,

Phase A rms current (A rms) = 2.0036 µA rms/LSB × 10,540,400 = 21.12 A rms

ERRATA

There is a bug in read with reset when using energy accumulation. Using line cycle or sample base accumulation is suggested. Register affected by this is RD_RST_EN, keep this register at the default value of 0.

REGISTER INFORMATION

Table 29. Register Summary

Address	Name	Description	Reset[1]	Access
0x000	AIGAIN	Phase A current gain adjust.	0x00000000	R/W
0x001	AIGAIN0	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x002	AIGAIN1	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x003	AIGAIN2	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x004	AIGAIN3	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x005	AIGAIN4	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x006	APHCAL0	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x007	APHCAL1	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x008	APHCAL2	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x009	APHCAL3	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x00A	APHCAL4	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x00B	AVGAIN	Phase A voltage gain adjust.	0x00000000	R/W
0x00C	AIRMSOS	Phase A current rms offset for the filter-based AIRMS calculation.	0x00000000	R/W
0x00D	AVRMSOS	Phase A voltage rms offset for the filter-based AVRMS calculation.	0x00000000	R/W
0x00E	APGAIN	Phase A power gain adjust for the AWATT, AVA, AVAR, AFWATT, AFVA, and AFVAR calculations.	0x00000000	R/W
0x00F	AWATTOS	Phase A total active power offset correction for the AWATT calculation.	0x00000000	R/W
0x010	AVAROS	Phase A total reactive power offset correction for the AVAR calculation.	0x00000000	R/W
0x011	AFWATTOS	Phase A fundamental active power offset correction for the AFWATT calculation.	0x00000000	R/W
0x012	AFVAROS	Phase A fundamental reactive power offset correction for the AFVAR calculation.	0x00000000	R/W
0x013	AIFRMSOS	Phase A current rms offset for the fundamental current rms, AIFRMS calculation.	0x00000000	R/W
0x014	AVFRMSOS	Phase A voltage rms offset for the fundamental voltage rms, AVFRMS calculation.	0x00000000	R/W
0x015	AVRMSONEOS	Phase A voltage rms offset for the fast RMS½ AVRMSONE calculation.	0x00000000	R/W

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x016	AIRMSONEOS	Phase A current rms offset for the fast RMS½ AIRMSONE calculation.	0x00000000	R/W
0x017	AVRMS1012OS	Phase A voltage rms offset for the 10 cycle rms/12 cycle rms AVRMS1012 calculation.	0x00000000	R/W
0x018	AIRMS1012OS	Phase A current rms offset for the 10 cycle rms/12 cycle rms AIRMS1012 calculation.	0x00000000	R/W
0x020	BIGAIN	Phase B current gain adjust.	0x00000000	R/W
0x021	BIGAIN0	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x022	BIGAIN1	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x023	BIGAIN2	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x024	BIGAIN3	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x025	BIGAIN4	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x026	BPHCAL0	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x027	BPHCAL1	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x028	BPHCAL2	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x029	BPHCAL3	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x02A	BPHCAL4	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x02B	BVGAIN	Phase B voltage gain adjust.	0x00000000	R/W
0x02C	BIRMSOS	Phase B current rms offset for the BIRMS calculation.	0x00000000	R/W
0x02D	BVRMSOS	Phase B voltage rms offset for the BVRMS calculation.	0x00000000	R/W
0x02E	BPGAIN	Phase B power gain adjust for the BWATT, BVA, BVAR, BFWATT, BFVA, and BFVAR calculations.	0x00000000	R/W
0x02F	BWATTOS	Phase B total active power offset correction for the BWATT calculation.	0x00000000	R/W
0x030	BVAROS	Phase B total reactive power offset correction for the BVAR calculation.	0x00000000	R/W
0x031	BFWATTOS	Phase B fundamental active power offset correction for the BFWATT calculation.	0x00000000	R/W
0x032	BFVAROS	Phase B fundamental reactive power offset correction for the BFVAR calculation.	0x00000000	R/W

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x033	BIFRMSOS	Phase B current rms offset for the fundamental current rms BIFRMS calculation.	0x00000000	R/W
0x034	BVFRMSOS	Phase B voltage rms offset for the fundamental voltage rms BVFRMS calculation.	0x00000000	R/W
0x035	BVRMSONEOS	Phase B voltage rms offset for the fast RMS½ BVRMSONE calculation.	0x00000000	R/W
0x036	BIRMSONEOS	Phase B current rms offset for the fast RMS½ BIRMSONE calculation.	0x00000000	R/W
0x037	BVRMS1012OS	Phase B voltage rms offset for the 10 cycle rms/12 cycle rms BVRMS1012 calculation.	0x00000000	R/W
0x038	BIRMS1012OS	Phase B current rms offset for the 10 cycle rms/12 cycle rms BVRMS1012 calculation.	0x00000000	R/W
0x040	CIGAIN	Phase C current gain adjust.	0x00000000	R/W
0x041	CIGAIN0	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x042	CIGAIN1	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x043	CIGAIN2	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x044	CIGAIN3	Phase C Multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x045	CIGAIN4	Phase C Multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x046	CPHCAL0	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x047	CPHCAL1	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x048	CPHCAL2	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x049	CPHCAL3	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x04A	CPHCAL4	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x00000000	R/W
0x04B	CVGAIN	Phase C voltage gain adjust.	0x00000000	R/W
0x04C	CIRMSOS	Phase C current rms offset for the CIRMS calculation.	0x00000000	R/W
0x04D	CVRMSOS	Phase C voltage rms offset for the CVRMS calculation.	0x00000000	R/W
0x04E	CPGAIN	Phase C power gain adjust for the CWATT, CVA, CVAR, CFWATT, CFVA, and CFVAR calculations.	0x00000000	R/W
0x04F	CWATTOS	Phase C total active power offset correction for the CWATT calculation.	0x00000000	R/W

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x050	CVAROS	Phase C total reactive power offset correction for the CVAR calculation.	0x00000000	R/W
0x051	CFWATTOS	Phase C fundamental active power offset correction for the CFWATT calculation.	0x00000000	R/W
0x052	CFVAROS	Phase C fundamental reactive power offset correction for the CFVAR calculation.	0x00000000	R/W
0x053	CIFRMSOS	Phase C current rms offset for the fundamental current rms CIFRMS calculation.	0x00000000	R/W
0x054	CVFRMSOS	Phase C voltage rms offset for the fundamental voltage rms CVFRMS calculation.	0x00000000	R/W
0x055	CVRMSONEOS	Phase C voltage rms offset for the fast RMS½ CVRMSONE calculation.	0x00000000	R/W
0x056	CIRMSONEOS	Phase C current rms offset for the fast RMS½ CIRMSONE calculation.	0x00000000	R/W
0x057	CVRMS1012OS	Phase C voltage rms offset for the 10 cycle rms/12 cycle rms CVRMS1012 calculation.	0x00000000	R/W
0x058	CIRMS1012OS	Phase C current rms offset for the 10 cycle rms/12 cycle rms CIRMS1012 calculation.	0x00000000	R/W
0x060	CONFIG0	Configuration Register 0.	0x00000000	R/W
0x061	MTTHR_L0	Multipoint phase/gain threshold. If MTEN = 1 in the CONFIG0 register, the MTGNTHR_Lx and MTGNTHR_Hx registers set up the ranges in which to apply each set of corrections, allowing hysteresis. See the Multipoint Phase/Gain Calibration section for more information.	0x00000000	R/W
0x062	MTTHR_L1	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x063	MTTHR_L2	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x064	MTTHR_L3	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x065	MTTHR_L4	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x066	MTTHR_H0	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x067	MTTHR_H1	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x068	MTTHR_H2	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x069	MTTHR_H3	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x06A	MTTHR_H4	Multipoint phase/gain threshold. See MTTHR_L0 for more information.	0x00000000	R/W
0x06B	NIRMSOS	Neutral current rms offset for the NIRMS calculation.	0x00000000	R/W
0x06C	ISUMRMSOS	Offset correction for the ISUMRMS calculation based on the sum of IA + IB + IC ± IN.	0x00000000	R/W
0x06D	NIGAIN	Neutral current gain adjust.	0x00000000	R/W
0x06E	NPHCAL	Neutral current phase compensation.	0x00000000	R/W
0x06F	NIRMSONEOS	Neutral current rms offset for the fast RMS½ NIRMSONE calculation.	0x00000000	R/W
0x070	NIRMS1012OS	Neutral current rms offset for the 10 cycle rms/12 cycle rms NIRMS1012 calculation.	0x00000000	R/W
0x071	VNOM	Nominal phase voltage rms used in the computation of apparent power, xVA, when the VNOMx_EN bit is set in the CONFIG0 register.	0x00000000	R/W
0x072	DICOEFF	Value used in the digital integrator algorithm. If the integrator is turned on, with INTEN or ININTEN equal to one in the CONFIG0 register, it is recommended to set this value to 0xFFFFE000.	0x00000000	R/W
0x073	ISUMLVL	Threshold to compare ISUMRMS against. Configure this register to receive a MISMTCH indication in STATUS0 if ISUMRMS exceeds this threshold.	0x00000000	R/W
0x20A	AI_PCF	Instantaneous Phase A current channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x20B	AV_PCF	Instantaneous Phase A voltage channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x20C	AIRMS	Phase A filter-based current rms value, updates at 8 kSPS.	0x00000000	R
0x20D	AVRMS	Phase A filter-based voltage rms value, updates at 8 kSPS.	0x00000000	R
0x20E	AIFRMS	Phase A current fundamental rms, updates at 8 kSPS.	0x00000000	R
0x20F	AVFRMS	Phase A voltage fundamental RMS, updates at 8 kSPS.	0x00000000	R
0x210	AWATT	Phase A low-pass filtered total active power, updated at 8 kSPS.	0x00000000	R
0x211	AVAR	Phase A low-pass filtered total reactive power, updated at 8 kSPS.	0x00000000	R
0x212	AVA	Phase A total apparent power, updated at 8 kSPS.	0x00000000	R
0x213	AFWATT	Phase A fundamental active power, updated at 8 kSPS.	0x00000000	R
0x214	AFVAR	Phase A fundamental reactive power, updated at 8 kSPS.	0x00000000	R
0x215	AFVA	Phase A fundamental apparent power, updated at 8 kSPS.	0x00000000	R
0x216	APF	Phase A power factor, updated every 1.024 sec.	0x00000000	R
0x217	AVTHD	Phase A voltage THD, updated every 1.024 sec.	0x00000000	R

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x218	AITHD	Phase A current THD, updated every 1.024 sec.	0x00000000	R
0x219	AIRMSONE	Phase A current fast RMS½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x21A	AVRMSONE	Phase A voltage fast RMS½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x21B	AIRMS1012	Phase A current fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x21C	AVRMS1012	Phase A voltage fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x21D	AMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, this register indicate which AIGAINx and APHCALx is currently being used.	0x0000000F	R
0x22A	BI_PCF	Instantaneous Phase B current channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x22B	BV_PCF	Instantaneous Phase B voltage channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x22C	BIRMS	Phase B filter-based current rms value, updates at 8 kSPS.	0x00000000	R
0x22D	BVRMS	Phase B filter-based voltage rms value, updates at 8 kSPS.	0x00000000	R
0x22E	BIFRMS	Phase B current fundamental rms, updates at 8 kSPS.	0x00000000	R
0x22F	BVFRMS	Phase B voltage fundamental rms, updates at 8 kSPS.	0x00000000	R
0x230	BWATT	Phase B low-pass filtered total active power, updated at 8 kSPS.	0x00000000	R
0x231	BVAR	Phase B low-pass filtered total reactive power, updated at 8 kSPS.	0x00000000	R
0x232	BVA	Phase B total apparent power, updated at 8 kSPS.	0x00000000	R
0x233	BFWATT	Phase B fundamental active power, updated at 8 kSPS.	0x00000000	R
0x234	BFVAR	Phase B fundamental reactive power, updated at 8 kSPS.	0x00000000	R
0x235	BFVA	Phase B fundamental apparent power, updated at 8 kSPS.	0x00000000	R
0x236	BPF	Phase B power factor, updated every 1.024 sec.	0x00000000	R
0x237	BVTHD	Phase B voltage THD, updated every 1.024 sec.	0x00000000	R
0x238	BITHD	Phase B current THD, updated every 1.024 sec.	0x00000000	R
0x239	BIRMSONE	Phase B current fast RMS½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x23A	BVRMSONE	Phase B voltage fast RMS½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x23B	BIRMS1012	Phase B current fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x23C	BVRMS1012	Phase B voltage fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x23D	BMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the COFIG0 register, this register indicate which BIGAINx and BPHCALx is currently being used.	0x0000000F	R
0x24A	CI_PCF	Instantaneous Phase C current channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x24B	CV_PCF	Instantaneous Phase C voltage channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x24C	CIRMS	Phase C filter-based current rms value, updates at 8 kSPS.	0x00000000	R
0x24D	CVRMS	Phase C filter-based voltage rms value, updates at 8 kSPS.	0x00000000	R
0x24E	CIFRMS	Phase C current fundamental rms, updates at 8 kSPS.	0x00000000	R
0x24F	CVFRMS	Phase C voltage fundamental rms, updates at 8 kSPS.	0x00000000	R
0x250	CWATT	Phase C low-pass filtered total active power, updated at 8 kSPS.	0x00000000	R
0x251	CVAR	Phase C low-pass filtered total reactive power, updated at 8 kSPS.	0x00000000	R
0x252	CVA	Phase C total apparent power, updated at 8 kSPS.	0x00000000	R
0x253	CFWATT	Phase C fundamental active power, updated at 8 kSPS.	0x00000000	R
0x254	CFVAR	Phase C fundamental reactive power, updated at 8 kSPS.	0x00000000	R
0x255	CFVA	Phase C fundamental apparent power, updated at 8 kSPS.	0x00000000	R
0x256	CPF	Phase C power factor, updated every 1.024 sec.	0x00000000	R

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Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x257	CVTHD	Phase C voltage THD, updated every 1.024 sec.	0x00000000	R
0x258	CITHD	Phase C current total THD, updated every 1.024 sec.	0x00000000	R
0x259	CIRMSONE	Phase C current fast RMS½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x25A	CVRMSONE	Phase C voltage fast RMS½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x25B	CIRMS1012	Phase C current fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x25C	CVRMS1012	Phase C voltage fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x25D	CMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which CIGAINx and CPHCALx is currently being used.	0x0000000F	R
0x265	NI_PCF	Instantaneous neutral current channel waveform processed by the DSP at 8 kSPS.	0x00000000	R
0x266	NIRMS	Neutral current filter-based rms value.	0x00000000	R
0x267	NIRMSONE	Neutral current fast RMS½ calculation, one cycle rms updated every half cycle.	0x00000000	R
0x268	NIRMS1012	Neutral current fast 10 cycle rms/12 cycle rms calculation. The calculation is performed over 10 cycles if SELFREQ = 0 for a 50 Hz network or over 12 cycles if SELFREQ = 1 for a 60 Hz network, in the ACCMODE register.	0x00000000	R
0x269	ISUMRMS	Filter-based rms based on the sum of IA + IB + IC ± IN.	0x00000000	R
0x26A	VERSION2	This register indicates the version of the metrology algorithms after the user writes run = 1 to start the measurements.	0x0000000C	R
0x2E4	AWATT_ACC_LO	Phase A accumulated total active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2E5	AWATT_ACC_HI	Phase A accumulated total active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2E6	AWATTHR_LO	Phase A accumulated total active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x2E7	AWATTHR_HI	Phase A accumulated total active energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0X2EE	AVAR_ACC_LO	Phase A accumulated total reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2EF	AVAR_ACC_HI	Phase A accumulated total reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2F0	AVARHR_LO	Phase A accumulated total reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x2F1	AVARHR_HI	Phase A accumulated total reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x2F8	AVA_ACC_LO	Phase A accumulated total apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2F9	AVA_ACC_HI	Phase A accumulated total apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x2FA	AVAHR_LO	Phase A accumulated total apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x2FB	AVAHR_HI	Phase A accumulated total apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x302	AFWATT_ACC_LO	Phase A accumulated fundamental active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x303	AFWATT_ACC_HI	Phase A accumulated fundamental active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x304	AFWATTHR_LO	Phase A accumulated fundamental active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x305	AFWATTHR_HI	Phase A accumulated fundamental active energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x30C	AFVAR_ACC_LO	Phase A accumulated fundamental reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x30D	AFVAR_ACC_HI	Phase A accumulated fundamental reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x30E	AFVARHR_LO	Phase A accumulated fundamental reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x30F	AFVARHR_HI	Phase A accumulated fundamental reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x316	AFVA_ACC_LO	Phase A accumulated fundamental apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x317	AFVA_ACC_HI	Phase A accumulated fundamental apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x318	AFVAHR_LO	Phase A accumulated fundamental apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x319	AFVAHR_HI	Phase A accumulated fundamental apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0X320	BWATT_ACC_LO	Phase B accumulated total active power, LSB.Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x321	BWATT_ACC_HI	Phase B accumulated total active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x322	BWATTHR_LO	Phase B accumulated total active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x323	BWATTHR_HI	Phase B accumulated total active energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0X32A	BVAR_ACC_LO	Phase B accumulated total reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x0000000	R
0x32B	BVAR_ACC_HI	Phase B accumulated total reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x32C	BVARHR_LO	Phase B accumulated total reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x32D	BVARHR_HI	Phase B accumulated total reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0X334	BVA_ACC_LO	Phase B accumulated total apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x335	BVA_ACC_HI	Phase B accumulated total apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x336	BVAHR_LO	Phase B accumulated total apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x337	BVAHR_HI	Phase B accumulated total apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x33E	BFWATT_ACC_LO	Phase B accumulated fundamental active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x33F	BFWATT_ACC_HI	Phase B accumulated fundamental active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x340	BFWATTHR_LO	Phase B accumulated fundamental active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x341	BFWATTHR_HI	Phase B accumulated fundamental active energy, MSB. Updated according to the settings in EP_CFG and EGY_TIME registers.	0x00000000	R
0x348	BFVAR_ACC_LO	Phase B accumulated fundamental reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x349	BFVAR_ACC_HI	Phase B accumulated fundamental reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x34A	BFVARHR_LO	Phase B accumulated fundamental reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x34B	BFVARHR_HI	Phase B accumulated fundamental reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x352	BFVA_ACC_LO	Phase B accumulated fundamental apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x353	BFVA_ACC_HI	Phase B accumulated fundamental apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x354	BFVAHR_LO	Phase B accumulated fundamental apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x355	BFVAHR_HI	Phase B accumulated fundamental apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x35C	CWATT_ACC_LO	Phase C accumulated total active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x35D	CWATT_ACC_HI	Phase C accumulated total active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x35E	CWATTHR_LO	Phase C accumulated total active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x35F	CWATTHR_HI	Phase C accumulated total active energy, MSB. Updated according to the settings in the P_CFG and EGY_TIME registers.	0x00000000	R
0x366	CVAR_ACC_LO	Phase C accumulated total reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x367	CVAR_ACC_HI	Phase C accumulated total reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x368	CVARHR_LO	Phase C accumulated total reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x369	CVARHR_HI	Phase C accumulated total reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x370	CVA_ACC_LO	Phase C accumulated total apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x371	CVA_ACC_HI	Phase C accumulated total apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x372	CVAHR_LO	Phase C accumulated total apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x373	CVAHR_HI	Phase C accumulated total apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x37A	CFWATT_ACC_LO	Phase C accumulated fundamental active power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x37B	CFWATT_ACC_HI	Phase C accumulated fundamental active power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x37C	CFWATTHR_LO	Phase C accumulated fundamental active energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x37D	CFWATTHR_HI	Phase C accumulated fundamental active energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x384	CFVAR_ACC_LO	Phase C accumulated fundamental reactive power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x385	CFVAR_ACC_HI	Phase C accumulated fundamental reactive power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x386	CFVARHR_LO	Phase C accumulated fundamental reactive energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x387	CFVARHR_HI	Phase C accumulated fundamental reactive energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x38E	CFVA_ACC_LO	Phase C accumulated fundamental apparent power, LSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x38F	CFVA_ACC_HI	Phase C accumulated fundamental apparent power, MSB. Updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x390	CFVAHR_LO	Phase C accumulated fundamental apparent energy, LSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x391	CFVAHR_HI	Phase C accumulated fundamental apparent energy, MSB. Updated according to the settings in the EP_CFG and EGY_TIME registers.	0x00000000	R
0x396	PWATT_ACC_LO	Accumulated positive total active power, LSB, from AWATT, BWATT, and CWATT registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x397	PWATT_ACC_HI	Accumulated positive total active power, MSB, from AWATT, BWATT, and CWATT registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x39A	NWATT_ACC_LO	Accumulated Negative total active power, LSB, from AWATT, BWATT, and CWATT registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x39B	NWATT_ACC_HI	Accumulated Negative total active power, MSB, from AWATT, BWATT, and CWATT registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x39E	PVAR_ACC_LO	Accumulated positive total reactive power, LSB, from AVAR, BVAR, and CVAR registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x39F	PVAR_ACC_HI	Accumulated positive total reactive power, MSB, from AVAR, BVAR, and CVAR registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x3A2	NVAR_ACC_LO	Accumulated Negative total reactive power, LSB, from AVAR, BVAR, and CVAR registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x3A3	NVAR_ACC_HI	Accumulated Negative total reactive power, MSB, from AVAR, BVAR, and CVAR registers, updated after PWR_TIME 8 kSPS samples.	0x00000000	R
0x400	IPEAK	Current peak register.	0x00000000	R
0x401	VPEAK	Voltage peak register.	0x00000000	R
0x402	STATUS0	Status Register 0.	0x00000000	R/W
0x403	STATUS1	Status Register 1.	0x00000000	R/W
0x404	EVENT_STATUS	Event status register.	0x00000000	R
0x405	MASK0	Interrupt Enable Register 0.	0x00000000	R/W
0x406	MASK1	Interrupt Enable Register 1.	0x00000000	R/W
0x407	EVENT_MASK	Event enable register.	0x00000000	R/W
0x409	OILVL	Over current detection threshold level.	0x00FFFFFF	R/W
0x40A	OIA	Phase A overcurrent RMS½ value. If a phase is enabled, with the OC_ENA bit set in the CONFIG3 register and AIRMSONE greater than the OILVL threshold, this value is updated.	0x00000000	R
0x40B	OIB	Phase B overcurrent RMS½ value. If a phase is enabled, with the OC_ENB bit set in the CONFIG3 register and BIRMSONE greater than the OILVL threshold, this value is updated.	0x00000000	R
0x40C	OIC	Phase C overcurrent RMS½ value. If a phase is enabled, with the OC_ENC bit set in the CONFIG3 register and CIRMSONE greater than the OILVL threshold, this value is updated.	0x00000000	R
0x40D	OIN	Neutral current overcurrent RMS½ value. If enabled, with the OC_ENN bit set in the CONFIG3 register and NIRMSONE greater than the OILVL threshold, this value is updated.	0x00000000	R
0x40E	USER_PERIOD	User configured line period value used for resampling, fast RMS½ and 10 cycle rms/ 12 cycle rms when the UPERIOD_SEL bit in the CONFIG2 register is set.	0x00500000	R/W
0x40F	VLEVEL	Register used in the algorithm that computes the fundamental active, reactive, and apparent powers as well as the fundamental IRMS and VRMS values.	0x00045D45	R/W
0x410	DIP_LVL	Voltage RMS½ dip detection threshold level.	0x00000000	R/W
0x411	DIPA	Phase A voltage RMS½ value during a dip condition.	0x007FFFFF	R
0x412	DIPB	Phase B voltage RMS½ value during a dip condition.	0x007FFFFF	R
0x413	DIPC	Phase C voltage RMS½ value during a dip condition.	0x007FFFFF	R
0x414	SWELL_LVL	Voltage RMS½ swell detection threshold level.	0x00FFFFFF	R/W
0x415	SWELLA	Phase A voltage RMS½ value during a swell condition.	0x00000000	R
0x416	SWELLB	Phase B voltage RMS½ value during a swell condition.	0x00000000	R
0x417	SWELLC	Phase C voltage RMS½ value during a swell condition.	0x00000000	R
0x418	APERIOD	Line period on Phase A voltage.	0x00A00000	R
0x419	BPERIOD	Line period on Phase B voltage.	0x00A00000	R
0x41A	CPERIOD	Line period on Phase C voltage.	0x00A00000	R
0x41B	COM_PERIOD	Line period measurement on combined signal from Phase A, Phase B, and Phase C voltages.	0x00A00000	R
0x41C	ACT_NL_LVL	No load threshold in the total and fundamental active power datapath.	0x0000FFFF	R/W
0x41D	REACT_NL_LVL	No load threshold in the total and fundamental reactive power datapath.	0x0000FFFF	R/W
0x41E	APP_NL_LVL	No load threshold in the total and fundamental apparent power datapath.	0x0000FFFF	R/W
0x41F	PHNOLOAD	Phase no load register.	0x00000000	R
0x420	WTHR	Sets the maximum output rate from the digital to frequency converter for the total and fundamental active power for the CFx calibration pulse output. It is recommended to write WTHR = 0x0010_0000.	0x0000FFFF	R/W

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x421	VARTHR	Sets the maximum output rate from the digital to frequency converter for the total and fundamental reactive power for the CFx calibration pulse output. It is recommended to write VARTHR = 0x0010_0000.	0x0000FFFF	R/W
0x422	VATHR	Sets the maximum output rate from the digital to frequency converter for the total and fundamental apparent power for the CFx calibration pulse output. It is recommended to write VATHR = 0x0010_0000.	0x0000FFFF	R/W
0x423	LAST_DATA_32	This register holds the data read or written during the last 32-bit transaction on the SPI port.	0x00000000	R
0x424	ADC_REDIRECT	This register allows any ADC output to be redirected to any digital datapath.	0x001FFFFF	R/W
0x425	CF_LCFG	CFx calibration pulse width configuration register.	0x00000000	R/W
0x472	PART_ID	This register identifies the IC. If the ADE9000_ID bit = 1, the IC is the ADE9000.	0xXX1XXXXX[2]	R
0x474	TEMP_TRIM	Temperature sensor gain and offset, calculated during the manufacturing process.	0xXXXXXXXX	R
0x480	RUN	Write this register to 1 to start the measurements.	0x0000	R/W
0x481	CONFIG1	Configuration Register 1.	0x0000	R/W
0x482	ANGL_VA_VB	Time between positive to negative zero-crossings on Phase A and Phase B voltages.	0x0000	R
0x483	ANGL_VB_VC	Time between positive to negative zero-crossings on Phase B and Phase C voltages.	0x0000	R
0x484	ANGL_VA_VC	Time between positive to negative zero-crossings on Phase A and Phase C voltages.	0x0000	R
0x485	ANGL_VA_IA	Time between positive to negative zero-crossings on Phase A voltage and current.	0x0000	R
0x486	ANGL_VB_IB	Time between positive to negative zero-crossings on Phase B voltage and current.	0x0000	R
0x487	ANGL_VC_IC	Time between positive to negative zero-crossings on Phase C voltage and current.	0x0000	R
0x488	ANGL_IA_IB	Time between positive to negative zero-crossings on Phase A and Phase B current.	0x0000	R
0x489	ANGL_IB_IC	Time between positive to negative zero-crossings on Phase B and Phase C current.	0x0000	R
0x48A	ANGL_IA_IC	Time between positive to negative zero-crossings on Phase A and Phase C current.	0x0000	R
0x48B	DIP_CYC	Voltage RMS½ dip detection cycle configuration.	0xFFFF	R/W
0x48C	SWELL_CYC	Voltage RMS½ swell detection cycle configuration.	0xFFFF	R/W
0x48F	OISTATUS	Overcurrent status register.	0x0000	R
0x490	CFMODE	CFx configuration register.	0x0000	R/W
0x491	COMPMODE	Computation mode register.	0x0000	R/W
0x492	ACCMODE	Accumulation mode register.	0x0000	R/W
0x493	CONFIG3	Configuration Register 3.	0xF000	R/W
0x494	CF1DEN	CF1 denominator register.	0xFFFF	R/W
0x495	CF2DEN	CF2 denominator register.	0xFFFF	R/W
0x496	CF3DEN	CF3 denominator register.	0xFFFF	R/W
0x497	CF4DEN	CF4 denominator register.	0xFFFF	R/W
0x498	ZXTOUT	Zero-crossing timeout configuration register.	0xFFFF	R/W
0x499	ZXTHRSH	Voltage channel zero-crossing threshold register.	0x0009	R/W
0x49A	ZX_LP_SEL	This register selects which zero-crossing and which line period measurement are used for other calculations.	0x001E	R/W
0x49C	SEQ_CYC	Number of line cycles used for phase sequence detection. It is recommended to set this register to 1.	0x00FF	R/W
0x49D	PHSIGN	Power sign register.	0x0000	R
0x4A0	WFB_CFG	Waveform buffer configuration register.	0x0000	R/W
0x4A1	WFB_PG_IRQEN	This register enables interrupts to occur after specific pages of the waveform buffer are filled.	0x0000	R/W
0x4A2	WFB_TRG_CFG	This register enables events to trigger a capture in the waveform buffer.	0x0000	R/W
0x4A3	WFB_TRG_STAT	This register indicates the last page that was filled in the waveform buffer and the location of trigger events.	0x0000	R/W
0x4A8	CRC_RSLT	This register holds the CRC of the configuration registers.	0x0000	R
0x4A9	CRC_SPI	This register holds the 16-bit CRC of the data sent out on the MOSI pin during the last SPI register read.	0x0000	R
0x4AC	LAST_DATA_16	This register holds the data read or written during the last 16-bit transaction on the SPI port.	0x0000	R

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x4AE	LAST_CMD	This register holds the address and read/write operation request (CMD_HDR) for the last transaction on the SPI port.	0x0000	R
0x4AF	CONFIG2	Configuration Register 2.	0x0C00	R/W
0x4B0	EP_CFG	Energy and power accumulation configuration.	0x0000	R/W
0x4B1	PWR_TIME	Power update time configuration.	0x00FF	R/W
0x4B2	EGY_TIME	Energy accumulation update time configuration.	0x00FF	R/W
0x4B4	CRC_FORCE	This register forces an update of the CRC of configuration registers.	0x0000	R/W
0x4B5	CRC_OPTEN	This register selects which registers are optionally included in the configuration register CRC feature.	0x0000	R/W
0x4B6	TEMP_CFG	Temperature sensor configuration register.	0x0000	R/W
0x4B7	TEMP_RSLT	Temperature measurement result.	0x0000	R
0x4B9	PGA_GAIN	This register configures the PGA gain for each ADC.	0x0000	R/W
0x4BA	CHNL_DIS	ADC channel enable/disable.	0x0000	R/W
0x4BF	WR_LOCK	This register enables the configuration lock feature.	0x0000	R/W
0x4E0	VAR_DIS	Enables/disables total reactive power calculation.	0x0000	R/W
0x4F0	RESERVED1	This register is reserved.	0x0000	R
0x4FE	Version	Version of ADE9000 IC.	0x0040	R
0x500	AI_SINC_DAT	Current channel A ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x501	AV_SINC_DAT	Voltage channel A ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x502	BI_SINC_DAT	Current channel B ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x503	BV_SINC_DAT	Voltage channel B ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x504	CI_SINC_DAT	Current channel C ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x505	CV_SINC_DAT	Voltage channel C ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x506	NI_SINC_DAT	Neutral current channel ADC waveforms from the sinc4 output at 32 kSPS.	0x00000000	R
0x510	AI_LPF_DAT	Current channel A ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x511	AV_LPF_DAT	Voltage channel A ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x512	BI_LPF_DAT	Current channel B ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x513	BV_LPF_DAT	Voltage channel B ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x514	CI_LPF_DAT	Current channel C ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x515	CV_LPF_DAT	Voltage channel C ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x516	NI_LPF_DAT	Neutral current channel ADC waveforms from the sinc4 + IIR LPF output at 8 kSPS.	0x00000000	R
0x600	AV_PCF_1	SPI burst read accessible. Registers organized functionally. See AV_PCF.	0x00000000	R/W
0x601	BV_PCF_1	SPI burst read accessible. Registers organized functionally. See BV_PCF.	0x00000000	R/W
0x602	CV_PCF_1	SPI burst read accessible. Registers organized functionally. See CV_PCF.	0x00000000	R/W
0x603	NI_PCF_1	SPI burst read accessible. Registers organized functionally. See NI_PCF.	0x00000000	R/W
0x604	AI_PCF_1	SPI burst read accessible. Registers organized functionally. See AI_PCF.	0x00000000	R/W
0x605	BI_PCF_1	SPI burst read accessible. Registers organized functionally. See BI_PCF.	0x00000000	R/W
0x606	CI_PCF_1	SPI burst read accessible. Registers organized functionally. See CI_PCF.	0x00000000	R/W
0x607	AIRMS_1	SPI burst read accessible. Registers organized functionally. See AIRMS.	0x00000000	R/W
0x608	BIRMS_1	SPI burst read accessible. Registers organized functionally. See BIRMS.	0x00000000	R/W
0x609	CIRMS_1	SPI burst read accessible. Registers organized functionally. See CIRMS.	0x00000000	R/W
0x60A	AVRMS_1	SPI burst read accessible. Registers organized functionally. See AVRMS.	0x00000000	R/W
0x60B	BVRMS_1	SPI burst read accessible. Registers organized functionally. See BVRMS.	0x00000000	R/W
0x60C	CVRMS_1	SPI burst read accessible. Registers organized functionally. See CVRMS.	0x00000000	R/W
0x60D	NIRMS_1	SPI burst read accessible. Registers organized functionally. See NIRMS.	0x00000000	R/W
0x60E	AWATT_1	SPI burst read accessible. Registers organized functionally. See AWATT.	0x00000000	R/W
0x60F	BWATT_1	SPI burst read accessible. Registers organized functionally. See BWATT.	0x00000000	R/W
0x610	CWATT_1	SPI burst read accessible. Registers organized functionally. See CWATT.	0x00000000	R/W

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x611	AVA_1	SPI burst read accessible. Registers organized functionally. See AVA.	0x00000000	R/W
0x612	BVA_1	SPI burst read accessible. Registers organized functionally. See BVA.	0x00000000	R/W
0x613	CVA_1	SPI burst read accessible. Registers organized functionally. See CVA.	0x00000000	R/W
0x614	AVAR_1	SPI burst read accessible. Registers organized functionally. See AVAR.	0x00000000	R/W
0x615	BVAR_1	SPI burst read accessible. Registers organized functionally. See BVAR.	0x00000000	R/W
0x616	CVAR_1	SPI burst read accessible. Registers organized functionally. See CVAR.	0x00000000	R/W
0x617	AFVAR_1	SPI burst read accessible. Registers organized functionally. See AFVAR.	0x00000000	R/W
0x618	BFVAR_1	SPI burst read accessible. Registers organized functionally. See BFVAR.	0x00000000	R/W
0x619	CFVAR_1	SPI burst read accessible. Registers organized functionally. See CFVAR.	0x00000000	R/W
0x61A	APF_1	SPI burst read accessible. Registers organized functionally. See APF.	0x00000000	R/W
0x61B	BPF_1	SPI burst read accessible. Registers organized functionally. See BPF.	0x00000000	R/W
0x61C	CPF_1	SPI burst read accessible. Registers organized functionally. See CPF.	0x00000000	R/W
0x61D	AVTHD_1	SPI burst read accessible. Registers organized functionally. See AVTHD.	0x00000000	R/W
0x61E	BVTHD_1	SPI burst read accessible. Registers organized functionally. See BVTHD.	0x00000000	R/W
0x61F	CVTHD_1	SPI burst read accessible. Registers organized functionally. See CVTHD.	0x00000000	R/W
0x620	AITHD_1	SPI burst read accessible. Registers organized functionally. See AITHD.	0x00000000	R/W
0x621	BITHD_1	SPI burst read accessible. Registers organized functionally. See BITHD.	0x00000000	R/W
0x622	CITHD_1	SPI burst read accessible. Registers organized functionally. See CITHD.	0x00000000	R/W
0x623	AFWATT_1	SPI burst read accessible. Registers organized functionally. See AFWATT.	0x00000000	R/W
0x624	BFWATT_1	SPI burst read accessible. Registers organized functionally. See BFWATT.	0x00000000	R/W
0x625	CFWATT_1	SPI burst read accessible. Registers organized functionally. See CFWATT.	0x00000000	R/W
0x626	AFVA_1	SPI burst read accessible. Registers organized functionally. See AFVA.	0x00000000	R/W
0x627	BFVA_1	SPI burst read accessible. Registers organized functionally. See BFVA.	0x00000000	R/W
0x628	CFVA_1	SPI burst read accessible. Registers organized functionally. See CFVA.	0x00000000	R/W
0x629	AFIRMS_1	SPI burst read accessible. Registers organized functionally. See AFIRMS.	0x00000000	R/W
0x62A	BFIRMS_1	SPI burst read accessible. Registers organized functionally. See BFIRMS.	0x00000000	R/W
0x62B	CFIRMS_1	SPI burst read accessible. Registers organized functionally. See CFIRMS.	0x00000000	R/W
0x62C	AFVRMS_1	SPI burst read accessible. Registers organized functionally. See AFVRMS.	0x00000000	R/W
0x62D	BFVRMS_1	SPI burst read accessible. Registers organized functionally. See BFVRMS.	0x00000000	R/W
0x62E	CFVRMS_1	SPI burst read accessible. Registers organized functionally. See CFVRMS.	0x00000000	R/W
0x62F	AIRMSONE_1	SPI burst read accessible. Registers organized functionally. See AIRMSONE.	0x00000000	R/W
0x630	BIRMSONE_1	SPI burst read accessible. Registers organized functionally. See BIRMSONE.	0x00000000	R/W
0x631	CIRMSONE_1	SPI burst read accessible. Registers organized functionally. See CIRMSONE.	0x00000000	R/W
0x632	AVRMSONE_1	SPI burst read accessible. Registers organized functionally. See AVRMSONE.	0x00000000	R/W
0x633	BVRMSONE_1	SPI burst read accessible. Registers organized functionally. See BVRMSONE.	0x00000000	R/W
0x634	CVRMSONE_1	SPI burst read accessible. Registers organized functionally. See CVRMSONE.	0x00000000	R/W
0x635	NIRMSONE_1	SPI burst read accessible. Registers organized functionally. See NIRMSONE.	0x00000000	R/W
0x636	AIRMS1012_1	SPI burst read accessible. Registers organized functionally. See AIRMS1012.	0x00000000	R/W
0x637	BIRMS1012_1	SPI burst read accessible. Registers organized functionally. See BIRMS1012.	0x00000000	R/W
0x638	CIRMS1012_1	SPI burst read accessible. Registers organized functionally. See CIRMS1012.	0x00000000	R/W
0x639	AVRMS1012_1	SPI burst read accessible. Registers organized functionally. See AVRMS1012.	0x00000000	R/W
0x63A	BVRMS1012_1	SPI burst read accessible. Registers organized functionally. See BVRMS1012.	0x00000000	R/W
0x63B	CVRMS1012_1	SPI burst read accessible. Registers organized functionally. See CVRMS1012.	0x00000000	R/W
0x63C	NIRMS1012_1	SPI burst read accessible. Registers organized functionally. See NIRMS1012.	0x00000000	R/W
0x680	AV_PCF_2	SPI burst read accessible. Registers organized by phase. See AV_PCF.	0x00000000	R/W
0x681	AI_PCF_2	SPI burst read accessible. Registers organized by phase. See AI_PCF.	0x00000000	R/W
0x682	AIRMS_2	SPI burst read accessible. Registers organized by phase. See AIRMS.	0x00000000	R/W

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x683	AVRMS_2	SPI burst read accessible. Registers organized by phase. See AVRMS.	0x00000000	R/W
0x684	AWATT_2	SPI burst read accessible. Registers organized by phase. See AWATT.	0x00000000	R/W
0x685	AVA_2	SPI burst read accessible. Registers organized by phase. See AVA.	0x00000000	R/W
0x686	AVAR_2	SPI burst read accessible. Registers organized by phase. See AVAR.	0x00000000	R/W
0x687	AFVAR_2	SPI burst read accessible. Registers organized by phase. See AFVAR.	0x00000000	R/W
0x688	APF_2	SPI burst read accessible. Registers organized by phase. See APF.	0x00000000	R/W
0x689	AVTHD_2	SPI burst read accessible. Registers organized by phase. See AVTHD.	0x00000000	R/W
0x68A	AITHD_2	SPI burst read accessible. Registers organized by phase. See AITHD.	0x00000000	R/W
0x68B	AFWATT_2	SPI burst read accessible. Registers organized by phase. See AFWATT.	0x00000000	R/W
0x68C	AFVA_2	SPI burst read accessible. Registers organized by phase. See AFVA.	0x00000000	R/W
0x68D	AFIRMS_2	SPI burst read accessible. Registers organized by phase. See AFIRMS.	0x00000000	R/W
0x68E	AFVRMS_2	SPI burst read accessible. Registers organized by phase. See AFVRMS.	0x00000000	R/W
0x68F	AIRMSONE_2	SPI burst read accessible. Registers organized by phase. See AIRMSONE.	0x00000000	R/W
0x690	AVRMSONE_2	SPI burst read accessible. Registers organized by phase. See AVRMSONE.	0x00000000	R/W
0x691	AIRMS1012_2	SPI burst read accessible. Registers organized by phase. See AIRMS1012.	0x00000000	R/W
0x692	AVRMS1012_2	SPI burst read accessible. Registers organized by phase. See AVRMS1012.	0x00000000	R/W
0x693	BV_PCF_2	SPI burst read accessible. Registers organized by phase. See BV_PCF.	0x00000000	R/W
0x694	BI_PCF_2	SPI burst read accessible. Registers organized by phase. See BI_PCF.	0x00000000	R/W
0x695	BIRMS_2	SPI burst read accessible. Registers organized by phase. See BIRMS.	0x00000000	R/W
0x696	BVRMS_2	SPI burst read accessible. Registers organized by phase. See BVRMS.	0x00000000	R/W
0x697	BWATT_2	SPI burst read accessible. Registers organized by phase. See BWATT.	0x00000000	R/W
0x698	BVA_2	SPI burst read accessible. Registers organized by phase. See BVA.	0x00000000	R/W
0x699	BVAR_2	SPI burst read accessible. Registers organized by phase. See BVAR.	0x00000000	R/W
0x69A	BFVAR_2	SPI burst read accessible. Registers organized by phase. See BFVAR.	0x00000000	R/W
0x69B	BPF_2	SPI burst read accessible. Registers organized by phase. See BPF.	0x00000000	R/W
0x69C	BVTHD_2	SPI burst read accessible. Registers organized by phase. See BVTHD.	0x00000000	R/W
0x69D	BITHD_2	SPI burst read accessible. Registers organized by phase. See BITHD.	0x00000000	R/W
0x69E	BFWATT_2	SPI burst read accessible. Registers organized by phase. See BFWATT.	0x00000000	R/W
0x69F	BFVA_2	SPI burst read accessible. Registers organized by phase. See BFVA.	0x00000000	R/W
0x6A0	BFIRMS_2	SPI burst read accessible. Registers organized by phase. See BFIRMS.	0x00000000	R/W
0x6A1	BFVRMS_2	SPI burst read accessible. Registers organized by phase. See BFVRMS.	0x00000000	R/W
0x6A2	BIRMSONE_2	SPI burst read accessible. Registers organized by phase. See BIRMSONE.	0x00000000	R/W
0x6A3	BVRMSONE_2	SPI burst read accessible. Registers organized by phase. See BVRMSONE.	0x00000000	R/W
0x6A4	BIRMS1012_2	SPI burst read accessible. Registers organized by phase. See BIRMS1012.	0x00000000	R/W
0x6A5	BVRMS1012_2	SPI burst read accessible. Registers organized by phase. See BVRMS1012.	0x00000000	R/W
0x6A6	CV_PCF_2	SPI burst read accessible. Registers organized by phase. See CV_PCF.	0x00000000	R/W
0x6A7	CI_PCF_2	SPI burst read accessible. Registers organized by phase. See CI_PCF.	0x00000000	R/W
0x6A8	CIRMS_2	SPI burst read accessible. Registers organized by phase. See CIRMS.	0x00000000	R/W
0x6A9	CVRMS_2	SPI burst read accessible. Registers organized by phase. See CVRMS.	0x00000000	R/W
0x6AA	CWATT_2	SPI burst read accessible. Registers organized by phase. See CWATT.	0x00000000	R/W
0x6AB	CVA_2	SPI burst read accessible. Registers organized by phase. See CVA.	0x00000000	R/W
0x6AC	CVAR_2	SPI burst read accessible. Registers organized by phase. See CVAR.	0x00000000	R/W
0x6AD	CFVAR_2	SPI burst read accessible. Registers organized by phase. See CFVAR.	0x00000000	R/W
0x6AE	CPF_2	SPI burst read accessible. Registers organized by phase. See CPF.	0x00000000	R/W
0x6AF	CVTHD_2	SPI burst read accessible. Registers organized by phase. See CVTHD.	0x00000000	R/W
0x6B0	CITHD_2	SPI burst read accessible. Registers organized by phase. See CITHD.	0x00000000	R/W
0x6B1	CFWATT_2	SPI burst read accessible. Registers organized by phase. See CFWATT.	0x00000000	R/W

REGISTER INFORMATION

Table 29. Register Summary (Continued)

Address	Name	Description	Reset[1]	Access
0x6B2	CFVA_2	SPI burst read accessible. Registers organized by phase. See CFVA.	0x00000000	R/W
0x6B3	CFIRMS_2	SPI burst read accessible. Registers organized by phase. See CFIRMS.	0x00000000	R/W
0x6B4	CFVRMS_2	SPI burst read accessible. Registers organized by phase. See CFVRMS.	0x00000000	R/W
0x6B5	CIRMSONE_2	SPI burst read accessible. Registers organized by phase. See CIRMSONE.	0x00000000	R/W
0x6B6	CVRMSONE_2	SPI burst read accessible. Registers organized by phase. See CVRMSONE.	0x00000000	R/W
0x6B7	CIRMS1012_2	SPI burst read accessible. Registers organized by phase. See CIRMS1012.	0x00000000	R/W
0x6B8	CVRMS1012_2	SPI burst read accessible. Registers organized by phase. See CVRMS1012.	0x00000000	R/W
0x6B9	NI_PCF_2	SPI burst read accessible. Registers organized by phase. See NI_PCF.	0x00000000	R/W
0x6BA	NIRMS_2	SPI burst read accessible. Registers organized by phase. See NIRMS.	0x00000000	R/W
0x6BB	NIRMSONE_2	SPI burst read accessible. Registers organized by phase. See NIRMSONE.	0x00000000	R/W
0x6BC	NIRMS1012_2	SPI burst read accessible. Registers organized by phase. See NIRMS1012.	0x00000000	R/W

[1] Not valid until run bit is set.

[2] The default value is unique to every individual IC.

REGISTER INFORMATION

REGISTER DETAILS

Table 30 details the registers of the ADE9000 that have bit fields. Additional registers listed in Table 29 do not have bit fields.

Table 30. Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
0x060	CONFIG0	[31:14]	RESERVED		Reserved.	0x0	R
		13	DISRPLPF		Set this bit to disable the low-pass filter in the total reactive power datapath.	0x0	R/W
		12	DISAPLPF		Set this bit to disable the low-pass filter in the total active power datapath.	0x0	R/W
		11	ININTEN		Set this bit to enable the digital integrator in the neutral current channel.	0x0	R/W
		10	VNOMC_EN		Set this bit to use the nominal phase voltage rms, V_{NOM}, in the computation of Phase C total apparent power, CVA.	0x0	R/W
		9	VNOMB_EN		Set this bit to use the nominal phase voltage rms, V_{NOM}, in the computation of Phase B total apparent power, BVA.	0x0	R/W
		8	VNOMA_EN		Set this bit to use the nominal phase voltage rms, V_{NOM}, in the computation of Phase A total apparent power, AVA.	0x0	R/W
		7	RMS_SRC_SEL		This bit selects which samples are used for the RMS½ and 10 cycle rms/12 cycle rms calculation.	0x0	R/W
				0	xI_PCF waveforms, after the high-pass filter and integrator.		
				1	ADC samples, before the high-pass filter and integrator.		
		6	ZX_SRC_SEL		This bit selects whether data going into the zero-crossing detection circuit comes before the high-pass filter, integrator, and phase compensation or afterwards.	0x0	R/W
				0	After the high-pass filter, integrator, and phase compensation.		
				1	Before the high-pass filter, integrator, and phase compensation.		
		5	INTEN		Set this bit to enable the integrators in the phase current channels. The neutral current channel integrator is managed by the ININTEN bit in the CONFIG0 register.	0x0	R/W
		4	MTEN		Set this bit to enable multipoint phase and gain compensation. If enabled, an additional gain factor, xIGAIN0 through xIGAIN5, is applied to the current channel based on the xIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x0	R/W
		3	HPFDIS		Set this bit to disable high-pass filters in all the voltage and current channels.	0x0	R/W
		2	RESERVED		Reserved.	0x0	R
		[1:0]	ISUM_CFG		ISUM calculation configuration.	0x0	R/W
				00	ISUM = AI_PCF + BI_PCF + CI_PCF (for approximated neutral current rms calculation).		
				01	ISUM = AI_PCF + BI_PCF + CI_PCF + NI_PCF (to determine mismatch between neutral and phase currents).		
				10	ISUM = AI_PCF + BI_PCF + CI_PCF − NI_PCF (to determine mismatch between neutral and phase currents).		
				11	ISUM = AI_PCF + BI_PCF + CI_PCF (for approximated neutral current rms calculation).		
0x21D	AMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	AREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which AIGAINx and APHCALx is currently being used	0xF	R
				0000	AIGAIN0, APHCAL0.		

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				0001	AIGAIN1, APHCAL1.		
				0010	AIGAIN2, APHCAL2.		
				0011	AIGAIN3, APHCAL3.		
				0100	AIGAIN4, APHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x23D	BMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	BREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which BIGAINx and BPHCALx is currently being used.	0xF	R
				0000	BIGAIN0, BPHCAL0.		
				0001	BIGAIN1, BPHCAL1.		
				0010	BIGAIN2, BPHCAL2.		
				0011	BIGAIN3, BPHCAL3.		
				0100	BIGAIN4, BPHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x25D	CMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which CIGAINx and CPHCALx is currently being used.	0xF	R
				0000	CIGAIN0, CPHCAL0.		
				0001	CIGAIN1, CPHCAL1.		
				0010	CIGAIN2, CPHCAL2.		
				0011	CIGAIN3, CPHCAL3.		
				0100	CIGAIN4, CPHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x400	IPEAK	[31:27]	RESERVED		Reserved.	0x0	R
		[26:24]	IPPHASE		These bits indicate which phases generate the IPEAKVAL value. Note that the PEAKSEL, Bits[4:2] in the CONFIG3 register determine which current channel to monitor the peak value on. When IPPHASE, Bit 0 is set to 1, Phase A current is generated by the IPEAKVAL, Bits[23:0] value. Similarly, IPPHASE, Bit 1 indicates that the Phase B and IPPHASE, Bit 2 indicates that the Phase C current generated the peak value.	0x0	R
		[23:0]	IPEAKVAL		The IPEAK register stores the signed value of the peak current. IPEAK is equal to xI_PCF/2^5.	0x0	R
0x401	VPEAK	[31:27]	RESERVED		Reserved.	0x0	R
		[26:24]	VPPHASE		These bits indicate which phase(s) generate the VPEAKVAL value. Note that the PEAKSEL, Bits[4:2] in the CONFIG3 register determine which voltage channels to monitor the peak value on. When VPPHASE, Bit 0 is 1, the Phase A voltage generated the VPEAKVAL, Bits[23:0] value. Similarly, VPPHASE, Bit 1 indicates Phase B and VPPHASE, Bit 2 indicates that the Phase C voltage generated the peak value.	0x0	R
		[23:0]	VPEAKVAL		The VPEAK register stores the signed value of the peak voltage. VPEAK is equal to xV_PCF/2^5.	0x0	R
0x402	STATUS0	[31:26]	RESERVED		Reserved.	0x0	R

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		25	TEMP_RDY		This bit goes high to indicate when a new temperature measurement is available.	0x0	R/W
		24	MISMTCH		This bit is set to indicate a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W
		23	COH_WFB_FULL		This bit is set when the waveform buffer is full with resampled data, which is selected when WF_CAP_SEL = 0 in the WFB_CFG register.	0x0	R/W
		22	WFB_TRIG		This bit is set when one of the events configured in WFB_TRG_CFG occurs.	0x0	R/W
		21	THD_PF_RDY		This bit goes high to indicate when the THD and power factor measurements update, every 1.024 sec.	0x0	R/W
		20	RMS1012RDY		This bit is set when the 10 cycle rms/12 cycle rms values update.	0x0	R/W
		19	RMSONERDY		This bit is set when the fast RMS½ values update.	0x0	R/W
		18	PWRRDY		This bit is set when the power values in the xWATT_ACC, xVA_ACC, xVAR_ACC, xFWATT_ACC, xFVA_ACC, and xFVAR_ACC registers update, after PWR_TIME 8 kSPS samples.	0x0	R/W
		17	PAGE_FULL		This bit is set when a page enabled in the WFB_PG_IRQEN register is filled with fixed data rate samples, when WF_CAP_SEL bit in the WFB_CFG register is equal to zero.	0x0	R/W
		16	WFB_TRIG_IRQ		This bit is set when the waveform buffer stops filling after an event configured in WFB_TRG_CFG occurs. This happens with fixed data rate samples only, when WF_CAP_SEL bit in the WFB_CFG register is equal to zero.	0x0	R/W
		15	DREADY		This bit is set when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W
		14	CF4		This bit is set when a CF4 pulse is issued, when the CF4 pin goes from a high to low state.	0x0	R/W
		13	CF3		This bit is set when a CF3 pulse is issued, when the CF3 pin goes from a high to low state.	0x0	R/W
		12	CF2		This bit is set when a CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W
		11	CF1		This bit is set when a CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W
		10	REVPSUM4		This bit is set to indicate if the CF4 polarity changed sign. For example, if the last CF4 pulse was positive reactive energy and the next CF4 pulse is negative reactive energy, the REVPSUM4 bit is set. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R/W
		9	REVPSUM3		This bit is set to indicate if the CF3 polarity changed sign. See REVPSUM4.	0x0	R/W
		8	REVPSUM2		This bit is set to indicate if the CF2 polarity changed sign. See REVPSUM4.	0x0	R/W
		7	REVPSUM1		This bit is set to indicate if the CF1 polarity changed sign. See REVPSUM4.	0x0	R/W
		6	REVRPC		This bit indicates if the Phase C total or fundamental reactive power has changed sign. The PWR_SIGN_SEL bit in the EP_CFG register selects whether total or fundamental reactive power is monitored. This bit is	0x0	R/W

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
					updated when the power values in the xVAR_ACC and xFVAR_ACC registers update, after PWR_TIME 8 kSPS samples.		
		5	REVRPB		This bit indicates if the Phase B total or fundamental reactive power has changed sign. See REVRPC.	0x0	R/W
		4	REVRPA		This bit indicates if the Phase A total or fundamental reactive power has changed sign. See REVRPC.	0x0	R/W
		3	REVAPC		This bit indicates if the Phase C total or fundamental active power has changed sign. The PWR_SIGN_SEL bit in the EP_CFG register selects whether total or fundamental active power is monitored. This bit is updated when the power values in the xWATT_ACC and xFWATT_ACC registers update, after PWR_TIME 8 kSPS samples.	0x0	R/W
		2	REVAPB		This bit indicates if the Phase B total or fundamental active power has changed sign. See REVAPC.	0x0	R/W
		1	REVAPA		This bit indicates if the Phase A total or fundamental active power has changed sign. See REVAPC.	0x0	R/W
		0	EGYRDY		This bit is set when the power values in the xWATTHR, xVAHR, xVARHR, xFVARHR, xFWATTHR, xFVAHR registers update, after EGY_TIME 8 kSPS samples or line cycles, depending on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W
0x403	STATUS1	31	ERROR3		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R/W
		30	ERROR2		This bit indicates that an error was detected and corrected. No action is required.	0x0	R/W
		29	ERROR1		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R
		28	ERROR0		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R
		27	CRC_DONE		This bit is set to indicate when the configuration register CRC calculation is complete, after initiated by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register.	0x0	R/W
		26	CRC_CHG		This bit is set if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W
		25	DIPC		This bit is set to indicates Phase C voltage entered or exited a dip condition.	0x0	R/W
		24	DIPB		This bit is set to indicates Phase B voltage entered or exited a dip condition.	0x0	R/W
		23	DIPA		This bit is set to indicates Phase A voltage entered or exited a dip condition.	0x0	R/W
		22	SWELLC		This bit is set to indicates Phase C voltage entered or exited a swell condition.	0x0	R/W
		21	SWELLB		This bit is set to indicates Phase B voltage entered or exited a swell condition.	0x0	R/W
		20	SWELLA		This bit it set to indicates Phase A voltage entered or exited a swell condition.	0x0	R/W
		19	RESERVED		Reserved.	0x0	R

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		18	SEQERR		This bit is set to indicate a phase sequence error on the Phase voltage zero-crossings.	0x0	R/W
		17	OI		This bit is set to indicate that an overcurrent event occurred on one of the phases indicated in the OISTATUS register.	0x0	R/W
		16	RSTDONE		This bit is set to indicate that the IC finished its power-up sequence after a reset or after changing between PSM3 operating mode to PSM0, which indicates that the user can configure the IC via the SPI port.	0x0	R/W
		15	ZXIC		When this bit is set to 1, it indicates a zero-crossing is detected on Phase C current.	0x0	R/W
		14	ZXIB		When this bit is set to 1, it indicates a zero-crossing is detected on Phase B current.	0x0	R/W
		13	ZXIA		When this bit is set to 1, it indicates a zero-crossing is detected on Phase A current.	0x0	R/W
		12	ZXCOMB		When this bit is set, it indicates a zero-crossing is detected on the combined signal from VA, VB, and VC.	0x0	R/W
		11	ZXVC		When this bit is set, it indicates a zero-crossing is detected on the Phase C voltage channel.	0x0	R/W
		10	ZXVB		When this bit is set, it indicates a zero-crossing is detected on the Phase B voltage channel.	0x0	R/W
		9	ZXVA		When this bit is set, it indicates a zero-crossing is detected on the Phase A voltage channel.	0x0	R/W
		8	ZXTOVC		This bit is set to indicate a zero-crossing timeout on Phase C. This means that a zero-crossing on the Phase C voltage is missing.	0x0	R/W
		7	ZXTOVB		This bit is set to indicate a zero-crossing timeout on Phase B. This means that a zero-crossing on the Phase B voltage is missing.	0x0	R/W
		6	ZXTOVA		This bit is set to indicate a zero-crossing timeout on Phase A. This means that a zero-crossing on the Phase A voltage is missing.	0x0	R/W
		5	VAFNOLOAD		This bit is set when one or more phase fundamental apparent energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		4	RFNOLOAD		This bit is set when one or more phase fundamental reactive energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		3	AFNOLOAD		This bit is set when one or more phase fundamental active energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		2	VANLOAD		This bit is set when one or more phase total apparent energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		1	RNLOAD		This bit is set when one or more phase total reactive energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
		0	ANLOAD		This bit is set when one or more phase total active energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W
0x404	EVENT_STATUS	[31:17]	RESERVED		Reserved.	0x0	R
		16	DREADY		This bit changes from a zero to a one when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		15	VAFNOLOAD		This bit is set when the fundamental apparent energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total apparent energy accumulation goes into no load.	0x0	R
		14	RFNOLOAD		This bit is set when the fundamental reactive energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of fundamental reactive energy accumulation goes into no load.	0x0	R
		13	AFNOLOAD		This bit is set when the fundamental active energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of fundamental active energy accumulation goes into no load.	0x0	R
		12	VANLOAD		This bit is set when the total apparent energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total apparent energy accumulation goes into no load.	0x0	R
		11	RNLOAD		This bit is set when the total reactive energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total reactive energy accumulation goes into no load.	0x0	R
		10	ANLOAD		This bit is set when the total active energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total active energy accumulation goes into no load.	0x0	R
		9	REVPSUM4		This bit indicates the sign of the last CF4 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R
		8	REVPSUM3		This bit indicates the sign of the last CF3 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF3 pulse is output, when the CF3 pin goes from high to low.	0x0	R
		7	REVPSUM2		This bit indicates the sign of the last CF2 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF2 pulse is output, when the CF2 pin goes from high to low.	0x0	R
		6	REVPSUM1		This bit indicates the sign of the last CF1 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF1 pulse is output, when the CF1 pin goes from high to low.	0x0	R
		5	SWELLC		This bit is equal to one when the Phase C voltage is in the swell condition and is zero when it is not in a swell condition.	0x0	R
		4	SWELLB		This bit is equal to one when the Phase B voltage is in the swell condition and is zero when it is not in a swell condition.	0x0	R
		3	SWELLA		This bit is equal to one when the Phase A voltage is in the swell condition and is zero when it is not in a swell condition.	0x0	R

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		2	DIPC		This bit is equal to one when the Phase C voltage is in the dip condition and is zero when it is not in a dip condition.	0x0	R
		1	DIPB		This bit is equal to one when the Phase B voltage is in the dip condition and is zero when it is not in a dip condition	0x0	R
		0	DIPA		This bit is equal to one when the Phase A voltage is in the dip condition and is zero when it is not in a dip condition.	0x0	R
0x405	MASK0	[31:26]	RESERVED		Reserved.	0x0	R
		25	TEMP_RDY_MASK		Set this bit to enable an interrupt when a new temperature measurement is available.	0x0	R/W
		24	MISMTCH		Set this bit to enable an interrupt when there is a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W
		23	COH_WFB_FULL		Set this bit to enable an interrupt when the waveform buffer is full with resampled data, which is selected when WF_CAP_SEL = 0 in the WFB_CFG register.	0x0	R/W
		22	WFB_TRIG		Set this bit to enable an interrupt when one of the events configured in WFB_TRIG_CFG occurs.	0x0	R/W
		21	THD_PF_RDY		Set this bit to enable an interrupt when the THD and power factor measurements are updated, every 1.024 sec.	0x0	R/W
		20	RMS1012RDY		Set this bit to enable an interrupt when the 10 cycle rms/12 cycle rms values are updated.	0x0	R/W
		19	RMSONERDY		Set this bit to enable an interrupt when the fast RMS½ values are updated.	0x0	R/W
		18	PWRRDY		Set this bit to enable an interrupt when the power values in the xWATT_ACC, xVA_ACC, xVAR_ACC, xFWATT_ACC, xFVA_ACC, and xFVAR_ACC registers update, after PWR_TIME 8 kSPS samples.	0x0	R/W
		17	PAGE_FULL		Set this bit to enable an interrupt when a page enabled in the WFB_PG_IRQEN register is filled.	0x0	R/W
		16	WFB_TRIG_IRQ		Set this bit to enable an interrupt when This bit is set when the waveform buffer has stopped filling after an event configured in WFB_TRIG_CFG occurs.	0x0	R/W
		15	DREADY		Set this bit to enable an interrupt when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W
		14	CF4		Set this bit to enable an interrupt when the CF4 pulse is issued, when the CF4 pin goes from a high to low state.	0x0	R/W
		13	CF3		Set this bit to enable an interrupt when the CF3 pulse is issued, when the CF3 pin goes from a high to low state.	0x0	R/W
		12	CF2		Set this bit to enable an interrupt when the CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W
		11	CF1		Set this bit to enable an interrupt when the CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W
		10	REVPSUM4		Set this bit to enable an interrupt when the CF4 polarity changed sign.	0x0	R/W
		9	REVPSUM3		Set this bit to enable an interrupt when the CF3 polarity changed sign.	0x0	R/W
		8	REVPSUM2		Set this bit to enable an interrupt when the CF2 polarity changed sign.	0x0	R/W
		7	REVPSUM1		Set this bit to enable an interrupt when the CF1 polarity changed sign.	0x0	R/W
		6	REVRPC		Set this bit to enable an interrupt when the Phase C total or fundamental reactive power has changed sign.	0x0	R/W

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		5	REVRPB		Set this bit to enable an interrupt when the Phase C total or fundamental reactive power has changed sign.	0x0	R/W
		4	REVRPA		Set this bit to enable an interrupt when the Phase A total or fundamental reactive power has changed sign.	0x0	R/W
		3	REVAPC		Set this bit to enable an interrupt when the Phase C total or fundamental active power has changed sign.	0x0	R/W
		2	REVAPB		Set this bit to enable an interrupt when the Phase B total or fundamental active power has changed sign.	0x0	R/W
		1	REVAPA		Set this bit to enable an interrupt when the Phase A total or fundamental active power has changed sign.	0x0	R/W
		0	EGYRDY		Set this bit to enable an interrupt when the power values in the xWATTHR, xVAHR, xVARHR, xFWATTHR, xFVAHR, and xFVARHR registers update, after EGY_TIME 8 kSPS samples or line cycles, depending on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W
0x406	MASK1	31	ERROR3		Set this bit to enable an interrupt if ERROR3 occurs. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		30	ERROR2		Set this bit to enable an interrupt if ERROR2 occurs.	0x0	R/W
		29	ERROR1		This interrupt is not maskable. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		28	ERROR0		This interrupt is not maskable. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		27	CRC_DONE		Set this bit to enable an interrupt when the configuration register CRC calculation is complete, after initiated by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register.	0x0	R/W
		26	CRC_CHG		Set this bit to enable an interrupt if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W
		25	DIPC		Set this bit to enable an interrupt when the Phase C voltage enters a dip condition	0x0	R/W
		24	DIPB		Set this bit to enable an interrupt when the Phase B voltage enters a dip condition.	0x0	R/W
		23	DIPA		Set this bit to enable an interrupt when the Phase A voltage enters a dip condition.	0x0	R/W
		22	SWELLC		Set this bit to enable an interrupt when the Phase C voltage enters a swell condition.	0x0	R/W
		21	SWELLB		Set this bit to enable an interrupt when the Phase B voltage enters a swell condition.	0x0	R/W
		20	SWELLA		Set this bit to enable an interrupt when the Phase A voltage enters a swell condition.	0x0	R/W
		19	RESERVED		Reserved.	0x0	R
		18	SEQERR		Set this bit to enable an interrupt when on a phase sequence error on the phase voltage zero-crossings.	0x0	R/W
		17	OI		Set this bit to enable an interrupt when one of the currents enabled in the OC_EN bits in the CONFIG3 register enters an overcurrent condition.	0x0	R/W
		16	RESERVED		Reserved.	0x0	R
		15	ZXIC		Set this bit to enable an interrupt when a zero-crossing is detected on the Phase C current channel.	0x0	R/W

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		14	ZXIB		Set this bit to enable an interrupt when a zero-crossing is detected on the Phase B current channel.	0x0	R/W
		13	ZXIA		Set this bit to enable an interrupt when a zero-crossing is detected on the Phase A current channel.	0x0	R/W
		12	ZXCOMB		Set this bit to enable an interrupt when a zero-crossing is detected on the combined signal from VA, VB, and VC.	0x0	R/W
		11	ZXVC		Set this bit to enable an interrupt when a zero-crossing is detected on the Phase C voltage channel.	0x0	R/W
		10	ZXVB		Set this bit to enable an interrupt when a zero-crossing is detected on the Phase B voltage channel.	0x0	R/W
		9	ZXVA		Set this bit to enable an interrupt when a zero-crossing is detected on the Phase A voltage channel.	0x0	R/W
		8	ZXTOVC		Set this bit to enable an interrupt when there is a zero-crossing timeout on Phase C. This means that a zero-crossing on the Phase C voltage is missing.	0x0	R/W
		7	ZXTOVB		Set this bit to enable an interrupt when there is a zero-crossing timeout on Phase B. This means that a zero-crossing on the Phase B voltage is missing.	0x0	R/W
		6	ZXTOVA		Set this bit to enable an interrupt when there is a zero-crossing timeout on Phase A. This means that a zero-crossing on the Phase A voltage is missing.	0x0	R/W
		5	VAFNOLOAD		Set this bit to enable an interrupt when one or more phase fundamental apparent energy enters or exits the no load condition.	0x0	R/W
		4	RFNOLOAD		Set this bit to enable an interrupt when one or more phase total reactive energy enters or exits the no load condition.	0x0	R/W
		3	AFNOLOAD		Set this bit to enable an interrupt when one or more phase fundamental active energy enters or exits the no load condition.	0x0	R/W
		2	VANLOAD		Set this bit to enable an interrupt when one or more phase total apparent energy enters or exits the no load condition.	0x0	R/W
		1	RNLOAD		Set this bit to enable an interrupt when one or more phase total reactive energy enters or exits the no load condition.	0x0	R/W
		0	ANLOAD		Set this bit to enable an interrupt when one or more phase total active energy enters or exits the no load condition.	0x0	R/W
0x407	EVENT_MASK	[31:17]	RESERVED		Reserved.	0x0	R
		16	DREADY		Set this bit to enable the EVENT pin to go low when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W
		15	VAFNOLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of fundamental apparent energy accumulation goes into no load.	0x0	R/W
		14	RFNOLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of fundamental reactive energy accumulation goes into no load.	0x0	R/W
		13	AFNOLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of fundamental active energy accumulation goes into no load.	0x0	R/W
		12	VANLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of total apparent energy accumulation goes into no load.	0x0	R/W

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		11	RNLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of total reactive energy accumulation goes into no load.	0x0	R/W
		10	ANLOAD		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low when one or more phases of total active energy accumulation goes into no load.	0x0	R/W
		9	REVPSUM4		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate if the last CF4 pulse was from negative energy. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R/W
		8	REVPSUM3		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate if the last CF3 pulse was from negative energy. This bit is updated when a CF3 pulse is output, when the CF3 pin goes from high to low.	0x0	R/W
		7	REVPSUM2		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate if the last CF2 pulse was from negative energy. This bit is updated when a CF2 pulse is output, when the CF2 pin goes from high to low.	0x0	R/W
		6	REVPSUM1		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate if the last CF1 pulse was from negative energy. This bit is updated when a CF1 pulse is output, when the CF1 pin goes from high to low.	0x0	R/W
		5	SWELLCEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase C voltage is in a swell condition.	0x0	R/W
		4	SWELLBEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase B voltage is in a swell condition.	0x0	R/W
		3	SWELLAEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase A voltage is in a swell condition.	0x0	R/W
		2	DIPCEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase C voltage is in a dip condition.	0x0	R/W
		1	DIPBEN		Set this bit to enable the $\overline{\text{EVENT}}$ pin to go low to indicate that the Phase B voltage is in a dip condition.	0x0	R/W
		0	DIPAEN		Set this bit to enable the EVENT pin to go low to indicate that the Phase A voltage is in a dip condition.	0x0	R/W
0x409	OILVL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OILVL_VAL		Over current detection threshold level.	0xFFFFFF	R/W
0x40A	OIA	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OI_VAL		Phase A overcurrent RMS½ value. If a phase is enabled, with the OC_ENA bit set in the CONFIG3 register and AIRMSONE greater than the OILVL threshold, this value is updated.	0x0	R
0x40B	OIB	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OIB_VAL		Phase B overcurrent RMS½ value. If a phase is enabled, with the OC_ENB bit set in the CONFIG3 register and BIRMSONE greater than the OILVL threshold, this value is updated.	0x0	R
0x40C	OIC	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	OIC_VAL		Phase C overcurrent RMS½ value. If a phase is enabled, with the OC_ENC bit set in the CONFIG3 register and CIRMSONE greater than the OILVL threshold, this value is updated.	0x0	R
0x40D	OIN	[31:24]	RESERVED		Reserved.	0x0	R

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Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		[23:0]	OIN_VAL		Neutral current overcurrent RMS½ value. If enabled, with the OC_ENN bit set in the CONFIG3 register and NIRMSONE greater than the OILVL threshold, this value is updated.	0x0	R
0x40F	VLEVEL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	VLEVEL_VAL		Register used in the algorithm that computes the fundamental active, reactive, and apparent powers, as well as the fundamental IRMS and VRMS values.	0x45D45	R/W
0x410	DIP_LVL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	DIPLVL		Voltage RMS½ dip detection threshold level.	0x0	R/W
0x411	DIPA	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	DIPA_VAL		Phase A voltage RMS½ value during a dip condition.	0x7FFFFF	R
0x412	DIPB	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	DIPB_VAL		Phase B voltage RMS½ value during a dip condition.	0x7FFFFF	R
0x413	DIPC	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	DIPC_VAL		Phase C voltage RMS½ value during a dip condition.	0x7FFFFF	R
0x414	SWELL_LVL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	SWELLLVL		Voltage RMS½ swell detection threshold level.	0xFFFFFF	R/W
0x415	SWELLA	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	SWELLA_VAL		Phase A voltage RMS½ value during a swell condition.	0x0	R
0x416	SWELLB	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	SWELLB_VAL		Phase B voltage RMS½ value during a swell condition.	0x0	R
0x417	SWELLC	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	SWELLC_VAL		Phase C voltage RMS½ value during a swell condition.	0x0	R
0x41F	PHNOLOAD	[31:18]	RESERVED		Reserved.	0x0	R
		17	CFVANL		This bit is set if the Phase C fundamental apparent energy is in no load.	0x0	R
		16	CFVARNL		This bit is set if the Phase C fundamental reactive energy is in no load.	0x0	R
		15	CFWATTNL		This bit is set if the Phase C fundamental active energy is in no load.	0x0	R
		14	CVANL		This bit is set if the Phase C total apparent energy is in no load.	0x0	R
		13	CVARNL		This bit is set if the Phase B total reactive energy is in no load.	0x0	R
		12	CWATTNL		This bit is set if the Phase C total active energy is in no load.	0x0	R
		11	BFVANL		This bit is set if the Phase B fundamental apparent energy is in no load.	0x0	R
		10	BFVARNL		This bit is set if the Phase B fundamental reactive energy is in no load.	0x0	R
		9	BFWATTNL		This bit is set if the Phase B fundamental active energy is in no load.	0x0	R
		8	BVANL		This bit is set if the Phase B total apparent energy is in no load.	0x0	R
		7	BVARNL		This bit is set if the Phase B total reactive energy is in no load.	0x0	R
		6	BWATTNL		This bit is set if the Phase B total active energy is in no load.	0x0	R

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Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		5	AFVANL		This bit is set if the Phase A fundamental apparent energy is in no load.	0x0	R
		4	AFVARNL		This bit is set if the Phase A fundamental reactive energy is in no load.	0x0	R
		3	AFWATTNL		This bit is set if the Phase A fundamental active energy is in no load.	0x0	R
		2	AVANL		This bit is set if the Phase A total apparent energy is in no load.	0x0	R
		1	AVARNL		This bit is set if the Phase A total reactive energy is in no load.	0x0	R
		0	AWATTNL		This bit is set if the Phase A total active energy is in no load.	0x0	R
0x424	ADC_REDIRECT	[31:21]	RESERVED		Reserved.	0x0	R
		[20:18]	VC_DIN		VC channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				000	IA ADC data.		
				001	IB ADC data.		
				010	IC ADC data.		
				011	IN ADC data.		
				100	VA ADC data.		
				101	VB ADC data.		
				110	VC ADC data.		
				111	VC ADC data.		
		[17:15]	VB_DIN		VB channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	VB ADC data.		
		[14:12]	VA_DIN		VA channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	VA ADC data.		
		[11:9]	IN_DIN		IN channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	IN ADC data.		
		[8:6]	IC_DIN		IC channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	IC ADC data.		
		[5:3]	IB_DIN		IB channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	IB ADC data.		
		[2:0]	IA_DIN		IA channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then	0x7	R/W
				111	IA ADC data.		
0x425	CF_LCFG	[31:23]	RESERVED		Reserved.	0x0	R
		22	CF4_LT		If this bit is set, the CF4 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, then the	0x0	R/W

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
					active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.		
		21	CF3_LT		If this bit is set, the CF3 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		20	CF2_LT		If this bit is set, the CF2 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		19	CF1_LT		If this bit is set, the CF1 pulse width is determined by the CF_LTMR register value. If this bit is equal to zero, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		[18:0]	CF_LTMR		If the CFx_LT bit in the CF_LCFG register is set, this value determines the active low pulse width of the CFx pulse.	0x0	R/W
0x472	PART_ID	[31:21]	RESERVED		Reserved.	0xX[2]	R
		20	ADE9000_ID		This bit is set to identify an ADE9000 IC.	0x1	R
		[19:0]	RESERVED		Reserved.	0xX	R
0x474	TEMP_TRIM	[31:16]	TEMP_OFFSET		Offset of temperature sensor, calculated during the manufacturing process.	0xX	R
		[15:0]	TEMP_GAIN		Gain of temperature sensor, calculated during the manufacturing process.	0xX	R
0x481	CONFIG1	15	EXT_REF		Set this bit if using an external voltage reference.	0x0	R/W
		[14:13]	RESERVED		Reserved.	0x0	R
		12	IRQ0_ON_IRQ1		Set this bit to combine all the interrupts onto a single interrupt pin, IRQ1, instead of using two pins, IRQ0 and IRQ1. Note that the IRQ0 pin still indicates the enabled IRQ0 events while in this mode and the IRQ1pin indicates both IRQ1 and IRQ0 events.	0x0	R/W
		11	BURST_EN		Set this bit to enable burst read functionality on the registers from Address 0x500 to Address 0x63C or Address 0x680 to Address 0x6BC. Note that this bit disables the CRC being appended to SPI register reads.	0x0	R/W
		10	DIP_SWELL_IRQ_MODE		Set interrupt mode for dip/swell.	0x0	R/W
				0	Receive continuous interrupts after every DIP_CYC/ SWELL_CYC cycles.		
				1	Receive one interrupt when entering dip/swell mode and another interrupt when exiting dip/swell mode.		
		[9:8]	PWR_SETTLE		These bits configure the time for the power and filter-based rms measurements to settle before starting the power, energy, and CF accumulations. 0: 64 ms. 1: 128 ms. 2: 256 ms. 3: 0 ms.	0x0	R/W
		[7:6]	RESERVED		Reserved.	0x0	R
		5	CF_ACC_CLR		Set this bit to clear the accumulation in the digital to frequency converter and the CFDEN counter. Note that this bit automatically clears itself.	0x0	W
		4	RESERVED		Reserved.	0x0	R
		[3:2]	CF4_CFG		These bits select which function to output on the CF4 pin.	0x0	R/W

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				00	CF4, from digital to frequency converter.		
				01	CF4, from digital to frequency converter.		
				10	$\overline{\text{EVENT}}$.		
				11	DREADY.		
		1	CF3_CFG		This bit selects which function to output on the CF3 pin.	0x0	R/W
				0	CF3, from digital to frequency converter.		
				1	Zero-crossing output selected by the ZX_SEL bits in the ZX_LP_SEL register.		
		0	SWRST		Set this bit to initiate a software reset. Note that this bit is self clearing.	0x0	W
0x48F	OISTATUS	[15:4]	RESERVED		Reserved.	0x0	R
		[3:0]	OIPHASE		OIPHASE, Bit 0 indicates Phase A is above OILVL. OIPHASE, Bit 1 indicates Phase B is above OILVL. OIPHASE, Bit 2 indicates Phase C is above OILVL. OIPHASE, Bit 3 indicates Phase N is above OILVL.	0x0	R
0x490	CFMODE	15	CF4DIS		CF4 output disable. Set this bit to disable the CF4 output and bring the pin high. Note that when this bit is set, the CFx bit in STATUS0 is not set when a CF pulse is accumulated in the digital to frequency converter.	0x0	R/W
		14	CF3DIS		CF3 output disable. See CF4DIS.	0x0	R/W
		13	CF2DIS		CF2 output disable. See CF4DIS.	0x0	R/W
		12	CF1DIS		CF1 output disable. See CF4DIS	0x0	R/W
		[11:9]	CF4SEL		Type of energy output on the CF4 pin. Configure TERMSEL4 in the COMPMODE register to select which phases are included.	0x0	R/W
				000	Total active power.		
				001	Total reactive power.		
				010	Total apparent power.		
				011	Fundamental active power.		
				100	Fundamental reactive power.		
				101	Fundamental apparent power.		
				110	Total active power.		
				111	Total active power.		
		[8:6]	CF3SEL		Selects type of energy output on CF3 pin. See CF4SEL.	0x0	R/W
		[5:3]	CF2SEL		Selects type of energy output on CF2 pin. See CF4SEL.	0x0	R/W
		[2:0]	CF1SEL		Selects type of energy output on CF1 pin. See CF4SEL.	0x0	R/W
0x491	COMPMODE	[15:12]	RESERVED		Reserved.	0x0	R
		[11:9]	TERMSEL4		Phases to include in CF4 pulse output. Set TERMSEL4, Bit 2 to 1 to include Phase C in the CF4 pulse output. Similarly, set TERMSEL4, Bit 1 to include Phase B, and TERMSEL4, Bit 0 for Phase A.	0x0	R/W
		[8:6]	TERMSEL3		Phases to include in CF3 pulse output. See TERMSEL4.	0x0	R/W
		[5:3]	TERMSEL2		Phases to include in CF2 pulse output. See TERMSEL4.	0x0	R/W
		[2:0]	TERMSEL1		Phases to include in CF1 pulse output. See TERMSEL4.	0x0	R/W
0x492	ACCMODE	[15:9]	RESERVED		Reserved.	0x0	R
		8	SELFREQ		Use this bit to configure the IC for a 50 Hz or 60 Hz system. This setting is used in the fundamental power measurements and to set the default line period used for VRMS½, 10 cycle rms/12 cycle rms and resampling calculations if a zero-crossing is not present.	0x0	R/W

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				0	50 Hz.		
				1	60 Hz.		
		7	ICONSEL		Set this bit to calculate the current flowing through IB from the IA and IC measurements. If this bit is set, IB = −IA − IC.	0x0	R/W
		[6:4]	VCONSEL		3-wire and 4-wire hardware configuration selection.	0x0	R/W
				000	4-wire wye.		
				001	3-wire delta. VB' = VA − VC.		
				010	4-wire wye, nonBlondel compliant. VB' = −VA − VC.		
				011	4-wire delta, nonBlondel compliant. VB' = −VA.		
				100	3-wire delta. VA' = VA − VB; VB' = VA − VC; VC' = VC − VB.		
		[3:2]	VARACC		Total and fundamental reactive power accumulation mode for energy registers and CFx pulses.	0x0	R/W
				00	Signed accumulation mode.		
				01	Absolute value accumulation mode.		
				10	Positive accumulation mode.		
				11	Negative accumulation mode.		
		[1:0]	WATTACC		Total and fundamental active power accumulation mode for energy registers and CFx pulses. See VARACC.	0x0	R/W
0x493	CONFIG3	[15:12]	OC_EN		Overcurrent detection enable. OC_EN[3:0] bits can all be set to 1 simultaneously to allow overcurrent detection on all three phases and/or neutral simultaneously. Bit 12. When OC_EN[3] is set to 1, the neutral line is selected for the overcurrent detection. Bit 13. When OC_EN[2] is set to 1, Phase C is selected for the overcurrent detection. Bit 14. When OC_EN[1] is set to 1, Phase B is selected for the overcurrent detection. Bit 15. When OC_EN[0] is set to 1, Phase A is selected for the overcurrent detection.	0xF	R/W
		[11:5]	RESERVED		Reserved.	0x0	R
		[4:2]	PEAKSEL		Set this bit to select which phase(s) to monitor peak voltages and currents on. Write 1 to PEAKSEL, Bit 0 to enable Phase A peak detection. Similarly, PEAKSEL, Bit 1 enables Phase B peak detection, and PEAKSEL, Bit 2 enables Phase C peak detection.	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R
0x49A	ZX_LP_SEL	[15:5]	RESERVED		Reserved.	0x0	R
		[4:3]	LP_SEL		Selects line period measurement used for VRMS½ cycle, 10 cycle rms/12 cycle rms, and resampling.	0x3	R/W
				00	APERIOD, line period measurement from Phase A voltage.		
				01	BPERIOD, line period measurement from Phase B voltage.		
				10	CPERIOD, line period measurement from Phase C voltage.		
				11	COM_PERIOD, line period measurement on combined signal from VA, VB, and VC.		
		[2:1]	ZX_SEL		Selects the zero-crossing signal, which can be routed to the CF3/ZX output pin and used for line cycle energy accumulation.	0x3	R/W
				00	ZXVA, Phase A voltage zero-crossing signal.		
				01	ZXVB, Phase B voltage zero-crossing signal.		
				10	ZXVC, Phase C voltage zero-crossing signal.		

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				11	ZXCOMB, zero-crossing on combined signal from VA, VB, and VC.		
		0	RESERVED		Reserved.	0x0	R
0x49D	PHSIGN	[15:10]	RESERVED		Reserved.	0x0	R
		9	SUM4SIGN		Sign of the sum of the powers included in the CF4 datapath. The CF4 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		8	SUM3SIGN		Sign of the sum of the powers included in the CF3 datapath. The CF3 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		7	SUM2SIGN		Sign of the sum of the powers included in the CF2 datapath. The CF2 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		6	SUM1SIGN		Sign of the sum of the powers included in the CF1 datapath. The CF1 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		5	CVARSIGN		Phase C reactive power sign bit. The PWR_SIGN_ SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R
		4	CWSIGN		Phase C active power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental active power.	0x0	R
		3	BVARSIGN		Phase B reactive power sign bit. The PWR_SIGN_ SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R
		2	BWSIGN		Phase B active power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental active power.	0x0	R
		1	AVARSIGN		Phase A reactive power sign bit. The PWR_SIGN_ SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R
		0	AWSIGN		Phase A active power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental active power.	0x0	R
0x4A0	WFB_CFG	[15:13]	RESERVED		Reserved.	0x0	R
		12	WF_IN_EN		This setting determines whether the IN waveform samples are read out of the waveform buffer through the SPI.	0x0	R/W
				0	IN waveform samples are not read out of waveform buffer through the SPI.		
				1	IN waveform samples are read out of waveform buffer through the SPI.		
		[11:10]	RESERVED		Reserved.	0x0	R
		[9:8]	WF_SRC		Waveform buffer source and DREADY (data ready update rate) selection.	0x0	R/W
				00	Sinc4 output at 32 kSPS.		
				01	Reserved.		
				10	Sinc4 + IIR LPF output at 8 kSPS.		
				11	Current and voltage channel waveform samples, processed by the DSP (xI_PCF, xV_PCF) at 8 kSPS.		
		[7:6]	WF_MODE		Fixed data rate waveforms filling and trigger based modes.	0x0	R/W
				00	Stop when waveform buffer is full.		
				01	Continuous fill—stop only on enabled trigger events.		

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				10	Continuous filling—center capture around enabled trigger events.		
				11	Continuous fill—save event address of enabled trigger events.		
		5	WF_CAP_SEL		This bit selects whether the waveform buffer is filled with resampled data or fixed data rate data, selected in the WF_CAP_SEL bits.	0x0	R/W
				0	Resampled data.		
				1	Fixed data rate data.		
		4	WF_CAP_EN		When this bit is set, a waveform capture is started.	0x0	R/W
				0	The waveform capture is disabled. The waveform buffer contents are maintained.		
				1	The waveform capture is started, according to the type of capture in WF_CAP_SEL and the WF_SRC bits when this bit goes from a 0 to a 1.		
		[3:0]	BURST_CHAN		Selects which data to read out of the waveform buffer through SPI.	0x0	R/W
				0000	All channels.		
				0001	IA and VA.		
				0010	IB and VB.		
				0011	IC and VC.		
				1000	IA.		
				1001	VA.		
				1010	IB.		
				1011	VB.		
				1100	IC.		
				1101	VC.		
				1110	IN if WF_IN_EN = 1 in the WFB_CFG register.		
				1111	Single address read (SPI burst read mode is disabled).		
0x4A2	WFB_TRG_CFG	[15:11]	RESERVED		Reserved.	0x0	R
		10	TRIG_FORCE		Set this bit to trigger an event to stop the waveform buffer filling.	0x0	R/W
		9	ZXCOMB		Zero-crossing on combined signal from VA, VB, and VC.	0x0	R/W
		8	ZXVC		Phase C voltage zero-crossing.	0x0	R/W
		7	ZXVB		Phase B voltage zero-crossing.	0x0	R/W
		6	ZXVA		Phase A voltage zero-crossing.	0x0	R/W
		5	ZXIC		Phase C current zero-crossing.	0x0	R/W
		4	ZXIB		Phase B current zero-crossing.	0x0	R/W
		3	ZXIA		Phase A current zero-crossing.	0x0	R/W
		2	OI		Over current event in any phase.	0x0	R/W
		1	SWELL		Swell event in any phase.	0x0	R/W
		0	DIP		Dip event in any phase.	0x0	R/W
0x4A3	WFB_TRG_STAT	[15:12]	WFB_LAST_PAGE		These bits indicate which page of the waveform buffer was filled last, when filling with fixed rate data samples.	0x0	R/W
		11	RESERVED		Reserved.	0x0	R
		[10:0]	WFB_TRIG_ADDR		These bits hold the address of the last sample put into the waveform buffer after a trigger event occurred, which is within a sample or two of when the actual trigger event occurred.	0x0	R
0x4AF	CONFIG2	[15:13]	RESERVED		Reserved.	0x0	R

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
		12	UPERIOD_SEL		Set this bit to use a user configured line period, in USER_PERIOD, for the VRMS½, 10 cycle rms/12 cycle rms and resampling calculation. If this bit is clear, the phase voltage line period selected by the LP_SEL[1:0] bits in the ZX_LP_SEL register is used.	0x0	R/W
		[11:9]	HPF_CRN		High-pass filter corner (f_{3dB}) enabled when the HPFDIS bit in the CONFIG0 register is equal to zero.	0x6	R/W
				000	77.39 Hz.		
				001	39.275 Hz.		
				010	19.79 Hz.		
				011	9.935 Hz.		
				100	4.98 Hz.		
				101	2.495 Hz.		
				110	1.25 Hz.		
				111	0.625 Hz.		
		[8:0]	RESERVED		Reserved.	0x0	R
0x4B0	EP_CFG	[15:13]	NOLOAD_TMR		This register configures how many 8 kSPS samples to evaluate the no load condition over.	0x0	R/W
				000	64 samples.		
				001	128 samples.		
				010	256 samples.		
				011	512 samples.		
				100	1024 samples.		
				101	2048 samples.		
				110	4096 samples.		
				111	Disable no load threshold.		
		[12:8]	RESERVED		Reserved.	0x0	R
		7	PWR_SIGN_SEL[1]		Selects whether the REVRPx bit follows the sign of the total or fundamental reactive power.	0x0	R/W
				0	Total reactive power.		
				1	Fundamental reactive power.		
		6	PWR_SIGN_SEL[0]		Selects whether the REVAPx bit follows the sign of the total or fundamental active power.	0x0	R/W
				0	Total active power.		
				1	Fundamental active power.		
		5	RD_RST_EN		Set this bit to enable the energy register read with reset feature. If this bit is set, when one of the xWATTHR, xVAHR, xVARH, xFWATTHR, xFVAHR, and xFVARHR register is read, it is reset and begins accumulating energy from zero.	0x0	R/W
		4	EGY_LD_ACCUM		If this bit is equal to zero, the internal energy register is added to the user accessible energy register. If the bit is set, the internal energy register overwrites the user accessible energy register when the EGYRDY event occurs.	0x0	R/W
		[3:2]	RESERVED		Reserved.	0x0	R
		1	EGY_TMR_MODE		This bit determines whether energy is accumulated based on the number of 8 kSPS samples or zero-crossing events configured in the EGY_TIME register.	0x0	R/W
				0	Accumulate energy based on 8 kSPS samples.		

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				1	Accumulate energy based on the zero-crossing selected by the ZX_SEL bits in the ZX_LP_SEL register.		
		0	EGY_PWR_EN		Set this bit to enable the energy and power accumulator, when the run bit is also set.	0x0	R/W
0x4B4	CRC_FORCE	[15:1]	RESERVED		Reserved.	0x0	R
		0	FORCE_CRC_UPDATE		Write this bit to force the configuration register CRC calculation to start. When the calculation is complete, the CRC_DONE bit is set in the STATUS1 register.	0x0	R/W
0x4B5	CRC_OPTEN	15	CRC_WFB_TRG_CFG_EN		Set this bit to include the WFB_TRG_CFG register in the configuration register CRC calculation.	0x0	R/W
		14	CRC_WFB_PG_IRQEN		Set this bit to include the WFB_PG_IRQEN register in the configuration register CRC calculation.	0x0	R/W
		13	CRC_WFB_CFG_EN		Set this bit to include the WFB_CFG register in the configuration register CRC calculation.	0x0	R/W
		12	CRC_SEQ_CYC_EN		Set this bit to include the SEQ_CYC register in the configuration register CRC calculation.	0x0	R/W
		11	CRC_ZXLPSEL_EN		Set this bit to include the ZX_LP_SEL register in the configuration register CRC calculation.	0x0	R/W
		10	CRC_ZXTOUT_EN		Set this bit to include the CRC_ZXTOUT_EN register in the configuration register CRC calculation.	0x0	R/W
		9	CRC_APP_NL_LVL_EN		Set this bit to include the APP_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		8	CRC_REACT_NL_LVL_EN		Set this bit to include the REACT_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		7	CRC_ACT_NL_LVL_EN		Set this bit to include the ACT_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		6	CRC_SWELL_CYC_EN		Set this bit to include the SWELL_CYC register in the configuration register CRC calculation.	0x0	R/W
		5	CRC_SWELL_LVL_EN		Set this bit to include the SWELL_LVL register in the configuration register CRC calculation.	0x0	R/W
		4	CRC_DIP_CYC_EN		Set this bit to include the DIP_CYC register in the configuration register CRC calculation.	0x0	R/W
		3	CRC_DIP_LVL_EN		Set this bit to include the DIP_LVL register in the configuration register CRC calculation.	0x0	R/W
		2	CRC_EVENT_MASK_EN		Set this bit to include the EVENT_MASK register in the configuration register CRC calculation.	0x0	R/W
		1	CRC_MASK1_EN		Set this bit to include the MASK1 register in the configuration register CRC calculation.	0x0	R/W
		0	CRC_MASK0_EN		Set this bit to include the MASK0 register in the configuration register CRC calculation.	0x0	R/W
0x4B6	TEMP_CFG	[15:4]	RESERVED		Reserved.	0x0	R
		3	TEMP_START		Set this bit to request a temperature sensor reading. The new temperature reading is available in 1.25 ms, indicated by the TEMP_RDY bit in the STATUS0 register. Note that this bit is self clearing.	0x0	W
		2	TEMP_EN		Set this bit to enable the temperature sensor.	0x0	R/W
		[1:0]	TEMP_TIME		Select the number of temperature readings to average.	0x0	R/W
				0	1 sample. New temperature measurement every 1.25 ms.		
				1	256 samples. New temperature measurement every 320 ms.		
				10	512 samples. New temperature measurement every 640 ms.		

REGISTER INFORMATION

Table 30. Register Details (Continued)

Addr.	Name	Bits	Bit Name	Settings	Description	Reset[1]	Access
				11	1024 samples. New temperature measurement every 1.3 sec.		
0x4B7	TEMP_RSLT	[15:12]	RESERVED		Reserved.	0x0	R
		[11:0]	TEMP_RESULT		12-bit temperature sensor result.	0x0	R
0x4B9	PGA_GAIN	[15:14]	RESERVED		Reserved.	0x0	R
		[13:12]	VC_GAIN		PGA gain for voltage Channel C ADC.	0x0	R/W
				00	Gain = 1.		
				01	Gain = 2.		
				10	Gain = 4.		
				11	Gain = 4.		
		[11:10]	VB_GAIN		PGA gain for Voltage Channel B ADC. See VC_GAIN.	0x0	R/W
		[9:8]	VA_GAIN		PGA gain for Voltage Channel A ADC. See VC_GAIN.	0x0	R/W
		[7:6]	IN_GAIN		PGA gain for neutral current channel ADC. See VC_GAIN.	0x0	R/W
		[5:4]	IC_GAIN		PGA gain for Current Channel C ADC. See VC_GAIN.	0x0	R/W
		[3:2]	IB_GAIN		PGA gain for Voltage Channel B ADC. See VC_GAIN.	0x0	R/W
		[1:0]	IA_GAIN		PGA gain for Current Channel A ADC. See VC_GAIN.	0x0	R/W
0x4BA	CHNL_DIS	[15:7]	RESERVED		Reserved.	0x0	R
		6	VC_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		5	VB_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		4	VA_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		3	IN_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		2	IC_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		1	IB_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		0	IA_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
0x4E0	VAR_DIS	[15:1]	RESERVED		Reserved.	0x0	R
		0	VARDIS		Set this bit to disable the total VAR calculation. This bit must be set before writing the run bit for proper operation.	0x0	R/W

[1] Not valid until run bit is set.

[2] The default value is unique to every individual IC.