ANALOG DEVICES

Evaluation Board User Guide
UG-064

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AD8099 Evaluation Boards
Offered in 8-Lead SOIC and 8-Lead LFCSP Packages

FEATURES

Enables quick breadboarding/prototyping
User-defined circuit configuration
Edge-mounted SMA connector provisions
Easy connection to test equipment and other circuits
RoHS compliant

INTRODUCTION

The evaluation boards described in this user guide are bare boards (that is, there are no components or amplifier soldered to the board; these must be ordered separately) that enables users to quickly prototype a variety of amplifier circuits, which lowers design time, minimizes risk, and reduces time to market.

The following evaluation boards are designed to work with the AD8099, a high performance externally compensated amplifier. The 8-lead SOIC inverting, 8-lead SOIC noninverting, 8-lead LFCSP inverting, and 8-lead LFCSP noninverting evaluation boards are designed to help users quickly implement and evaluate low noise, low distortion op amp designs.

GENERAL DESCRIPTION

There are two basic AD8099 evaluation board configurations: inverting and noninverting. These two configurations are offered for both package types, LFCSP and SOIC. Part numbers for the evaluation boards can be found in the evaluation board selection guide table in the AD8099 data sheet.

The evaluation boards feature edge-mounted SMA connectors at the input and output for efficient connection to other circuit boards or test equipment. The board is a 2-layer PCB with a ground plane on both sides of the board. The ground plane under the input pins has been removed. Removing the ground plane from under the input pins minimizes the stray capacitance at the input of the op amp, which improves stability and reduces peaking. The evaluation board components are SMTs and range from 0603 to 1206 case size. The electrolytic bypass capacitors are 3528 case size.

Supply bypassing for the AD8099 is a key consideration for optimal circuit performance, especially when distortion is of concern. The AD8099 uses a combination of common-mode bypassing (a capacitor between the two power supplies) and shunt bypassing (from the power supply pins of the amplifier to ground). The evaluation board schematics show the bypassing schemes in detail in Figure 1, Figure 2, Figure 9, and Figure 10.

Because the AD8099 is externally compensated and has a large gain bandwidth product, the component values and placement are critical. The AD8099 data sheet features a detailed section on the compensation networks and component values. In low gain configurations (G = +2), the compensation network consists of three components: a series-parallel combination of resistor and two capacitors to the negative supply.

To minimize stray capacitance, the evaluation board provides only one set of mounting pads for the parallel components. Therefore, the parallel combination of resistor and capacitor (R7 and C_P for the SOIC boards and RC and C_P for the LFCSP boards) must be soldered one on top of the other. Figure 17 illustrates the proper mounting configuration. The previously mentioned reference designators correspond to R_C and C1 found in the AD8099 data sheet.

The AD80999 output does not drive significant values of load capacitance (>5 pF); therefore, the output connections should be kept short, direct, and terminated when appropriate. Larger values of capacitance can be driven by placing a series resistor (25 Ω to 50 Ω) into the R5 position. This helps isolate the capacitive loading effects at the output of the AD8099. Minimizing the output capacitance helps ensure stability while minimizing peaking and ringing.

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REVISION HISTORY

4/11—Rev. 0 to Rev. A

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Changed CSP to LFCSP Throughout 6
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Deleted Table 1; Renumbered Sequentially 9
Added Ordering Information Section and Bill of Materials Section 10
Added Table 1 and Table 2 10

2/10—Revision 0: Initial Version

SOIC EVALUATION BOARD SCHEMATICS

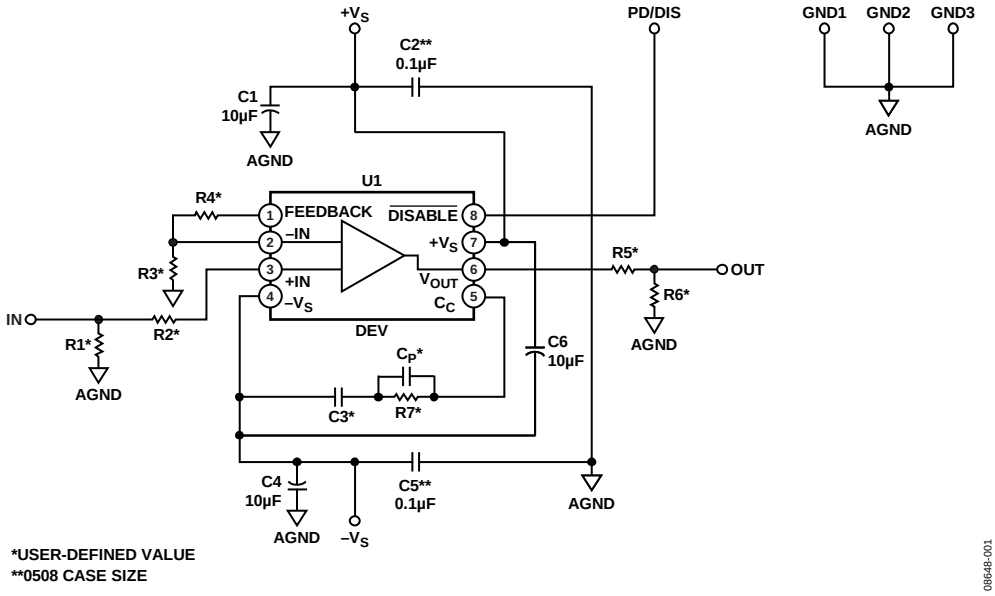


Figure 1. Noninverting Schematic

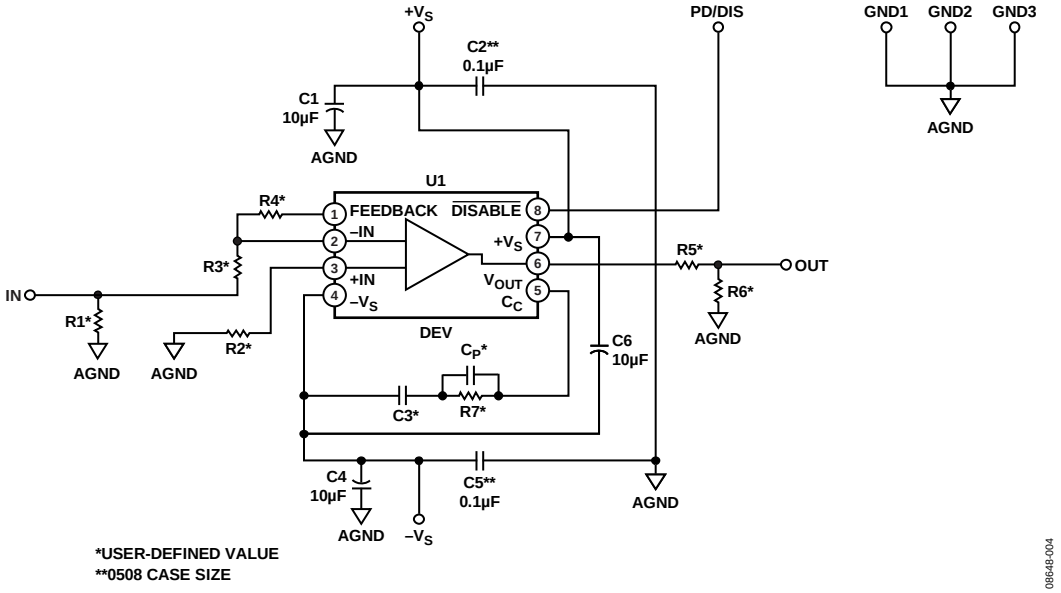
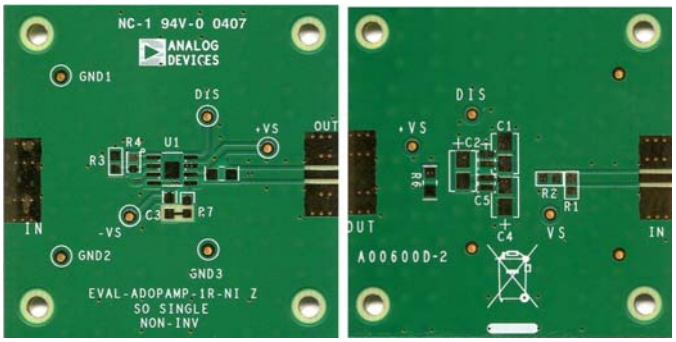


Figure 2. Inverting Schematic

SOIC EVALUATION BOARD, ASSEMBLY, AND LAYOUT DRAWINGS

NONINVERTING



COMPONENT SIDE CIRCUIT SIDE

NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

08648-002

Figure 3. Noninverting Evaluation Board, Component and Circuit Sides

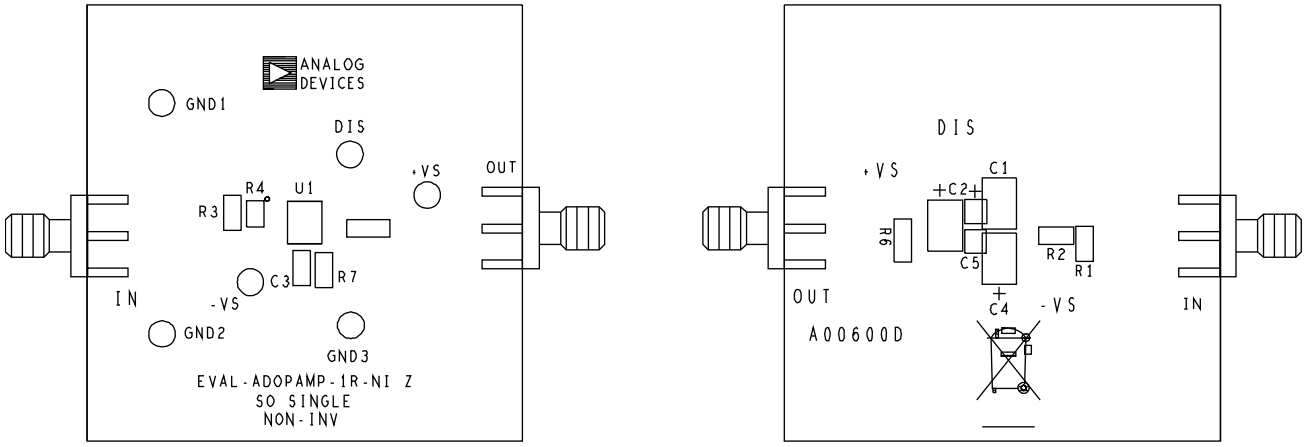


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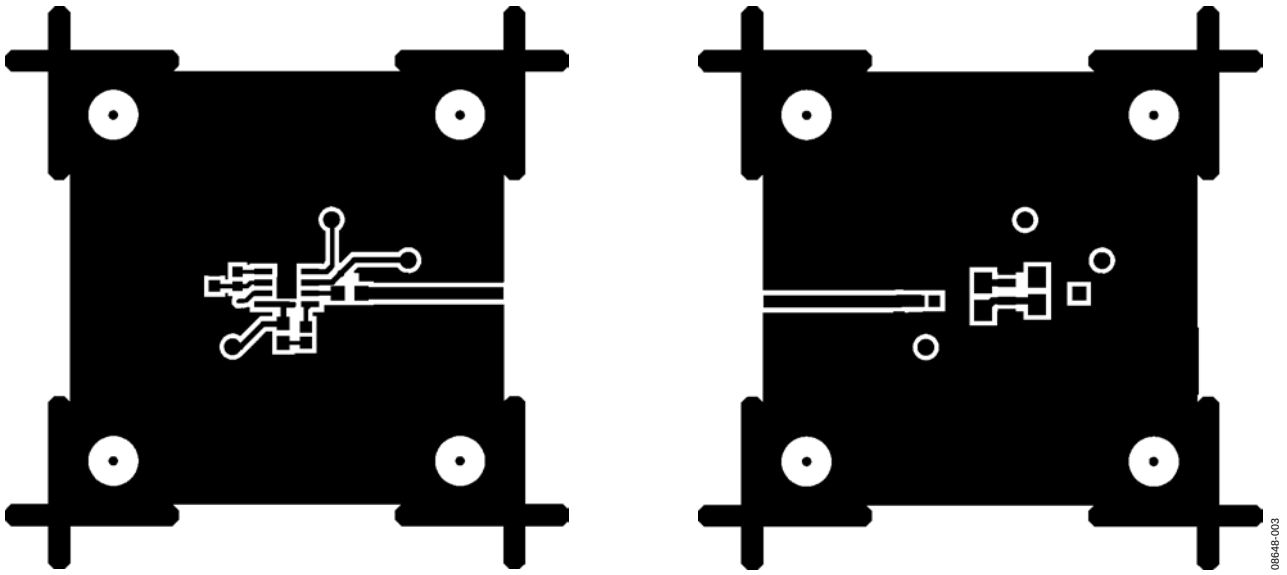
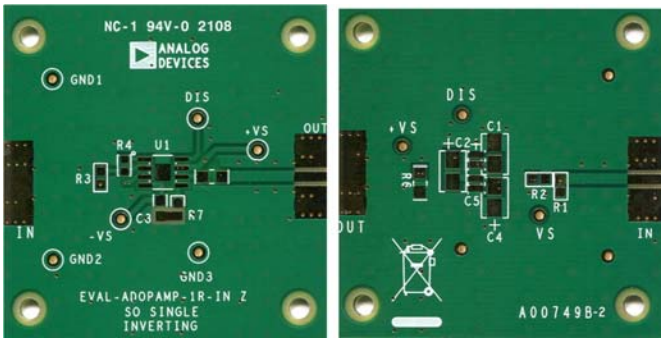
Figure 4. Noninverting Evaluation Board Assembly Drawings



08648-003

Figure 5. Noninverting Evaluation Board Layout Patterns

INVERTING



COMPONENT SIDE CIRCUIT SIDE

NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

08648-005

Figure 6. Inverting Evaluation Board, Component and Circuit Sides

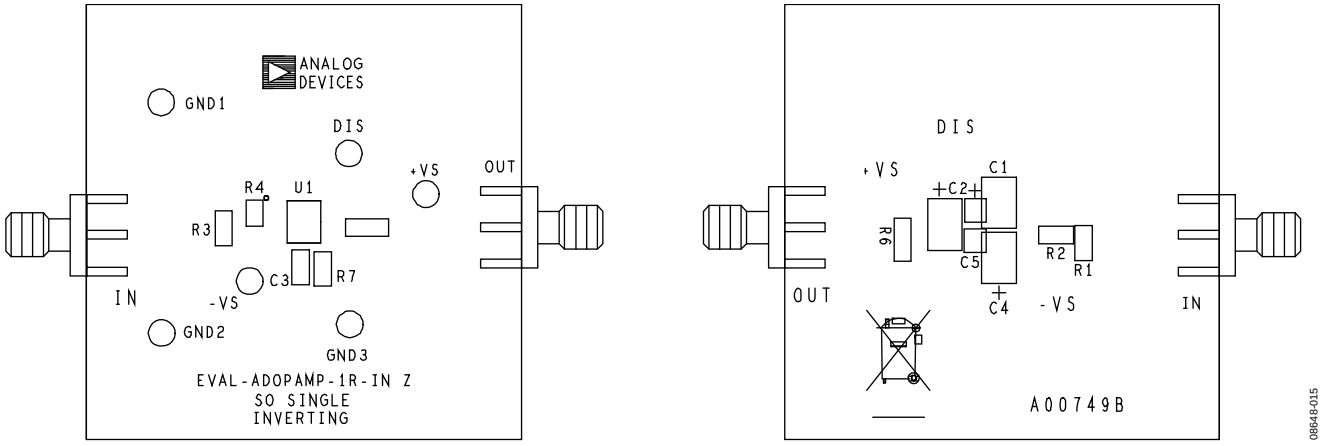


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Figure 7. Inverting Evaluation Board Assembly Drawings

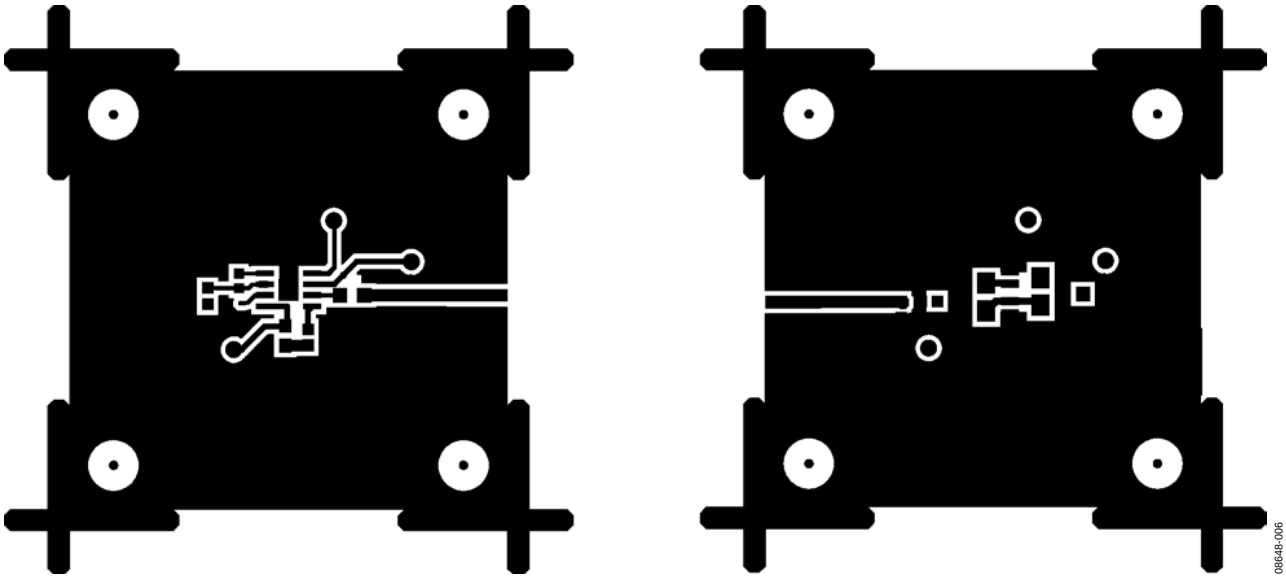

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Figure 8. Inverting Evaluation Board Layout Patterns

LFCSP EVALUATION BOARD SCHEMATICS

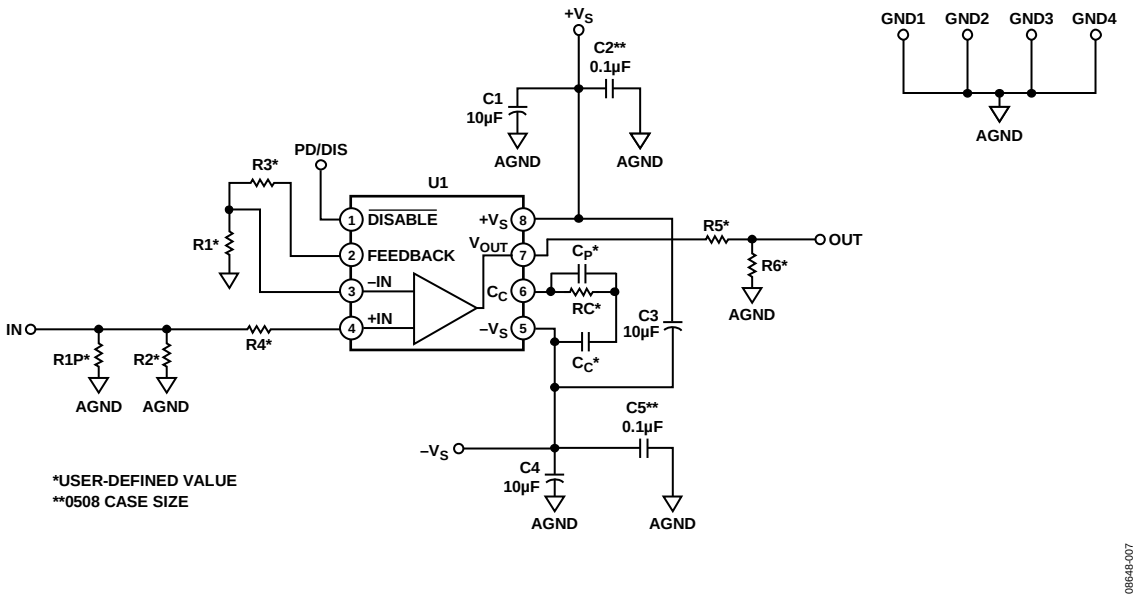


Figure 9. Noninverting Schematic

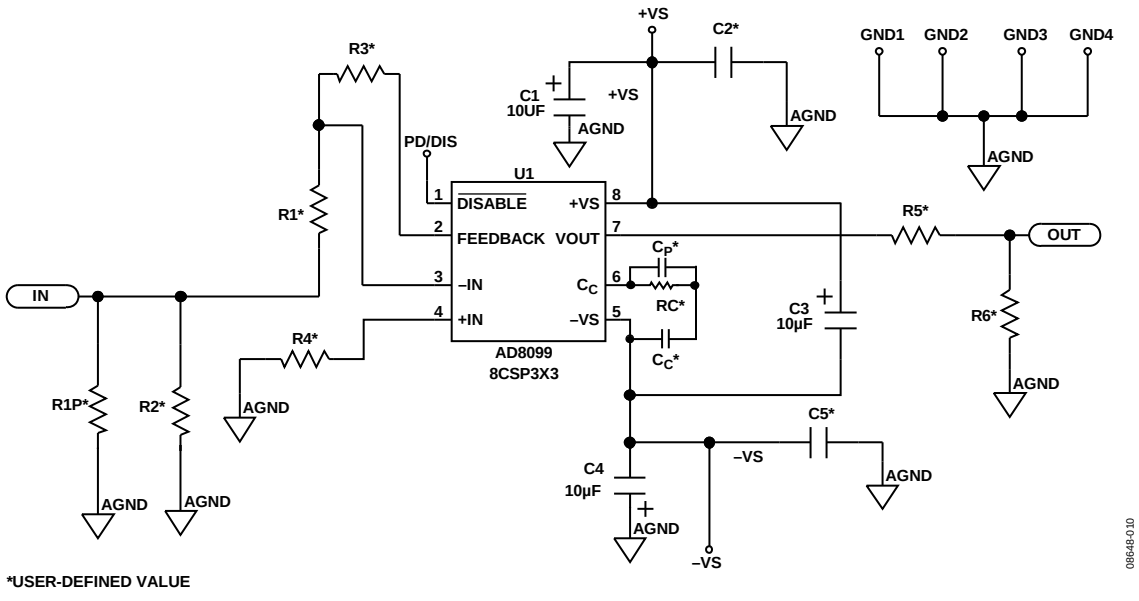
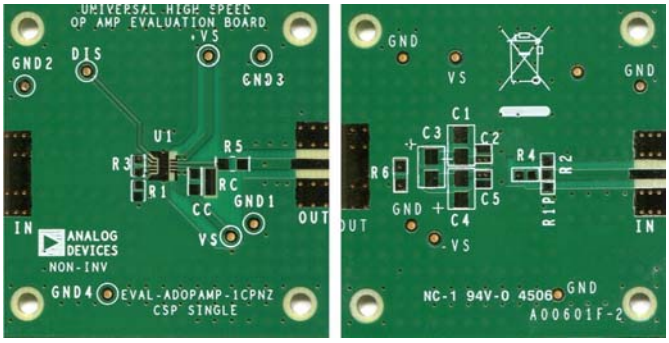


Figure 10. Inverting Schematic

LFCSP EVALUATION BOARD, ASSEMBLY, AND LAYOUT DRAWINGS

NONINVERTING



COMPONENT SIDE CIRCUIT SIDE

NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

08648-008

Figure 11. Noninverting Evaluation Board, Component and Circuit Sides

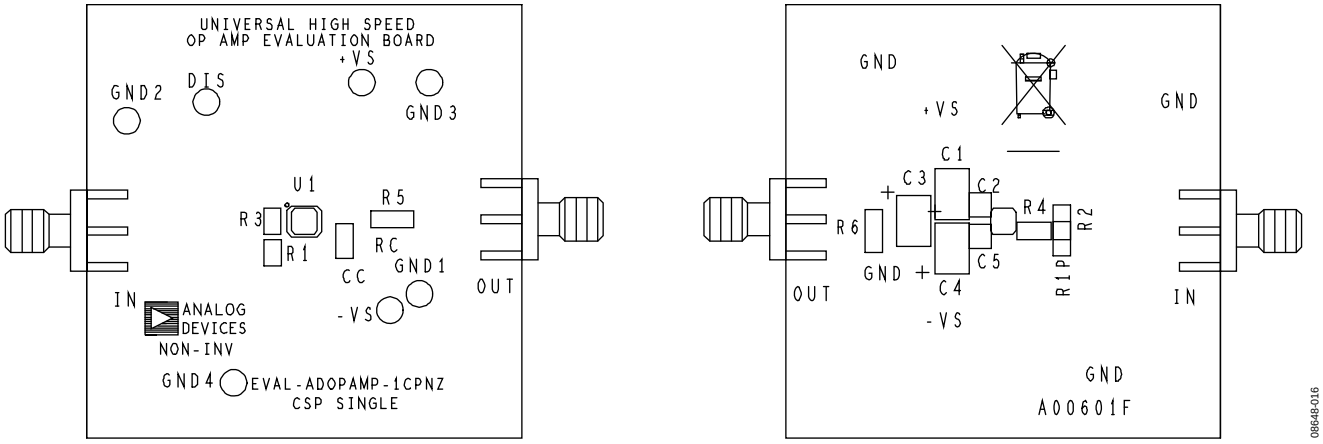


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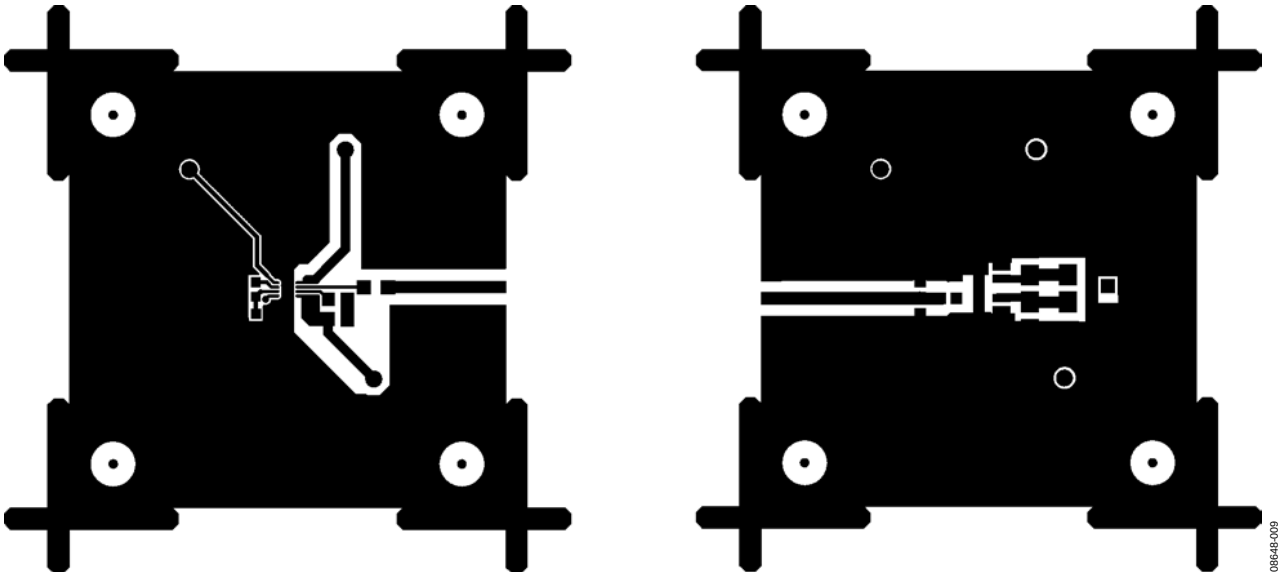
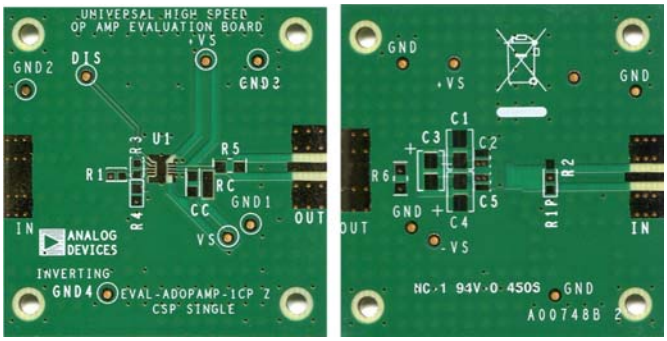
Figure 12. Noninverting Evaluation Board Assembly Drawings



08648-009

Figure 13. Noninverting Evaluation Board Layout Patterns

INVERTING



COMPONENT SIDE CIRCUIT SIDE

NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

08648-011

Figure 14. Inverting Evaluation Board, Component and Circuit Sides

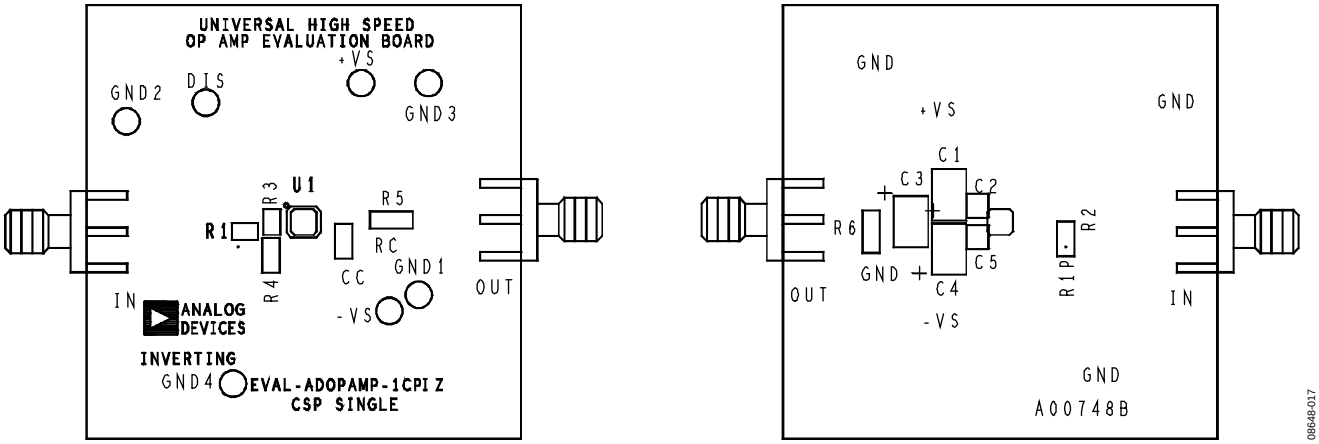


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Figure 15. Inverting Evaluation Board Assembly Drawings

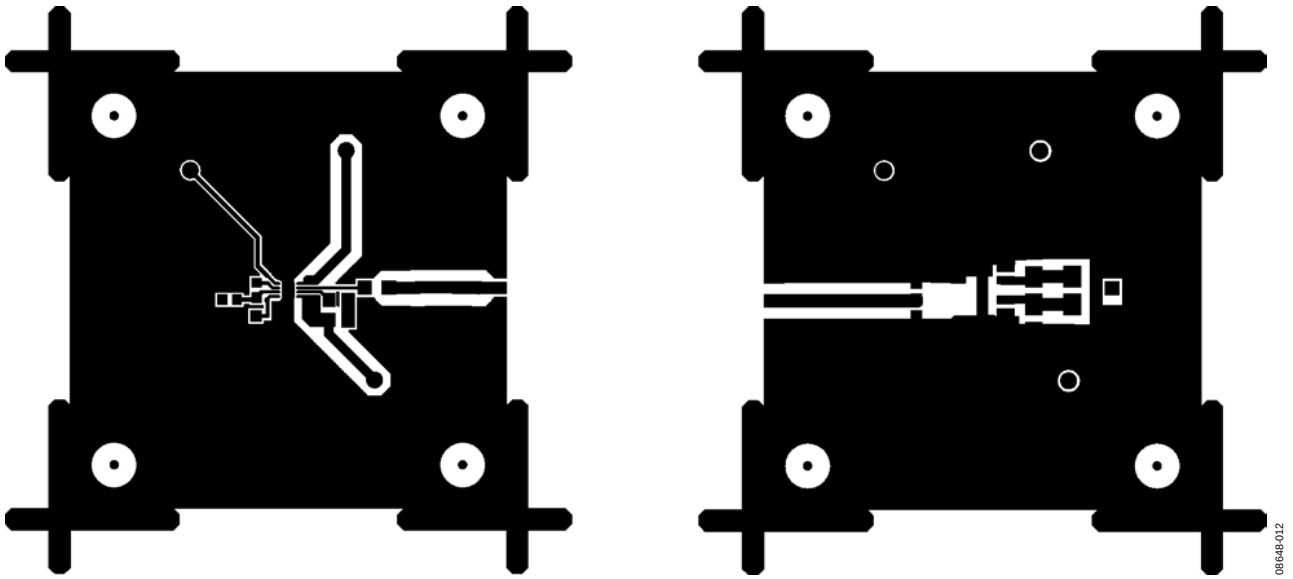

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Figure 16. Inverting Evaluation Board Layout Patterns

SOLDERING INFORMATION

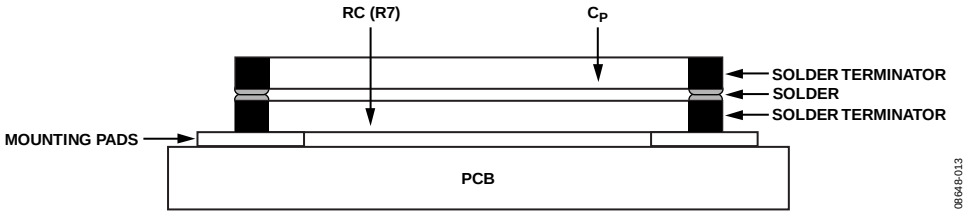

Figure 17. Soldering of Two Parallel Components

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. SOIC

Quantity	Reference Designator	Description	Package
6	+VS, −VS, DIS, GND1, GND2, GND3	Test point	TP
3	C1, C4, C6	10 µF capacitor	3528
2	C2, C5	Capacitor, user defined	C0508
1	C3	Capacitor, user defined	C0805
2	IN, OUT	SMA/SMT	SMA/SMT
4	R1 to R3, R7	Resistor, user defined	R0805
1	R4	Resistor, user defined	R0603
2	R5, R6	Resistor, user defined	R1206
1	U1	AD8099	8-lead SOIC_EP

Table 2. LFCSP

Quantity	Reference Designator	Description	Package
7	+VS, −VS, DIS, GND1, GND2, GND3, GND4	Test point	TP
3	C1, C3, C4	10 µF capacitor	3528
2	C2, C5	Capacitor, user defined	C0508
1	C_C	Capacitor, user defined	C0805
2	IN, OUT	SMA/SMT	SMA/SMT
2	R1, R3	Resistor, user defined	R0603
3	R1P, R2, R4	Resistor, user defined	R0805
2	R5, R6	Resistor, user defined	R1206
1	U1	AD8099	8-lead LFCSP, 3 mm × 3 mm

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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