

Nine Often Overlooked ADC Specifications

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IDEA IN BRIEF

Analog-to-digital converters (ADCs) have many specifications; some are more important for a given application than others. Understanding these specifications and controlling external devices affecting the ADC will lead to better performance.

With so many analog-to-digital converters (ADCs) available, it is always difficult to know which is right for a given application. Data sheets often confuse the issue, and many specifications impact performance in unanticipated ways.

When selecting converters, engineers often simply look at resolution, signal to noise ratio (SNR) or harmonics. While these are important, other specifications can be equally significant.

Resolution

Resolution, perhaps the most misunderstood specification refers to the number of output bits, but provides no useful information on performance. Some data sheets list effective number of bits (ENOB), which uses actual SNR measurements to compute the converter's effectiveness. An even more useful gauge for converter performance is noise spectral density (NSD) specified in either dBm/Hz or nV/ $\sqrt{\text{Hz}}$. NSD can be calculated by knowing the sample rate, input range, SNR, and input impedance (for dBm/Hz). Once these are known, a converter can be selected to match the analog performance of the front-end circuitry. This is a better method of selecting an ADC than simply stating the resolution.

Many users are also concerned with spurious and harmonic performance. These are not related to resolution, but converter designers generally adjust their designs such that harmonics fall in line with resolution.

Power Supply Rejection

Power supply rejection (PSR) measures how power supply ripple is coupled to the ADC input to appear on its digital outputs. With limited PSR, noise on the power supply line will be suppressed only 30 dB to 50 dB below the input level.

Normally, the unwanted signal on the power supply is relative to the input range of the converter. For example, if the noise on the power supply is 20 mV rms and converter input range is 0.7 V rms, then the noise on the input is -31 dBFS. If the converter has 30 dB PSR, coherent noise would show up as a -61-dBFS spectral line in the output. PSR is important in determining how much filtering and decoupling the power supply will need. PSR is important in high-noise environments, such as medical or industrial applications or where dc-to-dc converters may be used for high power efficiency.

Common-Mode Rejection

Common-mode rejection (CMR) measures the induced differential-mode signal in the presence of a common-mode signal. Many ADCs employ differential inputs to provide high immunity to common-mode signals and because differential input structures naturally reject even-order distortion products.

As with PSR, common-mode signals can be induced by power supply ripple, high-power signals induced on the ground plane, RF leakage through mixers and RF filters, and applications where high electric and magnetic fields are found. While many converters do not specify CMR, they often have CMR of 50 dB to 80 dB.

Clock Slew Rate

Clock slew rate is the minimum slew rate required to achieve the rated performance. Most converters have sufficient gain on the clock buffer to ensure that the sample instant is well defined, but excess noise will occur if the slew rate is slow enough to produce a high degree of uncertainty of the sample moment. If a minimum input slew rate is specified, users should meet that requirement to ensure the rated noise performance.

Aperture jitter

Aperture jitter is the internal clock uncertainty to the ADC. The noise performance of the ADC is limited by the clock jitter, both internal and external.

In a typical data sheet, aperture jitter is for the converter only. External aperture jitter sums in an rms manner with internal aperture jitter. For low-frequency applications, jitter may be unimportant, but as analog frequency increases, noise due to jitter becomes an increasing concern. Failure to use an adequate clock will result in poorer than expected performance.

In addition to increased noise from clock jitter, spectral lines in the clock signal that are not harmonically related to the clock will show up as distortion on the digitized output. Therefore, the clock signal should have the highest possible spectral purity. For more details on the effects of aperture jitter see Analog Devices applications notes [AN-501](#) and [AN-756](#).

Aperture delay

Aperture delay is the time delay between the application of the sampling signal and the moment the input signal is actually sampled. This time—typically a nanosecond or less—may be positive, negative or even zero. Unless knowing the exact sampling instant is important, aperture delay is unimportant.

Conversion Time and Conversion Latency

Conversion time and conversion latency are two closely related specifications. Conversion time generally applies to successive-approximation converters (SAR), where a high clock rate is used to process the input signal, which appears on the output much later than the conversion command, but prior to the next conversion command. The time between conversion command and conversion completion is the conversion time.

Conversion latency is usually applied to pipelined converters. A measure of the number of pipelines (internal digital stages) that are used to produce the digital output, it is usually stated in terms of pipeline delays. Actual conversion time may be calculated by multiplying this number by the sample period used in the application.

Wake Up Time

To conserve power in power-conscious applications, the device is commonly powered down during periods of relative disuse. While this does save considerable power, a

finite amount of time is required for internal references to stabilize and for internal clock functionality to resume when the device is turned back on. During this time, conversion data produced will not meet specifications.

Output Loading

Like all digital output devices, ADCs—especially CMOS output devices—specify output drive capability. While important to know for reliability reasons, optimal performance will usually occur at less than full drive capability.

In high performance applications, it is important to minimize the output loading and to provide proper decoupling and an optimized layout to minimize voltage drop on the supply. To avoid these problems, many converters provide LVDS outputs. Because LVDS is a symmetric, switching currents are reduced and overall performance is improved. If available, LVDS outputs should be used to ensure best performance.

Monotonicity

A non-monotonic converter is one where the digital codes exhibit a localized change in the sign of the slope. Therefore, for a constantly increasing analog input, the digital output exhibits a localized change in slope from positive to negative and back to positive. For applications where ac performance is important, non-monotonic behavior is likely to not cause a problem. However, for applications where the ADC is part of a closed loop, such behavior can often cause loop instability and poor performance. For such applications, a converter should be carefully chosen to ensure that it has monotonic performance.

Unspecified Criteria

One unspecified item that is of vital importance is PCB layout. While little can be specified, it can significantly impact converter performance. If the application failed to include sufficient decoupling capacitors, for example, excess power supply noise would exist. Because of finite PSR, noise on the supplies would couple into the analog inputs and corrupt the digital output spectrum as shown in Figure 1.

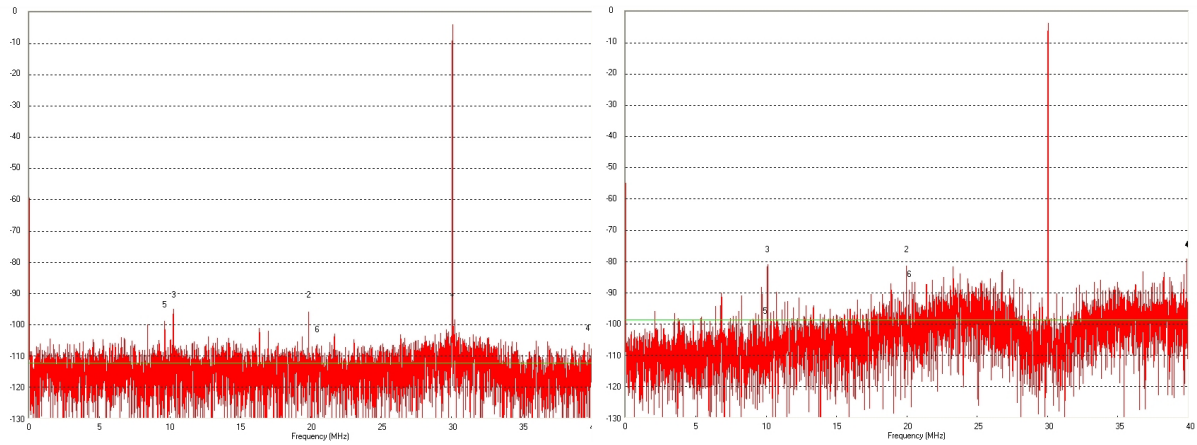


Figure 1. Performance with Caps (Left) and Performance with Limited Caps (Right)

RESOURCES

[AN-501 Application Note, Aperture Uncertainty and ADC System Performance.](#) Analog Devices, Inc.

[AN-756 Application Note, Sampled Systems and the Effects of Clock Phase Noise and Jitter.](#) Analog Devices, Inc.