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Presentation Title: SHARC Processor Overview

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Chapter 1: SHARC Family at a Glance

Hello and thank you for joining me today to learn more about the SHARC Processor. My name is David Miller and I'm the manager of the applications engineering team for SHARC at Analog Devices.

Today we're going to be covering the target markets for SHARC, SHARC processor advantages, take a look at the family of SHARC processors that are available. We're going to look at the SHARC hardware overview beginning with the SIMD architecture of the SHARC and looking at the IO processor, the direct memory access engine, and also at the SHARC peripherals. Finally we'll take a look at some additional support and resources that are available to learn more about the SHARC.

We'll start by taking a look at the SHARC processor family and some of the features. The SHARC processor is capable of the high performance with 2.4 gigaflops at 400 MHz. We also have a large set of partners that help customers develop their products.

For automotive applications and any other application where a high temperature is expected some of the SHARCs are available for ambient 105 degree C operation. Also there's a large set of peripherals and on-chip memory that are available on the SHARCs.

These features suit the SHARC for the following applications and many more, from digital home and the home theater systems and high definition DVD to pro audio applications where the SHARC is found in mixers, amplifiers, and synthesizers. Industrial and instrumentation markets such as medical and test and measurement as well as control. Also in the automotive environment where SHARC is found in many audio amplifiers.

Some of the features that the SHARC supports are high performance 32-bit and 40-bit extending floating-point operations, as well as 32-bit fixed-point operations. The core runs at up to 400 MHz on the fastest SHARCs providing again our 2.4 gigaflop.

The SHARC core is a single instruction multiple data architecture. This contains two computational units capable of concurrent code execution meaning you can operate the same instruction in both of these units within the same cycle.

The single cycle execution of dual multiply and ALU operations is one of the features of SHARC. Also within the single cycle can be a dual read or write and an instruction fetch.

There's a wide band width between the core and memory for maintaining this single cycle operation. Some of the floating-point advantages of SHARC; floating-point reduces quantization errors, also produces better precision, and higher dynamic range and this is helpful for applications such as filters.

Summary of some of the specific advantages for SHARC, in general for common applications, 32-bit floating-point is certainly a benefit. Large on-chip memory is available and also Glueless interface to external memory. If we look at some of the more specialized applications such as consumer and automotive there are audio decoders available in the ROM on some of the SHARC parts. Also in hardware our sample rate converters and an S/PDIF interface.

For automotive customers in specific we've added in hardware DTCP cipher engine and again our 105C ambient operating temperature is a large benefit to automotive customers.

Here we're talking a look at the portfolio of the SHARCs and this begins with our 2116x family. On the upper half of this we see our higher performance SHARCs. We go through the 2116x, 2126x, and 2136x families. Basically what you see as we go across here is in an increase in memory integration on the parts, an increase in the performance of the part, and an increase in the peripherals available on the part.

Across the bottom we see our lower cost SHARCs. Again we see some increase in memory in performance and peripherals, but these are designed for applications where maybe not as much performance is needed.

Taking a look at this chart and I promise that this is the only eye chart in the presentation today, this is a nice chart because it gives you the opportunity to see a lot of the features of all of the

SHARCs available. And these are all currently in production and available from Analog Devices.

What this chart shows is the amount of memory, the performance, the set of peripherals as well as the packages that these processors are available in, also noting which processors operate at which temperature gradients.

Now looking at one of the features of the SHARCs that's been maintained throughout is compatibility. What we've done with many of the SHARCs is maintained pin compatibility allowing for customers to be able to migrate from older applications to newer applications needing more performance. Or to move from an application that needs to be moved to a lower performance to build derivatives of products. In this case what we're looking at is moving from our 2126x family to our 2136x family. And this is as you notice here with the operating frequencies is an increase in performance. It's also an increase in the on-chip memory.

The thing here is that these are available in pin compatible packages. So when moving forward and developing new generations of products one is capable of not having to redesign your board, but being able to put down newer SHARCs with more features.

I would also mention at this point that these SHARCs are also code-compatible as they are in general across the whole family.

Now again taking a look at some compatibility in this case we're looking at moving from the 36x to the 37x family. The 37x family is a cost reduced version of the SHARC. Again we have pin compatibility for these parts.

Chapter 2: SHARC Hardware Overview

Now we'll move forward and take a little bit more detailed look at what's inside the SHARC. This is a block diagram that you'll find in the 21369 data sheet and I'm going to use this diagram to take us through a good portion of the rest of this presentation.

What we see here is the core processor, the memory interfaces and also our IO processor and we'll cover each of these separately. This block diagram is generally a superset of what's available on the SHARCs in terms of peripherals and the memory and the core, although the core is very common across the board.

Let's move forward and take a look at the core processor. If you'll notice here we have two processing elements providing for our SIMD architecture; processing element X and processing element Y. Within each of the processing elements there's an ALU, a barrel shifter, an independent register file, and also a multiplier or MAC unit.

Now if you look at the bus structure what we've provided for here are two 64-bit wide data buses which provide for keeping the register files and the data available to each of the processing elements to be able to operate on this data in each instruction cycle.

Looking up a little bit if you see the DAG, we have two DAGs or data address generators and these are capable of indirect and direct addressing as well as pre and post modify on the pointers.

Back to our block diagram again we're going to take a look now at some of the information about the memory structure. As I've said before the SHARCs have large internal RAM and ROM. The on-chip RAM operates at the same speed as the core. Providing for zero wait states during code and data accesses.

This is as usual performance improved over external memory. It's a predictable performance.

Also about the RAM memory, the RAMhas been partitioned into blocks. This is done so that it is easy to access RAM by the core as well as the DMA engine simultaneously.

Now let's take a look at the external memory interface on the SHARCs. The external memory interface allows for interfacing to SDRAM, SRAM, and parallel flash devices. This all is done gluelessly. For SDRAMs we support 64 megabit up through 512 megabit parts inconfigurations of 4, 8, and 16-bit wide.

Now the buses on the SHARC handle this with 16 or 32-bit wide buses, and these can be operated at up to 166 MHz which is the system clock frequency.

Now on the selected chart the 21368 you can handle shared memory between up to four processors. For parallel flash memories, again we have this 8 and 16-bit wide buses and this is handled through our asynchronous memory interface or AMI.

One of the boot features, or boot options for the SHARC is to be booted from a flash device.

And finally for SRAMs again with 8 and 16-bit wide buses this handled through our asynchronous memory interface.

This slide gives us a little bit of information about a change that was made between the 2136x family and the 2137x family. With the large amount of on-chip memory the SHARC for a long time has not had the need to execute code from the external memory. But what we've done with the 2137x family is reduced the amount of memory that's available on the parts and now we've added again the feature that allows execution of code from external memory.

This is a picture of our cache unit that is included in the 2137x family. Now it's an enhancement of the cache unit that's available on our previous SHARCs and what it does in this case is allow for the cache to act as an instruction cache when executing from external memories but still act as a traditional conflict cache when executing code from internal memory.

Chapter 3: I/O Processor

Let's now take a look at the I/O processor available on the SHARC. Looking back at our block diagram the I/O process is the long rectangular block that runs across the bottom here. You'll notice that the I/O processor includes the DMA controller, all of the peripherals as well as the GPIO flags.

What are the features of the I/O processor? The I/O processor is basically the interface from the real world to the SHARCs core and on the on-chip memory. Also included in the I/O processor our DMA controller. We'll talk more about this in a couple of slides, but generally the DMA controller has 34 DMA channels that are divided between many of the peripherals, 16 of the channels are dedicated to the sports four to the UARTS and so forth.

Also included in the I/O processor is the digital audio interface and the digital peripheral interface. If we look back at our block diagram you can see that the digital audio interface includes a number of the peripherals including the precision clock generators, the sample rate converters, the S/PDIF interface, serial ports. It also has a number of pins that are available that can be mapped through the signal routing unit to bring these peripherals outside the chip.

Now if we take a look at the digital peripheral interface, a similar thing here, a set of peripherals, the SPI port, the SPI port. The two wire interface, the UARTs, and the timers. The signal routing unit included here brings these peripherals out to the 14 pins that are external to the chip.

The signal routing unit that I just described allows for really reducing the costs of the SHARCs. With the large set of peripherals that we include on the SHARCs it would be very expensive to bring pins out each of these peripherals. What we've done is noticed that in many applications pins are unused and pins are connected in parallel and tied high or tied low. And so we use the SRU unit to bring down the number of pins to reduce the cost of the part and also make it possible for us to put all of these peripherals on the SHARC and then allow the user to determine which of those peripherals they use in their applications.

Chapter 4:Direct Memory Access (DMA)

Now we'll take a look at the direct memory access engine. Again the direct memory access engine is included within the I/O processor. So some of the features of the directory memory access engine are; the direct memory access engine allows for zero overhead back ground transfers at the full clock rate. What this means is that the core is capable of going on and executing it's program while these memory transfers take place. We can transfer both code and data during these DMA transfers. And also during the transfers there could be packing of 8, 16, 32, 40 or 48-bits automatically performed during the transfer and again without the cores intervention.

DMA transfers are programmed and handled by the core through a set of memory mapped registers. Some of the features of the DMA; DMA transfers are configured and initiated by the SHARC core through the memory map registers. Now there are 34 DMA channels available on the 2136x family and just 32 available on the 2137x family because of a slightly reduced peripheral set.

Our DMAs can be paused and restarted. Different peripherals support different flavors of DMA such as the circular buffering or chaining. As we noted before the RAM memory is organized in blocks and this is done to eliminate conflicts where the core and DMA are trying to access internal memory.

Chapter 5: SHARC Peripherals

Now let's take a look at some of the peripherals on the SHARC. Back to our block diagram. All of the peripherals are again included within the I/O processor and organized into groups with the digital audio interface and a digital peripheral interface. So let's take a look at some of those peripherals. First of all, the SHARC synchronous serial ports, or SPORTS as we call them. This is a very flexible serial interface. It allows the SHARC to interface to many other devices and also to interface between other SHARCs.

The SPORTS support a 3- to 32-bit serial word length, they have several operating modes, and also support a time division multiplexed mode.

Each of the SPORTS has four signals, a clock, a frame sync, a Data A and a Data B. Also SPORTS can be configured for one of four modes, the normal SPORT mode, a multichannel TDM mode capable of supporting up to 128 channels per frame. An I^2S mode, and also a left justified sample pair mode. SPORTS other sport programmable parameters include programmable for internal and external source for the clock and the frame sync, also early, late, or no frame sync. The TDM mode again programable for 1 to 128 channels. And the data directions for the SPORTS Channel A and B are programmable as transmit or receive.

A couple other things to notice about the SPORT and the configurations available there. The signal routing unit that we talked about earlier allows for multiple SPORTS to be combined to run off as little as one clock and frame sync. Also the SPORTS can be configured for a number of different input and output options. And finally the data signals that are configured through software as inputs and outputs can be configured to be for instance on a SHARC with six SPORTS can be all configured for 12 channels out to 12 channels in and any combination in between there in pairs.

Now in addition there are a number of peripherals that handle serial interfaces that are included within the SHARCs. The serial peripheral interface or the SPI, the UART, the two wire interface or TWI, and the S/PDIF interface or the Sony Phillips differential interface.

The SPI is a four wire serial interface and it enables the SHARC processor to communicate with a number of other SPI compatible devices such as other microcontrollers or microprocessors and also enable SHARC to SHARC communication.

SPI port again configurable by a set of memory map registers is capable of full duplex operation, master and slave modes word widths of 8, 16, 32-bits. Programmable bode rates, clock polarities and phases, and also master and slave booting is possible for the SHARC through the SPI device.

The UART is an industry standard 16450 compliant UART. There are two of the UARTs on each of the SHARCs. These support the half duplex IrDA interface.

The two wire interface fully compliant with the Phillips I^2C bus protocol supports master and slave operations. And also in the master mode supports the serial camera control bus. The S/PDIF interface supports a number of standards including the AES EBU standards. Again through memory map registers is programmable for left or right justified, I^2 S and serial data input with word widths of 16, 18, 20 and 24-bits.

Now on selected SHARCs the sample rate converters are included in hardware on those SHARCs. There are four independent sample rate converters. The sample rate converters again programmable through memory map registers are capable of performing synchronous or asynchronous sample rate conversion. Provide up to a 128 dB SNR. Left or right justified, I^2S, TDM and data modes. And data word lengths of 24, 20, 16 and 18-bits.

Now one of the nice features about the sample rate converters is they can be used to clean up a jittery clock for instance on an S/PDIF interface. Also on the SHARCs are the precision clock generators. There are four precision clock generators, each of these capable of generating a clock and a frame sync signal. They can be routed through the SRU to on-chip peripherals or off-chip.

The timers and the PDM modules pulse with modulation modules. There are up to four timers on each SHARC. Each SHARC has a core timer, core timer counts core clock cycles and generates an interrupt when a count expires. There are up to three general purpose timers. General purpose timers operate at the system clock rate and they're capable of generating pulse wave forms and also can be operated as a watch dog event timer.

In the pulse width modulation modules there's four of these modules on each of the SHARCs. Each of these are capable of four outputs for a total of 16 potential outputs. This module is useful in control applications where motor control may be involved and a number of different wave forms or needed to control a motor.

Again back to our block diagram we've gone through all the peripherals in the DAI or the digital audio interface. All the peripherals in the DPI or the digital peripheral interface. Also notice here that the GPIO flags are included within the I/O processor.

Chapter 6: Development Tools

Now let's take a look at the development tools that are provided by Analog Devices. CROSSCORE is Analog Devices development tools product line. And within the CROSSCORE line is included our VisualDSP++ integrated development and debug platform, our emulators, our evaluation boards, or EZ-KIT Litess and some daughter cards or EZ-Extender cards and we'll take a look at some of those.

Let's look at some of the features of VisualDSP++. Included in VisualDSP++ are our code generation tools, the C and C++ complier, the C and C++ runtime libraries as well as the assembler and linker. The complier for the SHARC which is included here in the VisualDSP++ takes advantage of the SIMDarchitecture of the SHARC. It also takes advantage and makes possible single cycle execution of floating-point operations.

Also included are the simulator which allows for development of applications without the need for hardware. Also included in VisualDSP++ is our VDK or real time operating system kernel and scheduler.

Now if we take a look here at the right side of this slide this is a screenshot of VisualDSP++ in action. What we see here is a code editing window, a window into program memory and also the disassembly of the code that's being run and whatever was being run at this time, also a window into the input and output of the program.

Now let's take a look at some of the hardware tools that are available from Analog Devices. First of all our EZ-KIT Litess. These are good evaluation platforms, inexpensive evaluation platforms that allow programming and developing of software on the SHARC. There's a number of EZ-KIT Litess available including the 2137x, 36x and 32x families. These interface through our USB emulators to the VisualDSP++ environment.

Also available are our EZ-Extender Cards. These EZ-Extender Cards give access to a number of various peripherals from Analog Devices and third parties.

Chapter 7: Additional Support

Let's take a look at some addition support areas for SHARC in terms our third party software and libraries that are available. Now there are number of third parties, some of them are listed here, AV Labs, Danville Signal Processing, DSP Concepts and Kaztek systems, Mathworks. These third parties offer a variety of services from software libraries to embedded system development to hardware support.

With Kaztek systems a lot of our worldwide training is done by Kaztek. With the Mathworks, Mathworks has developed the embedded the IDE length which allows interfacing between Matlab, Simulink and VisualDSP++, AV Labs, Danville Signal Processing and DSP Concepts again offer services from software, hardware, and embedded systems.

Here we take a look at some of the software that's available to run on a SHARC. From post processing algorithms to spatial algorithms to signal display algorithms.

Chapter 8: Conclusion

In conclusion we've looked a lot of things about the SHARC today. We've taken a look at the target markets that the SHARC is well suited for in terms of home applications, audio applications, industrial instrumentation, as well as automotive applications. We've taken a look at some of the advantages of the SHARC processor; from its rich set of peripherals to its large memory and its high performance.

We've taken a look at the large set of family members that are available in the SHARC family and the set of peripherals, memory, and performance that's available across the range. We've looked at the SHARC hardware over view starting with its SIMD architecture with dual computational units.

We've looked at our I/O processor with our signal routing units and the set of peripherals that are included with our digital applications interface and our digital peripheral interface.

We've taken a look at our direct memory access engine with up to 34 channels of DMA. It allows for moving data around without core intervention.

We've taken a look at SHARC peripherals from our serial interfaces to our sample rate converters and SPORTS and GPIO. Finally we've taken a look at some of the third parties that are available to help support development with the SHARC and the tools that are available from Analog Devices.

Thank you for joining me today to learn about the SHARC processor. For more information please go to the Analog Devices website at; www.analog.com there you will find white papers, applications notes, manuals, data sheets, sample code, development tools, and much more. In fact you can take a 90 day free test drive of the VisualDSP++ tools. You can also find information about multi-day workshops. Finally click on the "ask a question" button if you have something specific you'd like to find out about the SHARC.