

FEATURES

Automotive versions qualified per AEC-Q100

Low power operation

5 V operation

1.0 mA per channel maximum @ 0 Mbps to 2 Mbps

3.5 mA per channel maximum @ 10 Mbps

31 mA per channel maximum @ 90 Mbps

3 V operation

0.7 mA per channel maximum @ 0 Mbps to 2 Mbps

2.1 mA per channel maximum @ 10 Mbps

20 mA per channel maximum @ 90 Mbps

Bidirectional communication

3 V/5 V level translation

High temperature operation: 125°C

High data rate: dc to 90 Mbps (NRZ)

Precise timing characteristics

2 ns maximum pulse width distortion

2 ns maximum channel-to-channel matching

High common-mode transient immunity: >25 kV/ μ s

Output enable function

16-lead SOIC wide body package

RoHS-compliant models available

Safety and regulatory approvals

UL recognition: 2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice #5A

VDE Certificate of Conformity

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

$V_{IORM} = 560$ V peak

TÜV approval: IEC/EN/UL/CSA 61010-1

APPLICATIONS

General-purpose multichannel isolation

SPI interface/data converter isolation

RS-232/RS-422/RS-485 transceivers

Industrial field bus isolation

Automotive systems

GENERAL DESCRIPTION

The ADuM140x¹ are quad-channel digital isolators based on Analog Devices, Inc., *iCoupler*[®] technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *iCoupler* devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics.

The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth of the power of optocouplers at comparable signal data rates.

The ADuM140x isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM140x provides low pulse width distortion (<2 ns for CRW grade) and tight channel-to-channel matching (<2 ns for CRW grade). Unlike other optocoupler alternatives, the ADuM140x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and when power is not applied to one of the supplies.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

FUNCTIONAL BLOCK DIAGRAMS

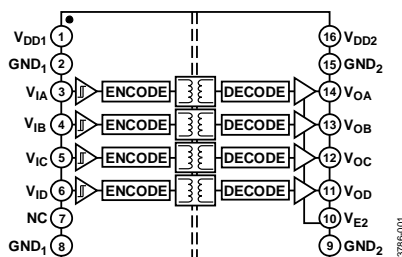


Figure 1. ADuM1400

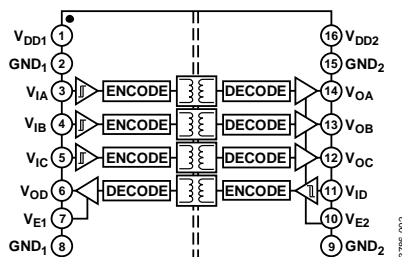


Figure 2. ADuM1401

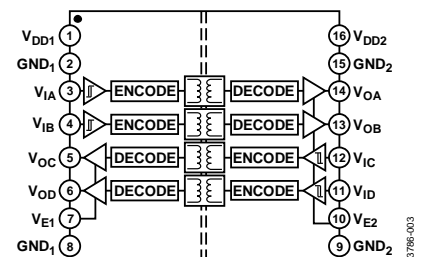


Figure 3. ADuM1402

Rev. G

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REVISION HISTORY

5/08—Rev. F to Rev. G

Added ADuM1400W, ADuM1401W, and ADuM1402W
 Parts Universal
 Added Table 4 11
 Added Table 5 13
 Added Table 6 15
 Added Table 7 17
 Changes to Table 12 20
 Changes to Table 13 21
 Added Automotive Products Section 29
 Changes to Ordering Guide 30

11/07—Rev. E to Rev. F

Changes to Note 1 1
 Added ADuM140xARW Change vs. Temperature Parameter ... 4
 Added ADuM140xARW Change vs. Temperature Parameter ... 5
 Added ADuM140xARW Change vs. Temperature Parameter ... 8
 Changes to Figure 17 18

6/07—Rev. D to Rev. E

Updated VDE Certification Throughout 1
 Changes to Features and Note 1 1
 Changes to Figure 1, Figure 2, and Figure 3 1
 Changes to Regulatory Information Section 10
 Changes to Table 7 11
 Added Table 10 12
 Added Insulation Lifetime Section 20
 Updated Outline Dimensions 21
 Changes to Ordering Guide 21

2/06—Rev. C to Rev. D

Updated Format Universal
 Added TÜV Approval Universal

5/05—Rev. B to Rev. C

Changes to Format Universal
 Changes to Figure 2 1
 Changes to Table 3 8
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6/04—Rev. A to Rev. B

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 Changes to Features 1
 Changes to Electrical Characteristics—5 V Operation 3
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 Changes to Electrical Characteristics—Mixed 5 V/3 V or 3 V/5 V Operation 7
 Changes to DIN EN 60747-5-2 (VDE 0884 Part 2) Insulation Characteristics Title 11
 Changes to the Ordering Guide 19

5/04—Rev. 0 to Rev. A

Updated Format Universal
 Changes to the Features 1
 Changes to Table 7 and Table 8 14
 Changes to Table 9 15
 Changes to the DC Correctness and Magnetic Field Immunity Section 20
 Changes to the Power Consumption Section 21
 Changes to the Ordering Guide 22

9/03—Revision 0: Initial Version

ADuM1400/ADuM1401/ADuM1402

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION¹

4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DD1(Q)}		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	I _{DDO(Q)}		0.19	0.21	mA	
ADuM1400 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} Supply Current	I _{DD1(10)}		8.6	10.6	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V _{DD1} Supply Current	I _{DD1(90)}		70	100	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(90)}		18	25	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} Supply Current	I _{DD1(10)}		7.1	9.0	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		4.1	5.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V _{DD1} Supply Current	I _{DD1(90)}		57	82	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(90)}		31	43	mA	45 MHz logic signal freq.
ADuM1402 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(Q), I_{DD2(Q)}}		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(10), I_{DD2(10)}}		5.6	7.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(90), I_{DD2(90)}}		44	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I _{IA} , I _{IB} , I _{IC} , I _{ID} , I _{E1} , I _{E2}	-10	+0.01	+10	μA	0 V ≤ V _{IA} , V _{IB} , V _{IC} , V _{ID} ≤ V _{DD1} or V _{DD2} , 0 V ≤ V _{E1} , V _{E2} ≤ V _{DD1} or V _{DD2}
Logic High Input Threshold	V _{IH} , V _{EH}	2.0			V	
Logic Low Input Threshold	V _{IL} , V _{EL}			0.8	V	
Logic High Output Voltages	V _{OAH} , V _{OBH} , V _{OCH} , V _{ODH}	(V _{DD1} or V _{DD2}) - 0.1	5.0		V	I _{OX} = -20 μA, V _{IX} = V _{IxH}
		(V _{DD1} or V _{DD2}) - 0.4	4.8		V	I _{OX} = -4 mA, V _{IX} = V _{IxH}
Logic Low Output Voltages	V _{OAL} , V _{OBL} , V _{OCL} , V _{ODL}		0.0	0.1	V	I _{OX} = 20 μA, V _{IX} = V _{IxL}
			0.04	0.1	V	I _{OX} = 400 μA, V _{IX} = V _{IxL}
			0.2	0.4	V	I _{OX} = 4 mA, V _{IX} = V _{IxL}
SWITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	50	65	100	ns	C _L = 15 pF, CMOS signal levels

ADuM1400/ADuM1401/ADuM1402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			40	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew ⁶	t_{PSK}			50	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching ⁷	t_{PSKCD}/t_{PSKOD}			50	ns	$C_L = 15$ pF, CMOS signal levels
ADuM140xBRW						
Minimum Pulse Width ³	PW			100	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay ⁵	t_{PHL}, t_{PLH}	20	32	50	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew ⁶	t_{PSK}			15	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t_{PSKCD}			3	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t_{PSKOD}			6	ns	$C_L = 15$ pF, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width ³	PW		8.3	11.1	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate ⁴		90	120		Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay ⁵	t_{PHL}, t_{PLH}	18	27	32	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD		0.5	2	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew ⁶	t_{PSK}			10	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t_{PSKCD}			2	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t_{PSKOD}			5	ns	$C_L = 15$ pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	$C_L = 15$ pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	$C_L = 15$ pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	$C_L = 15$ pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	$ CM_H $	25	35		kV/μs	$V_{IX} = V_{DD1}$ or V_{DD2} , $V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	$ CM_L $	25	35		kV/μs	$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current per Channel ⁹	$I_{DDI(D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	$I_{DDO(D)}$		0.05		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ADuM1400/ADuM1401/ADuM1402

ELECTRICAL CHARACTERISTICS—3 V, 105°C OPERATION¹

2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DD1(Q)}		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	I _{DD0(Q)}		0.11	0.14	mA	
ADuM1400 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} Supply Current	I _{DD1(10)}		4.5	6.5	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		1.4	2.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V _{DD1} Supply Current	I _{DD1(90)}		37	65	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(90)}		11	15	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} Supply Current	I _{DD1(10)}		3.7	5.4	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		2.2	3.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V _{DD1} Supply Current	I _{DD1(90)}		30	52	mA	45 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(90)}		18	27	mA	45 MHz logic signal freq.
ADuM1402 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(Q), I_{DD2(Q)}}		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(10), I_{DD2(10)}}		3.0	4.2	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(90), I_{DD2(90)}}		24	39	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I _{IA} , I _{IB} , I _{IC} , I _{ID} , I _{E1} , I _{E2}	-10	+0.01	+10	μA	0 V ≤ V _{IA} , V _{IB} , V _{IC} , V _{ID} ≤ V _{DD1} or V _{DD2} , 0 V ≤ V _{E1} , V _{E2} ≤ V _{DD1} or V _{DD2}
Logic High Input Threshold	V _{IH} , V _{EH}	1.6			V	
Logic Low Input Threshold	V _{IL} , V _{EL}			0.4	V	
Logic High Output Voltages	V _{OAH} , V _{OBH} , V _{OCH} , V _{ODH}	(V _{DD1} or V _{DD2}) - 0.1	3.0		V	I _{Ox} = -20 μA, V _{Ix} = V _{IxH}
Logic Low Output Voltages	V _{OAL} , V _{OBL} , V _{OCL} , V _{ODL}	(V _{DD1} or V _{DD2}) - 0.4	2.8		V	I _{Ox} = -4 mA, V _{Ix} = V _{IxH}
			0.0	0.1	V	I _{Ox} = 20 μA, V _{Ix} = V _{IxL}
			0.04	0.1	V	I _{Ox} = 400 μA, V _{Ix} = V _{IxL}
			0.2	0.4	V	I _{Ox} = 4 mA, V _{Ix} = V _{IxL}
SWITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	50	75	100	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} - t _{PHL} ⁵	PWD			40	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	C _L = 15 pF, CMOS signal levels

ADuM1400/ADuM1401/ADuM1402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM140xBRW						
Minimum Pulse Width ³	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	20	38	50	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} – t _{PHL} ⁵	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			22	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t _{PSKOD}			6	ns	C _L = 15 pF, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width ³	PW		8.3	11.1	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		90	120		Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	20	34	45	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} – t _{PHL} ⁵	PWD		0.5	2	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			16	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			2	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t _{PSKOD}			5	ns	C _L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t _{PHZ} , t _{PLH}		6	8	ns	C _L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t _{PZH} , t _{PZL}		6	8	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		3		ns	C _L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV/μs	V _{ix} = V _{DD1} or V _{DD2} , V _{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM _L	25	35		kV/μs	V _{ix} = 0 V, V _{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f _r		1.1		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI(D)}		0.10		mA/ Mbps	
Output Dynamic Supply Current per Channel ⁹	I _{DDO(D)}		0.03		mA/ Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ADuM1400/ADuM1401/ADuM1402

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V, 105°C OPERATION¹

5 V/3 V operation: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$; 3 V/5 V operation: $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$; $V_{DD1} = 3.0\text{ V}$, $V_{DD2} = 5\text{ V}$ or $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.0\text{ V}$. These specifications do not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DD1(Q)}$					
5 V/3 V Operation			0.50	0.53	mA	
3 V/5 V Operation			0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	$I_{DD0(Q)}$					
5 V/3 V Operation			0.11	0.14	mA	
3 V/5 V Operation			0.19	0.21	mA	
ADuM1400 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			2.2	2.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.5	0.9	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			8.6	10.6	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			1.4	2.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1(90)}$					
5 V/3 V Operation			70	100	mA	45 MHz logic signal freq.
3 V/5 V Operation			37	65	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(90)}$					
5 V/3 V Operation			11	15	mA	45 MHz logic signal freq.
3 V/5 V Operation			18	25	mA	45 MHz logic signal freq.
ADuM1401 Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			1.8	2.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.7	1.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			7.1	9.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			2.2	3.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			4.1	5.0	mA	5 MHz logic signal freq.

ADuM1400/ADuM1401/ADuM1402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
90 Mbps (CRW Grade Only)						
V _{DD1} Supply Current	I _{DD1 (90)}		57	82	mA	45 MHz logic signal freq.
5 V/3 V Operation			30	52	mA	45 MHz logic signal freq.
3 V/5 V Operation						
V _{DD2} Supply Current	I _{DD2 (90)}		18	27	mA	45 MHz logic signal freq.
5 V/3 V Operation			31	43	mA	45 MHz logic signal freq.
3 V/5 V Operation						
ADuM1402 Total Supply Current, Four Channels²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1 (Q)}		1.5	2.1	mA	DC to 1 MHz logic signal freq.
5 V/3 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation						
V _{DD2} Supply Current	I _{DD2 (Q)}		0.9	1.5	mA	DC to 1 MHz logic signal freq.
5 V/3 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation						
10 Mbps (BRW and CRW Grades Only)						
V _{DD1} Supply Current	I _{DD1 (10)}		5.6	7.0	mA	5 MHz logic signal freq.
5 V/3 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
3 V/5 V Operation						
V _{DD2} Supply Current	I _{DD2 (10)}		3.0	4.2	mA	5 MHz logic signal freq.
5 V/3 V Operation			5.6	7.0	mA	5 MHz logic signal freq.
3 V/5 V Operation						
90 Mbps (CRW Grade Only)						
V _{DD1} Supply Current	I _{DD1 (90)}		44	62	mA	45 MHz logic signal freq.
5 V/3 V Operation			24	39	mA	45 MHz logic signal freq.
3 V/5 V Operation						
V _{DD2} Supply Current	I _{DD2 (90)}		24	39	mA	45 MHz logic signal freq.
5 V/3 V Operation			44	62	mA	45 MHz logic signal freq.
3 V/5 V Operation						
For All Models						
Input Currents						
	I _{IA} , I _{IB} , I _{IC} , I _{ID} , I _{E1} , I _{E2}	-10	+0.01	+10	μA	0 V ≤ V _{IA} , V _{IB} , V _{IC} , V _{ID} ≤ V _{DD1} or V _{DD2} , 0 V ≤ V _{E1} , V _{E2} ≤ V _{DD1} or V _{DD2}
Logic High Input Threshold						
5 V/3 V Operation	V _{IH} , V _{EH}	2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold						
5 V/3 V Operation	V _{IL} , V _{EL}			0.8	V	
3 V/5 V Operation					0.4	V
Logic High Output Voltages						
	V _{OAH} , V _{OBH} , V _{OCH} , V _{ODH}	(V _{DD1} or V _{DD2}) - 0.1	(V _{DD1} or V _{DD2})		V	I _{ox} = -20 μA, V _{ix} = V _{ixH}
		(V _{DD1} or V _{DD2}) - 0.4	(V _{DD1} or V _{DD2}) - 0.2		V	I _{ox} = -4 mA, V _{ix} = V _{ixH}
Logic Low Output Voltages						
	V _{OAL} , V _{OBL} , V _{OCL} , V _{ODL}		0.0	0.1	V	I _{ox} = 20 μA, V _{ix} = V _{ixL}
			0.04	0.1	V	I _{ox} = 400 μA, V _{ix} = V _{ixL}
			0.2	0.4	V	I _{ox} = 4 mA, V _{ix} = V _{ixL}
SWITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	50	70	100	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} - t _{PHL} ⁵	PWD			40	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			11		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	C _L = 15 pF, CMOS signal levels
ADuM140xBRW						
Minimum Pulse Width ³	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	15	35	50	ns	C _L = 15 pF, CMOS signal levels

ADuM1400/ADuM1401/ADuM1402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD			3	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew ⁶	t_{PSK}			22	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t_{PSKCD}			3	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t_{PSKOD}			6	ns	$C_L = 15$ pF, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width ³	PW		8.3	11.1	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate ⁴		90	120		Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay ⁵	t_{PHL}, t_{PLH}	20	30	40	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^5$	PWD		0.5	2	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew ⁶	t_{PSK}			14	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t_{PSKCD}			2	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t_{PSKOD}			5	ns	$C_L = 15$ pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	$C_L = 15$ pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	$C_L = 15$ pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F					$C_L = 15$ pF, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output ⁸	$ CM_H $	25	35		kV/μs	$V_{ix} = V_{DD1}$ or V_{DD2} , $V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	$ CM_L $	25	35		kV/μs	$V_{ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current per Channel ⁹	$I_{DDI(D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	$I_{DDO(D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_o < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION¹

4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DD1(Q)}		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	I _{DD0(Q)}		0.19	0.21	mA	
ADuM1400W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		8.6	10.6	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		2.6	3.5	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		7.1	9.0	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		4.1	5.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(Q), I_{DD2(Q)}}		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(10), I_{DD2(10)}}		5.6	7.0	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I _{IA} , I _{IB} , I _{IC} , I _{ID} , I _{E1} , I _{E2}	-10	+0.01	+10	μA	0 ≤ V _{IA} , V _{IB} , V _{IC} , V _{ID} ≤ V _{DD1} or V _{DD2} , 0 ≤ V _{E1} , V _{E2} ≤ V _{DD1} or V _{DD2}
Logic High Input Threshold	V _{IH} , V _{EH}	2.0			V	
Logic Low Input Threshold	V _{IL} , V _{EL}			0.8	V	
Logic High Output Voltages	V _{OAH} , V _{OBH} , V _{OCH} , V _{ODH}	(V _{DD1} or V _{DD2}) - 0.1	5.0		V	I _{Ox} = -20 μA, V _{Ix} = V _{IxH}
		(V _{DD1} or V _{DD2}) - 0.4	4.8		V	I _{Ox} = -4 mA, V _{Ix} = V _{IxH}
Logic Low Output Voltages	V _{OAL} , V _{OBL} , V _{OCL} , V _{ODL}		0.0	0.1	V	I _{Ox} = 20 μA, V _{Ix} = V _{IxL}
			0.04	0.1	V	I _{Ox} = 400 μA, V _{Ix} = V _{IxL}
			0.2	0.4	V	I _{Ox} = 4 mA, V _{Ix} = V _{IxL}
SWITCHING SPECIFICATIONS						
ADuM140xWSRWZ						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	50	65	100	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} - t _{PHL} ⁵	PWD			40	ns	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	C _L = 15 pF, CMOS signal levels

ADuM1400/ADuM1401/ADuM1402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM140xWTRWZ						
Minimum Pulse Width ³	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	18	27	32	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} – t _{PHL} ⁵	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			15	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t _{PSKOD}			6	ns	C _L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t _{PHZ} , t _{PLH}		6	8	ns	C _L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t _{PZH} , t _{PZL}		6	8	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		2.5		ns	C _L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV/μs	V _{ix} = V _{DD1} /V _{DD2} , V _{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM _L	25	35		kV/μs	V _{ix} = 0 V, V _{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f _r		1.2		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI(D)}		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	I _{DDO(D)}		0.05		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_o > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_o < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V, 125°C OPERATION¹

3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DD1(Q)}		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	I _{DD0(Q)}		0.11	0.14	mA	
ADuM1400W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		4.5	6.5	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		1.4	2.0	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		3.7	5.4	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		2.2	3.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(Q), I_{DD2(Q)}}		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} or V _{DD2} Supply Current	I _{DD1(10), I_{DD2(10)}}		3.0	4.2	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I _{IA} , I _{IB} , I _{IC} , I _{ID} , I _{E1} , I _{E2}	-10	+0.01	+10	μA	0 ≤ V _{IA} , V _{IB} , V _{IC} , V _{ID} ≤ V _{DD1} or V _{DD2} , 0 ≤ V _{E1} , V _{E2} ≤ V _{DD1} or V _{DD2}
Logic High Input Threshold	V _{IH} , V _{EH}	1.6			V	
Logic Low Input Threshold	V _{IL} , V _{EL}			0.4	V	
Logic High Output Voltages	V _{OAH} , V _{OBH} , V _{OCH} , V _{ODH}	(V _{DD1} or V _{DD2}) - 0.1 (V _{DD1} or V _{DD2}) - 0.4	3.0 2.8		V	I _{OX} = -20 μA, V _{IX} = V _{IXH} I _{OX} = -4 mA, V _{IX} = V _{IXH}
Logic Low Output Voltages	V _{OAL} , V _{OBL} , V _{OCL} , V _{ODL}		0.0 0.04	0.1 0.1	V	I _{OX} = 20 μA, V _{IX} = V _{IXL} I _{OX} = 400 μA, V _{IX} = V _{IXL}
			0.2	0.4	V	I _{OX} = 4 mA, V _{IX} = V _{IXL}
SWITCHING SPECIFICATIONS						
ADuM140xWSRWZ						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	50	75	100	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} - t _{PHL} ⁵	PWD			40	ns	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	C _L = 15 pF, CMOS signal levels

ADuM1400/ADuM1401/ADuM1402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM140xWTRWZ						
Minimum Pulse Width ³	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	20	34	45	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} – t _{PHL} ⁵	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			22	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t _{PSKOD}			6	ns	C _L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t _{PHZ} , t _{PLH}		6	8	ns	C _L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t _{PZH} , t _{PZL}		6	8	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _r /t _f		3		ns	C _L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV/μs	V _{ix} = V _{DD1} /V _{DD2} , V _{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM _L	25	35		kV/μs	V _{ix} = 0 V, V _{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f _r		1.1		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI(D)}		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	I _{DDO(D)}		0.03		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V, 125°C OPERATION¹

4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 5 V, V_{DD2} = 3.0 V. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DD1(Q)}		0.50	0.53	mA	
Output Supply Current per Channel, Quiescent	I _{DD0(Q)}		0.11	0.14	mA	
ADuM1400W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		8.6	10.6	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		1.4	2.0	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		7.1	9.0	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		2.2	3.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.5	2.1	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		5.6	7.0	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		3.0	4.2	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I _{IA} , I _{IB} , I _{IC} , I _{ID} , I _{E1} , I _{E2}	-10	+0.01	+10	μA	0 ≤ V _{IA} , V _{IB} , V _{IC} , V _{ID} ≤ V _{DD1} or V _{DD2} , 0 ≤ V _{E1} , V _{E2} ≤ V _{DD1} or V _{DD2}
Logic High Input Threshold	V _{IH} , V _{EH}					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V _{IL} , V _{EL}					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V _{OAH} , V _{OBH} , V _{OCH} , V _{ODH}	(V _{DD1} or V _{DD2}) - 0.1	V _{DD1} or V _{DD2}		V	I _{Ox} = -20 μA, V _{Ix} = V _{IxH}
		(V _{DD1} or V _{DD2}) - 0.4	V _{DD1} , V _{DD2} - 0.2		V	I _{Ox} = -4 mA, V _{Ix} = V _{IxH}
Logic Low Output Voltages	V _{OAL} , V _{OBL} , V _{OCL} , V _{ODL}		0.0	0.1	V	I _{Ox} = 20 μA, V _{Ix} = V _{IxL}
			0.04	0.1	V	I _{Ox} = 400 μA, V _{Ix} = V _{IxL}
			0.2	0.4	V	I _{Ox} = 4 mA, V _{Ix} = V _{IxL}
SWITCHING SPECIFICATIONS						
ADuM140xWSRWZ						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	50	70	100	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} - t _{PHL} ⁵	PWD			40	ns	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	C _L = 15 pF, CMOS signal levels

ADuM1400/ADuM1401/ADuM1402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM140xWTRWZ						
Minimum Pulse Width ³	PW			100	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	20	30	40	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} – t _{PHL} ⁵	PWD			3	ns	C _L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			22	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t _{PSKCD}			3	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t _{PSKOD}			6	ns	C _L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t _{PHZ} , t _{PLH}		6	8	ns	C _L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t _{PZH} , t _{PZL}		6	8	ns	C _L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t _R /t _F		3.0		ns	C _L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	CM _H	25	35		kV/μs	V _{ix} = V _{DD1} /V _{DD2} , V _{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	CM _L	25	35		kV/μs	V _{ix} = 0 V, V _{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f _r		1.2		Mbps	
Input Dynamic Supply Current per Channel ⁹	I _{DDI(D)}		0.19		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	I _{DDO(D)}		0.03		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 3 V/5 V, 125°C OPERATION¹

3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5 V. These specifications apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	I _{DD1(Q)}		0.26	0.31	mA	
Output Supply Current per Channel, Quiescent	I _{DDO(Q)}		0.19	0.21	mA	
ADuM1400W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		4.5	6.5	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		2.6	3.5	mA	5 MHz logic signal freq.
ADuM1401W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		3.7	5.4	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		4.1	5.0	mA	5 MHz logic signal freq.
ADuM1402W, Total Supply Current, Four Channels ²						
DC to 2 Mbps						
V _{DD1} Supply Current	I _{DD1(Q)}		0.9	1.5	mA	DC to 1 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(Q)}		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (TRWZ Grade Only)						
V _{DD1} Supply Current	I _{DD1(10)}		3.0	4.2	mA	5 MHz logic signal freq.
V _{DD2} Supply Current	I _{DD2(10)}		5.6	7.0	mA	5 MHz logic signal freq.
For All Models						
Input Currents	I _{IA} , I _{IB} , I _{IC} , I _{ID} , I _{E1} , I _{E2}	-10	+0.01	+10	μA	0 ≤ V _{IA} , V _{IB} , V _{IC} , V _{ID} ≤ V _{DD1} or V _{DD2} , 0 ≤ V _{E1} , V _{E2} ≤ V _{DD1} or V _{DD2}
Logic High Input Threshold	V _{IH} , V _{EH}	1.6			V	
Logic Low Input Threshold	V _{IL} , V _{EL}			0.4	V	
Logic High Output Voltages	V _{OAH} , V _{OBH} , V _{OCH} , V _{ODH}	(V _{DD1} or V _{DD2}) - 0.1	V _{DD1} , V _{DD2}		V	I _{OX} = -20 μA, V _{IX} = V _{IxH}
Logic Low Output Voltages	V _{OAL} , V _{OBL} , V _{OCL} , V _{ODL}	(V _{DD1} or V _{DD2}) - 0.4	V _{DD1} , V _{DD2} - 0.2		V	I _{OX} = -4 mA, V _{IX} = V _{IxH}
			0.0	0.1	V	I _{OX} = 20 μA, V _{IX} = V _{IxL}
			0.04	0.1	V	I _{OX} = 400 μA, V _{IX} = V _{IxL}
			0.2	0.4	V	I _{OX} = 4 mA, V _{IX} = V _{IxL}
SWITCHING SPECIFICATIONS						
ADuM140xWSRWZ						
Minimum Pulse Width ³	PW			1000	ns	C _L = 15 pF, CMOS signal levels
Maximum Data Rate ⁴		1			Mbps	C _L = 15 pF, CMOS signal levels
Propagation Delay ⁵	t _{PHL} , t _{PLH}	50	70	100	ns	C _L = 15 pF, CMOS signal levels
Pulse Width Distortion, t _{PLH} - t _{PHL} ⁵	PWD			40	ns	C _L = 15 pF, CMOS signal levels
Propagation Delay Skew ⁶	t _{PSK}			50	ns	C _L = 15 pF, CMOS signal levels
Channel-to-Channel Matching ⁷	t _{PSKCD} /t _{PSKOD}			50	ns	C _L = 15 pF, CMOS signal levels

ADuM1400/ADuM1401/ADuM1402

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM140xWTRWZ						
Minimum Pulse Width ³	PW			100	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate ⁴		10			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay ⁵	t_{PHL} , t_{PLH}	20	30	40	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁵	PWD			3	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew ⁶	t_{PSK}			22	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁷	t_{PSKCD}			3	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁷	t_{PSKOD}			6	ns	$C_L = 15$ pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ} , t_{PLH}		6	8	ns	$C_L = 15$ pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH} , t_{PZL}		6	8	ns	$C_L = 15$ pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	$C_L = 15$ pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁸	$ CM_H $	25	35		kV/μs	$V_{IX} = V_{DD1}/V_{DD2}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁸	$ CM_L $	25	35		kV/μs	$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current per Channel ⁹	$I_{DDI(D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current per Channel ⁹	$I_{DDO(D)}$		0.05		mA/Mbps	

¹ All voltages are relative to their respective ground.

² The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate may be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1400W/ADuM1401W/ADuM1402W channel configurations.

³ The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

⁴ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁵ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

⁶ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁷ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁸ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁹ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 8.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output) ¹	R _{I-O}		10 ¹²		Ω	f = 1 MHz
Capacitance (Input-to-Output) ¹	C _{I-O}		2.2		pF	
Input Capacitance ²	C _i		4.0		pF	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 1	θ _{JCI}		33		°C/W	
IC Junction-to-Case Thermal Resistance, Side 2	θ _{JCO}		28		°C/W	

¹ Device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM140x are approved by the organizations listed in Table 9. Refer to Table 14 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 9.

UL	CSA	VDE	TÜV
Recognized under 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ²	Approved according to: IEC 61010-1:2001 (2 nd Edition), EN 61010-1:2001 (2 nd Edition) UL 61010-1:2004 CSA C22.2.61010.1:2005
Double/reinforced insulation, 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak	Reinforced insulation, 400 V rms maximum working voltage
File E214100	File 205078	File 2471900-4880-0001	Certificate U8V 05 06 56232 002

¹ In accordance with UL 1577, each ADuM140x is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).

² In accordance with DIN V VDE V 0884-10, each ADuM140x is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 10.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

ADuM1400/ADuM1401/ADuM1402

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 11.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A After Environmental Tests Subgroup 1 After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC $V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC	V_{PR}	896 672	V peak V peak
Highest Allowable Overvoltage Safety-Limiting Values	Transient overvoltage, $t_{TR} = 10$ seconds Maximum value allowed in the event of a failure (see Figure 4)	V_{TR}	4000	V peak
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	265	mA
Side 2 Current		I_{S2}	335	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	>10 ⁹	Ω

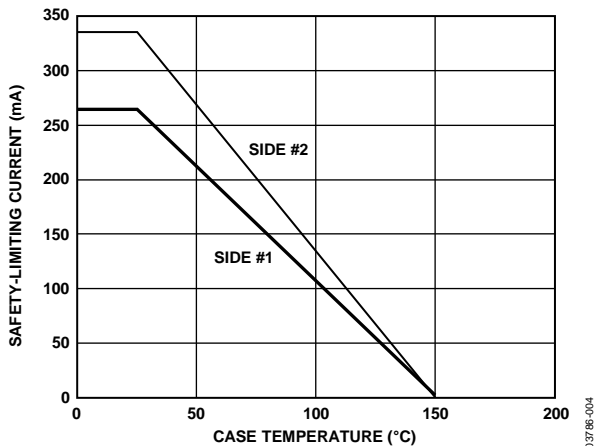


Figure 4. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN VVDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 12.

Parameter	Rating
Operating Temperature (T_A) ¹	-40°C to +105°C
Operating Temperature (T_A) ²	-40°C to +125°C
Supply Voltages (V_{DD1} , V_{DD2}) ^{1, 3}	2.7 V to 5.5 V
Supply Voltages (V_{DD1} , V_{DD2}) ^{2, 3}	3.0 V to 5.5 V
Input Signal Rise and Fall Times	1.0 ms

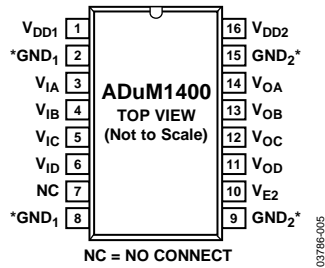
¹ Does not apply to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

² Applies to ADuM1400W, ADuM1401W, and ADuM1402W automotive grade versions.

³ All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ADuM1400/ADuM1401/ADuM1402

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

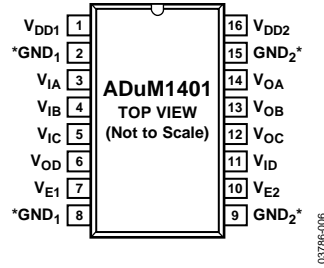


*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND₁ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND₂ IS RECOMMENDED.

Figure 5. ADuM1400 Pin Configuration

Table 16. ADuM1400 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	GND ₁	Ground 1. Ground reference for Isolator Side 1.
3	V _{IA}	Logic Input A.
4	V _{IB}	Logic Input B.
5	V _{IC}	Logic Input C.
6	V _{ID}	Logic Input D.
7	NC	No Connect.
8	GND ₁	Ground 1. Ground reference for Isolator Side 1.
9	GND ₂	Ground 2. Ground reference for Isolator Side 2.
10	V _{E2}	Output Enable 2. Active high logic input. V _{OA} , V _{OB} , V _{OC} , and V _{OD} outputs are enabled when V _{E2} is high or disconnected. V _{OA} , V _{OB} , V _{OC} , and V _{OD} outputs are disabled when V _{E2} is low. In noisy environments, connecting V _{E2} to an external logic high or low is recommended.
11	V _{OD}	Logic Output D.
12	V _{OC}	Logic Output C.
13	V _{OB}	Logic Output B.
14	V _{OA}	Logic Output A.
15	GND ₂	Ground 2. Ground reference for Isolator Side 2.
16	V _{DD2}	Supply Voltage for Isolator Side 2.



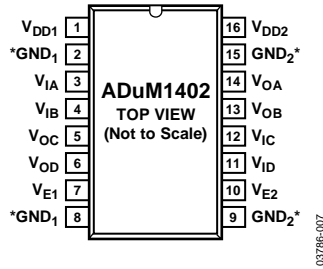
*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND₁ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND₂ IS RECOMMENDED.

Figure 6. ADuM1401 Pin Configuration

Table 17. ADuM1401 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	GND ₁	Ground 1. Ground reference for Isolator Side 1.
3	V _{1A}	Logic Input A.
4	V _{1B}	Logic Input B.
5	V _{1C}	Logic Input C.
6	V _{OD}	Logic Output D.
7	V _{E1}	Output Enable 1. Active high logic input. V _{OD} output is enabled when V _{E1} is high or disconnected. V _{OD} is disabled when V _{E1} is low. In noisy environments, connecting V _{E1} to an external logic high or low is recommended.
8	GND ₁	Ground 1. Ground reference for Isolator Side 1.
9	GND ₂	Ground 2. Ground reference for Isolator Side 2.
10	V _{E2}	Output Enable 2. Active high logic input. V _{OA} , V _{OB} , and V _{OC} outputs are enabled when V _{E2} is high or disconnected. V _{OA} , V _{OB} , and V _{OC} outputs are disabled when V _{E2} is low. In noisy environments, connecting V _{E2} to an external logic high or low is recommended.
11	V _{ID}	Logic Input D.
12	V _{OC}	Logic Output C.
13	V _{OB}	Logic Output B.
14	V _{OA}	Logic Output A.
15	GND ₂	Ground 2. Ground reference for Isolator Side 2.
16	V _{DD2}	Supply Voltage for Isolator Side 2.

ADuM1400/ADuM1401/ADuM1402



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND₁ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED, AND CONNECTING BOTH TO GND₂ IS RECOMMENDED.

Figure 7. ADuM1402 Pin Configuration

Table 18. ADuM1402 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	GND ₁	Ground 1. Ground reference for Isolator Side 1.
3	V _{1A}	Logic Input A.
4	V _{1B}	Logic Input B.
5	V _{0C}	Logic Output C.
6	V _{0D}	Logic Output D.
7	V _{E1}	Output Enable 1. Active high logic input. V _{0C} and V _{0D} outputs are enabled when V _{E1} is high or disconnected. V _{0C} and V _{0D} outputs are disabled when V _{E1} is low. In noisy environments, connecting V _{E1} to an external logic high or low is recommended.
8	GND ₁	Ground 1. Ground reference for Isolator Side 1.
9	GND ₂	Ground 2. Ground reference for Isolator Side 2.
10	V _{E2}	Output Enable 2. Active high logic input. V _{0A} and V _{0B} outputs are enabled when V _{E2} is high or disconnected. V _{0A} and V _{0B} outputs are disabled when V _{E2} is low. In noisy environments, connecting V _{E2} to an external logic high or low is recommended.
11	V _{1D}	Logic Input D.
12	V _{1C}	Logic Input C.
13	V _{0B}	Logic Output B.
14	V _{0A}	Logic Output A.
15	GND ₂	Ground 2. Ground reference for Isolator Side 2.
16	V _{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

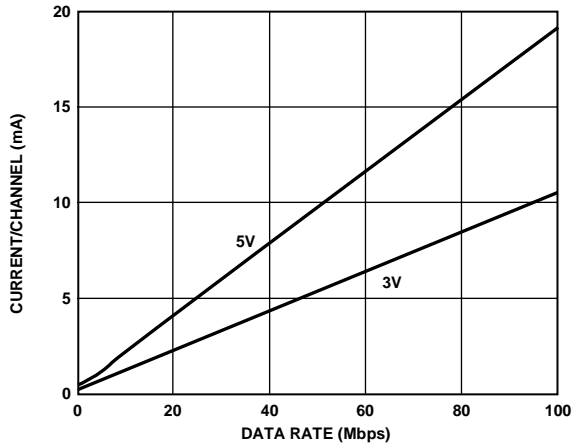


Figure 8. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

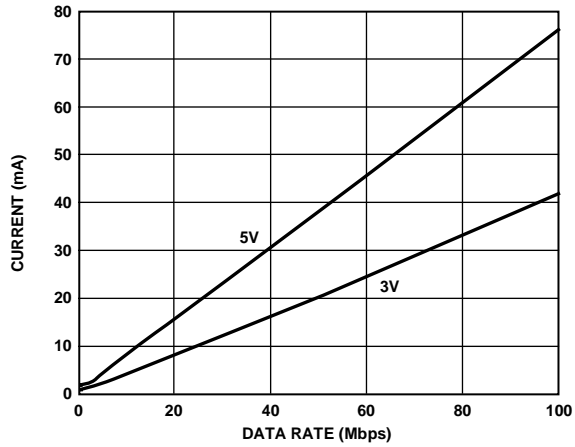


Figure 11. Typical ADuM1400 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

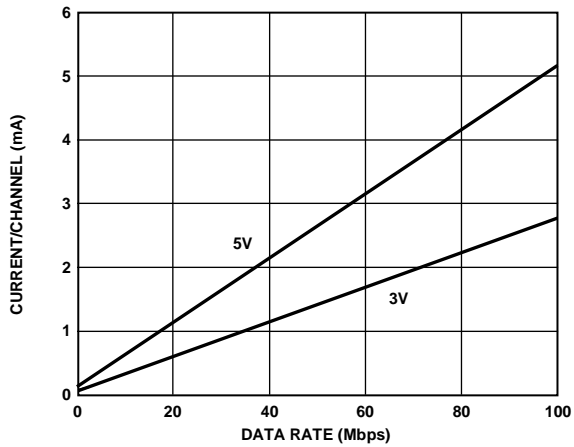


Figure 9. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

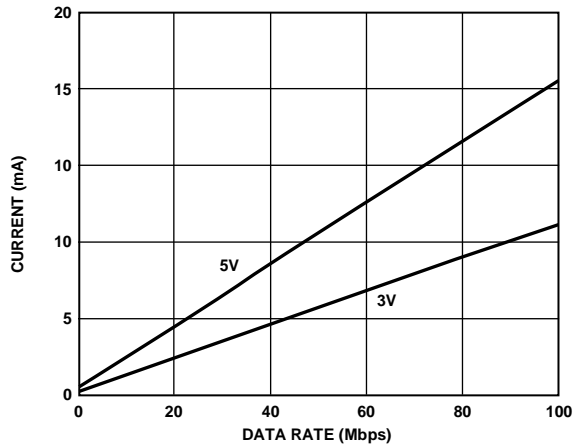


Figure 12. Typical ADuM1400 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

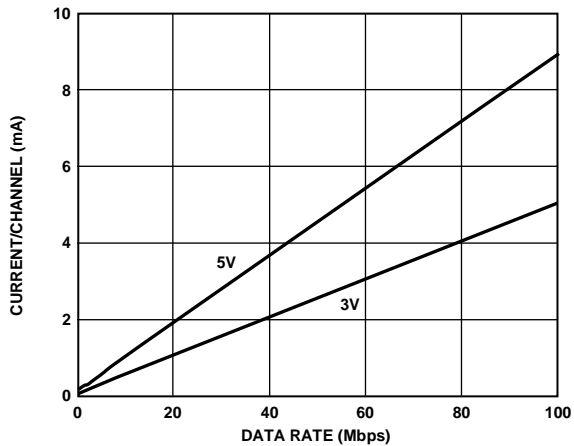


Figure 10. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

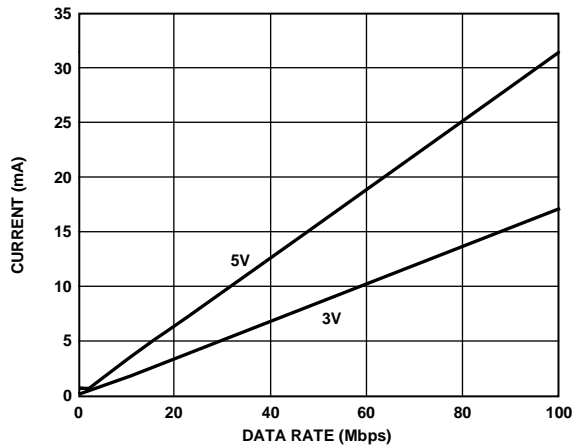


Figure 13. Typical ADuM1401 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

ADuM1400/ADuM1401/ADuM1402

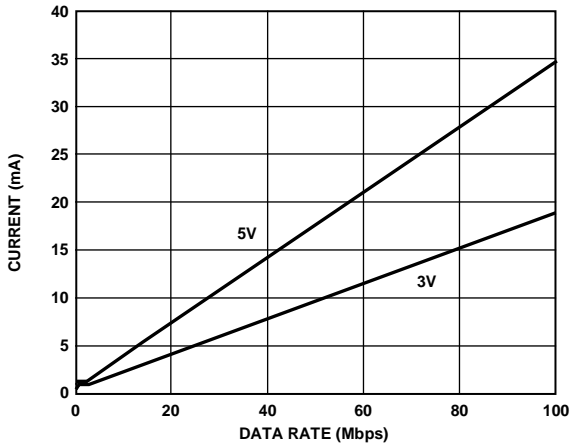


Figure 14. Typical ADuM1401 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

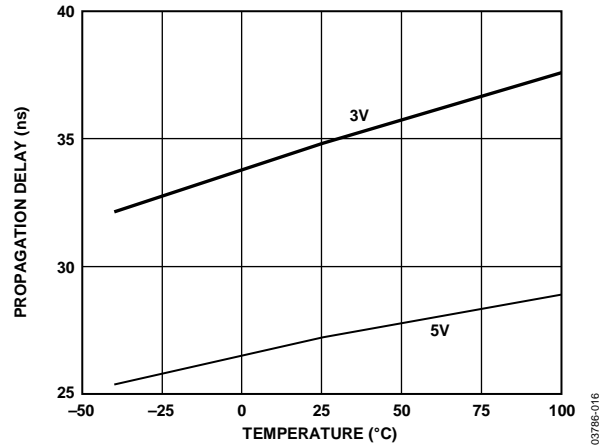


Figure 16. Propagation Delay vs. Temperature, C Grade

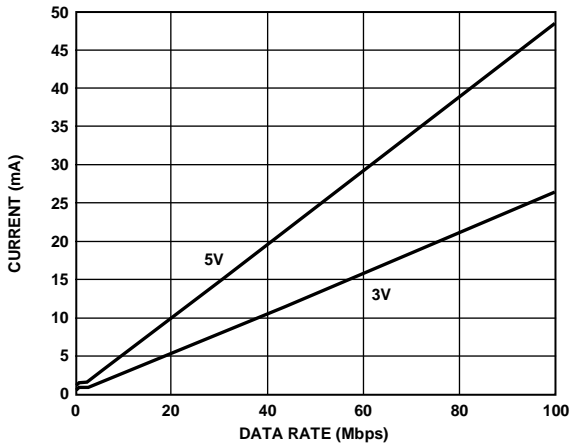


Figure 15. Typical ADuM1402 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

03786-014

03786-016

03786-015

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM140x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 μF and 0.1 μF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered, unless the ground pair on each package side is connected close to the package.

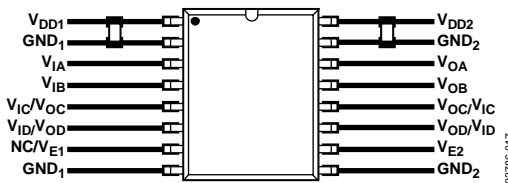


Figure 17. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

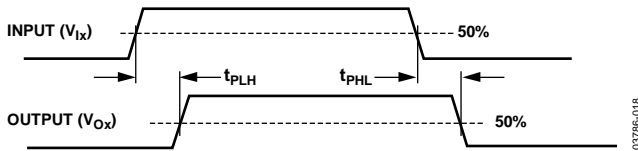


Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM140x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM140x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 μs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 15) by the watchdog timer circuit.

The limitation on the magnetic field immunity of the ADuM140x is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM140x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum r_n^2; n = 1, 2, \dots, N$$

where:

β is magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the n^{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM140x and an imposed requirement that the induced voltage be 50% at most of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.

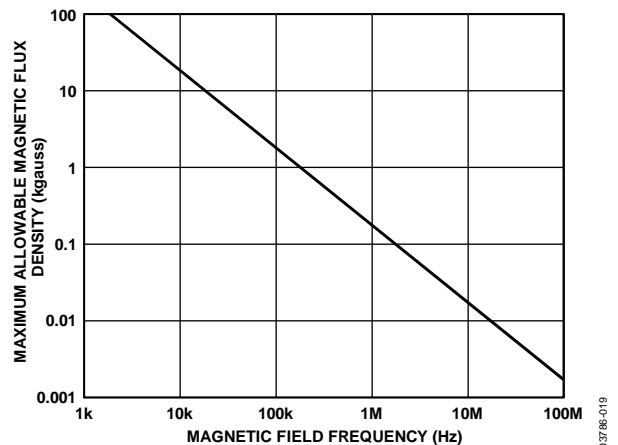


Figure 19. Maximum Allowable External Magnetic Flux Density

ADuM1400/ADuM1401/ADuM1402

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and has the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM140x transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM140x is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM140x to affect the operation of the component.

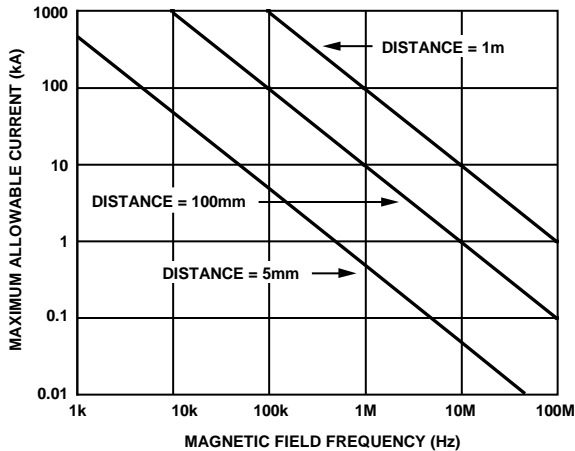


Figure 20. Maximum Allowable Current for Various Current-to-ADuM140x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM140x isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5 f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5 f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 8 and Figure 9 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 10 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 15 provide total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM1400/ADuM1401/ADuM1402 channel configurations.

NOTES

NOTES