Simultaneous Sampling Video Rate Codec

ADV7202

FEATURES

- Four 10-Bit Video DACs (4:2:2, YCrCb, RGB I/P Supported)
- 10-Bit Video Rate Digitization at up to 54 MHz
- AGC Control (±6 dB)
- Front End 3-Channel Clamp Control
- Up to Five CVBS Input Channels, Two Component YUV, Three S-Video, or a Combination of the Above. Simultaneous Digitization of Two CVBS Input Channels
- Aux 8-Bit SAR ADC @ 843 kHz Sampling Giving up to Eight General-Purpose Inputs
- I^2C Compatible Interface with I^2C Filter
- RGB Inputs for Picture-on-Picture of the RGB DACs
- Optional Internal Reference
- Power Save Mode

APPLICATIONS

- Picture-on-Picture Video Systems
- Simultaneous Video Rate Processing
- Hybrid Set-Top Box TV Systems
- Direct Digital Synthesis/I-Q Demodulation
- Image Processing

GENERAL DESCRIPTION

The ADV7202 is a video rate sampling codec.

It has the capability of sampling up to five NTSC/PAL/SECAM video I/P signals. The resolution on the front end digitizer is 12 bits; 2 bits (12 dB) are used for gain and offset adjustment. The digitizer has a conversion rate of up to 54 MHz.

The ADV7202 can have up to eight auxiliary inputs that can be sampled by an 843 kHz SAR ADC for system monitoring.

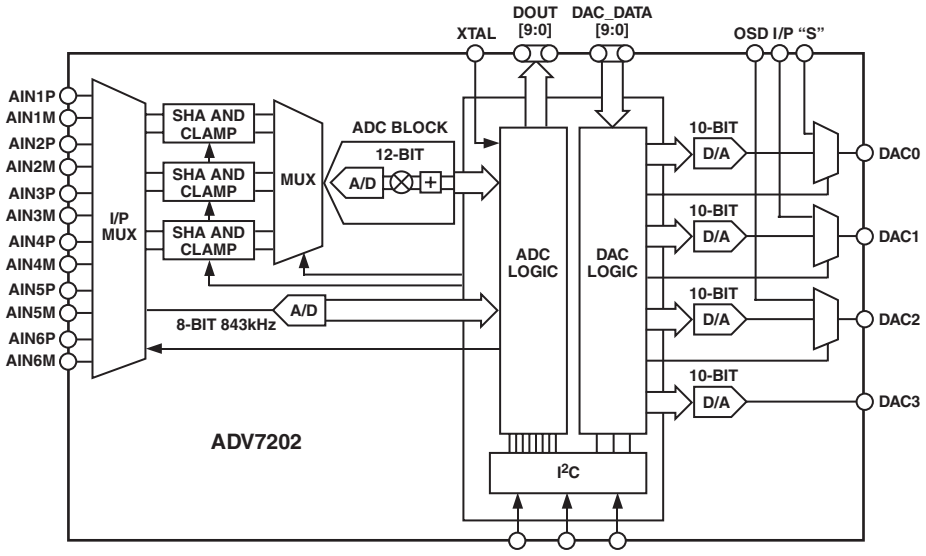
The back end consists of four 10-bit DACs that run at up to 200 MHz and can be used to output CVBS, S-Video, Component YCrCb, and RGB.

This codec also supports Picture-on-Picture.

The ADV7202 can operate at 3.3 V or 5 V. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7202 is packaged in a small 64-lead LQFP package.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

ADV7202–SPECIFICATIONS

5 V SPECIFICATIONS (AVDD/DVDD = 5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE_DAC					
Resolution (Each DAC)		10		Bits	
Accuracy (Each DAC)		10		Bits	
Integral Nonlinearity		±0.6		LSB	10-Bit Operation
Differential Nonlinearity	–1.5	–0.6/0.1	+0.5	LSB	10-Bit Operation
VIDEO ADC					
Resolution		12		Bits	(Including 2 Bits for Gain Ranging) 2.2 V Ref.
Accuracy		12		Bits	
Integral Nonlinearity		±2.5		LSB	12 Bit
Differential Nonlinearity		±0.7		LSB	12 Bit
Input Voltage Range[2]	$-V_{REFADC}$		$+V_{REFADC}$		
SNR		62		dB	27 MHz Clock
		57		dB	54 MHz Clock
AUX ADC					
Resolution		8		Bits	
Differential Nonlinearity		±0.4		LSB	Guaranteed No Missing Codes
Integral Nonlinearity		±0.4		LSB	
Input Voltage Range	0		2 V_{REFADC}	V	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Leakage Current, I_{IN}			±2	μA	
Input Capacitance, C_{IN}		6		pF	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 1.6 mA
Three-State Leakage Current			10	μA	
Output Capacitance		10		pF	
Digital Output Access Time, t_{14}		6		ns	See Figure 13
Digital Output Hold Time, t_{15}		5		ns	
ANALOG OUTPUTS					
Output Current Range	4.10	4.33	4.6	mA	R_{SET} = 1.2 kΩ, R_L = 300 Ω
DAC-to-DAC Matching		3		%	
Output Compliance, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		50		kΩ	
Output Capacitance, C_{OUT}		30		pF	I_{OUT} = 0 mA
Analog Output Delay[3]		5.5		ns	
DAC Output Skew		0.06		ns	
VOLTAGE REFERENCE					
Reference Range, V_{REFDAC}	1.17	1.235	1.30	V	
Reference Range, V_{REFADC}	2.1	2.2	2.30	V	Programmable 1.1 V or 2.2 V
Reference Range, V_{REFADC}		1.1		V	

NOTES
[1]0°C to 70°C.
[2]SHA gain = 1, half range for SHA gain = 2, see Table II.
[3]Output delay measured from 50% of the rising edge of the clock to the 50% point of full-scale transition.

Specifications subject to change without notice.

5 V SPECIFICATIONS (AVDD/DVDD = 5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
POWER REQUIREMENTS[1]					
AVDD/DVDD	4.75	5	5.25	V	
Normal Power Mode					
I_{DAC}[2]			22	mA	R_{SET} = 1.2 kΩ, R_L = 300 Ω
I_{DSC}[3]			12	mA	Inputs at Supply
I_{ADC}[4]		95	115	mA	Max Power YUV Mode
I_{ADC}[4]		65		mA	CVBS Input Mode
Sleep Mode Current[5]		400		µA	
Power-Up Time		4		ms	Internal Reference
MPU PORT[6]—I^2C					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period the first clock is generated.
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	

NOTES
[1]All DACs and ADCs on.
[2]I_{DAC} is the DAC supply current.
[3]I_{DSC} is the digital core supply current.
[4]I_{ADC} is the ADC supply current.
[5]This includes I_{ADC}, I_{DAC}, and I_{DSC}.
[6]Guaranteed by characterization.

Specifications subject to change without notice.

ADV7202–SPECIFICATIONS

5 V SPECIFICATIONS (AVDD/DVDD = 4.75 V – 5.25 V, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Condition[2]
PROGRAMMABLE GAIN AMPLIFIER					
Video ADC Gain	–6		+6	dB	Setup Conditions
CLAMP CIRCUITRY[3]					
Clamp Fine Source/Sink Current		4.0		μA	
Clamp Coarse Source/Sink Current		0.8		mA	
CLOCK CONTROL[4]					
DACCLK0/DACCLK1		27		MHz	Dual CLK Dual Edge Mode
DACCLK1[5, 6, 7]			200	MHz	Single Edge Single Clock Mode
DACCLK1		27		MHz	4:2:2 Mode
Data Setup Time, t_{12}[7]	1.5			ns	All Input Modes
Data Hold Time, t_{13}[7]	1.5			ns	
Min Clock High Time, t_{10}[7]		1.5		ns	
Min Clock Low Time, t_{11}[7]		1.5		ns	
Pipeline Delay[8]					
Video ADC		4		Clock Cycles	
RESET CONTROL					
$\overline{\text{RESET}}$ Low Time		10		ns	

NOTES

[1]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[2]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range.

[3]External clamp capacitor = 0.1 μF.

[4]TTL input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF.

[5]Maximum clock speed determined by setup and hold conditions.

[6]Single DAC only.

[7]Guaranteed by characterization.

[8]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Specifications subject to change without notice.

3.3 V SPECIFICATIONS (AVDD/DVDD = 3.3 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE_DAC					
Resolution (Each DAC)		10		Bits	
Accuracy (Each DAC)		10		Bits	
Integral Nonlinearity		±1		LSB	10-Bit Operation
Differential Nonlinearity		–0.8/0.1		LSB	10-Bit Operation
VIDEO ADC					
Resolution		12		Bits	(Including 2 Bits for Gain Ranging) 2.2 V Ref.
Accuracy		12		Bits	
Integral Nonlinearity		±4		LSB	12 Bit
Differential Nonlinearity		±1		LSB	12 Bit
Differential Input Voltage Range[2]	$-V_{REFADC}$		$+V_{REFADC}$		See Table II
SNR		60		dB	27 MHz Clock, f_{IN} = 100 kHz
		55		dB	54 MHz Clock
AUX ADC					
Resolution		8		Bits	
Differential Nonlinearity		±0.5		LSB	
Integral Nonlinearity		±0.5		LSB	
Input Voltage Range	0		2 V_{REFADC}	V	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}		±1		μA	
Input Capacitance, C_{IN}		10		pF	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 1.6 mA
Three-State Leakage Current		10		μA	
Output Capacitance		10		pF	
Digital Output Access Time, t_{14}		6		ns	See Figure 13
Digital Output Hold Time, t_{15}		5		ns	
ANALOG OUTPUTS					
Output Current		4.33		mA	R_{SET} = 1.2 kΩ, R_L = 300 Ω
DAC-to-DAC Matching		4		%	DAC 0, 1, and 2
Output Compliance, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		50		kΩ	
Output Capacitance, C_{OUT}		30		pF	I_{OUT} = 0 mA
Analog Output Delay[3]		5.5		ns	
DAC Output Skew		0.06		ns	
VOLTAGE REFERENCE					
Reference Range, V_{REFADC}		1.100		V	
Reference Range, V_{REFDAC}		1.235		V	

NOTES
[1]0°C to 70°C.
[2]SHA gain = 1, half range for SHA gain = 2, see Table II.
[3]Output delay measured from 50% of the rising edge of the clock to the 50% point of full-scale transition.

Specifications subject to change without notice.

ADV7202–SPECIFICATIONS

3.3 V SPECIFICATIONS (AVDD/DVDD = 3.3 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
POWER REQUIREMENTS[1]					
AVDD/DVDD	3.14	3.3	3.46	V	
Normal Power Mode					
I_{DAC}[2]		18		mA	
I_{DSC}[3]		8		mA	Inputs at Supply
I_{ADC}[4]		80		mA	
Sleep Mode Current[5]		350		µA	
Power-Up Time		4		ms	Internal Reference
MPU PORT[6]—I^2C					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period, the first clock is generated.
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	

NOTES
[1]All DACs and ADCs on.
[2]I_{DAC} is the DAC supply current.
[3]I_{DSC} is the digital core supply current.
[4]I_{ADC} is the ADC supply current.
[5]This includes I_{ADC}, I_{DAC}, and I_{DSC}.
[6]Guaranteed by characterization.

Specifications subject to change without notice.

3.3 V SPECIFICATIONS (AVDD/DVDD = 3.3 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Condition[2]
PROGRAMMABLE GAIN AMPLIFIER					
Video ADC Gain	–6		+6	dB	
CLAMP CIRCUITRY[3]					
Clamp Fine Source/Sink Current		4		µA	Up/Down
Clamp Coarse Source/Sink Current		0.8		mA	Up/Down
CLOCK CONTROL[4]					
DACCLK0/DACCLK1		27		MHz	Dual CLK Dual Edge Mode
DACCLK1[5, 6, 7]		180		MHz	Single Edge Single Clock Mode
DACCLK1[7]		27		MHz	4:2:2 Mode
Data Setup Time, t_{12}		2		ns	All Input Modes
Data Hold Time, t_{13}		2		ns	
Min Clock High Time, t_{10}[7]		3		ns	
Min Clock Low Time, t_{11}[7]		3		ns	
Pipeline Delay[8]					
Video ADC		4		Clock Cycles	
RESET CONTROL					
$\overline{\text{RESET}}$ Low Time		10		ns	

NOTES
[1]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[2]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range.
[3]External clamp capacitor = 0.1 µF.
[4]TTL input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF.
[5]Maximum clock speed determined by setup and hold conditions.
[6]Single DAC only.
[7]Guaranteed by characterization.
[8]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

AVDD to AVSS . . . . . 7 V
DVDD to DVSS . . . . . 7 V
Ambient Operating Temperature (T_A) . . . . . 0°C to 70°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . 150°C
Lead Temperature (Soldering, 10 secs) . . . . . 300°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
I_{OUT} to GND[2] . . . . . 0 V to V_{AA}

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanen t damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Analog output short circuit to any power supply or common can be of an indefinite duration.

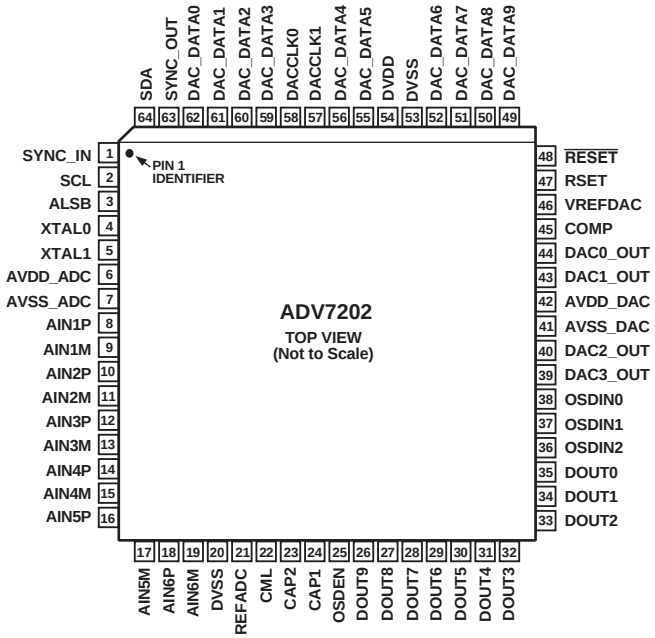
ORDERING INFORMATION

Model	Temperature Range	Package Description	Package Option
ADV7202	0°C to 70°C	64-Lead Plastic Quad Flatpack (LQFP)	ST-64

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7202 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Input/ Output	Function
1	SYNC_IN	I	This signal can be used to synchronize the updating of clamps. Polarity is programmable via I^2C.
2	SCL	I	MPU Port Serial Interface Clock Input
3	ALSB	I	This signal sets up the LSB of the MPU address. MPU address = 2cH, ALSB = 0, MPU address = 2eH, ALSB = 1. When this pin is tied high, the I^2C filter is activated, which reduces noise on the I^2C interface. When this pin is tied low, the input bandwidth on the I^2C lines is increased.
4	XTAL0	I	Input terminal for crystal oscillator or connection for external oscillator with CMOS-compatible square wave clock signal.
5	XTAL1	O	Second Terminal for Crystal Oscillator. Not connected if external clock source is used.
6	AVDD_ADC	P	ADC Supply Voltage (5 V or 3.3 V)
7	AVSS_ADC	G	Ground for ADC Supply
8–19	AIN1–AIN6	I	Analog Signal Inputs. Can be configured differentially or single-ended.
20	DVSS	G	Ground for Digital Core Supply
21	REFADC	I/O	Voltage Reference Input or Programmable Reference Out.
22	CML	O	Common-Mode Level for ADCs. Connect a 0.1 μF capacitor from CML pin to AVSS_ADC.
23, 24	CAP2, CAP1	I	ADC Capacitor Network. Connect a 0.1 μF capacitor from each CAP pin to AVSS_ADC and a 10 μF capacitor across the two CAP pins.
25	OSDEN	I	Enable data from OSDIN0–OSDIN2 to be switched to the outputs when set to a logic high.
26–35	DOUT[9:0]	O	ADC Data Output
36	OSDIN2	I	Third Input Channel for On-Screen Display
37	OSDIN1	I	Second Input Channel for On-Screen Display
38	OSDIN0	I	First Input Channel for On-Screen Display
39	DAC3_OUT	O	General-Purpose Analog Output
40	DAC2_OUT	O	Analog Output. Can be used to output CVBS, R, or U.
41	AVSS_DAC	G	Ground for DAC Supply
42	AVDD_DAC	P	DAC Supply Voltage (5 V or 3.3 V)
43	DAC1_OUT	O	Analog Output. Can be used to output CVBS, Y, G, or Luma.
44	DAC0_OUT	O	Analog Output. Can be used to output CVBS, V, B, or Chroma.
45	COMP	O	Compensation pin for DACs. Connect 0.1 μF capacitor from COMP pin to AVDD_DAC.
46	VREFDAC	I/O	DAC Voltage Reference Output Pin, Nominally 1.235 V. Can be driven by an external voltage reference.
47	RSET	I	Used to control the amplitude of the DAC output current, 1200 Ω resistor gives an I max of 4.33 mA.
48	$\overline{\text{RESET}}$	I	Master Reset (Asynchronous)
49–52, 55, 56, 59–62	DAC_DATA[9:0]	I	DAC Input Data for Four Video Rate DACs
53	DVSS	G	Ground for Digital Core Supply
54	DVDD	P	Supply Voltage for Digital Core (5 V or 3.3 V)
57, 58	DACCLK[1:0]	I	DAC Clocks
63	SYNC_OUT	O	Output Sync Signal, which goes to a high state while Cr data sample from a YCrCb data stream or C data from a Y/C data stream is output on DOUT[9:0].
64	SDA	I/O	MPU Port Serial Data Input/Output

FUNCTIONAL DESCRIPTION

Analog Inputs

The ADV7202 has the capability of sampling up to five CVBS video input signals, two component YUV, or three S-Video inputs. Eight auxiliary general-purpose inputs are also available. Table I shows the analog signal input options available and programmable by I^2C. When configured for auxiliary input mode, the CVBS inputs are single-ended with the second differential input internally set to VREFADC. The resolution on the front end digitizer is 12 bits; 2 bits (12 dB) are used for gain and offset adjustment. The digitizer has a conversion rate of up to 54 MHz. The eight auxiliary inputs can be used for system monitoring, etc. and are sampled by an 843 kHz* SAR ADC. The analog input signal range will be dependent on the value of VREFADC and the SHA gain see (Table II). Three on-screen display inputs OSDIN[2:0] mux to the DAC outputs to enable support for Picture-on-Picture applications.

Table I. Analog Input Signal Data

Register Setting	Description	SHA Used	Sync_Out
0000	CVBS in on AIN1	0	Figure 1
0001	CVBS in on AIN2	0	Figure 1
0010	CVBS in on AIN3	1	Figure 1
0011	Reserved	1	
0100	CVBS in on AIN5	0	Figure 1
0101	CVBS in on AIN6	2	Figure 1
0110	Y/C, Y on AIN1, C on AIN4	0, 1	Figure 2
0111	Y/C, Y on AIN2, C on AIN3	0, 1	Figure 2
1000	YUV, Y on AIN2, U on AIN3, V on AIN6	0, 1, 2	Figure 3
1001	CVBS on AIN1 and 8 AUX. I/Ps AIN3–AIN6*.	0	Figure 1
1010	CVBS on AIN2 and 8 AUX. I/Ps AIN3–AIN6*.	0	Figure 1

*AUX inputs are single-ended. All other inputs are differential.

Table II. Analog Input Signal Range

I/P Mode	V_{REFOUT} (V)	SHA Gain	Input Range (V) Min	Max
Differential	2.2	1	–2.2	+2.2
Differential	2.2	2	–1.1	+1.1
Differential	1.1	1	–1.1	+1.1
Differential	1.1	2	–0.55	+0.55
Single-Ended	2.2	1	0	4.4
Single-Ended	2.2	2	1.1	3.3
Single-Ended	1.1	1	0	2.2
Single-Ended	1.1	2	0.55	1.65

Digital Inputs

The DAC digital inputs on the ADV7202 [9:0] are TTL compatible. Data may be latched into the device in three different modes, programmable via I^2C.

DAC Mode 1, single clock, single edge (see Figure 10) uses only the rising edge of DACCLK1 to latch data into the device. DACCLK0 is a data line that goes high to indicate that the data is for DAC0. Subsequent data-words go to the next DAC in sequence.

DAC Mode 2, dual edge, dual clock (see Figure 11) clocks data in on both edges of DACCLK0 and DACCLK1. Using this option, data can be latched into the device at four times the clock speed. All four DACs are used in this mode.

DAC Mode 3, 4:2:2 mode (see Figure 12). Using this option, 4:2:2 video data is latched in using DACCLK1, while DACCLK0 is used as a data line that is brought to a high state when Cr data is input; hence Y will appear on DAC1, Cr on DAC2, and Cb on DAC0.

Analog Outputs

Analog outputs [DAC0–DAC3] consist of four 10-bit DACs that run at up to 54 MHz or up to 200 MHz if only DAC0 is used. These outputs can be used to output CVBS, S-Video, Component YCrCb, and RGB.

Digital Outputs

Video data will be clocked out on DOUT[9:0] on the rising edge of XTAL0 (see Figure 13). Auxiliary data can be read out via I^2C compatible MPU port.

I^2C Control

I^2C operation allows both reading and writing of system registers. Its operation is explained in detail in the MPU Port Description section.

*Fclk/32, 843 kHz for nominal 27 MHz

VIDEO CLAMPING AND AGC CONTROL

When analog signal clamping is required, the input signal should be ac-coupled to the input via a capacitor, the clamping control is via the MPU port. The AGC is implemented digitally. For correct operation, the user must program the clamp value to which the signal has been clamped into the ADV7202 I^2C Register. This allows the user to specify which signal level is unaffected by the AGC. The digital output signal will be a function of the *ADC* output, the *AGC Gain,* and the *Clamp Level* and can be represented as follows:

$$D_{OUT} = AGC\ Gain \times \left[ADC\_DATA - Clamp\ Level\right] + Clamp\ Level \quad (1)$$

D_{OUT} will be a 10-bit number (0–1023), the *AGC Gain* defaults to 2 and can have a value between 0 to 7.99. The *Clamp Level* is a 10-bit number (0–1023) equal to the 7-bit I^2C value × 16 (Clamp Level CR06-CR00); the ADC value can be regarded as a 10-bit number (0–1023) for the equation. It should be noted that the ADC resolution is 12 bits. The above equation is used to give a basic perspective and is mathematically correct.

When the clamps are operational, Equation 1 shows how the ADV7202 ensures that the level to which the user is clamping is unaffected by the AGC loop. When no clamps are operational, the operation should be regarded as a straightforward gain-and-level shift.

Equation 1 maps the ADC input voltage range to its output.

AGC Gain

The AGC gain can be set to a value from 0 to 7.99. The AGC Gain Register holds a 12-bit number that corresponds to the required gain. The first three MSBs hold the gain integer value while the remaining nine bits hold the gain fractional value. The new AGC multiplier is latched when the MSB register is written to. Example: The user requires a gain of 3.65.

The first three bits give the integer value 3, hence these will be set to '011.' The remaining nine bits will have to be set to give the fractional value 0.65, 512 × 0.65 = 333 = '101001101.' From Equation 2 it can be seen that the *Clamp Level* is subtracted from the signal before *AGC* is applied and then added on again afterwards; hence, if the *AGC Gain* is set to a value of one, the result would be as follows:

(*AGC Gain* = 1)

$$D_{OUT} = ADC\_DATA - Clamp\ Level + Clamp\ Level = ADC\_Data \quad (2)$$

FUNCTIONAL DESCRIPTION

Clamp and AGC Control

The ADV7202 has a front end 3-channel clamp control. To perform an accurate AGC gain operation, it is necessary to know to what level the user is clamping the black level; this value is programmable in Clamp Register 0 CR00–CR06. Each channel has a fine and coarse clamp; the clamp direction and its duration are programmable. Synchronization of the clamps and AGC to the input signal is possible using the SYNC_IN control pin and setting mode Register CR14 to Logic Level "1." Using this method, it is possible to ensure that AGC and clamping are only applied outside the active video area.

Control Signals

The function and operation of the SYNC_IN signal is described in the Clamp and AGC Control section. The SYNC_OUT will go high while Cr data from a YCrCb data stream or C data from a Y/C data stream has been output on DOUT[9:0] (see Figures 1 to 3).

I^2C Filter

A selectable internal I^2C filter allows significant noise reduction on the I^2C interface. In setting ALSB high, the input bandwidth on the I^2C lines is reduced and pulses of less than 50 ns are not passed to the I^2C controller. Setting ALSB low allows greater input bandwidth on the I^2C lines.

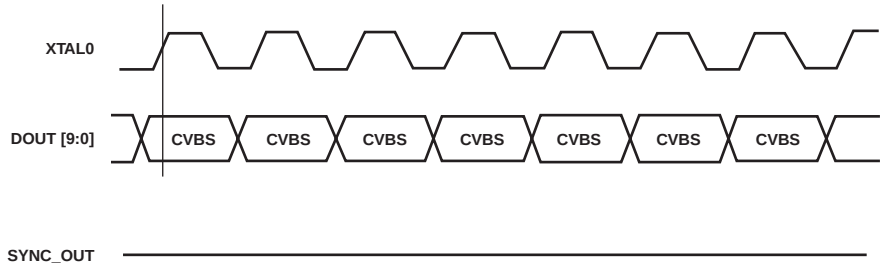


Figure 1. SYNC_OUT Output Timing, CVBS Input

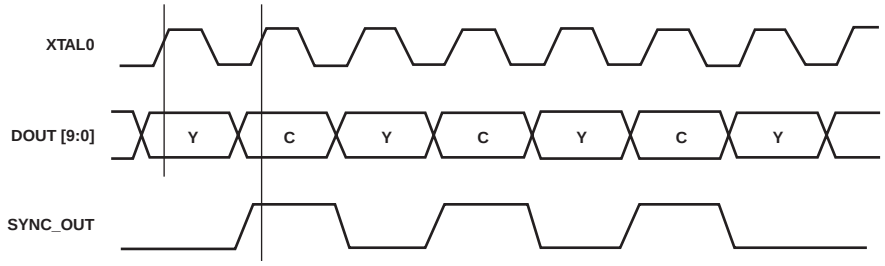


Figure 2. SYNC_OUT Output Timing, Y/C (S-VIDEO) Input

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