

ADP2300/ADP2301

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN	-0.3 V to +28 V
SW	-1.0 V to +28 V
BST to SW	-0.6 V to +6 V
BST	-0.3 V to +28 V
FB	-0.3 V to +3.3 V
Operating Junction Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to GND.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance¹

Package Type	θ_{JA}	θ_{JC}	Unit
6-Lead TSOT	186.02	66.34	°C/W

¹ θ_{JA} and θ_{JC} are measured using natural convection on a JEDEC 4-layer board.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

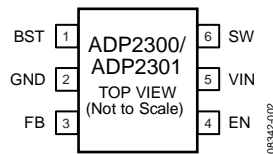


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST	Boost Supply for the High-Side MOSFET Driver. A 0.1 μF capacitor is connected between the SW and BST pins to form a floating supply to drive the gate of the MOSFET switch above the V_{IN} supply voltage.
2	GND	Ground. Connect this pin to the ground plane.
3	FB	Feedback Voltage Sense Input. Connect this pin to a resistive divider from V_{OUT} . Set the voltage to 0.8 V for a desired V_{OUT} .
4	EN	Output Enable. Pull this pin high to enable the output. Pull this pin low to disable the output. This pin can also be used as a programmable UVLO input. This pin has a 1.2 μA pull-down current to GND.
5	VIN	Power Input. Connect to the input power source with a ceramic bypass capacitor to GND directly from this pin.
6	SW	Switch Node Output. Connect an inductor to V_{OUT} and a catch diode to GND from this pin.

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TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $V_N = V_{IN}$, unless otherwise noted.

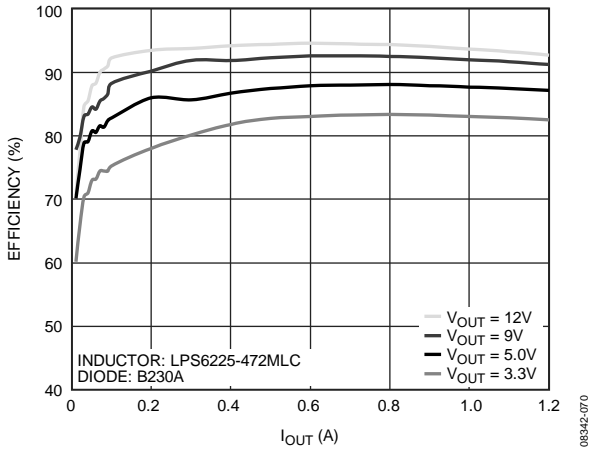


Figure 4. Efficiency Curve $V_{IN}=1.8\text{ V}$, $f_{sf}=1.4\text{ MHz}$

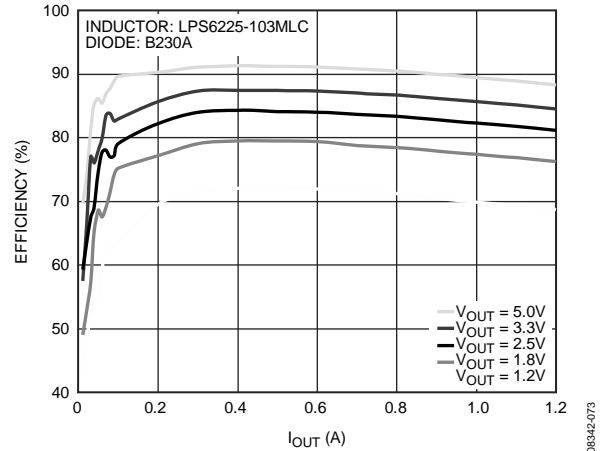


Figure 7. Efficiency Curve $V_{IN}=1.2\text{ V}$, $f_{sf}=700\text{ kHz}$

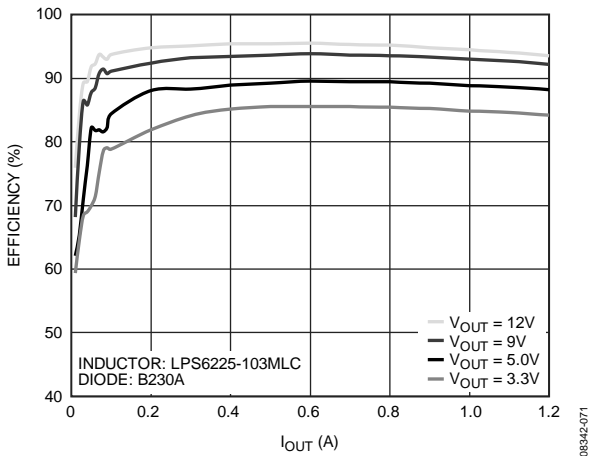


Figure 5. Efficiency Curve $V_{IN}=1.8\text{ V}$, $f_{sf}=700\text{ kHz}$

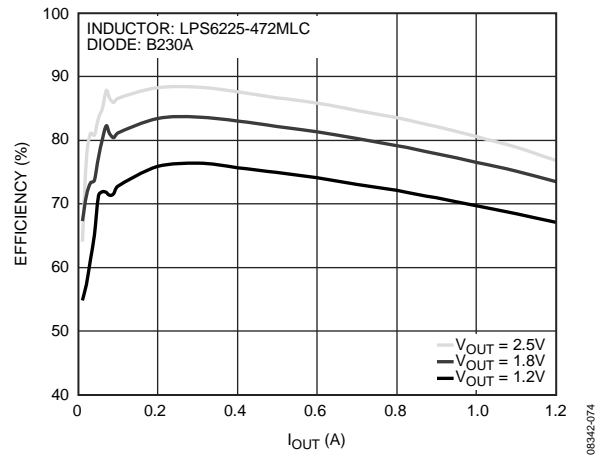


Figure 8. Efficiency Curve $V_{IN}=5.0\text{ V}$, $f_{sf}=1.4\text{ MHz}$

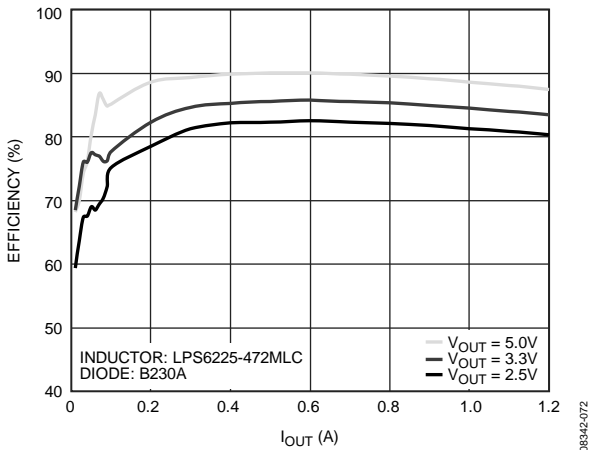


Figure 6. Efficiency Curve $V_{IN}=1.2\text{ V}$, $f_{sf}=1.4\text{ MHz}$

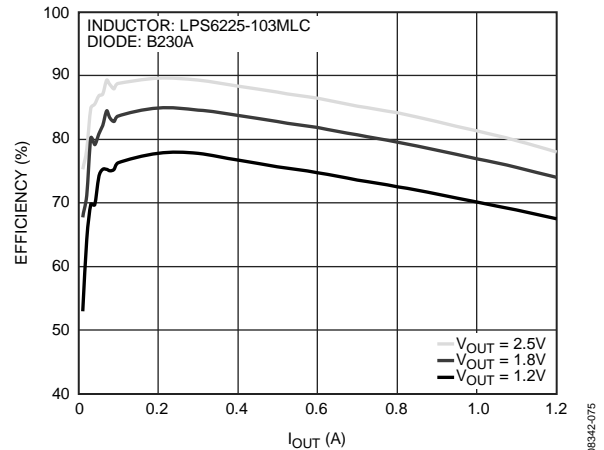


Figure 9. Efficiency Curve $V_{IN}=5.0\text{ V}$, $f_{sf}=700\text{ kHz}$

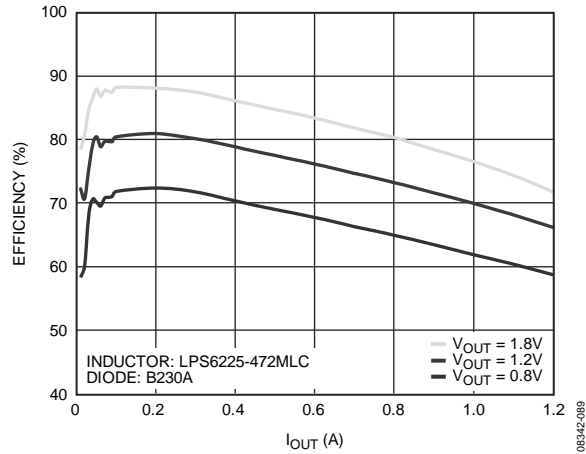


Figure 10. Efficiency Curve $V_{IN} = 3.3\text{ V}$ with External 5.0 V Bootstrap Bias Voltage, $f_{SW} = 1.4\text{ MHz}$

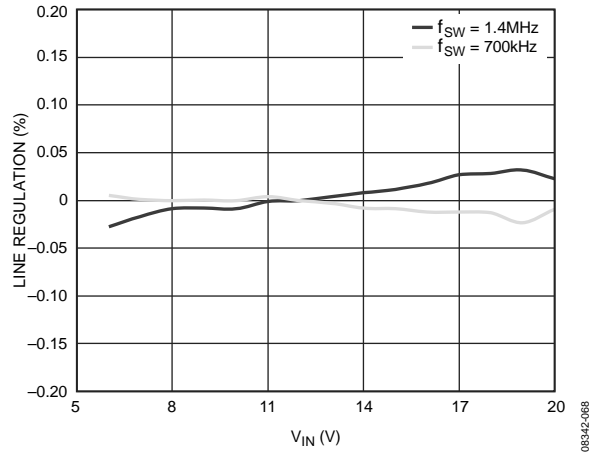


Figure 13. Line Regulation $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 500\text{ mA}$

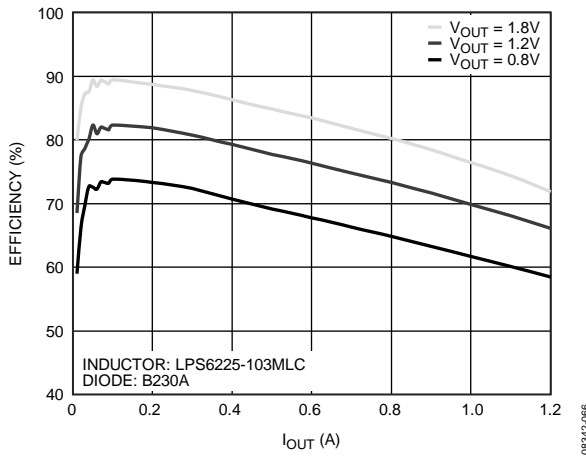


Figure 11. Efficiency Curve $V_{IN} = 3.3\text{ V}$ with External 5.0 V Bootstrap Bias Voltage, $f_{SW} = 700\text{ kHz}$

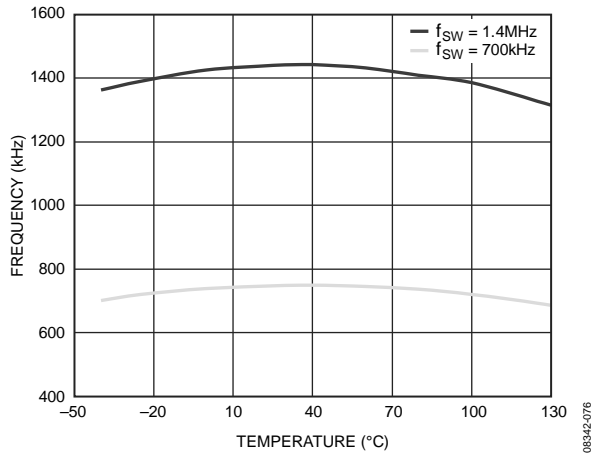


Figure 14. Frequency vs. Temperature

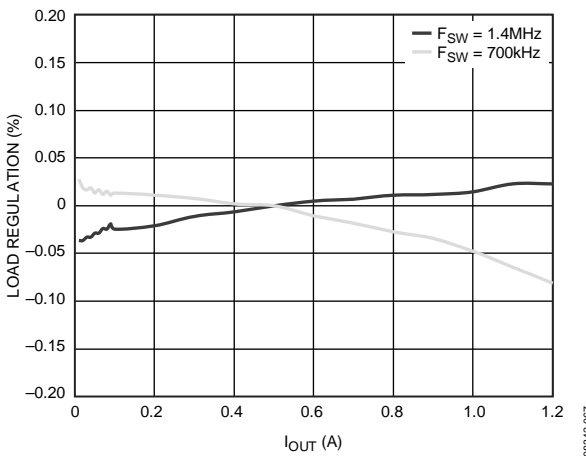


Figure 12. Load Regulation $V_{IN} = 3.3\text{ V}$, $V_{IN} = 12\text{ V}$

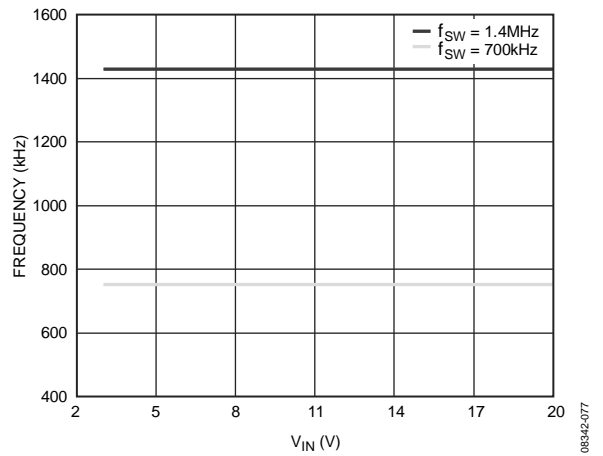


Figure 15. Frequency vs. V_{IN}

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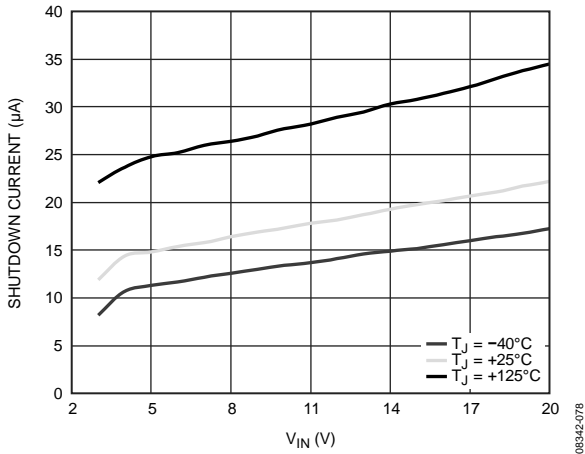


Figure 16. Shutdown Current vs. V_{IN}

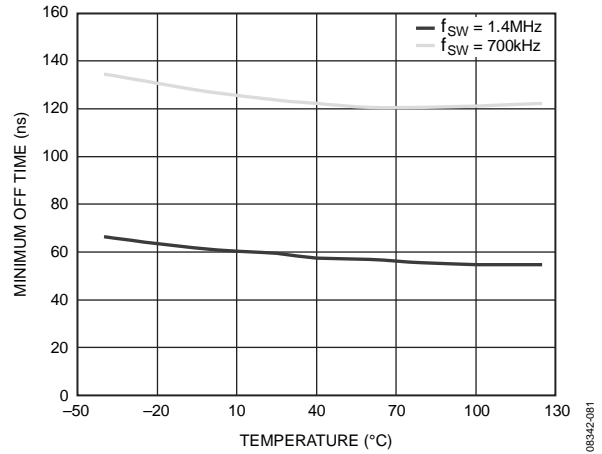


Figure 19. Minimum Off Time vs. Temperature

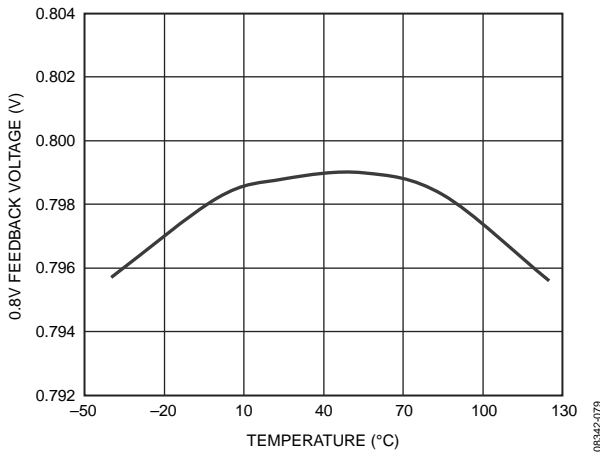


Figure 17. 0.8 V Feedback Voltage vs. Temperature

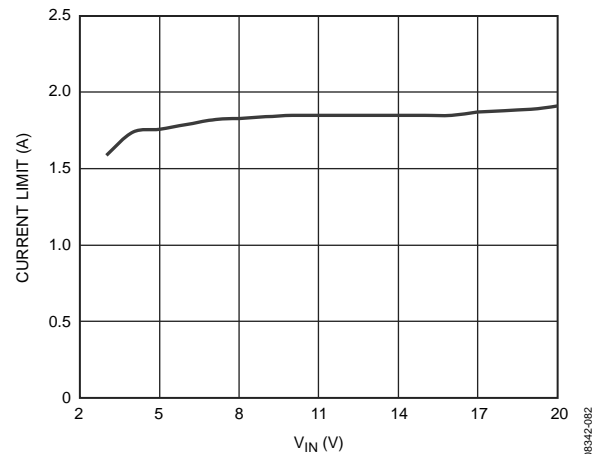


Figure 20. Current-Limit Threshold vs. V_{IN} at $f_{SW} = 5.0$ V

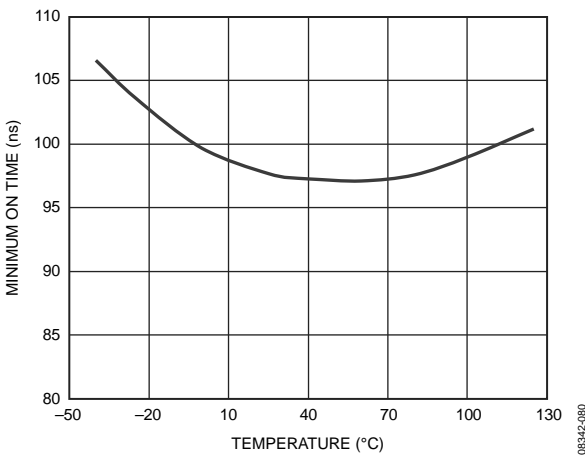


Figure 18. Minimum On Time vs. Temperature

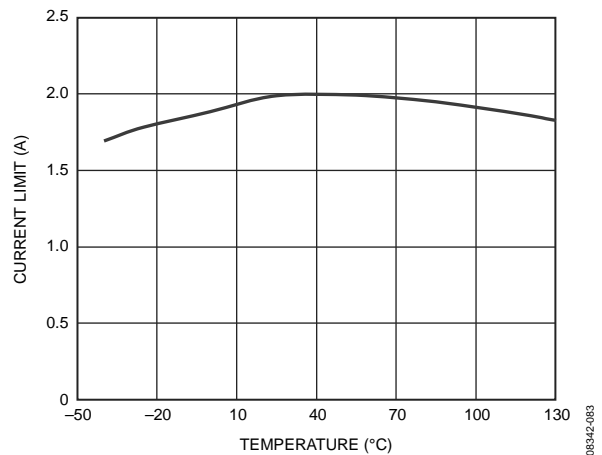


Figure 21. Current-Limit Threshold vs. Temperature

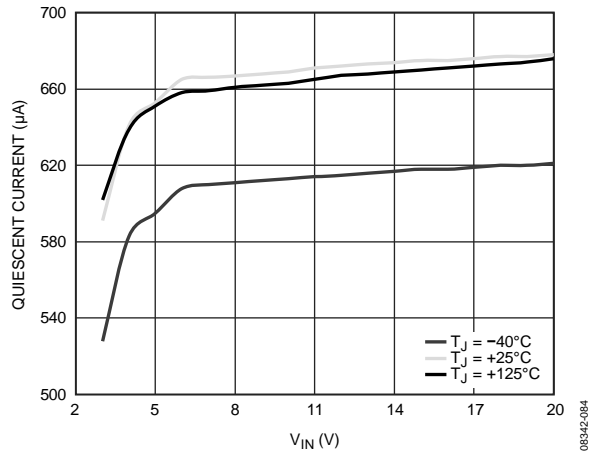


Figure 22. Quiescent Current vs. V

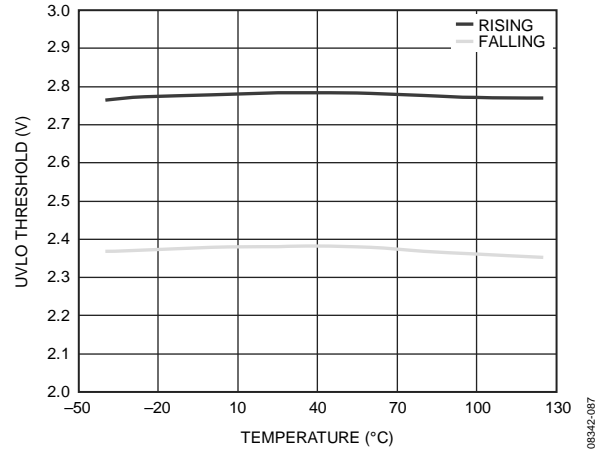


Figure 25. UVLO Threshold vs. Temperature

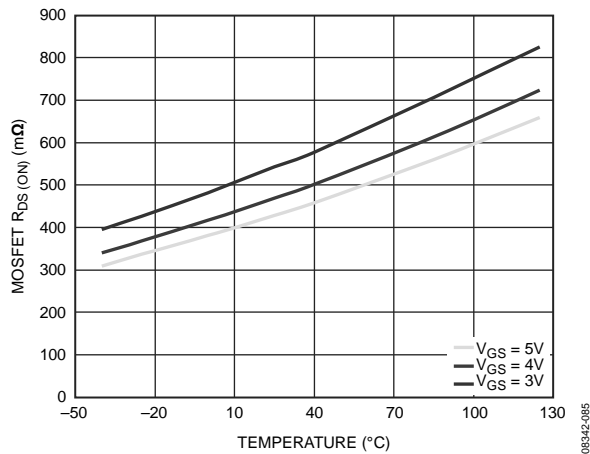


Figure 23. MOSFET $R_{DS(on)}$ vs. Temperature (Pin-to-Pin Measurements)

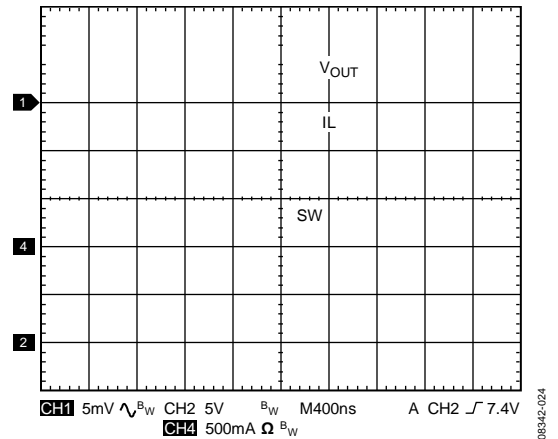


Figure 26. Steady State at Heavy Load, 1.4 MHz, $I_L = 1$ A

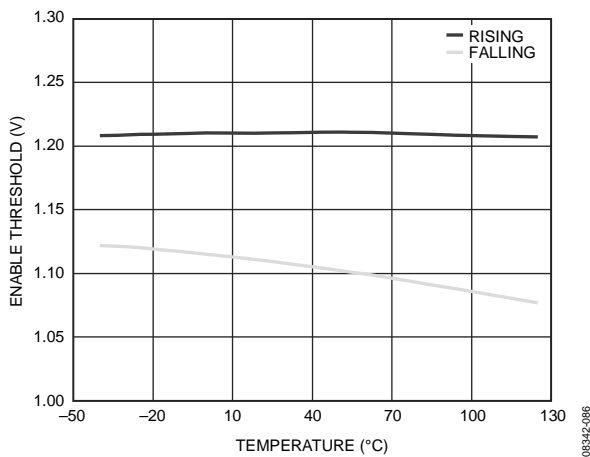


Figure 24. Enable Threshold vs. Temperature

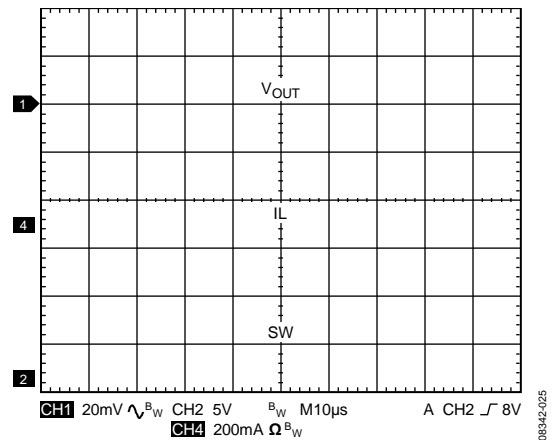


Figure 27. Steady State at Light Load, 1.4 MHz, $I_L = 40$ mA

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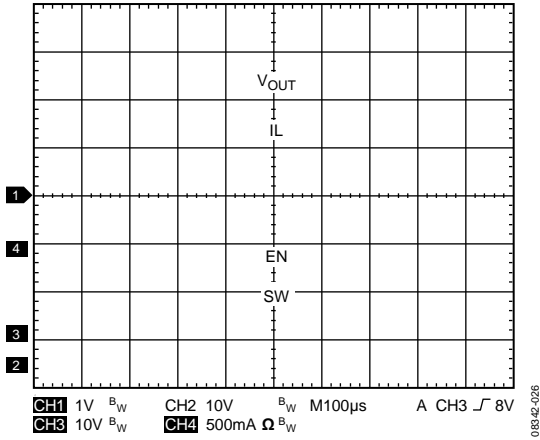


Figure 28. Soft Start with 1 A Resistance Load, $f_{sw} = 1.4$ MHz

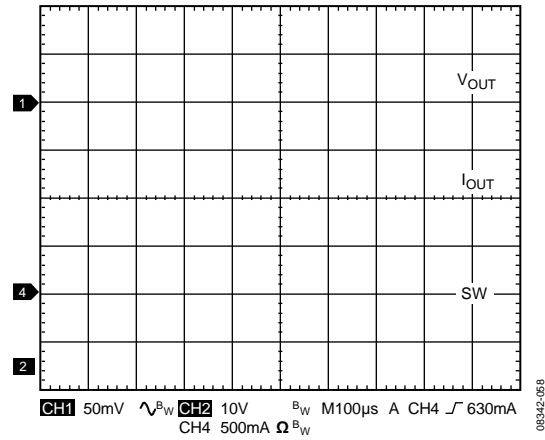


Figure 31. ADP2301 Load Transient, 0.2 A to 1.0 A, $V_{in} = 12$ V ($f_{sw} = 1.4$ MHz, $L = 4.7$ μ H, $C = 22$ μ F)

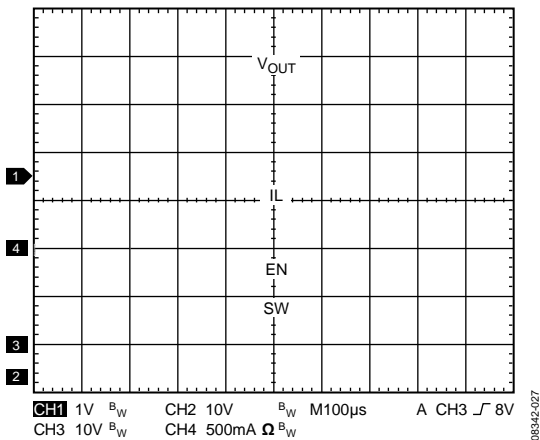


Figure 29. Soft Start with No Load, $f_{sw} = 1.4$ MHz

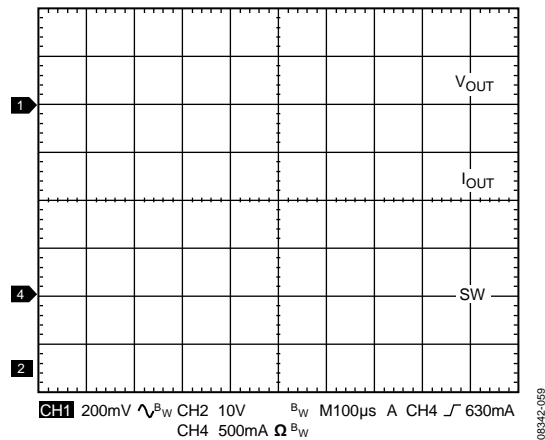


Figure 32. ADP2300 Load Transient, 0.2 A to 1.0 A, $V_{in} = 12$ V ($f_{sw} = 700$ kHz, $L = 10$ μ H, $C = 22$ μ F)

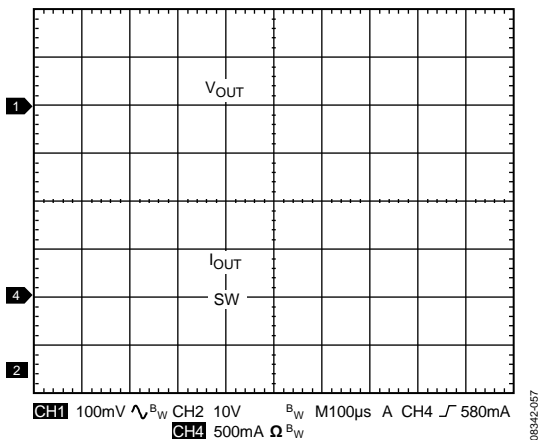


Figure 30. ADP2301 Load Transient, 0.2 A to 1.0 A, $V_{in} = 12$ V ($f_{sw} = 1.4$ MHz, $L = 4.7$ μ H, $C = 10$ μ F)

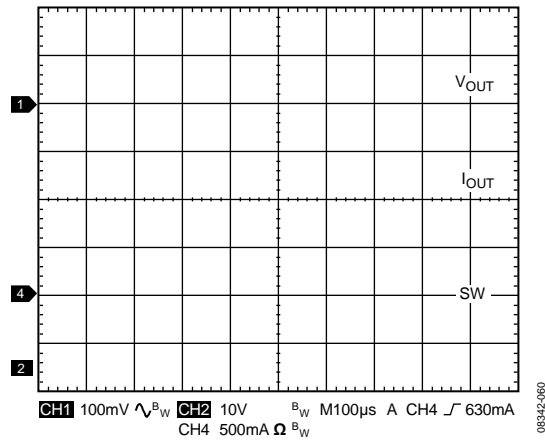


Figure 33. ADP2300 Load Transient, 0.2 A to 1.0 A, $V_{in} = 12$ V ($f_{sw} = 700$ kHz, $L = 10$ μ H, $C = 22$ μ F)

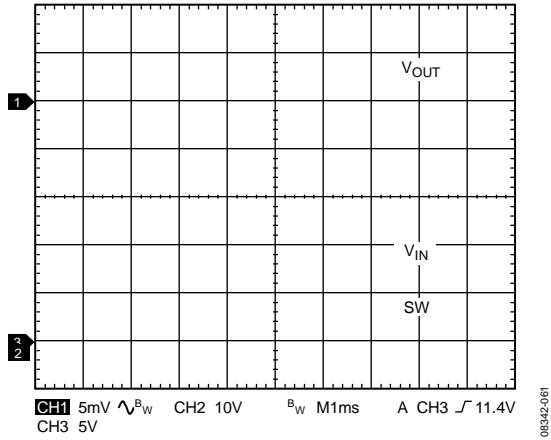


Figure 34. ADP2301 Line Transient, 7 V to 15 V, $V_{OUT} = 3.3$ V, $I_{OUT} = 1.2$ A, $f_{sw} = 1.4$ MHz

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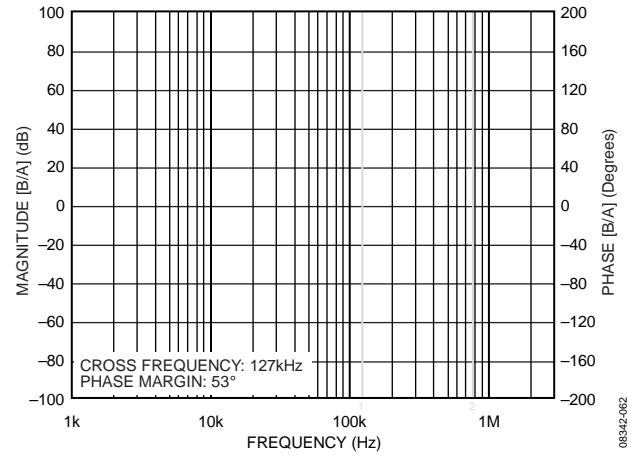


Figure 37. ADP2301 Bode Plot, $V_{IN} = 5.0$ V, $I_{OUT} = 12$ V ($f_{sw} = 1.4$ MHz, $L = 4.7$ μ H, $C = 10$ μ F)

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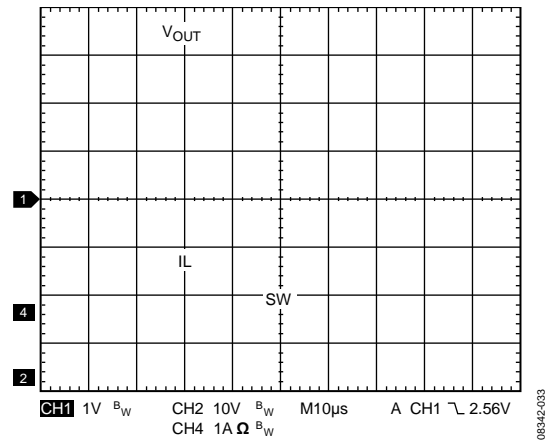


Figure 35. ADP2301 Short-Circuit Entry, $I_{OUT} = 3.3$ V ($f_{sw} = 1.4$ MHz)

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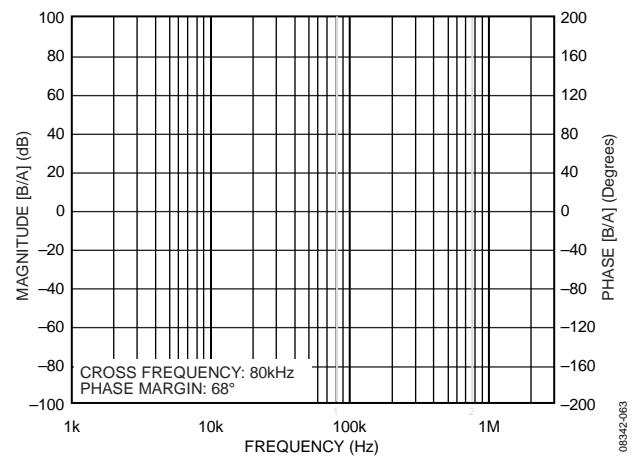


Figure 38. ADP2301 Bode Plot, $V_{IN} = 3.3$ V, $I_{OUT} = 12$ V ($f_{sw} = 1.4$ MHz, $L = 4.7$ μ H, $C = 22$ μ F)

08342-063

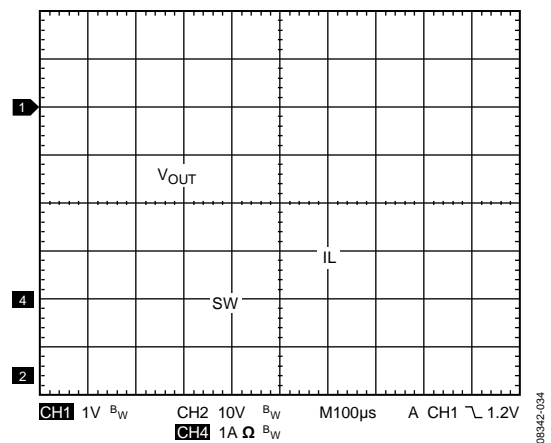


Figure 36. ADP2301 Short-Circuit Recovery, $I_{OUT} = 3.3$ V ($f_{sw} = 1.4$ MHz)

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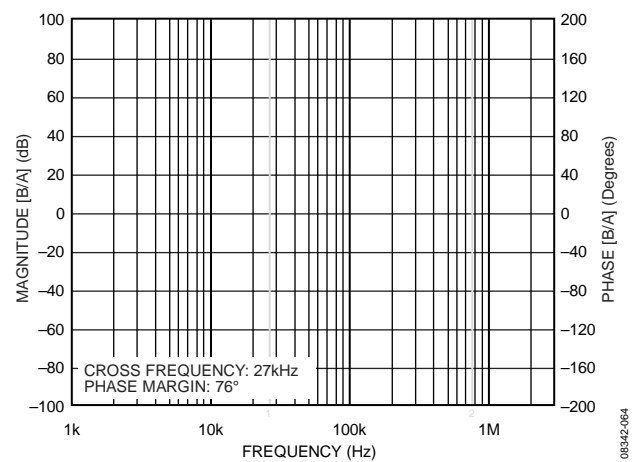


Figure 39. ADP2300 Bode Plot, $V_{IN} = 5.0$ V, $I_{OUT} = 12$ V ($f_{sw} = 700$ kHz, $L = 10$ μ H, $C = 22$ μ F)

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ADP2300/ADP2301

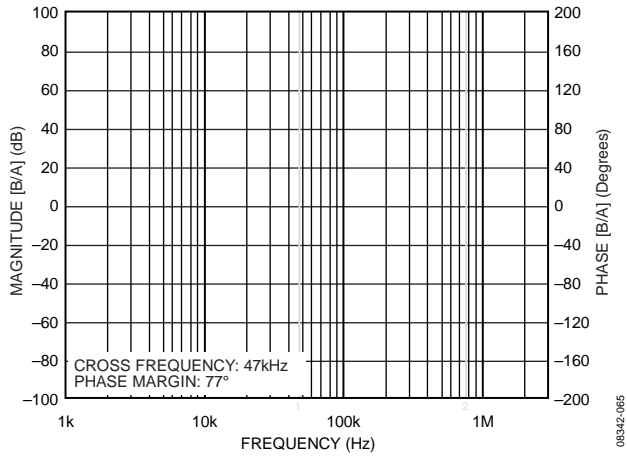


Figure 40. ADP2300 Bode Plot, $V_{in} = 3.3\text{ V}$, $V_{out} = 12\text{ V}$
($f_{sw} = 700\text{ kHz}$, $L = 10\text{ }\mu\text{H}$, $C = 22\text{ }\mu\text{F}$)

FUNCTIONAL BLOCK DIAGRAM

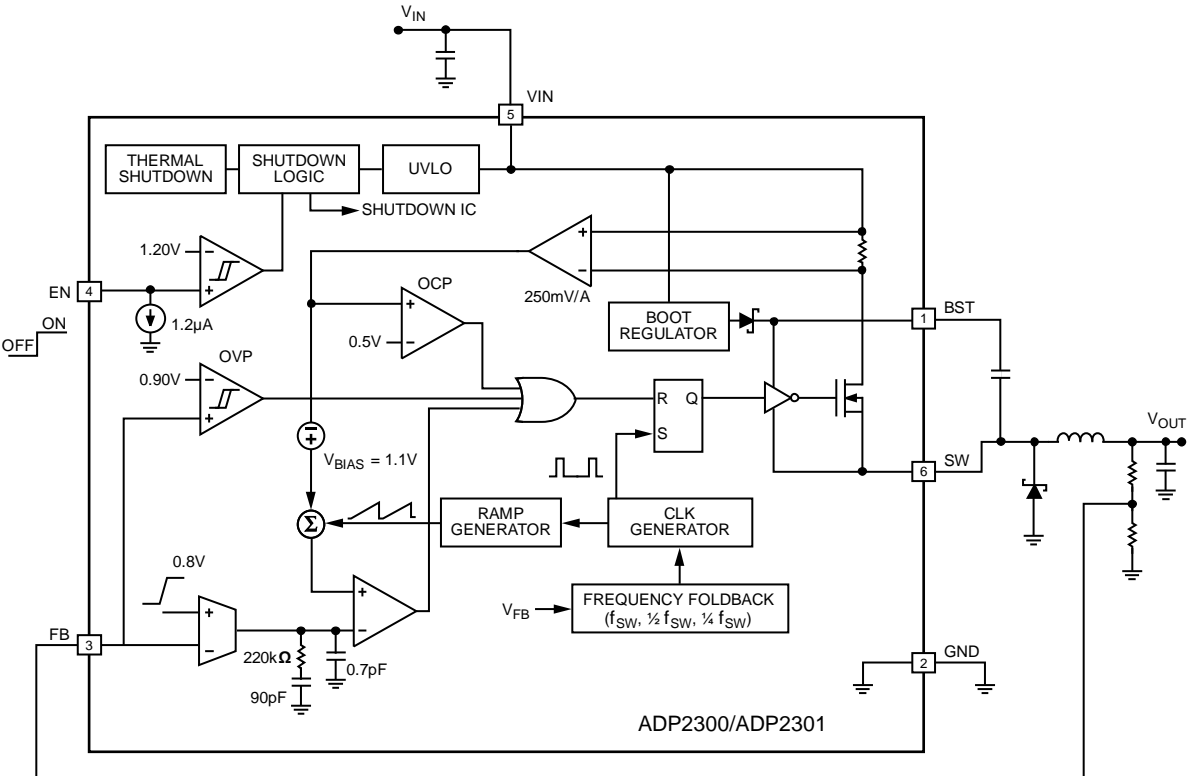


Figure 41. ADP2300/ADP2301 Functional Block Diagram

0.83.44-038

THEORY OF OPERATION

The ADP2300/ADP2301 are nonsynchronous, step-down dc-to-dc regulators, each with an integrated high-side power MOSFET. A high switching frequency and ultrasmall, 6-lead TSOT package allow small step-down dc-to-dc regulator solutions.

The ADP2300/ADP2301 can operate with an input voltage from 3.0 V to 20 V while regulating an output voltage down to 0.8 V.

The ADP2300/ADP2301 are available in two fixed-frequency options: 700 kHz (ADP2300) and 1.4 MHz (ADP2301).

BASIC OPERATION

The ADP2300/ADP2301 use the fixed-frequency, peak current-mode PWM control architecture at medium to high loads, but shift to a pulse-skip mode control scheme at light loads to reduce the switching power losses and improve efficiency. When the devices operate in fixed-frequency PWM mode, output regulation is achieved by controlling the duty cycle of the integrated MOSFET. When the devices operate in pulse-skip mode at light loads, the output voltage is controlled in a hysteretic manner with higher output ripple. In this mode of operation, the regulator periodically stops switching for a few cycles, thus keeping the conversion losses minimal to improve efficiency.

PWM MODE

In PWM mode, the ADP2300/ADP2301 operate at a fixed frequency, set by an internal oscillator. At the start of each oscillator cycle, the MOSFET switch is turned on, sending a positive voltage across the inductor. The inductor current increases until the current-sense signal crosses the peak inductor current threshold that turns off the MOSFET switch; this threshold is set by the error amplifier output. During the MOSFET off time, the inductor current declines through the external diode until the next oscillator clock pulse starts a new cycle. The ADP2300/ADP2301 regulate the output voltage by adjusting the peak inductor current threshold.

POWER SAVING MODE

To achieve higher efficiency, the ADP2300/ADP2301 smoothly transition to the pulse-skip mode when the output load decreases below the pulse-skip current threshold. When the output voltage dips below regulation, the ADP2300/ADP2301 enter PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET switch is turned off, and the output capacitor supplies all the output current.

Since the pulse-skip mode comparator monitors the internal compensation node, which represents the peak inductor current information, the average pulse-skip load current threshold depends on the input voltage (M), the output voltage (ΔU_T), the inductor, and the output capacitor.

Because the output voltage occasionally dips below regulation and then recovers, the output voltage ripple in the power saving mode is larger than the ripple in the PWM mode of operation.

BOOTSTRAP CIRCUITRY

The ADP2300/ADP2301 each have an integrated boot regulator, which requires that a 0.1 μF ceramic capacitor (X5R or X7R) be placed between the BST and SW pins to provide the gate drive voltage for the high-side MOSFET. There must be at least a 1.2 V difference between the BST and SW pins to turn on the high-side MOSFET. This voltage should not exceed 5.5 V in case the BST pin is supplied with an external voltage source through a diode.

The ADP2300/ADP2301 generate a typical 5.0 V bootstrap voltage for a gate drive circuit by differentially sensing and regulating the voltage between the BST and SW pins. A diode integrated on the chip blocks the reverse voltage between the VIN and BST pins when the MOSFET switch is turned on.

PRECISION ENABLE

The ADP2300/ADP2301 feature a precision enable circuit that has a 1.2 V reference voltage with 100 mV hysteresis. When the voltage at the EN pin is greater than 1.2 V, the part is enabled. If the EN voltage falls below 1.1 V, the chip is disabled. The precision enable threshold voltage allows the ADP2300/ADP2301 to be easily sequenced from other input/output supplies. It can also be used as programmable UVLO input by using a resistive divider. An internal 1.2 μA pull-down current prevents errors if the EN pin is floating.

INTEGRATED SOFT START

The ADP2300/ADP2301 include internal soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time is typically fixed at 1460 μs for the ADP2300 and at 730 μs for the ADP2301.

CURRENT LIMIT

The ADP2300/ADP2301 include current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET switch. The positive current limit on the power switch limits the amount of current that can flow from the input to the output.

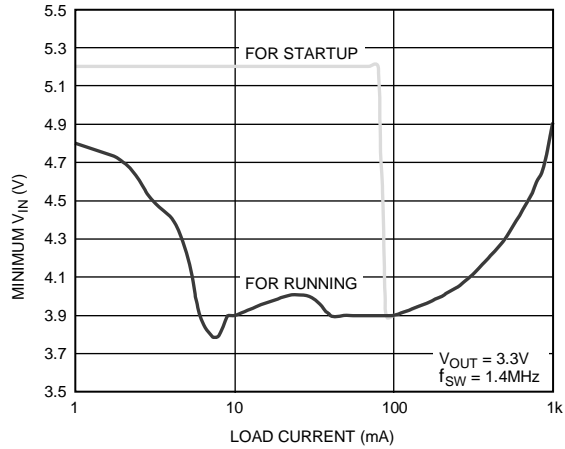


Figure 43. Minimum Input Voltage vs. Load Current

Based on three conversion limitations (the minimum on time, the minimum off time, and the bootstrap dropout voltage) Figure 44 shows the voltage conversion limitations.

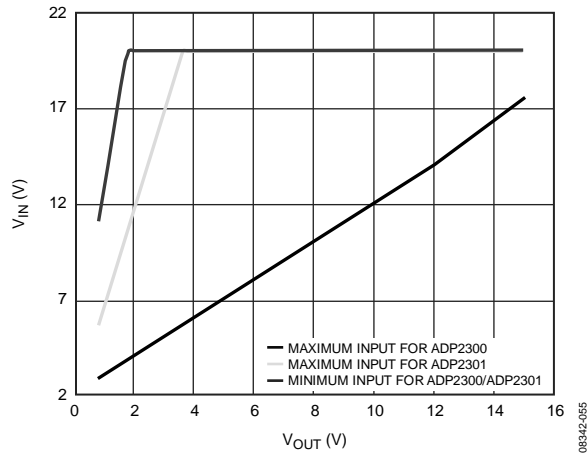


Figure 44. Voltage Conversion Limitations

LOW INPUT VOLTAGE CONSIDERATIONS

For low input voltage between 3 V and 5 V, the internal boot regulator cannot provide enough 5.0 V bootstrap voltage due to the internal dropout voltage. As a result, the increased MOSFET $R_{DS(ON)}$ reduces the available load current. To prevent this, add an external small-signal Schottky diode from a 5.0 V external bootstrap bias voltage. Because the absolute maximum rating between the BST and SW pins is 6.0 V, the bias voltage should be less than 5.5 V Figure 45 shows the application diagram for the external bootstrap circuit.

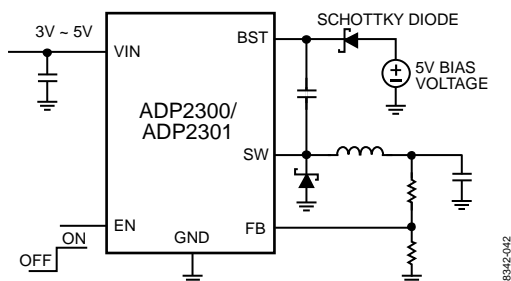


Figure 45. External Bootstrap Circuit for Low Input Voltage Application

PROGRAMMING THE PRECISION ENABLE

Generally, the EN pin can be easily tied to the VIN pin so that the device automatically starts up when the input power is applied. However, the precision enable feature allows the ADP2300/ADP2301 to be used as a programmable UVLO by connecting a resistive voltage divider to EN as shown in Figure 46. This configuration prevents the start-up problems that can occur when V_{IN} ramps up slowly in soft start with a relatively high load current.

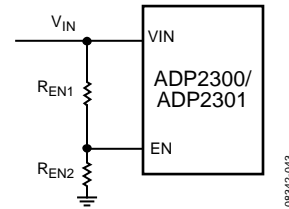


Figure 46. Precision Enable Used as a Programmable UVLO

The precision enable feature also allows the ADP2300/ADP2301 to be sequenced precisely by using a resistive voltage divider with another dc-to-dc output supply, as shown in Figure 47.

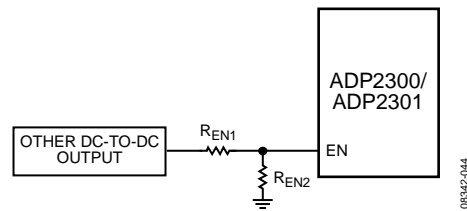


Figure 47. Precision Enable Used as a Sequencing Control from Another DC-to-DC Output

With a 1.2 μA pull-down current on the EN pin, the equation for the start-up voltage in Figure 46 and Figure 47 is

$$V_{STARTUP} = \left(\frac{12 \text{ V}}{R_{EN2}} + 1.2 \text{ A} \right) \times R_{EN1} + 12 \text{ V}$$

where:

$V_{STARTUP}$ is the start-up voltage to enable the chip.

R_{EN1} is the resistor from the dc source to EN.

R_{EN2} is the resistor from EN to GND.

ADP2300/ADP2301

THERMAL CONSIDERATIONS

The ADP2300/ADP2301 store the value of the inductor current only during the on time of the internal MOSFET. Therefore, a small amount of power is dissipated inside the ADP2300/ADP2301 package, which reduces thermal constraints.

However, when the application is operating under maximum load with high ambient temperature and high duty cycle, the heat dissipated within the package may cause the junction temperature of the die to exceed the maximum junction temperature of 125°C. If the junction temperature exceeds 140°C, the regulator goes into thermal shutdown and recovers when the junction temperature drops below 125°C.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as indicated in the following equation:

$$T_j = T_A + T_R$$

where:

T_j is the junction temperature.

T_A is the ambient temperature.

T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:

T_R is the rise in temperature of the package.

θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package.

P_D is the power dissipation in the package.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential to obtain the best performance from the ADP2300/ADP2301. Poor layout can affect the regulation and stability, as well as the electromagnetic interface (EMI) and electromagnetic compatibility (EMC) performance. A PCB layout example is shown in Figure 50. Refer to the following guidelines for a good PCB layout:

- Place the input capacitor, inductor, catch diode, output capacitor, and bootstrap capacitor close to the IC using short traces.
- Ensure that the high current loop traces are as short and wide as possible. The high current path is shown in Figure 49.
- Maximize the size of ground metal on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

- Minimize the length of the FB trace connecting the top of the feedback resistive voltage divider to the output. In addition, keep these traces away from the high current traces and the switch node to avoid noise pickup.

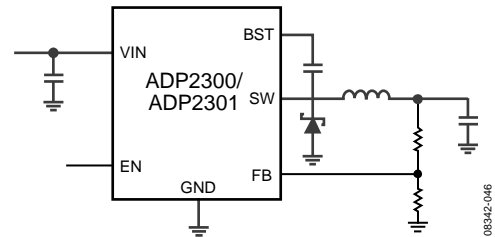


Figure 49. Typical Application Circuit with High Current Traces Shown in Blue

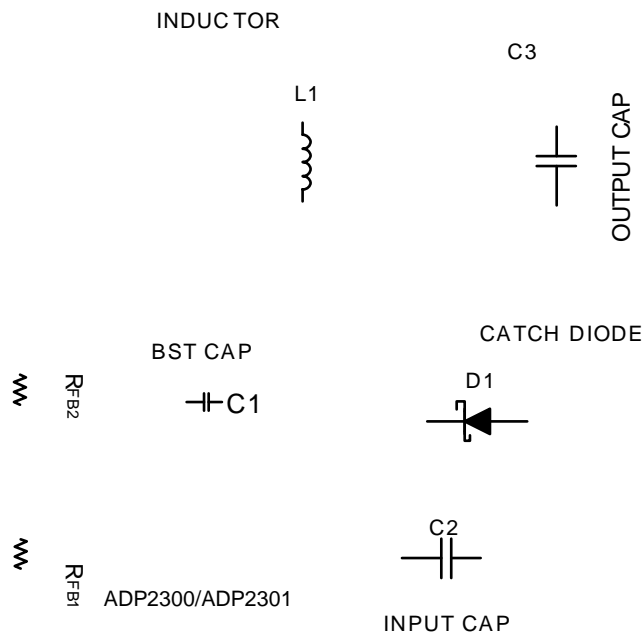


Figure 50. Recommended PCB Layout for the ADP2300/ADP2301

TYPICAL APPLICATION CIRCUITS

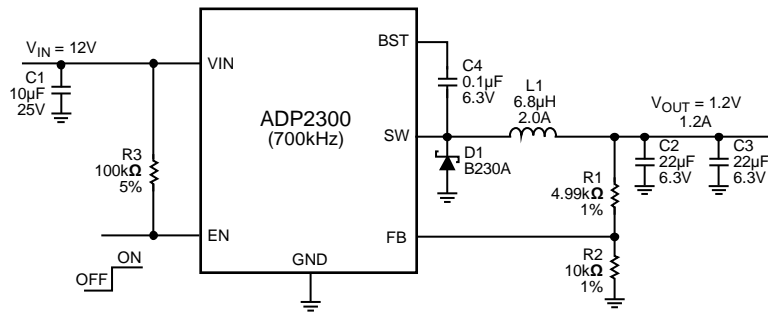


Figure 51. ADP2300, 700 kHz Typical Application $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.2\text{ V}/1.2\text{ A}$ with External Enabling

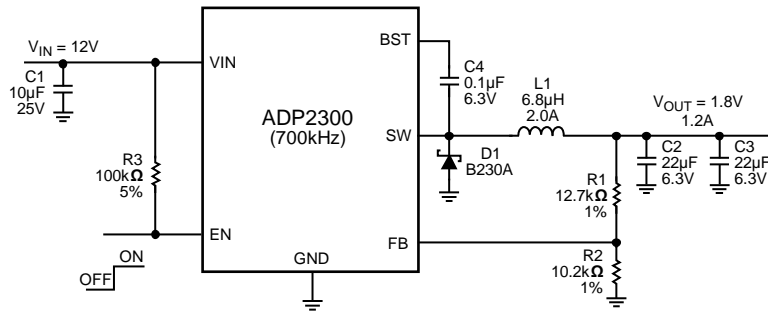


Figure 52. ADP2300, 700 kHz Typical Application $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.8\text{ V}/1.2\text{ A}$ with External Enabling

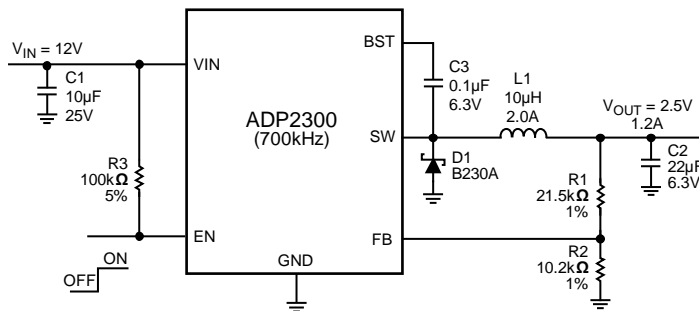


Figure 53. ADP2300, 700 kHz Typical Application $V_{IN} = 12\text{ V}$, $V_{OUT} = 2.5\text{ V}/1.2\text{ A}$ with External Enabling

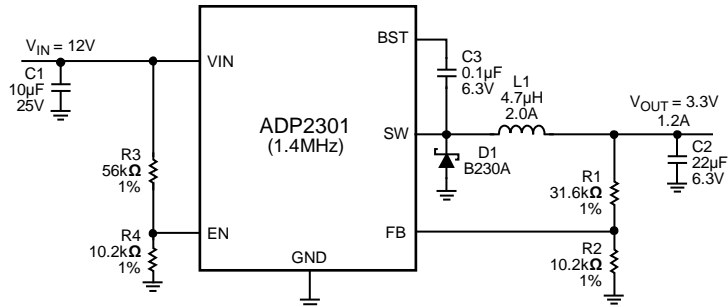


Figure 54. ADP2301, 1.4 MHz Typical Application $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}/1.2\text{ A}$ (with Programmable 7.8 V Start-Up Input Voltage)

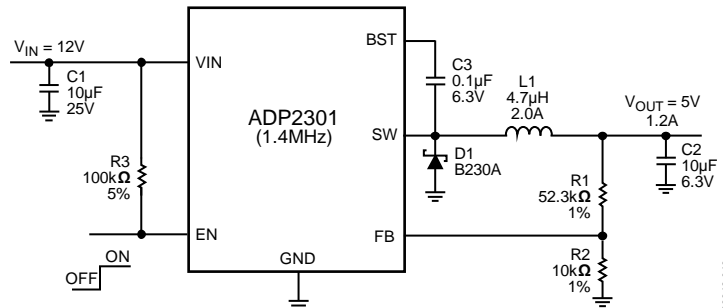


Figure 55. ADP2301, 1.4 MHz Typical Application $V_{IN} = 12\text{ V}$, $V_{OUT} = 5.0\text{ V}/1.2\text{ A}$ with External Enabling

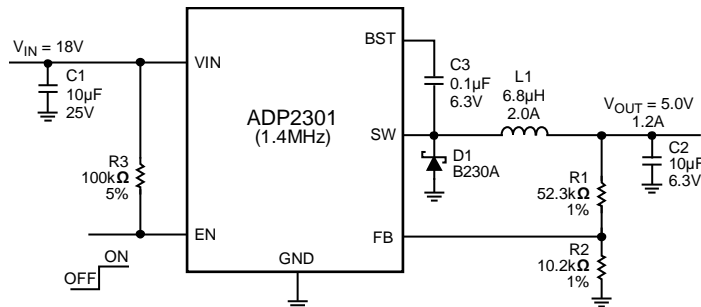


Figure 56. ADP2301, 1.4 MHz Typical Application $V_{IN} = 18\text{ V}$, $V_{OUT} = 5.0\text{ V}/1.2\text{ A}$ with External Enabling

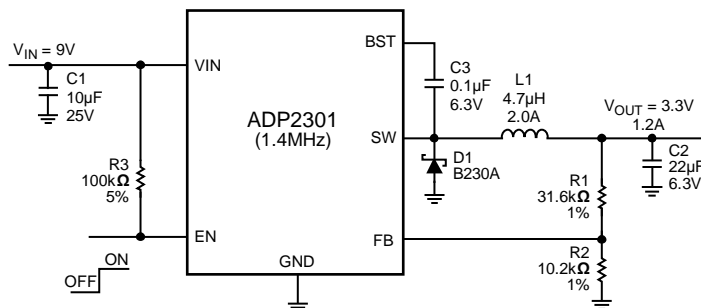


Figure 57. ADP2301, 1.4 MHz Typical Application $V_{IN} = 9\text{ V}$, $V_{OUT} = 3.3\text{ V}/1.2\text{ A}$ with External Enabling

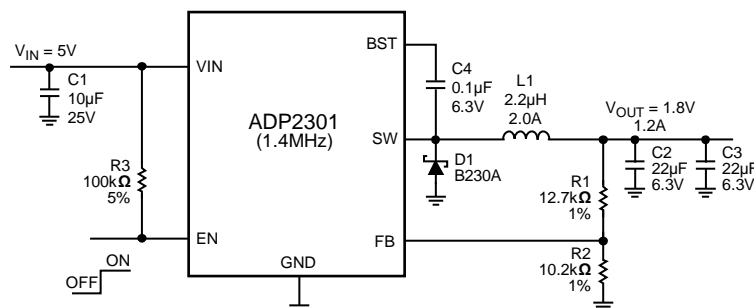
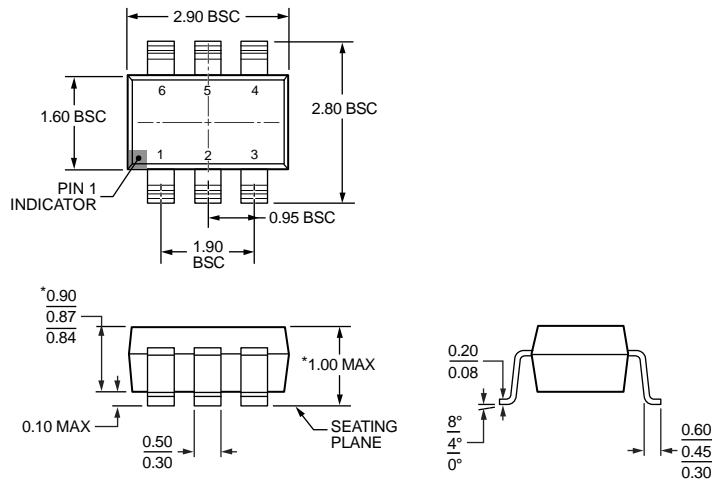


Figure 58. ADP2301, 1.4 MHz Typical Application $V_{IN} = 5\text{ V}$, $V_{OUT} = 1.8\text{ V}/1.2\text{ A}$ with External Enabling

ADP2300/ADP2301

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-193-AA WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 59. 6-Lead Thin Small Outline Transistor Package [TSOT] (UJ-6)

Dimensions shown in millimeters

102808-A

ORDERING GUIDE

Model ¹	Switching Frequency	Temperature Range	Package Description	Package Option	Branding
ADP2300AUJZ-R7	700 kHz	-40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	L87
ADP2300-EVALZ			Evaluation Board		
ADP2301AUJZ-R7	1.4 MHz	-40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	L86
ADP2301-EVALZ			Evaluation Board		

¹ Z = RoHS Compliant Part.

NOTES

NOTES