Low Noise, Precision, Rail to Rail Output, JFET Dual Operational Amplifier

ADA4610S

1.0 Scope

1.1. This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

1.2. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aeroinfo

1.3. This data specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at http://www.analog.com/ADA4610-2

2.0 Part Number

2.1. The complete part number(s) of this specification follows:

Specific Part Number	Description
ADA4610R703F	Precision, Low Noise, Low Input Bias Current, Wide Bandwidth, Dual JFET, Operational Amplifier. Radiation tested to 100Krads (Si)

3.0 Case Outline

3.1. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline Letter	Descriptive Designator	Terminals	Package style
X	CDFP3-F10	10 lead	Bottom Brazed Flat Pack

Package: X			
Pin Number	Terminal Symbol	Pin Type	Pin Description
1	NC/GND	N/A	No connection or ground this terminal
2	OUTA	Analog output	Operational amplifier output, Amp-A
3	-INA	Analog input	Operational amplifier negative input, Amp-A
4	+INA	Analog input	Operational amplifier positive input, Amp-A
5	-Vsy	Power	Negative power supply
6	NC/GND	N/A	No connection or ground this terminal
7	+INB	Analog input	Operational amplifier positive input, Amp-B
8	-INB	Analog input	Operational amplifier negative input, Amp-B
9	OUTB	Analog output	Operational amplifier output, Amp-B
10	+Vsy	Power	Positive power supply

Figure 1 – Terminal Connections

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

4.0 Specifications

4.1. Absolute Maximum Ratings 1/

Supply voltage ($+V_{SY}$ to $-V_{SY}$) ..... 36 V
Input voltage (V_{IN})..... $-V_{SY}$ to $+V_{SY}$ 7/
Differential Input Voltage..... $\pm V_{SY}$ 7/
Storage temperature range ..... -65°C to +150°C
Junction temperature maximum (T_J) ..... +150°C 2/
Lead temperature (soldering, 60 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 22 °C/W 3/
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 132 °C/W 3/

4.2. Recommended Operating Conditions

Supply voltage ($\pm V_{SY}$) ..... ±5.0 V to ±15.0 V
Ambient operating temperature range (T_A)…… -55°C to +125°C

4.3. Nominal Operating Performance Characteristics 4/

Input Capacitance
Differential (C_{DM}) ..... 3.1 pF
Common Mode (C_{CM}) ..... 4.8 pF
Input Resistance ..... $>1 \times 10^{13}$

Unity-Gain Crossover (V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ, A_V = -10)
$\pm V_{SY}$ = ±5 V ..... 9.3 kHz
$\pm V_{SY}$ = ±15 V ..... 9.3 kHz

Phase Margin 5/
$\pm V_{SY}$ = ±5 V ..... 61 Degrees
$\pm V_{SY}$ = ±15 V ..... 66 Degrees

-3 dB Closed-Loop Bandwidth (V_{IN} = 5 mV_{p-p}, A_V = 1) 6/
$\pm V_{SY}$ = ±5 V ..... 10.6 MHz
$\pm V_{SY}$ = ±15 V ..... 9.4 MHz

Total Harmonic Distortion (THD)+Noise
1 kHz, G = +1, RL = 2 kΩ, VIN = 6 V rms 0000.6%

4.4. Radiation Features

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)….100 k rads(Si)

1/ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
2/ While the ADA4610 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. Do not exceed maximum Tj in application with output current load.
3/ Measurement taken under absolute worst case condition and represents data taken with thermal camera for highest power density location. See MIL-STD-1835 for average Θ_{JC} number.
4/ T_A = 25ºC, +/-VSY=+/-5, +/-VSY = +/- 15V and V_{CM} = 0V unless otherwise noted
5/ See Figures 14 and 17 in Section 7.0 Application Notes for Open-Loop, Gain and Phase vs. Frequency performance.
6/ See Figures 15 and 18 in Section 7.0 Application Notes for Closed-Loop Gain vs. Frequency performance.
7/ See Section 7.3 for information on how to limit input current.

TABLE IA – ELECTRICAL PERFORMANCE CHARACTERISTICS (+/-V_{SY} = +/-5V)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		1,3	-0.4	0.4	mV
			2	-0.8	0.8	mV
		M,D,P,L,R	1	-0.4	0.4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	3/4/	2,3	-8	8	µV/°C
Input Bias Current 5/	I_B		1,3	-25	25	pA
			2	-1.5	1.5	nA
		M,D,P,L,R	1	-25	25	pA
Input Offset Current	I_{OS}		1,3	-20	20	pA
			2	-0.4	0.4	nA
		M,D,P,L,R	1	-20	20	pA
Input Voltage Range	IVR		1,2,3	-2.5	2.5	V
		M,D,P,L,R	1	-2.5	2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -2.5V to +2.5V	1	94		dB
			2,3	86		
		M,D,P,L,R	1	94		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = -3.5 to + 3.5V	1,3	98		dB
			2	86		
		M,D,P,L,R	1	98		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	1,3	4.85		V
			2	4.6		
		M,D,P,L,R	1	4.85		V
		R_L = 600Ω	1,3	4.6		V
			2	4.05		
		M,D,P,L,R	1	4.6		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ	1,3		-4.9	V
			2		-4.75	
		M,D,P,L,R	1		-4.9	V
		R_L = 600Ω	1,3		-4.8	V
			2		-4.4	
		M,D,P,L,R	1		-4.8	V
Short-Circuit Limit 7/	$+I_{SC}$	Source	1,2	-65		mA
			3	-70		mA
		M,D,P,L,R	1	-65		mA
	$-I_{SC}$	Sink	1,2		+65	mA
			3		+70	mA
		M,D,P,L,R	1		+65	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+/-V_{SY} = ±4.5V to ±18V	1	106		dB
			2,3	103		
		M,D,P,L,R	1	106		dB
Total Supply Current (Both Amplifiers)	I_{SY}	I_O = 0mA	1		3.4	mA
			2,3		3.7	mA
		M,D,P,L,R	1		3.4	mA

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
TRANSIENT RESPONSE						
Rise Time	t_R	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4		31	nS
		C_L = 100pF, AV =-1 2/ 3/ 6/	5		57	
			6		24	
Fall Time	t_F	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4		51	nS
		C_L = 100pF, AV =-1 2/ 3/ 6/	5		69	
			6		39	
Settling Time	$+T_S$	0.1% error, AV =-1 2/ 3/	4		430	nS
			5		540	
			6		410	
	$-T_S$	0.1% error, AV =-1 2/ 3/	4		450	nS
			5		670	
			6		650	
Overshoot	+OVR	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4		12	nS
		C_L = 100pF, AV =-1 2/ 3/	5,6		14	
	-OVR	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4,5,6		20	nS
		C_L = 100pF, AV =-1 2/ 3/				
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4	17		MHz
		A_V = -100 2/ 3/	5	9		
			6	24		
Slew Rate	+SR	R_L = 2 kΩ, C_L = 100pF 2/ 3/ 6/	4	25		V/µs
			5	13		
			6	33		
	-SR	R_L = 2 kΩ, C_L = 100pF 2/ 3/ 6/	4	-17		V/µs
			5	-11		
			6	-19		
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth	4		1.7	µV p-p
		2/ 3/	5		4	
			6		3.2	
Voltage Noise Density	e_n	f = 10 kHz 2/ 3/	4		7.3	nV/√Hz
			5		10.5	
			6		5.5	

TABLE IA NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, T_A min = -55ºC and V_{CM} = 0V unless otherwise noted

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ Calculated from 25ºC to -55ºC, 25ºC to 125ºC and -55ºC to 125ºC

5/ Input bias current increases exponentially as T>45°C. See Figure 10 in Section 7.0 Application Notes.

6/ Measured from 10% to 90% and 90% to 10% of output swing.

7/ While the ADA4610 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. Do not exceed maximum Tj in application with output current load.

TABLE IB – ELECTRICAL PERFORMANCE CHARACTERISTICS (+/-V_{SY} = +/-15V)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		1,3	-0.4	0.4	mV
			2	-0.8	0.8	
		M,D,P,L,R	1	-0.4	0.4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	3/4/	2,3	-8	8	µV/°C
Input Bias Current 5/	I_B		1,3	-25	25	pA
			2	-1.5	1.5	nA
		M,D,P,L,R	1	-25	25	pA
Input Offset Current	I_{OS}		1,3	-20	20	pA
			2	-0.4	0.4	nA
		M,D,P,L,R	1	-20	20	nA
Input Voltage Range	IVR		1,2,3	-12.6	12.6	V
		M,D,P,L,R	1	-12.6	12.6	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -12.6V to +12.6V	1	100		dB
			2,3	96		
		M,D,P,L,R	1	100		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = -13.5V to +13.5V	1,3	104		dB
			2	91		
		M,D,P,L,R	1	104		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	1,3	14.80		V
			2	14.65		
		M,D,P,L,R	1	14.80		V
		R_L = 600 Ω to GND	1,3	14.25		V
			2	13.35		
		M,D,P,L,R	1	14.25		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND	1,3		-14.85	V
			2		-14.75	
		M,D,P,L,R	1		-14.85	V
		R_L = 600 Ω to GND	1,3		-14.60	V
			2		-14.30	
		M,D,P,L,R	1		-14.60	V
Short-Circuit Limit 7/	$+I_{SC}$	Source	1,2	-85		mA
			3	-95		
		M,D,P,L,R	1	-85		mA
	$-I_{SC}$	Sink	1,2		+85	mA
			3		+95	
		M,D,P,L,R	1		+85	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+/-V_{SY} = ±4.5V to ±18V	1	106		dB
			2,3	103		
		M,D,P,L,R	1	106		dB
Total Supply Current (Both Amplifiers)	I_{SY}	I_O = 0mA	1,3		3.7	mA
			2		4	
		M,D,P,L,R	1		3.7	
TRANSIENT RESPONSE						
Rise Time	t_R	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4		31	nS
		C_L = 100pF, AV =-1 2/ 3/ 6/	5		57	
			6		24	

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
Fall Time	t_F	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4		51	nS
		C_L = 100pF, AV =-1 2/ 3/ 6/	5		69	
			6		39	
Settling Time	+T_S	0.1% error, AV =-1 2/ 3/	4		430	nS
			5		540	
			6		410	
	-T_S	0.1% error, AV =-1 2/ 3/	4		450	nS
			5		670	
			6		650	
Overshoot	+OVR	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4		12	nS
		C_L = 100pF, AV =-1 2/ 3/	5,6		14	
	-OVR	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4,5,6		20	nS
		C_L = 100pF, AV =-1 2/ 3/				
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	V_{IN} = 5 mV_{p-p}, R_L = 2 kΩ,	4	17		MHz
		A_V = -100 2/ 3/	5	9		
			6	24		
Slew Rate	+SR	R_L = 2 kΩ, C_L = 100pF 2/ 3/ 6/	4	25		V/µs
			5	13		
			6	33		
	-SR	R_L = 2 kΩ, C_L = 100pF 2/ 3/ 6/	4	-17		V/µs
			5	-11		
			6	-19		
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth	4		1.7	µV p-p
		2/ 3/	5		4	
			6		3.2	
Voltage Noise Density	e_n	f = 10 kHz 2/ 3/	4		7.3	nV/√Hz
			5		10.5	
			6		5.5	

TABLE IB NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, T_A min = -55ºC and V_{CM} = 0V unless otherwise noted

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ Calculated from 25ºC to -55ºC, 25ºC to 125ºC and -55ºC to 125ºC

5/ Input bias current increases exponentially as T>45°C. See Figure 10 in Section 7.0 Application Notes.

6/ Measured from 10% to 90% and 90% to 10% of output swing.

7/ While the ADA4610 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. Do not exceed maximum Tj in application with output current load.

TABLE IIA – ELECTRICAL TEST REQUIREMENTS:

Table IIA	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1,2,3, 1/ 2/
Group A Test Requirements	1,2,3,
Group C end-point electrical parameters	1,2,3, 2/
Group D end-point electrical parameters	1,2,3,
Group E end-point electrical parameters	1 3/

Table IIA Notes:
1/ PDA applies to Table I subgroup 1 and Table IIB delta parameters.
2/ See Table IIB for delta parameters
3/ Parameters noted in Table IA, IB are not tested post irradiation.

TABLE IIB – LIFE TEST/BURN-IN DELTA LIMITS (+/-V_{SY} = +/-5V & +/-V_{SY} = +/-15V)

Table IIB			
Parameter	Symbol	Delta	Units
Offset voltage	V_{OS}	±120	µV
Input Bias Current V_{CM} = 0V	I_B	±9.4	pA
Supply Current	I_{SY}	±0.7	mA

5.0 Burn-In Life Test, and Radiation

5.1. Burn-In Test Circuit, Life Test Circuit

5.1.1. The test conditions and circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 test condition B and alternate test condition D of MIL –STD-883.

5.1.2. HTRB is not applicable for this drawing.

5.2. Radiation Exposure Circuit

5.2.1. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A.

6.0 MIL-PRF-38535 QMLV Exceptions

6.1. Wafer Fabrication

Wafer fabrication occurs at MIL-PRF-38535 QML Class Q certified facility.

6.2. Wafer Lot Acceptance (WLA)

WLA per MIL-STD-883 TM 5007 is not available for this product.

7.0 Application Notes

7.1. General Description

The ADA4610 is a dual precision JFET amplifier that features low offset voltage, low input bias current, low input voltage noise, low input current noise, and rail-to-rail output.

Unlike many competitive amplifiers, the ADA4610 maintains fast settling performance even with substantial capacitive loads. Unlike many older JFET amplifiers, the ADA4610 does not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

7.2. Electrical Characteristics

For reference figures 2 through 39 are typical performance characteristics at T_A = 25°C unless otherwise stated taken from Rev B of the ADA4610-2 commercial datasheet.

Typical Performance Characteristics

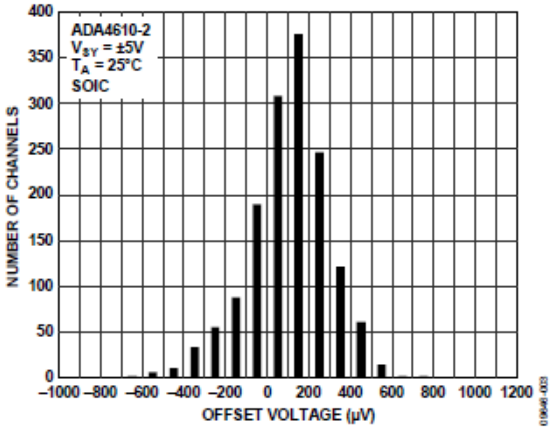

Figure 2. Input Offset Voltage Distribution

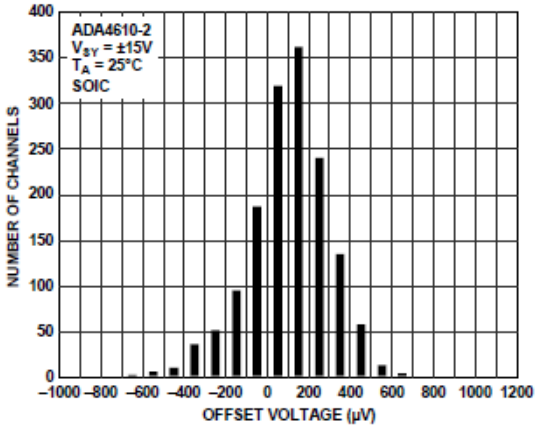

Figure 5. Input Offset Voltage Distribution

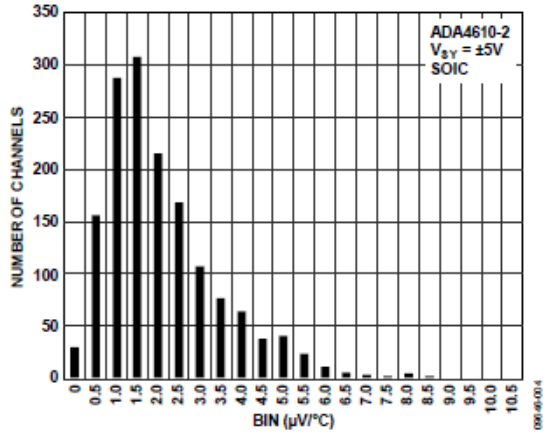

Figure 3. T_CV_{OS} Distribution

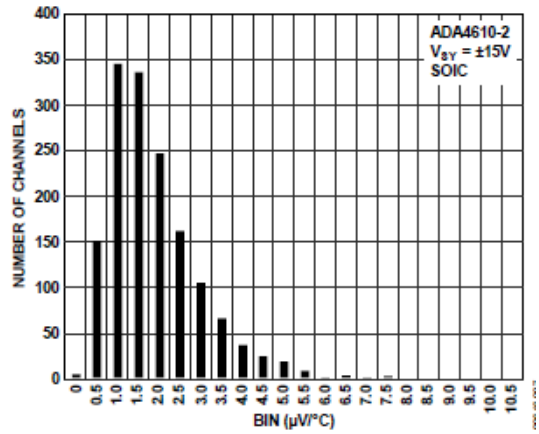

Figure 6. T_CV_{OS} Distribution

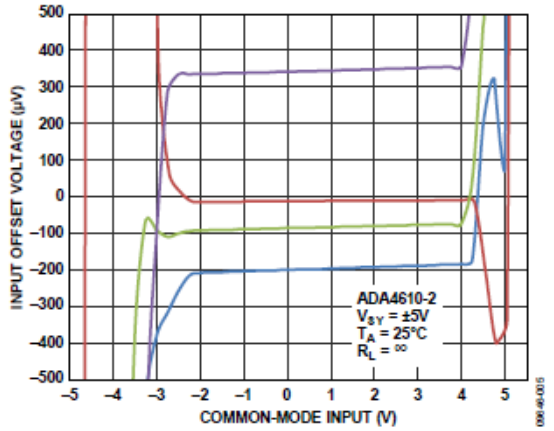

Figure 4. Input Offset Voltage vs. Common-Mode Input Voltage

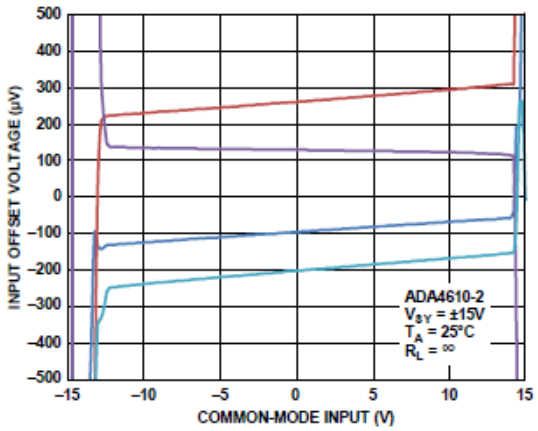

Figure 7. Input Offset Voltage vs. Common-Mode Input Voltage

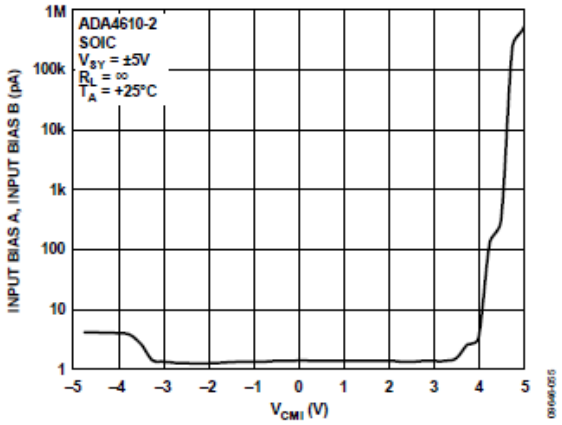

Figure 8. Input Bias Current vs. Common Mode Voltage

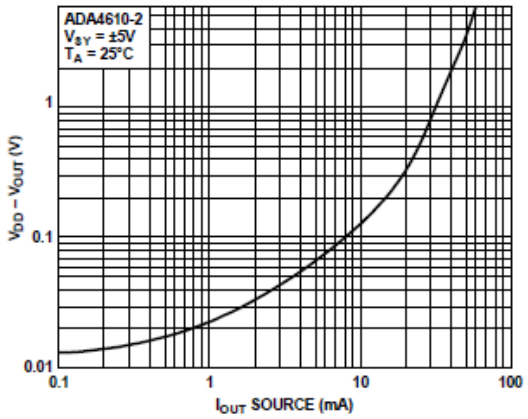

Figure 11. Dropout Voltage vs. Source Current

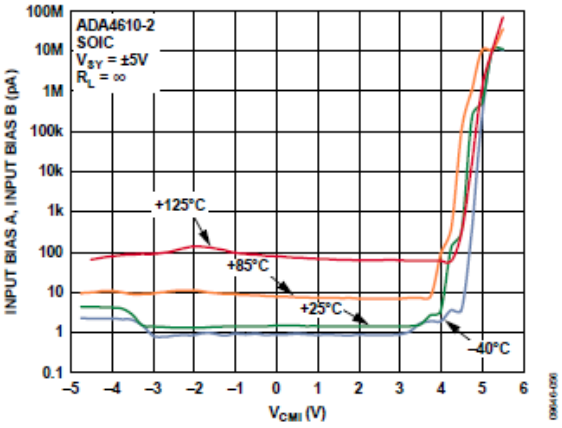

Figure 9. Input Bias Current vs. Common Mode Voltage and Temperature

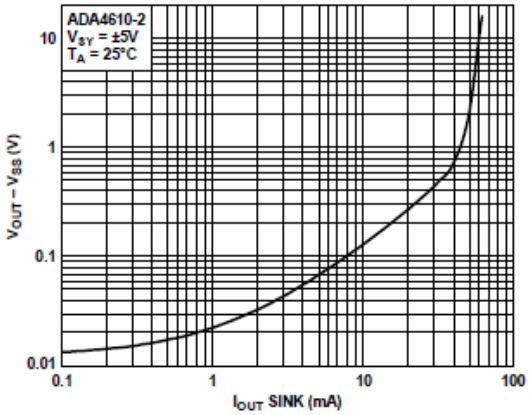

Figure 12. Dropout Voltage vs. Sink Current

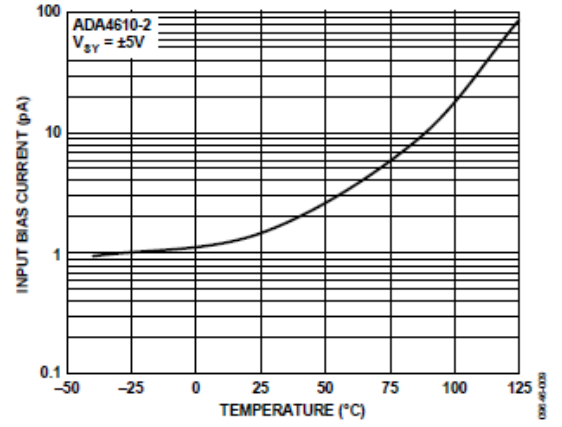

Figure 10. Input Bias Current vs. Temperature

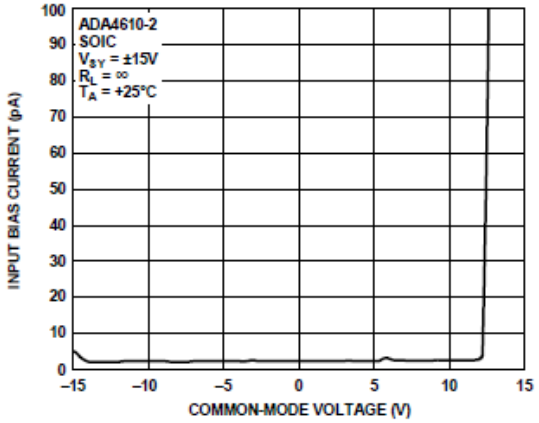

Figure 13. Input Bias Current vs. Common-Mode Voltage

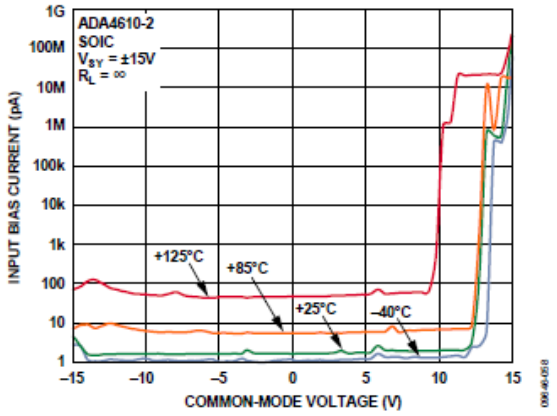

Figure 14. Input Bias Current vs. Common-Mode Voltage and Temperature

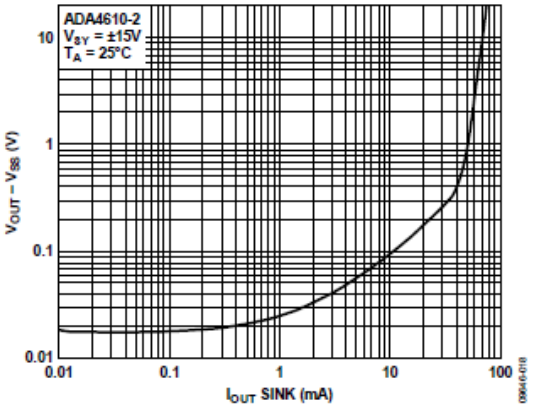

Figure 17. Dropout Voltage vs. Sink Current

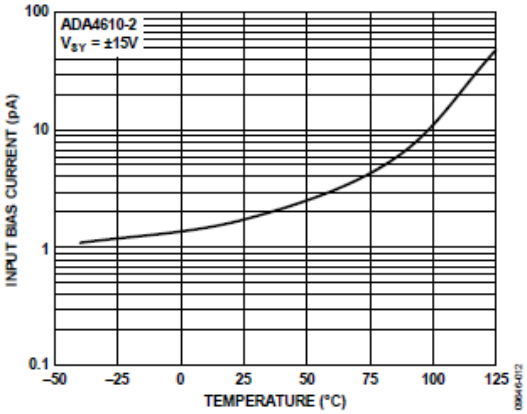

Figure 15. Input Bias Current vs. Temperature

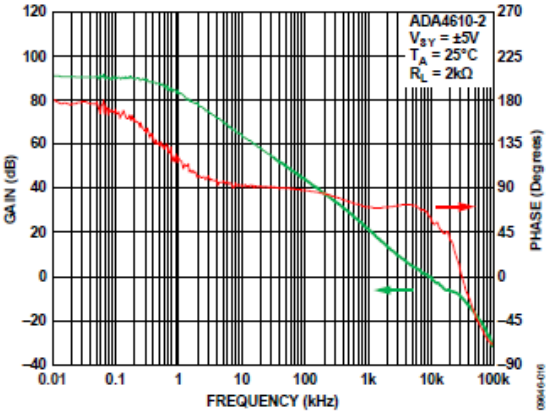

Figure 18. Open-Loop Gain and Phase vs. Frequency

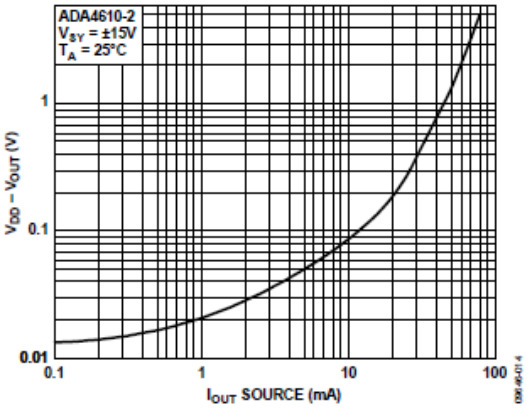

Figure 16. Dropout Voltage vs. Source Current

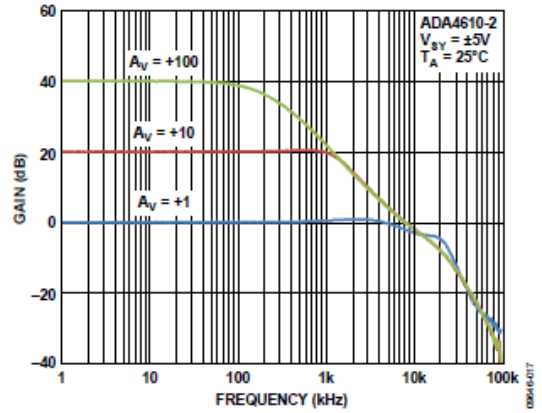

Figure 19. Closed-Loop Gain vs. Frequency

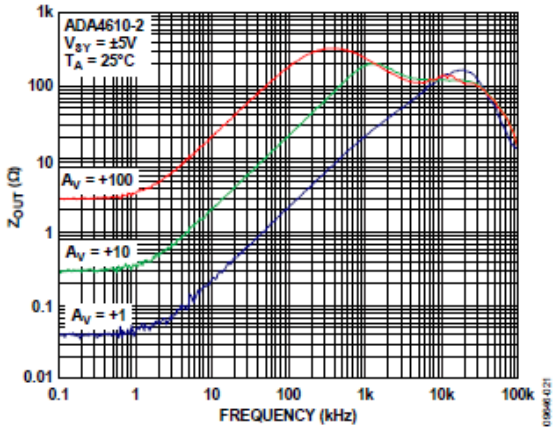

Figure 20. Closed-Loop Output Impedance vs. Frequency

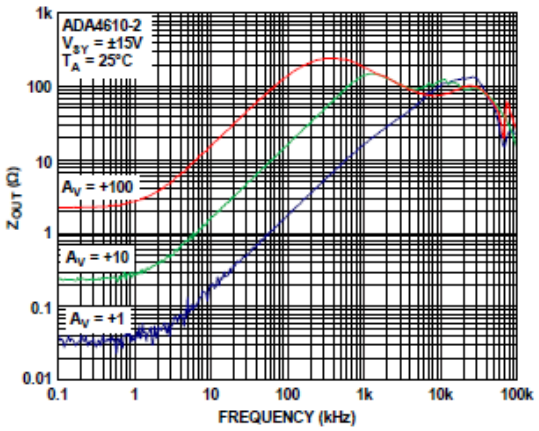

Figure 23. Closed-Loop Output Impedance vs. Frequency

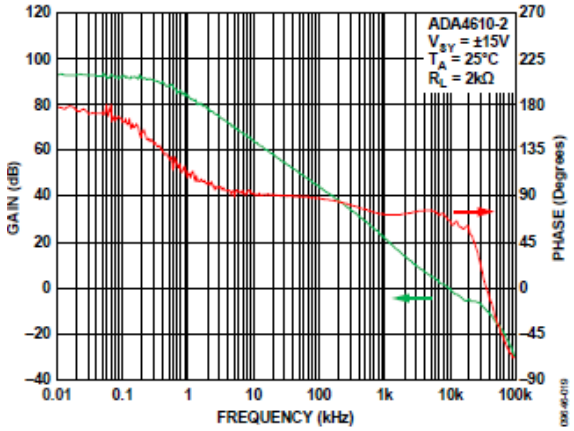

Figure 21. Open-Loop Gain and Phase vs. Frequency

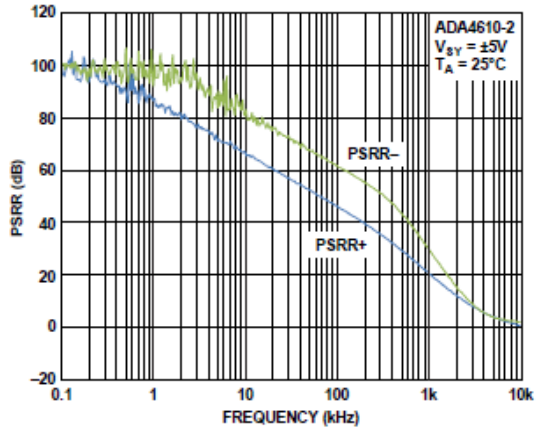

Figure 24. PSRR vs. Frequency

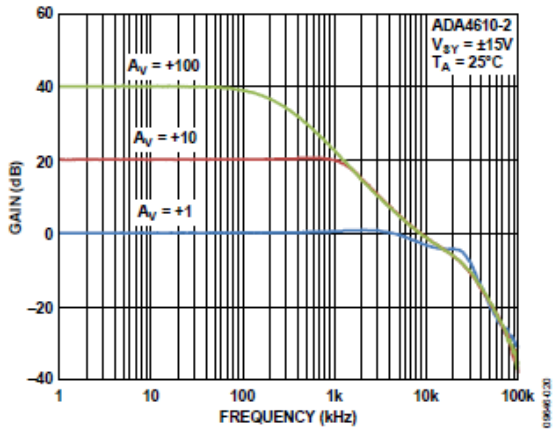

Figure 22. Closed-Loop Gain vs. Frequency

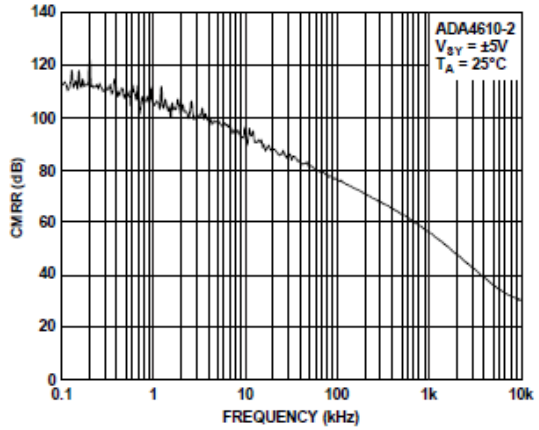

Figure 25. CMRR vs. Frequency

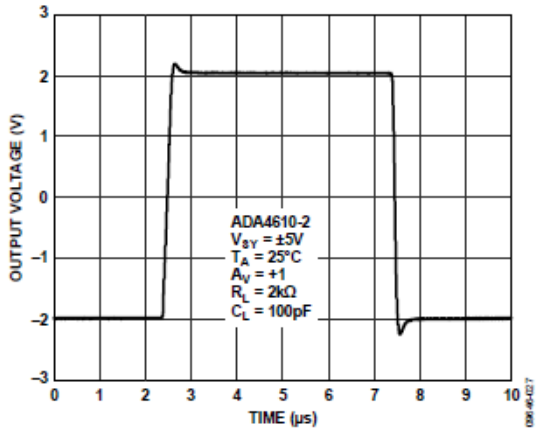

Figure 26. Large Signal Transient Response

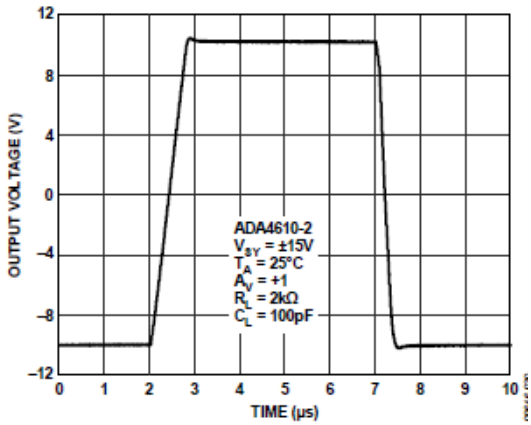

Figure 29. Large Signal Transient Response

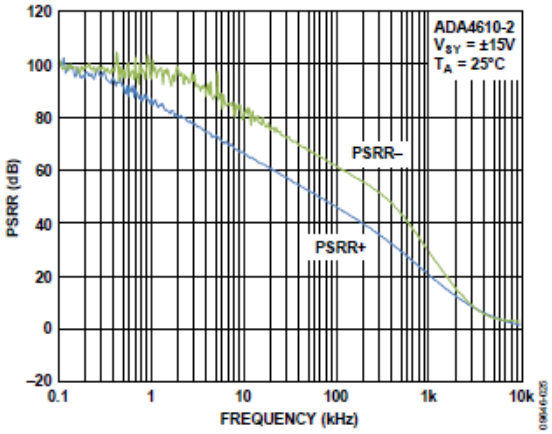

Figure 27. PSRR vs. Frequency

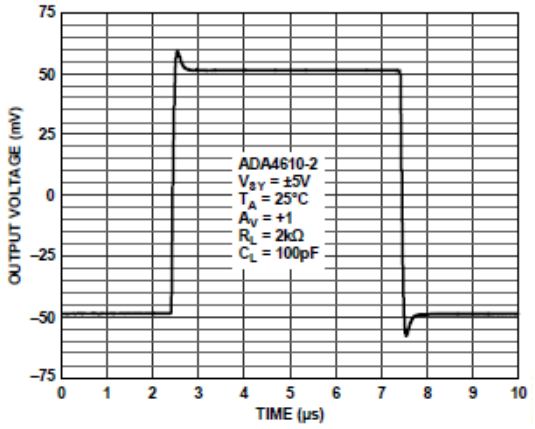

Figure 30. Small Signal Transient Response

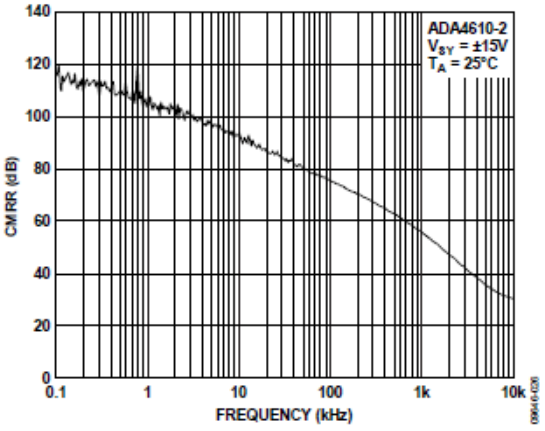

Figure 28. CMRR vs. Frequency

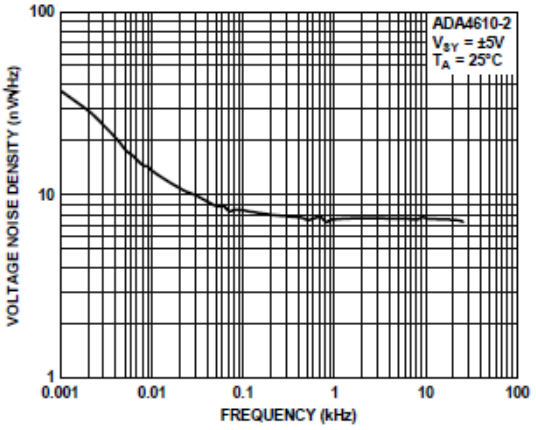

Figure 31. Voltage Noise Density

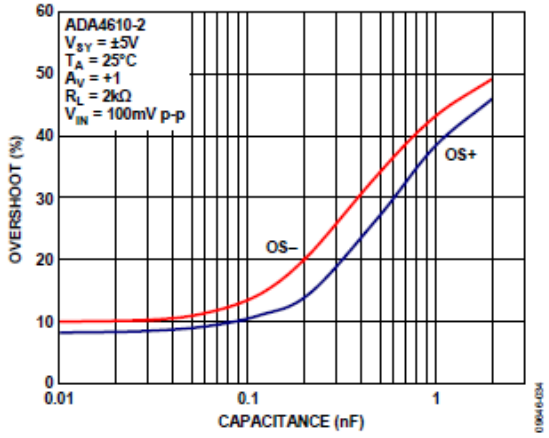

Figure 32. Overshoot vs. Load Capacitance

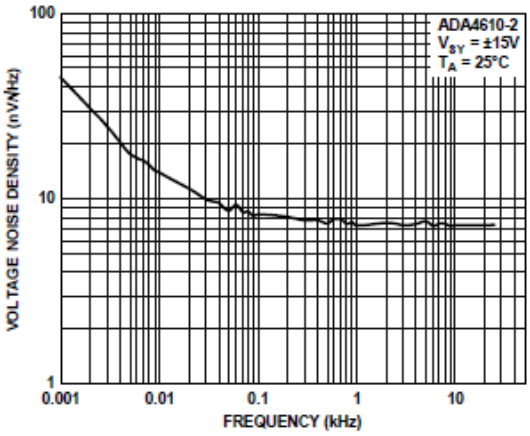

Figure 34. Voltage Noise Density

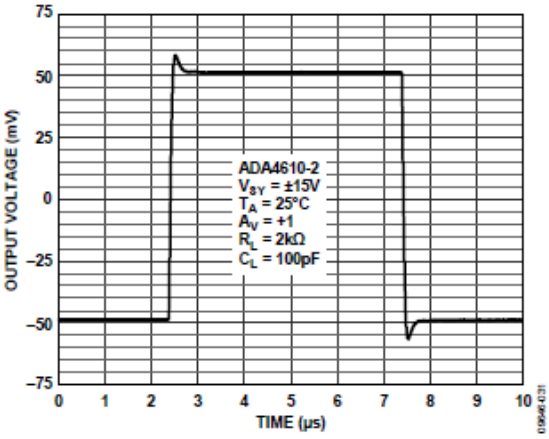

Figure 33. Small Signal Transient Response

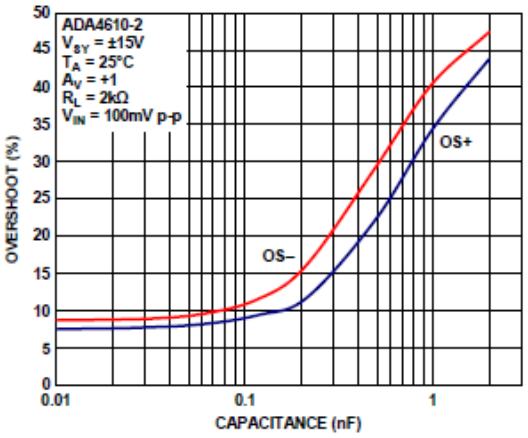

Figure 35. Overshoot vs. Load Capacitance

Comparative Voltage and Varitive Voltage Graphs

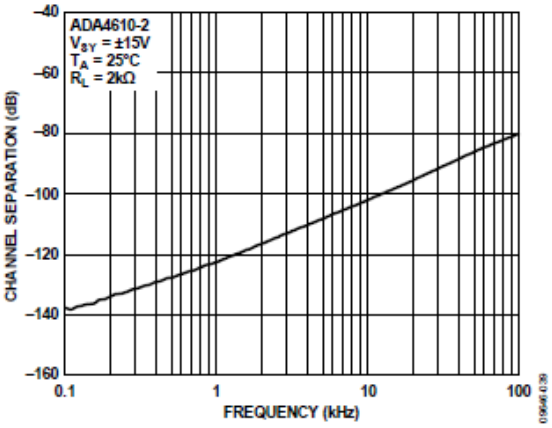

Figure 36. Channel Separation

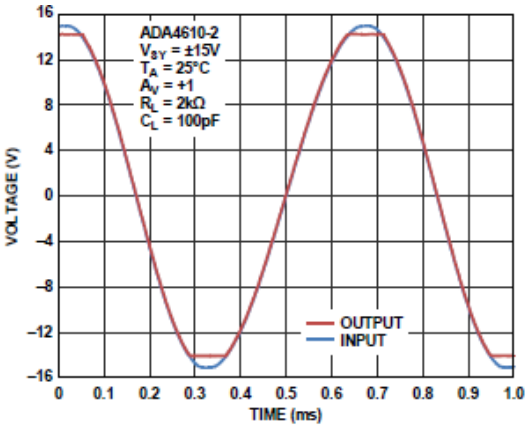

Figure 39. No Phase Reversal

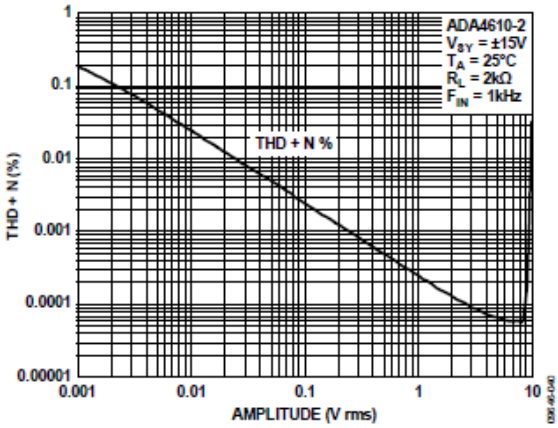

Figure 37. THD + N vs. Amplitude

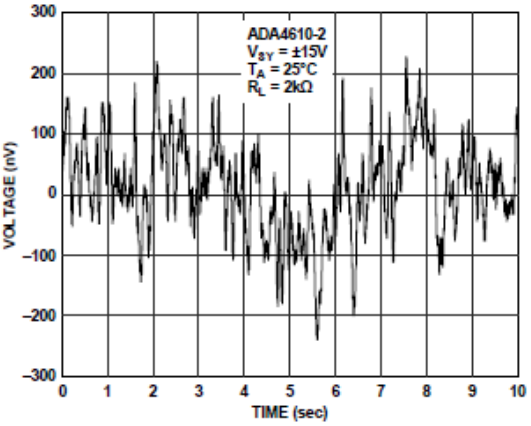

Figure 40. Voltage Noise, 0.1 Hz to 10 Hz

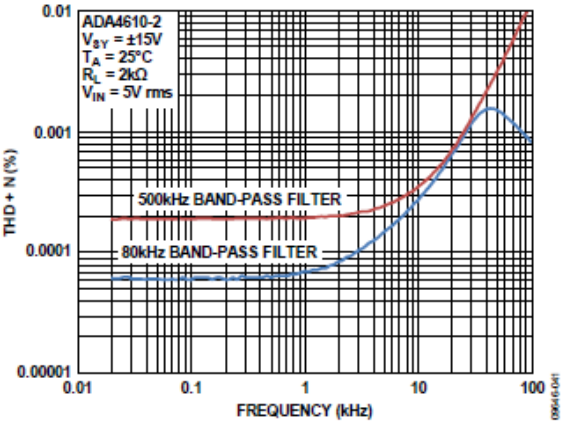

Figure 38. THD + N vs. Frequency

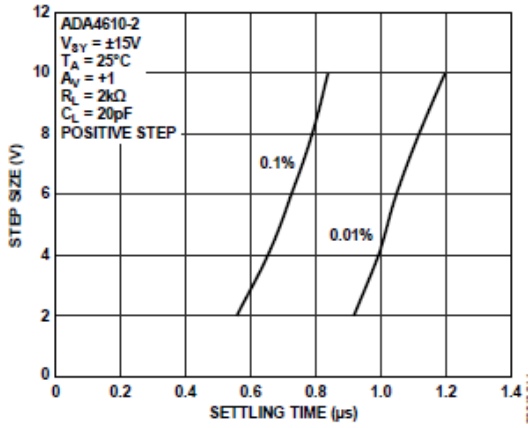

Figure 41. Positive Step Settling Time

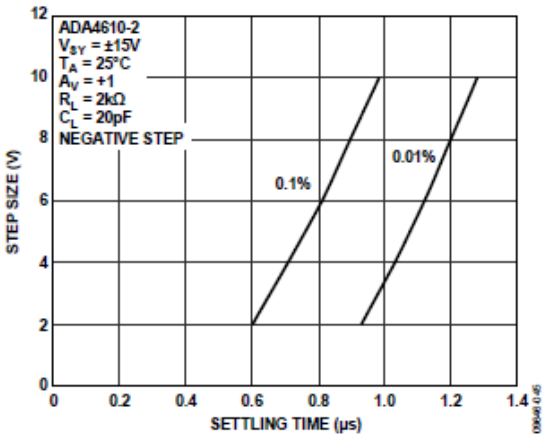

Figure 42. Negative Step Settling Time

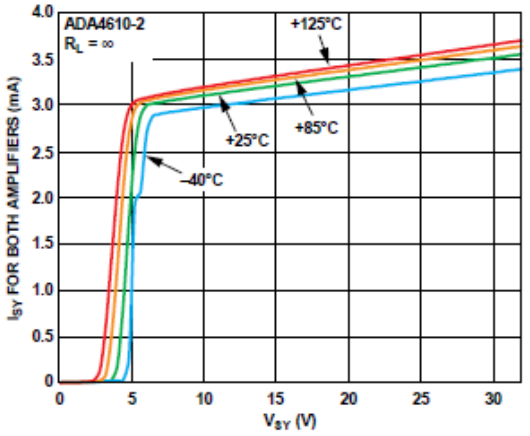

Figure 43. Supply Current vs. Supply Voltage and Temperature

7.3. INPUT OVERVOLTAGE PROTECTION

The ADA4610 have internal protective circuitry that allows voltages as high as 0.7 V beyond the supplies to be applied at the input of either terminal without causing damage. For higher input voltages, a series resistor is necessary to limit the input current. The resistor value can be determined from the formula

$$\frac{V_{IN} - V_S}{R_S} \leq 5mA$$

7.4. COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp may be used as a comparator; however, this is not recommended for any rail-to-rail output op amp. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the part operating open loop, the second stage increases the current drive to the ratioed mirror to close the loop. However, the second stage cannot close the loop, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 44). Configuring an unused section as a voltage follower with the noninverting input connected to a voltage within the input voltage range is recommended. The ADA4610 has a unique output stage design that reduces the excess supply current, but does not entirely eliminate this effect when the op amp is operating open loop.

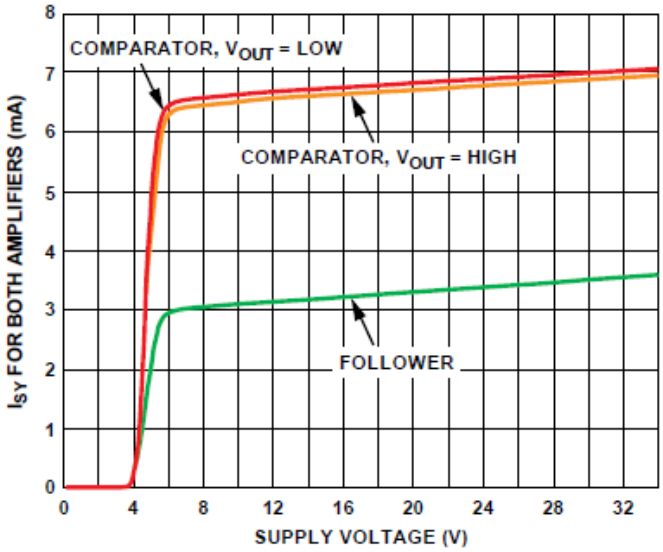

Figure 44. Supply Current vs. Supply Voltage

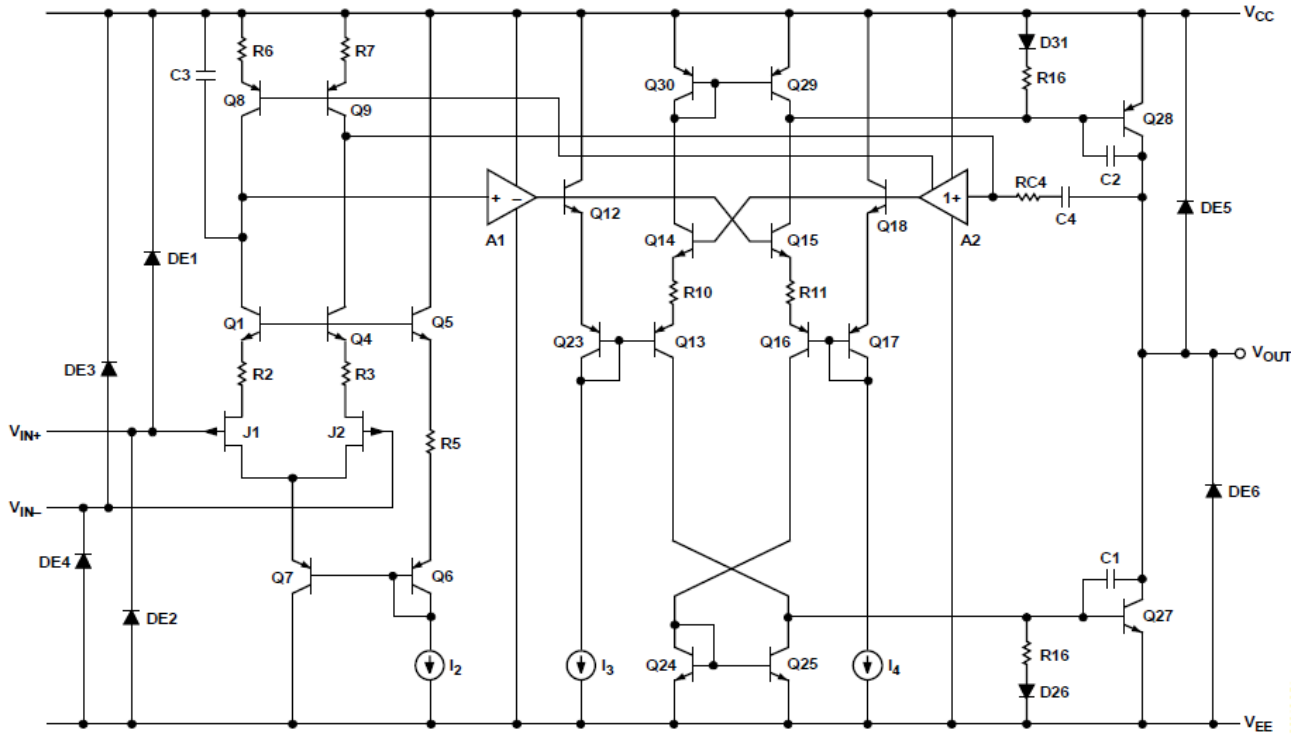

Figure 45. Simplified Schematic

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4610R703F	−55°C to +125°C	10 Lead Bottom Brazed Flat Pack	CDFP3-F10

Revision History		
Rev	Description of Change	Date
A	Initial Release	Nov 8, 2013

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