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REVISION HISTORY

4/07—Rev. 0 to Rev. A

Updated Layout ... 5
Changes to Figure 45 Caption ... 12
Added Figure 48 ... 12
Changes to Figure 51 Caption ... 13

2/07—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V, V_{CM} = 0 V, V_O = 0 V, T_A = +25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			10	120	μV
		−40°C ≤ T_A ≤ +125°C			180	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.8	2.2	μV/°C
Input Bias Current	I_B			25	180	nA
		−40°C ≤ T_A ≤ +125°C			300	nA
Input Offset Current	I_{OS}			25	180	nA
		−40°C ≤ T_A ≤ +125°C			220	nA
Input Voltage Range	IVR	V_{DD} = ±15 V	−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	−12.5 V ≤ V_{CM} ≤ +12.5 V	120	140		dB
		−40°C ≤ T_A ≤ +125°C	115			dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 600 Ω, V_O = −11 V to +11 V	110	116		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
Input Capacitance	C_{DIFF}			4.8		pf
	C_{CM}			4.5		pf
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 600 Ω	13.1	13.4		V
		−40°C ≤ T_A ≤ +125°C	12.8			V
		R_L = 2 kΩ	13.5	13.7		V
		−40°C ≤ T_A ≤ +125°C	13.2			V
Output Voltage Low	V_{OL}	R_L = 600 Ω		−13.2	−12.9	V
		−40°C ≤ T_A ≤ +125°C			−12.8	V
		R_L = 2 kΩ		−13.5	−13.4	V
		−40°C ≤ T_A ≤ +125°C			−13.3	V
Output Source Circuit	I_{SC}			±52		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, A_V = 1		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{DD} = ±18 V to ±4.5 V	120	140		dB
		−40°C ≤ T_A ≤ +125°C	118			dB
Supply Current per Amplifier	I_{SY}			4.7	5.7	mA
		−40°C ≤ T_A ≤ +125°C			6.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	A_V = −1, R_L = 2 kΩ		16.8		V/μs
		A_V = 1, R_L = 2 kΩ		15		V/μs
Settling Time	t_s	To 0.01%, step = 10 V		2		μs
Gain Bandwidth Product	GBP			10		MHz
Phase Margin	ϕ_M			68		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		76		nV
Voltage Noise Density	e_n	f = 1 kHz		1.07	1.15	nV/√Hz
		f = 10 Hz			1.5	nV/√Hz
Current Noise		f = 1 kHz		1.5		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	G = 1, R_L ≥ 1 kΩ, f = 1 kHz, V_{RMS} = 3 V		−108		dB
		G = 1, R_L ≥ 1 kΩ, f = 20 kHz, V_{RMS} = 3 V		−105		dB
Channel Separation	CS	f = 10 kHz		−120		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	GND to V_{DD}
Differential Input Voltage	±1 V
Output Short-Circuit to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R-8)	120	36	°C/W

POWER SEQUENCING

The op amp supplies must be established simultaneously with, or before, any input signals are applied.

If this is not possible, the input current must be limited to 10 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

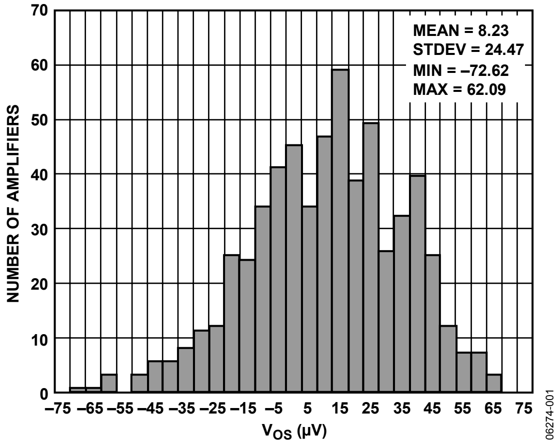

Figure 2. Input Offset Voltage Distribution, V_S = ±5 V

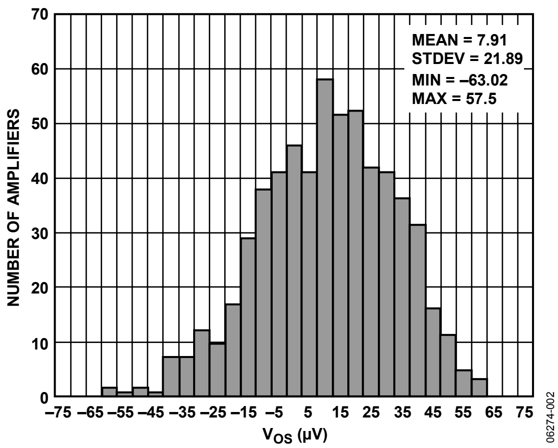

Figure 3. Input Offset Voltage Distribution, V_S = ±15 V

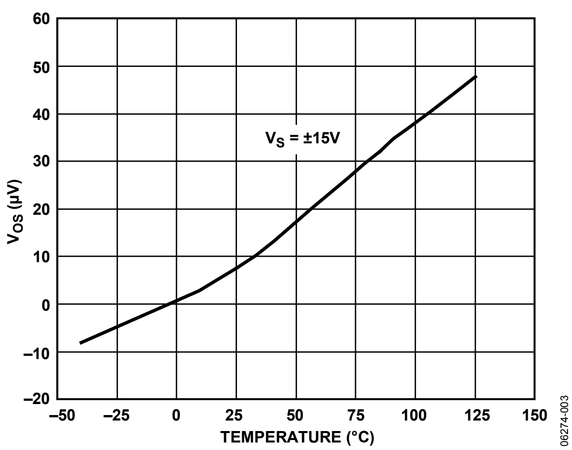

Figure 4. Input Offset Voltage vs. Temperature

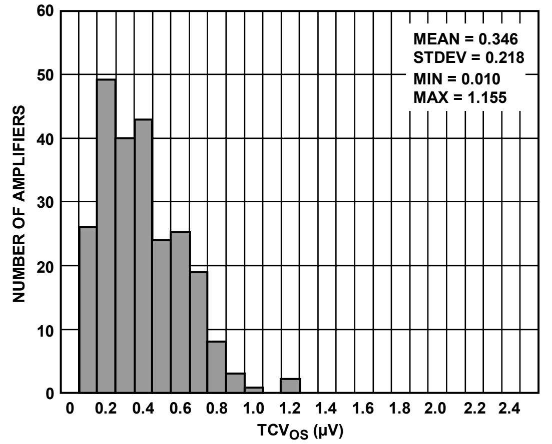

Figure 5. TCV_{OS} Distribution, V_S = ±5 V, −40°C ≤ T_A ≤ +125°C

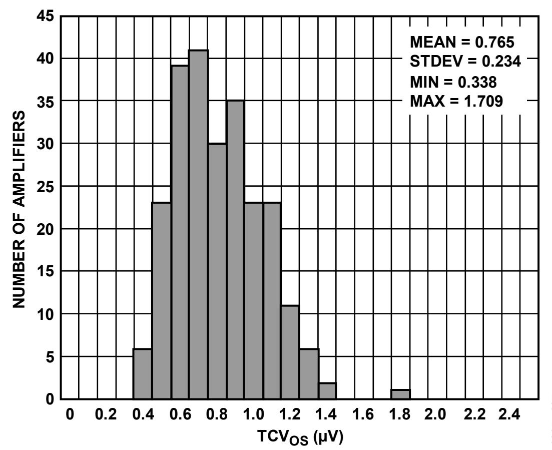

Figure 6. TCV_{OS} Distribution, V_S = ±15 V, −40°C ≤ T_A ≤ +125°C

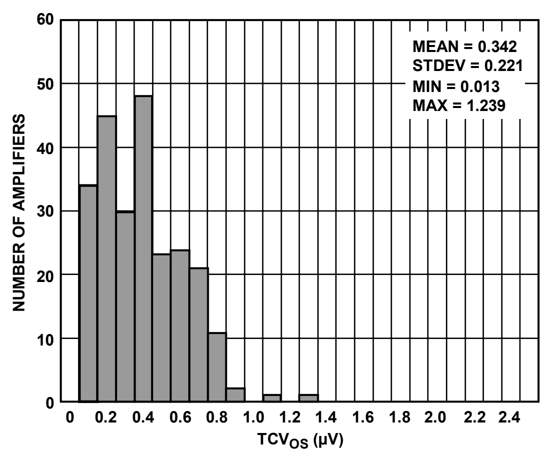

Figure 7. TCV_{OS} Distribution, V_S = ±15 V , −40°C ≤ T_A ≤ +85°C

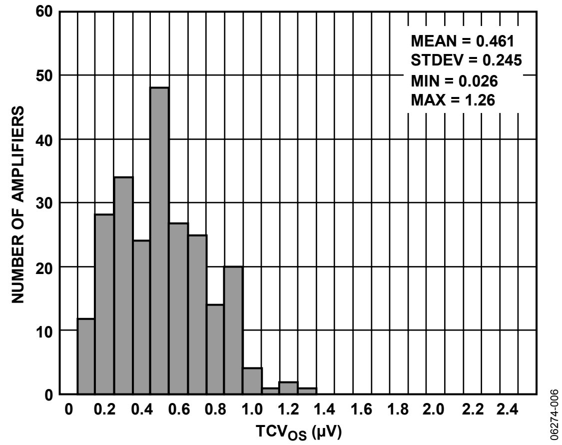

Figure 8. TCV_{OS} Distribution, V_S = ±5 V, −40°C ≤ T_A ≤ +85°C

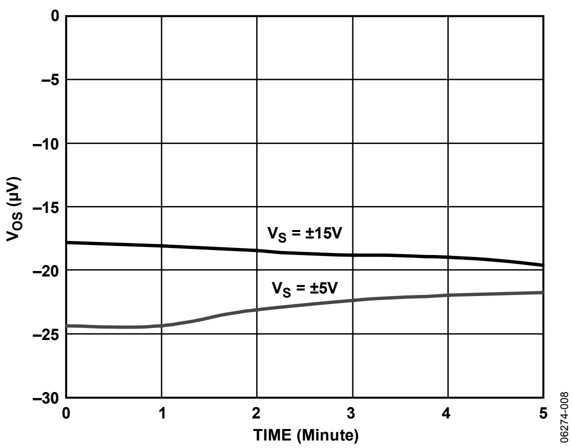

Figure 9. Offset Voltage vs. Time

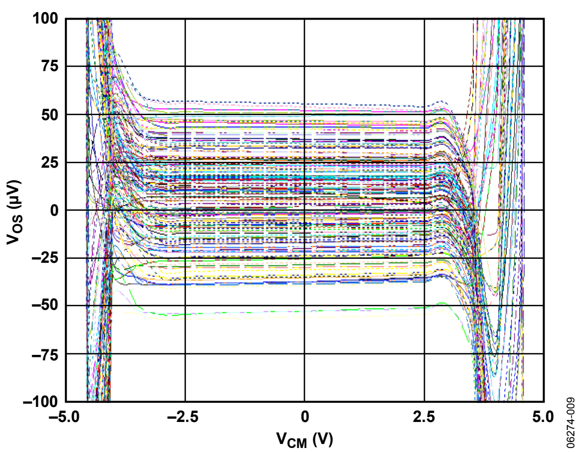

Figure 10. Offset Voltage vs. Common-Mode Voltage, V_S = ±5 V

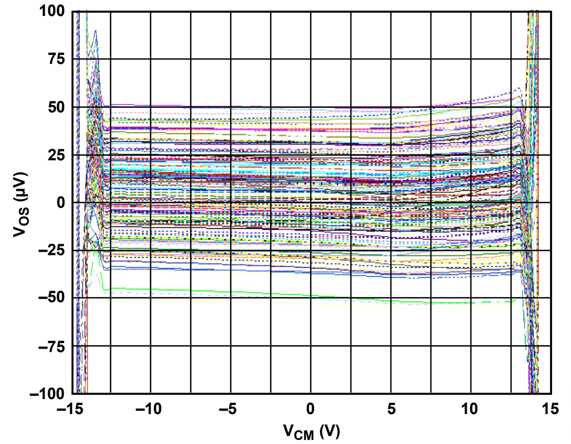

Figure 11. Offset Voltage vs. V_{CM}, V_S = ±15 V

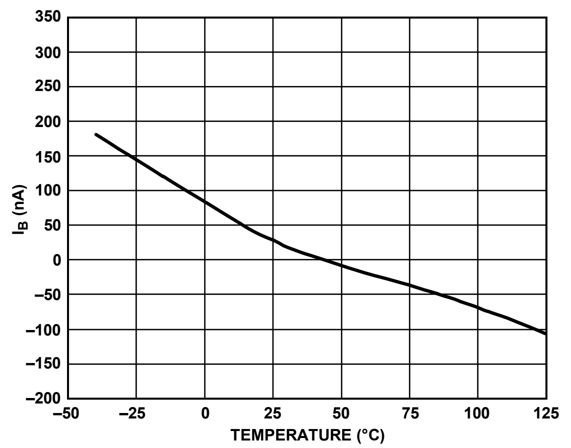

Figure 12. Input Bias Current vs. Temperature, V_S = ±5 V, V_{CM} = 0 V

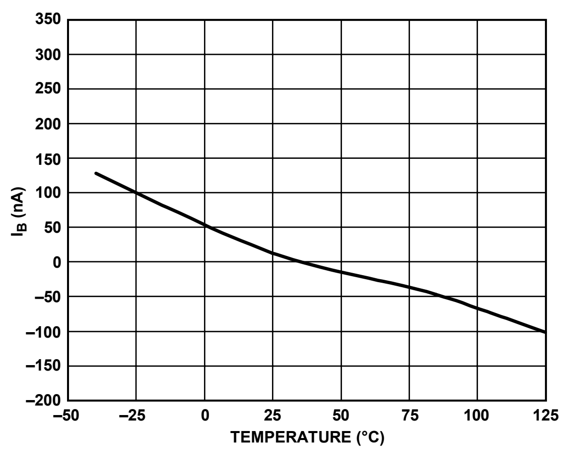

Figure 13. Input Bias Current vs. Temperature, V_S = ±15 V, V_{CM} = 0 V

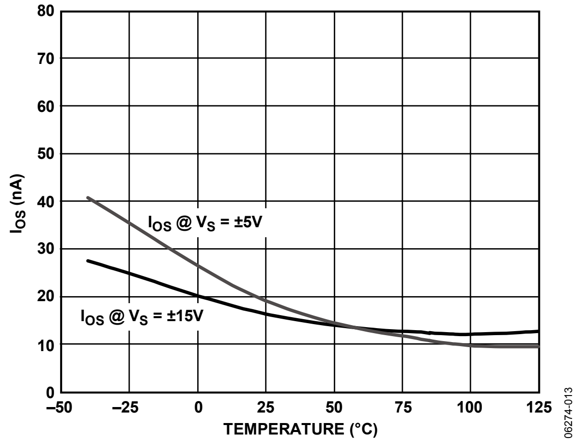

Figure 14. Input Offset Current vs. Temperature

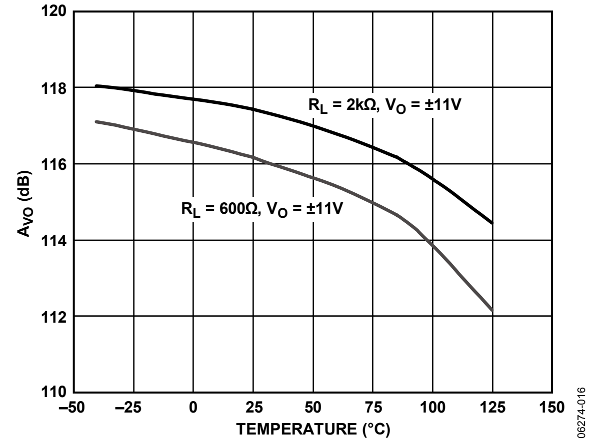

Figure 17. Large Signal Voltage Gain vs. Temperature, V_S = ±15 V

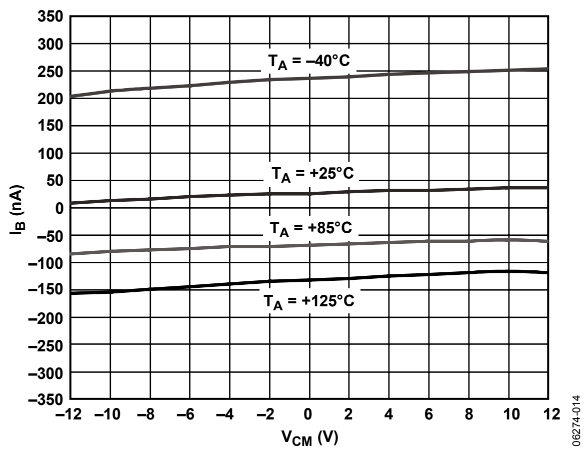

Figure 15. Input Bias Current vs. Voltage Common Mode; V_S = ±15 V

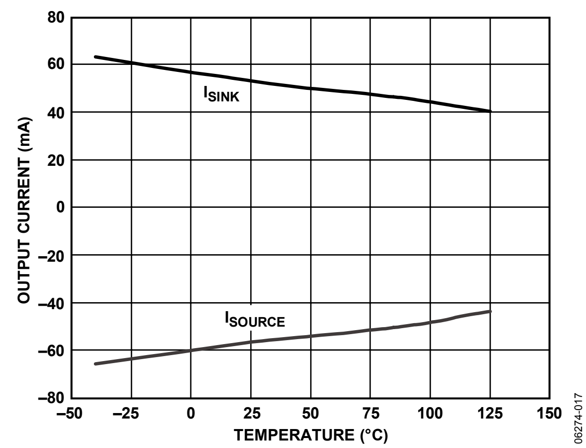

Figure 18. Output Current vs. Temperature, V_S = ±5 V

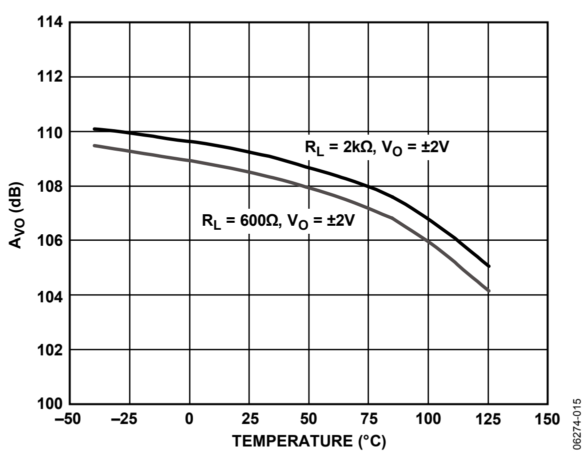

Figure 16. Large Signal Voltage Gain vs. Temperature, V_S = ±5 V

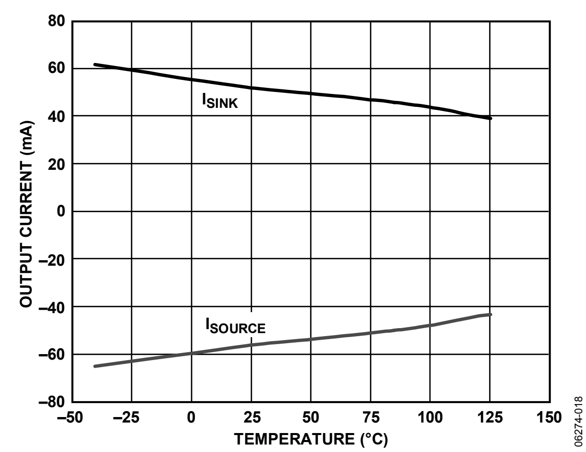

Figure 19. Output Current vs. Temperature, V_S = ±15 V

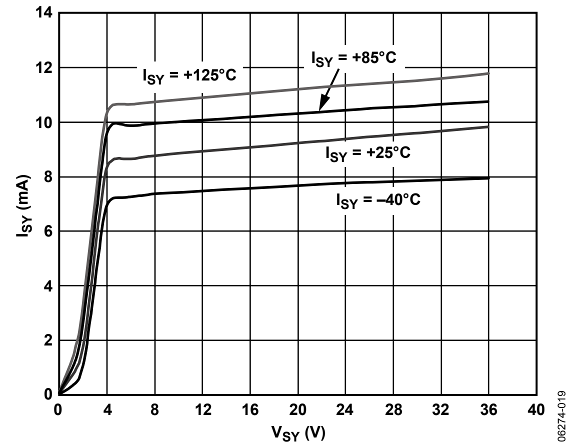

Figure 20. Supply Current vs. Supply Voltage

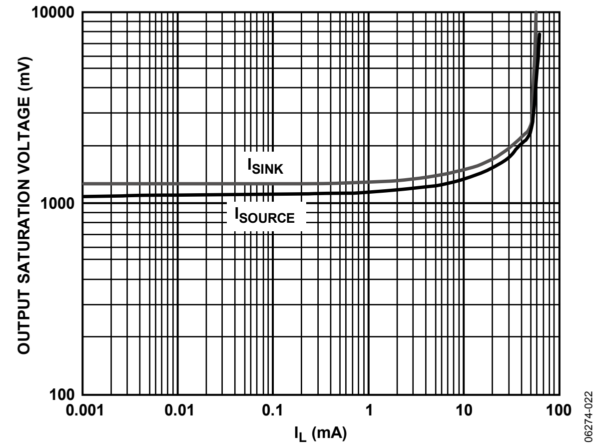

Figure 23. Output Saturation Voltage vs. Current Load, V_S = ±15 V

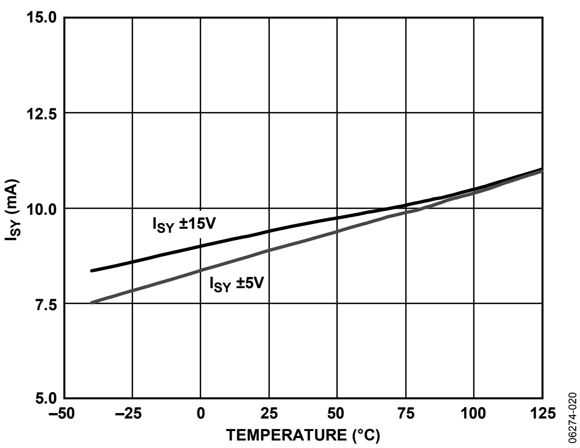

Figure 21. Supply Current vs. Temperature

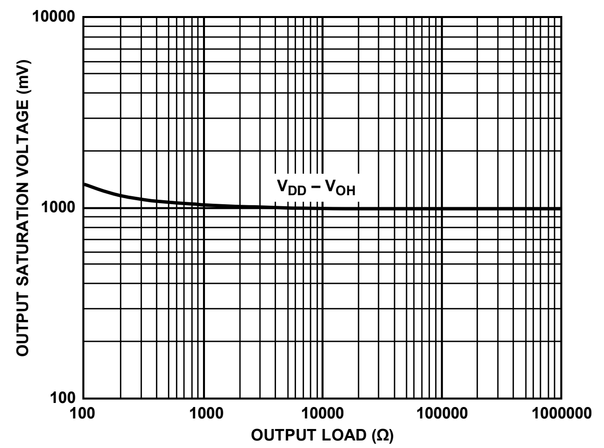

Figure 24. Output Saturation Voltage vs. R_L, V_S = ±5 V

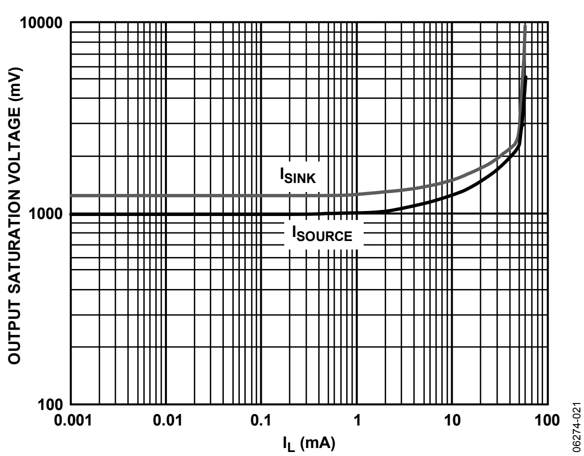

Figure 22. Output Saturation Voltage vs. Current Load, V_S = ±5 V

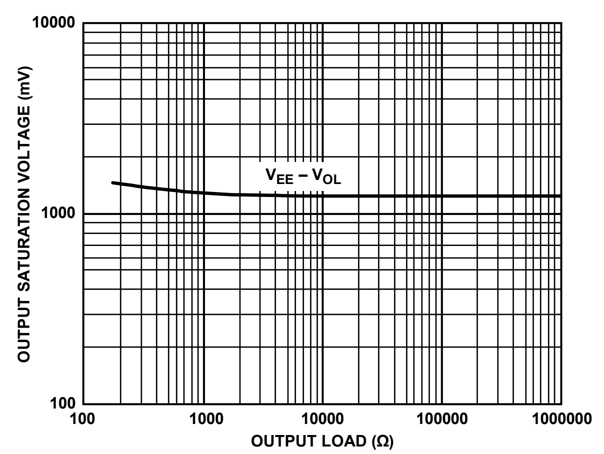

Figure 25. Output Saturation Voltage vs. R_L, V_S = ±5 V

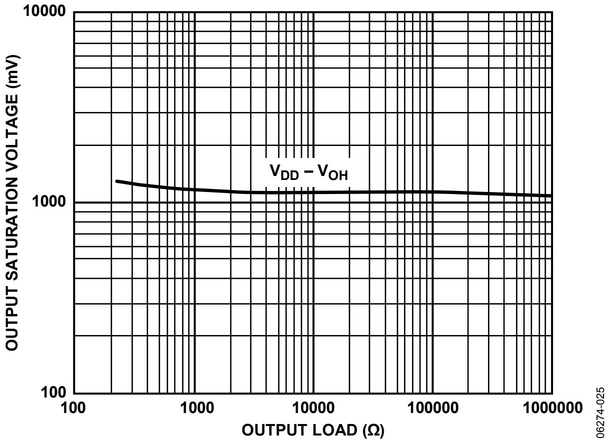

Figure 26. Output Saturation Voltage vs. R_L, V_S = ±15 V

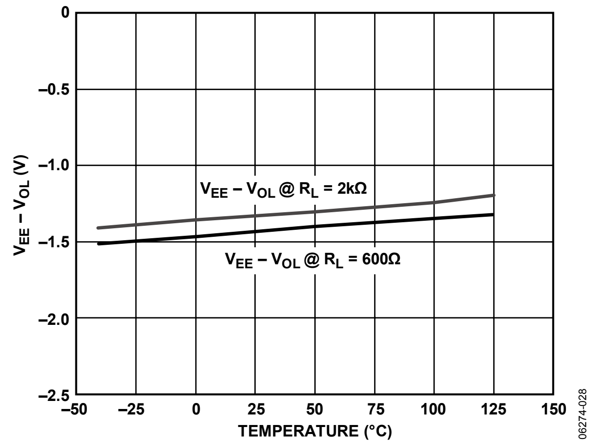

Figure 29. Output Saturation Voltage vs. Temperature, V_S = ±5 V

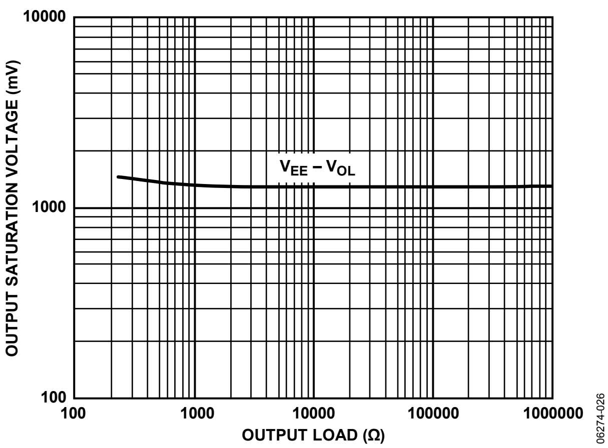

Figure 27. Output Saturation Voltage vs. R_L, V_S = ±15 V

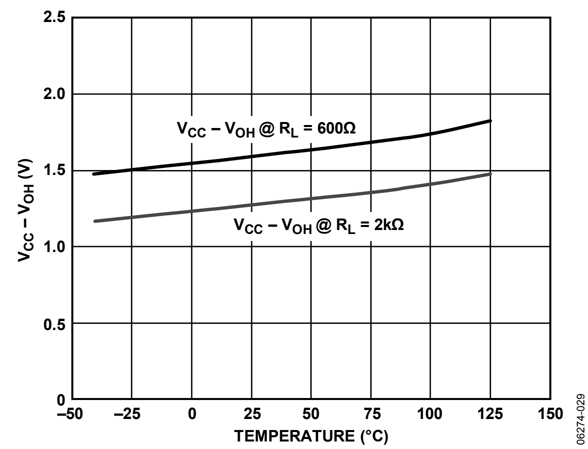

Figure 30. Output Saturation Voltage vs. Temperature, V_S = ±15 V

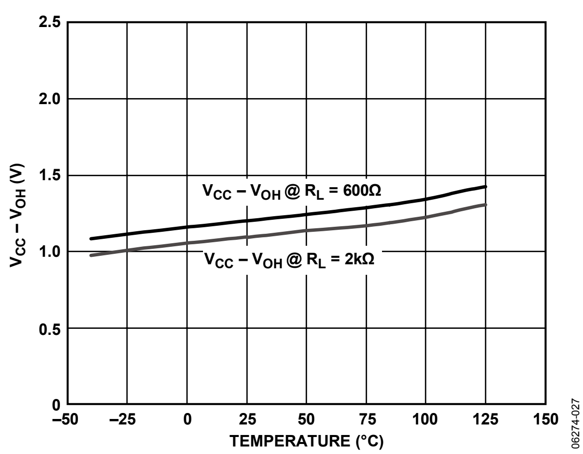

Figure 28. Output Saturation Voltage vs. Temperature, V_S = ±5 V

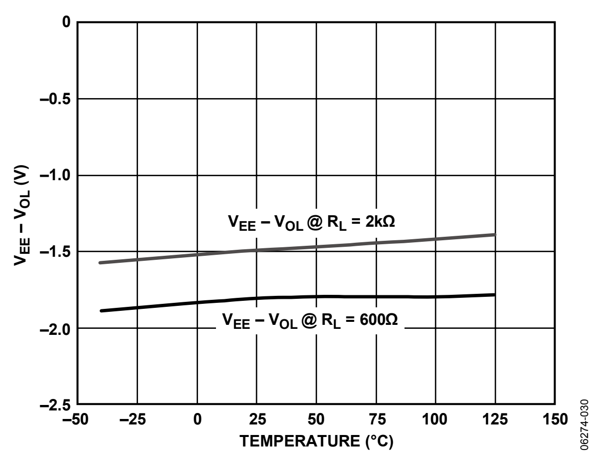

Figure 31. Output Saturation Voltage vs. Temperature, V_S = ±15 V

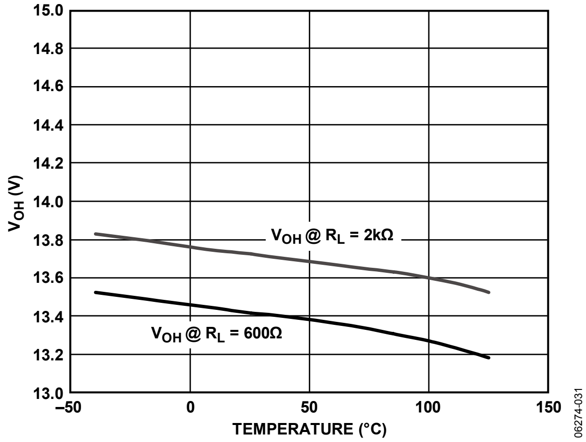

Figure 32. Output Voltage High vs. Temperature, V_S = ±15 V

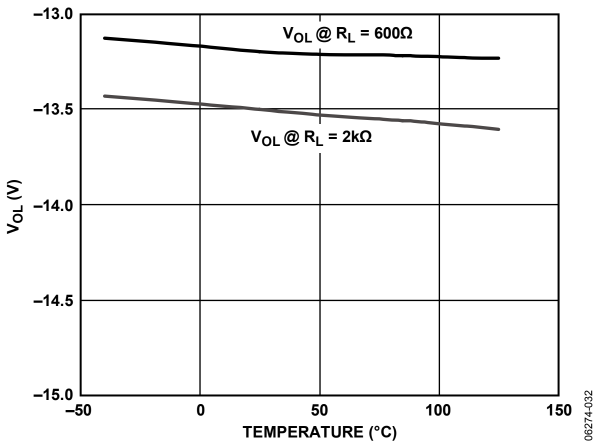

Figure 33. Output Voltage Low vs. Temperature, V_S = ±15 V

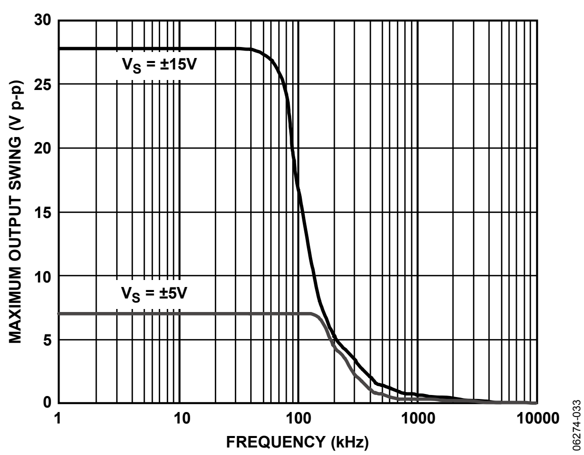

Figure 34. Maximum Output Swing vs. Frequency

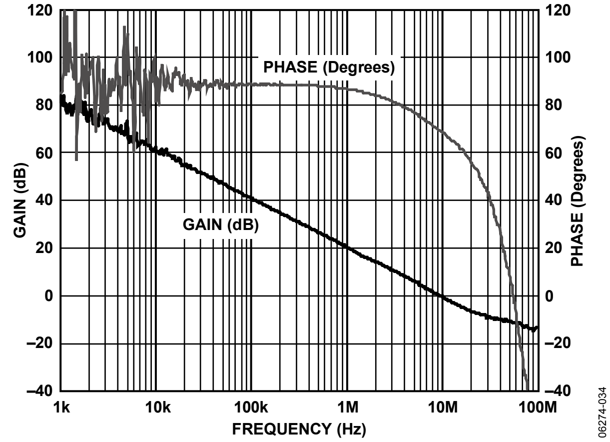

Figure 35. Gain and Phase vs. Frequency, ±5 V ≤ V_S ≤ ±15 V

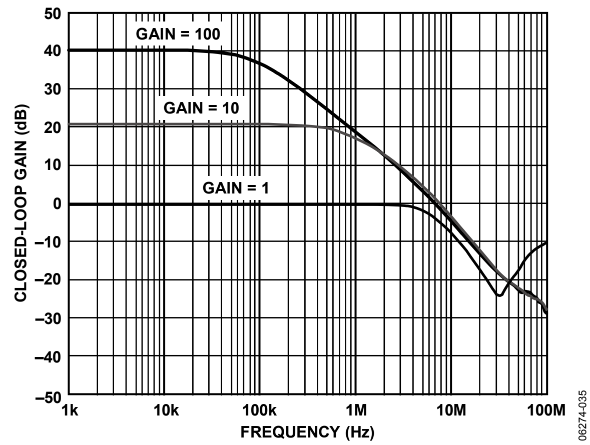

Figure 36. Closed-Loop Gain vs. Frequency, ±5 V ≤ V_S ≤ ±15 V

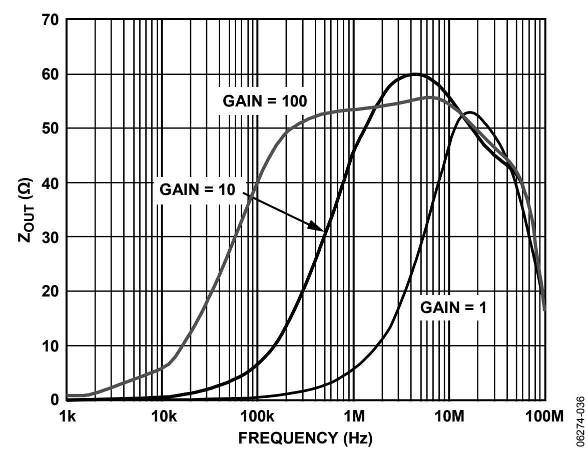

Figure 37. Closed-Loop Output Impedance vs. Frequency, ±5 V ≤ V_S ≤ ±15 V

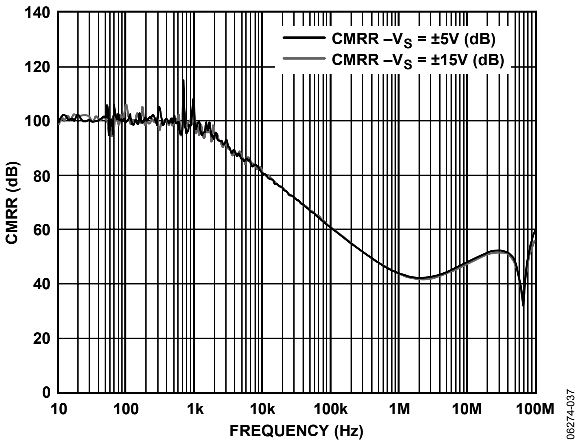

Figure 38. Common-Mode Rejection Ratio vs. Frequency

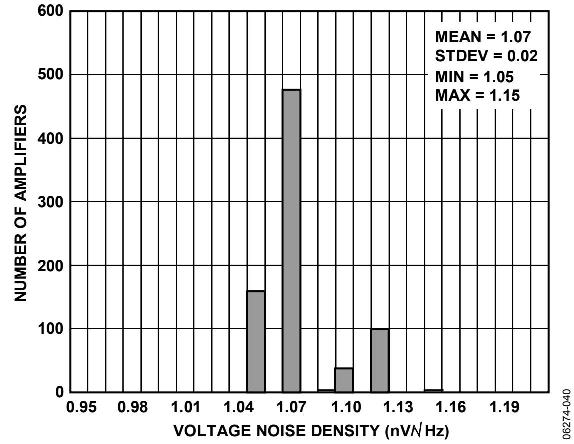

Figure 41. Voltage Noise Density @ 1 kHz, ±5 V ≤ V_S ≤ ±15 V

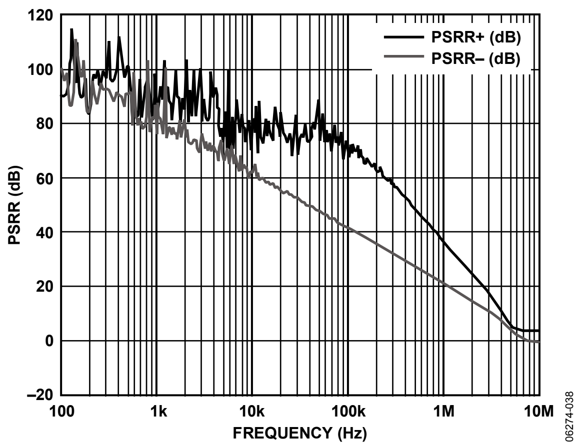

Figure 39. Power Supply Rejection Ratio vs. Frequency, ±5 V ≤ V_S ≤ ±15 V

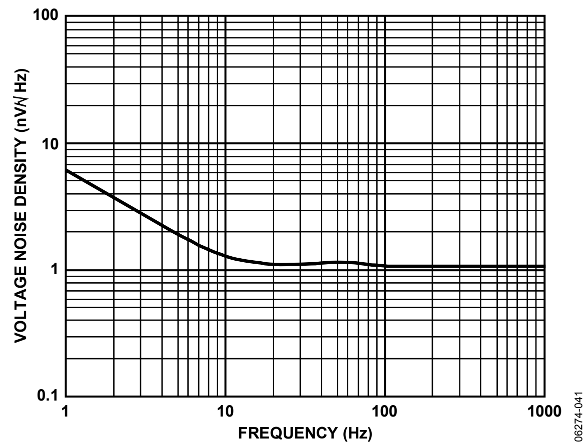

Figure 42. Voltage Noise Density vs. Frequency, ±5 V ≤ V_S ≤ ±15 V

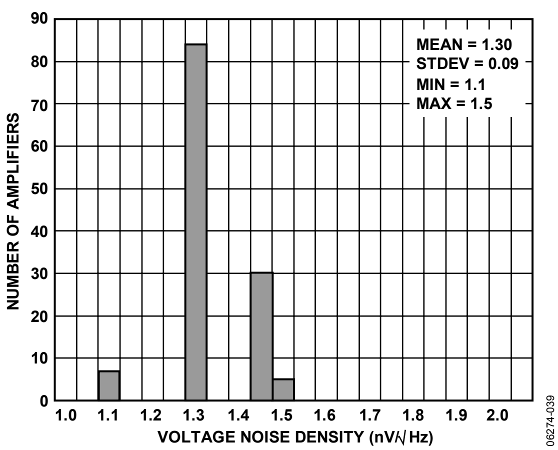

Figure 40. Voltage Noise Density @ 10 kHz, ±5 V ≤ V_S ≤ ±15 V

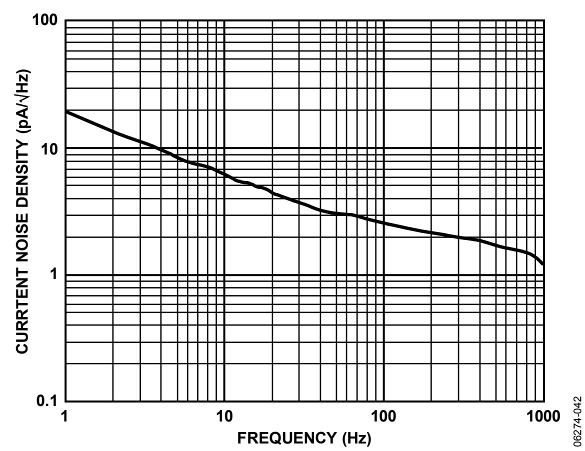

Figure 43. Current Noise Density vs. Frequency, ±5 V ≤ V_S ≤ ±15 V

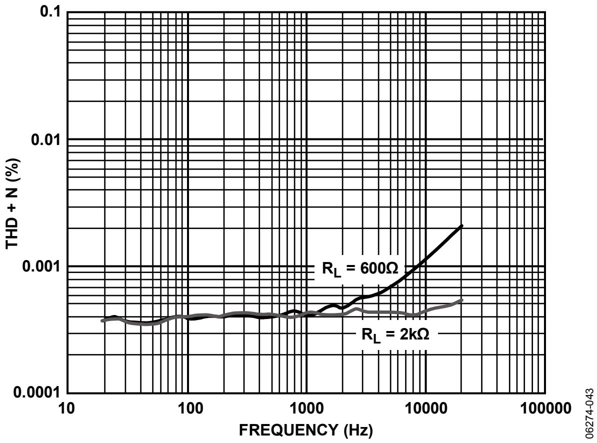

Figure 44. Total Harmonic Distortion + Noise vs. Frequency, V_S = ±15 V, V_{IN} = 3 V rms

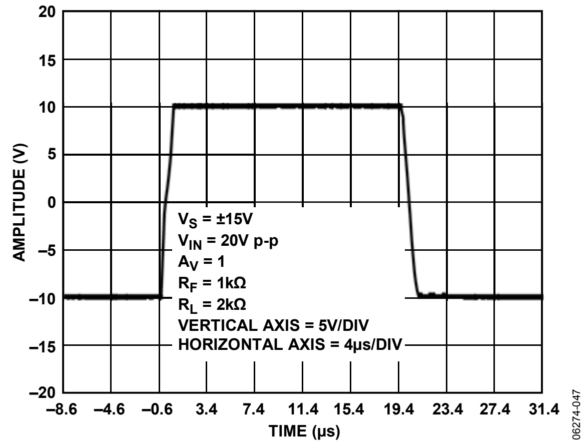

Figure 47. Large Signal Response, A_V = 1

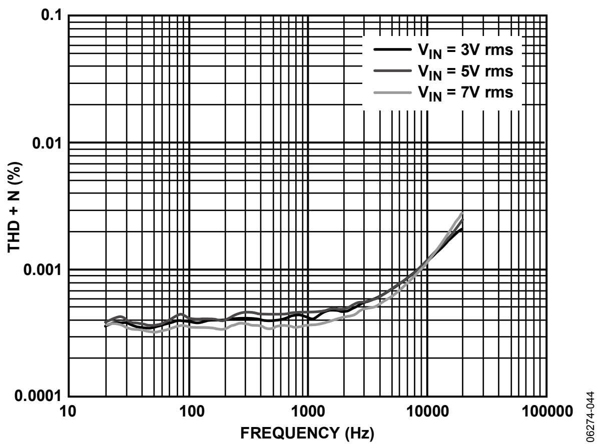

Figure 45. Total Harmonic Distortion + Noise vs. Frequency, V_S = ±15 V

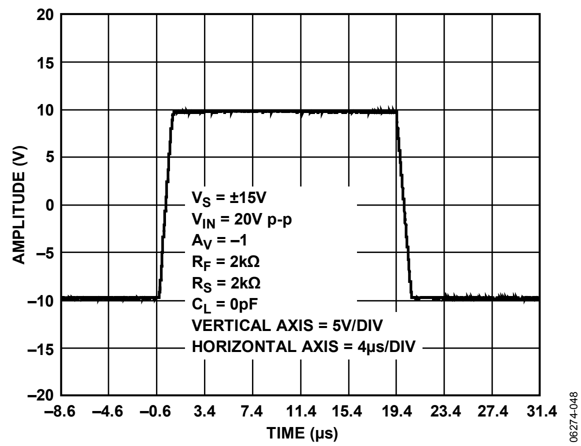

Figure 48. Large Signal Response, A_V = −1

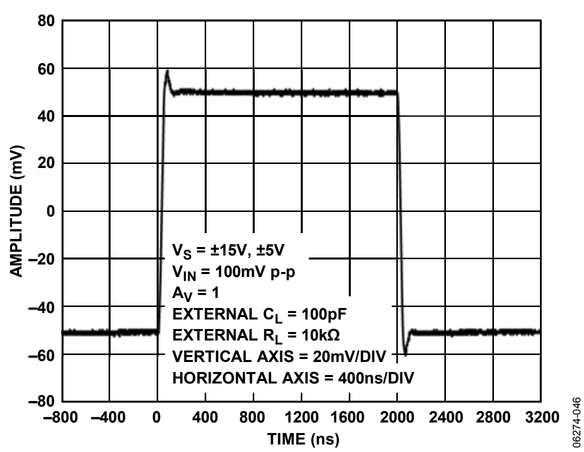

Figure 46. Small Signal Response

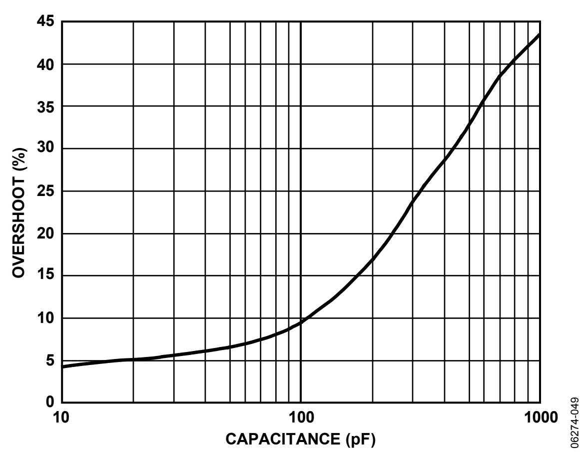

Figure 49. Overshoot vs. Capacitance, ±5 V ≤ V_S ≤ ±15 V, A_V = 1, R_L = 10 kΩ

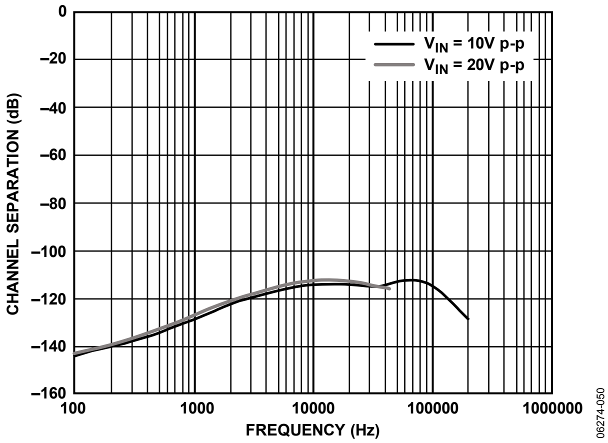

Figure 50. Channel Separation vs. Frequency, $V_S = \pm 15$ V, $A_V = 100$, $R_L = 1$ kΩ

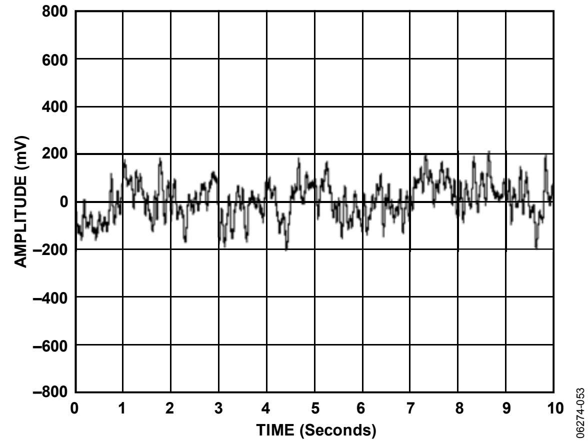

Figure 51. Peak-to-Peak Noise, ± 5 V ≤ V_S ≤ ± 15 V, $A_V = 1$ M

OUTLINE DIMENSIONS

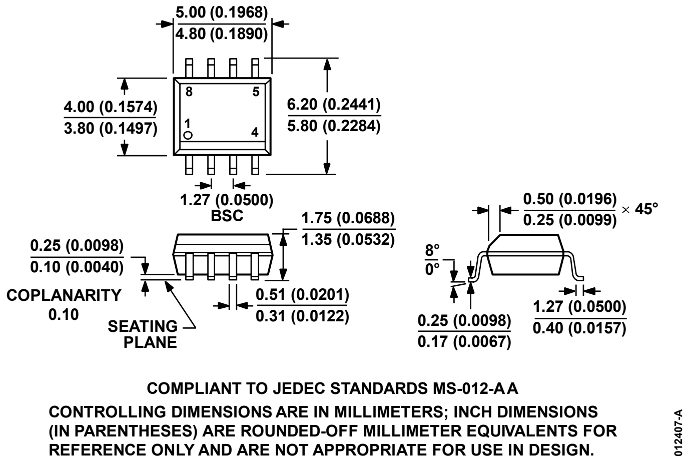

Figure 52. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8599ARZ[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8599ARZ-REEL[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8599ARZ-REEL7[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.

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