

AD607—SPECIFICATIONS

(@ T_A = 25°C, Supply = 3.0 V, IF = 10.7 MHz, unless otherwise noted.)

Model	Conditions	AD607ARS			Unit
		Min	Typ	Max	
DYNAMIC PERFORMANCE					
MIXER					
Maximum RF and LO Frequency Range	For Conversion Gain > 20 dB		500		MHz
Maximum Mixer Input Voltage	For Linear Operation; Between RFHI and RFLO		±54		mV
Input 1 dB Compression Point	RF Input Terminated in 50 Ω		-15		dBm
Input Third-Order Intercept	RF Input Terminated in 50 Ω		-5		dBm
Noise Figure	Matched Input, Max Gain, f = 83 MHz, IF = 10.7 MHz		14		dB
	Matched Input, Max Gain, f = 144 MHz, IF = 10.7 MHz		12		dB
Maximum Output Voltage at MXOP	Z _{IF} = 165 Ω, at Input Compression		±1.3		V
Mixer Output Bandwidth at MXOP	-3 dB, Z _{IF} = 165 Ω		45		MHz
LO Drive Level	Mixer LO Input Terminated in 50 Ω		-16		dBm
LO Input Impedance	LOIP to VMID		1		kΩ
Isolation, RF to IF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		30		dB
Isolation, LO to IF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		20		dB
Isolation, LO to RF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		40		dB
Isolation, IF to RF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		70		dB
IF AMPLIFIERS					
Noise Figure	Max Gain, f = 10.7 MHz		17		dB
Input 1 dB Compression Point	IF = 10.7 MHz		-15		dBm
Output Third-Order Intercept	IF = 10.7 MHz		18		dBm
Maximum IF Output Voltage at IFOP	Z _{IF} = 600 Ω		±560		mV
Output Resistance at IFOP	From IFOP to VMID		15		Ω
Bandwidth	-3 dB at IFOP, Max Gain		45		MHz
GAIN CONTROL					
Gain Control Range	(See Figures 23 and 24) Mixer + IF Section, GREF to 1.5 V		90		dB
Gain Scaling	GREF to 1.5 V		20		mV/dB
	GREF to General Reference Voltage V _R		75/V _R		dB/V
Gain Scaling Accuracy	GREF to 1.5 V, 80 dB Span		±1		dB
Bias Current at GAIN			5		μA
Bias Current at GREF			1		μA
Input Resistance at GAIN, GREF			1		MΩ
I AND Q DEMODULATORS					
Required DC Bias at DMIP			VPOS/2		V dc
Input Resistance at DMIP	From DMIP to VMID		50		kΩ
Input Bias Current at DMIP			2		μA
Maximum Input Voltage	IF > 3 MHz		±150		mV
	IF ≤ 3 MHz		±75		mV
Amplitude Balance	IF = 10.7 MHz, Outputs at 600 mV p-p, F = 100 kHz		±0.2		dB
Quadrature Error	IF = 10.7 MHz, Outputs at 600 mV p-p, F = 100 kHz		-1.2		Degrees
Phase Noise in Degrees	IF = 10.7 MHz, F = 10 kHz		-100		dBc/Hz
Demodulation Gain	Sine Wave Input, Baseband Output		18		dB
Maximum Output Voltage	R _L ≥ 20 kΩ		±1.23		V
Output Offset Voltage	Measured from I _{OUT} , Q _{OUT} to VMID	-150	+10	+150	mV
Output Bandwidth	Sine Wave Input, Baseband Output		1.5		MHz
PLL					
Required DC Bias at FDIN			VPOS/2		V dc
Input Resistance at FDIN	From FDIN to VMID		50		kΩ
Input Bias Current at FDIN			200		nA
Frequency Range			0.4 to 12		MHz
Required Input Drive Level	Sine Wave Input at Pin 1		400		mV
Acquisition Time to ±3°	IF = 10.7 MHz		16.5		μs
POWER-DOWN INTERFACE					
Logical Threshold	For Power Up on Logical High		2		V dc
Input Current for Logical High			75		μA
Turn-On Response Time	To PLL Locked		16.5		μs
Standby Current			550		μA
POWER SUPPLY					
Supply Range		2.92		5.5	V
Supply Current	Midgain, IF = 10.7 MHz		8.5		mA
OPERATING TEMPERATURE					
T _{MIN} to T _{MAX}	Operation to 2.92 V Minimum Supply Voltage	-25		+85	°C
	Operation to 4.5 V Minimum Supply Voltage	-40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage VPS1, VPS2 to COM1, COM2	5.5 V
Internal Power Dissipation ²	600 mW
2.92 V to 5.5 V Operating Temperature Range	-25°C to +85°C
4.5 V to 5.5 V Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

¹ Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² Thermal Characteristics: 20-lead SSOP Package: $\theta_{JA} = 126^{\circ}\text{C}/\text{W}$.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD607ARS	-25°C to +85°C for 2.92 V to 5.5 V Operation; -40°C to +85°C for 4.5 V to 5.5 V Operation	20-Lead Plastic SSOP	RS-20

CAUTION

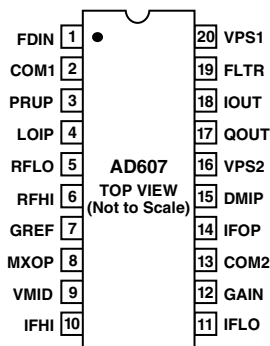
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD607 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Reads	Function
1	FDIN	Frequency Detector Input	PLL Input for I/Q Demodulator Quadrature Oscillator, ± 400 mV Drive Required from External Oscillator. Must be biased at $V_P/2$.
2	COM1	Common #1	Supply Common for RF Front End and Main Bias
3	PRUP	Power-Up Input	3 V/5 V CMOS compatible power-up control; logical high = powered-up; max input level = $V_{PS1} = V_{PS2}$.
4	LOIP	Local Oscillator Input	LO input, ac-coupled ± 54 mV LO input is required (-16 dBm for 50Ω input termination).
5	RFLO	RF "Low" Input	Usually Connected to AC Ground
6	RFHI	RF "High" Input	AC-Coupled, ± 56 mV, Max RF Input for Linear Operation
7	GRES	Gain Reference Input	High Impedance Input, typically 1.5 V, sets gain scaling.
8	MXOP	Mixer Output	High Impedance, Single-Sided Current Output, ± 1.3 V Max Voltage Output (± 6 mA Max Current Output)
9	VMID	Midsupply Bias Voltage	Output of the Midsupply Bias Generator ($VMID = V_{POS}/2$)
10	IFHI	IF "High" Input	AC-Coupled IF Input, ± 56 mV Max Input for Linear Operation
11	IFLO	IF "Low" Input	Reference Node for IF Input; Auto-Offset Null
12	GAIN	Gain Control Input	High Impedance Input, 0 V–2 V Using 3 V Supply, Max Gain at $V = 0$
13	COM2	Common #2	Supply Common for IF Stages and Demodulator
14	IFOP	IF Output	Low Impedance, Single-Sided Voltage Output, 5 dBm (± 560 mV) Max
15	DMIP	Demodulator Input	Signal input to I and Q demodulators has a ± 150 mV max input at $IF > 3$ MHz for linear operation; ± 75 mV max input at $IF < 3$ MHz for linear operation. Must be biased at $V_P/2$.
16	VPS2	VPOS Supply #2	Supply to High Level IF, PLL, and Demodulators
17	QOUT	Quadrature Output	Low Impedance Q Baseband Output; ± 1.23 V Full Scale in 20 k Ω Min Load; AC-Coupled
18	IOUT	In-Phase Output	Low Impedance I Baseband Output; ± 1.23 V Full Scale in 20 k Ω Min Load; AC-Coupled
19	FLTR	PLL Loop Filter	Series RC PLL Loop Filter, Connected to Ground
20	VPS1	VPOS Supply #1	Supply to Mixer, Low Level IF, PLL, and Gain Control

PIN CONNECTION 20-Lead SSOP (RS-20)



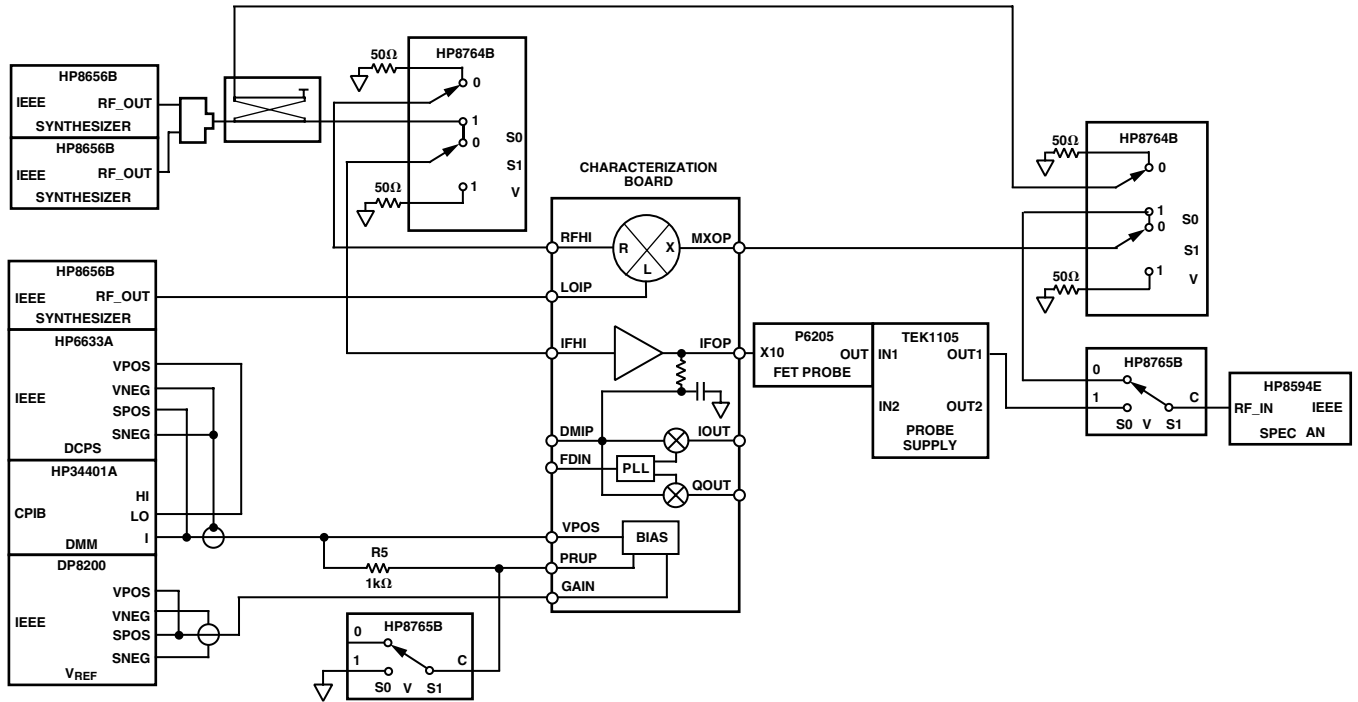


Figure 1. Mixer/Amplifier Test Set

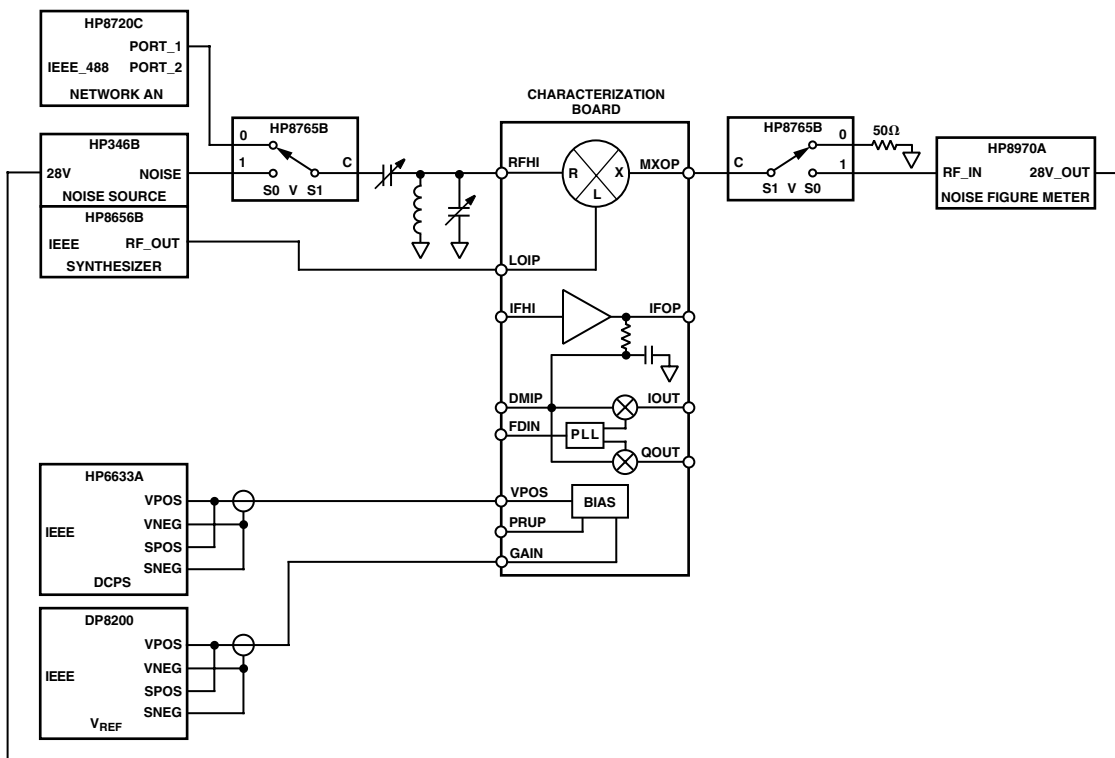


Figure 2. Mixer Noise Figure Test Set



Figure 27b. Evaluation Board Layout, Bottom Side

Table III. AD607 Evaluation Board Input and Output Connections

Reference Designation	Connector Type	Description	Coupling	Approximate Signal Level	Comments
J1	SMA	Frequency Detector Input	DC	± 400 mV	This pin needs to be biased at VMID and ac-coupled when driven by an external signal generator.
J2	SMA	Power-Up	DC	CMOS Logic Level Input	Tied to Positive Supply by Jumper J10
J3	SMA	LO Input	AC	-16 dBm (± 50 mV)	Input is terminated in 50 Ω .
J4	SMA	RF Input	AC	-15 dBm max (± 54 mV)	Input is terminated in 50 Ω .
J5	SMA	MGC Input	DC	0.4 V to 2.0 V (3 V Supply) (GREF = VMID)	Jumper is set for manual gain control input; see Table I for control voltage values.
J6	SMA	IF Output	AC	NA	This signal level depends on the AD607's gain setting.
J7	SMA	Q Output	AC	NA	This signal level depends on the AD607's gain setting.
J8	SMA	I Output	AC	NA	This signal level depends on the AD607's gain setting.
J9	Jumper	Ties GREF to VMID	NA	NA	Sets gain-control scale factor (SF); $SF = 75/VMID$ in dB/V, where $VMID = VPOS/2$.
J10	Jumper	Ties Power-Up to Positive Supply	NA	NA	Remove to test power-up/-down.
T1	Terminal Pin	Power Supply Positive Input (VPS1, VPS2)	DC	DC	2.92 V to 5.5 V Draws 8.5 mA at midgain connection.
T2	Terminal Pin	Power Supply Return (GND)	DC	0 V	

AD607

Revision History

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