



# AD565A—SPECIFICATIONS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 15 V, V<sub>EE</sub> = 15 V, unless otherwise noted.)

Parameter	AD565AJ			AD565AK			Unit
	Min	Typ	Max	Min	Typ	Max	
<b>DATA INPUTS<sup>1</sup></b> (Pins 13 to 24)							
TTL or 5 V CMOS							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"			0.8			0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		120	300		120	300	μA
Bit OFF Logic "0"		35	100		35	100	μA
RESOLUTION			12			12	Bits
<b>OUTPUT</b>							
Current							
Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits On or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	6	8	10	6	8	10	kΩ
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R2 = 50 Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T <sub>MIN</sub> to T <sub>MAX</sub>	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale) 25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±0.35 (0.0084)	LSB % of F.S. Range
T <sub>MIN</sub> to T <sub>MAX</sub>		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY 25°C		±1/2	±3/4		±1/4	±1/2	LSB
T <sub>MIN</sub> to T <sub>MAX</sub>		<b>MONOTONICITY GUARANTEED</b>			<b>MONOTONICITY GUARANTEED</b>		
TEMPERATURE COEFFICIENTS With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL-SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V <sub>CC</sub> , +11.4 to +16.5 V dc		3	5		3	5	mA
V <sub>EE</sub> , -11.4 to -16.5 V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY <sup>2</sup>							
V <sub>CC</sub> = +11.4 to +16.5 V dc		3	10		3	10	ppm of F.S./%
V <sub>EE</sub> = -11.4 to -16.5 V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (See Figures 2, 3, 4)		0 to +5 -2.5 to +2.5			0 to +5 -2.5 to +2.5		V V
		0 to +10 -5 to +5			0 to +10 -5 to +5		V V
		-10 to +10			-10 to +10		V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50 Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15	20	25	15	20	25	kΩ
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads) <sup>3</sup>	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

## NOTES

<sup>1</sup>The digital inputs are guaranteed but not tested over the operating temperature range.

<sup>2</sup>The power supply gain sensitivity is tested in reference to a V<sub>CC</sub>, V<sub>EE</sub> of ±15 V dc.

<sup>3</sup>For operation at elevated temperatures, the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

Specifications subject to change without notice.

# AD565A/AD566A

Parameter	AD565AS			AD565AT			Unit
	Min	Typ	Max	Min	Typ	Max	
DATA INPUTS <sup>1</sup> (Pins 13 to 24)							
TTL or 5 V CMOS							
Input Voltage							
Bit ON Logic "1"	<b>2.0</b>		<b>5.5</b>	<b>2.0</b>		<b>5.5</b>	V
Bit OFF Logic "0"			<b>0.8</b>			<b>0.8</b>	V
Logic Current (Each Bit)							
Bit ON Logic "1"		120	<b>300</b>		120	<b>300</b>	μA
Bit OFF Logic "0"		35	<b>100</b>		35	<b>100</b>	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (All Bits On)	<b>-1.6</b>	-2.0	<b>-2.4</b>	<b>-1.6</b>	-2.0	<b>-2.4</b>	mA
Bipolar (All Bits On or Off)	<b>±0.8</b>	±1.0	<b>±1.2</b>	<b>±0.8</b>	±1.0	<b>±1.2</b>	mA
Resistance (Exclusive of Span Resistors)	6	8	10	6	8	10	kΩ
Offset							
Unipolar		0.01	<b>0.05</b>		0.01	<b>0.05</b>	% of F.S. Range
Bipolar (Figure 3, R2 = 50 Ω Fixed)		0.05	<b>0.15</b>		0.05	<b>0.1</b>	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T <sub>MIN</sub> to T <sub>MAX</sub>	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale) 25°C		±1/4 (0.006)	<b>±1/2</b> <b>(0.012)</b>		±1/8 (0.003)	<b>±0.35</b> <b>(0.0084)</b>	LSB % of F.S. Range
T <sub>MIN</sub> to T <sub>MAX</sub>		±1/2 (0.012)	<b>±3/4</b> <b>(0.018)</b>		±1/4 (0.006)	<b>±1/2</b> <b>(0.012)</b>	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY 25°C		±1/2	<b>±3/4</b>		±1/4	<b>±1/2</b>	LSB
T <sub>MIN</sub> to T <sub>MAX</sub>		<b>MONOTONICITY GUARANTEED</b>			<b>MONOTONICITY GUARANTEED</b>		
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL-SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V <sub>CC</sub> , +11.4 to +16.5 V dc		3	5		3	5	mA
V <sub>EE</sub> , -11.4 to -16.5 V dc		-12	<b>-18</b>		-12	<b>-18</b>	mA
POWER SUPPLY GAIN SENSITIVITY <sup>2</sup>							
V <sub>CC</sub> = +11.4 to +16.5 V dc		3	10		3	10	ppm of F.S./%
V <sub>EE</sub> = -11.4 to -16.5 V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES							
(See Figures 2, 3, 4)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50 Ω Resistor for R2 (Figure 2)		±0.1	<b>±0.25</b>		±0.1	<b>±0.25</b>	% of F.S. Range
Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 3)		±0.05	<b>±0.15</b>		±0.05	<b>±0.1</b>	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15	20	25	15	20	25	kΩ
REFERENCE OUTPUT							
Voltage	<b>9.90</b>	10.00	10.10	<b>9.90</b>	10.00	<b>10.10</b>	V
Current (Available for External Loads) <sup>3</sup>	<b>1.5</b>	2.5		<b>1.5</b>	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specification subject to change without notice.

# AD566A—SPECIFICATIONS (T<sub>A</sub> = 25°C, V<sub>EE</sub> = -15 V, unless otherwise noted)

Parameter	AD566AJ			AD566AK			Unit
	Min	Typ	Max	Min	Typ	Max	
DATA INPUTS <sup>1</sup> (Pins 13 to 24) TTL or 5 V CMOS							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0		0.8	0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		120	300		120	300	μA
Bit OFF Logic "0"		35	100		35	100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits On or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	6	8	10	6	8	10	kΩ
Offset							
Unipolar (Adjustable to Zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 4, R1 and R2 = 50 Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T <sub>MIN</sub> to T <sub>MAX</sub>	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale) 25°C							
T <sub>MIN</sub> to T <sub>MAX</sub>		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±0.35 (0.0084)	LSB % of F.S. Range
		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY 25°C							
T <sub>MIN</sub> to T <sub>MAX</sub>		±1/2	±3/4		±1/4	±1/2	LSB
		<b>MONOTONICITY GUARANTEED</b>			<b>MONOTONICITY GUARANTEED</b>		
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
All Bits ON-to-OFF or OFF-to-ON		250	350		250	350	ns
FULL-SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V <sub>EE</sub> , -11.4 to -16.5 V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY <sup>2</sup>							
V <sub>EE</sub> = -11.4 to -16.5 V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (see Figures 3, 4, 5)							
		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50 Ω Resistor for R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15	20	25	15	20	25	kΩ
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants		Two (2): Bipolar Operation at Digital Input Only					
Reference Voltage		1 V to 10 V, Unipolar					
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1 V dc Reference Voltage					
Reference Feedthrough (Unipolar Mode, All Bits OFF, and 1 V to 10 V [p-p], Sine Wave Frequency for 1/2 LSB [p-p] Feedthrough)		40					kHz typ
Output Slew Rate 10%–90%		5					mA/μs
90%–10%		1					mA/μs
Output Settling Time (All Bits ON and a 0 V–10 V Step Change in Reference Voltage)		1.5 μs to 0.01% F.S.					
CONTROL AMPLIFIER							
Full Power Bandwidth		300					kHz
Small-Signal Closed-Loop Bandwidth		1.8					MHz

## NOTES

<sup>1</sup>The digital input levels are guaranteed but not tested over the temperature range.

<sup>2</sup>The power supply gain sensitivity is tested in reference to a V<sub>EE</sub> of -1.5 V dc.

Specifications subject to change without notice.

# AD565A/AD566A

Parameter	AD566AS			AD566AT			Unit
	Min	Typ	Max	Min	Typ	Max	
DATA INPUTS <sup>1</sup> (Pins 13 to 24) TTL or 5 V CMOS							
Input Voltage							
Bit ON Logic "1"	<b>2.0</b>		<b>5.5</b>	<b>2.0</b>		<b>5.5</b>	V
Bit OFF Logic "0"	<b>0</b>		<b>0.8</b>	<b>0</b>		<b>0.8</b>	V
Logic Current (Each Bit)							
Bit ON Logic "1"		120	<b>300</b>		+120	<b>300</b>	μA
Bit OFF Logic "0"		35	<b>100</b>		+35	<b>100</b>	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (All Bits On)	<b>-1.6</b>	-2.0	<b>-2.4</b>	<b>-1.6</b>	-2.0	<b>-2.4</b>	mA
Bipolar (All Bits On or Off)	<b>±0.8</b>	±1.0	<b>±1.2</b>	<b>±0.8</b>	±1.0	<b>±1.2</b>	mA
Resistance (Exclusive of Span Resistors)	6	8	10	6	8	10	kΩ
Offset							
Unipolar (Adjustable to Zero per Figure 3)		0.01	<b>0.05</b>		0.01	<b>0.05</b>	% of F.S. Range
Bipolar (Figure 4, R1 and R2 = 50 Ω Fixed)		0.05	<b>0.15</b>		0.05	<b>0.1</b>	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T <sub>MIN</sub> to T <sub>MAX</sub>	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale) 25°C							
T <sub>MIN</sub> to T <sub>MAX</sub>		±1/4 (0.006)	<b>±1/2</b> ( <b>0.012</b> )		±1/8 (0.003)	<b>±0.35</b> ( <b>0.0084</b> )	LSB % of F.S. Range
		±1/2 (0.012)	<b>±3/4</b> ( <b>0.018</b> )		±1/4 (0.006)	<b>±1/2</b> ( <b>0.012</b> )	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY 25°C							
T <sub>MIN</sub> to T <sub>MAX</sub>		±1/2	<b>±3/4</b>		±1/4	<b>±1/2</b>	LSB
		<b>MONOTONICITY GUARANTEED</b>			<b>MONOTONICITY GUARANTEED</b>		
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
All Bits ON-to-OFF or OFF-to-ON		250	350		250	350	ns
FULL-SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V <sub>EE</sub> -11.4 to -16.5 V dc		-12	<b>-18</b>		-12	<b>-18</b>	mA
POWER SUPPLY GAIN SENSITIVITY <sup>2</sup>							
V <sub>EE</sub> = -11.4 to -16.5 V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (see Figures 3, 4, 5)							
		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50 Ω Resistor for R2 (Figure 3)		±0.1	<b>±0.25</b>		±0.1	<b>±0.25</b>	% of F.S. Range
Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 4)		±0.05	<b>±0.15</b>		±0.05	<b>±0.1</b>	% of F.S. Range
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15	20	25	15	20	25	kΩ
POWER DISSIPATION		180	<b>300</b>		180	<b>300</b>	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants		Two (2): Bipolar Operation at Digital Input Only					
Reference Voltage		1 V to 10 V, Unipolar					
Accuracy		10 Bits (±0.05% of Reduced F.S.) for 1 V dc Reference Voltage					
Reference Feedthrough (Unipolar Mode, All Bits OFF, and 1 V to 10 V [p-p], Sine Wave Frequency for 1/2 LSB [p-p] Feedthrough)		40					kHz typ
Output Slew Rate 10%–90%		5					mA/μs
90%–10%		1					mA/μs
Output Settling Time (All Bits ON and a 0 V–10 V Step Change in Reference Voltage)		1.5 μs to 0.01% F.S.					
CONTROL AMPLIFIER							
Full Power Bandwidth		300					kHz
Small-Signal Closed-Loop Bandwidth		1.8					MHz

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specification subject to change without notice.













