

FEATURES

- Nonvolatile memory stores wiper setting**
- 4-channel independent programmable**
- 64-position resolution**
- Power-on refreshed with EEMEM settings**
- EEMEM restore time: 140 μ s typical**
- Full monotonic operation**
- 10 k Ω , 50 k Ω , and 100 k Ω terminal resistance**
- Permanent memory write protection**
- Wiper setting readback**
- Predefined linear increment/decrement instructions**
- Predefined ± 6 dB/step log taper increment/decrement instructions**
- SPI-compatible serial interface with readback function**
- 2.7 V to 5.5 V single supply or ± 2.5 V dual supply**
- 11 bytes extra nonvolatile memory for user-defined data**
- 100-year typical data retention, $T_A = 55^\circ\text{C}$**

APPLICATIONS

- Mechanical potentiometer replacement**
- Instrumentation: gain, offset adjustment**
- Programmable voltage-to-current conversion**
- Programmable filters, delays, time constants**
- Programmable power supply**
- Sensor calibration**

GENERAL DESCRIPTION

The AD5233 is a quad-channel nonvolatile memory,¹ digitally controlled potentiometer² with a 64-step resolution. The device performs the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid-state reliability, and remote controllability. The AD5233 has versatile programming using a serial peripheral interface (SPI) for 16 modes of operation and adjustment, including scratchpad programming, memory storing and restoring, increment/decrement, ± 6 dB/step log taper adjustment, wiper setting readback, and extra EEMEM for user-defined information such as memory data for other components, look-up tables, or system identification information.

¹ The terms nonvolatile memory and EEMEM are used interchangeably.

² The terms digital potentiometer and RDAC are used interchangeably.

FUNCTIONAL BLOCK DIAGRAM

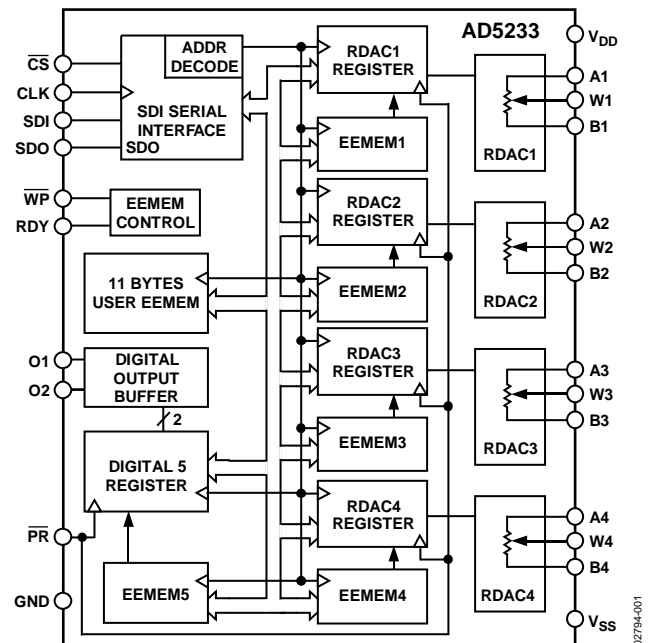


Figure 1.

In the scratchpad programming mode, a specific setting can be programmed directly to the RDAC register, which sets the resistance between Terminal W to Terminal A and Terminal W to Terminal B. This setting can be stored into the EEMEM and is transferred automatically to the RDAC register during system power-on.

The EEMEM content can be restored dynamically or through external PR strobing. A WP function protects EEMEM contents. To simplify the programming, independent or simultaneous increment or decrement commands can be used to move the RDAC wiper up or down, one step at a time. For logarithmic ± 6 dB step changes in wiper settings, the left or right bit shift command can be used to double or halve the RDAC wiper setting.

The AD5233 is available in a thin 24-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of -40°C to $+85^\circ\text{C}$.

Rev. B

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—10 k Ω , 50 k Ω , AND 100 k Ω VERSIONS

$V_{DD} = 3\text{ V} \pm 10\%$ or $5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $V_A = V_{DD}$, $V_B = 0\text{ V}$, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE						
Resistor Differential Nonlinearity ²	R-DNL	R_{WB} , $V_A = \text{NC}$, monotonic	-0.5	± 0.1	+0.5	LSB
Resistor Integral Nonlinearity ²	R-INL	R_{WB} , $V_A = \text{NC}$	-0.5	± 0.1	+0.5	LSB
Nominal Resistor Tolerance	R_{AB}/R_{AB}	$D = 0x3F$	-40		+20	%
Resistance Temperature Coefficient	$(R_{WB}/R_{WB})/T \times 10^6$			600		ppm/ $^\circ\text{C}$
Wiper Resistance	R_W	$I_W = 100\ \mu\text{A}$, code = half scale		15	100	
DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE						
Resolution	N				6	Bits
Differential Nonlinearity ³	DNL	Monotonic	-0.5	+0.1	+0.5	LSB
Integral Nonlinearity ³	INL		-0.5	+0.1	+0.5	LSB
Voltage Divider Temperature Coefficient	$(V_W/V_W)/T \times 10^6$	Code = half scale		15		ppm/ $^\circ\text{C}$
Full-Scale Error	V_{WFSE}	Code = full scale	-1.5		0	% FS
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		1.5	% FS
RESISTOR TERMINALS						
Terminal Voltage Range ⁴	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, Capacitance B ⁵	C_A, C_B	$f = 1\text{ MHz}$, measured to GND, code = half scale		35		pF
Capacitance W ⁵	C_W	$f = 1\text{ MHz}$, measured to GND, code = half scale		35		pF
Common-Mode Leakage Current ^{5, 6}	I_{CM}	$V_W = V_{DD}/2$		0.015	1	μA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	With respect to GND, $V_{DD} = 5\text{ V}$ With respect to GND, $V_{DD} = 3\text{ V}$ With respect to GND, $V_{DD} = 2.5\text{ V}$, $V_{SS} = -2.5\text{ V}$	2.4 2.1 2.0			V V V
Input Logic Low	V_{IL}	With respect to GND, $V_{DD} = 5\text{ V}$ With respect to GND, $V_{DD} = 3\text{ V}$ With respect to GND, $V_{DD} = 2.5\text{ V}$, $V_{SS} = -2.5\text{ V}$			0.8 0.6 0.5	V V V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP} = 2.2\text{ k}\Omega$ to 5 V (see Figure 35)	4.9			V
Output Logic Low	V_{OL}	$I_{OL} = 1.6\text{ mA}$, $V_{LOGIC} = 5\text{ V}$ (see Figure 35)			0.4	V
Input Current	I_{IL}	$V_{IN} = 0\text{ V}$ or V_{DD}			± 2.5	μA
Input Capacitance ⁵	C_{IL}			4		pF
Output Current ⁵	I_{O1}, I_{O2}	$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, sourcing only $V_{DD} = 2.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, sourcing only		50 7		mA mA

AD5233

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
POWER SUPPLIES						
Single-Supply Power Range	V _{DD}	V _{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V _{DD} /V _{SS}		±2.5		±2.75	V
Positive Supply Current	I _{DD}	V _{IH} = V _{DD} or V _{IL} = GND		3.5	10	µA
Negative Supply Current	I _{SS}	V _{IH} = V _{DD} or V _{IL} = GND, V _{DD} = 2.5 V, V _{SS} = -2.5 V		0.55	10	µA
EEMEM Store Mode Current	I _{DD} (store)	V _{IH} = V _{DD} or V _{IL} = GND, V _{SS} = 0, I _{SS} ≈ 0		40		mA
	I _{SS} (store)	V _{DD} = 2.5 V, V _{SS} = -2.5 V		-40		mA
EEMEM Restore Mode Current ⁷	I _{DD} (restore)	V _{IH} = V _{DD} or V _{IL} = GND, V _{SS} = GND, I _{SS} ≈ 0	0.3	3	9	mA
	I _{SS} (restore)	V _{DD} = 2.5 V, V _{SS} = -2.5 V	-0.3	-3	-9	mA
Power Dissipation ⁸	P _{DISS}	V _{IH} = V _{DD} or V _{IL} = GND		0.018	0.05	mW
Power Supply Sensitivity ⁵	P _{SS}	V _{DD} = 5 V ± 10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS^{5, 9}						
Bandwidth	BW	-3 dB, R _{AB} = 10 k / 50 k / 100 k		630/135/66		kHz
Total Harmonic Distortion	THD _W	V _A = 1 V rms, V _B = 0 V, f = 1 kHz, R _{AB} = 10 k		0.04		%
		V _A = 1 V rms, V _B = 0 V, f = 1 kHz, R _{AB} = 50 k , 100 k		0.015		%
V _W Settling Time	t _S	V _A = V _{DD} , V _B = 0 V, V _W = 0.50% error band, Code 0x000 to Code 0x200 for R _{AB} = 10 k / 50 k / 100 k		0.6/2.2/3.8		µs
Resistor Noise Voltage	e _{N_WB}	R _{WB} = 5 k , f = 1 kHz		9		nV/ Hz
Crosstalk (C _{W1} /C _{W2})	C _T	V _A = V _{DD} , V _B = 0 V, measure V _W with adjacent RDAC making the full-scale code change		-1		nV/sec
Analog Crosstalk (C _{W1} /C _{W2})	C _{TA}	V _{DD} = V _{A1} = +2.5 V, V _{SS} = V _{B1} = -2.5 V, measure V _{W1} with V _{W2} = 5 V p-p @ f = 10 kHz, Code 1 = 0x20, Code 2 = 0x3F, R _{AB} = 10 k / 50 k / 100 k		-86/-73/-68		dB

¹ Typical values represent average readings at 25°C and V_{DD} = 5 V.

² Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. I_W > 50 µA @ V_{DD} = 2.7 V for the R_{AB} = 10 k version, I_W > 50 µA for the R_{AB} = 50 k , and I_W > 25 µA for the R_{AB} = 100 k version (see Figure 25).

³ INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output ADC. V_A = V_{DD} and V_B = V_{SS}. DNL specification limits of -1 LSB minimum are guaranteed monotonic operating conditions (see Figure 26).

⁴ Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.

⁵ Guaranteed by design and not subject to production test.

⁶ Common-mode leakage current is a measure of the dc leakage from Terminal B and Terminal W to a common-mode bias level of V_{DD}/2.

⁷ EEMEM restore mode current is not continuous. Current is consumed while EEMEM locations are read and transferred to the RDAC register (see Figure 22). To minimize power dissipation, a NOP instruction should be issued immediately after Instruction 1 (0x1).

⁸ Power dissipation is calculated by P_{DISS} = (I_{DD} × V_{DD}) + (I_{SS} × V_{SS}).

⁹ All dynamic characteristics use V_{DD} = 2.5 V and V_{SS} = -2.5 V.

TIMING CHARACTERISTICS

$V_{DD} = 3\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$, and $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Unit
INTERFACE TIMING CHARACTERISTICS ^{2,3}						
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{\text{CS}}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{\text{CS}}$ Rise	t_3		1			t_{CYC}
Input Clock Pulse Width	t_4, t_5	Clock level high or low	10			ns
Data Setup Time	t_6	From positive CLK transition	5			ns
Data Hold Time	t_7	From positive CLK transition	5			ns
$\overline{\text{CS}}$ to SDO-SPI Line Acquire	t_8				40	ns
$\overline{\text{CS}}$ to SDO-SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay ⁴	t_{10}	$R_{PULL-UP} = 2.2\text{ k}\Omega$, $C_L < 20\text{ pF}$			50	ns
CLK to SDO Data Hold Time	t_{11}	$R_P = 2.2\text{ k}\Omega$, $C_L < 20\text{ pF}$	0			ns
$\overline{\text{CS}}$ High Pulse Width ⁵	t_{12}		10			ns
$\overline{\text{CS}}$ High to $\overline{\text{CS}}$ High ⁵	t_{13}		4			t_{CYC}
RDY Rise to $\overline{\text{CS}}$ Fall	t_{14}		0			ns
$\overline{\text{CS}}$ Rise to RDY Fall Time	t_{15}			0.1	0.15	ms
Read/Store to Nonvolatile EEMEM ⁶	t_{16}	Applies to Instruction 0x2, Instruction 0x3, and Instruction 0x9		25		ms
$\overline{\text{CS}}$ Rise to Clock Rise/Fall Setup	t_{17}		10			ns
Preset Pulse Width (Asynchronous)	t_{PRW}	Not shown in timing diagram	50			ns
Preset Response Time to Wiper Setting	t_{PRESP}	$\overline{\text{PR}}$ pulsed low to refresh wiper positions		70		μs
Power-On EEMEM Restore Time	t_{EEMEM1}	$R_{AB} = 10\text{ k}\Omega$		140		μs
FLASH/EE MEMORY RELIABILITY						
Endurance ⁷			100			kCycles
Data Retention ⁸				100		Years

¹ Typicals represent average readings at 25°C and $V_{DD} = 5\text{ V}$.

² Guaranteed by design and not subject to production test.

³ See the timing diagrams (Figure 2 and Figure 3) for the location of the measured values. All input control voltages are specified with $t_R = t_F = 2.5\text{ ns}$ (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both $V_{DD} = 3\text{ V}$ and $V_{DD} = 5\text{ V}$.

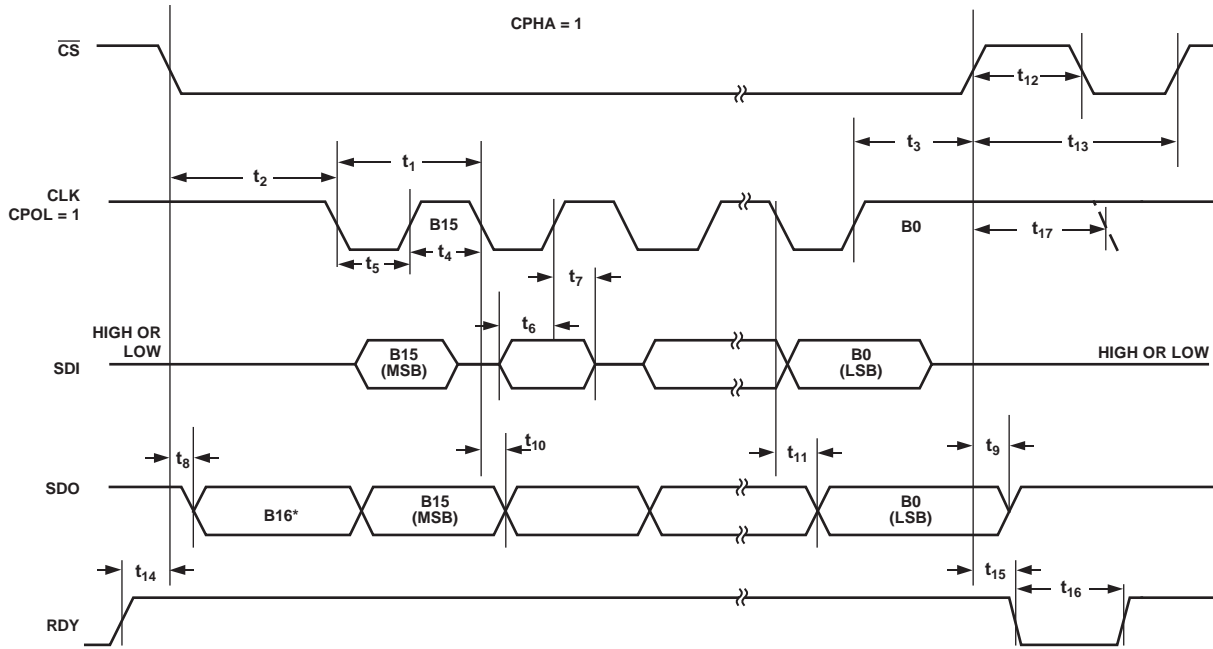
⁴ Propagation delay depends on the value of V_{DD} , $R_{PULL-UP}$, and C_L .

⁵ Valid for commands that do not activate the RDY pin.

⁶ The RDY pin is low only for Command 2, Command 3, Command 8, Command 9, Command 10, and the $\overline{\text{PR}}$ hardware pulse: $\text{CMD}_8 > 1\text{ ms}$; $\text{CMD}_9, \text{CMD}_{10} > 0.12\text{ ms}$; $\text{CMD}_2, \text{CMD}_3 > 20\text{ ms}$. Device operation at $T_A = -40^{\circ}\text{C}$ and $V_{DD} < 3\text{ V}$ extends the save time to 35 ms.

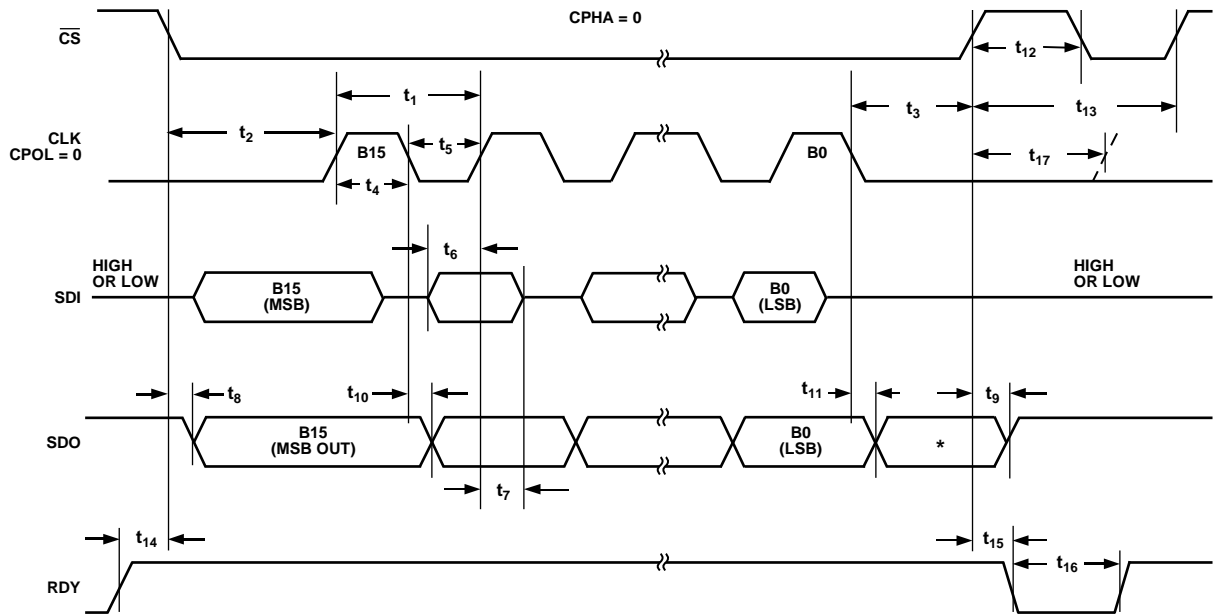
⁷ Endurance is qualified to 100,000 cycles per JEDEC Standard 22, Method A117, and measured at -40°C , $+25^{\circ}\text{C}$, and $+85^{\circ}\text{C}$; typical endurance at 25°C is 700,000 cycles.

⁸ Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Standard 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature, as shown in Figure 45 in the Flash/EEMEM Reliability section.



*EXTRA BIT THAT IS NOT DEFINED, BUT NORMALLY LSB OF CHARACTER PREVIOUSLY TRANSMITTED.
 THE CPOL = 1 MICROCONTROLLER COMMAND ALIGNS THE INCOMING DATA TO THE POSITIVE EDGE OF THE CLOCK.

Figure 2. CPHA = 1 Timing Diagram



*NOT DEFINED, BUT NORMALLY MSB OF CHARACTER PREVIOUSLY RECEIVED.
 THE CPOL = 0 MICROCONTROLLER COMMAND ALIGNS THE INCOMING DATA TO THE POSITIVE EDGE OF THE CLOCK.

Figure 3. CPHA = 0 Timing Diagram

02794-002

02794-003

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	-0.3 V to +7 V
V_{SS} to GND	+0.3 V to -7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	$V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$
I_A, I_B, I_W	
Pulsed ¹	±20 mA
Continuous	±2 mA
Digital Inputs and Output Voltage to GND	-0.3 V to $V_{DD} + 0.3 \text{ V}$
Operating Temperature Range ²	-40°C to +85°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	-65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance Junction-to-Ambient, θ_{JA} ³	50°C/W
Package Power Dissipation	$(T_J \text{ max} - T_A) / \theta_{JA}$

¹ Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

² Includes programming of nonvolatile memory.

³ Thermal Resistance (JEDEC 4-layer (2S2P) board).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

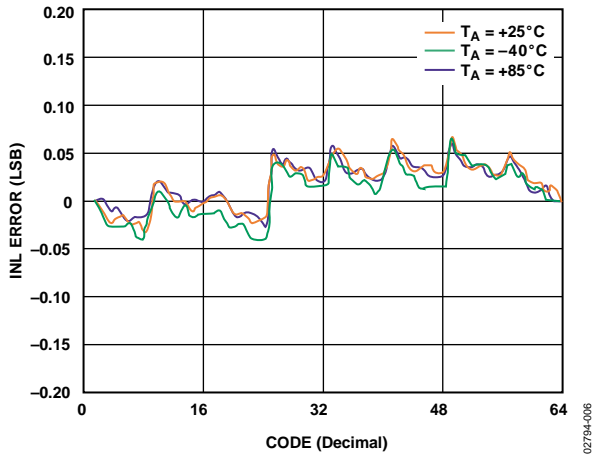


Figure 5. INL Error vs. Code, $T_A = -40^\circ\text{C}, +25^\circ\text{C}, +85^\circ\text{C}$ Overlay, $R_{AB} = 10\text{ k}$

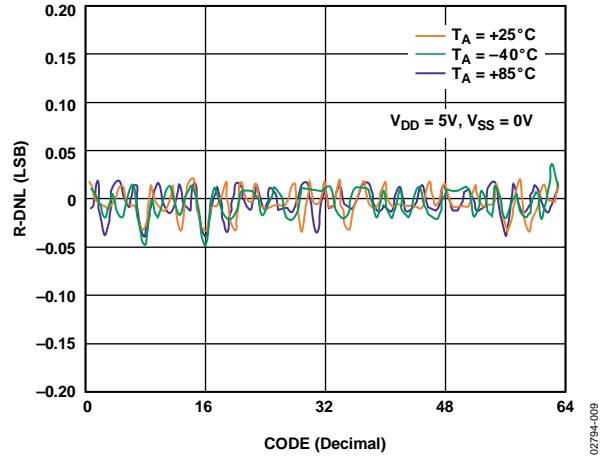


Figure 8. R-DNL vs. Code, $T_A = -40^\circ\text{C}, +25^\circ\text{C}, +85^\circ\text{C}$ Overlay, $R_{AB} = 10\text{ k}$

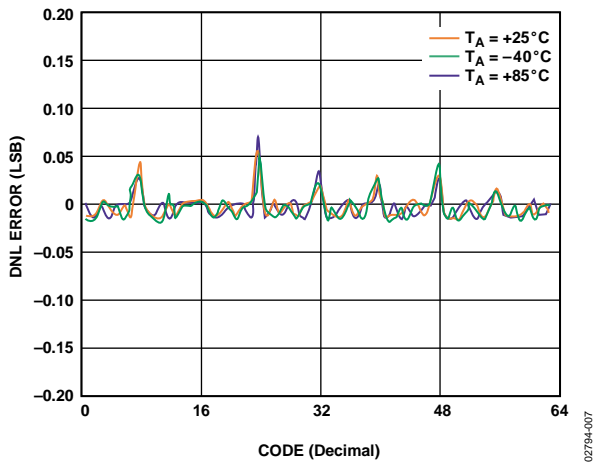


Figure 6. DNL Error vs. Code, $T_A = -40^\circ\text{C}, +25^\circ\text{C}, +85^\circ\text{C}$ Overlay, $R_{AB} = 10\text{ k}$

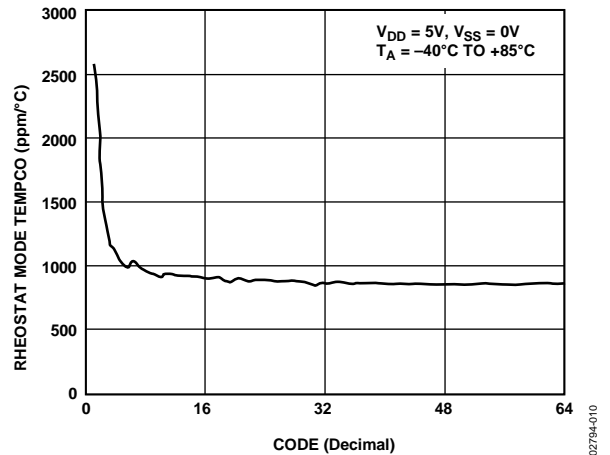


Figure 9. $(R_{WB}/R_{IB}) / T \times 10^6$

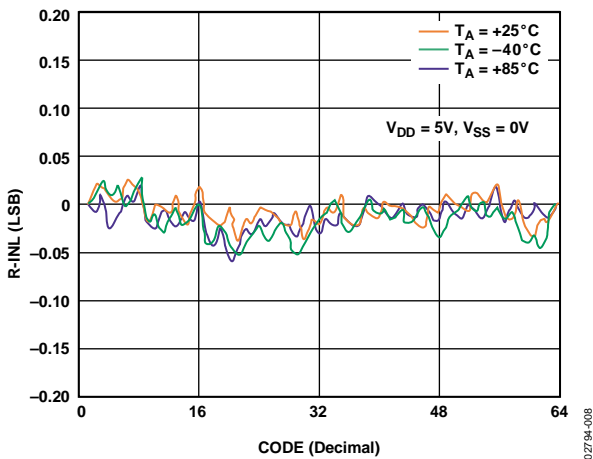


Figure 7. R-INL vs. Code, $T_A = -40^\circ\text{C}, +25^\circ\text{C}, +85^\circ\text{C}$ Overlay, $R_{AB} = 10\text{ k}$

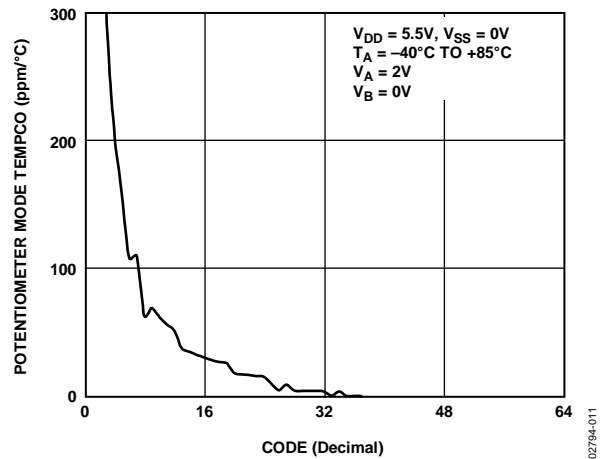


Figure 10. $(V_W/V_W) / T \times 10^6$ vs. Code, $R_{AB} = 10\text{ k}$

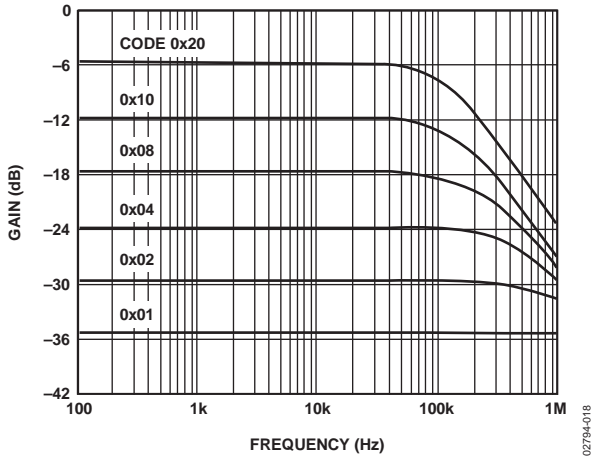


Figure 17. Gain vs. Frequency vs. Code, $R_{AB} = 50\text{ k}$ (Figure 31)

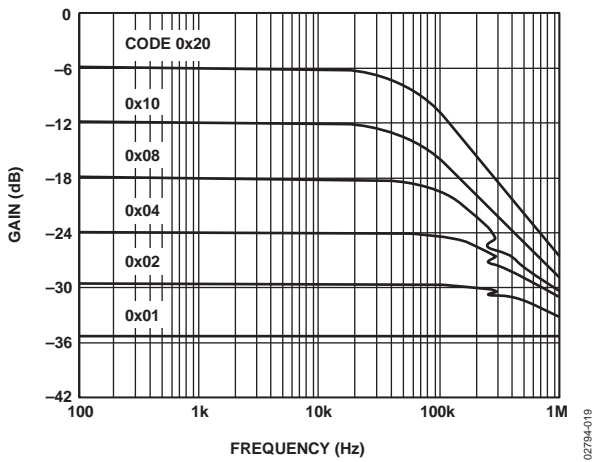


Figure 18. Gain vs. Frequency vs. Code, $R_{AB} = 100\text{ k}$ (Figure 31)

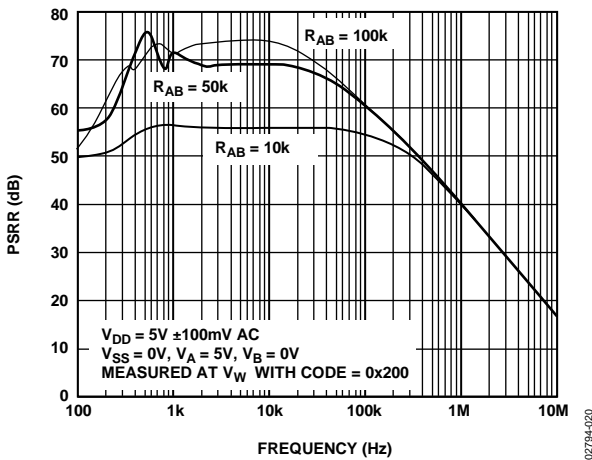


Figure 19. PSRR vs. Frequency

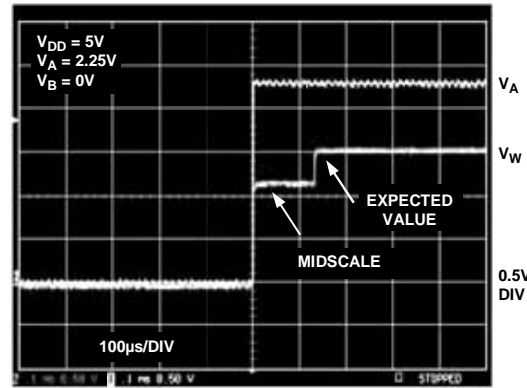


Figure 20. Power-On Reset, $V_A = 2.25\text{ V}$, $V_B = 0\text{ V}$, Code = 101010

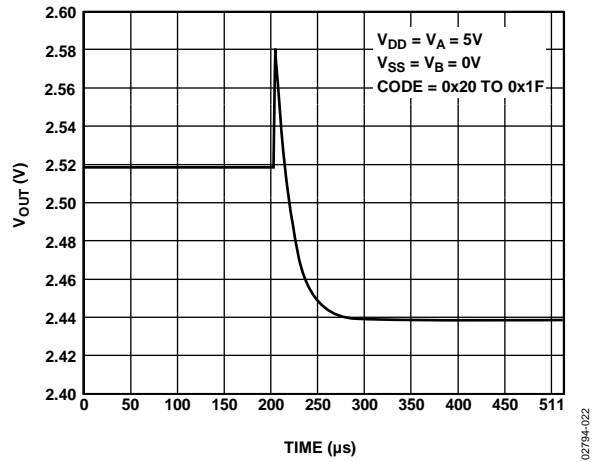


Figure 21. Midscale Glitch Energy, Code 0x20 to Code 0x1F

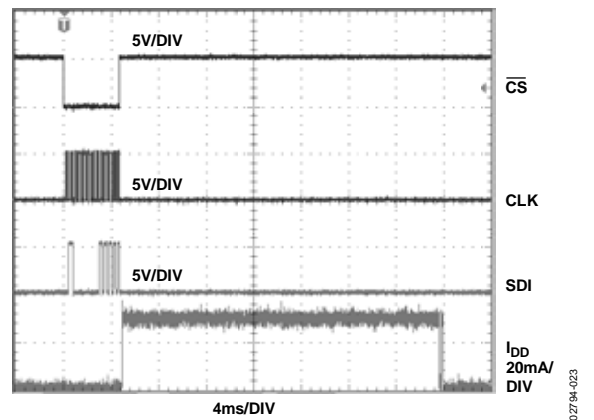
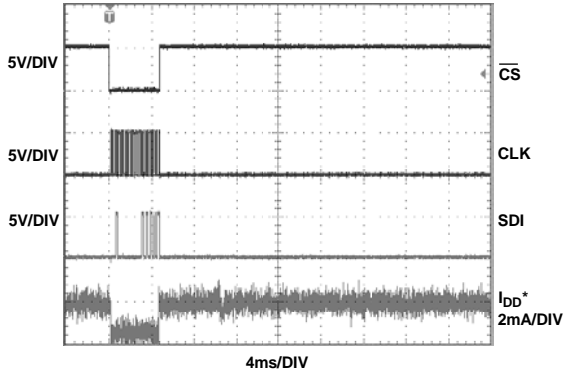


Figure 22. I_{DD} vs. Time When Storing Data to EEMEM



*SUPPLY CURRENT RETURNS TO MINIMUM POWER CONSUMPTION, IF INSTRUCTION 0 (NOP) IS EXECUTED IMMEDIATELY AFTER INSTRUCTION 1 (READ EEMEM).

Figure 23. I_{DD} vs. Time When Reading Data from EEMEM

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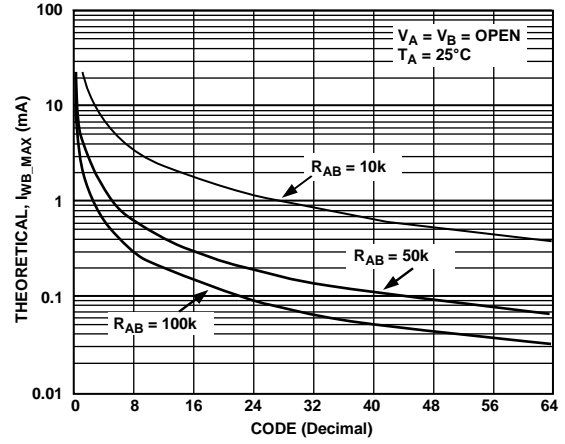


Figure 24. I_{WB_MAX} vs. Code

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TEST CIRCUITS

Figure 25 to Figure 35 define the test conditions used in the specifications.

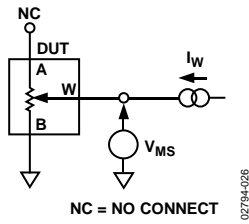


Figure 25. Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

02794-026

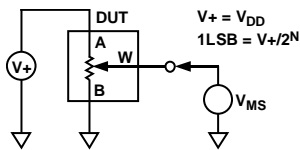


Figure 26. Potentiometer Divider Nonlinearity Error (INL, DNL)

02794-027

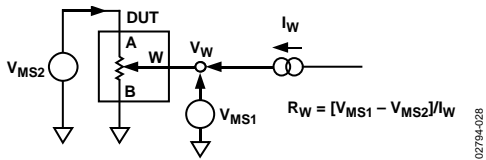


Figure 27. Wiper Resistance

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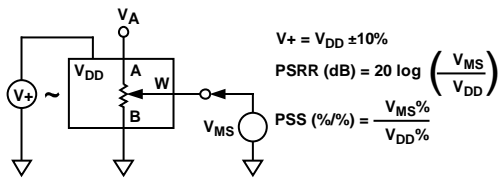


Figure 28. Power Supply Sensitivity (PSS, PSRR)

02794-029

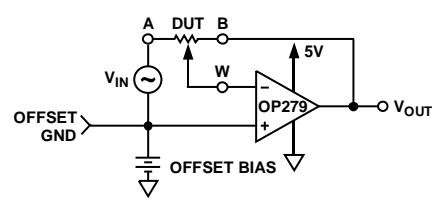


Figure 29. Inverting Gain

02794-030

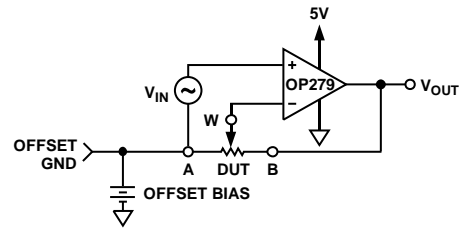


Figure 30. Noninverting Gain

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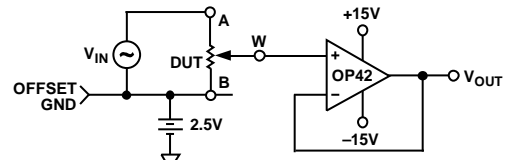


Figure 31. Gain vs. Frequency

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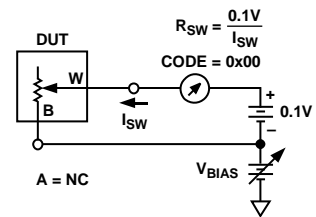


Figure 32. Incremental On Resistance

02794-033

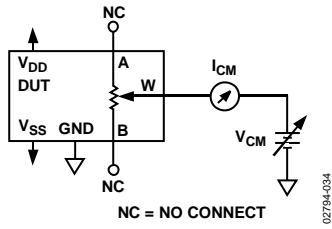


Figure 33. Common-Mode Leakage Current

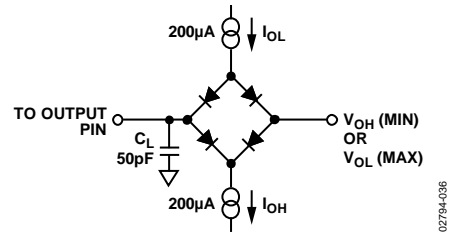


Figure 35. Load Circuit for Measuring V_{OH} and V_{OL} ; the Diode Bridge Test Circuit Is Equivalent to the Application Circuit with $R_{PULL-UP}$ of 2.2 k

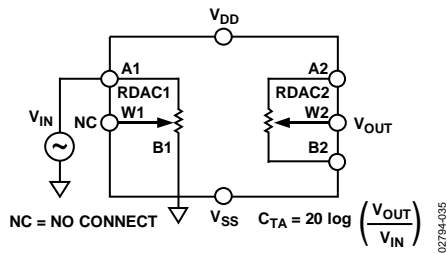


Figure 34. Analog Crosstalk

DAISY-CHAIN OPERATION

The serial data output (SDO) pin serves two purposes. It can be used to read the contents of the wiper setting and EEMEM values using Instruction 10 and Instruction 9, respectively. The remaining instructions (0 to 8, 11 to 15) are valid for daisy-chaining multiple devices in simultaneous operations. Daisy-chaining minimizes the number of port pins required from the controlling IC (Figure 39). The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor, if this function is used. As shown in Figure 39, users need to tie the SDO pin of one package to the SDI pin of the next package.

Users might need to increase the clock period, because the pull-up resistor and the capacitive loading at the SDO to SDI interface might require an additional time delay between subsequent packages. When two AD5233s are daisy-chained, 32 bits of data is required. The first 16 bits go to U2 and the second 16 bits go to U1. \overline{CS} should be kept low until all 32 bits are clocked into their respective serial registers. \overline{CS} is then pulled high to complete the operation.

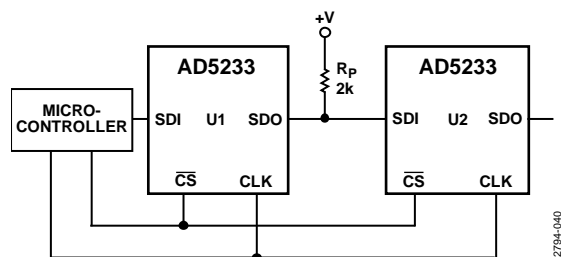


Figure 39. Daisy-Chain Configuration Using SDO

TERMINAL VOLTAGE OPERATION RANGE

The AD5233's positive V_{DD} and negative V_{SS} power supplies define the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 40).

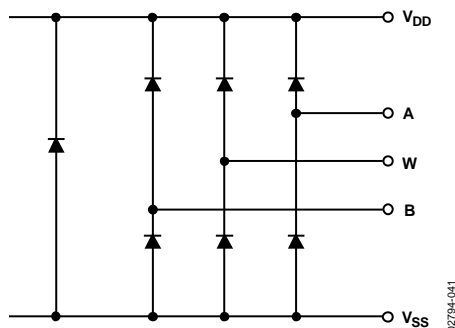


Figure 40. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5233 device is used primarily as a digital ground reference, which needs to be tied to the PCB's common ground. The digital input control signals to the AD5233 must be referenced to the device ground pin (GND) and satisfy the logic level defined in the Specifications section. An internal level-shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD} , regardless of the digital input level.

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 40), it is important to power on V_{DD}/V_{SS} first before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD}/V_{SS} are powered unintentionally. For example, applying 5 V across the A and B terminals prior to V_{DD} causes the V_{DD} terminal to exhibit 4.3 V. It is not destructive to the device, but it might affect the rest of the system. The ideal power-up sequence is GND, V_{DD} , V_{SS} , digital inputs, and $V_A/V_B/V_W$. The order of powering V_A , V_B , V_W , and digital inputs is not important as long as they are powered after V_{DD}/V_{SS} .

Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{DD}/V_{SS} are powered, the power-on preset remains effective, which restores the EEMEM values to the RDAC registers.

LATCHED DIGITAL OUTPUTS

A pair of digital outputs, O1 and O2, is available on the AD5233. These outputs provide a nonvolatile Logic 0 or Logic 1 setting. O1 and O2 are standard CMOS logic outputs, shown in Figure 41. These outputs are ideal to replace the functions often provided by DIP switches. In addition, they can be used to drive other standard CMOS logic-controlled parts that need an occasional setting change. Pin O1 and Pin O2 default to Logic 1, and they can drive up to 50 mA of load at 5 V/25°C.

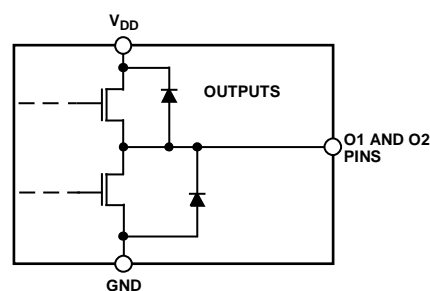


Figure 41. Logic Output O1 and Logic Output O2

AD5233

In Table 6, C0 to C3 are command bits, A3 to A0 are address bits, D0 to D5 are data bits that are applicable to the RDAC wiper register, and D0 to D7 are applicable to the EEMEM register.

Table 6. 16-Bit Serial Data-Word

MSB	Instruction Byte								LSB	Data Byte							
RDAC	C3	C2	C1	C0	0	0	A1	A0	X	X	D5	D4	D3	D2	D1	D0	
EEMEM	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	

Command instruction codes are defined in Table 7.

Table 7. Instruction/Operation Truth Table^{1, 2, 3}

Inst. No.	Instruction Byte 0								Data Byte 0								Operation
	B16							B8	B7	B6	B5	B4	B3	B2	B1	B0	
	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	NOP: Do nothing. See Table 14 for programming example.
1	0	0	0	1	0	0	A1	A0	X	X	X	X	X	X	X	X	Restore EEMEM contents to the RDAC register. This command leaves the device in read program power state. To return the part to the idle state, perform NOP instruction 0. See Table 14.
2	0	0	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Store wiper setting: Store RDAC (ADDR) setting to EEMEM. See Table 13.
3 ⁴	0	0	1	1	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Store contents of Serial Register Data Byte 0 (total eight bits) to EEMEM (ADDR). See Table 16.
4 ⁵	0	1	0	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Decrement 6 dB: right-shift contents of RDAC register, stop at all 0s.
5 ⁵	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Decrement all 6 dB: right-shift contents of all RDAC registers, stop at all 0s.
6 ⁵	0	1	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Decrement content of RDAC register by 1, stop at all 0s.
7 ⁵	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Decrement contents of all the RDAC registers by 1, stop at all 0s.
8	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	Reset: refresh all RDACs with their corresponding EEMEM previously stored values.
9	1	0	0	1	A3	A2	A1	A0	X	X	X	X	X	X	X	X	Read content of EEMEM (ADDR) from SDO output in the next frame. See Table 17.
10	1	0	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Read RDAC wiper setting from SDO output in the next frame. See Table 18.
11	1	0	1	1	0	0	A1	A0	X	X	D5	D4	D3	D2	D1	D0	Write contents of Serial Register Data Byte 0 (total six bits) to RDAC. See Table 12.
12 ⁵	1	1	0	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Increment 6 dB: Left-shift contents of RDAC register, stop at all 1s. See Table 15.
13 ⁵	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Increment all 6 dB: left-shift contents of RDAC registers, stop at all 1s.
14 ⁵	1	1	1	0	0	0	A1	A0	X	X	X	X	X	X	X	X	Increment contents of the RDAC register by 1, stop at all 1s. See Table 13.
15 ⁵	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	Increment contents of all RDAC registers by 1, stop at all 1s.

¹ The SDO output shifts out the last 16 bits of data clocked into the serial register for daisy-chain operation. Exception: for any instruction following Instruction 9 or Instruction 10, see details of these instructions for proper usage.

² The RDAC register is a volatile scratchpad register that is automatically refreshed at power-on from the corresponding nonvolatile EEMEM register.

³ Execution of these operations takes place when the CS strobe returns to Logic 1.

⁴ Instruction 3 writes one data byte (eight bits of data) to EEMEM. In the case of Address 0, Address 1, Address 2, and Address 3, only the last six bits are valid for wiper position setting.

⁵ The increment, decrement, and shift instructions ignore the contents of the Shift Register Data Byte 0.

APPLICATIONS INFORMATION

BIPOLAR OPERATION FROM DUAL SUPPLIES

The AD5233 can be operated from dual supplies ± 2.5 V, which enables control of ground-referenced ac signals or bipolar operation. AC signals as high as V_{DD}/V_{SS} can be applied directly across Terminal A and Terminal B with output taken from Terminal W. See Figure 46 for a typical circuit connection.

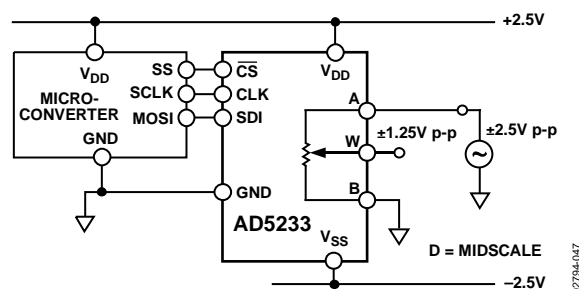


Figure 46. Bipolar Operation from Dual Supplies

GAIN CONTROL COMPENSATION

A digital potentiometer is commonly used in gain control such as the noninverting gain amplifier shown in Figure 47.

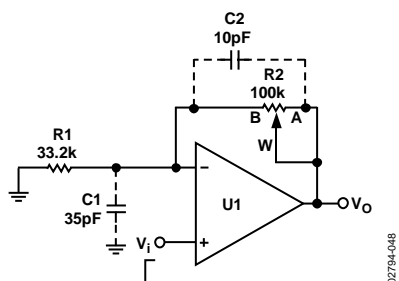


Figure 47. Typical Noninverting Gain Amplifier

When RDAC B terminal parasitic capacitance is connected to the op amp noninverting node, it introduces a 0 for the $1/b_0$ term with 20 dB/dec, while a typical op amp GBP has -20 dB/dec characteristics. A large R_2 and finite C_1 can cause this zero's frequency to fall well below the crossover frequency. Therefore, the rate of closure becomes 40 dB/dec, and the system as a 0° phase margin at the crossover frequency. The output can ring or oscillate if an input is a rectangular pulse or step function. Similarly, it is also likely to ring when switching between two gain values; this is equivalent to a stop change at the input.

Depending on the op amp GBP, reducing the feedback resistor might extend the zero's frequency far enough to overcome the problem. A better approach is to include a compensation capacitor, C_2 , to cancel the effect caused by C_1 . Optimum compensation occurs when $R_1 \times C_1 = R_2 \times C_2$. This is not an option because of the variation of R_2 .

As a result, one can use the previous relationship and scale C_2 as if R_2 were at its maximum value. Doing this might over-compensate and compromise the performance when R_2 is set at low values. On the other hand, it avoids the ringing or oscillation at the worst case. For critical applications, C_2 should be found empirically to suit the need. In general, C_2 in the range of picofarads is usually adequate for the compensation.

Similarly, W and A terminal capacitances are connected to the output (not shown); their effect at this node is less significant and the compensation can be avoided in most cases.

HIGH VOLTAGE OPERATION

The digital potentiometer can be placed directly in the feedback or input path of an op amp for gain control, provided that the voltage across Terminal A and Terminal B, Terminal W and Terminal A, or Terminal W and Terminal B does not exceed $|5$ V|. When high voltage gain is needed, users should set a fixed gain in an op amp operated at high voltage and let the digital potentiometer control the adjustable input. Figure 48 shows a simple implementation.

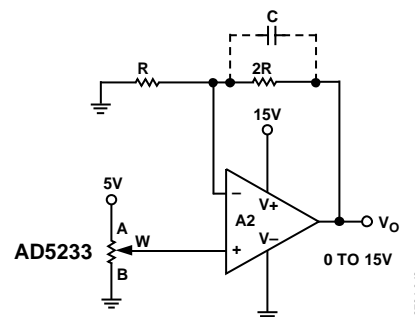


Figure 48. 5 V Voltage Span Control

Similarly, a compensation capacitor, C , might be needed to dampen the potential ringing when the digital potentiometer changes steps. This effect is prominent when stray capacitance at the inverted node is augmented by a large feedback resistor. Usually, a capacitor (C) of a few picofarads, is adequate to combat the problem.

DAC

Figure 49 shows a unipolar 8-bit DAC using the AD5233. The buffer is needed to drive various loads.

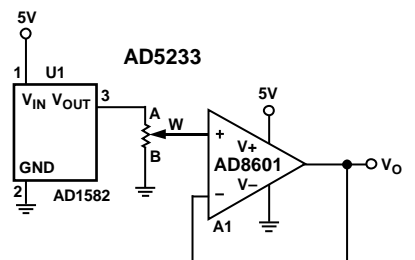


Figure 49. Unipolar 8-Bit DAC

PROGRAMMABLE STATE-VARIABLE FILTER

One of the standard circuits used to generate a low-pass, high-pass, or band-pass filter is the state-variable active filter. The AD5233 digital potentiometer allows full programmability of the frequency, the gain, and the Q of the filter outputs.

Figure 52 shows a filter circuit using a 2.5 V virtual ground, which allows a ±2.5 V peak input and output swing. RDAC2 and RDAC3 set the low-pass, high-pass, and band-pass cutoff and center frequencies, respectively. RDAC2 and RDAC3 should be programmed with the same data (as with ganged potentiometers) to maintain the best Circuit Q.

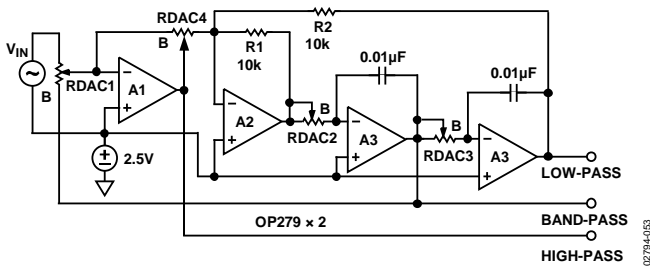


Figure 52. Programmable State-Variable Filter

The transfer function of the band-pass filter is

$$\frac{V_{BP}}{V_i} = \frac{A_O \frac{\omega_O}{Q} S}{S^2 + \frac{\omega_O}{Q} S + \omega_O^2} \tag{9}$$

where A_O is the gain.

For $R_{WB2(D2)} = R_{WB3(D3)}$, $R1 = R2$, and $C1 = C2$:

$$\omega_O = \frac{1}{R_{WB2} C1} \tag{10}$$

$$A_O = \frac{R_{WB1}}{R_{WA1}} \tag{11}$$

$$Q = \frac{R_{WA4}}{R_{WB4}} \times \frac{R_{WB1}}{R1} \tag{12}$$

Figure 53 shows the measured filter response at the band-pass output as a function of the RDAC2 and RDAC3 settings, which produce a range of center frequencies from 2 kHz to 20 kHz. The filter gain response at the band-pass output is shown in Figure 54. At a center frequency of 2 kHz, the gain is adjusted over the -20 dB to +20 dB range, determined by RDAC1. Circuit Q is adjusted by RDAC4 and RDAC1. Suitable op amps for this application are OP4177, AD8604, OP279, and AD824.

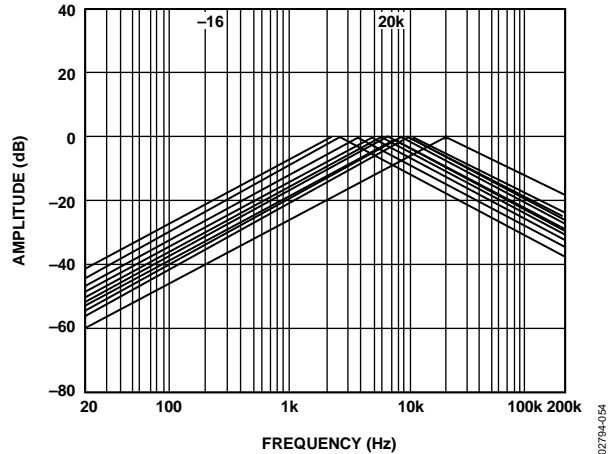


Figure 53. Programmed Center Frequency Band-Pass Response

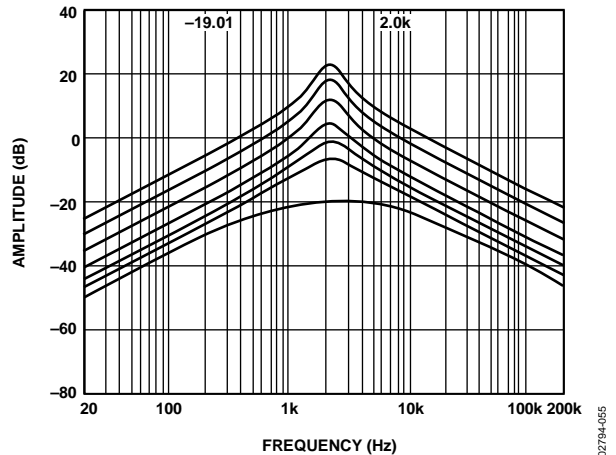


Figure 54. Programmed Amplitude Band-Pass Response

PROGRAMMABLE OSCILLATOR

In a classic Wien-bridge oscillator, shown in Figure 55, the Wien network (R, R', C, C') provides positive feedback, while R1 and R2 provide negative feedback. At the resonant frequency, f₀, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. If the op amp is chosen with a relatively high gain bandwidth product, the frequency response of the op amp can be neglected.

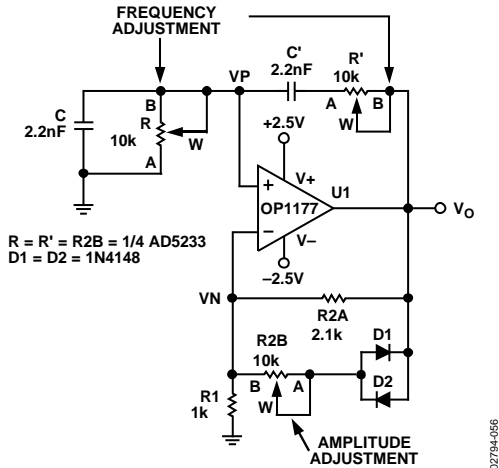


Figure 55. Programmable Oscillator with Amplitude Control

With $R = R'$, $C = C'$, and $R2 = R2A || (R2B + R_{DIODE})$, the oscillation frequency is

$$\omega_O = \frac{1}{RC} \text{ or } f_O = \frac{1}{2\pi RC} \tag{13}$$

where R is equal to R_{WA} such that

$$R = \frac{64 - D}{64} R_{AB} \tag{14}$$

At resonance, setting

$$\frac{R2}{R1} = 2 \tag{15}$$

balances the bridge. In practice, R2/R1 should be set slightly larger than 2 to ensure that the oscillation can start. On the other hand, the alternate turn-on of the diodes, D1 and D2, ensures that R1/R2 is smaller than 2 momentarily and, therefore, stabilizes the oscillation.

Once the frequency is set, the oscillation amplitude can be turned on by R2B, because

$$\frac{2}{3} V_O = I_D R2B + V_D \tag{16}$$

where V_O, I_D, and V_D are interdependent variables.

With proper selection of R2B, an equilibrium is reached such that V_O converges. R2B can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large or it saturates the output. In this configuration, R2B can be adjusted from minimum to full scale with amplitude varied from ±0.6 V to ±0.9 V. Using 2.2 nF for C and C', 10 kΩ dual

digital potentiometer, with R and R' set to 8.06 kΩ, 4.05 kΩ, and 670 Ω, oscillation occurs at 8.8 kHz, 17.6 kHz, and 102 kHz, respectively (see Figure 56).

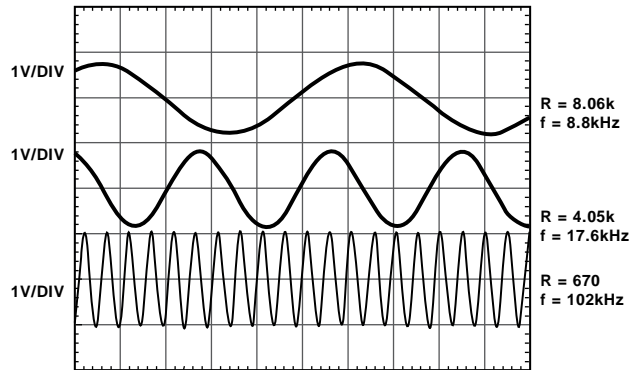


Figure 56. Programmable Oscillation

In both circuits (shown in Figure 51 and Figure 55), the frequency tuning requires that both RDACs be adjusted to the same settings. Because the two channels might be adjusted one at a time, an intermediate state occurs that might not be acceptable for some applications. Of course, the increment/decrement all instructions (5, 7, 13, and 15) can be used. Different devices can also be used in daisy-chain mode so that parts can be programmed to the same setting simultaneously.

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 57).

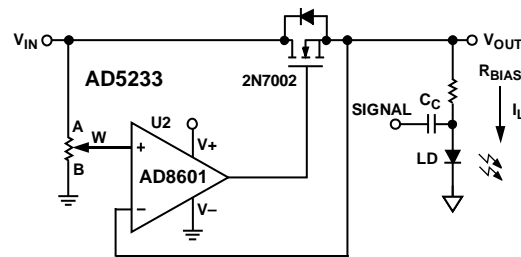


Figure 57. Programmable Boosted Voltage Source

In this circuit, the inverting input of the op amp forces the V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET N_i. N_i power handling must be adequate to dissipate (V_i - V_O) × I_L power. This circuit can source a maximum of 100 mA with a 5 V supply.

For precision applications, a voltage reference such as ADR421, ADR03, or ADR370 can be applied at Terminal A of the digital potentiometer.

PROGRAMMABLE CURRENT SOURCE

A programmable current source can be implemented with the circuit shown in Figure 58.

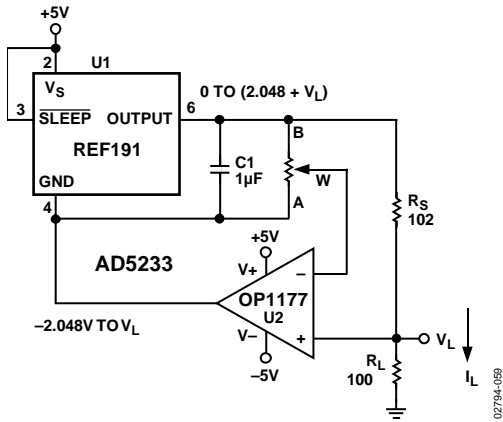


Figure 58. Programmable Current Source

REF191 is a unique low supply headroom precision reference that can deliver the 20 mA needed at 2.048 V. The load current is simply the voltage across Terminal B to Terminal W of the digital potentiometer divided by R_S .

The circuit is simple, but be aware that there are two issues. First, dual-supply op amps are ideal, because the ground potential of REF191 can swing from -2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of the system is reduced. Second, the voltage compliance at V_L is limited to 2.5 V or equivalently a 125 Ω load. If higher voltage compliance is needed, users can consider digital potentiometers AD5260, AD5280, and AD7376. Figure 58 shows an alternative circuit for high voltage compliance.

To achieve higher current, such as when driving a high power LED, the user can replace the U1 with an LDO, reduce R_S , and add a resistor in series with the AD5233's A terminal. This limits the potentiometer's current and enhances the current adjustment resolution.

PROGRAMMABLE BIDIRECTIONAL CURRENT SOURCE

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be used (see Figure 59).

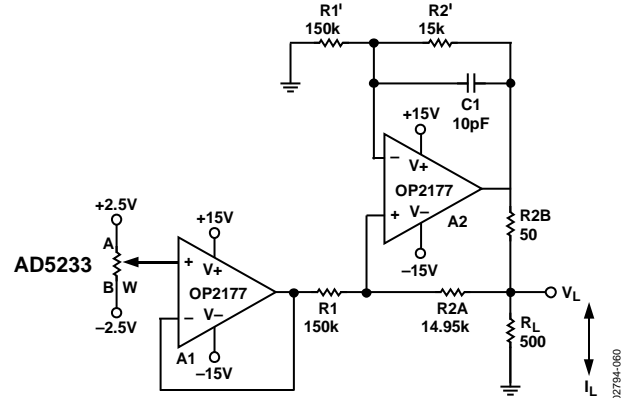


Figure 59. Programmable Bidirectional Current Source

If the resistors are matched, the load current is

$$I_L = \frac{(R2A + R2B)}{R2B} \times V_W \quad (17)$$

$R2B$, in theory, can be made as small as necessary to achieve the current needed within the A2 output current-driving capability. In this circuit, OP2177 delivers ± 5 mA in both directions, and the voltage compliance approaches 15 V. Without $C1$, it can be shown that the output impedance is

$$Z_O = \frac{R1' \times R2B (R1 + R2A)}{R1 \times R2' - R1' (R2A + R2B)} \quad (18)$$

Z_O can be infinite if the $R1'$ and $R2'$ resistors match precisely with $R1$ and $R2A + R2B$, respectively. On the other hand, Z_O can be negative if the resistors are not matched. As a result, $C1$ in the range of 1 pF to 10 pF is needed to prevent oscillation from the negative impedance.

RESISTANCE SCALING

AD5233 offers 10 k Ω , 50 k Ω , and 100 k Ω nominal resistance. Users who need lower resistance but want to maintain the number of adjustment steps can parallel multiple devices. For example, Figure 60 shows a simple scheme of paralleling two AD5233 channels. To adjust half the resistance linearly per step, users need to program both devices concurrently with the same settings.

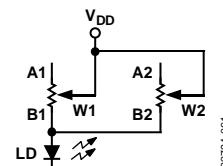
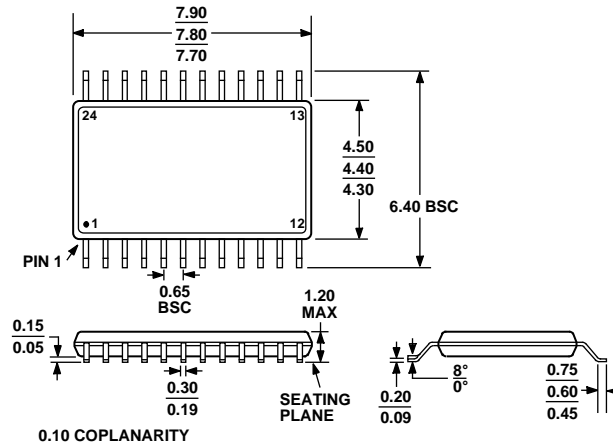


Figure 60. Reduce Resistance by Half with Linear Adjustment Characteristics

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 66. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)

Dimensions shown in millimeters

ORDERING GUIDE

Model	No. of Channels	R _{AB} (k)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding ¹
AD5233BRU10	4	10	-40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B10
AD5233BRU10-REEL7	4	10	-40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B10
AD5233BRUZ10 ²	4	10	-40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B10
AD5233BRUZ10-R7 ²	4	10	-40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B10
AD5233BRU50	4	50	-40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B50
AD5233BRU50-REEL7	4	50	-40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B50
AD5233BRUZ50 ²	4	50	-40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B50
AD5233BRUZ50-R7 ²	4	50	-40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B50
AD5233BRU100	4	100	-40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B100
AD5233BRU100-REEL7	4	100	-40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B100
AD5233BRUZ100 ²	4	100	-40°C to +85°C	24-Lead TSSOP	RU-24	96	5233B100
AD5233BRUZ100-R7 ²	4	100	-40°C to +85°C	24-Lead TSSOP	RU-24	1,000	5233B100

¹ Line 1 contains the model number. Line 2 contains the Analog Devices logo followed by the end-to-end resistance value. Line 3 contains the date code, YWW or #YWW, for RoHS compliant parts.

² Z = RoHS Compliant Part.

AD5233

NOTES

NOTES

AD5233

NOTES

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