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AN-617
APPLICATION NOTE

MicroCSP™ Wafer Level Chip Scale Package

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GENERAL DESCRIPTION

The MicroCSP from Analog Devices, Inc. is a wafer level chip scale package that allows direct connection, without wires, to a printed circuit board by inverting the die and connecting by solder balls. The technology is similar to flip chip technology, except that for the MicroCSP the solder balls are larger, underfill is not required, and the larger ball pitch allows assembly with surface mount equipment.

Some advantages include the following:

- Considerable space savings resulting from the elimination of the first level package (mold compound, lead frame, or organic substrate). For example, an 8-lead MicroCSP occupies only 8% of the board area taken up by an 8-lead SOIC.
- Improved electrical performance, such as reduced inductance, due to the elimination of wire bonds and leads used in standard plastic packaging.
- Lighter weight and thinner package profile, due to the elimination of lead frame and molding compound.
- No underfill required; standard SMT assembly equipment can be used.
- High assembly yields resulting from the self-aligning characteristic of the low mass die during solder attachment.

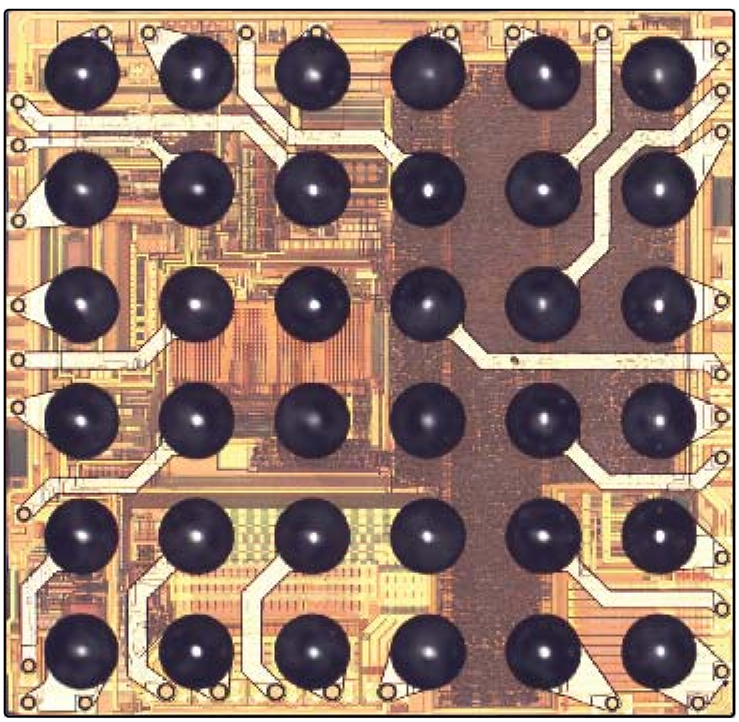

Figure 1. Photograph of a 6 x 6 MicroCSP

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MicroCSP CONSTRUCTION AND CONFIGURATIONS

MicroCSP CONSTRUCTION

A MicroCSP die has a first layer of organic dielectric (polymer-1) and, if redistribution to a standard array is required, a metal layer to carry current from the bond pad to the solder ball. This metal redistribution layer (RDL) is then covered with a second polymer layer (polymer-2) that is patterned into the solder ball array. To prevent diffusion and enable solder wetting, an under-bump metallization (UBM) layer is deposited on the RDL. The solder ball is a lead-free alloy.

Figure 2 illustrates a redistributed die of bump-on-polymer construction. The bump sits on polymer-1, which provides a compliant support for relief of mechanical stress after assembly on a circuit board.

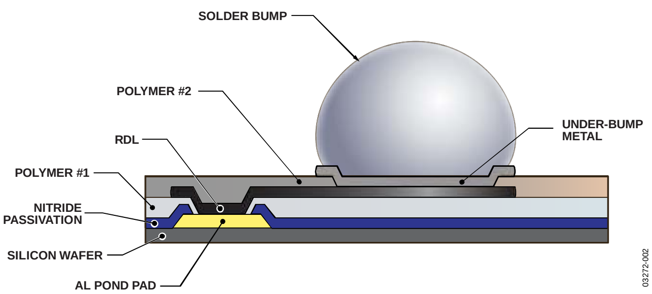

Figure 2. Typical Construction of a MicroCSP Redistributed Die

Figure 3 illustrates direct placement of a ball on a wirebond pad, which is typically smaller than the solder ball. Polymer-1 isolates the ball from the passivation, and polymer-2 defines the solder-wetted area of the UBM.

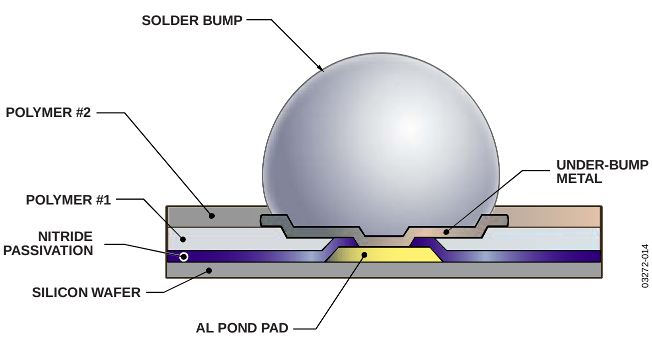

Figure 3. Typical Construction of a Direct Bump MicroCSP

MicroCSP CONFIGURATIONS

All MicroCSP parts from Analog Devices have a standard pitch of 0.5 mm and a standard bump diameter of either 0.320 mm (large bump) or 0.180 mm (small bump).

For this reason, each array offered has a minimum die size (and, therefore, package size) to accommodate the standard bumps and pitches. See Table 1 for details of standard MicroCSP arrays, which have an array pitch of 0.5 mm and a ball approximately 320 μm wide.

Table 1. Minimum Die Size for MicroCSP Arrays at 500 μm

Array	Maximum I/O	Minimum Die Size
2 × 2	4	1.0 mm × 1.0 mm (39 mils × 39 mils)
2 × 3	6	1.0 mm × 1.5 mm (39 mils × 59 mils)
3 × 3	9	1.5 mm × 1.5 mm (59 mils × 59 mils)
3 × 4	12	1.5 mm × 2.0 mm (59 mils × 79 mils)
4 × 4	16	2.0 mm × 2.0 mm (79 mils × 79 mils)
4 × 5	20	2.0 mm × 2.5 mm (79 mils × 99 mils)
5 × 5	25	2.5 mm × 2.5 mm (99 mils × 99 mils)
6 × 6	36	3.0 mm × 3.0 mm (119 mils × 119 mils)

TYPICAL MicroCSP DIMENSIONS

A photograph and a package outline drawing of a 3 × 2 array are shown in Figure 4 and Figure 5. All MicroCSP devices are laser marked to provide product identification and production lot tracking. Because this is a die size package, the exact size varies with the die, but the solder ball array is fixed according to Table 1, which complies with dimensional specifications of JEDEC Standard MO-211. Silicon thickness is standardized at14 mil.

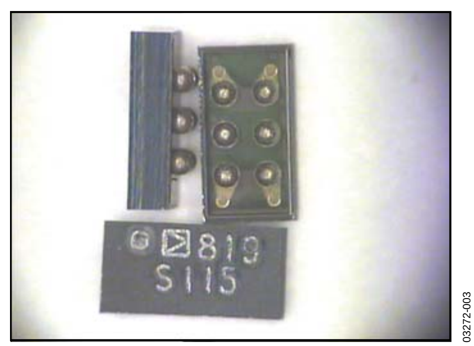

Figure 4. MicroCSP 2 × 3 Array

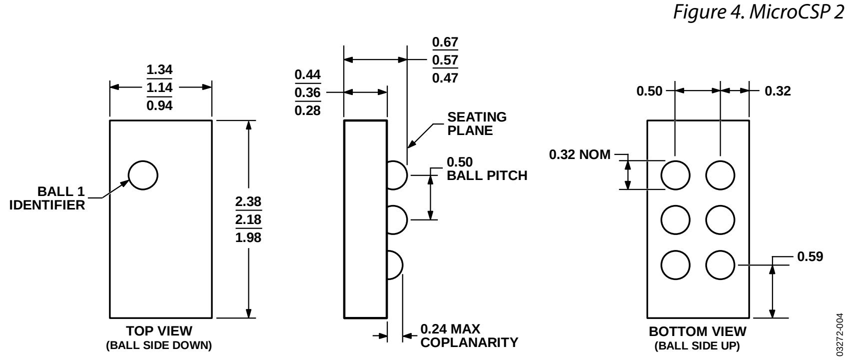

Figure 5. Typical Dimensions Before Assembly

BOARD CONSIDERATIONS

STANDOFF

The actual separation (standoff) after assembly varies with the amount of solder screened on the substrate, weight of the die, wetted area, and so on. Typical dimensions for a die thinned to the standard 14 mils are shown in Table 2.

Table 2. Typical Die Dimensions

Type of Ball	Total Height	Standoff Height
Large Ball	0.575 mm ± 0.03 mm	0.22 mm ± 0.02 mm
Small Ball	0.460 mm ± 0.03 mm	0.115 mm ± 0.05 mm

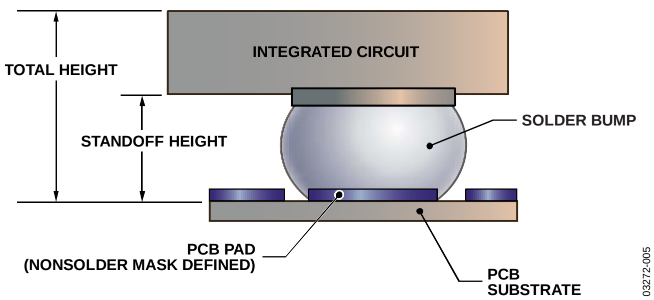

Figure 6. Typical MicroCSP Dimensions After Assembly

SOLDER MASK DESIGN

For PCB fabrication, the following two types of PCB pads/land patterns are used for surface mount assembly:

- Nonsolder mask defined (NSMD). The metal pad on the PCB (to which a package I/O is attached) is smaller than the solder mask opening.
- Solder mask defined (SMD). The solder mask opening is smaller than the metal pad.

The difference between these two types of land patterns is shown in Figure 7.

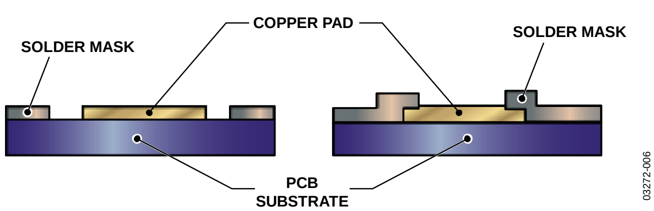

Figure 7. Cross-Sections of NSMD and SMD Pads/Land Patterns

Because the copper etching process has tighter control than the solder mask opening process, NSMD is preferred over SMD. The solder mask opening on NSMD pads is larger than the copper pads, allowing the solder to attach to the sides of the copper pad and improving the reliability of the solder joints.

For an NSMD pad, the trace width connecting the pad diameter should be no more than 60% of the pad diameter. If the PBC design uses via-in-pad, the via should be filled to prevent voiding of the solder joint.

When designing the board, the solder mask registration capability of the board manufacturer should be checked to ensure that the correct solder mask opening dimension is 50 µm on either side of the copper pad. The actual size of the copper pad to be used should be 80% of the diameter of the MicroCSP solder ball. A copper thickness of less than 1 oz is required to achieve the required definition.

BOARD MATERIAL

Standard epoxy glass substrates are compatible with the MicroCSP. Assembly can be performed on standard epoxy glass substrate; however, changing from standard FR-4 to high temperature FR-4, which has a smaller thermal expansion, improves package reliability. The CTE of a PC board can also be affected by factors such as number of metal layers, laminate material, trace density, laminate material, operating environment, site population density, and other considerations. Ideally, the glass transition temperature of the substrate is above the application temperature of the assembled part.

The finish layer on the metal pads has a significant effect on assembly yield and reliability.

- Organic surface preservative (OSP) is recommended as the most appropriate finish. It is less expensive than gold. Check with the PCB supplier on shelf life.
- Immersion silver or tin is an acceptable alternative to OSP.
- Gold can cause embrittlement and reduce reliability. Electroless nickel/immersion gold is acceptable, provided the thickness is limited to <0.5 µm.
- Thinner boards are more flexible and, consequently, show greater reliability during thermal cycling. Standard board thicknesses used in the industry range from 0.4 mm to 2.3 mm. The thickness selected depends on the required robustness of the populated system assembly.

BOARD DESIGN

Due to the high pad density and 0.5 mm pitch of the MicroCSP, any array larger than 3 × 3 bumps that requires connection to the inner bumps is unlikely to be routed on the top PCB layer only.

The traces (track and space) must fit between the limits of the solder mask openings. Routing on the top surface layer of the board, while possible, is usually not a feasible solution, due to the limitations of the geometries imposed by the board fabrication technology. Typical PCB track and space rules are shown in Figure 8.

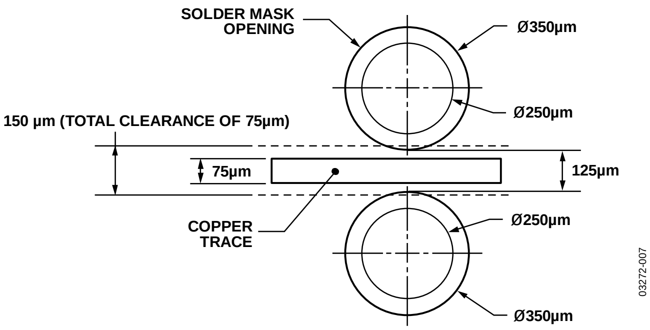

Figure 8. Typical PCB Track and Space Rules

Given a pitch of 500 µm with a typical solder mask opening diameter of 350 µm, there is only 150 µm distance between the solder mask openings. Applying a typical track width and clearance of 75 µm each, this is greater than the required separation between the solder mask openings. Traces and separations of this size are not suitable for high yield manufacturing.

To achieve the necessary separation between pads and traces, using the dimensions outlined above, the pads may need to be modified to nonstandard shapes to allow the traces to pass between them. An example of this is shown in Figure 9, where circular pads have been modified to accommodate adjacent copper traces. However, because changing the PCB pad size and shape affects the actual joint between the bump and the PCB, this also affects the reliability of the joint between the MicroCSP part and the PCB and is not a recommended solution.

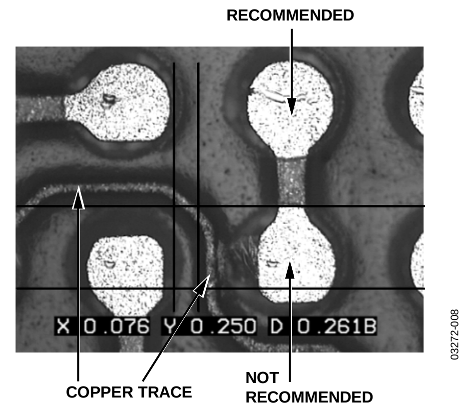

Figure 9. Circular Pads Are Preferred

An alternative to routing on the top surface is to route out on buried layers. To achieve this, the pads are connected to the lower layers using microvias. Standard vias are drilled approximately 300 µm with a pad of approximately 400 µm or larger.

By placing the vias in the pad, the clearance is increased. However, a standard via opening of 300 µm causes the solder to wick down into the via, resulting in weak or open solder joints. In addition, the capture pad is larger than the solder pad.

The use of laser-drilled microvias allows a hole of 100 µm to be drilled in the board that, after plating, is further reduced to 50 µm. The resulting via hole needs to be eliminated by plating to prevent solder wicking down the via. To maximize assembly yield, filled vias must be planar and void free.

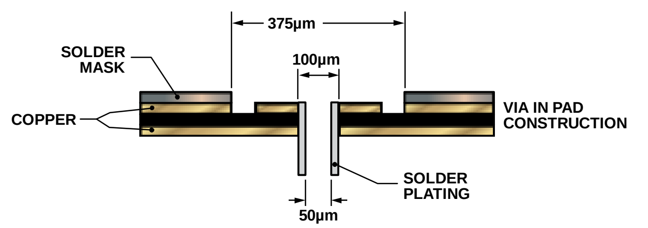

Figure 10. Plated Laser-Drilled Microvia Before Filling

ASSEMBLY CONSIDERATIONS

Board assembly requires solder paste to be screen-printed on the board prior to reflow. The process flow follows:

1. Incoming MicroCSP tape and reel inspection
2. Solder paste print and inspection
3. Chip placement on PCB
4. Solder reflow and inspection
5. Optional flux clean
6. Inspection

Particular attention should be paid to the paste printing. All in-process inspections, such as height and registration, need to be carefully monitored. In addition,

- The stencil should be laser-cut or electroformed. It should be 100 µm to 125 µm thick, with 250 µm square apertures with radius corners. For fine pitch printing, a Type 3 no-clean paste is required and the usual in-process controls (for example, print height) must be applied.
- Automated placement with vision alignment should be used to place the parts, and placement force should be kept to a minimum. Local fiducials are, therefore, required on the board. To minimize mechanical damage, the pickup tool must have a compliant tip.
- After reflow, we recommend X-ray inspection for alignment, bridging, and voids; die shear, and/or die pull.
- A solder paste with a maximum particle size of 40 µm or finer (no-clean) paste is recommended. Because of potential corrosion issues, it is not advisable to use solder paste with active flux.

Reflow profile and peak temperature have a strong influence on void formation.

The reflow temperature should not exceed the maximum temperature for which the package is qualified, according to moisture sensitivity level. The time above liquidus temperature should be about 60 sec, and the ramp rate during preheat should not exceed 3°C/sec. A typical Pb-free profile is shown in Figure 11, based on JEDEC J-STD-20C. The furnace should have a nitrogen purge, and the oxygen content of the furnace must be monitored and kept below 100 ppm. Actual reflow temperature settings need to be determined by the end-user, based on thermal loading effects.

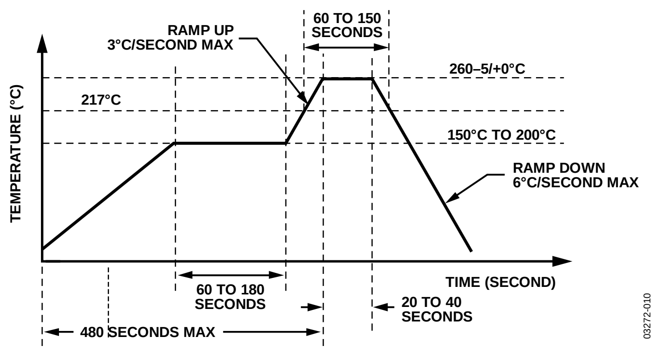

Figure 11. Typical Furnace Profile for Lead-Free Solder

MicroCSP RELIABILITY

FAILURE MECHANISMS

The usual package-related effects due to the encapsulant surrounding the die rarely impact an encapsulant-free MicroCSP package. For example, high temperature electrical failure is often due to movement of ionic impurities derived from the molding compound. Also, moisture can become trapped within the encapsulant and popcorning or corrosion may occur. Neither of these failure modes is observed with MicroCSP packaging technology. Nevertheless, because the die is mounted on a printed circuit board, second level packaging concerns, such as solder fracture during thermal cycling, need to be considered.

Electromigration within the solder ball occurs at the point of highest current density, namely at the passivation opening. At sufficiently high current density, phase separation occurs and voids can form between the solder bump and the UBM.

As with electromigration in thin films such as aluminum, there is a strong dependence on temperature. Data sheet maximum current limits should be observed.

Analog Devices follows a comprehensive new product/new process qualification procedure that is failure mechanism driven. Tests performed accelerate failure mechanisms that may occur under normal life conditions. Failure mechanisms associated with the MicroCSP technology and appropriate stress tests are detailed in Table 3.

QUALIFICATIONS

For several years, Analog Devices has developed test methods for MicroCSP using daisy-chain die to generate solder joint reliability data. This work has been used to complement the qualification of actual die. For actual device qualification, the MicroCSP is mounted on a test board that can be connected to an ATE for full electrical testing. See Table 4 for qualification procedure tests for a 6 × 6 ball array.

Table 3. MicroCSP Failure Mechanisms

Failure Mechanism	Description	Stress Test
Solder Fatigue	Results from the mismatch between coefficient of thermal expansion of the bumped chip and the substrate. This produces high stress at the solder joint, and the bump fails at a low cycle fatigue.	Board level temperature cycling
Corrosion	Corrosion of bump or UBM may result in several types of failures. Chemical reactions may result in an open circuit, or dentritic formation may result in shorts or current leakage.	Autoclave HAST
Intermetallic Compound Formation	May cause solder bump failure due to the excessive formation of intermetallics that can cause solder joint enbrittlement.	High temperature storage
Thermomigration/Electromigration	Describes the migration of bump solder over time. Excessive Sn/Cu or Sn/Ni can result in an open bump at the UBM/solder interface.	High temperature operating life (HTOL)
Underbump Fracture	The fracture of the silicon or passivation under a bump during thermal cycling, resulting in a loss of functionality. The primary factors for controlling fracture are design/layout, brittle passivation, and the manufacturing environment.	Bump/die shear

Table 4. Reliability Qualification Results (6 × 6 Ball Array)

Test Name	Conditions	Test Duration	Sample Size	Fail Quantity
Temperature Cycling	JEDEC-STD-22, Method A104 −40°C to +125°C, one cycle per hour	1000 cycles	135	0
Autoclave	JEDEC-STD-22, Method A102 121°C/15 Psi/100% RH	168 hr	135	0
HAST	JEDEC-STD-22, Method A110 130°C/15 Psi/85% RH	96 hr	135	0
High Temperature Operating Bias	MIL-STD-883, Method 1005 125°C	1000 hr	132	0
High Temperature Storage	MIL-STD-883, Method 1008 150°C	1000 hr	135	0

For MicroCSP packages, the most critical test is temperature cycling. JEDEC-STD-22, Method A104 requires the cycle shown in Figure 12.

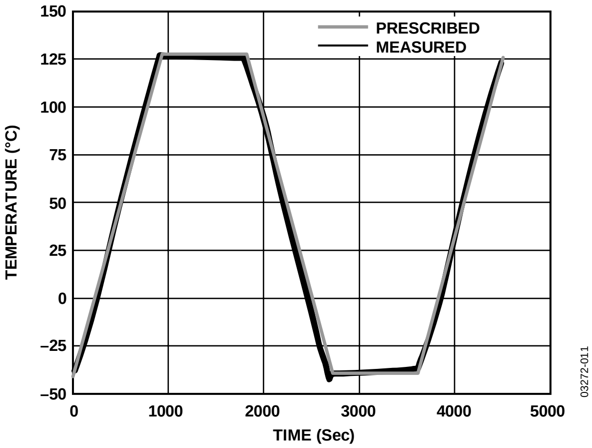

Figure 12. Comparison of Prescribed and Actual Temperature Cycle

A typical board-mounted die is shown in Figure 13. ATE testing is performed before and after the stress tests shown in Table 4.

FATIGUE SIMULATION

As mentioned, solder fatigue is affected by many variables, such as the following:

- Board design, including composition (number of copper layers), thickness, NSMD opening, and composite expansion in all dimensions
- Pad size compared to the wetted area on die
- Solder composition and material properties, such as elastic modulus, plasticity, CTE, and creep
- Temperature range and dwell at temperature extremes
- Ball size and distance from the center of the array to the furthermost ball, known as the distance from the neutral point (DNP)

To affirm published reliability predictions, Analog Devices can provide support for stress modeling using computer simulation. Specific solder ball arrays can be modeled to reinforce internally generated reliability data. Note that the maximum recommended array size for a 500 µm pitch MicroCSP is 6 mm × 6 mm. Beyond that, underfill is required to maintain solder joint integrity.

Figure 13. Example of MicroCSP Reliability Test Boards

THERMAL PERFORMANCE

Thermal performance is determined by heat transfer through the solder balls to the board. This means that MicroCSP thermal comparisons need to include number of balls, board construction, and density of copper traces. Thermal balls that are connected to the ground plane also need to be considered.

The comparison simulations can be simplified by assuming the die is mounted on standard boards (JESD51-9 1s0p and JESD51-9 2s2p), the die is fully populated, and die size increases in approximately 500 μm increments. Table 5 lists the series of arrays, die sizes, and thermal ball counts that modeled with a three-dimensional finite element analysis based on the commercial code ANSYS.

Table 5. Package Constructions Considered for FEA

Array	Max I/O	Thermal Ball	Min Die Size (mm)
2 × 2	4	0	0.96 × 0.96
2 × 1 × 2	5	0	1.3 × 0.9
2 × 3	6	1	0.95 × 1.45
3 × 3	9	1	1.3 × 1.3
3 × 4	10	1	1.5 × 2.0
4 × 4	16	2	2.0 × 2.0
4 × 5	20	2	2.0 × 2.5
5 × 5	25	2	2.5 × 2.5
6 × 6	36	4	3.0 × 3.0
8 × 8	64	7	4.0 × 4.0

Each of the 10 arrays is modeled at 0.25 W power dissipation and 1.25 W power dissipation, with an ambient temperature of 85°C on both 1s0p and 2s2p substrates at three different air flow conditions. Typical results are shown in Table 6, and graphs of the overall trends are shown in Figure 14. The most common thermal metric is the junction-to-air thermal resistance (θ_{JA}), which is the difference in temperature between the junction and ambient, divided by the total power dissipated by the device.

The value of θ_{JA} is dependent on board construction. More copper layers enable heat to be removed more effectively. This relationship is demonstrated by comparing the low effective thermal conductivity test board (JESD51-9 1s0p) with the high effective version (JESD51-9 2s2p) (see Figure 14).

As shown in Figure 14, in the absence of a heat sink attached to the backside (not recommended), the most effective heat transfer occurs through the board.

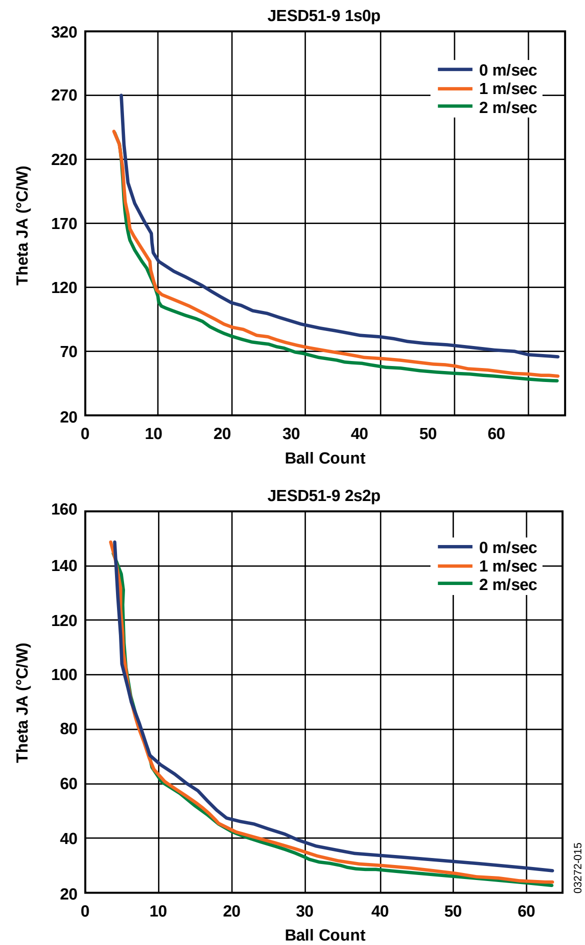

Figure 14. Comparison of θ_{JA} with1-Layer and 4-Layer Boards (0.25 W)

Table 6. Typical Results From Modeling Package Constructions Shown in Table 5

Package Type	PCB	Power	θ_{JA} (°C/W)			θ_{JC} (°C/W)	θ_{JB} (°C/W)
			0 m/sec	1 m/sec	2 m/sec		
5L WLCSP	1S0P	0.25 W	266.6	231.5	217.2	2.5	57.6
		1.25 W	249.5	224.3	212.1	2.7	56.3
	2S2P	0.25 W	148.7	139.7	136.5	2.5	54.6
		1.25 W	146.9	139.4	136.4	2.6	55.2
20L WLCSP	1S0P	0.25 W	108.5	89.0	82.3	0.6	17.1
		1.25 W	101.1	87.3	81.2	0.6	17.5
	2S2P	0.25 W	47.9	43.4	42.1	0.7	9.1
		1.25 W	46.8	43.3	42.1	0.7	9.2
64L WLCSP	1S0P	0.25 W	65.5	50.4	45.8	0.1	7.1
		1.25 W	60.6	49.7	45.4	0.2	7.3
	2S2P	0.25 W	28.0	23.8	22.8	0.2	4.5
		1.25 W	26.9	23.7	22.7	0.2	4.5

REWORK

MicroCSP rework is similar to that of a ball grid array. The board is baked to prevent moisture damage on rework, and the part for rework is heated to approximately 190°C. At this temperature, the solder is molten, and the device is removed with a vacuum wand or tweezers.

The pads need to be dressed and refluxed, and the replacement part precision-placed at the site. Reflow is accomplished in a similar manner to removal, with a nozzle-directed hot air flow.

SHIPPING MEDIA

MicroCSP die are shipped as tape and reel. Pocket tape is dimensioned according to the size of the die. Static dissipative polymer is used for the tape fabrication. Figure 15 shows the typical dimensions in millimeters for the tape to transport a die that measures 1.14 mm × 2.18 mm × 0.56 mm.

To enable pickup from the top, the die are placed in the antistatic carrier tape bump side down. In accordance with EIA-481-C, Pin A1 is on the sprocket hole side.

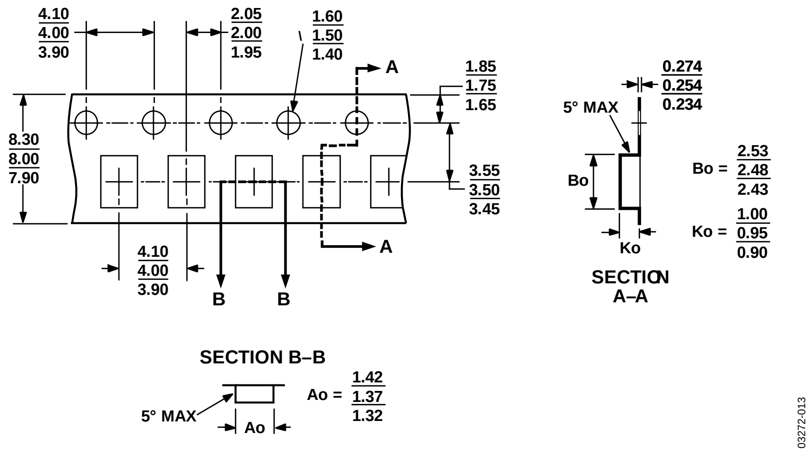

Figure 15. Typical Dimensions for the Tape to Transport a Die

NOTES

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