ANALOG DEVICES

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APPLICATION NOTE

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Evaluation Board for the AD7712, 24-Bit Sigma-Delta A/D Converter

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INTRODUCTION

This application note describes the evaluation board for the AD7712 24-bit signal conditioning A/D converter. This converter utilizes sigma-delta techniques to offer 16-bit accuracy (0.0015% FSR) and no missing codes to 24 bits. It contains a two-channel programmable gain front end, a programmable low-pass digital filter and a bidirectional serial interface. One of the analog inputs and the reference input are differential, and the part can accept inputs as low as 20 mV full scale on this differential analog input. The second analog input contains an input attenuation circuit and can accept inputs up to ±10 V. The part features a self-calibration mode that removes internal offset and gain errors, a system calibration mode that removes external circuit offset and gain errors, and a background calibration mode that automatically removes internal offset and gain errors. In addition, its flexible serial interface allows the AD7712 to connect directly to digital signal processors (ADSP-2101, TMS320C25, etc.) and microcontrollers (8XC51, 68HC11, etc.). Full data on the AD7712 is provided in the AD7712 data sheet available from AnalogDevices and should be consulted in conjunction with this application note when using the evaluation board.

On-board components include an AD680, +2.5 V reference (the part's own +2.5 V reference can also be used), a 10 MHz crystal (an external clock source can also be used), and bus buffers to facilitate the AD7712's two serial interface modes.

The basic evaluation board schematic is shown in Figure 1 while a full circuit diagram for the board is shown in Figure 3. The component silkscreen, component side layout and solder side layout for the evaluation board are given in Figures 4, 5 and 6 respectively.

LINK OPTIONS

The AD7712 Evaluation Board has several link options available to facilitate a variety of operating conditions and these are summarized in Table I. The position of the link options should be chosen before any power is applied to the evaluation board.

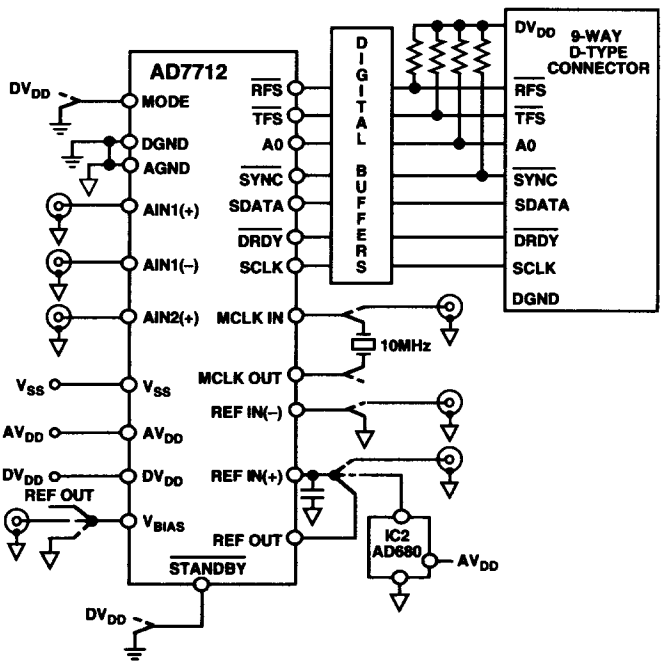

Figure 1. Evaluation Board Basic Schematic Diagram

Table I. Link Options

Link No.	Function
LK1	This option selects the serial interface mode for the AD7712. It is a double link (both links must be moved together for correct operation) which sets the AD7712 MODE pin and configures the bidirectional buffer on the serial clock. With both links in Position A, the MODE input is low putting the device into its external clocking mode; the AD7712 SCLK pin is configured as an input, and the serial clock buffer (74HC125) is configured as an input. With both links in Position B, the MODE input is high putting the device into its self-clocking mode; the AD7712 SCLK pin is configured as an output, and the serial clock buffer (74HC125) is also configured as an output.
LK2	This option selects the master clock source for the AD7712. The master clock source comes from the on-board crystal or from an external clock source via SKT6. It is a double link (both links must be moved together for correct operation). With both links in Position A, the external clock is selected. The external clock for the AD7712 must be applied to SKT6 which is routed to the MCLK IN pin of the AD7712. With both links in Position B, the on-board 10 MHz crystal (XTAL 1) provides the master clock for the device. With the links in this position, the crystal is connected between the MCLK IN and MCLK OUT pins of the AD7712.
LK3	This link is used to short out the resistor in the reference decoupling scheme. With this link option in place the reference decoupling resistor, R4, is shorted out. When the AD680 reference is used as the reference source for the device, this link option should not be in place. When using the AD7712's own internal reference or when using an external reference which does not require any decoupling resistor, this link should be in place.
LK4	This option is used to select the reference source for the AD7712's REF IN(+) pin. With this link in Position A, the AD7712's own on-chip reference is used as the reference source for the AD7712 and REF OUT is connected directly to the REF IN(+) input. With this link in Position B, the AD680 +2.5 V reference is used as the reference source for the AD7712 and the AD680's V_{OUT} pin is connected, via the decoupling components, to the REF IN(+) input. With this link in Position C, an external reference, applied to SKT7, can be used as the reference source for the AD7712 and SKT7 is connected, via the decoupling components (see LK3), to the REF IN(+) input.
LK5	This option is used to select the voltage source for the AD7712's REF IN(−) pin. With this link in Position A, the REF IN(−) pin of the AD7712 is connected directly to AGND. If the AD7712's own reference is used as the reference source for REF IN(+), REF IN(−) should be connected to AGND. With this link in Position B, an external voltage, applied to SKT8, can be used as the reference source for the AD7712's REF IN(−) input and SKT8 is connected directly to the REF IN(−) input. If an external differential voltage is required for the AD7712 it should be applied between SKT7 and SKT8 with LK4 and LK5 set appropriately.
LK6	This option is used to select the voltage source for the AD7712's V_{BIAS} pin. With this link in Position A, the AD7712's own on-chip reference is used as the voltage source for the V_{BIAS} input and REF OUT is connected directly to the V_{BIAS} input. With this link in Position B, the V_{BIAS} input is connected directly to AGND. With this link in Position C, an external voltage, applied to SKT5, can be used as the voltage source for the V_{BIAS} input and SKT9 is connected directly to the V_{BIAS} input.
LK7–LK9	These links are in series with the AIN1(+), AIN1(−), and AIN2 analog inputs respectively. With link LK7 in place, SKT2 is connected directly to the AIN1(+) input. With LK8 in place, SKT3 is connected directly to the AIN1(−) input. With link LK9 in place, SKT4 is connected directly to the AIN2 input. These links may be removed so that the input signals at SKT2 to SKT4 can be connected to the component grid for signal conditioning before being applied to the analog inputs of the AD7712.
LK10	This link is used to short out the Schottky diode, D2, on the AV_{DD} supply when the device is operated with AV_{DD} and DV_{DD} driven from the same supply. When AV_{DD} and DV_{DD} are driven from different supplies, and the short-circuit current capability of the DV_{DD} supply is too large for the Schottky diode, D1, then link option LK10 should be removed placing diode D2 in series with the AV_{DD} line.
LK11	This link is used to determine whether the AD7712 operates in its normal or standby mode. With this link in Position A, the device is in its normal operating mode. With this link in Position B, the part is in its standby mode, shutting down internal analog and digital circuitry with power consumption reduced to less than 100 μW.

POWER SUPPLIES AND GROUNDING

The AD7712 has three power supply inputs: AV_{DD}, DV_{DD} and V_{SS}. The AV_{DD} range is from +5 V to +10 V, DV_{DD} is +5 V, and V_{SS} is 0 V or −5 V. There is an additional requirement that $AV_{DD} - V_{SS}$ must be less than 10.5 V. The evaluation board caters for all options by providing AV_{DD}, DV_{DD} and V_{SS} inputs. If AV_{DD} = +5 V and DV_{DD} = +5 V, it is recommended that AV_{DD} and DV_{DD} are driven from the same +5 V supply to avoid any power sequencing issues. In applications where two separate supply voltages are required for AV_{DD} and DV_{DD}, the 10 Ω resistor, R9, and the SD103C Schottky diode, D1, provide protection for the AD7712. In applications where the short-circuit current capability of the DV_{DD} supply is too large for the SD103C, link option LK10 should be removed placing diode D2 in series with the AV_{DD} line.

All supplies are decoupled to ground with 10 μF tantalum and 0.1 μF ceramic disc capacitors. The AV_{DD} and V_{SS} supplies are decoupled to the AGND plane while the DV_{DD} supply is decoupled to the DGND plane. Power for the digital section of the board and the DV_{DD} pin of the AD7712 is routed separately from the power for the analog section and AV_{DD} on the AD7712. For systems using a single +5 V supply for AV_{DD} and DV_{DD}, the AV_{DD} and DV_{DD} input terminals should be connected together.

The evaluation board uses extensive ground planing to minimize any high frequency noise interference from the on-board clocks or any other sources. Once again, the ground planing for the analog section is kept separate from that for the digital section, and they are joined only at the AD7712 AGND and DGND pins.

ANALOG INPUT SECTION

The AD7712 provides two analog input channels, one differential input and one attenuated single-ended input. The analog inputs to the evaluation board are applied to the subminiature BNC connectors labelled SKT2, SKT3 and SKT4. With links LK7 through LK9 in place these BNC connector inputs are routed directly to the AIN1(+), AIN1(−), and AIN2 inputs of the AD7712. These links can be removed to allow the input signals at SKT2 to SKT4 to be routed to the component grid if input signal conditioning is required. There is also the option of placing R, C antialiasing filters on each analog input line. These antialiasing components are not provided with the board, but the wire links can be removed on the analog input lines to insert resistors (these resistor positions are labelled R1 through R3 on the silkscreen). There are also plated-through holes to allow insertion of capacitors on each line (these capacitor positions are labelled C11 through C13 on the silkscreen).

REFERENCE INPUT

The reference input for the AD7712 is a differential input with the reference voltage, V_{REF}, equal to the difference between the REF IN(+) pin and the REF IN(−) pin. The evaluation board allows the reference to be generated from three sources using link options, LK4 and LK5. Table II summarizes the reference link options. There is an additional link, LK3, also used with the reference. When in place, LK3 shorts out the reference decoupling resistor, R4. This decoupling resistor is required when using the AD680's V_{OUT} pin as the reference source for REF IN(+). It may also be required by external reference sources. The REF IN(+) input is decoupled to AGND via C14, a 0.1 μF ceramic disc capacitor.

Table II. Reference Link Options

LK4 Position	LK5 Position	REF IN(+) Voltage	REF IN(−) Voltage
A	A	REF OUT	AGND
B	A	AD680 V_{OUT}	AGND
C	A	SKT7 I/P	AGND
C	B	SKT7 I/P	SKT8 I/P

The first of the reference options is to derive the reference voltage from the AD7712's own internal reference. R4 can be shorted out using LK3 when REF OUT is driving REF IN(+). REF OUT provides a single-ended, +2.5 V reference which is referred to AGND. Therefore, when REF OUT is connected to REF IN(+), the REF IN(−) input should be connected to AGND via LK5. The second option is to use the AD680's V_{OUT} pin as the reference source for REF IN(+). In this case, LK3 should be removed. Once again, the AD680 provides a single-ended, +2.5 V reference which is referred to AGND. Therefore, when the AD680 V_{OUT} pin is connected to REF IN(+), the REF IN(−) input should be connected to AGND via LK5.

The third option is to use an external voltage as the reference source for the part. This external reference voltage is applied to the evaluation board at SKT7. This external reference voltage can be single-ended (in which case REF IN(−) is connected to AGND via LK5) or it can be a differential voltage applied between SKT7 and SKT8. LK5 can route the voltage on SKT8 directly to the REF IN(−) input of the AD7712.

V_{BIAS} INPUT

The V_{BIAS} input for the AD7712 provides the return path for most of the currents flowing in the analog modulator. It provides the bias point for much of the analog circuitry in the modulator. The limits on the V_{BIAS} voltage depend on the reference voltage and on the AV_{DD} and V_{SS} voltages. Consult the datasheet to ensure correct biasing. The evaluation board allows the V_{BIAS} voltage to be generated from three sources using link option, LK6. Table III summaries the V_{BIAS} link options.

Table III. V_{BIAS} Link Options

LK6 Position	V_{BIAS} Input
A	REF OUT
B	AGND
C	SKT5 I/P

The first of the options connects the V_{BIAS} input directly to the REF OUT pin of the AD7712. This connection point can be used for either single supply systems (V_{SS} = 0 V) or dual supply systems (V_{SS} = −5 V) with a V_{REF} of +2.5 V. The second option connects the V_{BIAS} input directly to AGND. This connection point can be used for dual supply systems with a V_{REF} of +2.5 V. The third option connects the V_{BIAS} input to SKT5 to allow an external bias voltage to be applied to the AD7712. Note, the V_{BIAS} input should be driven from a low impedance point.

The V_{BIAS} voltage does have an effect on the AV_{DD} power supply rejection performance of the AD7712. If the V_{BIAS} voltage tracks the AV_{DD} supply, it improves the power supply rejection from the AV_{DD} supply line from 80 dB to 95 dB typ. Using an external Zener diode, connected between the AV_{DD} line and the V_{BIAS} input, as the source for the V_{BIAS} voltage gives the improvement in the AV_{DD} power supply rejection performance.

CLOCK GENERATION

There are two clock source options for the master clock for the AD7712 selected by link LK2. This is a double link option, and the device will not operate correctly unless both links of LK2 are in the same position. When both links are in position B, the on-board 10 MHz crystal oscillator is connected between the MCLK IN and MCLK OUT pins of the AD7712, and this generates the master clock for the AD7712. With both links in position A, MCLK OUT is left open-circuit, and MCLK IN is connected directly to SKT6. An external, CMOS-compatible, clock applied to SKT6 will provide the master clock for the AD7712. The frequency of this clock must be in the range from 400 kHz to 10 MHz. Note, for AV_{DD} voltages in excess of +5.25 V, the AD7712 is only specified to operate with a master clock frequency up to 8 MHz.

AD7712 INTERFACE MODE SELECTION

The AD7712 may be set up for either of two serial interface modes. These are controlled on the evaluation board by link option LK1. This is a double link option and the device will not operate correctly in either of the modes unless both links of LK1 are in the same position. The modes are as follows:

1. The Self-Clocking Mode can be used with processors which allow an external device to clock their serial port including most digital signal processors and microcontrollers such as the 68HC11 and 68HC05. It also allows easy interfacing to serial-parallel conversion circuits, allowing interfacing to 74XX299 Universal Shift registers without any additional decoding. In this mode, the AD7712 acts as the master device in the serial system, and data is clocked out of the part on the falling edge of the internally generated SCLK and is clocked into the device during the high time of the same internally generated clock.
2. The External Clocking Mode, is designed for systems which provide a serial clock output which is synchronized to the serial data output including microcontrollers such as the 8XC51, 68HC11 and 68HC05 and most digital signal processors. In this mode, the AD7712 acts as a slave device in the serial system, and data is clocked out of the part on the falling edge of the externally applied SCLK and is clocked into the device during the high time of the same externally applied clock.

Table IV gives the link option positions for the interface modes. Note, inputs A0, $\overline{SYNC}$, $\overline{TFS}$ and $\overline{RFS}$ all have 10 kΩ pull-up resistors to DV_{DD}.

Table IV. Interface Mode Selection

LK1 Position	Interface Mode
A	External-Clocking Mode
B	Self-Clocking Mode

EVALUATION BOARD INTERFACING

Interfacing to the evaluation board is via a 9-way D-Type connector, SKT1. The pinout for this connector is shown in Figure 2, its pin designations are given in Table V, and the pin function descriptions are given in Table VI. The port can be used in both the Self-Clocking Mode and the External-Clocking Mode. The port has nine lines which are described below.

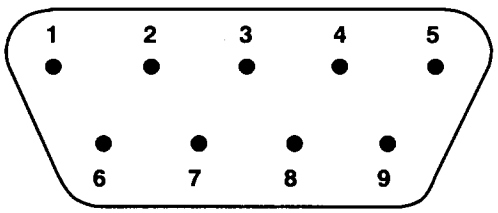

Figure 2. Pin Configuration for SKT1, D-Type Connector

Table V. SKT1 Pin Function

Pin No.	Mnemonic
1	SCLK
2	$\overline{DRDY}$
3	$\overline{RFS}$
4	$\overline{TFS}$
5	A0
6	DGND
7	SDATA
8	DV_{DD}
9	$\overline{SYNC}$

Table VI. SKT1 Pin Function Description

Mnemonic	Description
SCLK	Serial Clock Input/Output. When the device is operating in the External-Clocking Mode, the external serial clock is applied to this terminal and goes via IC3 (74HC125 Quadruple Bus Buffer) to the SCLK pin of the AD7712. When the device is operating in the Self-Clocking Mode, the internal serial clock of the AD7712 is routed to this terminal via IC3. The MODE line controls the direction of buffering on this SCLK line.
$\overline{DRDY}$	This output is the $\overline{DRDY}$ signal from the AD7712 buffered via IC4 (74HC4050 Hex Buffer).
$\overline{RFS}$	This buffered input controls the AD7712 $\overline{RFS}$ input and in conjunction with $\overline{TFS}$ controls the direction of the buffering on the SDATA line. This $\overline{RFS}$ input has a 10 kΩ pull-up resistor to DV_{DD} so that the $\overline{RFS}$ line will be pulled up to its inactive high state even if the $\overline{RFS}$ input terminal is unconnected.
$\overline{TFS}$	This buffered input controls the AD7712 $\overline{TFS}$ input and in conjunction with $\overline{RFS}$ controls the direction of the buffering on the SDATA line. This $\overline{TFS}$ input has a 10 kΩ pull-up resistor to DV_{DD} so that the $\overline{TFS}$ line will be pulled up to its inactive high state even if the $\overline{TFS}$ input terminal is unconnected.
A0	This buffered input controls the AD7712 A0 input. This A0 input has a 10 kΩ pull-up resistor to DV_{DD} so that the A0 line will be pulled up to a logic high state even if the A0 input terminal is unconnected.
DGND	Digital Ground. This line is connected to the digital ground plane on the evaluation board. It allows the user to provide the digital supply via the connector along with the other digital signals.
SDATA	Serial Data Input/Output. When writing to the AD7712 ($\overline{TFS}$ is low), the external serial data is applied to this terminal and goes via IC3 (74HC125 Quadruple Bus Buffer) to the SDATA pin of the AD7712. When reading from the AD7712 ($\overline{RFS}$ is low), the internal serial data output of the AD7712 is routed to this terminal via IC3.
DV_{DD}	Digital +5 V Supply. This line is connected to the DV_{DD} supply line on the evaluation board. It allows the user to provide the digital supply via the connector along with the other digital signals.
$\overline{SYNC}$	This buffered input controls the AD7712 $\overline{SYNC}$ input. This $\overline{SYNC}$ input has a 10 kΩ pull-up resistor to DV_{DD} so that the $\overline{SYNC}$ line will be pulled up to its inactive high state even if the $\overline{SYNC}$ input terminal is unconnected.

SOCKETS

There are eight sockets on the evaluation board. The function of these sockets is outlined in Table VII.

Table VII. Socket Function

Socket	Function
SKT1	9-Way D-Type Connector
SKT2–SKT4	Subminature BNC Sockets for Analog Inputs
SKT5	Subminature BNC Socket for External V_{BIAS}
SKT6	Subminature BNC Socket for External Master Clock
SKT7	Subminature BNC Socket for External REF IN(+)
SKT8	Subminature BNC Socket for External REF IN(−)

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. Figure 4 gives the physical layout of all the links on the board in order to ease setup. Table VIII gives the positions in which the links are set when the evaluation board is sent out.

Table VIII. Initial Link Position

Link	Initial Position
LK1	Double Link in Position A, Setting Board for External Clocking Mode
LK2	Double Link in Position B, Generating AD7712 Master Clock from Crystal Oscillator
LK3	Link in Place, Shorting Out R4
LK4	Link in Position A, Connecting REF IN(+) to REF OUT
LK5	Link in Position A, Connecting REF IN(−) to AGND
LK6	Link in Position A, Connecting V_{BIAS} to REF OUT
LK7	Link in Place, Connecting SKT2 to AIN1(+)
LK8	Link in Place, Connecting SKT3 to AIN1(−)
LK9	Link in Place, Connecting SKT4 to AIN2
LK10	Link Not in Place, Therefore, D2 Is in Series with the AV_{DD} Line
LK11	Link in Position A, Setting Part for Normal Operation

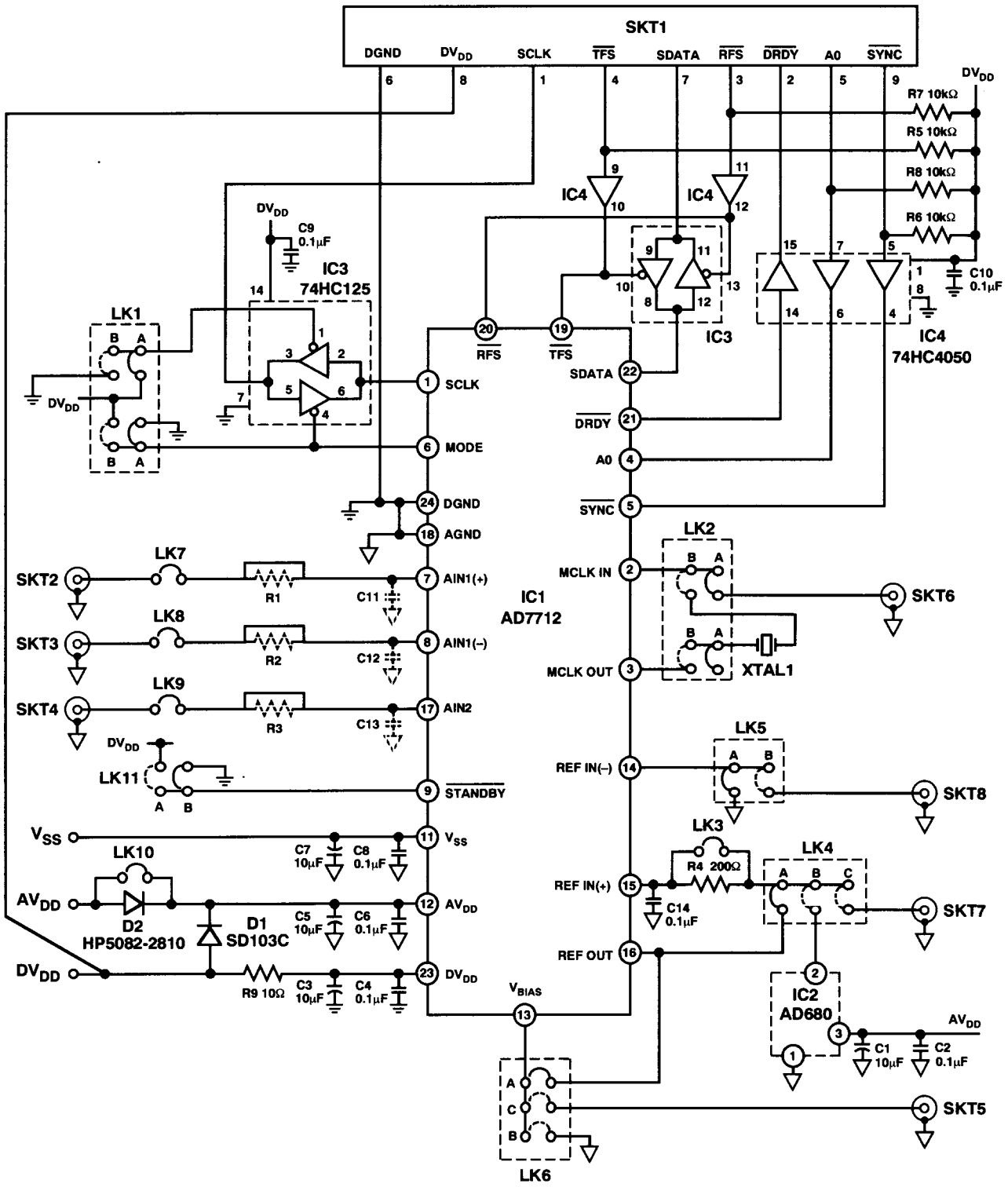

Figure 3. AD7712 Evaluation Board Circuit Diagram

COMPONENT LIST

Integrated Circuits

IC1	AD7712
IC2	AD680 Voltage Reference
IC3	74HC125 Quad Bus Buffers with Three State Outputs
IC4	74HC4050 Hex Buffer

Capacitors

C1, C3, C5, C7	10 μF Capacitors
C2, C4, C6, C8, C9, C10, C14	0.1 μF Capacitors

Resistors

R4	200 Ω Resistor
R5, R6, R7, R8	10 kΩ Pull-Up Resistors
R9	10 Ω Resistor

Optional Filter Components

R1 C11, R2 C12, R3 C13	Can Be Used on Analog Inputs for Filtering. Not Included on Board

Crystals

XTAL 1	10 MHz Crystal

Links

LK1, LK2, LK3, LK4, LK5, LK6, LK7, LK8, LK9, LK10, LK11	Shorting Plugs

Sockets

SKT1	9-Way D Type Connector
SKT2 to SKT8	Subminature BNC Sockets

Diodes

D1	SD103C, Schottky Diode
D2	HP5082-2810, Schottky Diode

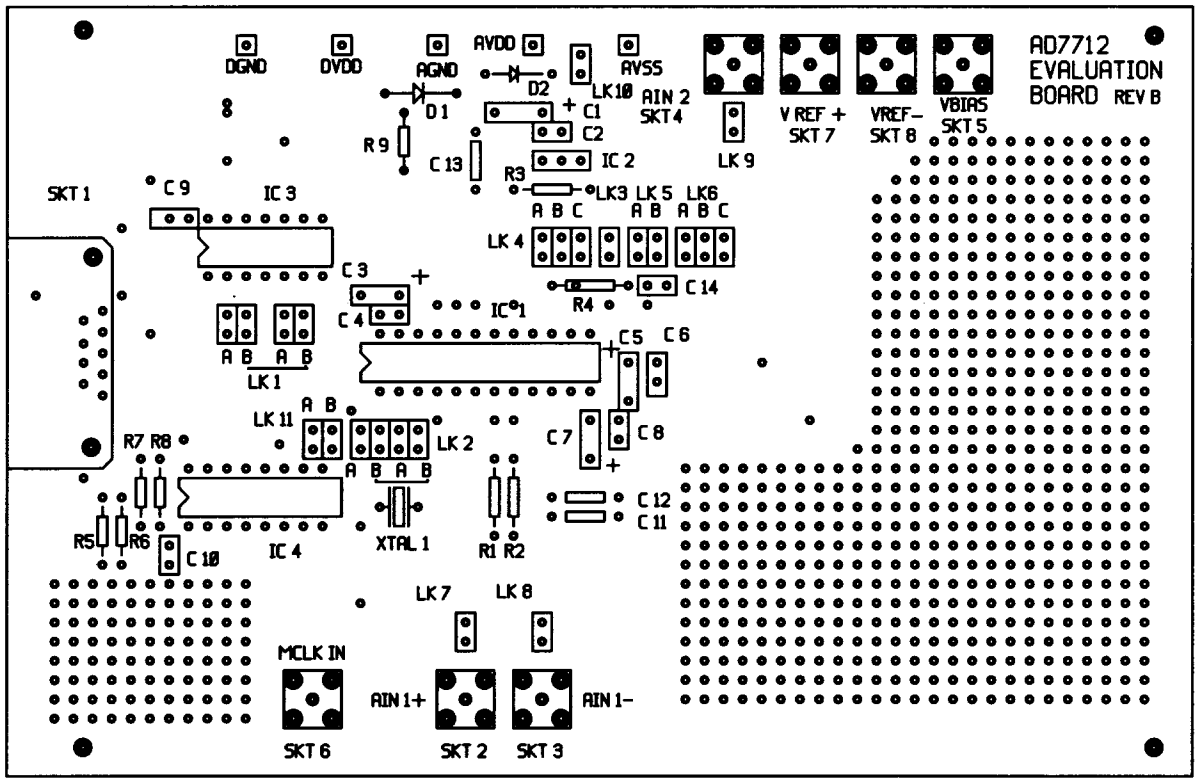

Figure 4. AD7712 Evaluation Board Silkscreen

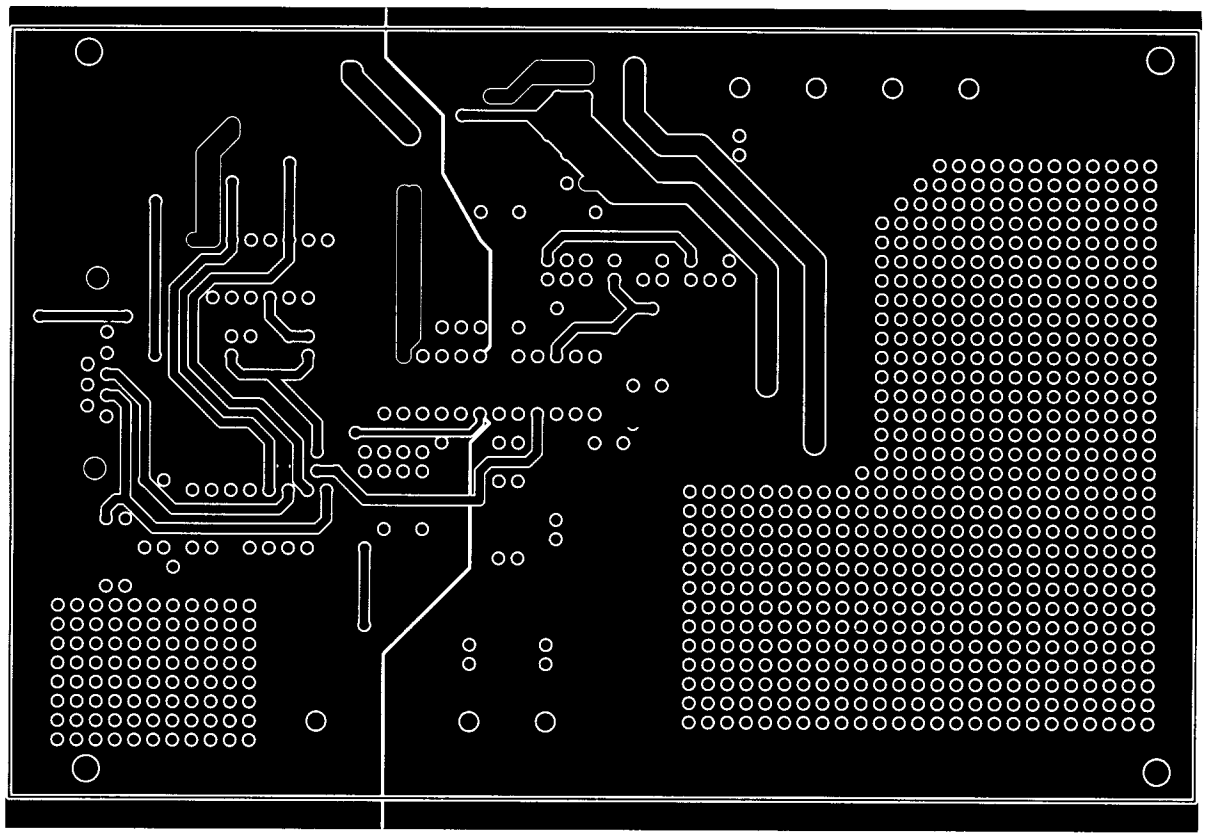

Figure 5. PCB Component Side Layout for Figure 3.

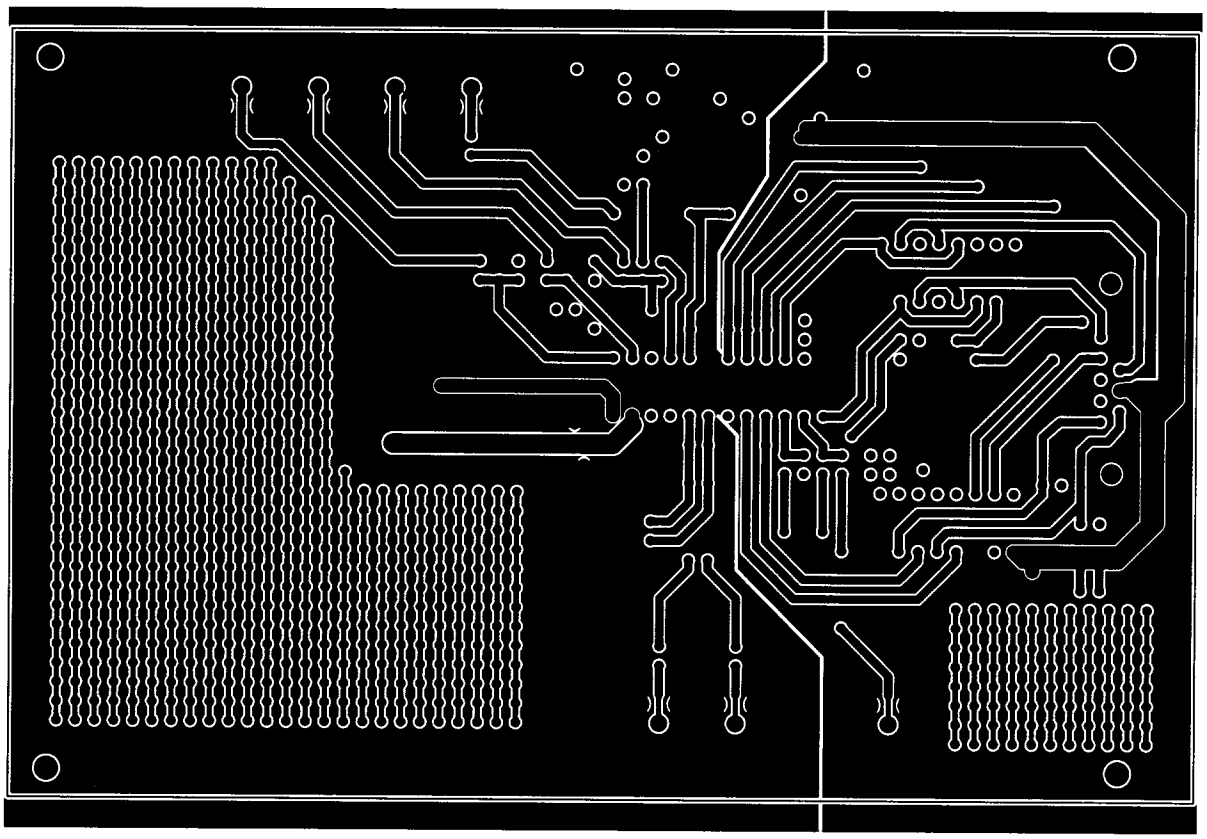

Figure 6. PCB Solder Side Layout for Figure 3.

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