

Using the ADAU1761 in DSP Bypass Mode to Emulate an ADAU1361

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INTRODUCTION

The ADAU1761 and ADAU1361 are low power audio codecs. The primary difference between the two devices is that the ADAU1761 includes a 50 MHz SigmaDSP® core. This document explains how to use the ADAU1761 in a DSP bypass configuration to emulate the ADAU1361.

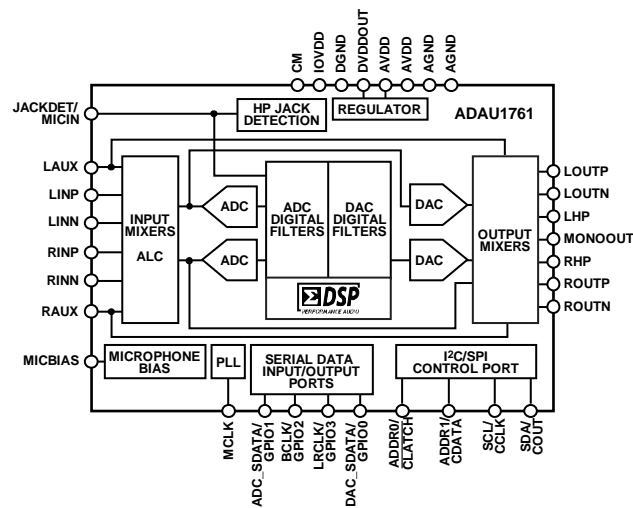


Figure 1. ADAU1761 Functional Block Diagram

REGISTER SETTINGS

Figure 1 depicts the functional block diagram of the ADAU1761. By default, the DSP of the ADAU1761 is disabled upon startup. To emulate the ADAU1361, the following steps should be taken:

1. Enable the IC's clocks in the clock enable registers (Register R65 and Register R66).
2. To bypass the DSP, route the ADC outputs directly to the serial port using Register R59 and route the DAC inputs directly from the serial port using Register R58.
3. Set the serial port sampling rate in Register R64 to the appropriate sampling frequency (f_s) for the application.

Clock Enable Registers

Register R65, Clock Enable 0, and Register R66, Clock Enable 1, enable or disable the digital clock engines throughout the chip. To emulate the ADAU1361, these digital engines must be enabled as specified in Table 1.

Table 1. Clock Enable Register Settings

Register	Address	Data-Word
R65	0x40F9	0xEF
R66	0x40FA	0x03

Bypass the DSP

The ADAU1761 DSP can be bypassed using the serial routing control registers (R58, serial input route control, and R59, serial output route control) as specified in Table 2.

Table 2. Serial Port Routing Register Settings

Register	Address	Data-Word
R58	0x40F2	0x01
R59	0x40F3	0x01

With these settings, the SINRT[3:0] bits in Register R58 are set to serial input [L0, R0] to DACs [L, R]. This setting routes the DAC_SDATA input pin directly to the DACs. L0 refers to the left channel in Slot 0, which is the slot for standard stereo data. Similarly, R0 is the right channel.

The SOUTRT[3:0] bits in Register R59 are set to route the ADC data to serial output [L0, R0]. This setting routes the ADC output directly to the ADC_SDATA output pin.

Serial Port Sampling Rate

The ADAU1361 serial port sampling rate mirrors the converter sampling rate set in bit field CONVSR[2:0] in Register R17, Converter Control 0. The ADAU1761 has a separate register for the serial port sampling rate that needs to be set manually to mirror the converter sampling rate set in bit field CONVSR[2:0] in Register R17. Table 3 shows the proper setting for Register R64, serial port sampling rate.

Table 3. Serial Port Sampling Rate Register Setting

Register	Address	Data-Word
R64	0x40F8	Mirror setting of CONVSR[2:0] in R17

SigmaStudio IMPLEMENTATION

This section explains how to implement the DSP bypass settings on the ADAU1761 using SigmaStudio™. The two main work areas in SigmaStudio are **Hardware Configuration** and **Schematic**. The **Schematic** work area can be ignored because SigmaDSP is not used.

1. Drag a **USBi** communication channel and an **ADAU176x** processor into the **Config** tab of the **Hardware Configuration** tab.
2. Connect the two devices by clicking and dragging from the top blue output pin of the **USBi** cell to the green input pin of the **ADAU176x** cell (see Figure 2).

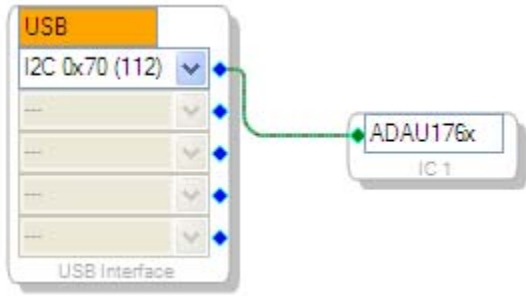


Figure 2. Hardware Configuration Tab

- Go to the **IC1-ADAU1761 Register Controls** tab. Choose a preset for the appropriate input/output configuration and load it by clicking **Load Preset** in the **Codec Setup** tab (see Figure 3). Do not use the **Link/Compile/Download** button.

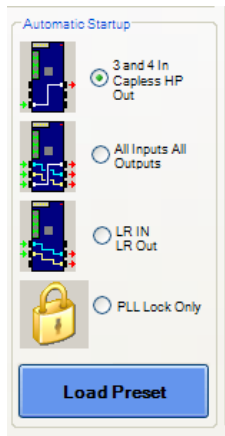


Figure 3. EVAL-ADAU1761Z Presets

This action configures the PLL for operation with the on-board 12.288 MHz oscillator of the ADAU1761 evaluation board. Depending on the preset chosen, different hardware registers are also set. All of the presets enable the clock enable registers in the **DSP Registers** tab, as shown in Figure 4.

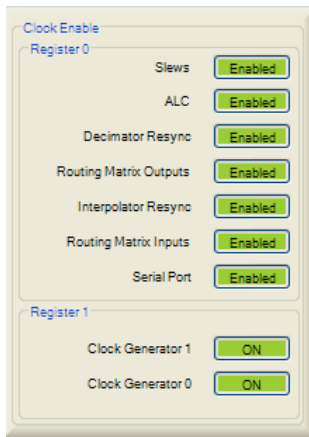


Figure 4. Clock Enable Registers

- In the **DSP Registers** tab, the serial input route control and the serial output route control settings should be set as shown in Figure 5.

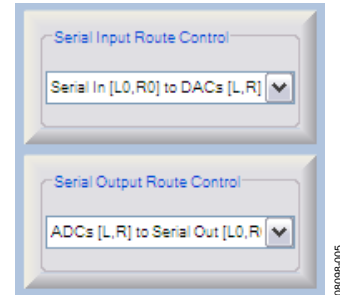


Figure 5. Serial Input/Output Route Controls

- In the **DSP Registers** tab, set the serial port sampling rate to the same value as the converter sampling rate in the **Digital Setup** tab (**Control 0** box).

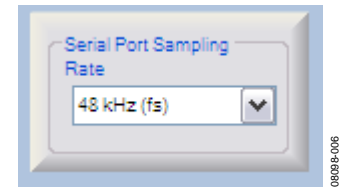


Figure 6. Serial Port Sampling Rate

- The **DSP ON/OFF** and **DSP Run** options in the **DSP Registers** tab are set to be on when SigmaStudio first opens. Turn these options off, as shown in Figure 7.



Figure 7. Disabling the DSP Core

- In the **Codec Setup** tab, click **Load All Registers** (see Figure 8) at the bottom right corner of the window. This action downloads all the settings to the ADAU1761 and enables it with the functionality of the ADAU1361 codec.



Figure 8. Load All Registers Button