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Reliability Handbook

INTRODUCTION

Analog Devices, Inc., would like to thank its customers for making Analog Devices a leading supplier of high quality LSI, VLSI, and ULSI integrated circuits by choosing its products for their design solutions. Analog Devices products are innovative and leading edge from a design perspective. In addition, based on Analog Devices' reliability data, they are exceptionally robust and meet industry standards due to their high reliability.

The broad range of applications of integrated circuit technology has driven Analog Devices' customers' IC quality and reliability requirements to extremely high levels, and Analog Devices has met these challenges. With an extensive variety of programs to ensure high quality and reliability, Analog Devices meets the existing and emerging needs of customers in the true spirit of total quality management (TQM).

This Reliability Handbook introduces customers and potential customers to the research, technological developments, quality/reliability philosophy, and programs employed by Analog Devices. We hope readers find it informative and that the manual becomes a standard reference they find helpful should they wish to set up similar procedures. Analog Devices reserves the right to modify this handbook at any time.

This handbook is published as a reference guide and is in no way to be interpreted as a guarantee that certain products meet the criteria defined here. For specific information regarding dedicated products, refer to the applicable data specification sheet.

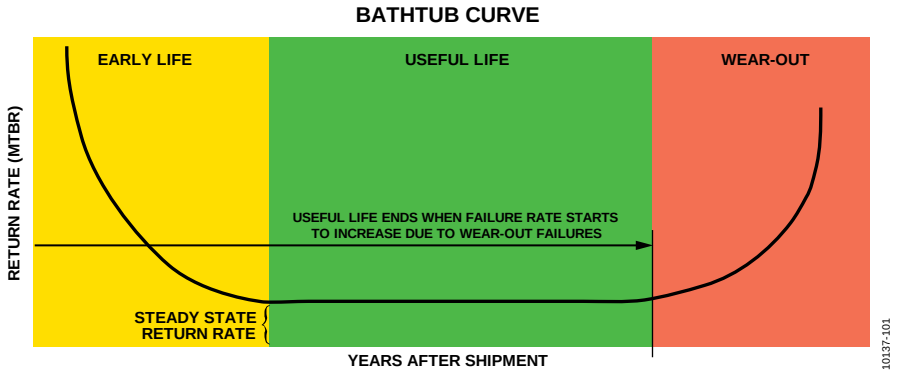

Figure 1. Bathtub Curve

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OVERVIEW

PURPOSE

This document focuses on the activities and criteria that Analog Devices uses to produce very reliable and high quality products that meet customers' requirements. This document is also designed to convey the embedded philosophies on quality and reliability that are embodied in every step of the manufacturing process and in all personnel. Also discussed is Analog Devices' commitment to customer needs and its quest for excellence through continuous improvement at all levels in the design, manufacturing, and support areas of the company.

Using the Bibliography

A Bibliography section is found at the end of this handbook. Numbers in square brackets, such as [1 – 8], indicate references to major topics in reliability. Keeping with this example, [1 – 8] when seen in the text indicates that references 1 through 8 in the bibliography provide more information on the subject under discussion.

ANALOG DEVICES RELIABILITY CHARTER

Analog Devices has always placed the highest emphasis on delivering products that meet the customer's total requirements and, as a result, generate complete customer satisfaction—critical for success and survival in today's integrated circuit industry. This is achieved by incorporating quality and reliability checks not only in all realms of product and process design, but in the manufacturing process as well. This is achieved through careful planning in the design phases of any new development or equipment introduction into any of our facilities utilizing communication and teamwork. Analog Devices strongly believes in the necessity for cross-functional teams and the contributions of individuals to attain excellence in quality and reliability. Our employees are committed to the quality and reliability goals of the company and to continually improving the quality and reliability of Analog Devices processes and services on a global basis.

Consequently, the Analog Devices policy statement on quality is placed in all meeting rooms and in all prominent positions throughout the plant to remind employees that the quest for total customer satisfaction is continual and every employee has a responsibility in ensuring the quality objectives of Analog Devices.

Analog Devices is committed to establishment and continuous improvement of world-class systems and processes aimed at satisfying our customers' evolving needs. We embrace a total quality philosophy with an emphasis on prevention rather than detection. We focus on technology, quality, reliability, service and costs in order to make innovative solutions available to our customers at minimized total cost.

Analog Devices Reliability Goal

The charter of the reliability groups in Analog Devices is to consistently strive to ensure that the reliability of production, new products and processes developed meet and exceed the industry reliability requirements. This is achieved by working in teams with development groups such as wafer fabrication, new product design, packaging and focusing on all aspects of product/process design, incorporating the combined knowledge of the team with the classical bathtub curve and reliability statistics used to describe reliability.

In addition to introducing quality systems that are in full accordance with ISO9000, QS9000, and TS16949 procedures, Analog Devices is continually seeking methodologies to improve quality and reliability through a variety of in-house and internationally developed techniques. With customer satisfaction the key goal, Analog Devices continually focuses its efforts on meeting this objective. This handbook has been developed in keeping with this goal.

Analog Devices is a leading manufacturer of precision high-performance integrated circuits used in analog and digital signal processing applications. The company is organized into product lines with product line management structures for each market segment. These product lines use the design and manufacturing resources from a number of design and manufacturing locations around the world. These sites have exceptionally close linkages and are supported and kept informed by a very capable worldwide sales force with office locations in all major population and industrial centers.

Locations

With design centers worldwide, the corporate headquarters of Analog Devices is in North America is located at

Three Technology Way
Norwood, MA 02062
U.S.A.

Analog Devices' other major U.S. manufacturing locations are as follows:

- 804 Woburn Street
  Wilmington, MA 01187-3462
- 831 Woburn Street
  Wilmington, MA 01187-4601
- 7910 Triad Centre Drive
  Greensboro, NC 27409-9605

Analog Devices' major overseas manufacturing locations are as follows:

- Analog Devices General Trias
  Gateway Business Park
  Javalera, General Trias
  Cavite, Philippines
- Raheen Industrial Estate
  Limerick, Ireland

Analog Devices also contracts with other wafer fabrication and packaging facilities on an ongoing basis, as needed. Consequently, Analog Devices maintains an active program with its vendors and strives to ensure that the highest standards of quality and reliability are achieved. To this end, every vendor must comply with certification, qualification, and a predefined audit program as part of Analog Devices' vendor assurance program. Analog Devices believes that excellence in product and process reliability comes from the people who design and manufacture the products and processes. Upon joining the company, all Analog Devices employees undergo extensive training in their particular functions, followed by ongoing external/internal professional development.

NEW PRODUCT PHILOSOPHY

INTRODUCTION

Analog Devices has achieved its leadership position in the marketplace by releasing innovative products that meet the latent needs of the electronic industry. In turn, these leading-edge products have become market leaders, setting the standards for future products. Produced at various locations around the world, these products serve to illustrate the strong teamwork that is the hallmark of Analog Devices.

Table 1. Examples of Analog Devices' Leading-Edge Products

Model	Leadership Position
AD5790	20-bit DAC with reference with full accuracy
AD7541A	World's first 12-bit CMOS DAC
AD7572	Industry-standard, 12-bit, 5 ms ADC
AD5300	World's first SOT-23 DAC
ADXL362	Nanopower, 3-axis digital accelerometer
AD7714	3 V, low power, 24-bit, Σ-Δ ADC
ADT7320	0.25°C accurate digital output temperature sensor
ADG508F	8-channel, overvoltage, fault-protected multiplexer
AD7723	460 kHz bandwidth, 16-bit, Σ-Δ ADC
AD7891	Multiplexed 12-bit DAC
AD7472	Lowest power, 12-bit MSPS and ADC
AD5700	HART FSK half-duplex industrial modem
AD9250	14-bit, 250 MSPS, dual 1.8 V ADC with JESD204B interface
ADG7xx	Lowest leakage, lowest R_{ON} family of switches
AD7705/AD7706	Lowest power, 16-bit, Σ-Δ ADCs
ADSP-21160 SHARC®DSP	Single instruction, multiple data architecture
ADSP-21065L SHARC DSP	Single instruction, single data architecture
AD9054A	8-bit, 200 MSPS
AD9772	14-bit, 160 MSPS TxDAC+™ with 2× interpolation filter
AD9856	CMOS, 200 MHz, quadrature digital upconverter
AD8361	LF to 2.5 GHz TruPwr™ detector
AD8016	Low power, high output current xDSL line driver
AD8051/AD8052/AD8054	Low cost, high speed, rail-to-rail amplifier
AD8229	Low noise instrumentation amplifier for 210C operation
ADuM6200	Dual-channel signal and power isolator
ADF4351	4.4 GHz phase-lock loop with voltage-controlled oscillator
ADuC7126	ARM7 microcontroller with 16-channel ADC, 4-channel DAC
AD9279	8-channel, low noise ultrasound analog front end
AD8475	18-bit accurate ADC driver amplifier with precision attenuator
AD9523	4 GHz precision clock generator with 14 output drives
ADF7023	ISM band RF transceiver
AD6643	11-bit IF diversity 3G receiver
AD8283	Automotive radar receiver analog front end
AD8488	Digital X-ray charge amplifier
ADIS16407	3-axis accelerometer, 3-axis gyro, and 3-axis magnometer
ADMP521	High fidelity omni-directional microphone with digital output
ADN3000	11 Gbps photo detector with amplifier
ADuM5010	Isolated dc-to-dc converter
ADSP-21479	266 MHz floating-point SHARC DSP with 5 MB SRAM
ADIS16228	3-axis vibration sensor with frequency analysis
ADA4897	31 nV/√Hz, 230 MHz low power amplifier
AD8124	Triple Cat 5 cable equalizer
AD9739	14-bit, 2.5 GSPS transmission DAC

Analog Devices' leadership position has been realized through effective cross-functional teamwork and a new product introduction policy that is extremely proactive. This policy incorporates all aspects of the new product development cycle, culminating in the creation, agreement, and execution of a qualification plan.

Specific development teams are set up for the design, introduction, qualification, and release of each new product. During the new product development cycle, a support group works with the development teams to: (1) ensure adherence to and continuous improvement of procedures across all aspects of the release process; and (2) provide a centralized link between all development areas and manufacturing sites.

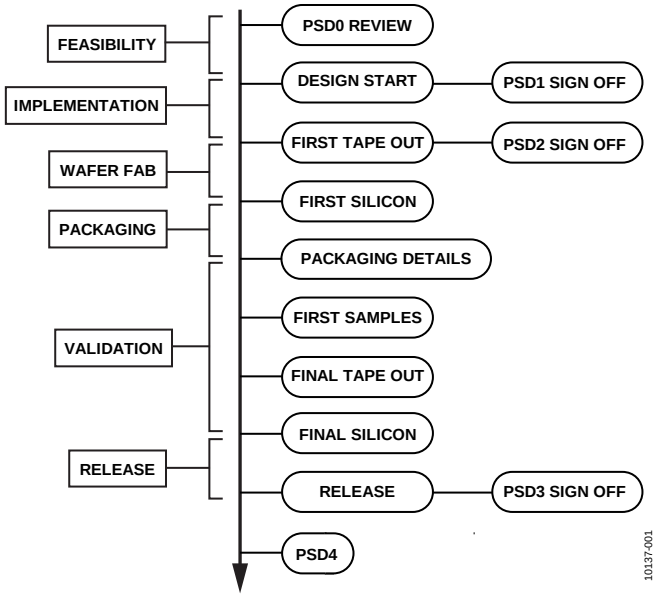

Figure 2. New Product Development Process

There are seven basic milestones in the release of any new product within Analog Devices, starting with the design initiation and ending with the release of the product. The process by which each milestone is met is divided into five distinct phases:

- Feasibility
- Implementation
- Wafer Fabrication
- Packaging and Validation
- Release

If any step in the process is deemed not to be applicable to the development of a new product, the development team is responsible for documenting the reasons. These phases are outlined in Figure 2. Step 1 is the development of a PSD0. This document is a review of 12 critical factors highlighting the strengths and weaknesses of the project. The development team uses it to create a high-quality product start document (PSD1).

FEASIBILITY

The feasibility study begins with a product definition that can come from any number of sources, such as marketing, engineering, or directly from customers. Once agreement has been reached on product definition and feasibility, the product lines allocate the generic model number in accordance with corporate policy. An upper management team sponsor is appointed and a design team is formed consisting of but not limited to: design, CAD, manufacturing, test, quality, and reliability. During the feasibility phase, design engineers assess how to meet market requirements, and various architectures and package options are explored. The manufacturing process is selected, die size estimates are made, and time frames are established for development and release. This work allows the PSD1 to be completed.

During this stage, various resources are allocated to the project and decisions made. An in-depth architecture review is conducted among the project designers and other design engineers outside the project group to secure a balanced perspective on the proposed architecture. The product team also convenes during this period to decide on the characterization plan for the product and to allocate responsibilities. The designer supplies a high-level product simulation to enable the test engineer to gain a good understanding of how the part will perform and to investigate design for test (DFT) strategies.

Prior to completing the product start document, the design engineer discusses with the relevant assembly engineer any issues related to assembly. CAD requirements are also reviewed and resources allocated at this time. Once this step is completed, the PSD1 is signed off.

The PSD1 is a controlled document and signifies the formal start of the project. The PSD1 outlines the roles and responsibilities of the team sponsor, leader, and members. In completing the PSD1, the new product release team must generate a schedule for development and release of the product outlining the resources required. The test feasibility phase begins once the assigned test engineer receives a controlled copy of the data sheet. During this phase, the test engineer considers the technical risks involved and where possible effort can be made to eliminate these risks. The test engineer provides DFT inputs to the design engineer to give the maximum coverage at the probe and final test stages.

IMPLEMENTATION

Prior to commencing a detailed design, the development team generates a list of simulations planned during the design phase. These simulations become the basis of the design review and, at this point, a detailed design is completed and a set of schematics produced. The design engineer calls a design review meeting in which the engineer shows that the desired product performance can be achieved by providing simulation data. If no changes are required, the design proceeds while the characterization plans are reviewed and updated as needed. The layout now begins in accordance with the specified design rules, and additional simulations are done to achieve full-chip simulation. Also during this phase, burn-in, highly accelerated stress testing (HAST), and temperature humidity bias (THB) diagrams are generated and the current density calculations for electromigration are completed. The layout engineer then calls a meeting to review the layout vs. the schematic, and the results of the automated checking procedure are analyzed.

The test implementation phase occurs in conjunction with the design development. During this phase, the test plan and device under test (DUT) board schematics are generated for die sort and final test. Using the agreed upon test plan, the test engineer generates test code and test boards. Following the test review meeting, boards are ordered and the test program completed. At this point, sign-off is given for the stress test diagrams and the qualification plan generated by the product line along with the appropriate reliability engineering group. A manufacturing review is then conducted and the manufacturing review checklist completed. If no issues arise, the die finishing is completed and masks are generated.

WAFER FABRICATION PHASE

While the wafers are being fabricated, the test and wafer sort programs and hardware are prepared along with any stress test boards that are required for qualification. It is also during this phase that the design engineer develops functionality testing capability while the test engineer ports his vectors onto the target test system and performs the required test simulations. While the wafers are in the target wafer fabrication facility, their progress is tracked and monitored by the new products coordinator.

DESIGN VALIDATION

The validation phase consists of design and test validation using very stringent criteria.

On receipt of silicon from the wafer fabrication group, it is the responsibility of the design engineering group to evaluate the level of functionality of the silicon, issue results regularly, and generate a functionality report. On receipt of the report the new product development team will review performance and decide the appropriate course of action. The design evaluation has been completed and the design engineer working with the design evaluation group evaluates all the parameters decided at a characterization review meeting. At this point, the design evaluation engineer issues a design evaluation report, which in conjunction with the test engineering report, provides a basis for continuing with the qualification or redesigning the product. Concurrently, ESD and latch-up are also evaluated to give an indication of the product performance.

TEST VALIDATION PHASE

During this phase, all test programs and hardware are debugged and modifications made. The hardware and software for stress testing during qualification are also analyzed and debugged. Simultaneously, samples are collated for reliability qualification testing per the agreed qualification plan designed as part of the implementation phase. During test validation further program modification occurs and the yield analysis report is generated for review.

RELEASE PHASE

Assuming that all criteria set out to date are achieved, the product moves into the release phase. A formal ESD and latch-up qualification test is performed, as well as the complete qualification testing as dictated by the qualification plan. The release inventory is tested and dispositioned, and the release certificate generated and signed. A PSD4 document, which is a market survey of the product's performance vs. expectations, is produced approximately 18 months after release. Any results from this survey are fed back into the new product development process allowing for continuous improvement.

While the previous description is a snapshot of the new product process, other major milestones, such as provision of samples and data sheet generation, are also underway. One of the major items receiving significant attention on the new product schedule is the new product qualification. This is the final hurdle to overcome before product release; Analog Devices has a proactive qualification procedure based on customer and market requirements. Where applicable, end customers provide input for qualification plans that reflect their individual needs.

QUALIFICATION PLANNING

Analog Devices has a defined corporate qualification procedure that is customer-driven. It recognizes different market segments together with the performance capabilities of manufacturing processes as they mature [1 – 8]. The use of certified processes, qualified product design and layout tools, and continuous improvement is standard.

In the context of process development, process change evaluation, and the evaluation of new products, the approach and philosophy of Analog Devices is to prevent failure. All certification work is failure-mechanism driven, and Analog Devices encourages the use of qualified design rules and software tools for product development to underscore this approach.

The development of both the characterization and qualification plans for significant process changes, new processes, and new products is a team effort with the relevant parties forming a technical review board. The board is comprised of the vested parties as well as reliability engineers. This is Analog Devices' standard qualification plan development procedure; it is incorporated into the new product process just as a dedicated reliability engineer is involved in all phases of product development.

A table of known and potential failure mechanisms is developed, from which the qualification plan is generated based on substitution data. This approach is summarized in Figure 3, Part a and Part b.

Once the failure mechanisms are identified, the appropriate stress tests are defined and evaluated against suitable substitution data. In deciding whether the data is applicable for substitution, some items to consider include

1. When the data was generated
2. Die sizes used
3. Package types used
4. Details of layout
5. New elements introduced
6. Passivation type and laser trim, and so on
7. Design rule violations
8. Process developments and changes

Once the preceding questions are answered, a table of failure mechanisms vs. test methods is generated and a similarity review conducted to investigate the applicability of substitution data. This table is then linked with a process or product change reliability test criteria matrix and the final qualification plan developed. The qualification test list then feeds into another table that indicates the appropriate package types to be used, as well as the test sequence for burn-in, temperature cycle, and so on. Finally, a detailed description of each test is supplied as outlined in Figure 3, Part a and Part b.

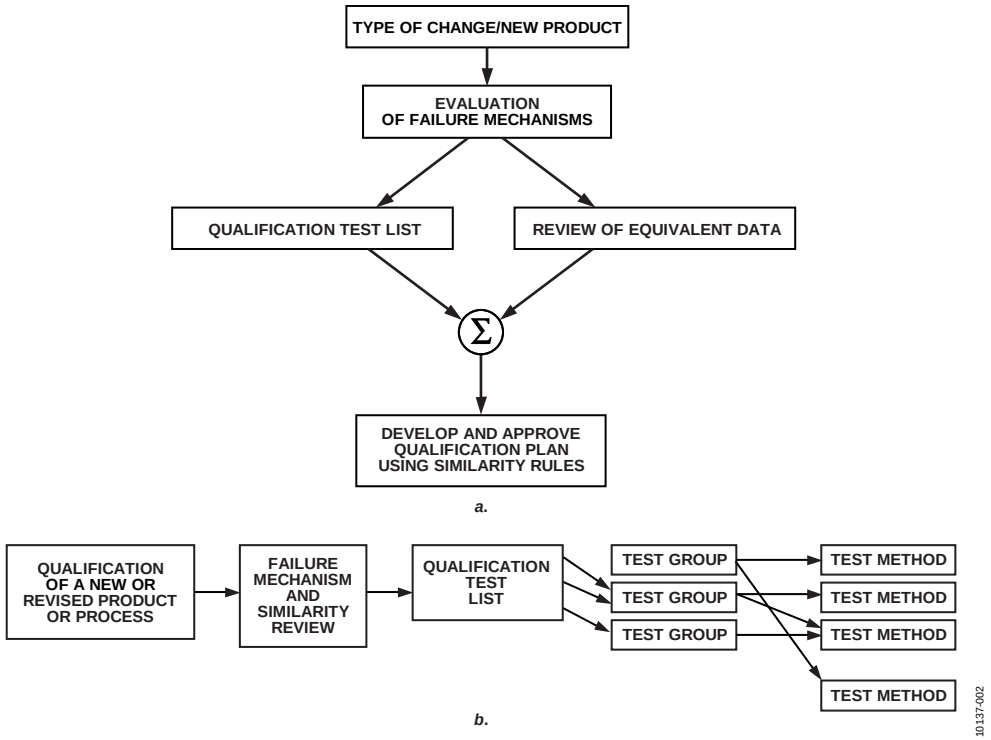

Figure 3. Analog Devices Qualification Philosophy

TEST GENERATION METHOD

This qualification planning methodology allows high quality reliability decisions to be made about the qualification process and reliability criteria by a team of project engineers who, by the nature of their involvement, are exceptionally knowledgeable on these issues. Input on all aspects of design, quality, process, reliability, and manufacturing leads to a well-informed decision and agreement from all departments. It ensures successful completion of the qualification and adherence to standards for the highest quality and reliability. Once the qualification is completed and the product released, a product reliability report is generated. This product reliability report is available upon request.

PRODUCT RELIABILITY MONITORING AND PREDICTION

INTRODUCTION

Analog Devices maintains a very active reliability monitoring program. Analog Devices operates state-of-the-art reliability testing laboratories at its major production facilities; smaller reliability test locations are strategically located around the world.

The objective of the monitoring program is to provide assurance that the product shipped by Analog Devices is of the highest quality. Analog Devices acknowledges that only a snapshot of the production can be monitored. The true reliability of products cannot be gauged by reliability tests alone. Reliability tests are restricted by sample sizes and test capacity. Other factors, such as process control, total quality management, employee training and education, and design for reliability and building in reliability programs are all important factors in the true evaluation of reliability. However, because Analog Devices strongly believes that true reliability is built in and designed in, the company has developed active monitoring programs targeted to these areas.

PRODUCT/PROCESS RELIABILITY

The question often asked of reliability engineers is, "What makes a reliable process and how do you know yours is reliable?" The answer is often quite complex. It is not any one facet of the reliability process that makes a process and product reliable, but a vast combination of items, such as a good product design methodology, good process development and process control, and consistency of manufacturing.

In this chapter, the reliability prediction and monitoring philosophy of Analog Devices is explained. This philosophy is founded on giving the customer the utmost confidence in the reliability of our processes, based on historical data in conjunction with philosophies such as Design for Reliability, and Building In Reliability, as well as tight statistical process control on all our processes and materials.

RELIABILITY GOALS

The reliability goals in the IC industry are generally discussed in conjunction with the traditional bathtub curve shown in Figure 4. This curve shows the failure rate of products with respect to time and is made up of three individual curves related to constant failure rate, quality defects, and wear-out.

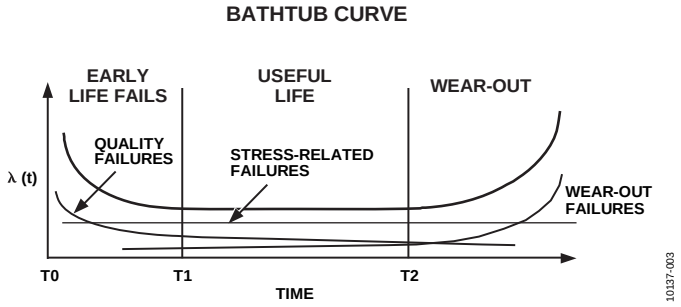

Figure 4. Classic Bathtub Curve

Figure 4 shows that the curve follows a classic bathtub shape [9] (although this is a generalization). The curve consists of three distinct regions: early life, useful life, and wear-out. Each region is characterized separately with potential failures classified as quality failures, random failures, and wear-out failures, respectively. The early life failures can be process related, such as defect-induced, and are characterized by a decreasing failure rate. The wear-out failures, on the other hand, are inherent process limitations and are generally well characterized before process release. These failures are due to oxide wear-out, electromigration, and hot electron effects, all of which limit the life of the product. Wear-out failures typically have an increasing failure rate. Random failures occur for a variety of reasons and typically account for only a very small number of failures. Random failures are characterized by a constant failure rate. The ideal shape to the curve is a very long useful life period and a low amount of quality defects.

PRODUCT RELIABILITY STRESSING

An integrated circuit can potentially undergo a number of stresses during its life; therefore, reliability stress tests have been designed to evaluate the effects of these stresses over time. A device shipped by Analog Devices to a customer is assembled onto a printed circuit board (PCB) using thermal stresses and put into a system for use in the automotive, military, or commercial environments where it will complete its useful life. During its lifetime, the device will likely endure thermal, humidity, and electrical stresses. Therefore, reliability testing must encompass the types of reliability stresses the device will operate under for the test to be meaningful and to evaluate the ability of the product to resist such stresses. Stated another way, the function of reliability stress testing is to evaluate how the product will perform when used in the machines, systems, and environments for which it is manufactured.

This evaluation of reliability begins when the device is in the planning stage. Analog Devices works with its customers to study and understand the application and environment in which the product will be used to establish the appropriate levels of quality and reliability, which are then built into the product design and manufacturing flows and verified at the qualification stage of the new product cycle.

Because of the different types of failures that can occur, many different reliability stress tests can be applied to a product. Generally, they are separated into electrical-, thermal-, and moisture-related tests that have been developed and refined over a period of time. Various models exist to extrapolate the accelerated test conditions to useful life.

RELIABILITY TESTING AT ANALOG DEVICES

Analog Devices conducts all major classes of reliability tests on each of its processes. These tests are conducted in conjunction with the IC design stage and extend to all levels of production to enable the devices to meet customer quality and reliability requirements. At the process design and product design stages, reliability issues such as electromigration, TDDB, and hot electrons are characterized at the process level and checked/verified in the product design phase to provide a robust product. The tests discussed in this section are primarily product-related stress tests; the process-related stress testing used to identify and verify wear-out mechanisms is discussed in the Product/Process Reliability section.

In product stress testing, the main emphasis is on the useful life section of the bathtub curve. The test methodology used to predict the useful life period is typically a steady-state life test, which typically done at Analog Devices under a static or dynamic bias and at a steady-state temperature at 125°C, 135°C, or 150°C for the maximum specified use voltage of the product. The duration at these temperatures is 1,000 hours, 750 hours, and 500 hours, respectively. Analog Devices uses state-of-the-art microprocessor-based equipment. In some instances, the equipment has been designed by Analog Devices engineers in conjunction with vendors to provide the maximum versatility based on operational needs and the product mix test. Accelerated tests are performed on products, and these results are then extrapolated to standard operating conditions.

Because Analog Devices uses these tests to determine product failure rates, it is important to understand how these tests are related to standard operating conditions at accelerated test conditions. It is quite common to use both temperature and voltage acceleration. Before explaining why, it is important to understand the underlying statistical distribution [9 – 11] that is the exponential distribution as well as some of the related terms.

The basic reliability terms are as follows.

Unreliability F(t) expresses the percentage of a population that will fail during time (t).

$$F(t) = r/n$$

where:
r is the number of failing items.
n is the total population.

Reliability R(t) expresses the percentage of a population that will be good during time (t)

$$R(t) = (n - r)/n$$

Failure Density f(t) expresses the percentage of a population that will have failed per unit time during time (t).

$$f(t, t + \Delta t) = \Delta r/n$$

Failure Rate A(t) expresses the percentage of a population that was good until time (t) and will fail during the next unit of time.

$$\lambda(t, t + \Delta t) = \Delta r/(n - r)$$

Other terms include mean time to failure (MTTF or MTBF) and useful life. MTTF is the time period over which a meaningful portion of the population will have failed. In the case of an exponential distribution with a constant failure rate, approximately 63% of the population will have failed by the MTTF = 1/λ.

The exponential distribution is applied to a constant failure rate and is determined by the λ alone, where λ is the failure rate. Mathematically, it is simple to deal with and expresses the useful life period of the bathtub curve with a constant failure rate. Therefore, the exponential distribution is used for the failure rate distribution in failure rate sampling tests. It is also the most fundamental distribution in the field of reliability where:

$$\textit{Probability distribution function} = f(t) = \lambda\, e^{-\lambda t}\ (0 \le t < \alpha)$$

$$\textit{Cumulative distribution function} = F(t) = 1 - e^{-\lambda t}$$

$$\textit{Failure rate} = \lambda\,(t) = \lambda$$

These distributions are shown in Figure 5.

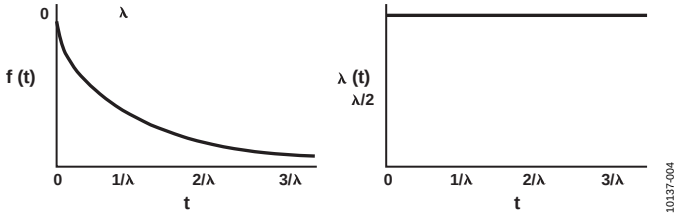

Figure 5. Exponential Distribution

DEVICE TESTING

The practical and effective way of conducting long-term reliability testing to generate long-term failure rates is to expose devices to accelerated conditions of voltage and temperature for periods of time. Long-term reliability testing is done in microprocessor controlled ovens at Analog Devices. These systems are all software controlled with very accurate temperature and voltage control. The schematics are also controlled and coded into the controllers. A major advantage is that the systems are fully operator controlled by one person; this person can perform all of the testing operations, thus eliminating any sources of error in these critical tests. The test results generated at these high conditions are then extrapolated to use conditions. For this extrapolation to be valid, the following two requirements must be met:

1. The accelerated test conditions must not introduce any new failure mechanisms. The accelerated test conditions, that is, temperature and/or voltage, must not generate failure mechanisms that would not be encountered under normal operating conditions.
2. Extrapolation from accelerated conditions to use conditions must be possible.

TEMPERATURE ACCELERATION

This acceleration factor, A_T, is calculated using the Arrhenius equation. Equation 1 relates the use/application temperature of the device to the actual stress condition by using the activation energy (E_a).

$$A_T = t1/t2 = Exp.\ [-E_a/k\ (1/T_{TEST} - 1/T_{USE})] \quad (1)$$

where:
t1 and *t2* are the mean time to failure (MTTF) at T_{TEST} and T_{USE}, respectively.
T_{TEST} and T_{USE} are the test acceleration and use temperatures in Kelvin (K), respectively.
k is Boltzmann's constant (8.617×10^{-5}) eV/K.
E_a is the thermal activation energy for the specific failure mechanism (eV).

Because of the nature of the test and the variety of the products being tested, Analog Devices applies a generic activation energy to its calculation based on the process characterization and its knowledge of the processes. Analog Devices uses an average activation energy of 0.7 eV. This is quite a conservative activation energy compared to Table 2,which lists some of the typical failure mechanisms that could occur in the steady-state period and their activation energies.

Table 2.

Failure Mechanism	E_a (eV)
Oxide	0.8
Contamination	1.4
Silicon Junction Defects	0.8

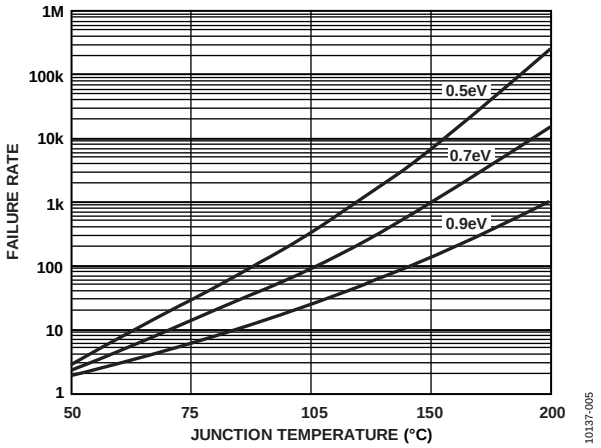

Figure 6. Failure Rate vs. Junction Temperature

The equation also predicts that the reliability will be degraded (increased failure rate) at the higher use temperatures, as indicated in Figure 6.

VOLTAGE ACCELERATION

Voltage-accelerated stress test results can also be translated to nominal voltage conditions in a manner similar to the temperature conditions outlined above by applying a voltage acceleration factor (V_{AF}). The acceleration factor due to voltage stress is approximated by the following exponential relationship:

$$V_{AF} = Exp.\ [\gamma\ (V_T - V_U)] \quad (2)$$

where:
V_T and V_U are the stress and use voltage, respectively, in volts.
γ is a constant value derived experimentally.

Analog Devices sometimes uses voltage acceleration; if it is used, the voltage acceleration constant (γ) is derived from time dependent dielectric breakdown testing, which is equal to 1.

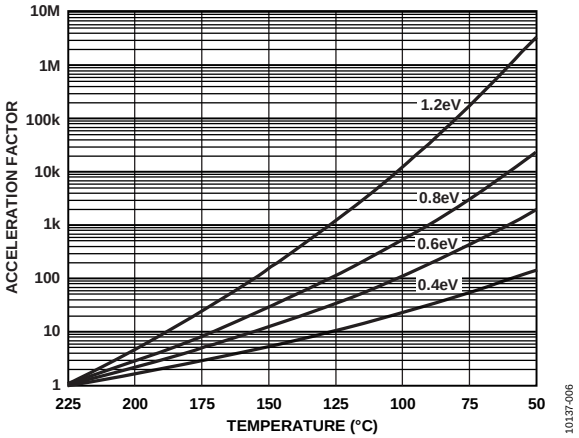

Figure 7. Acceleration Factor vs. Temperature

Analog Devices typically applies temperature acceleration only. This factor dependency on temperature for several activation energies is shown in Figure 7. The graph is normalized to one hour of testing at 225°C.

SAMPLE FAILURE RATE CALCULATION

There are two commonly used failure rate calculations: the instantaneous and the average. The average failure rate is applied to the constant portion of the bathtub curve. The device hours are calculated based on the time the products are being life tested. The appropriate junction temperatures and acceleration factors are calculated. Because the majority of the products manufactured by Analog Devices are low-power CMOS and the ovens can cater to a variety of products, the ambient temperature is primarily used for these calculations. Rather than calculate the lifetimes for each failure mechanism, Analog Devices uses a standard activation of 0.7 eV for the failure rate calculation; for each calculation, Analog Devices reports the results at 60% and 90% upper confidence limits using the chi-squared tables.

The data generated is generally reported in FITs (failures in time), which is the number of failures in 109 device hours that can then be translated to an MTTF. Using this calculation methodology, the infant mortality is commonly reported in DPM or PPM and is simply the proportion of failures compared to the quantity tested.

The following example illustrates the calculation and additional reliability data on all Analog Devices processes. Table 3 is a sample of data collected on an Analog Devices CMOS process at 125°C and 135°C over a 2000 hour, 1000 hour, and 750 hour life test.

Table 3. Data Sampling

Model	Test Temperature (°C)	Sample Size	Reject 168 Hours	Reject 500 Hours	Reject 750 Hours	Reject 1000 Hours	Reject 2000 Hours
AD7357	125	77	0	0		0	
		77	0	0		0	
		77	0	0		0	
ADA4830	125	77		0		0	
		77		0		0	
		77		0		0	
AD8229	125	77		0		0	0
		77		0		0	0
		77		0		0	0

Model	Test Temperature (°C)	Sample Size	Reject 168 Hours	Reject 500 Hours	Reject 750 Hours	Reject 1000 Hours	Reject 2000 Hours
AD9739	135	45	0		0		
		45	0		0		
		45	0			0	
AD9856	135	77	0	0	0		
		77	0	0	0		
		77					0
AD7302	135	45			0	0	
		45			0	0	
		45			0	0	

The failure rate at an operating temperature of T°C. is expressed as

$$Fr = Nf/Ndt$$

where:
Nf is the number of failures.
Ndt is the number of device hours at a test temperature of T°C.

$$Ndt = Nd \times Nh \times A_T \quad (3)$$

where:
Nd is the number of devices tested.
Nh is the number of hours of testing.
A_T is the acceleration factor between the test and the use/application temperature.

The Arrhenius equation

$$A_T = Exp. - [E_a/k\ (1/T_{TEST} - 1/T_{USE})]$$

can be applied to find the acceleration factors where T is measured in K.

At 0.7 eV, the acceleration factors at 135°C and 125°C to 55°C (408 K and 398 K to 328 K), respectively, are (assuming an ambient use temperature of 55°C) as follows:

- 135°C to 55°C $A_T = 128$
- 125°C to 55°C $A_T = 77$

(If voltage acceleration is used, the total acceleration factor (A_{TOT}) can be found by multiplying the two factors to give $A_{TOT} = A_T \times V_{AF}$.)

Applying these acceleration factors to the data shown previously, the equivalent device hours at 55°C can be calculated for 125°C and 135°C.

Table 4.

Test Temperature	No. of Device Hours at Test Temperature	Use Temperature	A_T	Equivalent Device Hours at 55°C
135°C	517000	55°C	128	66176000
125°C	924000	55°C	77	71148000
Total Equivalent Device Hours				137324000

The failure rate can now be expressed in a number of ways.

FIT (failures in time) = $Fr \times 10^9$

Failure Rate (% reject per 1000 hrs.) = $Fr \times 10^5$

MTTF (mean time to failure) = $1/Fr$

The failure rate is essentially the expected frequency of the failures while the MTTF is the interval period between the failures.

The calculation of the failure rate mentioned previously (Nf/Ndt) gives an average expected failure rate, meaning the results are at the 50% confidence level because 50% of the parts are at this rate or better. However, because of the limitations of the test and the fact that small random samples are chosen, statistical effects are significant and the chi-squared distribution is used to put confidence intervals on the results. The confidence intervals typically used are 60% and 90%, respectively.

Using the chi-squared table [12] the failure rate is calculated at

$$Failure\ Rate\ (Fr) = \chi^2\ (x, v)/2\ Ndt$$

where χ^2 is the chi-square value.

$$2\ Ndt = 2 \times device\ hours\ at\ 55°C$$

The chi-square value is based on a particular type of distribution and is found in the χ^2 table where

$$x = (1 - C.L.)$$

where:
C.L. is the confidence level.
$v = (2N + 2)$, where N is the number of rejects

Using the equivalent device hours generated above with zero failures, the calculation is

$$Failure\ Rate\ (Fr) = \chi^2\ (x, v)/2Ndt$$

$$60\%\ C.I.\ \chi^2\ Value = 1.83$$

$$90\%\ C.I.\ \chi^2\ Value = 4.61$$

$$At\ 60\%\ C.I.\ Fr = 1.27 \times 10^{-8}$$

$$At\ 90\%\ C.I.\ Fr = 3.3 \times 10^{-8}$$

Using these figures, the MTTF and FIT rates can be calculated as shown in Table 5.

Table 5.

MTTF	60%	78740157 (Hours)
MTTF	90%	30303030 (Hours)
FIT	60%	11
FIT	90%	27

Using all the data generated for the process from which the previous sample was taken, the actual FIT rates and MTTF figures are as shown in Table 6.

Table 6.

MTTF	60%	150080874 (Hours)
MTTF	90%	59576572 (Hours)
FIT	60%	6
FIT	90%	16

The Annual Analog Devices Reliability Reports indicate the type of data collected from the steady-state life testing conducted by Analog Devices.

When doing MTTF and failure calculations and applying the results for system reliability, various issues must be understood, especially when comparing vendor data. If vendors are using a standard activation energy, this should be realistic and the same activation energy should be applied to both calculations because it can have a significant impact on the thermal acceleration factor.

It is important to know the sample sizes involved. If the sample sizes used are small, the equivalent device hours are small and the resulting failure rate may be artificially high. It is also very important to know the use/application temperature for the product or the temperature to which the vendor has derated because this has a considerable impact on the calculated acceleration factor and the resultant failure rate.

The other predominant mathematical distributions associated with reliability engineering are the Weibull, normal, and the log-normal.

WEIBULL DISTRIBUTION

The Weibull distribution [9 – 11] is a minimum value asymptotic distribution. It is used to express the distribution of material breakdown strength and is very useful for the analysis of lifetime data where the failure time is dependent on the weakest-link phenomena. In this situation the failure of the weakest component causes the part or system to fail. The Weibull can be used to express the wear-out period or the random failure period of the bathtub curve. The distribution has three basic parameters associated with it: a shaping parameter m, a scaling parameter η, and a location parameter γ. The equations, which describe the Weibull distribution, are as follows:

$$f(t) = m/\eta\ \{[(t - \gamma)/\eta]^{m-1}\}\ Exp.\ \{[\ -(t - \gamma)/\eta]^m\}$$

$$F(t) = 1 - Exp.\ \{[\ -(t - \gamma)/\eta]^m\}$$

$$\lambda\ (t) = m/\eta\ [(t - \gamma)/\eta]^{m-1}$$

NORMAL DISTRIBUTION

The normal distribution [9 – 11] is the basic statistical distribution and primarily used to analyze characteristic distributions or variations in either their initial design or after a defined period of time. This distribution is typically associated with statistical process control and determined by a mean, μ, and a standard deviation, σ. The equations, which define the normal distribution, are as follows:

$$f(t) = [1/(2\pi\sigma)^{-0.5}]\ Exp.\ \{-0.5\ [(t-\mu)/\sigma]^2\}(-\alpha < t < \alpha)$$

$$F(t) = [1/(2\pi\sigma)^{-0.5}] \int_{-a}^{t} Exp.\ \{-0.5\ [(t-\mu)/\sigma]^2\}\ dx$$

A normal distribution is called a standard distribution when the mean is 0 and the variance is 1. In this case, f(t) and F(t) are as follows:

$$f(t) = [1/(2\pi)^{-0.5}]\ Exp.\ (-0.5\ t^2)$$

$$F(t) = [1/\ (2\pi)^{-0.5}] \int_{-a}^{t} Exp.\ (-0.5\ x2)\ dx$$

LOG-NORMAL DISTRIBUTION

When the variable is converted to a logarithm, the logarithmic distribution [9 – 11] is generated. This follows the normal distribution. In measuring reliability, the log-normal distribution is used as a distribution for lifetime and for maintenance time. The distribution is defined by a mean value, μ, and a standard deviation, σ, as follows:

$$f(t) = [1/(2\pi\sigma\ t)^{-0.5}\ ]\ Exp.\ \{-0.5\ [\ln\ (t-\mu)/\sigma]^2\}\ (0 < t < \alpha)$$

$$F(t) = [1/(2\pi\sigma)^{-0.5}] \int_{-a}^{t} (1/x)\ Exp.\ \{-0.5\ [(\ln\ (x-\mu)/\sigma]^2\}\ dx$$

Which distribution to use for any given reliability situation is defined by the data obtained and the goodness of fit obtained for the raw data. Therefore, for any given failure mechanism, different models can be applied depending on the process and the data obtained.

Figure 8. Bank of Life Test Ovens

In addition to long-term steady and dynamic life testing, Analog Devices performs continuous short-term monitoring of its processes to establish the PPM infant mortality (IM) or early-life failure rate (ELFR). The ELFR is achieved by burning in products for short durations (<168 hours) at 125°C. The sample sizes for these tests are statistically chosen and products are picked at random from all high volume fabrication processes and package families.

The equipment for doing these tests is all microprocessor controlled, and the schematics for stimulating the product during burn-in and life test are stored as a program to facilitate ease of use and to prevent the wrong programs from being loaded. The typical oven types used vary from location to location, but all can run over a wide range of temperatures. A typical oven configuration is a shown in Figure 8.

Other tests [13 – 18] performed by Analog Devices include combined moisture and thermal testing; equally important from a package assembly and wafer fabrication process perspective. These tests are performed as part of the qualification processes outlined previously and as part of the standard Analog Devices reliability monitoring program.

AUTOCLAVE

The autoclave test, sometimes referred to as the pressure cooker, or steam bomb test, is performed for the purpose of evaluating the moisture resistance of nonhermetic packaged integrated circuits. It employs severe conditions of pressure, humidity, and temperature, not typical of actual operating environments, that accelerate the penetration of moisture through the protective material (molding compound) or along the interface between the external protective material and the metallic conductors passing through it.

When moisture reaches the surface of the die, contaminants and other constituent reactive agents that may be present from manufacturing can corrode the metallization, affecting parametric performance and eventually causing device failure. Other die-related failure mechanisms are activated by this method, including various temperature- and moisture-related phenomena.

Test Conditions (JEDEC-STD-22 METHOD A102)

The devices are placed in a chamber pressurized to 30 ± 1 psia (206 ± 6.8 kPa absolute) with continuous saturated conditions (100% relative humidity). The temperature is held at 121°C and the test duration is 96 hours. Upon completion, the devices are fully electrically tested and all failures analyzed.

Prediction Methodology for Autoclave Testing

Analog Devices views this testing as a rough evaluation of the reliability performance of its products. It is a saturated test, and no models are available for extrapolation to use conditions. Therefore, Analog Devices chooses to publish the raw data in its reliability reports.

Figure 9. Bank of Autoclave Chambers

TEMPERATURE HUMIDITY BIAS (85°C/85%RH)

Temperature humidity bias (or 85/85) life test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid state devices in humid environments. It employs severe conditions of temperature, humidity, and bias, which accelerates the penetration of moisture through the external protective material (molding compound) or along the interface between the external material and the metallic conductors passing through it. While the test is less accelerated than the autoclave testing and takes longer to complete, it provides more realistic results with regard to the field reliability of the device relative to device performance.

When moisture reaches the surface of the die, the applied potential forms an electrolytic cell that can corrode the aluminum. This failure mechanism affects the dc parameters through its conduction and possibly causes failure by opening the metal. The presence of any contaminants greatly accelerates this reaction.

Test Conditions (JEDEC-STD-22 METHOD A101)

The test is conducted for 1000 hours with interval readouts at 168 hours and 500 hours in a controlled environment of 85°C and 85% relative humidity. A dc bias potential is applied continuously in a manner that maximizes the formation of electrolytic cells but minimizes device power dissipation. Before beginning the stress test, all devices are fully tested and receive the appropriate precondition, per JEDEC specifications, to simulate printed circuit board manufacture. On completion of the stress testing, the devices are fully electrically tested and all failures analyzed to determine root cause. When conducting this test, care must be taken to minimize the junction temperature to allow the moisture to reach the die surface.

Reliability Prediction Methodology for Temperature Humidity Bias Testing

THB is the most established humidity test. The methods of prediction are based on the Eyring equation because two stresses are involved. The accelerating factors are temperature and humidity. The acceleration factor is given by the following equation, developed by D.S. Peck [13],

where H1 and H2 are the relative humilities at test that use conditions expressed as a fraction (0 < H <1), and T1, T2 are the test and use temperatures. The other values, E_a and n, are constants derived from testing, while k is Boltzmann's constant.

$$A = (H2/H1)^n \, Exp. \, [E_a/k(1/T1 - 1/T2)]$$

Using this equation, the time to failure can be calculated if the values for E_a and n are known. These values derived by Peck are equal to 2.66 and 0.76, respectively, for electrolytic corrosion. When using these equations, care must be taken to derive the correct values of n and E_a for the particular failure mechanism being evaluated.

Figure 10. Temperature and Humidity Chamber

HIGHLY ACCELERATED STRESS TESTING

HAST uses a pressurized environment to produce extremely severe temperature, humidity, and bias conditions. HAST accelerates the same failure mechanisms as THB but in a much shorter time. In this test, unlike the autoclave test, the devices being tested are biased. Care is taken to keep the power dissipation at a minimum to enable moisture to progress to the die surface. Using the HAST technique, the devices can be operated at temperatures that exceed the boiling point of water while avoiding the unrelated factors introduced by condensation.

Test Conditions

The test is performed at a temperature of 130°C and a relative humidity of 85% RH with a pressure of 33.3 psia or 230 kPa. A dc bias potential is applied in a manner that maximizes the formation of electrolytic cells but minimizes device power dissipation. The equipment and schematics are again microprocessor controlled. Stringent cleaning procedures are followed because cleanliness is exceptionally important for this type of testing. The equipment is shown in Figure 11.

Figure 11. Typical HAST Test System

Reliability Prediction Methodology for HAST Testing

HAST testing is an accelerated form of the 85/85 testing outlined previously. There are three accelerating factors: pressure, temperature, and moisture. The pressure is set by the temperature and humidity settings. The acceleration factors generated are relative to those for 85/85 testing, and the formulae used are similar to those for 85/85 C lifetime prediction. Using Peck's [13] paper and activation energies, the following acceleration factors can be calculated relative to 85/85:

85/85 = 1

120/85 = 10

130/85 = 18

140/85 = 33

TEMPERATURE CYCLE

Temperature cycle testing is conducted to determine the resistance of solid-state devices to alternate exposures at extremes of high and low temperatures. Permanent changes in electrical characteristics and physical damage produced during temperature cycling may result, principally from mechanical stress caused by thermal expansion and contraction. Effects of temperature cycling include cracking and delamination of packages and internal structures, and changes in electrical characteristics resulting from mechanical damage.

Figure 12. Typical Temperature Cycle Test Chambers

Test Conditions (MIL-STD-883 Method 1010 Condition C)

The devices are placed in a chamber so there is no substantial obstruction to the flow of circulating air across each unit. The devices are then cycled between temperature extremes for the required number of cycles.

The temperature extremes are −65°C to +150°C. The time at temperature shall be greater than 10 minutes and the devices under test must reach temperature in less than 15 minutes. The transfer time from hot to cold or from cold to hot must not exceed one minute. Some of the types of equipment available within Analog Devices are shown in Figure 12. While the conditions mentioned above are the maximum that Analog Devices employs, from time to time Analog Devices can use less stringent conditions (that is, −40°C to +125°C), depending on the technology being qualified

Prediction Methodology for Thermal Cycling Tests

There are various methods of predicting lifetimes from thermal tests [19] based on the Coffin Manson laws. One such method is outlined below. Because of the various prediction methodologies, Analog Devices prefers to provide the raw data rather than do lifetime predictions.

$$A = N1/N2 = (\delta T1/\delta T2)^{\alpha}$$

where:
N1 and *N2* are the failed cycle counts.
$\delta T1$ and $\delta T2$ are the operating and test temperature range.
α is derived from experimentation.
A is the acceleration coefficient.

The device lifetime in years is then given by

$$(N \times A)/365$$

where N is the number of days to failure.

HIGH TEMPERATURE STORAGE

The purpose of this test is to determine the effect on solid-state electronic devices of storage at elevated temperature without electrical stress applied.

Test Conditions

The device is subjected to continuous storage at +150°C (−0, +4) for 1000 (−0, +72) hours, except it may be returned to room ambient conditions for interim electrical measurements.

Prediction Methodology For High Temperature Storage Tests

Analog Devices uses the Arrhenius equation if prediction is required from this test to use conditions.

LOW TEMPERATURE STORAGE

The purpose of this test is to determine the effect on solid-state electronic devices of storage at cold temperatures without electrical stress applied.

Test Conditions

The device is subjected to continuous storage at −400°C (0, −5) hours, except it may be returned to room ambient conditions for interim electrical measurements.

LOW TEMPERATURE OPERATING LIFE

The purposes of this test is to subject CMOS devices that are less than 1 µm in size to temperature below −10°C or less junction temperature to measure the time dependent dielectric breakdown with bias.

Test Conditions

The device is subjected to continuous bias at −40°C (0, −5) hours, except it may be returned to room ambient conditions for interim electrical measurements.

RELIABILITY MONITORING PROGRAM

The reliability monitoring program (RMP) employed by Analog Devices is a corporate-wide program driven by corporate manufacturing teams. It is centrally driven to avoid duplication of effort and to free up this valuable reliability resource for qualification and engineering functions. The program is not to be viewed in isolation; it must be remembered that the RMP only gives a snapshot in time of the reliability of the product being produced. The statistical process control, the reduction of variability, yield monitoring, and improvement are among the additional factors that must be considered when reviewing the RMP.

The RMP is intended to generate reliability data for Analog Devices on the most recently manufactured material on a continuous basis. It is intended to identify major life-limiting failure mechanisms, detect long-term process shifts, reduce unnecessary end-of-line testing, and to provide customers with data in continuous support of reliability efforts. The RMP also strives to ensure that in-line controls used for assembly and wafer fabrication are effective.

The procedure generated for the RMP is a live document that is continually updated at the corporate level. The procedure governs all package families, fabrication processes, and manufacturing locations. The product selection plan is based on volume production and reliability sensitivity. Device types are selected based on moderate to consistently high production volumes, susceptibility to stress, ease of failure analysis, and availability.

WAFER FABRICATION PROCESS FAMILIES

Analog Devices' wafer fabrication processes are grouped into families according to similarities. The processes must have the same production design rules, features, fabrication facilities, and reliability characteristics to be similar. One or more products within these wafer fabrication process families are selected as monitor vehicles. Wherever possible, different device types are rotated into the monitor program giving the best possible product-to-process mix, thus ensuring that all stress sensitivities are attended to.

ASSEMBLY PACKAGE FAMILIES

The package characteristics and assembly locations are the primary considerations when grouping packages into package families. The two main packaging families are hermetic and plastic, which are then further subdivided based on lead counts, cavity/lead-frame size, die-attach method, and so on. As a result, a package family can consist of a group of 14-lead to 20-lead SOIC packages manufactured at a particular manufacturing location.

SAMPLE PLANS

Based on expected production volumes, a forecast is given three months in advance to each manufacturing site by the worldwide manufacturing group. This forecast details for each location the agreed-upon wafer fabrication processes by foundry, and the package families/foundries to be monitored in the upcoming quarterly monitor period. Because the RMP is based on production volumes, it also applies to any subcontractors used to manufacture Analog Devices products. An example of the breakdown of lots per production volume is shown in Table 7.

Table 7.

Volume (%)	Lots	Size
0 to 2.5	1	45/77
2.5 to 5.0	2	45/77
…	…	…
>20	5	45/77

The tests run in RMP are based on international standards and include the following tests:

- Early life failure rate
- High temperature operating life test
- Temperature humidity bias or HAST
- Autoclave
- Solderability
- Temperature cycle
- Solder heat resistance

A devised RMP gives as much as a real-time monitor, but Analog Devices recognizes that it is only a snapshot in time for selected lots, as are all reliability monitors. RMP is not Analog Devices' only monitor on reliability; the company maintains a very active and rigorous Statistical Process Control Program as well as a Risk Management Program, both of which use early detection of reliability issues to significantly improve end-of-line reliability. Coupled with these programs is the use of a corporate-wide production management information system and database (PROMIS) that provides all manufacturing instructions and collects all engineering data associated with production lots. This system allows the immediate location and containment of potentially discrepant material, pending any problem resolution and/or corrective actions.

Any failures generated from the reliability monitor plan are failure analyzed to root cause; results are reported to the appropriate wafer manufacturing facilities where corrective actions are established. The data generated by the RMP is published annually on the company website and available for review at the Reliability Data page.

PROCESS RELIABILITY

INTRODUCTION

The reliability of any product depends on the product test, design, assembly, and wafer fabrication processes. There are strict design rules for each of these stages. The function of these rules is to allow the introduction of new products without introducing reliability concerns. The function of the Reliability Engineering group is to see that new wafer fabrication and assembly technologies meet the existing reliability requirements, and to provide a strong platform for future new products and process development.

The Analog Devices philosophy on product and process reliability is based on the premise that reliability must be designed/built-in and cannot be tested-in at a later stage [20 – 32]. As a result, the Analog Devices reliability system is based on three fundamental activities:

1. The independent verification, certification, and qualification of new wafer fabrication processes and package technologies at the extremities of known design parameters.
2. The use of statistical process control at all stages of manufacturing to drive continuous improvement and improve the reliability of the processes
3. The use of rigorous design tools and checkers to identify any potential reliability issues very early in the design phase before committing to silicon.

This system focuses on process development, control, and design rules, and produces highly reliable products. Process reliability is achieved through the building in reliability (BIR) and design for reliability (DFR) programs.

The models used for intrinsic reliability wear-out are industry standard models as recommended by JEDEC specifications for time dependent dielectric breakdown (TDDB), electromigration (EM), stress voiding (SV), hot carrier (MOS HC), bipolar reverse V_{BE} hot carrier, and negative bias temperature instability (NBTI) testing. Safe operating areas (SOAs) are generated for processes using these models by extrapolating lifetimes from characterization data at different conditions.

BIR MONITORS

The BIR monitor program is carried out to monitor all released proprietary processes. The periodicity of the monitor program is dependent on the process run rate and can vary from quarterly to annually, covering all relevant intrinsic wear-out mechanisms. Substitute data is used where possible, and process coverage is defined per process node, for example, 0.6 µm, while treating every wafer fabrication site as a separate entity in terms of coverage.

BUILDING IN RELIABILITY (BIR)

Analog Devices holds the belief that for a process to be reliable, the reliability must be built in at the foundation level because it is very difficult and costly to change and modify the process once it is in production. The reliability groups work in tandem with the process development and manufacturing engineers when they are developing new technologies to facilitate BIR. They strive to ensure that defect densities are reduced to sufficient levels to allow product to be manufactured without significant yield losses or reliability risks. They also characterize the lifetimes for the products by thorough characterization of all wear-out failure mechanisms and by performing accelerated tests on specifically designed test chips.

The main activities related to process reliability are the modeling of wear-out failure mechanisms, detection and reduction of latent defects, and elimination of contamination. Process reliability also includes the determination of reliability related design rules, for example, for EM and hot carrier effects, and the qualification of the process using leading technology products.

TIME-DEPENDENT DIELECTRIC BREAKDOWN (TBBD)

There are various test methods used to predict oxide quality and reliability. Analog Devices uses time-dependent dielectric breakdown testing, commonly known as TDDB [23 – 40] testing, to characterize oxide from a reliability perspective. Other methods such as Qbd and Vbd can also be used; Analog Devices uses both as ongoing monitors within its wafer fabrication facilities to determine the ongoing quality of the oxide.

TDDB testing is done at a constant electric field or voltage and fixed temperature. The test methodology dictates that a constant voltage is placed on the capacitors and the current continuously monitored until a predefined value is reached. When the predefined value is reached, the device under test is considered a failure and the time is recorded for each failure. The failure criterion is generally in microamps and preselected from the Fowler-Nordheim breakdown curves generated for the devices under test. Figure 13 indicates the Fowler-Nordheim curve for 5E4 μm^2 capacitor on a p-type substrate on a 0.6 µm DPDM CMOS process.

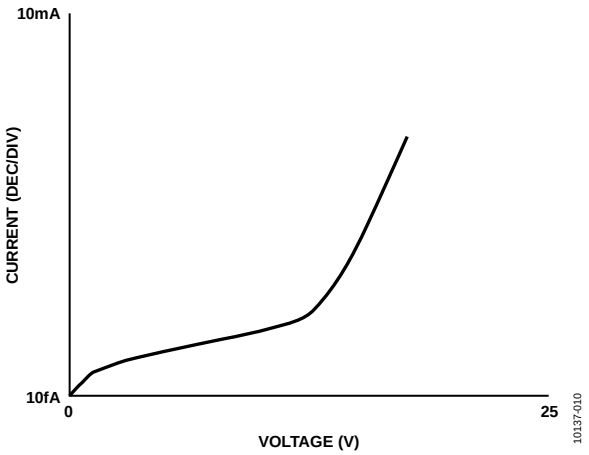

Figure 13. Dielectric Breakdown Curve

BACKGROUND THEORY

Time-dependent dielectric breakdown (TDDB) is a charge injection mechanism, the process of which may be divided into two stages: the build-up stage and the runaway stage.

During the build-up stage, charges invariably are trapped in various parts of the oxide as current flows. The trapped charges increase in number with time, forming high electric fields (electric field = voltage/oxide thickness) and high current regions along the way. This process of electric field build-up continues until the runaway stage is reached.

During the runaway stage, the sum of the electric field built up by charge injection and the electric fields applied to the device exceeds the dielectric breakdown threshold in some of the weakest points of the dielectric. These points start conducting large currents that further heat up the dielectric, which further increases the current flow. This positive feedback loop eventually results in electrical and thermal runaway, destroying the oxide in the end. The runaway stage happens in a very short period.

The gate dielectric varies depending on the gate thickness used in the MOS transistors for a particular process. TDDB is done either on the transistors themselves or more generally on capacitor structures that have a gate oxide thickness equivalent to the MOS structure. Capacitors are typically small, flat structures with the oxide grown on either the substrate or well. It is important to note that TDDB testing is done in accumulation, as shown in Figure 14.

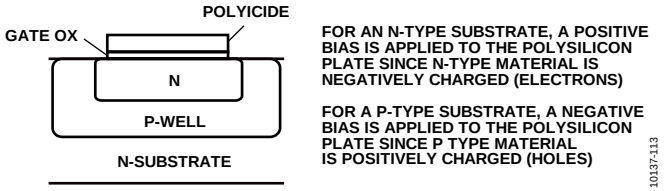

Figure 14. Testing in Accumulation

TDDB testing is done at a constant electric field or voltage and a fixed temperature. A constant voltage is placed across the capacitor, and the current is continuously monitored until a predefined value is reached. When this value is reached, the device under test is considered a failure and the time is recorded for each failure. The failure criterion is generally in microamps (μA) and preselected from the Fowler-Norheim breakdown curves generated for devices under test.

TEST STRUCTURES/DEVICES

TDDB testing is performed on the gate dielectric used in the MOS transistors to give a measure of the reliability of the specific structure tested. It is generally done either on the transistors themselves or on capacitor structures that have a gate oxide thickness equivalent to the MOS structure. Capacitors are generally used, and these are typically small, flat structures with the oxide grown on either the substrate or well while testing is done in accumulation, that is, for a P substrate capacitor, a negative bias is applied to the polysilicon plate.

EQUIPMENT

The testing equipment can be either purchased or built within the company. It is, however, specifically built for wear-out type testing. The equipment generally consists of a microprocessor, controlled mainframe containing the voltage supply, and current measuring units. The devices under test are placed in ovens on printed circuit boards. The ovens are capable of running at 300°C but the maximum use temperature is limited to 250°C due to the material constraints of the circuit boards.

TEST CONDITIONS

The test conditions used vary depending on the results required. For process monitors, generally one voltage and one temperature are used. For process characterization, a matrix of voltages, temperatures, and capacitor sizes is used. These allow the calculation of the voltage acceleration factor, γ (gamma), thermal activation energy, E_a, and the area dependency of the time to failure for the different area sizes, all of which are necessary to accurately predict product reliability.

The sample sizes chosen should be statistically significant and allow the determination of the intrinsic and extrinsic (if present) distributions.

DATA ANALYSIS/MODELING

The data generated from the testing is in the form of times to failure. This is analyzed using log-normal statistics to give the time to 50% cumulative failure for various test conditions to calculate the E_a and γ.

The collection of data sets such as these allows the calculation of the field acceleration and thermal activation energies. The oxide lifetime can be predicted using the appropriate model. The Linear E model is used by Analog Devices to predict the oxide reliability. The basic equation is shown in Equation 4, which has been shown to be the equation that adequately fits the data derived for Analog Devices processes. Care must be taken when analyzing the TDDB data that all capacitors used are the same size and that the distributions being analyzed to calculate the acceleration parameters are the intrinsic distributions.

$$TTF_{USE} = Exp.\ [-E_a/k\ (1/T_{TEST} - 1/T_{USE})] \times Exp.\ \gamma\ (V_{TEST} - V_{USE}) \times TTF_{TEST} \quad (4)$$

where:
TTF_{USE} and TTF_{TEST} are the use and test times, respectively, to failure (that is, 0.1% cumulative failure).
T_{USE} and T_{TEST} are the use and test temperatures, respectively (K).
E_a is the thermal activation energy (typically 0.7 eV).
k is Boltzmann's constant = 8.63 E-5 eV/K.
γ is the voltage acceleration factor (typically 2).
V_{TEST} and V_{USE} are the test and use voltages, respectively (V).

It is important to use the same size capacitor to calculate the field and thermal acceleration factors, because large area capacitors have a shorter failure time than the smaller ones, even though the field and thermal acceleration factors are similar. As a result, the lifetime for the larger transistors and capacitors is less than the expected lifetime for the smaller ones. Figure 15 shows the time to failure for different area capacitors under constant voltage stressing at 225°C; the difference in the T50% failure can be appreciated. Figure 16 shows the time to 50% failure vs. the inverse of the temperature on a SEMI log plot for several groups of capacitors. The thermal activation energy can be calculated from the slopes of the lines fitted to the data.

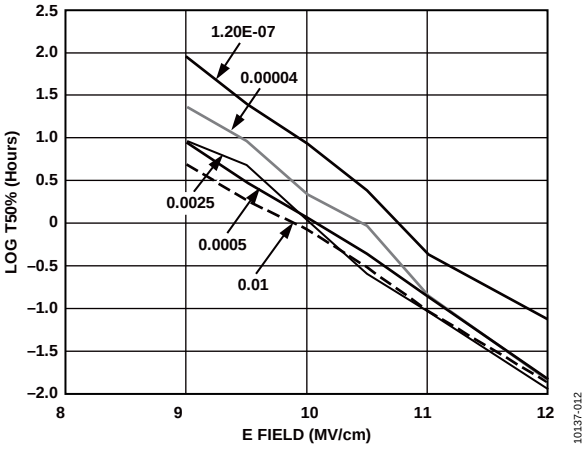

Figure 15. T50% Failure Time vs. Electric Field

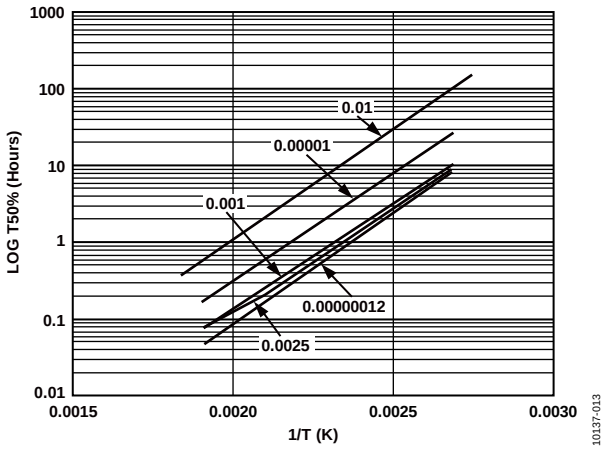

Figure 16. T50% Failure Time vs. (1/T(K))

The Linear E model is manipulated as shown in Equation 5 for calculating useful lifetimes from experiments.

$$TTF_{USE} = Exp\left[\frac{-Ea}{k}\left(\frac{1}{T_{TEST}} - \frac{1}{T_{USE}}\right)\right] \times Exp\,\gamma\left(V_{TEST} - V_{USE}\right) \times TTF_{TEST} \quad (5)$$

The TDDB analysis provides a means whereby the structures are tested under constant voltage and temperature, which can then be extrapolated back to user conditions (Equation 5). The test stress voltage is chosen close to the breakdown voltage and the test temperature is generally at 225°C. The user conditions vary depending on the maximum user voltage rating for the process/product as well as the temperature at which the product will be used.

The JEDEC specifications used in conjunction with TDDB testing are

- JP001.01: Foundry Process Qualification Guidelines
- JEP122: Failure Mechanisms and Models for Semiconductor Devices

ELECTROMIGRATION

Electromigration (EM) is the mass material transportation of metals through diffusion, under the driving force of an electron wind. Electromigration occurs when current flows in a metal interconnect, where an electron wind is generated, and the electron wind applies a force to aluminum atoms resulting in diffusion in the direction of electron flow. This movement of material results in voids or hillock growth, as shown in Figure 17, which eventually results in failure due to open circuit, shorting of adjacent tracks, or the change in line resistance.

The two forces that decide the drift of the ions are (1) the force from the static field on the thermally activated ion, which acts in the direction of the applied force, and (2) the force from the electron wind, which is the force applied by electrons colliding with thermally activated ions in the opposite direction of the applied field. This failure mode is escalated with the increase in temperature and the increase in current. The electron wind is the dominating force that causes ionic drift along diffusion paths, such as solid surfaces, grain boundaries, and interfaces. The failure modes associated with EM are mainly the creation of voids in the cathode or negative terminal, because ions upstream in terms of electron flow have a higher probability of occupying a vacancy than ions surrounding the vacancy. The electron flow also leads to a buildup of metal at the anode terminal leading to hillocks or extrusions, which can cause short circuits.

Although EM has been widely recognized as an IC failure mode for many years [49 – 54], concern has increased over the probability of its occurrence toward the end of useful life. This heightened concern coincides with the reduction of feature sizes into the submicron regime, with multiple levels of metallization. These technology trends result in increased interconnect current densities and device operating temperatures, both of which exacerbate EM. The complexity of assuring EM reliability is significant, requiring much more than the generation of design rules to limit current densities. Many aspects of the manufacturing process ranging from metal quality, dielectric processing, topography severity, and circuit density influence EM failure.

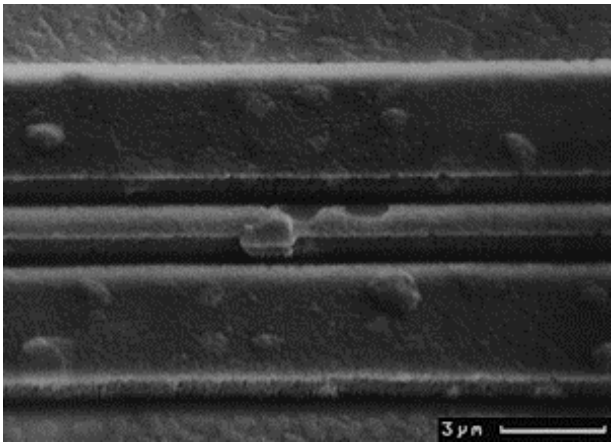

Figure 17. EM Failures

TESTING METHODOLOGY

Dedicated EM test structures are tested at accelerated test conditions for temperature (180°C to 225°C) and current densities (20 mA/µm^2 to 55 mA/µm^2). The time to failures recorded from these tests are translated to typical end-user conditions for temperature and current density. This translation of the accelerated test to end-user conditions is achieved using Black's equation (Equation 6).

$$Tf = A \times J^{-n} \times exp\ (E_a/kT) \quad (6)$$

where:
Tf is the time to failure (hours).
A is a process dependent parameter.
J is the current density (mA/µm^2).
n is the current density exponent.
E_a is the activation energy (eV).
k is Boltzmann's constant (eV/k).
T is the temperature (K).

The dedicated EM test structures consist of metal lines on flat and topography substrate with various widths designed per the ASTM F-1259 design rules. Via and contact chains are also used to determine the reliability of these structures.

PROCESS MONITOR RESULTS

Once the process is characterized, and finalized with design rules in place, a sample of material from dedicated, specifically designed test chips is tested on a monthly basis and the results are fed back to the wafer fabrication manufacturing groups. An example of typical results is plotted in Figure 18 showing data points representing monitor experiments all of which meet lifetime limit. The variation in the data is due to the population consisting of numerous types of EM structure. By using Black's equation to translate from the accelerated test conditions to the end-use conditions, control lines for the process are obtained for a process. Control lines are established by using the minimum time for 50% of the test sample to fail and the corresponding sigma (Σ) value, required to give <0.1% cumulative failure in 10 years at 125°C from the EM test conditions, as in Equation 7.

$$Tf\ (test50\%) = Exp.\ (93.08 \times \Sigma) \times (10\ Years\ (A_{JD} \times A_T) \quad (7)$$

A_{JD} and A_T are the current and temperature acceleration factors from use to test conditions; they are calculated in a similar fashion as those for the TDDB testing previously outlined. The sigma value is the dispersion of the distribution.

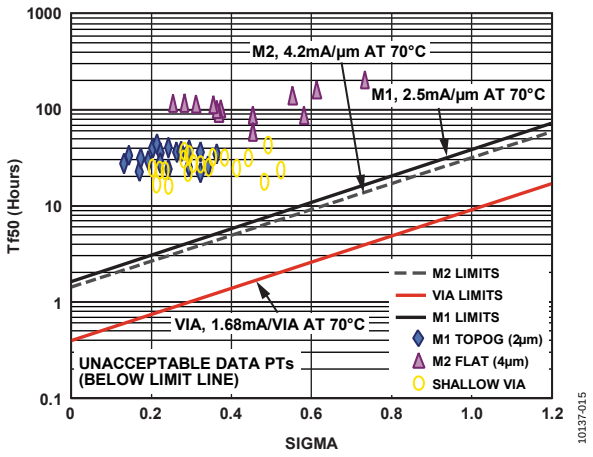

Figure 18. Selection of EM Monitor Results from a 0.6 µm Process

All units subjected to testing are analyzed on completion of the test to verify that the failures found are indeed true EM failures. Figure 18 indicates the position of the voids (gaps from which metal has migrated) and hillocks (areas where metal has been deposited) with respect to the current flow.

EM TESTING AND ANALYSIS

Relevant JEDEC standards and ASTM structures used are JESD61, JESD87, JESD33A, JESD37, JESD63, and ASTM: F1260-96 EIAJ-986.

Figure 19 shows the testing and analysis of data carried out for a typical EM experiment. Graph #1 shows a quick check of DUTs to confirm that they are the correct resistance. Graph #4 shows a TCR plot for calculating this value for each DUT. Graph #2 shows monitoring of resistance over time to a fail criteria of 20% increase in this example. Finally, Graph #3 shows a log-normal plot of four different experimental splits which is used to gather statistics to calculate EM lifetimes.

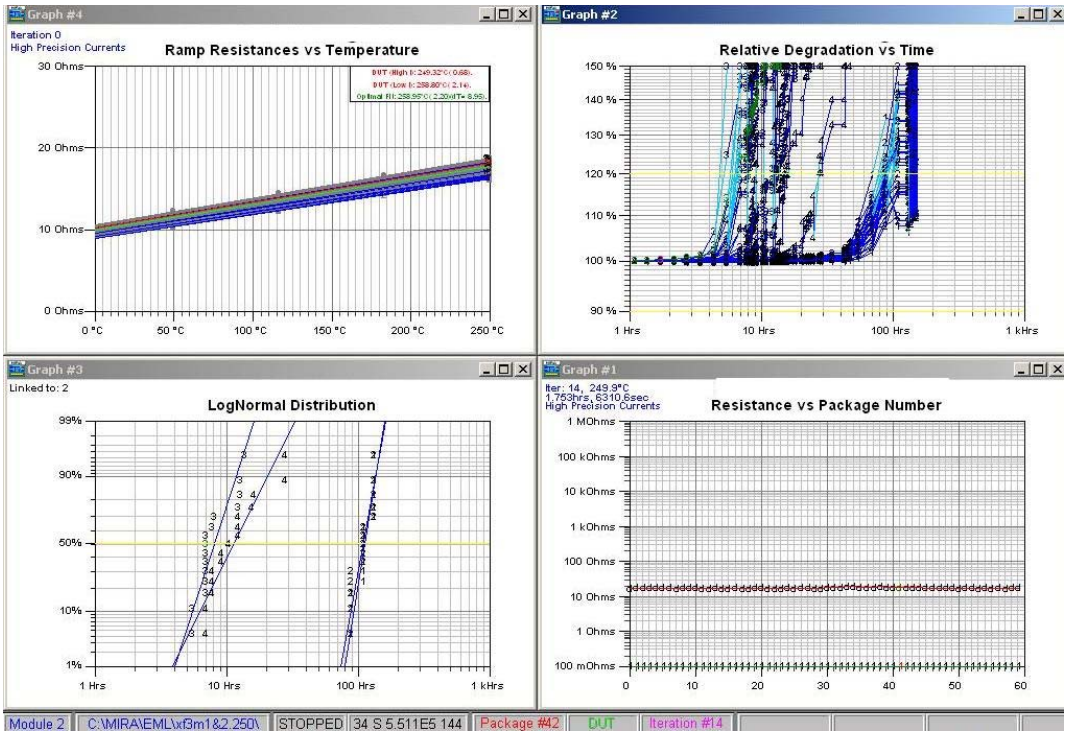

Figure 19. EM Testing and Analysis

The analysis method for EM assumes that linear regression analysis allows the calculation of EM model parameters. The method also assumes that MTTF data from EM experiments can be modeled by Black's equation.

For the activation energy (E_a) calculation, three EM experiments are conducted at three different temperatures with a constant current density. A plot of the three MTTF vs. 1/KT is a straight-line fit whose slope is the activation energy, as shown in the example in Figure 20.

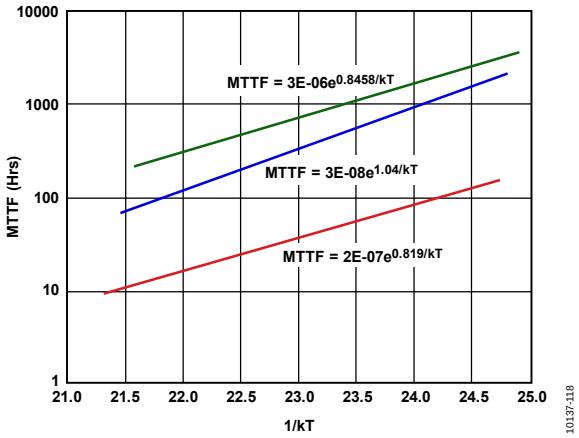

Figure 20. Activation Energy (E_a)

For the current exponent (n) calculation, three EM experiments are conducted at three different current densities with a constant temperature. A plot of the three MTTF vs. 1/J is a straight line whose slope is the current density exponent, as shown in Figure 21.

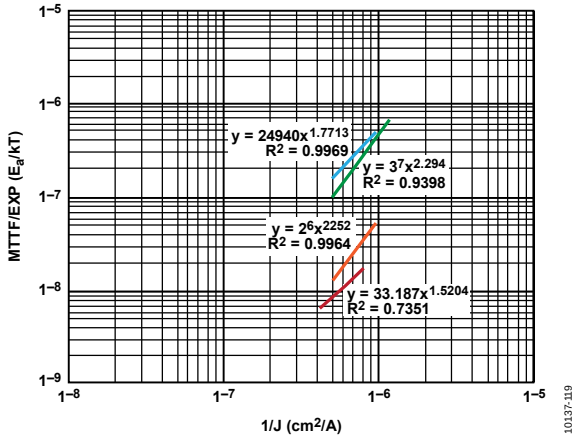

Figure 21. Current Exponent (n)

When all the parameters of Black's equation are determined and data is gathered for each metal level, contact, and via, then current density limits can be calculated vs. junction temperature (T_J) on a process-by-process basis.

MOS HOT CARRIER INJECTION

The effects of MOS hot carrier degradation [61 – 68] are now an important issue as device scaling has outpaced the reduction in supply voltages resulting in increased electric fields in the silicon and gate oxide. nMOS only is normally tested, because it shows far greater degradation than pMOS.

Hot carriers are generated in the channel by the large electric field in the drain region, as shown in Figure 22. This lateral electric field occurs as a result of high doping levels and shorter channel lengths. The hot carriers are created by electrons in the channel gaining energy from the field faster than they lose it to the lattice. As a result, they are no longer in thermal equilibrium with the lattice. Impact ionization of these high energy electrons causes the generation of electron/hole pairs. From these pairs, the holes can flow as substrate current and the electrons can, if they gain sufficient energy, surmount the energy barrier and tunnel into the oxide. These electrons become trapped in the oxide and create interface states. These interface states result in changes in parameters such as V_T, I_{DS}, and G_M (transconductance).

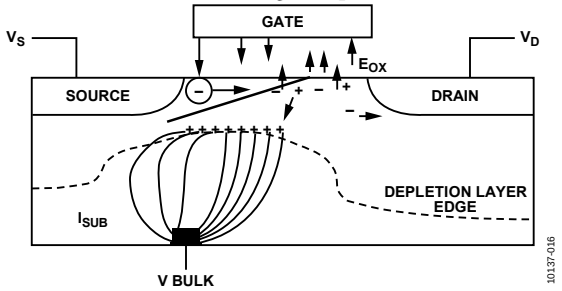

Figure 22. Hot Electron Injection

TEST METHOD

For hot carrier testing, nMOS nominal Leff devices are used with the minimum gate length for the process. The stress is applied as a dc bias at room temperature. Typically, the total sample size used is 24, with 8 devices at 3 different stress V_{DS} conditions (dependent on the process). The x stress voltages used are higher than the maximum user voltage and lower than the on-state breakdown voltage. V_{GS} is set to the maximum substrate current while VSS and VBS are set to 0 V. The fail criteria are a 10% shift in $G_{M(MAX)}$ (maximum transconductance).

LIFETIME PREDICTION

Lifetime predictions are made using the Berkeley model.

$$ttf \times I_{DS} = Cx^{-m} \quad (8)$$

where:
ttf is the time to 0.1% failure.
C is a process-dependent parameter obtained from Figure 23, y axis intercept.
x is I_{BS}/I_{DS}.
m indicates hole or electron injection, obtained from Figure 23, slope of line.

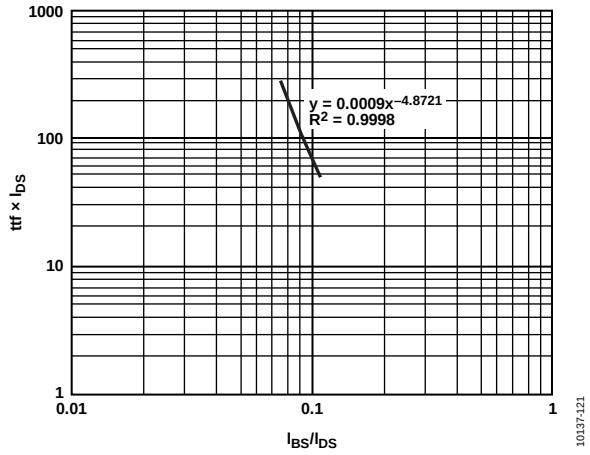

Figure 23. Typical Time to Failure vs.(I_{BS}/I_{DS}) Curve for Hot Carrier Injection

DATA ANALYSIS

The data from a typical nMOS hot carrier experiment is analyzed as follows:

- The time to 10% degradation for each device is plotted on a cumulative probability plot, as shown in Figure 24. The extrapolated time to 0.1% failure is obtained from this graph for each stress level.
- T 0.1% × I_{DS} vs. I_{BS}/I_{DS} is plotted on a log/log scale for each stress level (see Figure 23). A trend line is fitted to the data using a power law, and the resulting equation represents the model used for lifetime prediction. The m factor from the Berkley equation is generally known for mature process, for example, typically 4.2 for 0.6 μm and 3 for 0.35 μm nodes.
- Using the equation from the previous step, the lifetime at worst-case operating conditions can be calculated. This results in a dc lifetime. An ac lifetime value can be calculated by using the following conversion factor:

$$t_{AC} = t_{DC} \times 170/2.2$$

where 170 is a dc-to-ac conversion factor (developed by Intel) and 2.2 is a room temperature to −55°C conversion factor. There is no thermal acceleration factor (E_a) in the equation; the room temperature conversion factor is used because the failure mechanism is more pronounced at cold temperatures as a result of lattice stability. Typical lifetime criteria is 10 years ac and 0.2 years dc.

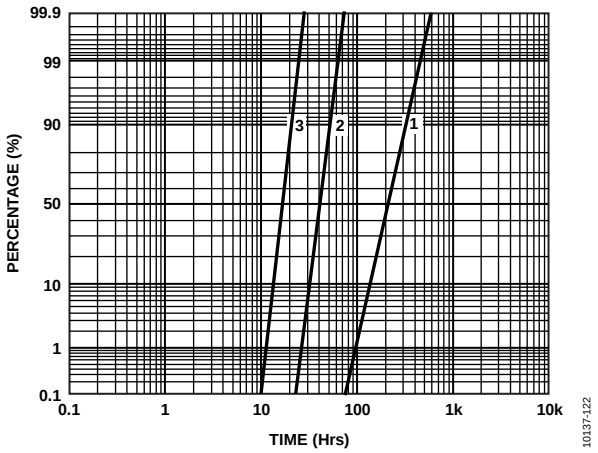

Figure 24. Cumulative Probability for Hot Carrier Degradation

The JEDEC specifications used for hot carrier testing are JESD28-A, *A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation under DC Stress* and JESD28-1, *N-Channel MOSFET Hot Carrier Data Analysis*.

DMOS HOT CARRIER INJECTION

This section refers to the characterization and HC stress testing of double-diffused metal oxide semiconductor (DMOS) devices, as shown in Figure 25 [69]. While such transistors are rated up to ±10%, these ratings only apply to V_{DS}. The thickness of the gate oxide matches that of the 5 V MOS devices and, as such, V_{GS} is only rated to 5 V ±10%. While the principles of standard HC testing as described previously still apply to DMOS devices, there are additional stress and experimental setup conditions that must be included to properly characterize DMOS devices.

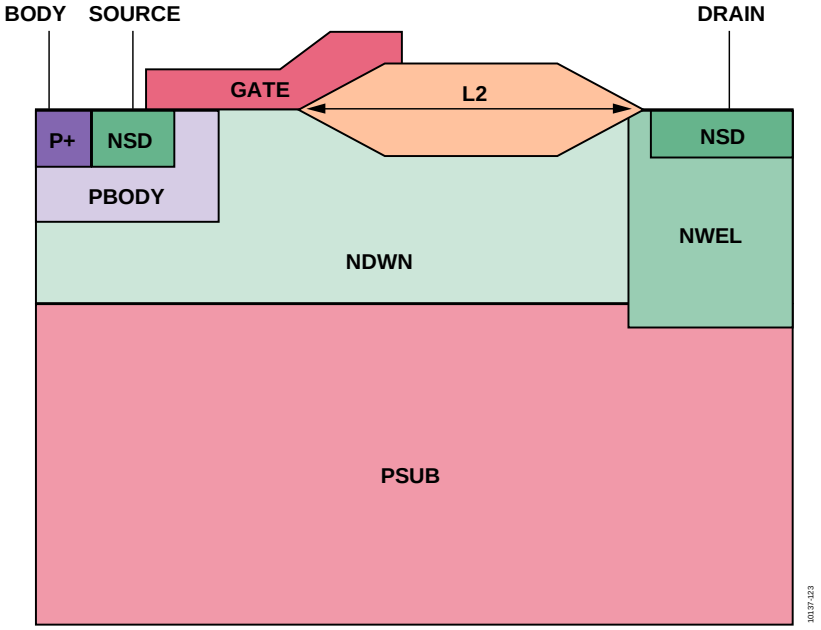

Figure 25. n DMOS Device

DMOS CHARACTERIZATION

As with standard MOS structures, an initial device characterization is required to determine the stress and use conditions. To determine these conditions, I_D/V_G and I_{SUB}/V_G curves must first be generated for the device under characterization.

One significant difference between the device characteristics of MOS and DMOS devices is the subsequent increase in substrate current for V_{GS} values greater than those corresponding to I_{SUBMAX}. An example of this is shown in Figure 26 for a 40 V DMOS device, which shows I_{BS} plotted as a function of V_{GS} for various values of V_{DS}. The second peak in current at higher V_{GS} values is termed $I_{SUBKICK}$ to distinguish it from $I_{SUBKIRK}$ that is generally associated with bipolar devices. As shown, $I_{SUBKICK}$ is greater than I_{SUBMAX} for higher values of V_{DS}. Considering that substrate current is generally used as an indicator of hot carrier activity, it makes sense to monitor hot carrier degradation not only under I_{SUBMAX} conditions, but also under $I_{SUBKICK}$ conditions.

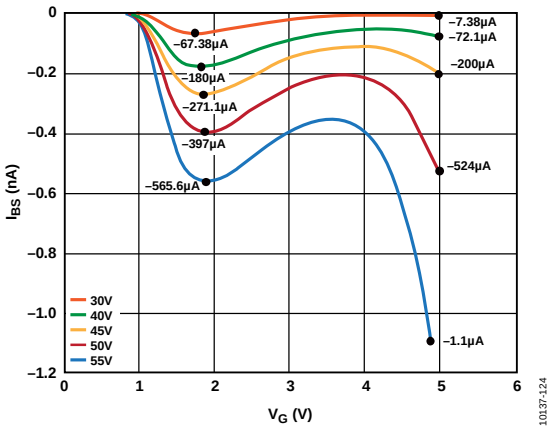

Figure 26. 40 V HVDMOS I_{BS}/V_{GS} Characteristics Plotted as a Function of V_{DS}

Note that while stressing under $I_{SUBKICK}$ conditions the device power dissipation is greater than that under I_{SUBMAX} conditions particularly for the HVDMOS devices. This can result in significant device self-heating, which can mask true hot carrier degradation. An example of this is shown in Figure 27.

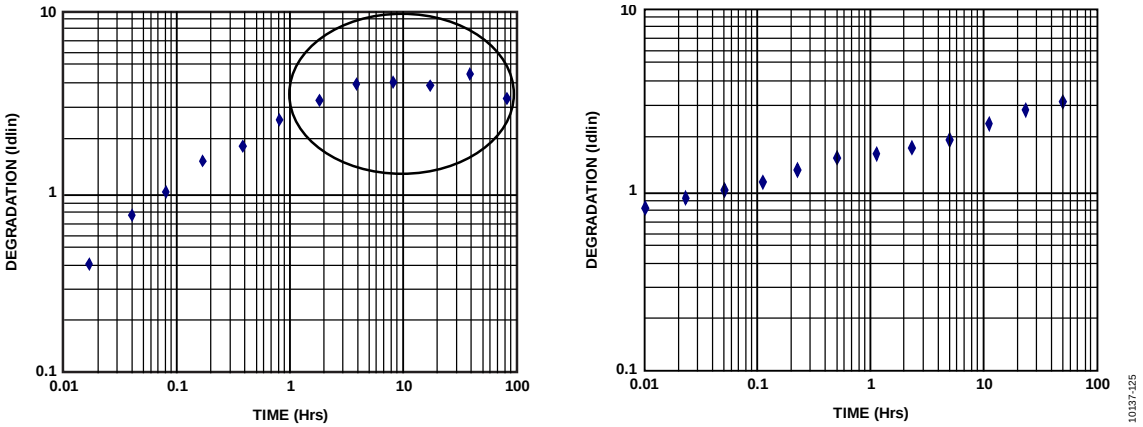

Figure 27. Effect of 1-Hour Recovery Period Post Stressing

RULE OF THUMB

For all DMOS hot carrier stress testing (in particular HVDMOS), a 1 hour recovery period after each interim stress period is required before the device characteristics are monitored. This recovery period is required to allow the device to cool down such that the device parametrics can be accurately measured and compared to their initial T0 values and a true percentage degradation obtained.

BIPOLAR HOT CARRIERS

Description

A major reliability issue for high-performance bipolar transistors is the reduction of forward current gain (hfe) resulting from hot carrier (HC) generation during reverse bias operation of the emitter-base pn junction [70]. Bipolar HC-induced degradation is strongly dependent on device size. The overall objective is to develop reliability-driven rules that can be used to reduce HC degradation and improve transistor reliability.

As vertical and lateral dimensions are scaled down to increase device performance, the doping levels must be increased to maintain an optimal performance. Because of the high doping densities of the emitter and the base, a very large electric field exists along the periphery of the emitter. When the emitter-base junction is reverse-biased, the large electric field can create hot carriers that degrade the spacer oxide around the emitter edge, causing an increase in the forward-bias recombination current. The collector current remains the same. The result is a decrease in the current gain due to an increase in I_B, which, in turn, can limit the performance of the bipolar circuit.

TEST METHOD

Two methods of accelerating the HC-induced degradation are available: reverse e-b voltage stressing and reverse e-b current stressing. Constant current stressing is used at Analog Devices. This method provides more consistent results than the constant voltage stressing because the reverse current is a more sensitive function of the electric field than the reverse voltage.

The test system is used to force a range of currents (normally 3), depending on the process, to stress the devices. Three measurements are taken per decade of stress time starting at 0.01 hours. The fail criterion is the time to degrade hfe by 10%.

BIPOLAR LIFETIME CALCULATION

A cumulative probability plot of the times to 10% degradation of hfe is drawn up for each current and the time to T 0.1% failure determined.

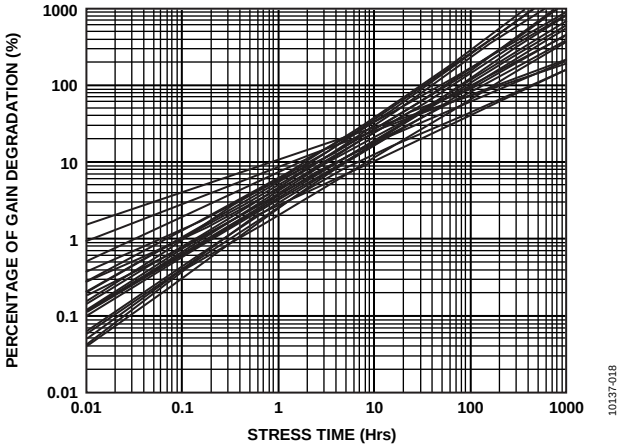

Figure 28. Graph of % Gain Degradation vs. Stress Time

When bipolar transistors are stressed, the gain, or hfe, of the transistor shifts, as shown in Figure 28. If the gain shifts appreciably during the lifetime of the transistor, it no longer operates as specified causing circuit failure and, as a result, becomes a long-term reliability hazard. The gain (hfe) is simply the ratio of I_C and I_B. These parameters vary with V_{BE} (Gummel plot) and, as a result, the gain varies with I_C as shown in Figure 29 and Figure 30. In Figure 29, the Gummel plot and the I_C values are the upper curve while the I_B values are the lower one. The gain also varies with I_C as shown in Figure 30.

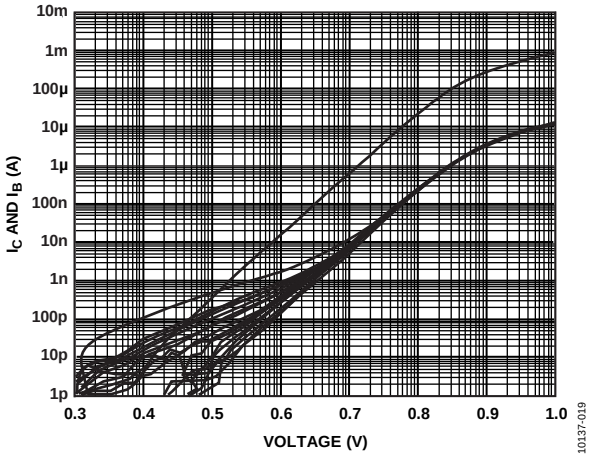

Figure 29. Gummel Plot I_C (Upper Curve) and I_B (Lower Curve) vs. Voltage

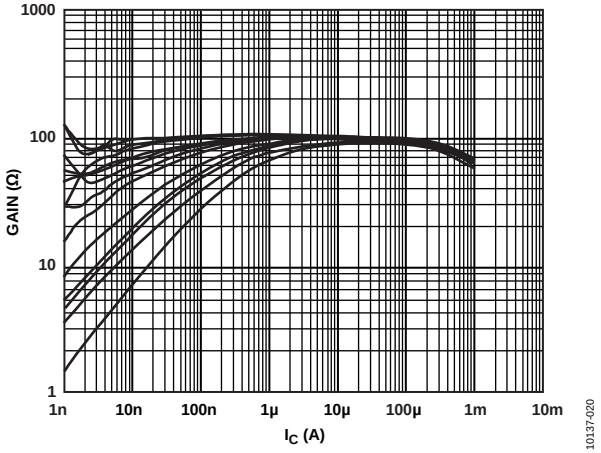

Figure 30. Plot of Gain vs. I_C

When the degradation in gain is achieved, the times for 10% degradation of each device under test are calculated. These are plotted as shown in Figure 31 and the time for 0.1% cumulative failure for each sample population is extrapolated assuming a log normal distribution.

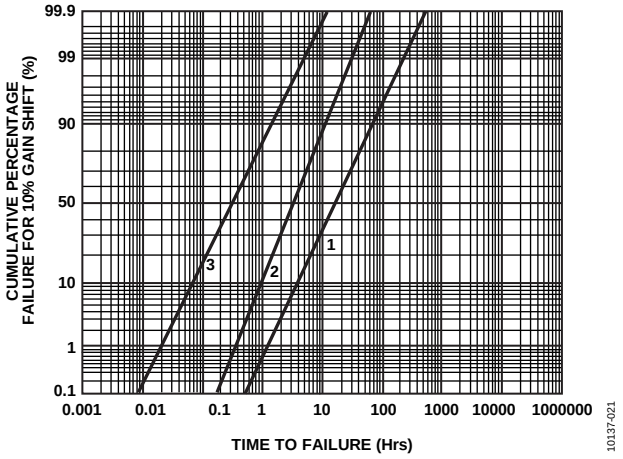

Figure 31. Cumulative % Failure for 10% Gain Shift vs. Time to Failure (Hrs.)

When the time to 0.1% failure is calculated for each stress condition, these values are plotted against the reverse I_E (nA) as in Figure 32.

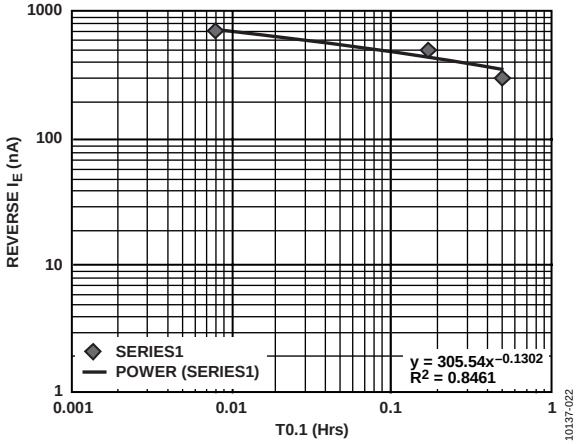

Figure 32. Lifetime vs. Reverse Bias I_E

The time to failure at use voltage is calculated for a specific I_E that can be translated into a max reverse V_{BE} voltage for the process using a reverse I_E vs. reverse V_{BE} curve. This measurement is made on virgin devices, allowing the equivalent current of the specified voltage to be calculated.

STRESS MIGRATION

As metal lines become thinner (that is, <2 μm), failures can occur due to high temperature and heat cycling. The metal interconnect lines can go open circuit as a result of stress. This is called stress migration or stress voiding [71]. In this failure mechanism, unlike EM and corrosion, no bias is applied. The stress migration is generated by a thermal mismatch between the aluminum interconnects and the passivation film or the interlayer insulating film. The aluminum atoms migrate to relieve this stress. The aluminum atoms can migrate from the boundary to continue relieving the stress, thus widening the voids at the boundary and eventually creating an open circuit. If the line does not go completely open circuit, this migration reduces the effective width of the metal lines and increases the probability of EM failures occurring. The resistance to stress migration is increased by the use of aluminum alloys, and TiN, TiW, and Ti in the metal layer structure.

The stress migration test involves baking at constant temperature/ss (isothermal) while monitoring resistance change. The analysis involves generation of activation energies to a specific fail criteria and subsequent lifetime calculation.

PROCESS BACKGROUND THEORY

Stress-induced voiding, which can occur during processing, storage, and use, is a reliability concern for microelectronics chips that, in Analog Devices' case, use Al-based alloys for on-chip wiring. Susceptible metallizations can grow voids in lines and under or over W studs. For simple metallizations, like AlSi, such voids can cause catastrophic failure. For metallizations of Al alloys layered with a refractory shunt layer, voids cause resistance increases and interact with other failure mechanisms, such as EM and mechanical failure, to shorten lifetime.

STRESS MIGRATION TESTING AND ANALYSIS

The model used for stress migration is the standard Arrhenius model for temperature acceleration, as shown in Equation 9.

$$MTTF = ExpE_a/kT \quad (9)$$

Void volume equations and integration with the Arrhenius model are available in the stress migration JEDEC standard JEP139, *Constant Temperature Aging to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding.*

The test structures used are narrow meander structures, preferably Met 1 (higher stress), with the line widths being 2 µm or wider, because there is negligible stress voiding for <1 µm width since it is a bamboo structure. The recommend stress conditions are several different temperature splits from 150°C to 250°C for Al alloys. The graphs used to measure data for analysis are absolute and relative delta R, linked to Lognormal for T0.1, T50, and sigma for extrapolation to useful life conditions using the Arrhenius model.

NBTI

Negative bias temperature instability (NBTI) is a degradation mechanism that manifests itself in pMOS devices. NBTI reduces the drive current in the pMOS, as shown in Figure 33. However, this degradation is only seen when the pMOS is powered up and recovers almost immediately when power is removed making it difficult to capture or measure.

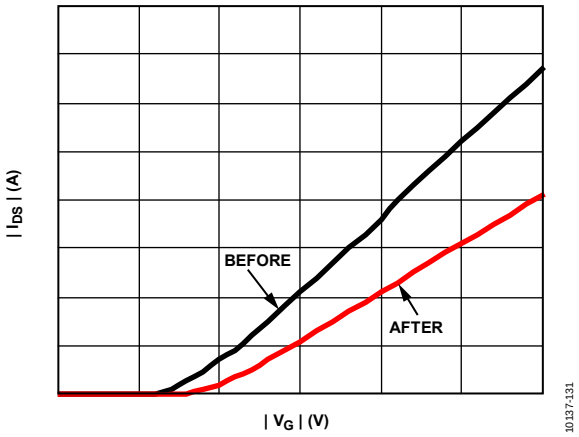

Figure 33. NBTI Degradation Mechanism

Figure 34 shows a cross section of a pMOS device in a mode where NBTI can occur, where the source and drain are tied to the supply and the gate is at ground. Positive charge collects at the SiO2 silicon interface resulting in an offset in V_T and a reduction in drive current when the device is switched on.

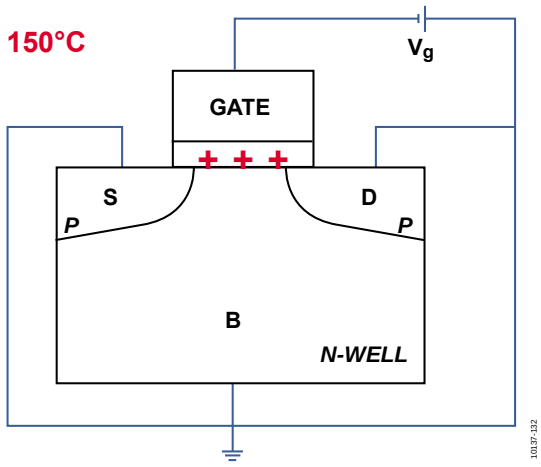

Figure 34. NBTI Bias Condition for pMOS

CIRCUIT IMPACT

An example of how NBTI can impact at the circuit level is shown for an input stage of an amplifier in Figure 35. In power-down mode, the M2 and M3 gates are biased at a high ambient temperature. With asymmetric operation there are different input signals, therefore, the operation of M2 and M3 differs and the ambient temperature is high, which also means the junction temperature is high. The result of this is an I/P VOFFSET shift.

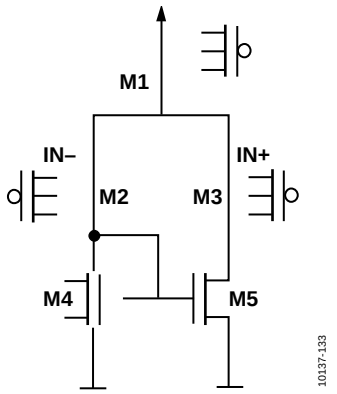

Figure 35. Circuit Impact

WHY NOW?

Why have NBTI failures become more likely? The answer is the increasing shrinkage of process geometries resulting in significant increases in electric field as shown in Figure 36 [72].

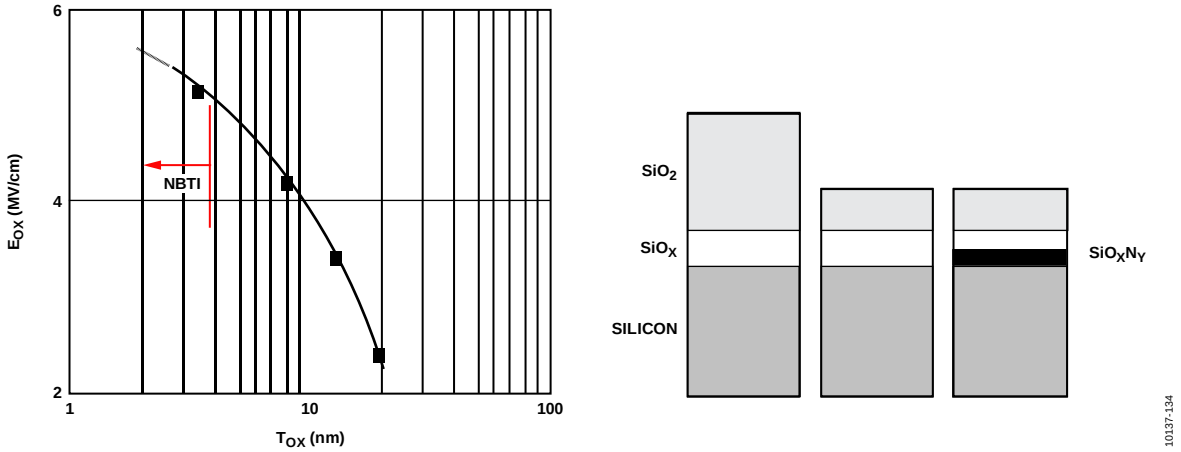

Figure 36. Shrinking Geometries and Increasing E-Fields

The shrinking geometries also means a reduction in gate oxide thickness and a greater sensitivity in MOSFETs while the expectations of operation remain high. The main target from a process technology point of view to reduce the impact of NBTI is the reduction of Boron penetration in the active area region, which can result in damage at the SiO2 silicon interface leading to potential for NBTI.

WHAT IS THE NBTI MECHANISM?

There are numerous theories behind explaining the NBTI mechanism according to the literature available. The following are some of the explanations given:

- Electron tunneling from SiO2 to Si
- Strained bond reactions
- Oxygen vacancy formation
- Electrochemical reactions
- Hole tunneling into the SiO2
- Hole trapping in the oxide
- Hole trapping on intrinsic hole traps

In summary, however, the generally accepted definition of the NBTI mechanism is the diffusion reaction chemistry between hydrogenated trivalently bonded silicon defects and a by-product diffusing species. In terms of the process impact, the penetration of boron implantation can result in the diffusion of boron from the gate to the channel. Nitrogen is inherently incorporated into the gate oxide during the process where it takes up the form of SiON in between the Si/SiO2 interface. Fluorine is also present since it is used to carry the boron during source-drain implantation in the form of BF3. The SiOxNy interface can result in positive charge traps, which cause the NBTI mechanism to occur. Increasing the SiON layer with increased nitrogen during processing means a reduction in boron

penetration, but an increased NBTI. Increasing fluorine through increased BF2 reduced NBTI but results in increased boron penetration into the channel, which can detrimentally affect device characteristics.

Deep submicron processes used by Analog Devices are all foundry based while process engineering for NBTI is a complex activity. The key areas of interest with respect to NBTI are:

- Surface vs. buried channel pMOS
- Gate dielectric material
- Gate dielectric defect reduction
- Hydrogen vs. deuterium anneal

RELIABILITY STRESS TEST METHOD

The NBTI stress method recommended by Analog Devices is the JEDEC Standard, JESD90. This involves a biased temperature stress with a high E_{OX} (MV/cm) and temperature stress (100° to 200°C). The V_{TH} measurement also needs to be defined whether it is an extrapolated V_{TH} or an empirical V_{TH}, that is, at I_D = 200 µA, while the fail criteria is defined as a relative percentage change or a delta change in a MOSFET parameter. The flow chart in Figure 37 shows the test flow as defined by JEDEC.

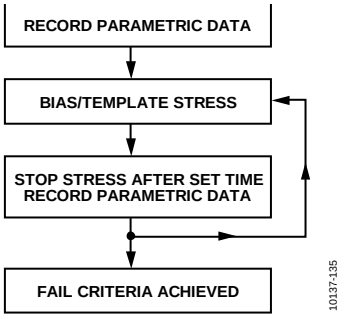

Figure 37. JEDEC NBTI Flow Chart

The reliability data shows a time dependence. The literature on NBTI supports a delta V_{TH} proportional to time to the power of 0.25, that is, delta V_{TH} α time 0.25, and evaluations of a 0.18 µm process showed good correlation to this as shown in Figure 38.

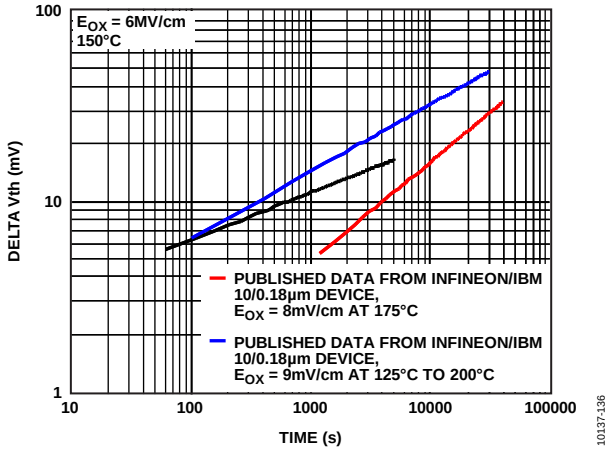

Figure 38. Delta V_{TH} Proportional to Time

The reliability data also shows an E_{OX} dependence. The literature supports D_{VTH} α V_{OX} or $E_{OX} = V_{OX}/t_{OX}$. Data from a 0.18 µm process shows this as in Figure 39.

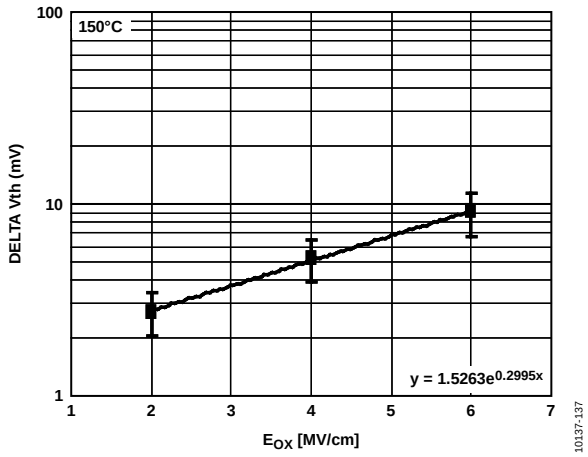

Figure 39. D_{VTH} α V_{OX}

The reliability data also suggests temperature dependence. The literature supports lifetimes where t α 1/T similar to the Arrhenius equation and data from a 0.25 µm process technology shows a good correlation here also, as shown in Figure 40.

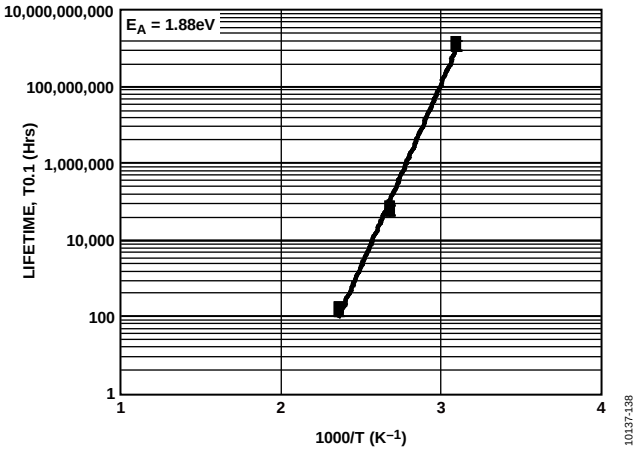

Figure 40. Lifetime vs. 1/T

In terms of recovery or relaxation of the mechanism, NBTI degradation is both permanent and recoverable in that the degradation does not recover when the bias is applied to the pMOS, but disappears when bias is removed, that is, it is difficult to measure afterwards. There are multiple theories on the recovery mechanism, and charge pumping techniques are required for clarification. An example is shown in Figure 41 [73].

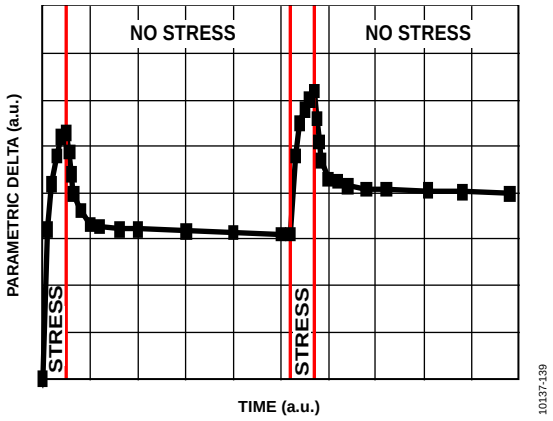

Figure 41. Permanent and Recoverable Degradation

Due to the recovery phenomenon, dc NBTI is unduly pessimistic because it is dependent on a stress-relaxation phase symmetry, where there is ~40% recovery and an order of magnitude lifetime improvement. There is also a frequency dependence, depending on whether it is a unipolar or a bipolar Vg stress, while the duty factor also contributes. Overall, dc to ac provides a significant reduction in NBTI, while the frequency and duty factor demonstrate variable grades of sensitivity, very specific to the technology reported.

MANAGING NBTI AT DEVICE LEVEL

Key features of NBTI are voltage acceleration (E_{OX}) and temperature acceleration (Arrhenius). The device level test method is based on JESD90.

THE FUTURE FOR BIAS TEMPERATURE STRESS

Future work on NBTI industry wide includes charge pumping based resolution of the mechanism, a focus on generic dc/ac gain, product level working examples, and gate oxide technology developments, such as Hafnium based High-K dielectrics (HfO2) while both pMOS NBTI and nMOS PBTI (at even lower geometries) are being investigated.

In summary, NBTI is an anode-hole/reaction-diffusion mechanism that differs from other mechanisms, such as HCI, and is the result of the impact of process features. The reliability test for NBTI has a time dependence and is accelerated through temperature and voltage. At the product level, it occurs in analog circuitry, has a recovery mechanism, and is dependent on dc/ac conditions.

NBTI is a relatively new reliability phenomenon. While NBTI is not a showstopper, it is important to gain an ability to understand and to manage NBTI. At Analog Devices, NBTI is irrelevant to many processes where the gate dielectric is quite thick, while it is monitored to the latest industry standards for leading edge technologies.

HIGH VOLTAGE ENDURANCE

HV endurance is Analog Devices terminology for stress testing of isolation technology on Analog Devices' patented *i*Coupler® processes. High voltage endurance is the maximum voltage that can be applied continuously between the input and the output pins of an isolator (organic dielectric) without causing any damage. Constant voltage, temperature, and humidity are used to accelerate the dielectric failure, because the dielectric only allows a finite amount of charge to pass through it before the breakdown. The goal of HV endurance testing is to determine when the leakage current starts flowing through the dielectric and thus determine the lifetime and quality of the insulation. This section outlines testing capabilities and demonstrates the process of analyzing experimental results. It also includes details on theory of life model for electrical insulation materials.

BACKGROUND THEORY

This is a review of high voltage (HV) lifetime characteristics and how it differs from other insulation materials, such as SiO2, that may also be used for high voltage insulation [74]. Using demonstrated models and empirical data, the HV lifetime of *i*Coupler products is much greater than 10 years at working voltages of up to 400 V rms.

The dominant breakdown mechanism is through charge injections as a result of the direct electron impact from the electrodes to the dielectric surface regions. The breakdown process begins as charges are injected into the dielectric surface under HV ac conditions. The charges can become trapped in some local trapping sites at the surface. When trapped, energy is released, which causes local mechanical tension because of stored electrostatic energy. Through a quantum activation process, this tension eventually causes local free volumes, voids, or microcracks, which act as more local trapping sites. If the HV ac remains long enough, this process leads to the continued degradation of the insulation and eventually electrical punch through.

Through thermodynamic analysis, the lifetime, L, can be expressed as

$$L \approx \frac{e^{-(e-e_t)n}}{(E-E_t)^m} \tag{10}$$

where:
E_t is the threshold field where no charge injection will happen.
m and n are scaling constants.

The HV ac endurance data of these devices was analyzed according to the procedure specified by ANSI/IEEE Std. 930-1987, the *IEEE Guide for the Statistical Analysis of Electrical Insulation Voltage Endurance Data*, and is observed to follow

$$L \approx e^{V-N} \tag{11}$$

This phenomenological fit was used to obtain worst-case lifetime because it assumes no threshold field as specified by the thermodynamic model. The duration of the HV test becomes prohibitively long if we try to measure the threshold field. As shown in Figure 42, Equation 10 (green curve) fits well with the data (black circles), and Equation 11 (red curve) tends to predict much longer lifetime at low voltages. The Arrhenius equation $L \sim e^V$ (black curve) followed by other dielectric material, such as oxide, clearly cannot fit the data.

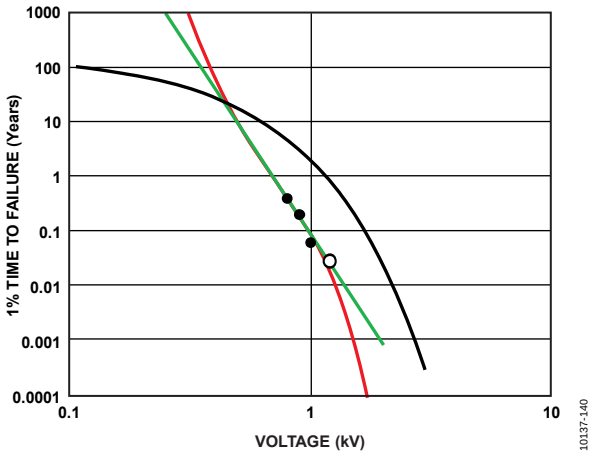

Figure 42. HV Lifetime Characteristic for Isolator Devices

It was also observed that the lifetime of isolator devices under dc or unipolar ac is much longer compared to that under bipolar ac; it is at least two orders of magnitude higher. For unipolar waveforms, the trapped charges tend to form an internal field barrier region around the electrodes that prevents further injection of charge into the polyimide as shown in Figure 43. With a bipolar ac waveform, the reverse field prevent formation of this steady field barrier, and the trapped regions keep progressing into the polyimide and eventually lead to the electrical breakdown. SiO2, on the other hand, tends to give worse lifetime for dc or unipolar ac.

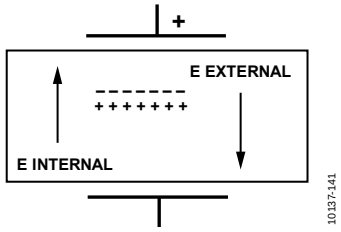

Figure 43. Field Barrier Region with Zero Net E-Field

This lifetime is based on worst-case bipolar ac waveforms. HV lifetime is even greater for unipolar ac or dc waveforms. Note that the models described here relate to an organic insulation and have no bearing on isolators that use SiO2 insulators as the primary means for isolation. Likewise, models that predict the HV lifetime of SiO2 based digital isolators have no bearing on polyimide-based isolation systems.

DATA ANALYSIS

A profile of typical dielectric breakdown during HV endurance testing is shown in Figure 44.

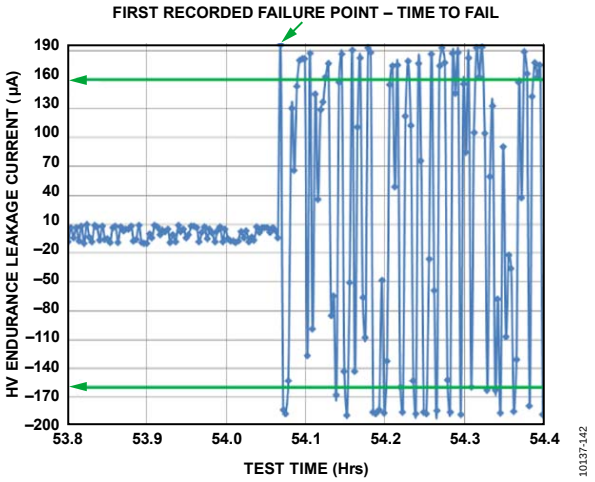

Figure 44. HV Endurance Profile

Figure 45 shows a Weibull plot of HV endurance test results for a particular isolator process at +25°C and 40%RH. The parallel fit lines suggest the same mechanism for each stress.

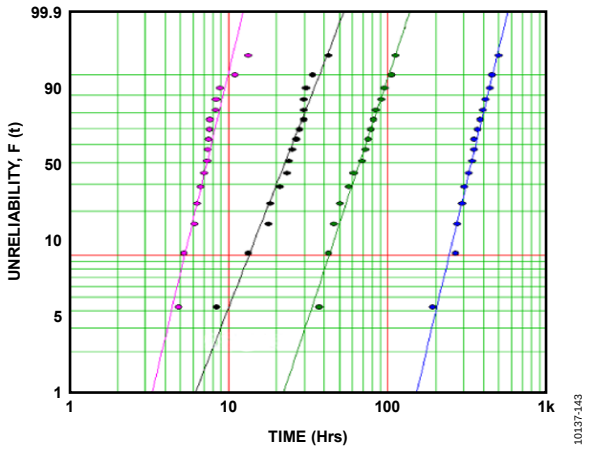

Figure 45. Weibull Plot of HV Endurance Experiment

Figure 46 shows an example of a safe operating area (SOA) plot for a particular isolator process based on T50% TTF and the use voltage.

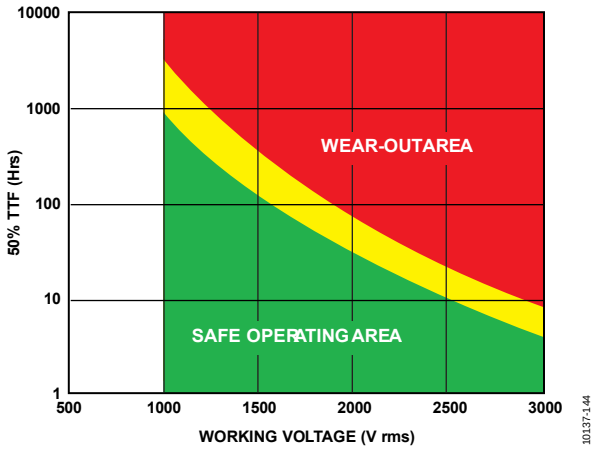

Figure 46. Safe Operating Area (SOA)

The section on high voltage endurance provides in-depth information and analysis of isolators with organic dielectrics and provides details on testing set-up, bias conditions, equipment configuration and analysis of tests.

DETAILS ON BUILDING IN RELIABILITY

The relationship between yield quality and reliability is the fundamental cornerstone of the building in reliability methodology [20, 22, 25, 30 – 32, 75 – 81]. It assumes that certain fundamental killer failure mechanisms can be traced back through the process, and that indicators of poor reliability due to process issues can be found at the very early stages of manufacture. Therefore, by knowing the reliability indicators for particular failure mechanisms, the occurrence of such failure mechanisms can be limited in the field either by screening them out in production or instigating redesign procedures or process modifications. When issues critical to field reliability and performance are identified, a process change or product redesign may be required. Since this can be a lengthy process, interim screening procedures must be implemented to allow the continued supply of high quality reliable products into the field.

The definitions used for yield, quality, and reliability are

- Yield: the proportion of devices operating on a manufacturer's product before any burn-in or screening has occurred (for example, first test, wafer sort, wafer acceptance test)
- Quality: measured by the proportion of components that fall out in a short burn-in (for example, 48 or 168 hours), and may be measured in a PPM fashion.
- Reliability: measured by the number of components that fail during life test stress testing, usually expressed as an MTTF.

Wafer sort and acceptance testing relate to yield; burn-in relates to quality; and life test relates to reliability. As the conclusive issue, field failure is defined as any failure that occurs once a product has left the manufacturing site and been returned for failure analysis, that is, reliability.

During an early life failure rate (ELF) evaluation of product from a specific process, a variation in the quality of the product was observed and analysis of the rejects indicated the failure mechanism was the same in all instances. The failure mechanism was a gate oxide rupture on a polysilicon to p+ channel stop capacitor, manifested by a high IDD at wafer sort (probe). The data at the various yield stages was

analyzed and it was found that there was a positive correlation between the yield, quality, and reliability of the product for this particular failure mechanism. The data from the field returns at the time also indicated that this was indeed the major source of failure in the field. Figure 47 indicates the correlation between the burn-in quality and the IDD as measured at wafer sort.

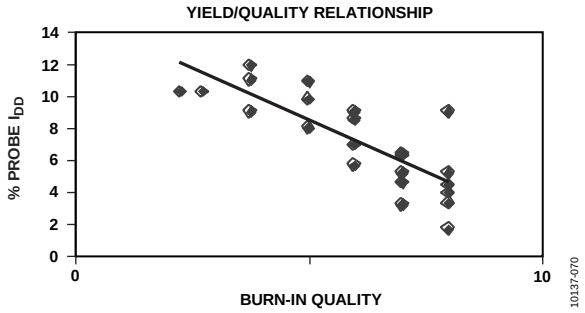

Figure 47. Yield vs. Burn-In Quality

For this particular failure mechanism, the graph illustrates that lots with high probe IDD failure rate had a lower quality as measured by 48 hours burn-in than those with low percentage fallout for IDD. This correlation also held true when the quality results from the burn-in were compared with reliability of the lots as measured through life tests, as shown in Figure 48. As expected, lots with a higher burn-in quality have a low failure rate but those with a high failure rate have a low burn-in quality.

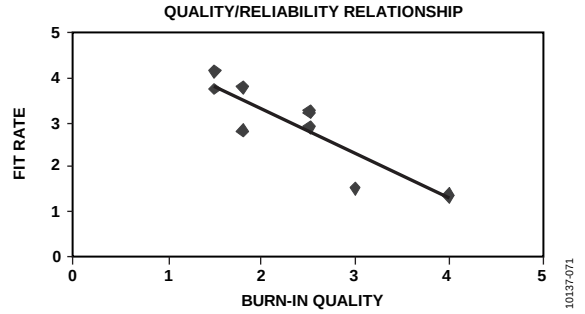

Figure 48. Relationship Between Quality and Reliability

The final relationship shown for this particular failure mechanism is between yield and reliability measured in FITs. This relationship is shown in Figure 49, which shows that the higher failure rate corresponds to a higher value of IDD rejects at probe or wafer sort.

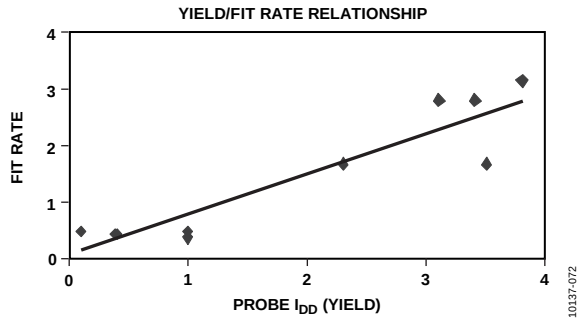

Figure 49. Reliability vs. Yield

The reliability aspect of this data has been augmented by the analysis of the field performance data for the product. Shown in Figure 50, the data indicates that the major customer return for this failure mechanism is gate oxide rupture on a polysilicon to p+ channel stop structure.

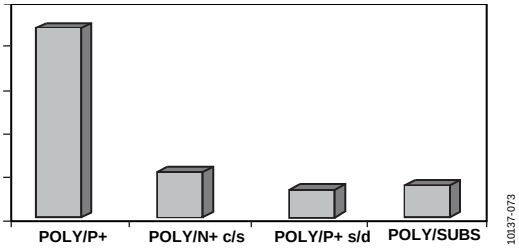

Figure 50. Customer Return Data

The correlations indicate the strong relationship between yield, quality, and reliability. The generation of such data indicates the possibility of screening out potentially defective product and improving customer reliability while embarking on more permanent solutions.

As defined previously, defect density correlation to the quality of the product indicates that the quality and reliability can be related directly back into the wafer fabrication process. Figure 51 and Figure 52 indicate the relationship between the infant mortality (ppm) quality of the process vs. the defect density recorded in wafer fabrication based on the number of reject die found at probe (wafer sort). Both figures indicate that the higher the IME PPM figure, the higher the figure (defect density times area) showing the relationship between IME and defect density.

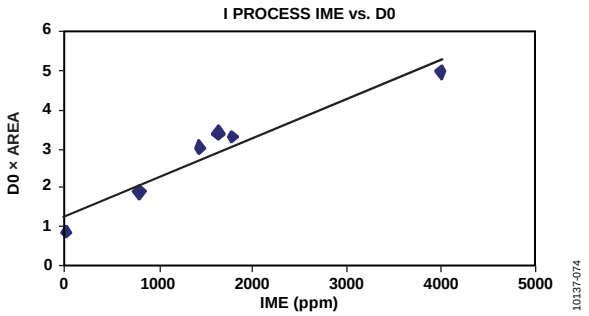

Figure 51. Infant Mortality Rate (PPM) Related to Defect Density (D0) and Die Area

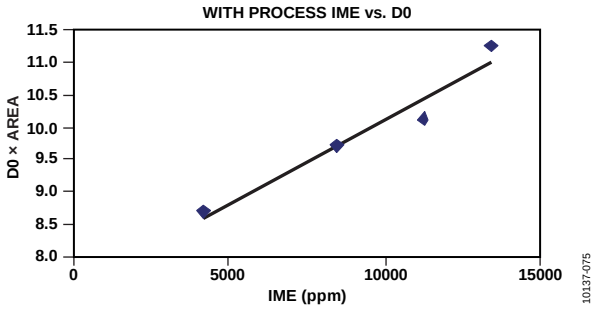

Figure 52. Infant Mortality Rate (PPM) Related to Defect Density (D0) and Die Area

From this, it is logical to assume that if the yield, quality, and reliability parameters outlined previously are related, the quality control indices in wafer fabrication are all controllers and indicators of reliability. The use of experimental design and the validation of the entire building in reliability philosophy have led to a fundamental adoption of this concept for all reliability projects in Analog Devices, as exemplified by the example described in the next paragraph.

During the development and introduction to manufacture of a new process, an Analog Devices wafer fabrication facility adopted a building in reliability approach. The process that was in development was a 0.6 µm dual polysilicon, dual metal process with a 150 nm gate dielectric. As part of the integrated reliability process development, cross-functional teams were established among all concerned groups to understand the reliability characteristics. Also involved was defining the reliability measurement methods, the structures and targets to be used, as well as discussing and evaluating the critical in-line controls to meet the targets and the final reliability qualification. The approach required teamwork and implementation of TQM concepts in partnership with reliability, manufacturing, and development.

The methodology employed is shown in Figure 53, where the goal was the successful qualification of the process.

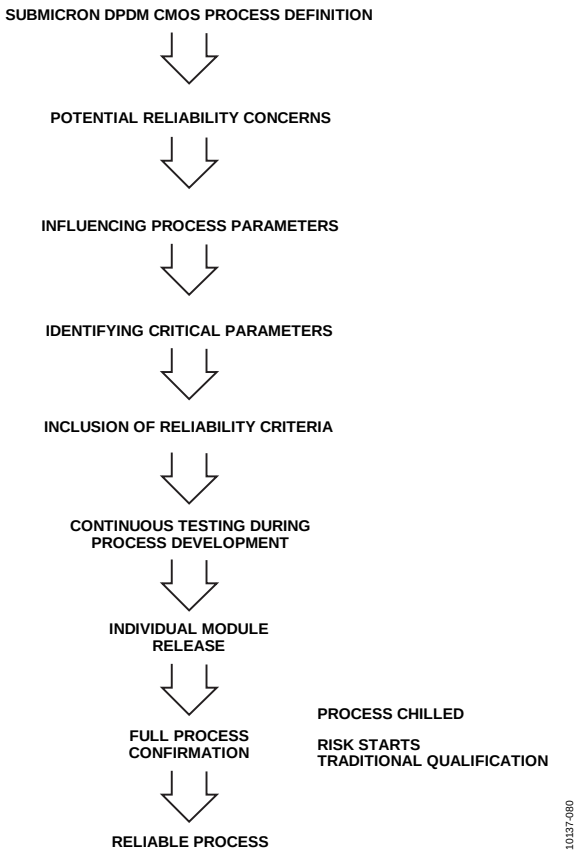

Figure 53. Building in Reliability Flow

Once the process was defined, the potential reliability hazards were identified in conjunction with the process engineers. This involved process development, process manufacturing, and reliability. These mechanisms were then analyzed to discover which processing steps, equipment, and process settings would affect these reliability parameters. This enabled the development of a joint process development/ reliability test chip; it also made the process engineers aware of how their actions could impact the reliability of the process. Based on the reliability knowledge and the literature surveys that were conducted, the critical failure mechanisms to focus on were EM, stress migration, dielectric wear-out, and MOS hot carrier effects. Other issues such as defect density and particle control, which impact quality and reliability, were left solely to development and manufacturing. Figure 54 shows a subset of an example of the relationship diagram developed for EM.

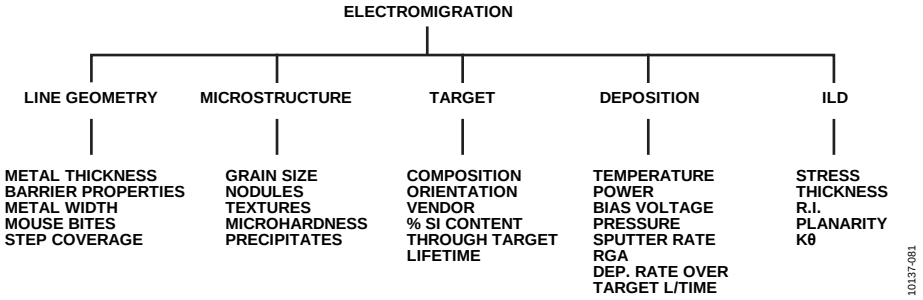

Figure 54. Section of Electromigration Flow Chart

The targets for the reliability were agreed to at the start of the development process. They were included in the module contracts along with electrical and defectivity performance, which were the responsibility of each process owner. Consequently, process modules could not be released into production until the agreed criteria were achieved. In effect, this transferred the ownership of the process reliability from the reliability engineering groups to the process development groups.

An example of the data generated for the gate dielectric reliability using TDDB testing is shown in Figure 55, which illustrates the build-up of data from single polysilicon, single metal to single polysilicon, dual metal to dual polysilicon, dual metal processing. Also included are the results of various experiments conducted to optimize the process. The example demonstrates the value of having a total integrated development test chip that could simultaneously evaluate the yield, quality, and reliability. There were significant advantages in using this

approach. The reliability engineers were able to run reliability tests on each process split and identify any reliability hazards early in the process development stage and implement immediate fixes.

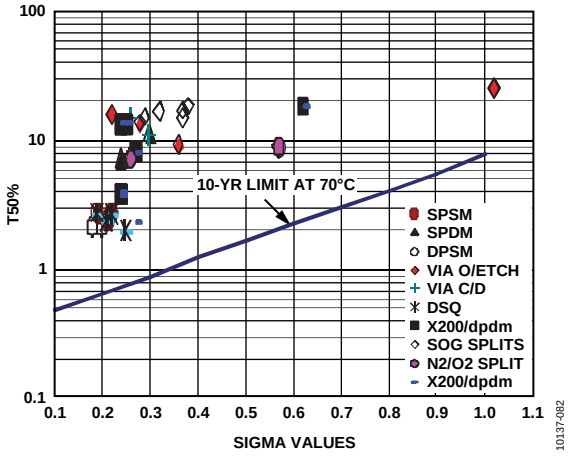

Figure 55. Gate Dielectric Reliability During Process Development

Another example was the aluminum interconnect via (with specific underlying topography) that was not meeting its EM target. This was largely due to an extrinsic population on Via B not evident on other structures as shown in Figure 56. In conjunction with the module owners, a series of evaluations was established to understand the cause of this extrinsic population, with the intent of maximizing the interconnect via performance. This was quickly identified as the duration of the IMD via opening etch process.

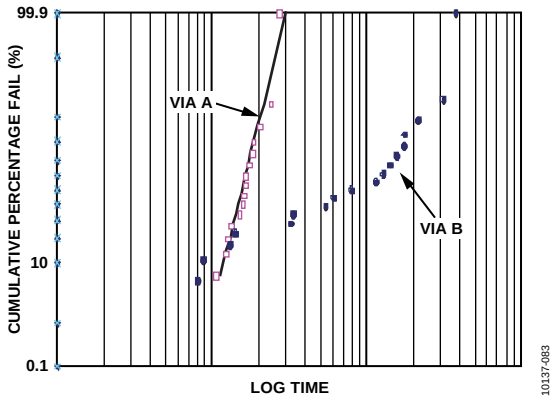

Figure 56. Via EM

From the FMEAs carried out, it was realized that front-end parameters could be adversely affected through later stages of processing (due to plasma charging, and so on). As a result, any change in the back-end manufacturing process could affect gate dielectric and hot carrier reliability performance. A change in the etch time of the via was the solution to the via EM issue. The evaluation consisted of three different etch rates and the via EM, hot carrier, and oxide performance was measured for each of the three etch rates. Figure 57 shows the impact of the different etch rates on the via EM. The data shows that etch rate C produces the best reliability, that is, a very tight σ value and a high T0.1% failure time.

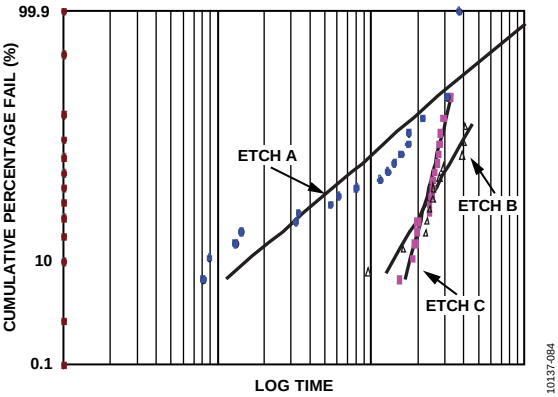

Figure 57. EM Lifetime Data for Various Etch Rates

If the only test performed at this stage were via EM, this would be the obvious choice of etch rate. However, the hot carrier reliability data showed that this etch rate gave the poorest reliability performance, as indicated in Figure 58.

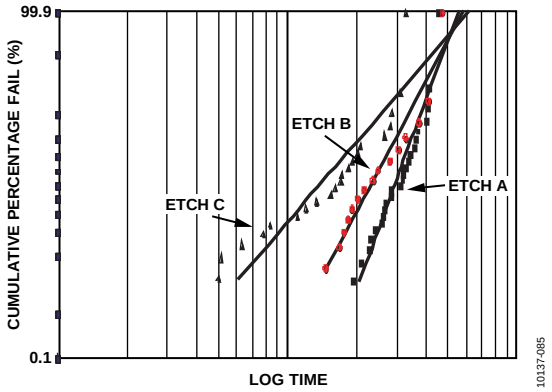

Figure 58. Hot Carrier Reliability vs. Different Via Etch Rates

In Figure 58, Etch C produced a low T0.1% and a very large sigma (Σ) compared with Etch A and Etch B. Etch A and Etch B produced acceptable hot carrier lifetimes. Etch B also proved acceptable via EM performance and, as a result, was the one chosen for the process. The use of the building-in reliability approach also led to the correlation of reliability figures to in-line parameters. This further enhanced the use of statistical process and reliability control to maintain process reliability, as shown in Figure 59, where the relationship between CMOS hot carrier reliability and substrate current was verified.

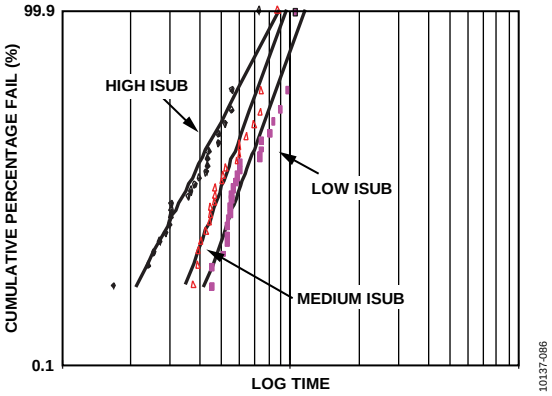

Figure 59. Hot Carrier Lifetimes and Their Relationship to Substrate Currents

The use of the building-in reliability approach meant that the traditional qualification was a formality because all foreseen issues were investigated and eliminated before qualification began.

SUMMARY

The primary benefit of the building-in reliability process was the development of a stable, reliable process through the understanding, controlling, and measuring of process parameters. The increased interaction between the process and reliability groups lead to a greater understanding of each other's requirements and embodied a spirit of teamwork and cross-departmental cooperation that proved to be very productive. The approach enabled any issues to be immediately verified and resolved in a very effective manner. By adopting the approach outlined, the traditional end-of-line qualification was simply a formality since any issues that could have adversely affected it were handle during the development process.

PACKAGE RELIABILITY

INTRODUCTION

The reliability of the assembly process is exceptionally important with regards to the life of the product. The packaging process provides first-level protection for the die and active circuitry against harsh printed circuit board manufacturing techniques.

Products manufactured by Analog Devices fall into two categories: hermetic and plastic. Thanks to today's assembly processes, issues that dogged the plastic packaging process in the past, such as corrosion and purple plague, have been eliminated due to improved processing techniques and controls. Today the majority of integrated circuits are produced in plastic packages. It is not always easy to determine whether or not a failure mechanism is due to a package, design, or wafer fabrication issue, since there is a strong interdependence in all areas once the die is assembled, tested, and placed on a printed circuit board. Figure 60 indicates this interdependence and the role of environmental stress testing.

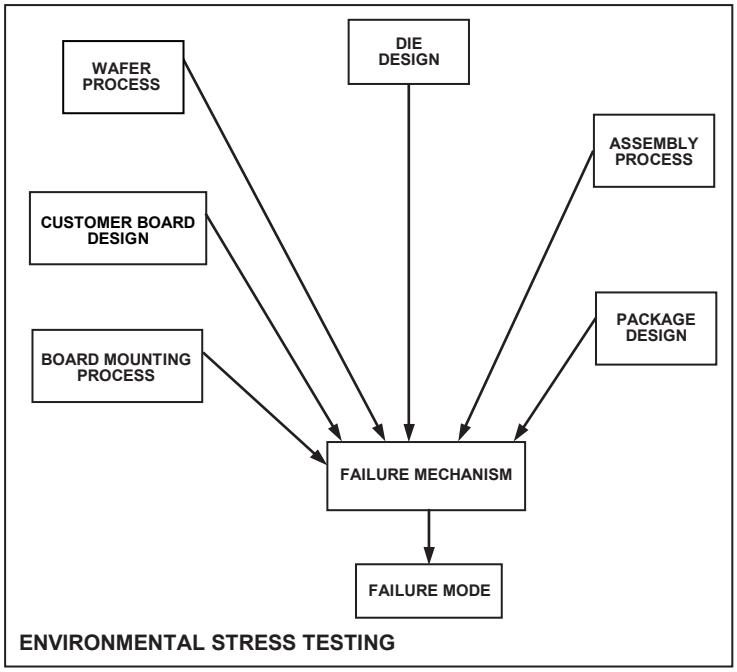

Figure 60. Process Interaction on Failure Mechanisms

It is easy to understand how the die design, wafer fabrication process, and so on can affect the performance of the product and how this interaction can lead to specific failure mechanisms. However, as discussed previously, other stresses such as temperature, humidity, mechanical or electrical also affect the device reliability. These stresses are normal for the service life of the product.

These stress conditions can be accelerated in a controlled environment by thermal, mechanical, electrical, and humidity stimuli that result in failure and are used to generate reliability data. However, running the devices in these tests alone is not sufficient. Today the processes of IC manufacturers extend to their customers; the manufacturer must include a precondition and the appropriate thermal and moisture data to simulate printed circuit board production to generate accurate reliability figures for the products produced.

THERMAL ISSUES

The reliability of all integrated circuits is very dependent on environmental conditions. Considering all the factors that can influence package reliability, thermal stress has the most significant impact. All integrated circuits dissipate some power while operating, which in turn causes the temperature of the integrated circuit to rise. The temperature rise of the integrated circuit is a complex function of the device construction, electrical operating conditions, part placement on the printed circuit board, and the airflow around the device (laminar or turbulent). The IC producer controls some of these while the user and the environment in which the parts operate control the others. As a result, the thermal characteristics of integrated circuits are a major concern to both users and producers of ICs. The increase in temperature due to a junction temperature (T_J) rise of the components can adversely affect the long-term reliability of the product.

RELIABILITY IMPLICATIONS

The bathtub curve shown in Figure 61 has long been used to represent the reliability of integrated circuits. The curve represents the cumulative failure rate over time and has three distinct sections: early life failure rate (infant mortality), useful life period, and the wear-out stage.

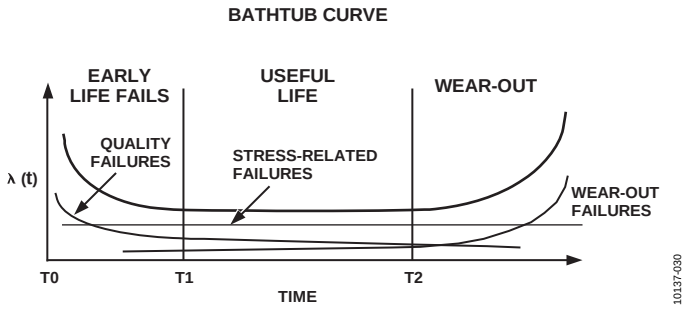

Figure 61. Classical Bathtub Curve

The infant mortality or early life period is typically the first few months of circuit operation and is characterized by a decreasing failure rate (T0 to T1 above). The types of failures found in this period are quality failures induced by the manufacturing process and are generally found at board level test. Most reputable IC manufacturers have programs in place to reduce the infant mortality and to provide early life failure rate data and outgoing quality figures.

The useful life period is characterized by a constant failure rate λ(t) from time T1 to T2 in Figure 61, where the failure rate is the number of devices that are expected to fail in a given period of time, for example, % failures per 1000 hours. This can then be translated into a mean time to failure (MTTF), which is the time interval between failures. This is simply the inverse of the failure rate. Both the failure rate and the MTTF are the primary units of measure for device reliability. The useful life period is typically quite long for integrated circuits, extending for decades before going into the wear-out stage where life-limiting failure mechanisms such as oxide wear-out and electromigration come into play.

Many factors affect the length of the useful life period of the product, including pressure, humidity, and electrical stress. However, the most critical and common factor to most failure mechanisms is the die temperature. The temperature at which devices operate shortens the useful life period of the product, increases the failure rate in the useful life period, and shortens the time to wear-out. As a result, die temperature plays a significant role in the operating reliability of the product. The relationship between integrated circuit failure rates and temperature is very well established and represented by the Arrhenius Model.

$$\lambda = A\ Exp.\ (E_a/kT)$$

where:
λ is the failure rate.
A is a constant.
E_a is the activation energy for the particular failure mechanism (0. 5 to 1.2 eV range).
k is Boltzmann's constant (8.63×10^{-5} eV/K).
T is the temperature in Kelvin.

The failure rate is an exponential function of the temperature stress: the higher the stress, the higher the failure rate of the components. Most IC manufacturers conduct reliability testing at elevated temperatures to demonstrate the reliability of their products. The temperature relationship between these tests and the actual use conditions is derived from the previous equation and is as follows:

$$Acc.\ Factor = \lambda 1/\lambda 2 = Exp.\ [-E_a/k\ (1/T2 - 1/T1)]$$

where:
$T1$ and $T2$ are the use and test temperature, respectively (K).
$\lambda 1$ and $\lambda 2$ are the failure rates at use and test temperature, respectively (K).

Based on the previous equation, a normalized graph in Figure 62 can be drawn to indicate the effect of junction temperature on failure rate.

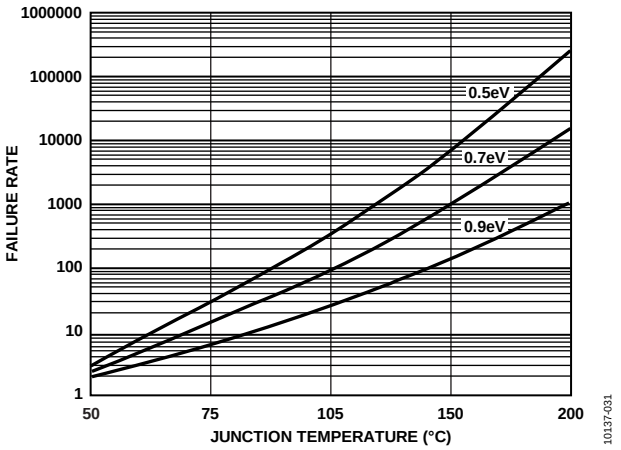

Figure 62. Failure Rate vs. Temperature (C)

The graph is normalized but gives a good indication of how the failure rate can vary with the junction temperature. The graph indicates that reducing the junction temperature increases the reliability. Table 8 indicates the effect of reducing the junction temperature from 105°C to 75°C in an application for the different activation energies.

Table 8.

Activation Energy (eV)	Improvement
0.9	10×
0.7	8×
0.5	4×

As illustrated, the reliability improvement depends on the activation energy. Significant reliability improvements (10× improvement being possible for 0.9 eV) can be made by reducing the device junction temperature [82 – 85] in the application.

The thermal resistance between two points in space is the temperature difference needed to drive heat at the rate of one watt from one point to the other. It is used as a measure of how easy it is to remove heat from the center of an IC package to the exterior surface, or into the ambient surroundings of the package. A high value of thermal resistance means that it is more difficult to remove the heat. Thermal resistance is measured between two points or, more typically, between two planes. For example, thermal resistance is stated as being from X to Y or from junction to case.

Thermal resistance from junction to case is defined as the temperature gradient required to drive heat at the rate of one watt from a diode junction on the circuit to the hottest point on the surface of the package. In practice, this is the temperature gradient from anywhere on the surface of the chip to a point on the surface of the package directly underneath the center of the chip. For the latter location, it is often more convenient to use a point on the surface of the package directly above the center of the chip. Another term used for this parameter is Theta J-C, often written as θ_{JC}.

There are detailed standard methods defined for carrying out the measurements to determine the value of θ_{JC}. For example, see SEMI Standard Methods G38-87 and G43-87, and MIL STD 883C, Method 1012.

Thermal resistance from junction to ambient is defined as the temperature gradient required to drive heat at the rate of one watt from a junction on the circuit to the air or other surroundings of the package.

In practice, this is measured as the temperature gradient from anywhere on the surface of the chip to a point in the air one-half inch away from the package and one inch upstream from the package. Another term used for this parameter is Theta J-A, often written as θ_{JA}.

Again, detailed standards explain how these measurements are taken. For example, see SEMI Standard Method G38-87, and SEMI Standard Specification G42-88.

DERATING FACTOR

Derating is the term used to specify how the power dissipated in a device must be reduced when the temperature of the ambient environment exceeds a particular level. In such circumstances, there is a concern that the maximum junction temperature for the device may be exceeded because the package may not be able to transfer the heat from the chip out to the warm environment.

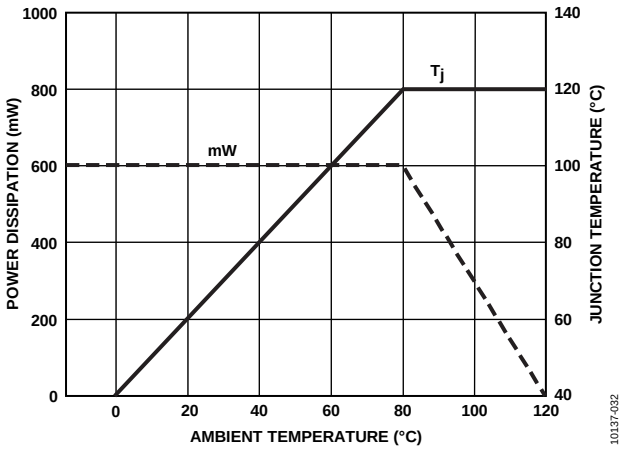

Figure 63. Power Dissipation (mW) and Junction Temperature (°C) vs. Ambient Temperature

In Figure 63, the device dissipates up to 600 mW of power (illustrated by dotted line). The junction-to-ambient thermal resistance of the device is 67°C per watt. The temperature of the junction rises by 67°C if one watt of power is dissipated. Thus, at 600 mW, the junction temperature is not exceeded.

In this example, it has been determined that the junction temperature should not exceed 120°C. This means that the maximum allowable junction temperature is reached if the device is in an ambient of 80°C, and dissipating 600 mW. The only way in which the device can be operated in an ambient above 80°C is to reduce the power dissipation.

By derating the power dissipation by 15 mW for each degree centigrade rise in the ambient temperature above 80°C, the junction temperature remains at 120°C. This is as a result of the derating factor, 0.015 W per °C, which is actually the inverse of the junction to ambient thermal resistance, 67°C/W.

For some devices such as power controllers, the power dissipation is almost totally dependent on the application. Such a device in the previous example may theoretically be operated at 15 mW in an ambient of 119°C, where the maximum junction temperature is not exceeded.

In some instances, manufacturers choose to set derating to begin at an ambient temperature that is even lower than typical application environments. For example, a manufacturer may specify a device as capable of dissipating 1700 mW, with derating required in conditions above 25°C. The package may be derated at 20 mW per degree centigrade. In such case, in an environment of 70°C, the device is limited to 800 mW.

ENHANCING THE HEAT DISSIPATION

There are two generalized construction types for all IC assemblies. In the first, the chip is enclosed in a hermetic space, with the base of the chip attached over its full area to the inner surface of the package. No other part of the chip is in contact with the package. In the second type, the chip is encapsulated in the center of a solid plastic molding that also supports the leads by which the package is mounted onto the printed circuit board.

In the hermetic package, the portion of the package to which the chip is attached becomes almost as hot as the chip, and the heat is then conducted to the remainder of the package body. The heat is removed from the package by conduction through the leads into the printed circuit board, and from the surfaces of the package body by convection into the surrounding environment. The top surface of the package body is usually the coolest, having the longest thermal path to the chip, and is poor at dissipating heat into the ambient. Typically, most of the heat is conducted away, through the leads, into the printed circuit board. However, where the package is constructed in a die-down configuration, the upper surface of the package is the hottest, and is suitable for the mounting of supplementary heat sinks. These die down packages offer a substantial amount of increased surface area to the ambient environment. In this way, the thermal resistance of the package can be greatly reduced, especially where there is a significant flow of cooling air.

Heat sink manufacturers supply data on the thermal performance of their products specifying the thermal resistance from mounting face to ambient. Because the heat sink is mounted at the hottest point on the package, the full thermal resistance of the assembly (that is, from junction to ambient) can be estimated from the θ_{JC} of the package plus the thermal resistance of the heat sink.

In the plastic encapsulated packages (PEP), the chip is mounted onto a metal (usually copper) paddle. The plastic encloses the chip and paddle on all its faces, and heat can thus be conducted in all directions away from the chip. The plastic is a poor conductor of heat, but because heat can flow in all directions, the overall performance of typical plastic packages is at least as good as their hermetic equivalents.

Thermal performance can be enhanced in plastic encapsulated devices by

1. Incorporating a metal heat spreader internally in the package;
2. Mounting the chip onto a thick copper slug instead of a paddle with the opposite face of the copper slug extending to the surface of the package;
3. Directly connecting some of the leads to the paddle on which the die is mounted; or
4. Arranging the layout of the leads and paddle to maximize the flow of heat from the paddle to the leads.

External heat sinks are very effective when mounted directly onto the slug face in the package with the thick copper slug, but otherwise are seldom used with plastic encapsulated packages. High thermal conductivity plastics are occasionally used to improve thermal performance. There are major disadvantages in terms of manufacturability and package reliability for almost all such compounds, and they are to be avoided if at all possible.

SIMILARITIES BETWEEN MANUFACTURERS

In most cases, IC manufacturers use the same package materials and the same method of construction for packages that are visually similar. Therefore, devices in packages of identical outline will have virtually identical thermal performances, if measured under identical conditions. There are, however, significant differences in the thermal performance quoted on data sheets by different manufacturers. Even for identical packages, these products are sometimes, in fact, produced in the same factory from the same materials, perhaps on the same day, with the only difference being the details of the circuit on the chip. In such cases, the difference between the quoted thermal performances rests solely on the circumstances under which the measurements were taken.

EFFECT OF COMPONENT MOUNTING ON THERMAL RESISTANCE

The primary routes for thermal dissipation from an integrated circuit are by radiation from the package (and heat sink, if used) to the ambient air, and by conduction to the circuit board. Ultimately, all of the dissipated heat finds its way to the ambient environment. The thermal resistance figures published for Analog Devices products are generated on standard SEMI boards. The SEMI standard board is a double-sided board, with 20% of each side covered with 1 oz/sq. ft. copper. This provides a conservative measure of junction to ambient thermal resistance. It is important that component users understand the factors under their control that affect the junction temperature of the die.

SOCKET VS. BOARD MOUNTING

The thermal data published for Analog Devices products is based on direct mounting of the component to the board, with all leads soldered. Sockets provide a less efficient heat sink than direct board attach, and therefore increase the junction temperature of the component. Where sockets are used for high power dissipation products, it is recommended that thermal resistance measurements are made for that component/socket combination.

THERMAL GAP FILLERS

Where the thermal resistance of a board or individual component needs to be lowered, one option is to use a thermal gap filler material. These are compliant, electrically nonconductive, elastomer-filled sheets that can be cut to size, placed over the component(s) in question, and used to fill the gap between the component and the enclosure or surface above, which acts as a heat sink. Because of their compliance, they can usually accommodate the height differences between various components, and also provide a reduced thermal contact resistance due to their ability to conform to surface irregularities. The filler is usually a highly thermally conductive ceramic, such as boron nitride or aluminum oxide. For suitable applications, these materials can provide a cost-effective solution to power dissipation problems.

COMPONENT SELECTION

One option to consider when dealing with any thermal resistance problem is to select the same product in a different package outline, if space permits. Table 9 shows an example of a 20-lead component mounted on a SEMI standard board in still air. If the device, dissipating 0.5 W, is required to operate in an ambient of 80°C without exceeding the maximum permitted junction temperature of 125°C, changing from the SSOP to SOIC outline provides a solution without any additional heat sinking.

Table 9.

0.150" SOIC	5.3 mm SSOP	4.4 mm TSSOP	Delta
79	126	134	θ_{JA} °C/W
119.5	143	147	< Junction temperature (°C) while dissipating 0.5 W in 80°C ambient.

FORCED AIR COOLING AND HEAT SINKS

Unless otherwise stated, the thermal data provided by Analog Devices is based on still air conditions as specified in SEMI G42-88. For applications where the ambient temperature is too high and cannot easily be reduced, one option is the use of forced air cooling, with or without a heat sink. Figure 64 shows the effect of forced air cooling on a component, with and without a heat sink.

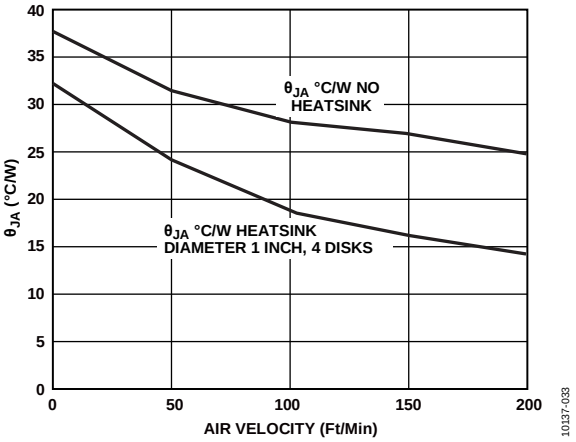

Figure 64. θ_{JA} vs. Airflow

When selecting a heat sink, it is important to consider how the heat sink manufacturer generated the thermal resistance data. Some manufacturers attach an insulating block to the base plate of the heat sink, thus preventing heat loss from this surface, while others suspend the heat sink in the air, allowing heat dissipation from all surfaces. The first method is a better representation of how heat sinks are used in practice.

Where a heat sink is used, the power dissipated can be expressed as follows:

$$Q = (T_J - T_A)/(J_C + J_{CH} + J_{HA})$$

where:
Q is the power dissipated in watts.
T_J is the silicon junction temperature (°C).
T_A is the air temperature (°C).
J_C is the junction to case resistance (°C/W).
J_{CH} is the case to heat sink resistance (°C/W).
J_{HA} is the heat sink to ambient air resistance (°C/W).

The airflow and repeatability of the manufacturing process must also be considered.

The optimum board position is vertical because this facilitates natural convection giving a reduction in thermal resistance of 8% to 10% over horizontally positioned boards. Board vertical length can also have an effect because the greater this length, the more the air has been heated by the lower components before it passes the upper ones. This principle is also applicable to forced air cooling; therefore, the shortest board side should be parallel to the airflow.

BOARD CONSTRUCTION AND MOUNTING

For normal still air conditions, the primary heat dissipation path is via the component leads into the PCB. The critical factor is the thermal resistance of the board. Thermal resistance can be lowered by maximizing the use of GND planes as heat sinks, and also by optimizing the means by which the heat can be dissipated: for example, conduction into the board mounting chassis and by maximizing the potential for natural convection cooling. The greater the percent copper in the board, the lower the thermal resistance. Thermal modeling for an 8-lead SOIC has shown that doubling the conductivity of the board (W/M K) reduced the component junction temperature from 130°C to 98°C. The use of wide tracks and thermal vias to the ground plane also have a significant effect.

Placing critical components close to where the edge of the board is attached to the chassis can provide additional cooling without the use of heat sinks or forced air. For best results, it is advisable to avoid close spacing of high power devices, allowing the heat to be dissipated over the maximum possible area.

One result of the ongoing trend towards miniaturization in packages is that the thermal resistance of the packages increases with the reduction in size. It is now more important than ever that the user of semiconductor packages understands not only the issues arising from the increase in thermal resistance, but also the importance of correct component selection and mounting techniques. Possibly the most important point to bear in mind when comparing thermal data, whether it be for a semiconductor package, heat sink or gap filler, is to understand the test methodology used. If the test method is not clearly described, the values must be treated with caution.

MOISTURE EFFECTS

The advent of the plastic surface-mount component (PSMC) has enabled printed circuit board designers to obtain a greater packing density of components on boards and to utilize both sides of the boards for component placement. This progression has considerably increased the use of PSMC. Unfortunately, this progression necessitated an increase in the temperatures used to place the components on the boards. Modern surface-mount techniques can expose the surface-mount components to temperatures of up to 260°C, which placed additional stress on the components and highlighted new failure mechanisms [86 – 98]. As a result, mechanisms such as popcorning and delamination have occurred. The plastic molding compound used for the PSMCs is hydrophilic and absorbs moisture from the surrounding air, reaching a saturation level dependent on the surrounding ambient. The quantity of moisture absorbed depends on the quantity of moisture in the surrounding atmosphere, while the rate at which the moisture is absorbed depends on the temperature at which the component is sitting. The higher the temperature, the higher the absorption rate and the faster the package reaches equilibrium with the surrounding air. The graphs in Figure 65 and Figure 66 illustrate this effect.

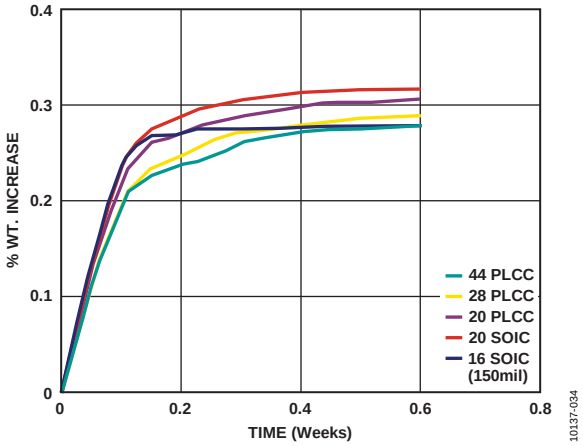

Figure 65. Moisture Absorption Graph for Various Packages at 85°C and 85% R/H

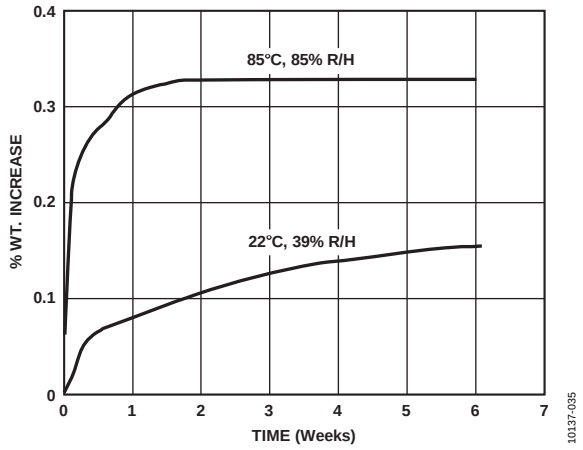

Figure 66. Moisture Absorption Graphs for a 44 PLCC Package at Various Conditions

For this particular package, the quantity of absorbed moisture was measured after exposure in a controlled environment at various times. A selection of the packages was identified and weighed at time zero, after a bake to initialize the moisture content of the packages. The packages then underwent exposure to various conditions of temperature and humidity for predefined times and the graphs plotted. The graphs show that the units saturate, that is, they do not take in any more moisture, at a level that depends on the humidity. The moisture can congregate in the package body at the areas indicated in Figure 67.

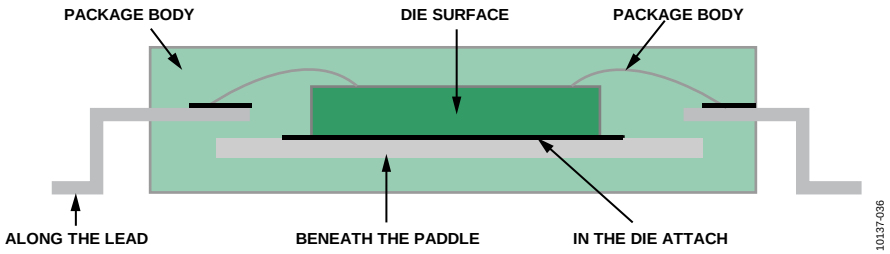

Figure 67. Cross Section of a Typical Package

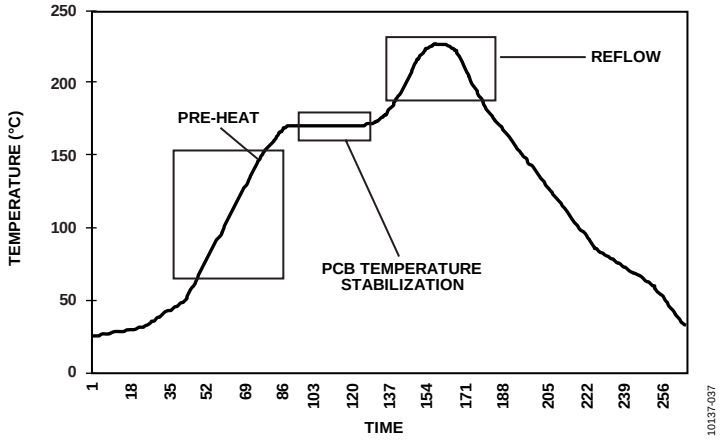

Figure 68. Typical Solder Profile

The moisture has a relatively benign effect on the reliability of the product unless it has brought some impurities into the body of the package. However, the subsequent printed circuit board manufacturing process subjects the board to extremely high temperatures as the convection profile in Figure 69 indicates.

In the manufacture of the printed circuit board, the components can reach temperatures of up to 260°C in seconds. This rapid rise in temperature vaporizes and moisture present in the packages causes it to expand. This expansion of vapor, particularly in the areas of the die attach and lead frame, can cause a separation of the molding compound from the die surface (popcorning) or lead frame. This separation then creates gaps on top of the die and at the back of the lead frame, which can have a detrimental effect on the reliability of the product. If the separation is at the back of the lead frame paddle, it can degrade the thermal performance of the product, and if it is on the die surface, it provides a gap where moisture and contaminants from the printed circuit board process can congregate and cause device failure.

If the quantity of moisture absorbed is very large, due to exposure to extreme humidity levels, the damage can be more significant. Cracks can propagate from the hard surfaces such as the die and paddle to the outside surfaces of the package as shown in Figure 69. These cracks can significantly degrade the moisture resistance of the package and can shear bond wires leading to device failure. In Figure 69, the delamination is shown in red on the fixed surfaces while the cracks propagating from the stress points are shown in yellow. The cracks generally tend to start at the immovable surfaces such as the die and leadframe and propagate to the outside of the package. In some instances, the cracks sever the bond wires thus breaking the connection between the die and the outside world leading to device malfunction.

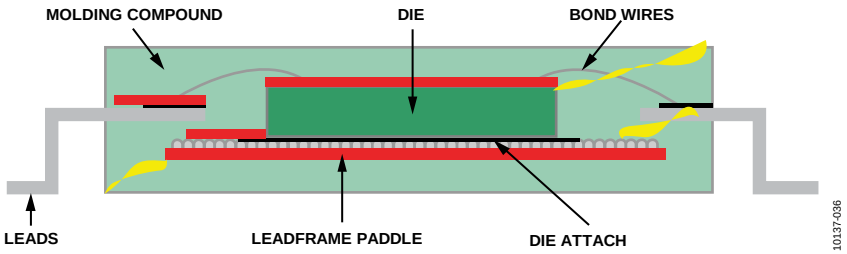

Figure 69. Package Cross Section Showing Delamination (Red) and Cracking (Yellow)

The IC manufacturer can measure the resistance to failure mechanisms, such as those outlined previously, by conducting specific reliability tests. These tests include the use of an acoustic microscope to view the extent of delamination and cracking because of exposure to a simulated soldering process after exposure to various temperature and humidity conditions.

Figure 70 shows the acoustic microscope image for a 44-lead PLCC package after exposure to high conditions of temperature and humidity.

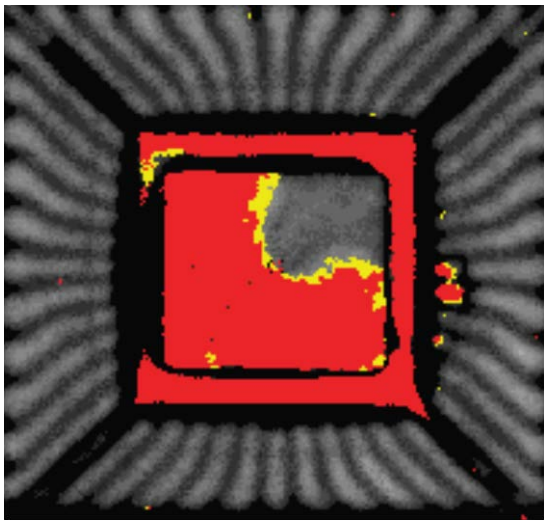

Figure 70. Acoustic Microscope Micrograph of a Delaminated 44 PLCC

The red areas in the figure indicate delamination on the die surface; the gray areas indicate that there is still adhesion between the die surface and the plastic molding compound. Research shows that the influencing factors that contribute to package cracking and delamination are

1. Peak temperature reached during solder reflow.
2. Dimensions of the die paddle.
3. Percentage of moisture absorbed by the molding compound.
4. Adhesion of the molding compound to the die and leadframe.
5. Thickness of the molding compound under the paddle.

Fukuzawa, et. al., have tied together the above factors in a simple model. The steam pressure in the gap under the paddle in Figure 69 causes the molding compound to expand from the paddle and form a dome (popcorn). A crack occurs when the maximum bending stress on the plastic, S_{MAX}, exceeds a fracture stress characteristic of the molding compound being used at an elevated soldering temperature.

Therefore, cracking occurs if

$$S_{MAX} > S_{CRIT}\ (T_{SOLDER}) \tag{12}$$

The maximum bending stress is first reached at the center of the long side of the die pad and is given by

$$S_{MAX} = 6K\ (a/t)^{2P} \tag{13}$$

where:
K is a dimensionless stress concentration factor which depends on the aspect ratio of the paddle.
a is the length of the short side of the paddle.
t is the thickness of the molding compound under the paddle.
P is the water pressure in the cavity based on the above equation packages with large die paddles and thin layers of molding compound under the die paddle are more prone to package cracking. Fukuzawa found that for an (a/t) ratio of less than five, package cracking did not occur.

To predict a cracking sensitivity as a function of moisture saturation or dryout, a model is required for P in Equation 12. This has been derived as

$$P = H \times P_{SAT}\ (T_{SOLDER}) \tag{14}$$

where:
H is the relative humidity of the saturation ambient prior to solder shock.
P is the water vapor pressure in the cavity, which varies with the peak solder temperature.

The second failure mechanism associated with moisture absorption is cratering. In this type of failure, the sudden evaporation of the moisture due to the high reflow temperatures in conjunction with the quantity of silicon modules in the aluminum can cause the gold ball bonds to lift as a result of excessive moisture pressure. Figure 71 is a graphic example of what occurs.

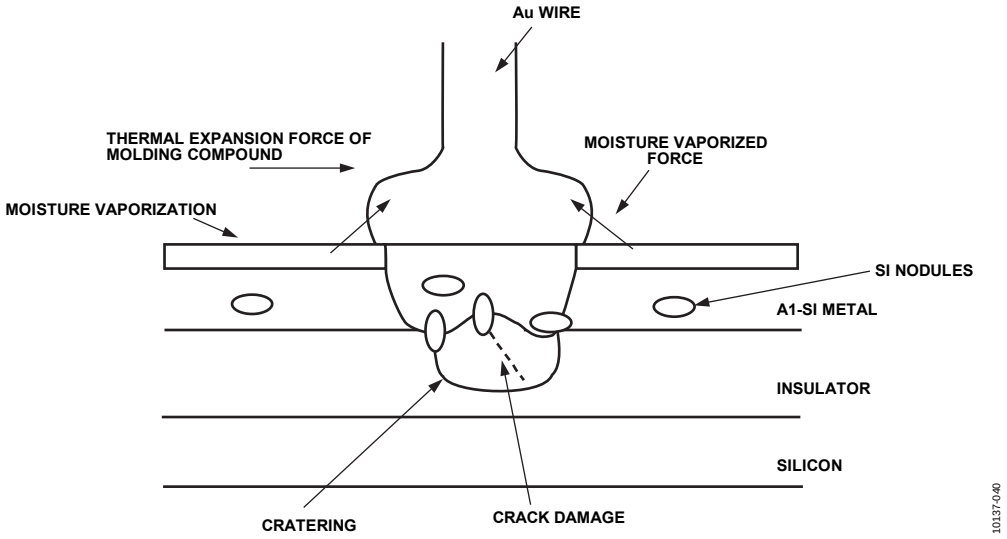

Figure 71. Bond Pad Cratering

The Si nodules are formed on the insulator from the silicon added to the aluminum in the deposited Al-Si metallization. At wire bonding, excessive bonding force can cause silicon nodules to damage the insulator during the bonding process and the accompanying ultrasonic vibration can exaggerate the damage causing microcracks in the insulator under the ball bond. Once the molding occurs, the package absorbs moisture that penetrates to the die surface. The very high temperatures experienced during reflow soldering causes the moisture to vaporize, creating very high pressure in the vicinity of the ball bond. The underlying insulator is weakened by microcracks. This, in conjunction with the thermal expansion force of the molding compound and the moisture-vaporized force, can cause the ball bond to lift leaving behind a crater in the silicon as shown in Figure 72.

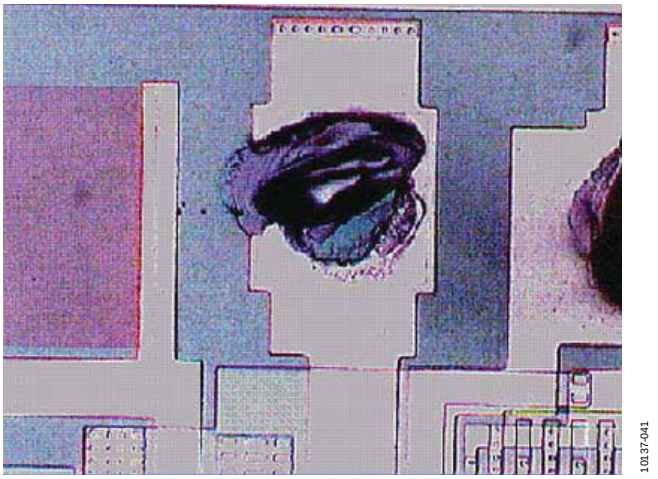

Figure 72. Bond Pad After Cratering has Occurred

In much the same way that the devices absorb moisture, this same moisture can be expelled from the package by baking the products prior to circuit board manufacture. This is shown in Figure 73, in which packages that had been soaked in moisture until saturation occurred were dried out by baking.

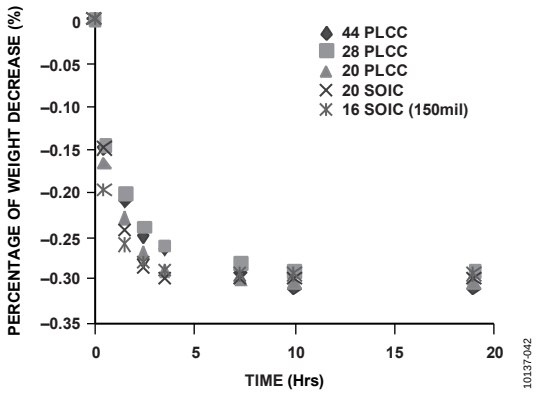

Figure 73. Bake-Out of Various Packages

Analog Devices has developed a strong understanding of this reliability concern. It has led to the development of in-house reliability tests and procedures to evaluate the reliability of Analog Devices products post-solder simulation. For larger packages, Analog Devices has a procedure that involves baking the components to expel all moisture and then sealing them with desiccant and humidity indicators in moisture barrier bags. These units should be used within a predefined timeframe and should be rebaked only once. The full details of Analog Devices' procedure are available on request.

ADDITIONAL MOISTURE-RELATED FAILURE MECHANISMS

Popcorning and delamination are not the only failure mechanisms associated with moisture intrusion in plastic packages. Other failure mechanisms such as corrosion also occur, although these are not as prevalent today as they were more than a decade ago. To have moisture-related failure mechanisms in plastic packages, four prerequisites must occur:

1. There must be a path for moisture.
2. There must be moisture.
3. There must be a voltage.
4. There must be a contaminant.

All four of these prerequisites are present in some degree in plastic packages, and the goal is to minimize them and reduce the moisture-related failure rate of the products.

As previously discussed, the plastic package is hydrophilic, absorbing moisture from the surrounding ambient until it reaches equilibrium with that ambient. Therefore, the most important issue is whether or not there is a path for contamination or impurities. The path to the die for impurities can be along the interfaces, such as the leadframe/package interface, which are formed as part of the package construction. These paths could be the result of unintentionally introduced cracks, voids, or gaps during manufacture. Figure 74 shows the interfaces that occur inherently in the package and how these provide paths for impurities to reach the die surface. Figure 75 shows the results when these contaminants reach the die surface. It has been shown that for corrosion types of failure, the highest density of failures occur on the pins with the shortest path to the die surface.

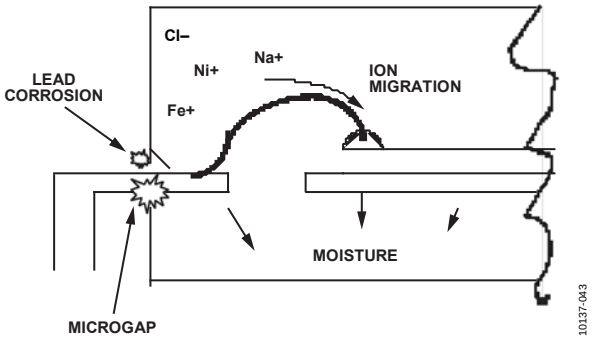

Figure 74. Ingression Paths

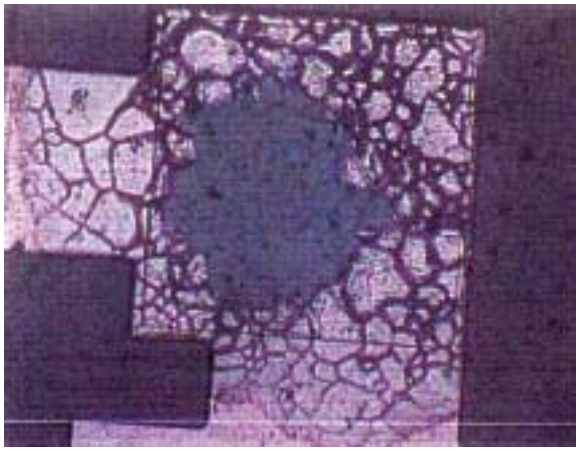

Figure 75. Corroded Bond Pad

The analytical evidence suggests that the impurities diffuse along the interfaces between the epoxy and the leadframe and up onto the bond wires where they make their way down to the die surfaces, aiding the corrosion process. The corrosion process is regenerative as the following equations for aluminum corrosion in the presence of chlorine show. As a result, minute quantities of contaminant can cause significant amounts of corrosion.

The aluminum reacts with the Cl– in the following fashion:

$$Al + 4\,Cl^- \rightarrow Al\,(Cl)^-_4 + 3e^-$$

The $Al\,(Cl)^-_4$ then reacts with the available water by the following reaction:

$$2\,Al\,(Cl)^-_4 + 6\,H_2O \rightarrow 2\,Al\,(OH)_3 + 6H^+ + 8Cl^-$$

From this reaction, the Cl– ion is always available to continue further corrosion. This is known as a regenerative process. The resulting product is aluminum hydroxide Al (OH)3, whose volume of expansion is sufficient to crack the passivation layer.

The paths for moisture and contaminants can be provided by cracks that can occur

- During mold ejection.
- Due to deflash, trim, and form due to poor tooling.
- Due to thermal shock.
- Due to reflow soldering.
- Due to the test process in IC manufacture.

When the moisture and impurities reach the die, the path to active circuitry can be provided by

- Pinholes in the passivation.
- Poor passivation step coverage over aluminum steps where passivation is cracked.
- Cracks in the passivation due to thermo mechanical type stresses.
- Inadequate gettering in the passivation.
- Poor step coverage at the bond pads on the die surface.

The contaminants can reach the active circuitry by one or all of these paths or they can be introduced by poor contamination control during the wafer fabrication or assembly processes. When these are accelerated by temperature, humidity, and bias, the failure mechanisms that occur can be either aluminum corrosion, which causes a gross circuit malfunction, or a more subtle type of failure such as a V_T shift, which can cause a parametric failure. The aluminum metal corrosion failure mechanism is well understood and occurs in one of two ways:

- Moisture combines with phosphorous to form phosphoric acid. The phosphorous is an integral part of the fabrication process and contained in the phosphosilicate glass (PSG) in the process. This can cause corrosion either with or without bias. Under bias, corrosion can occur at the cathode and the phosphorous can be detected by analytical techniques, such as EDX and SIMS. The PSG can be exposed to the moisture by cracked passivation or misaligned openings in the passivation.
- One of the most efficient catalysts for anodic aluminum corrosion is ionic chlorine. As outlined in the previous example, this is regenerative. The main sources of chlorine include chemical deflash, old generation molding compounds, handling, and oxide strippers.

More subtle failure mechanisms can occur as a result of sodium, such as localized V_T shifts resulting in very subtle failures. This type of failure can occur as a result of poor handling techniques in the fabrication or assembly process.

Metal corrosion is no longer a significant failure mechanism in plastic packaging. The phosphoric content of the glass exposed to the moisture is carefully controlled. In addition, chlorine and other ionic components such as iron and sodium have been greatly reduced in the newer generation molding compounds and processing materials. Stringent contamination controls and monitors have also been introduced to eliminate contamination in the manufacturing processes. The elimination of aluminum corrosion and other associated failure mechanisms is evidenced by the decreasing failure rates for these mechanisms. Evidence of this can be found by referencing the annually published Analog Devices reliability data, as well as papers published over the past decade on HAST and other related testing methodologies.

Other failure mechanisms related to the lead finish and trim, form, and deflash process can result from moisture and humidity. These failure mechanisms are exceptionally rare and do not require discussion.

STRESS MIGRATION

As metal lines become thinner (that is, <2 µm), failures can occur due to high temperature and heat cycling. The metal interconnect lines can go open circuit as a result of stress. This is called stress migration. In this failure mechanism, unlike electromigration and corrosion, no bias is applied. The stress migration is generated by a thermal mismatch between the aluminum interconnects and the passivation film or the interlayer insulating film. The aluminum atoms migrate to relieve this stress. The aluminum atoms can migrate from the boundary to continue relieving the stress, thus widening the voids at the boundary and eventually creating an open circuit. If the line does not go completely open circuit, this migration reduces the effective width of the metal lines and increases the probability of electromigration failures occurring. The resistance to stress migration is increased by the use of aluminum alloys, and TiN, TiW, and Ti in the metal layer structure.

THERMAL-INDUCED GOLD WIRE FAILURE

The wire bonding process is also a potential cause of failure in the IC process. The Au and Al are two dissimilar metals that can easily interdiffuse to form intermetallic phases such as the purple plague ($AuAl_2$). Characterized by a distinctive purple-like color on the bond pad, purple plague was generally caused by excessive bonding temperatures in the assembly process. Any imbalances of the atomic fluxes in the Au or Al are balanced by a vacancy flux. These vacancy fluxes coalesce to form what are called Kirkendall voids in the intermetallic producing a weakening of the intermetallic. This results in a lower than optimum bond strength that can cause the bond to break during subsequent thermal cycling.

Most molding compounds contain a flame retardant that can be bromine and small amounts of chlorine. The bromine is released by the molding compound at high temperatures and is activated by the chlorine, which is also released from the molding compound, to form Br^-. The Br^- attacks the intermetallic formed between the gold and aluminum, degrading the integrity of the bond and causing failure. Cross sections of a good bond and one degraded by elongated life testing at excessively high temperatures are shown in Figure 76 and Figure 77. The flame retardant, which is required by international specifications, is released at above 150°C and has a life-limiting effect on the bond. This is critical for high-temperature electronics and when conducting extended life tests at junction temperatures of 150°C or greater.

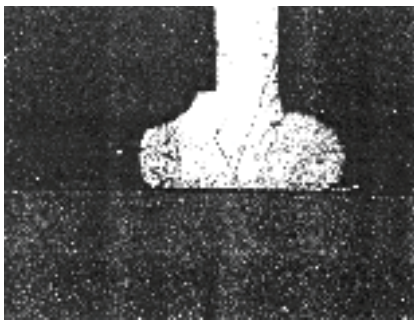

Figure 76. A Good Ball Bond

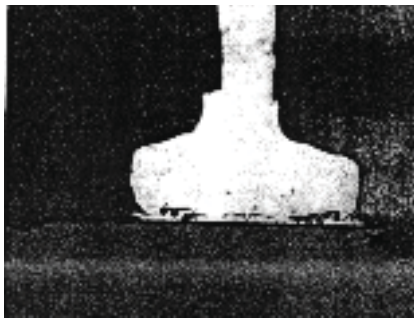

Figure 77. A Thermally Degraded Ball Bond

The presence of contaminants on the bond pads can also affect the reliability of the ball bond. Silicon dust from the sawing process and inadequate cleans can accelerate the AuAl interdiffusion. Other issues, such as residual passivation or stained bond pads, can have a detrimental effect on the reliability of the ball bond.

In today's processes, the thermal degradation of wire bonds is not a major issue because of the lower processing temperatures. This has been brought about by the introduction of thermosonic bonding where the use of ultrasonic energy results in a much lower bonding temperature, and which has had the effect of lowering the temperatures from approximately 350°C to somewhere in the region of 260°C.

PACKAGE CRACKING

Interconnect miniaturization and chip size enlargement advances are occurring rapidly as chip sizes become larger. As a result of these advances, there is an increased risk of aluminum slide or shear stress damage to the IC metallization. Thermal stress from the sealing resins and the different expansion coefficients for the individual components of the IC enhance the probability of these failure mechanisms occurring. Table 10 shows the typical expansion coefficients of the IC components. They are not matched, so it is easy to understand how an internal stress can occur.

Table 10.

Component	TCE
Silicon	3 ppm/°C
Molding Compound	20 ppm/°C
Copper Leadframe	17 ppm/°C
Alloy42	4.7 ppm/°C

The equilibrium assembly processing temperatures where zero stress occurs is approximately 170°C for epoxy adhesive die attach. At this temperature, the zero stress is established and the TCE differentials cause increasing stress as the temperature is lowered. When the TCE values and the processing temperatures are known, the stress conditions can be modeled using finite element techniques (FEM).

The FEM analysis shows that the die attach leads to a bending moment that places the top of the die under a tensile stress and the bottom of the die under a compressive stress. The magnitude of the tensile stress varies with the die thickness, and the die thickness should be optimized for the process. The molding process superimposes a compressive stress on the die, which places the molding compound under tension and, as a result, cracks can propagate in the molding compound. As discussed previously, these cracks can provide paths for contaminants and degrade the reliability of the product.

Once cracks are in the molding compound, temperature cycling can enlarge them. Nishimura has studied this mechanism of crack growth, and it was found that the rate of crack propagation is given by

$$da/dN = C\,(\delta K)^m$$

where:
a is the crack length.
N is the number of cycles.
δK is the stress intensity factor range.
C and m are constants.

The package cracking can be controlled in several ways by:

- Downsetting the die pad below the plane of the leads so that there is an almost equal thickness of molding compound above the die and below the die paddle.
- Modifying the molding compound to control the crack propagation characteristics. This includes modifying the filler particle coating and controlling the size and quantity of the filler particles.
- Providing in-line monitors and controls to minimize the occurrence of voids.

THIN FILM CRACKING AND WIRE BOND FAILURES

Package cracking is not the only failure mechanism of concern in plastic molded parts. The molding compound completely encases the die and, as discussed above, induces many different stresses in the package and die. The adhesion between the molding compound and the die is so great that it forms an exact replica of the die in the molding compound as shown in Figure 78. This picture shows a section of the molding compound after the die was mechanically removed from the package. This implies that the molding compound transmits a force to the die and the bond wires, and these forces can cause bond wire and die-related failures during the thermal and temperature cycle testing. The two different aspects to consider are:

- Package cracking and propagation.
- How bond wires respond to the internal package stressing.

To understand these issues, the forces in the package must be understood.

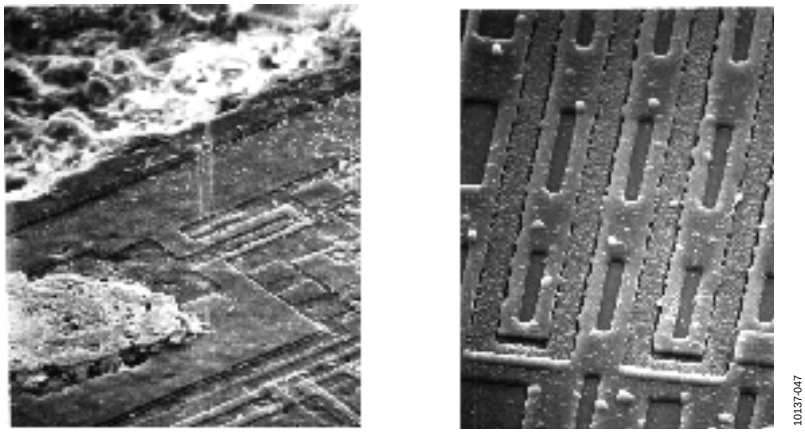

Figure 78. Imprints of the Die on the Plastic Molding Compound After Processing

NATURE OF THE FORCES

The forces acting on the surface of the die are shown in Figure 79. The zero stress point is around 170°C where the die attach and molding processes occur. All thermal tests run from around +150°C to −65°C or −45°C. These temperatures represent the range of operation for most products. Figure 79 represents the nonzero stress condition.

There are two components of force acting on the die. There is a shear force directed towards the center of the die that vanishes toward the center, and a compressive normal force that is almost constant along the die surface, which can be highly compressive. As a result, if a crack initiates at the top corner of the die, it redistributes the forces acting on the die surface. The crack increase the shear stress acting near the edge of the die and the stress can change from compressive to tensile. The shear force can be represented graphically as shown in Figure 80.

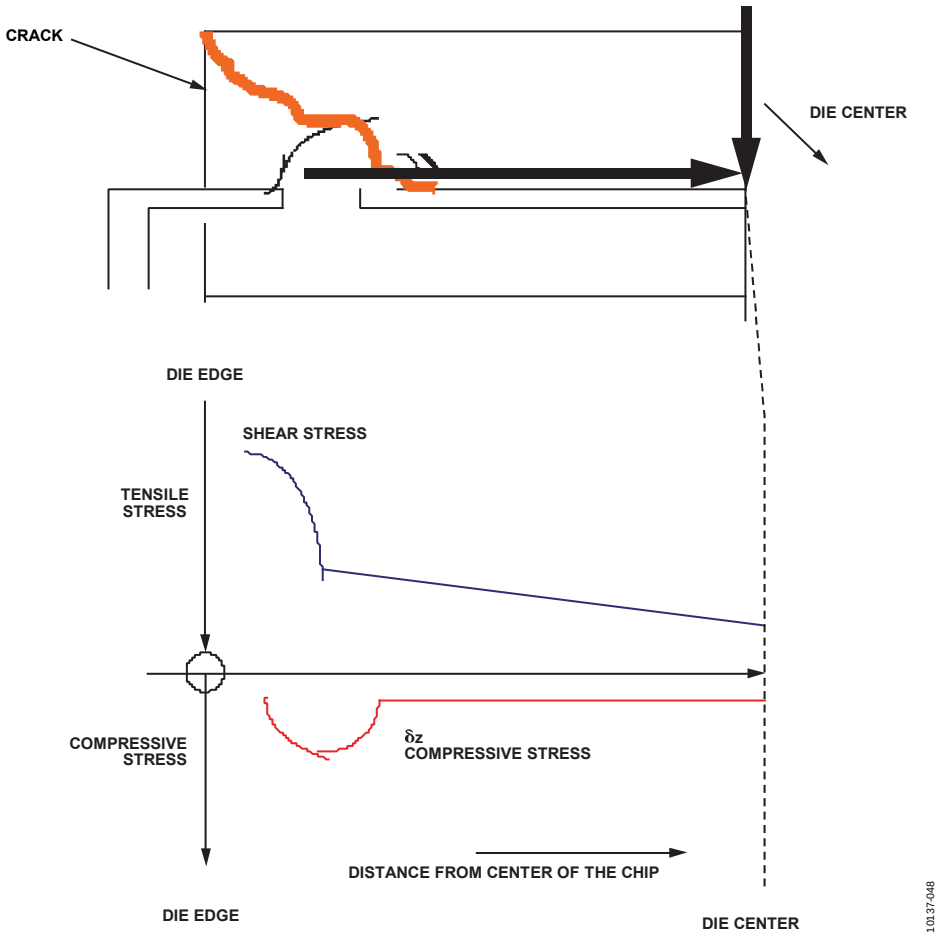

Figure 79. Die Stresses

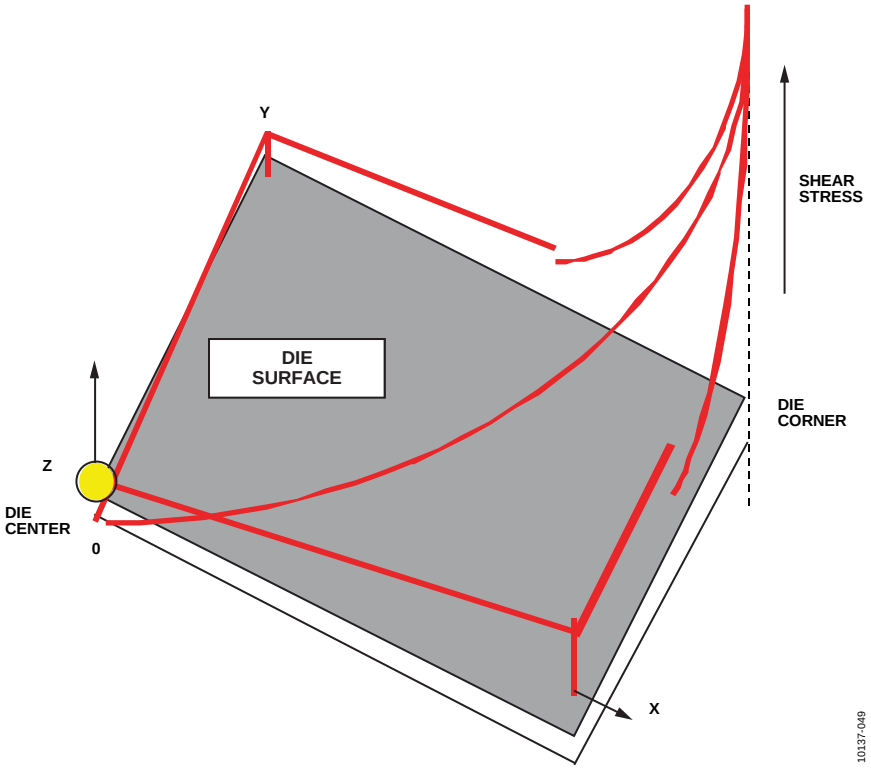

Figure 80. Shear Stress

WIRE BOND DAMAGE

Figure 80 shows the make up of the Au ball bond and the Au wire in the package. It shows the position of the wire relative to a potential crack in the package. The crack can be induced by a combination of moisture ingression and reflow solder, or initiated and propagated during temperature cycling or thermal shock testing.

The crack has intersected the wire and cracked it. The normal shear stresses on the ball are enhanced by delamination between the die and the plastic; the ball bonds may or may not shear depending on the stress experienced. Even if the bond does not shear, there may be sufficient stress to cause the Au wire to sever at the neck of the ball bond. This happens because the gold wire moves with the plastic while the ball bond is firmly attached to the die. The wire at the neck of the ball bond is particularly susceptible to damage since it has been annealed during the formation of the ball bond. This annealing generally leaves the neck of the wire at the ball bond thinner than the wire and, as a result, more susceptible to breaking.

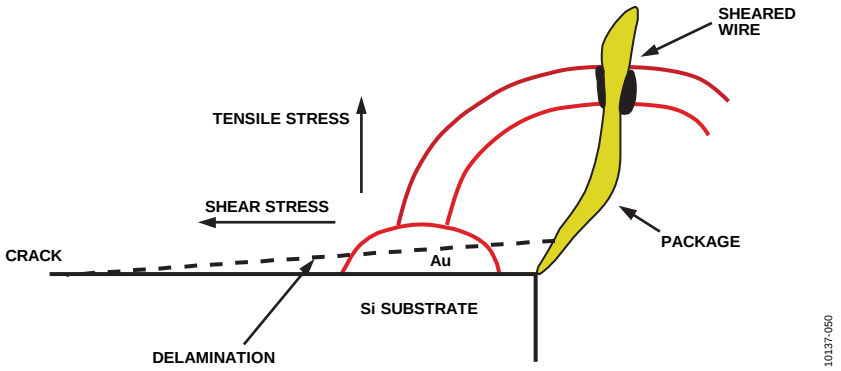

Figure 81. Bond Wire Shearing as a Result of Microcracks

This type of damage can also be compounded by additional damage such as cratering, discussed previously. Figure 82 shows the SEM shot of a bond pad where cratering has occurred during extensive thermal cycling testing. Figure 83 shows the ball bonds that have cratered while the Si is visible under the ball bond.

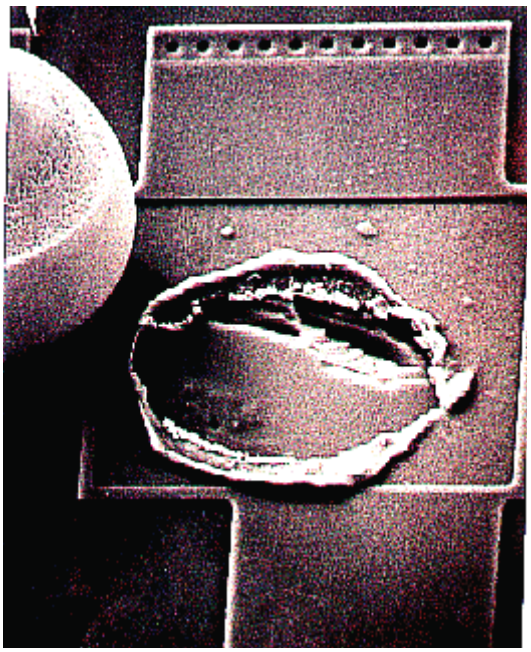

Figure 82. Bond Pad after Lifted Bonds During Extended Temperature Cycle

Figure 82 shows the ball bonds of this test chip lifted during an extended temperature cycling test. On decapsulation, the ball bond moved off the bond pad, leaving a crater exposed at the top. Figure 83 shows the underside of the bonds and the silicon visible under the lower bond.

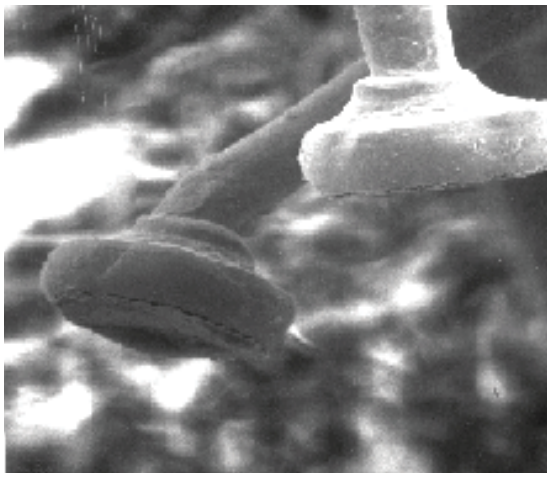

Figure 83. Lifted Ball Bonds after Extended Temperature Cycle

THIN FILM CRACKING

The shearing force exerted on the die by the package can damage thin film structures, particularly those situated at the edge of the die where the stress is highest. This is especially true in large area packages such as PLCCs. Most of the shear stress that is applied to the aluminum interconnect is through the passivation directly on top of the aluminum. The passivation cracks when the applied force exceeds its yield strength, and the aluminum deforms when the applied force through the passivation exceeds its yield strength. The failure mechanism is shown in Figure 84.

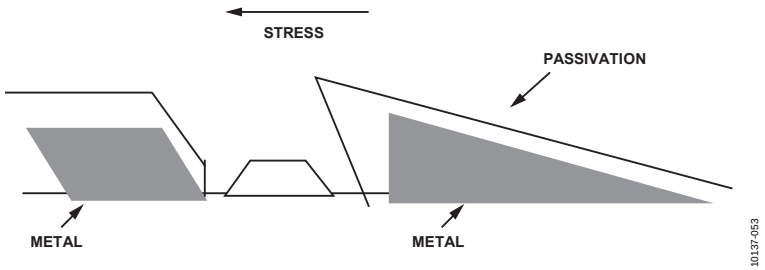

Figure 84. Metal Deformation Due to Shear Stress

The metal slides in the direction of the shear stress resulting in substantial deformation, bending of the metal tracks, and also deformation of the bond pad periphery metal. Figure 85 shows the resultant damage that occurred on a specifically designed test chip after extended temperature cycling.

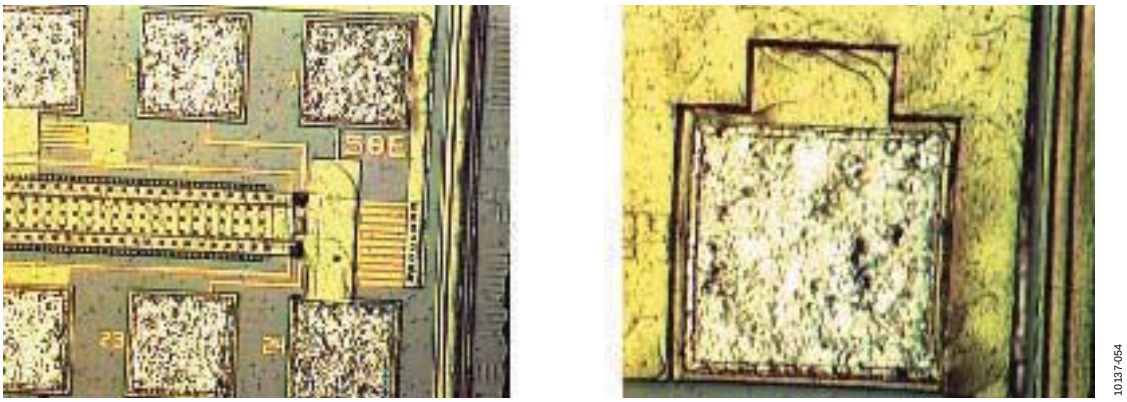

Figure 85. Metal Deformation as a Result of Shear Stress

The deformation lines can be clearly seen as can the bowing of the bond pad periphery at the edge of the die. The aluminum damage occurs more readily when there are very thick metal lines at the die edge because the stress on the lines is greater.

Localized aluminum deformation can also occur as a result of filler particles in the molding compound. This occurs when the compressive stress from the resin and a shear stress component are applied to a local area through the filler particles in the molding compound. This type of metal deformation is not particularly dependent on the location within the chip. Figure 86 shows the failure mechanism.

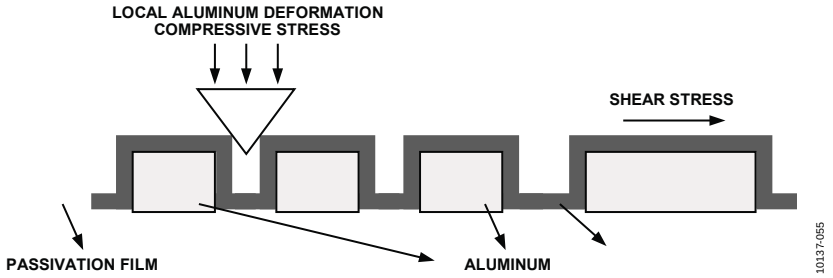

Figure 86. Metal Deformation Due to Filler Particles

Local aluminum deformation depends on the grain size filler. This is of concern as it has the ability to cause small, geometric metal lines to go open-circuit, resulting in device failure. Various factors that affect both types of thin film cracking are as follows:

- Die size
- Molding compound filler size used
- Type of molding compound used
- Width of aluminum tacks, that is, die design rules
- Use of die overcoats

In terms of thermal range of the thermal cycle or thermal shock based on the failure kinetics, Analog Devices has in place a comprehensive range of programs and practices aimed at preventing these failure mechanisms from being translated to the customers' applications. Analog Devices also supports comprehensive quality and reliability control procedures that strive to ensure these failure mechanisms do not occur in its qualified packages. Reliability test chips specifically designed with these and other potential failure mechanisms are used to characterize newer packages before any qualification begins. These test chips are used not only to characterize newer packages but also to evaluate and make changes to existing processes for packaging, assembly, and wafer fabrication.

BOARD-LEVEL RELIABILITY

INTRODUCTION

Handheld electronic devices have continued to proliferate across several market spaces, increasing pressure on semiconductor suppliers to provide integrated circuits (ICs) that meet the BLR demands of the device manufacturers.

Recognizing the importance of BLR performance, consortiums such as JEDEC and IPC have published standardized BLR test methods for industry compliance. At the same time, several key customers have produced test methods of their own, reinforcing the fact that BLR performance is now a competitive advantage for doing business in the handheld market.

In response to these market demands, Analog Devices has developed BLR assessment capabilities. These capabilities help Analog Devices to assess chip-scale packaging (CSP) technologies in advance of product deployments, reducing risk to product release and enhancing field reliability in customers' end applications. This section provides an overview of these capabilities.

For BLR testing, the ICs are soldered onto a printed circuit board, whereas the ICs are not soldered for component-level testing. When an IC is soldered onto a PCB, it is mechanically constrained to the plane of the PCB, resulting in stress and strain distributions and responses that are wholly different than those the IC would encounter if not soldered. Additionally, there may be unique fixturing and test hardware challenges associated with testing PCB-mounted parts, challenges not encountered during component level testing.

For this reason, and to facilitate the acquisition of real-time in-situ data, the devices used for BLR testing are daisy-chain devices. By accumulating and plotting the in-situ data, it is possible to show lifetime distributions, which can then be correlated to potential field-life estimates and statistical confidence intervals.

BLR testing addresses processes and materials that affect the interconnection of the IC to a printed circuit board, whereas component-level reliability testing addresses a broader range of failure mechanisms at the die and package levels.

The BLR test suite is run on each major CSP technology and technology change. The suite consists of four test regimes: solder joint reliability (SJR) test, mechanical shock/drop test, PCB bending test, and vibration test.

SOLDER JOINT RELIABILITY

SJR testing consists of temperature cycling per JEDEC JESD22-A104. The test specimens are PCB-mounted, daisy-chain devices (see Figure 87).

Figure 87. SJR Test Board

The temperature extremes to which the devices are subjected range from −40°C to +125°C at a rate of one cycle per hour (see Figure 88).

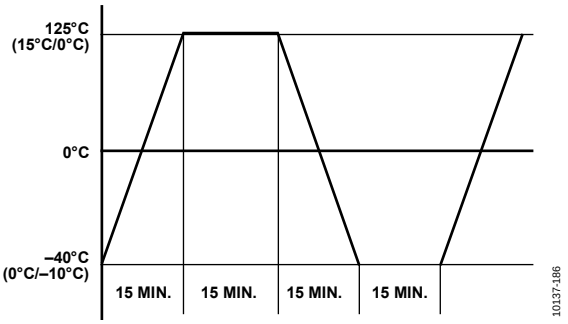

Figure 88. SJR Temperature Cycling Profile

Temperature cycling acts as an accelerated determination of the response of ICs in handheld devices when they are exposed to the extremes of temperature in use (left on a car dashboard, waiting for a bus in winter, and so on).

Failures at the interface where the daisy chain is soldered to the PCB are identified through physical failure analysis of devices, which are detected through in-situ monitoring. The failure mechanisms identified through failure analysis are compared to the lifetime distribution, which in turn provides targeting for process improvements.

MECHANICAL SHOCK/DROP TEST

In the mechanical shock/drop test, a PCB with daisy-chain devices soldered onto it is attached to a mass, which, in turn, is fixtured to a set of guide rails, which provides a drop path (see Figure 89 and Figure 90). The Bluelec drop test system is used in the BLR Lab at Analog Devices-Wilmington.

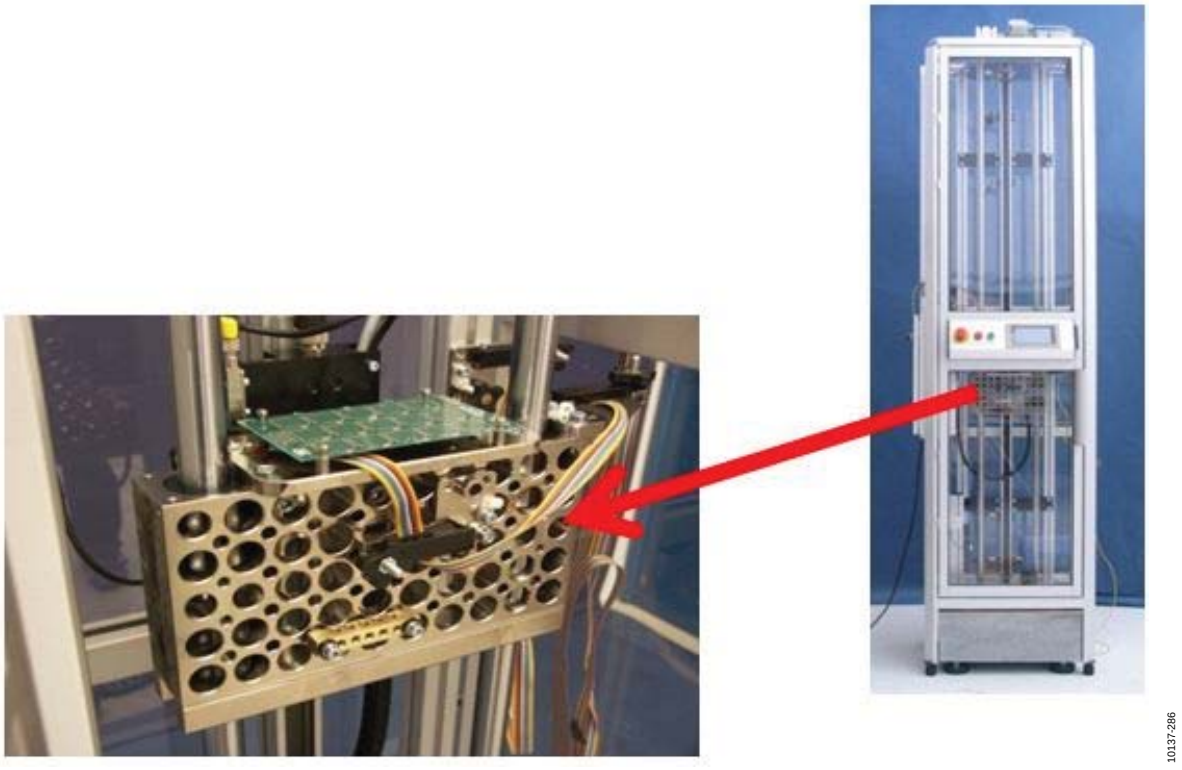

Figure 89. Bluelec Drop Test System

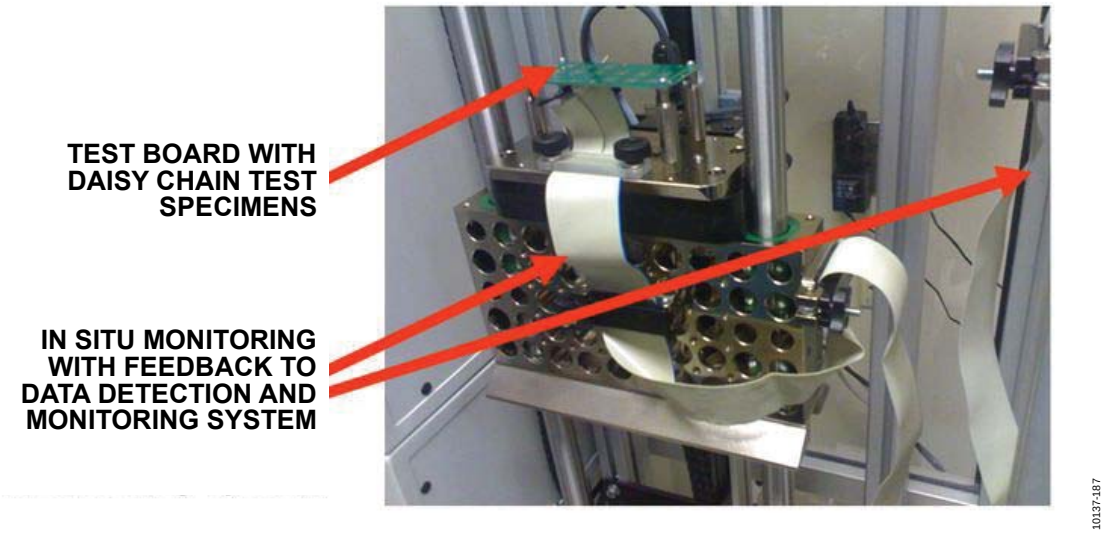

Figure 90. Mechanical Shock/Drop Test System

The drop height and mass are precalibrated to accelerate to 1500 *g* (as measured on the devices on the PCB).

The shock waveform is a ½-sine pulse with a 1500 *g* amplitude and 0.5 ms duration.

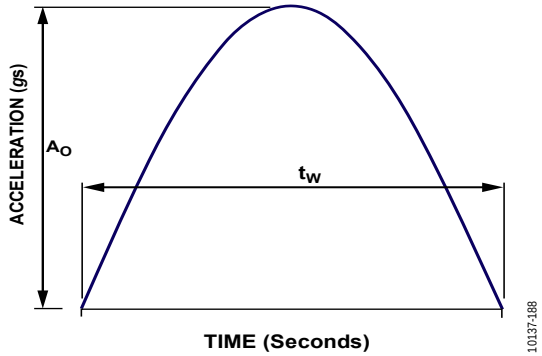

Figure 91. Mechanical Drop/Shock Profile

This shock level is prescribed by JEDEC Specification JESD22-B111, *Board-Level Drop Test Method of Components for Handheld Electronic Products*. The rationale for mechanical drop/shock is obvious to anyone who has ever dropped a device, such as a cell phone, SmartPhone, or PDA onto the floor, that is, the user wants the device to work after the drop.

As with SJR, the drop test setup features in-situ monitoring of the daisy-chained devices on the board so that a loss of continuity can be detected and logged.

Again, as in SJR, failures at the interface where the daisy chain is soldered to the PCB are identified through physical failure analysis of devices, which are detected through in-situ monitoring.

PCB BEND TEST

The solder joints of IC devices soldered to PCBs are subjected to strain due to flexure of the PCB during board assembly, PCB handling, and field use conditions. PCB bend testing allows Analog Devices to characterize the intrinsic fracture strength of the solder joints on Analog Devices CSPs, as well as to understand the strain rates and times to failure in use conditions.

PCB bend testing is conducted in accordance with IPC/JEDEC-9702, *Monotonic Bend Characterization of Board-Level Interconnects* and JEDEC JESD22-B113, *Board-Level Cyclic Bend Test Method for Interconnect Reliability Characterization of Components for Handheld Electronic Products*.

The PCB bend test method is fairly straight forward; daisy-chain devices with in-situ monitoring are attached to a PCB, which is then subjected to either a one-time bend-to-break (intrinsic strength) or cyclic bending to a lesser displacement. Figure 92 shows the test schema for PCB bend testing.

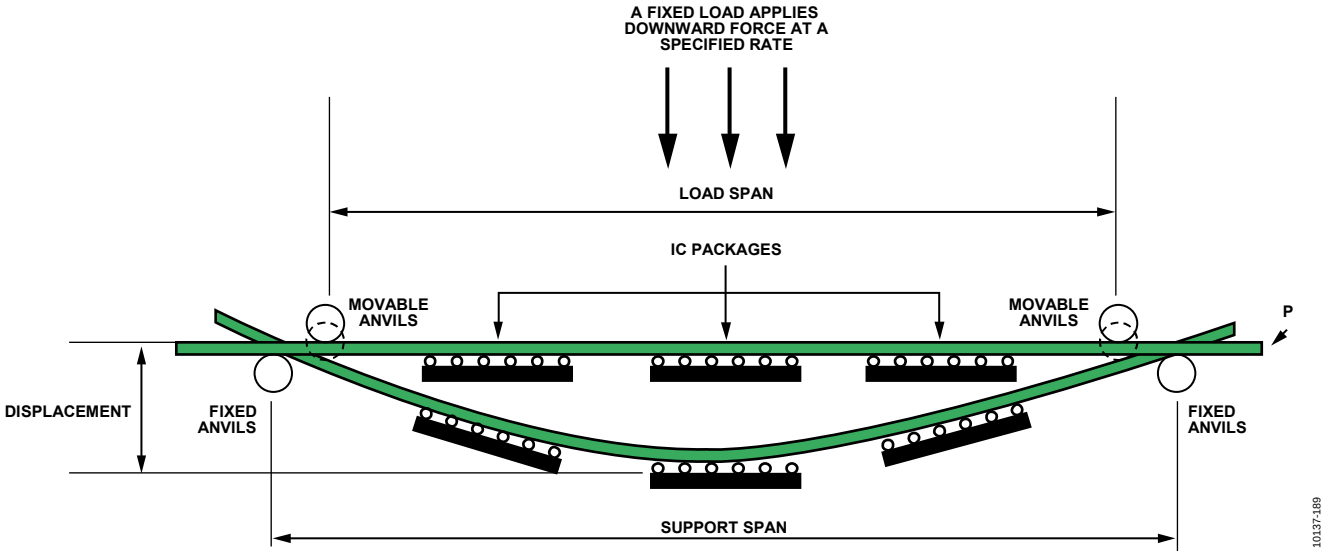

Figure 92. PCB Bend Testing Schema

The configuration shown is called four-point bending. This configuration results in a uniform stress level for all devices within the load span. Different stress levels are achieved by varying the load and support span lengths. Three-point bending is also available, and is achieved by using a single movable anvil to apply the downward force. Analog Devices uses the Instron 4455A bend tester for conducting PCB bend testing (see Figure 93).

Figure 93. Instron 4455A Bend Tester

As with the SJR and drop tests, failures from PCB bending are analyzed to root cause of failure. The resulting failure rates are categorized to determine reliability compliance levels.

VIBRATION TEST

The vibration test is the newest of the items in the BLR test suite. The vibration test was added to meet the demanding requirements of key commercial and automotive customers for both characterization and reliability testing of Analog Devices CSP and MEMS technologies. The rationale for vibration testing is straightforward. Electronic systems with Analog Devices parts may be subjected to application environments, such as automotive and industrial in which the electronic apparatus is subject to mechanical vibration. This vibration can in turn cause failures of weak solder joints.

The key operational specifications used for vibration testing reflect these application environments.

- MIL-STD-883G Method 2007.3 Condition B (50 g sweep from 20 Hz to 2000 Hz)—Standard Group D Vibration Test
- ISO 16750-3:2007 Test IV (Table 7) Automotive—Car (vibration and temperature)
- ISO 16750-3:2007 Test VII (Table 12) Automotive—Truck (vibration and temperature
- ISO 16750-3:2007 Test VII (Table 13) Automotive—Truck (vibration and temperature)

The system used at Analog Devices for vibration testing is the Thermotron DXS-2250 temperature vibration system shown in Figure 95.

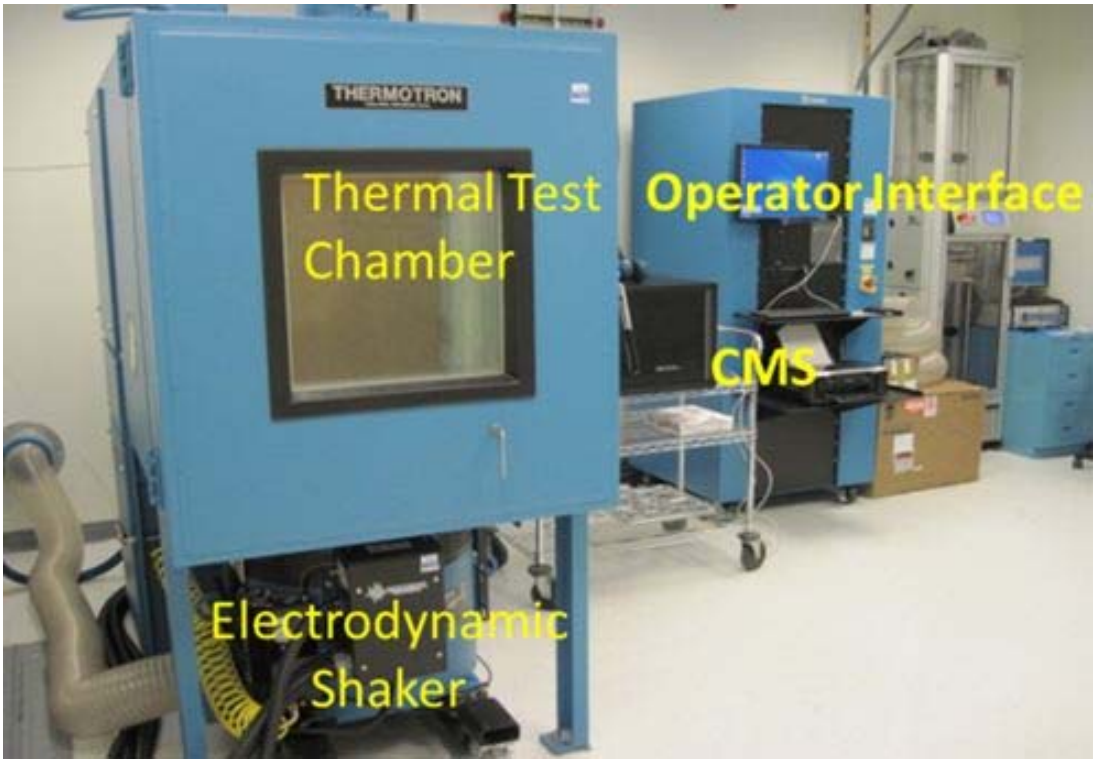

Figure 94. Thermotron DXS-2250 Vibration Tester

Figure 95. Thermotron DSX-2250 Temperature/Vibration System
–50 g Shock Profile Shown on Operator Interface

This system includes a continuity monitoring system (CMS) that allows continuous in-situ testing of test chips during test. In-situ monitoring of data is a prerequisite for the generation of failure distribution plots, which in turn give a quantifiable measure of the failures encountered during test as well as a statistical basis for their occurrence. Failures from vibration testing are subject to physical failure analysis to determine root cause and drive improvement cycles.

SUMMARY

Analog Devices performs extensive board-level reliability characterization testing of its CSP technologies to ensure that its products meet the stringent demands of the handheld marketplace.

MEMS RELIABILITY

Microelectromechanical systems (MEMS), also known as Microelectromechanical machines (MEMs), consist of tiny structures fabricated using semiconductor processing techniques. Applications of MEMS devices range from sensors and actuators to energy harvesters and microfluidic devices. The materials used for the structural layers are in many cases the same as those used in traditional semiconductor devices, and are primarily some form of silicon. Other materials used include gold and piezoelectric materials.

There are two fundamental strategies for fabricating MEMS devices: integrated MEMS and MEMS only. Integrated MEMS refers to processes in which the MEMS structure is formed on the same die as the signal conditioning circuitry. MEMS only refers to devices in which the MEMS structure is on a separate die from the signal conditioning circuitry. This distinction, however, is becoming more ambiguous as more complex forms of interconnect enable ASICs to be bonded directly to MEMS only die to form wafer scale packages. The fabrication processes used across the MEMS industry vary greatly.

MEMS devices are packaged using technologies ranging from hermetic ceramic packages to standard organic packages to wafer scale packaging. As with the different fabrication processes, each package and package/fabrication technology combination brings with it its own set of reliability considerations, such as thermal and moisture stress mechanisms and shock transmission.

While MEMS devices are manufactured using predominantly standard semiconductor fabrication and assembly processes, they bring with them their own set of reliability considerations [111 – 114]. Several MEMS process technologies and packaging solutions are in currently in use, each with their own subset of reliability considerations. Few industry standards are available to provide qualification planning guidance to manufacturers or users; therefore, MEMS failure mechanism based qualification planning must be employed, especially when qualifying design and process changes.

MEMS FAILURE MECHANISMS

MEMS devices are susceptible to a new set of failure mechanisms, in addition to traditional semiconductor mechanisms. Stiction and foreign material (that is, particles) are the most common mechanisms for MEMS devices with moving parts. Other mechanisms to be considered include

- Sensor breakage
- MEMS cap hermeticity loss
- Package stress
- Charge trapping
- Creep

Mechanisms such as creep and charge trapping are time dependent; however, most MEMS failure mechanisms are event driven. Mechanisms such as stiction and beam impediments require some event, usually mechanical shock, to occur.

Foreign Material

Foreign material, such as particles (see Figure 96) or residues, has historically been the most common failure mechanism for MEMS devices. Foreign material can obstruct proper MEMS function through mechanical impedance, electrical shorting, capacitance shifts, or electric field disruption. Foreign material obstruction affects inertial sensors in one or more of the following ways:

- Offset out of range: output of the device at rest is either above or below specifications
- Low or no self-test/sensitivity: sensitivity and self-test magnitude are out-of-specification low
- Offset hysteresis: output does not return to original value after shock or self-test actuation

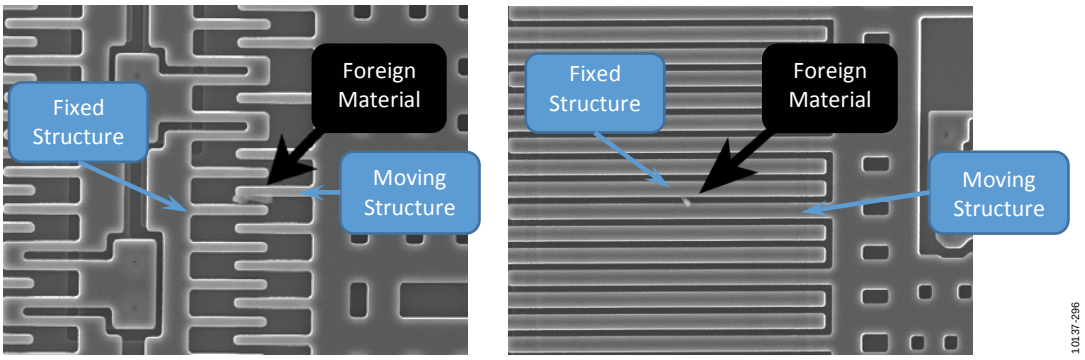

Figure 96. Foreign Material Impeding Sensor Motion

Foreign material is an event driven and probabilistic failure mechanism. For foreign material to cause a failure, it must be in a critical location within the structure that causes a failure. An event such as a mechanical shock of sufficient magnitude is required to move foreign material from a benign to a critical location. The mechanism is probabilistic in that, when moved by the event, the foreign material may or may not land in a critical area. Therefore, for a failure to occur; a shock must occur, the shock must be of sufficient magnitude to move the foreign material, and the foreign material must land in critical location (see Figure 97).

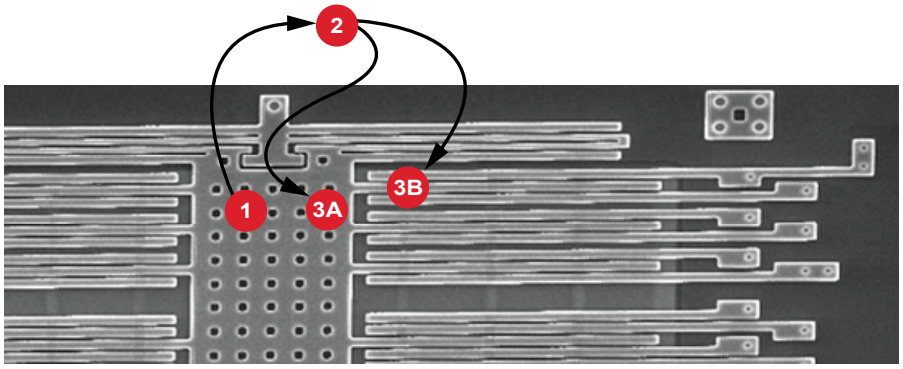

Figure 97. The Probabilistic Nature of the Foreign Material Failure Mechanism

Many factors constitute the probability of foreign material, such as a particle, moving; these factors include the magnitude of the mechanical shock event, the characteristics of the material, the characteristics of the substrate, the type of bonding mechanism, and environmental factors. As such, it is impossible to definitively answer the question of how many g's are required to move a particle. Typically, larger particles are more easily dislodged and are more likely to eventually land in a critical area of the structure. Similarly, higher g shocks are typically more likely to move particles. From a practical perspective, it is best to take proactive steps to minimize the possibility of the introduction of any foreign material contamination during fabrication, and likewise to minimize the exposure of MEMS devices to high g mechanical shocks during handling and processing. Failure due to foreign material is typically much more likely to occur during manufacturing than in the field.

The probabilistic nature of most foreign material failures makes this mechanism very difficult to assess during qualification testing. Most foreign material failures encountered during qualification testing are caused by an event outside of the stress test, such as handling. It is important to note that bare components can be exposed to shock events more often and of much higher magnitude than they are once they are mounted on a PCB and, ultimately, into a finished product. The occurrence of foreign material failures during qualification is not a good predictor of occurrence rates in use.

Stiction

Stiction occurs when a movable structure comes into contact with an adjacent structure, and the restoring force is insufficient to overcome attractive forces, such as electrostatics and surface forces. There are generally two types of stiction:

- Lateral stiction is the condition by which two adjacent structures stick together (Figure 98).
- Vertical stiction is the condition by which the beams stick to the substrate or cap stopper (Figure 99).

Stiction is also an event related mechanism and is often probabilistic. The causes of stiction include high g mechanical shock, capillary force due to moisture ingression or residue, or faulty or degraded antistiction coating. In some cases, stiction can be a fully reversible mechanism, leaving no permanent visible or electrical signature. The root cause of a particular stiction event can be difficult to determine; however, stiction that does not recover or that is easily repeatable with mild mechanical shock is more often due to an assignable cause, such as contamination, moisture, or inadequate antistiction coating, while stiction that recovers, but is not repeatable, is more often due to a mechanical overstress event. Stiction failures observed during qualification testing must be dispositioned carefully to distinguish between stress induced failure or failure due to an extraneous event.

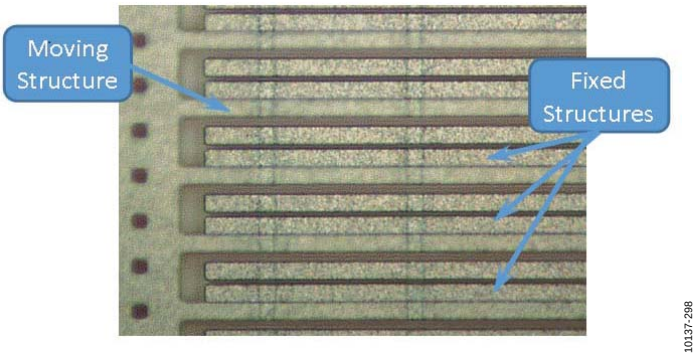

Figure 98. Lateral Stiction: Moving Structure is Stuck to Adjacent Fixed Structure

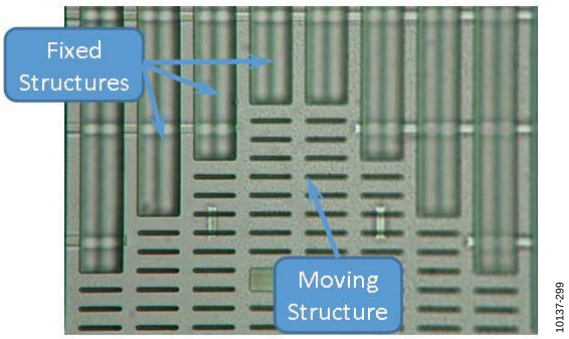

Figure 99. Vertical Stiction: Moving Structure is Stuck to the Substrate (Note Fixed Structures Out of Focus)

Other Mechanisms

Sensor Breakage

The robustness of MEMS devices to mechanical shocks is primarily design driven; however, defects in the MEMS structure or damage can cause increased susceptibility to breakage. Mechanical stresses are used to draw out breakage mechanisms, but temperature cycling can also accelerate crack propagation. Breakage is often the result of extremely high g levels. Fatigue and stress crack corrosion are also ways in which MEMS structures can fracture; however, these mechanisms are not common for silicon structures in hermetic environments.

MEMS Cap Hermeticity Loss

Devices packaged in overmolded packages require a sealed cap over the MEMS structure. Loss of cap hermeticity can cause parametric shifts due to changes to the sensor ambient gas viscosity, pressure changes, or excessive moisture ingress. Loss of MEMS cap hermeticity often results in stiction caused by capillary forces due to condensing moisture. Accelerated moisture stressing, biased or unbiased, can draw out hermeticity failures.

Package Stress

MEMS devices are often sensitive to package stress interactions, which can cause parametric shifting. Temperature cycling, preconditioning, moisture stresses, and high temperature storage can draw out various package stress mechanisms.

Charge Trapping

Charge trapping can affect electronic device performance, but also can cause mechanical effects to the MEMS structure due to electrostatic deflection. Charge trapping can result in parametric shifting or lower actuation thresholds. Biased stresses, such as high temperature operating life (HTOL), draw out this mechanism.

Creep

The creep failure mechanism is the accumulated effect of plastic deformation under thermal and/or mechanical loads, or cyclic strain damage during thermal and/or mechanical load cycling. Creep is the most common wear out mechanism for solder joints, but also can cause distortion of MEMS structures that can affect parametric performance. Creep is especially important to consider for MEMS devices constructed of ductile metals. Creep is not a significant risk for silicon based structures. Temperature cycling with extended soak times or high temperature storage can draw out this mechanism. Accelerated moisture stresses can draw out creep mechanisms outside of hermetic environments.

QUALIFICATION PLANNING

The qualification planning for new MEMS products can be relatively straightforward. Many of the standard semiconductor qualification stresses also draw out MEMS failure mechanisms. Moisture stresses, for example, draw out MEMS cap hermeticity problems. Standard semiconductor qualification testing can be employed and augmented with mechanical stresses to draw out shock related failure mechanisms. While there are currently no industry standards for MEMS qualification, Analog Devices has focused on a suit of key mechanical stresses for qualification testing.

Handling of MEMS devices often requires some level of caution, although more and more of today's MEMS products can survive very high g shock levels. Shock related mechanisms encountered during qualifications require scrutiny to determine whether they were induced by the stress, handling, or fixturing. Some industries also have qualification requirements, often based on macromechanical technologies that the MEMS technology is displacing. These requirements should be discussed during the planning process, as they often add little value or added assurance.

Planning for the qualification of design and process changes are less straightforward than for new products. For example, semiconductor industry standards typically call for HTOL, ESD, and latch-up for mask changes; however, these stresses are most likely not appropriate for changes only affecting the MEMS sensor layout. MEMS sensor changes require consideration for shock related mechanisms rather than intrinsic dielectric breakdown. Similarly, MEMS process changes should be reviewed to identify potential MEMS related mechanisms, such as increased stiction susceptibility, hermeticity loss, stress interactions, or exposure to contaminants that can become sensor impediments. Given the variety of MEMS processes and packaging technologies available across the MEMS industry, it is difficult to standardize these types of qualification requirements; therefore, failure mechanism based qualification planning should be employed.

MEMS RELIABILITY TESTS

Powered Mechanical Shock

Powered mechanical shock is performed on devices mounted on carrier boards using a guillotine drop test fixture (see Figure 100). The drop height and base material can be varied to derive various shock pulse amplitudes and durations. The amplitude is typically the absolute maximum rating for the individual device and is, therefore, product specific. Stiction, breakage, and package integrity (especially cavity packages) are the primary failure mechanisms associated with this test. Power is applied during this test to introduce electrostatic forces, which couple with the mechanical forces to draw out stiction. It is important to note that it is not possible to perform testing at all possible amplitudes and durations; therefore, any shock profiles that are critical to an application mission profile should be explicitly specified and qualified.

Figure 100. Guillotine Powered Mechanical Shock Test Fixture

When setting up mechanical shock testing, whether powered or unpowered, take care to ensure that proper measurement equipment and techniques are applied. The reference accelerometer used to measure the shock amplitude and pulse width must be as close as possible to the device under test. The reference accelerometer must have sufficient headroom to measure high g shocks, and must have a high enough measurement bandwidth. The data acquisition and signal conditioning equipment must also have sufficient bandwidth. These requirements are particularly important for shocks involving hard materials, such as metal on metal or metal on ceramic. These shocks produce significant energy at high frequencies that can be ignored by low bandwidth measurement setups. The shock can result in overstresses of the device under test, which in turn can result in false failure. This effect is illustrated in Figure 101, which displays the shock amplitude resulting from 38 mm guillotine drops of a metal block on the metal base, and the same metal block on torlon. The metal on torlon drop produced a low amplitude, wide pulse-width shock that can be accurately measured with a measurement bandwidth as low as 6.4 kHz. The metal on metal shock with the same setup, however, only shows roughly 30% of the total shock amplitude measured with a bandwidth of 51 kHz.

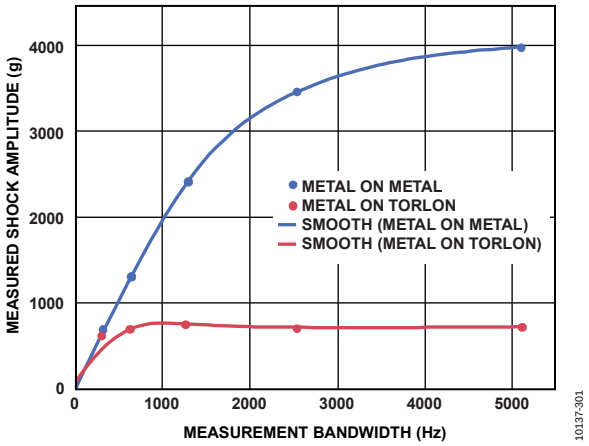

Figure 101. Shock Amplitude vs. Analysis Bandwidth, 38 mm Drop Height

Mechanical Sequence: Unpowered Mechanical Shock, Variable Frequency Vibration, and Constant Acceleration

The mechanical sequence test was originally developed to validate hermetic package integrity and includes a 1500 g, 0.5 ms unpowered mechanical shock (6 axis), 50 g variable frequency vibration (20 Hz to 2 kHz), and 30,000 g constant acceleration (Y1 orientation only). For hermetic packages, this was followed by fine and gross leak testing. This testing was adopted for MEMS devices to demonstrate mechanical robustness. Inertial sensors with especially large mass or low resonant frequencies are stressed at a lower constant acceleration of 10,000 g to avoid overstress. In addition to cavity package integrity issues, this stress draws out stiction and breakage related failure mechanisms.

Other unpowered mechanical shock testing can be performed as required for certain end applications. For example, lower amplitude, wider pulse-width testing can be performed to simulate a car door slam. Other sine vibration or random vibration tests are also performed as required. Random vibration profiles apply to conditions such as truck cargo or gear friction, while sine vibration applies to conditions near engines or motors. ISO-16750-3 is a good reference for mechanical profiles for automotive applications [115]. It is not possible to perform testing at all possible mechanical load conditions; therefore, any shock and/or vibration profiles that are critical to an application mission profile should be explicitly specified and qualified.

Random Drop Test or Guided Drop Test

Random and/or guided drop tests are often requirements for end applications, especially hand held consumer devices. Therefore, these requirements are often carried over to the component level qualification plans. Random drop is simply dropping an individual device from a specified height, 1.2 meters by default, onto concrete multiple times. Guided drop uses a piece of equipment to control the orientation of the device upon contact.

The random and guided drop tests impart much higher shock amplitudes than are specified in device data sheets. The shock amplitudes from these tests are also typically much higher than those imparted to modules into which the devices are assembled during the same drop condition. Therefore, failures encountered during this test are not necessarily grounds to automatically fail qualification. Drop testing with the device mounted to a test coupon can be used as a referee, or additional shock characterization can be performed that are specific to the application. Drop testing on coupons can also be performed when the devices are too small to be reasonably handled, or for packages that have more sensitive leads.

Tumble Testing

Tumble testing is a method by which devices are subjected to multiple random drops using a rotating chamber with a hard surface on either end, typically 1 m in length. This test is sometimes required for hand held or portable consumer electronics applications and simulates handling in use.

SUMMARY

There are several MEMS process and package solutions, each with their own reliability considerations. MEMS devices introduce a new set of failure mechanisms in addition to traditional semiconductor device failure mechanisms. It is important to consider the specific process and package being qualified to ensure coverage for all failure mechanism susceptibilities, as well as consideration for end application(s), if known.

Additional information about Analog Devices MEMS devices and technology can be found in the following links:

- MEMS Web Page
- MEMS Sensors Video Channel
- Basic MEMS Terminology

ELECTRICAL OVERSTRESS

INTRODUCTION

Electrical overstress (EOS) has historically been one of the leading causes of IC failure, regardless of the semiconductor manufacturer. In general terms, electrical overstress is defined as any condition where one or more pins on an IC are subjected to current and/or voltage levels that exceed the Absolute Maximum Ratings per the IC data sheet. The result of an EOS event varies with the energy and duration of the event, and can range from no damage, to failing electrical behavior, or catastrophic damage where severe electrical and physical damage can result. EOS covers the broad spectrum of overvoltage/overcurrent events. It includes electrostatic discharge (ESD), latch-up (LU), power-up/power-down supply transients, and excessive dc current/voltage levels. ESD is the subset of EOS generally describing events less than 1 µs in duration. Analog Devices recognizes the need to design ICs that are robust to all forms of EOS to maximize reliability in customer applications.

ESD DEFINITIONS

Electrostatic Discharge

Electrostatic discharge (ESD) is the current that results from the transfer of charge between two objects at different electrostatic potentials. The transfer of charge to an IC can be tribolectric (friction) between two dissimilar materials, or it can be induced by an external electric field. The resulting discharge when an IC or IC path is discharged to ground is characterized by a short duration (sub sec) high amplitude current and voltage pulse, which exceeds the Absolute Maximum Rating voltage.

ESD Pass Voltage

The ESD pass voltage of a particular ESD test model is the highest voltage level at which all pins can be subjected to ESD events of that model with the device passing all data sheet test limits during subsequent electrical testing.

ESD MODELS/TEST METHODS

Overview

Failure analysis (FA) at Analog Devices on ICs with ESD failure signatures has consistently shown that the vast majority can be simulated by either the charged device model (CDM) or the human body model (HBM). All Analog Devices products (including major product revisions) are tested to the CDM and HBM test methods prior to release.

A third ESD model referenced in the semiconductor industry as the machine model (MM) corresponds to a nonrealistic worst-case human body model. Analog Devices and industry studies have shown that real-world ESD events do not correlate to the MM; therefore, Analog Devices does not place significant emphasis on this model. However, limited in-house MM testing and subsequent FAs have shown that the failure signature for HBM and MM simulations are highly correlated. Therefore, Analog Devices design rules and proprietary design techniques for achieving CDM and HBM ESD robustness also guarantee MM ESD robustness.

Human Body Model (HBM)

The human body model is the oldest and best-known ESD model. This model first gained acceptance in the semiconductor industry in the late 1960s as a method for simulating failures of junction field effect transistors (JFETs) used in the flight control computer of the United States' Titan III Space Program. The model consists of a simple series RC circuit with the values of R and C selected to simulate the discharge from the fingertip of a standing person that touches an IC. Although the HBM was used extensively during the 1970s, lack of consensus on a standard for test systems (in particular, what values of R and C to use) resulted in poor correlation between HBM thresholds measured using different ESD test systems.

Correlation between testers greatly improved after MIL-STD-883 Method 3015 *Electrostatic Discharge Sensitivity Classification* was released in 1979 [99]. This HBM test method specifies an RC network of R2 = 1500 Ω and C1 = 100 pF, as shown in Figure 103. The current industry standard using this model is the ANSI/ESDA/JEDEC JS-001 HBM standard. Real-world RC values vary considerably from person-to-person and are a function of many variables, including the person's clothing, shoes, position, and surroundings. Consequently, the 1500 Ω/100 pF model should be considered more of a benchmark than a true model for discharges from people's fingers. As shown in Figure 103, capacitor C1 is charged via a high voltage generator in series with a resistor R1. When the high voltage relay S1 is switched, the charged capacitor, C1 (with a voltage of VESD), is discharged as current IESD through the series combination of discharge resistor R2 and the device under test (DUT). The peak value of IESD is given by

$$I_P = V_{ESD}/(R_2 + R_{DUT}) \quad (15)$$

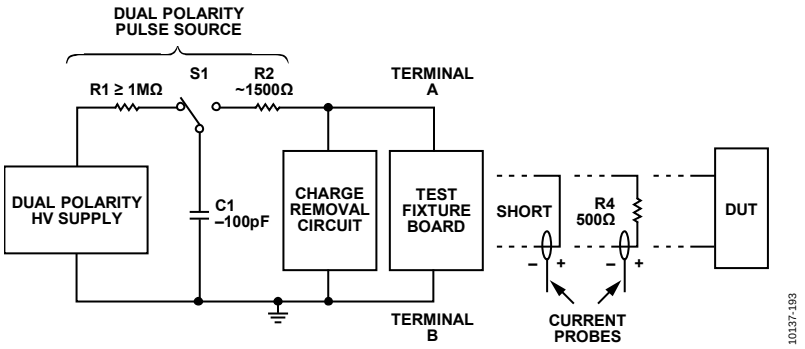

Figure 102. HBM ESD Test Circuit (Excerpted from ANSI/ESDA/JEDEC JS-001-2011)

In Figure 102, R1 = 10^6 Ω to 10^7 Ω,C1 = 100 pF ±10% (insulation resistance 1012 minimum); R2 = 1500 ± 1% Ω; S1 is the high voltage relay (bounceless, mercury wetted, or equivalent); and S2 is the normally closed switch (open during discharge pulse and capacitance measurement).

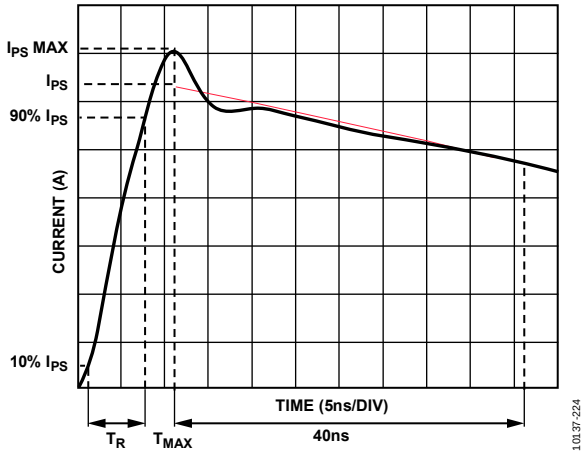

Figure 103. Current Waveform Through a Shorting Wire (I_{PS} MAX)
HBM ESD Short-Circuit Current Waveform (Excerpted from ANSI/ESDA/JEDEC JS-001-2011)

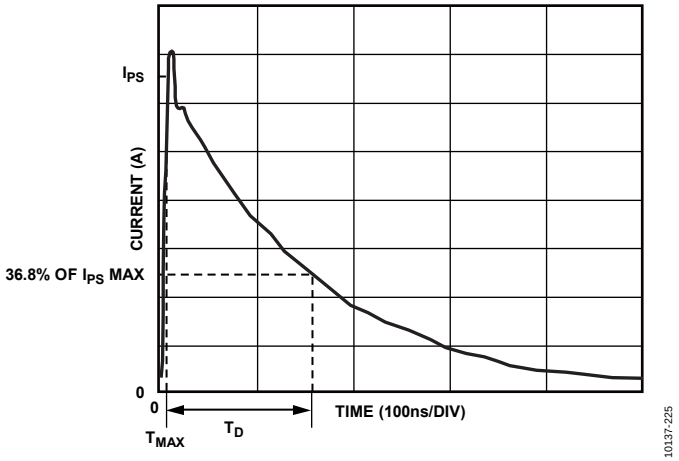

Figure 104. Current Waveform through a Shorting Wire (t_D)
HBM ESD Short-Circuit Current Waveform (Excerpted from ANSI/ESDA/JEDEC JS-001-2011)

The current pulse shall have the following characteristics:

- T_{RISE} (rise time) <10 ns
- Tdi (delay time) 150 ± 20 ns
- I_P (peak current) within ±10% of the I_P value shown in Table 11 for the voltage step selected
- Ir (ringing) the decay is smooth, with ringing, break points, double time constants, or discontinuities less than 15% I_P maximum, but not observable 100 ns after start of the pulse.

The HBM ESD test circuit in Figure 102 essentially acts as an ideal current source that injects current into the DUT. Figure 103 shows the ESD current, I_{ESD}, vs. time when the DUT is a short circuit (R_{DUT} = 0). This HBM ESD waveform has a characteristic double exponential shape, with a rise time typically in the 6 ns to 8 ns range and a fall-time of $\tau = R2 \times C1 = 1500 \times 100$ pF = 150 ns.

Table 11 shows the peak HBM ESD current, I_P, into a short circuit (R_{DUT} = 0 Ω) for the typical minimum set of stress voltages used to classify the HBM ESD robustness of Analog Devices products. Substituting R_{DUT} = 0 Ω into Equation 15, $I_{P(0\ \Omega)} = V_{ESD}/R_2$, or $I_{P(0\Omega)} = V_{ESD}/1500$.

Therefore, for a 1000 V HBM event into a short circuit, $I_{P(0\ \Omega)}$ = 1000 V/1500 V or 0.67 A.

Table 11. Analog Devices HBM ESDS Testing Stress Levels and Associated Classifications

Stress Voltage	Peak Current, I_P (±10%)	Sample Size	Corresponding HBM ESDS Classification for any Electrical Failures at this Stress Voltage
±500 V	±0.33 A	3	Class 1
±1000 V	±0.67 A	3	Class 1
±1500 V	±1.00 A	3	Class 1
±2000 V	±1.33 A	3	Class 1
±2500 V	±1.67 A	3	Class 2
±3000 V	±2.00 A	3	Class 2
±3500 V	±2.33 A	3	Class 2
±4000 V[1]	±2.67 A	3	Class 2

[1] If all samples pass following stress testing through 4000 V, the HBM ESDS classification is Class 3.

Analog Devices follows the ESD Association/JEDEC Joint HBM document ANSI/ESDA/JEDEC JS-001 [100].

ANSI/ESDA/JEDEC JS-001 also provides waveform specifications for a 500 Ω load. This provides for a more realistic evaluation of the ESD test system because DUTs obviously have finite (nonzero) resistance during stress testing. Substituting R_{DUT} = 500 Ω into Equation 15, $I_{P(500\ \Omega)} = V_{ESD}/(R_2 + R_{DUT})$. Therefore, for a 1000 V HBM event into a 500 Ω load, $I_{P(500\ \Omega)}$ = 1000 V/(1500 Ω + 500 Ω) or 0.50 A. As shown in Table 12, the rise time of the ESD current waveform is slower when R_{DUT} = 500 Ω than when R_{DUT} = 0 Ω.

Table 12. Significant Differences Between Industry HBM ESD Specifications

Test Parameter	ANSI/ESDA/JEDEC JS-001
Rise Time into a Short Circuit	2 ns to 10 ns
Rise Time into a 500 Ω Load	5 ns to 20 ns (for V_{ESD} = 500 V)
Number of pulses per pin combination in Figure 105	1 positive + 1 negative
Failure criteria	Testing to data sheet limits (both functional and parametric)

IMPORTANCE OF UNDERSTANDING PIN COMBINATIONS ZAPPED

Analog Devices conducts HBM ESD classification testing on all new or redesigned products as described in ANSI/ESDA/JEDEC JS-001. During this testing, one positive and one negative discharge (zap), each 0.3 sec to 1.0 sec apart, is applied to all the pin combinations specified in Table 13. HBM testing is typically conducted at ±500 V, ±1000 V, ±1500 V, …±4000 V, with three new samples used at each stress voltage level.

Table 13. Pin Combination Groups for HBM ESD Testing at Analog Devices

Group	Connection to Terminal A in Figure 102	Connection to Terminal B in Figure 102
1	Each pin one at a time (other pins floating)	Power Supply 1
2	Each pin one at a time (other pins floating)	Power Supply 2
n	Each pin one at a time (other pins floating)	Power Supply n
N + 1	Each nonsupply pin one at a time	All other nonsupply pins as a group

In Table 13, each power supply (1, 2, … n) is the pin or group of pins that are shorted-together by metal either on-chip or in the IC package to form a unique power supply group. For example, if two V_{DD} pins are not shorted together by metal, these two pins are treated as separate power supply pins. To illustrate the application of Table 13, consider the AD724 RGB to NTSC/PAL encoder. As indicated by the pinout in Figure 105, this product has n = 4 distinct power supplies: APOS, DPOS, AGND, and DGND. During HBM ESD classification testing, the AD724 is subjected to a total of 144 zaps (72 positive zaps, 72 negative zaps) using the 72 pin combinations shown in Figure 105. Note that all pins not connected to Terminal A or Terminal B are left floating.

Semiconductor companies other than Analog Devices may not be as stringent about the pin combinations zapped during HBM ESD testing. Using the AD724 example, some companies might treat the APOS and DPOS supplies as a single positive supply pin group, and likewise treat the AGND and DGND supplies as a single GND pin group. By grouping the supplies together in this manner, the AD724 is only be subjected to a total of 84 zaps (42 positive zaps, 42 negative zaps). Moreover, if the APOS pin has effective on-chip ESD protection and the DPOS pin does not, grouping these two pins together during zapping hides the weakness of the DPOS pin. Therefore, such testing can potentially result in a significantly higher HBM ESD pass voltage than would be obtained with Analog Devices' more stringent testing. This higher pass voltage can provide the user with a false sense of security when using the product in an environment with static problems.

PIN	TERMINAL A	TERMINAL B
1	STND	APOS
2	AGND	APOS
3	FIN	APOS
4	ENCD	APOS
5	RIN	APOS
6	GIN	APOS
7	BIN	APOS
8	CRMA	APOS
9	COMP	APOS
10	LUMA	APOS
11	SELCT	APOS
12	DGND	APOS
13	DPOS	APOS
14	VSYNC	APOS
15	HSYNC	APOS

PIN	TERMINAL A	TERMINAL B
16	STND	DPOS
17	AGND	DPOS
18	FIN	DPOS
19	APOS	DP OS
20	ENCD	DPOS
21	RIN	DPOS
22	GIN	DPOS
23	BIN	DPOS
24	CRMA	DPOS
25	COMP	DPOS
26	LUMA	DPOS
27	SELCT	DPOS
28	DGND	DPOS
29	VSYNC	DPOS
30	HSYNC	DPOS

PIN	TERMINAL A	TERMINAL B
31	STND	AGND
32	FIN	AGND
33	APOS	AGND
34	ENCD	AGND
35	RIN	AGND
36	GIN	AGND
37	BIN	AGND
38	CRMA	AGND
39	COMP	AGND
40	LUMA	AGND
41	SELCT	AGND
42	DGND	AGND
43	DPOS	AGND
44	VSYNC	AGND
45	HSYNC	AGND

PIN	TERMINAL A	TERMINAL B
46	STND	DGND
47	AGND	DGND
48	FIN	DGND
49	APOS	DGND
50	ENCD	DGND
51	RIN	DGND
52	GIN	DGND
53	BIN	DGND
54	CRMA	DGND
55	COMP	DGND
56	LUMA	DGND
57	SELCT	DGND
58	DPOS	DGND
59	VSYNC	DGND
60	HSYNC	DGND

PIN	TERMINAL A	TERMINAL B
61	STND	ALL OTHER I/Os
62	FIN	ALL OTHER I/Os
63	ENCD	ALL OTHER I/Os
64	RIN	ALL OTHER I/Os
65	GIN	ALL OTHER I/Os
66	BIN	ALL OTHER I/Os
67	CRMA	ALL OTHER I/Os
68	COMP	ALL OTHER I/Os
69	LUMA	ALL OTHER I/Os
70	SELCT	ALL OTHER I/Os
71	VSYNC	ALL OTHER I/Os
72	HSYNC	ALL OTHER I/Os

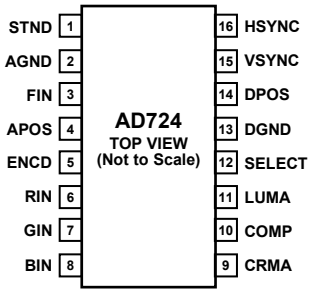

Figure 105. AD724 Pin Configuration and 72 Pin Combinations Zapped During AD724 HBM ESD Testing

CHARGED DEVICE MODEL (CDM)

The charged device model originated at AT&T in 1974 as a new ESD model to simulate field failure damage that could not be simulated by HBM testing [101]. Conceptually, the CDM represents the DUT being the source of charge, with the discharge taking place through any one pin of the DUT to ground. This model assumes the IC package is charged either directly via the triboelectric effect (that is, via frictional contact with other material) or indirectly due to an external electric field. One or more package pins (for example, leads and solder balls) subsequently contact a conductive surface at or near ground potential. This causes the charge stored on the die and associated conductive materials in the package (for example, the bond wires and lead frame) to be dissipated in an ultra-fast spark discharge. The discharge is almost instantaneous due to the low resistance (typically ~1 Ω) and low inductance (typically only a few nH) of these conductive materials in the package.

Typical examples of triboelectric charging followed by a CDM discharge include

- ICs are charged by sliding down an automatic test equipment (ATE) handler chute and then corner pins discharge to a grounded stop pin.
- ICs are charged by sliding down a plastic shipping tube, and then corner pins discharge to a grounded bench mat.

Typical examples of external field induced charging followed by a CDM discharge include

- Rubber rollers in laser marking equipment generate a high electric field that induces charge on ICs. Corner pins then contact and discharge to a grounded stop pin.
- Cover tape is quickly removed from tape-and-reeled ICs during automated PCB assembly operations, thus creating a high electric field that induces charge on ICs. Pin(s) on each IC are then discharged when they subsequently contact conductive traces on the PCB.

The charged device model is highly effective at simulating ESD damage induced by automated equipment and automated shipping/handling. Automated equipment and IC packing materials can be designed to minimize charging, such as by using grounded conductive rubber rollers, antistatic shipping tubes, and antistatic tape-and-reel cover tape in the above examples. The amount of charging is also a function of numerous environmental variables. For example, charging decreases rapidly with increasing humidity and air ionization levels. However, no matter what precautions are taken, some degree of charging always occurs when an IC package contacts and moves over a dissimilar material. In fact, due to the automation of IC and PCB manufacturing operations, CDM ESD is now recognized as the primary real world model for ESD events, being more prevalent than HBM ESD damage in the semiconductor industry [102]. Therefore, Analog Devices places heavy emphasis on designing ICs that are robust to CDM events as well as HBM events.

CDM testing can be conducted with the device resting on a field plate, which may be tied to ground or driven to a voltage to induce charge onto a device. This device capacitance can be charged either directly using a charging probe or indirectly using a charging field plate. The latter option, referred to as field induced charged device model (FICDM) testing, is the basis for the Analog Devices CDM classification program. As indicated in Figure 106, after the DUT is charged to the desired stress voltage (positive or negative) using the field plate, the robotic pogo probe is used to discharge each pin through the 1 Ω resistor to ground.

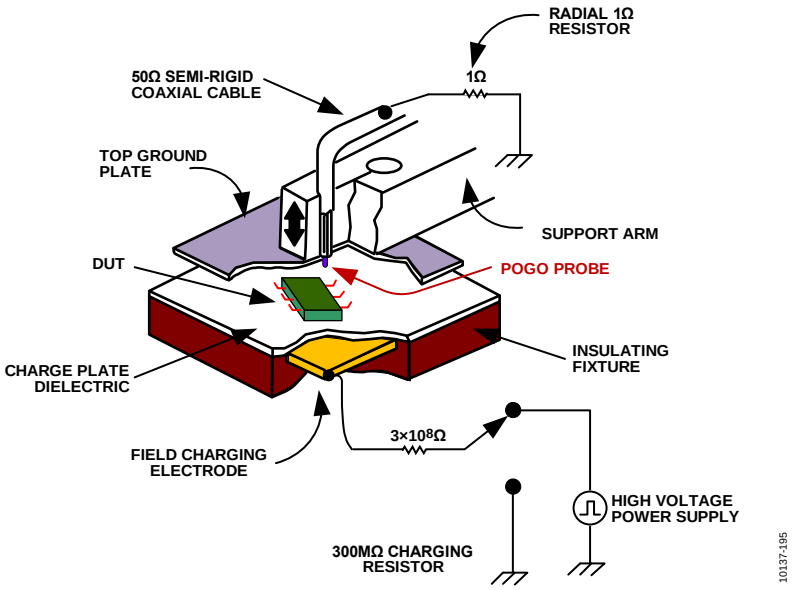

Figure 106. Field Induced CDM ESD Test Circuit (Excerpted from JEDEC Test Method JESD22-C101)

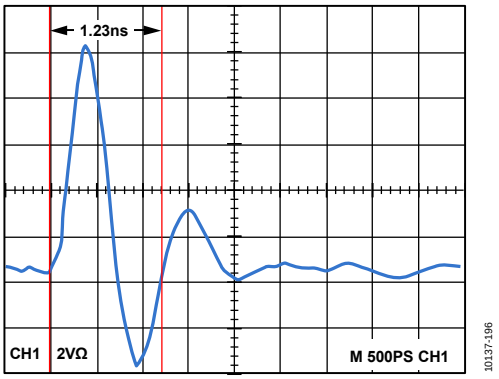

Figure 107. Field-Induced CDM ESD Current Waveform for a +250 V Discharge, Using a 30 pF Test Module and 3 GHz BW Oscilloscope (10 GS/s Sampling Rate); Note a Vertical Scale of 2 V/div Through a 1Ω resistor = 2 A/div, I_{PEAK} ≈ 9.6 A, and a Horizontal Scale of 500 ps/div, T_{RISE} (10% to 90% I_{PEAK}) ≈ 200 ps.

For a 4 pF test module (C_D = 4 pF) and a 1 GHz oscilloscope, Table 14 shows the peak FICDM ESD current, I_P, through the 1 Ω discharge resistor for the typical minimum set of ESD stress voltages used to classify the FICDM robustness of Analog Devices products.

Table 14. Analog Devices CDM ESDS Testing Stress Levels and Associated Classifications

Stress Voltage	Peak Current, I_P (±20%)[1]	Minimum Sample Size	Corresponding CDM ESDS Classification for any Electrical Failures at this Stress Voltage
±125 V	±1.13 A	3	Class C1
±250 V	±2.25 A	3	Class C2
±500 V	±4. 5 A	3	Class C3
±1,000 V	±9.0 A	3	Class C4
±1500 V[2]	±13.5 A	3	Class C5

[1] This peak current is measured using a 4 pF test module and a 1 GHz bandwidth measuring system.
[2] If all samples pass following stress testing through ±1,500 V, the FICDM ESDS classification is Class C6.

The CDM waveform replicates the fastest known real-world ESD event. Figure 107 shows the ESD current, I_{ESD}, vs. time when a 30 pF calibration module charged to +250 V is discharged through R = 1 Ω to GND. Note the extremely fast rise time and very short total duration of the CDM ESD event. The measured rise time using a 3 GHz oscilloscope is approximately 200 ps, and the entire discharge event is over in approximately 2 ns. In comparison, the duration of an HBM event is approximately a hundred times longer, as shown in Table 14. The true rise time of a CDM ESD event is unknown; faster oscilloscopes than those currently available are needed to determine this. Unfortunately, the difficulty in measuring CDM waveforms and the availability of various competing test method options has impeded the widespread deployment of CDM testing. However, Analog Devices recognizes the growing importance of this model and, thus, Analog Devices now classifies all new products and major die revisions to the CDM prior to product release.

No MIL-STD-883 test method exists for conducting CDM testing. The two CDM standards most commonly used in the semiconductor industry are

- ANSI/ESD S5.3.1, *ESD Association Standard for Electrostatic Discharge Sensitivity Testing: Charged Device Model (CDM) Non-Socketed Mode—Component Level.* [103]
- JEDEC Test Method JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components.* [104]

JESD22-C101, is the basis of the Analog Devices CDM ESD classification program.

Unlike the relatively complicated pin combinations used during HBM testing, FICDM stressing is straightforward. Each pin on the DUT is charged/discharged once positively and once negatively as follows:

1. The DUT is charged positively to the desired voltage level and then Pin 1 is discharged. This sequence is repeated two more times.
2. The DUT is charged negatively to this same voltage level and then Pin 1 is discharged. This sequence is repeated two more times.
3. Step 1 and Step 2 are repeated for each and every other pin on the DUT.

Unlike human body model pass voltages, CDM pass voltages depend significantly on the package type. For a given product offered in multiple packages, smaller packages are typically less susceptible to CDM damage than larger packages. This is primarily because smaller packages have less lead frame area to store charge than do larger packages. Consequently, when Analog Devices conducts FICDM testing on a new or revised product offered in multiple package styles, testing is either conducted on all available package styles or the worst-case package (typically the largest one) based on previous CDM test results.

Exercise Caution When Comparing Competitor ESD Results

When comparing competitors' ESD data on a given device type, it is essential to understand exactly how the data was generated and what failure criteria were used. Analog Devices follows stringent ESD test requirements based on ESD Association standards and JEDEC specifications. However, some semiconductor companies still follow less stringent test methods. One major cause of inconsistent ESD data from different semiconductor companies is differences in the failure criteria used when testing samples after ESD stressing. Consistent with ESD Association and JEDEC standards, Analog Devices uses electrical testing to data sheet limits (including all functionality tests and all dc and ac parametric tests) as the post-stress failure criteria. Any sample that does not meet all data sheet limits after zapping is considered a failure. For instance, on an operational amplifier with a maximum bias current (I_B) specification of 1.0 pA, if ESD stressing results in an I_B of 1.1 pA, the sample is considered a failure. Other semiconductor companies may consider this a marginal failure and discount it, whereas Analog Devices treats it as a legitimate failure. In addition, other companies may simply use curve tracer testing or open/short testing as their failure criteria, resulting in artificially high ESD pass voltages.

In summary, when comparing ESD results provided by different suppliers, it is essential to find out all of the following:

- What test method was used by the supplier
- What pin combinations were zapped
- What failure criteria were used

Otherwise, an improper ESD robustness conclusion is drawn from an invalid purely numerical comparison.

Summary of HBM and FICDM Test Methods

Table 15 provides a summary comparison of the human body model and the field induced charged device model as deployed at Analog Devices. As the table indicates, these two models represent fundamentally different ESD events. Consequently, correlation between the test results for these models is minimal.

Table 15. Summary of HBM and FICDM Test Methods

Basis of Comparison	Human Body Model	Field-Induced Charged Device Model
Simulates	Discharge from finger of a standing person	Discharge when a charged IC contacts a grounded surface
First Used for ICs	Late 1960s	1974
Basis for Analog Devices Test Methods	ANSI/ESDA/JEDEC JS-001	JEDEC JESD22-C101
RC	1500 Ω, 100 pF	1 Ω, typically 1 pF to 20 pF
Rise Time	<10 ns (typically 6 ns to 8 ns)	<400 ps (with a 1 GHz scope)
I_{PEAK} at +1500 V	1.0 A	13.5 A (with a 1 GHz scope)
Energy for V_{PEAK} = +1500 V	~1.5 µJ	~2.0 µJ
Total Duration	~500 ns	~2 ns
Number of Discharges Per Pin	Variable; function of pin-out	1 (1 positive and 1 negative)
Failure Criteria	Testing to data sheet limits (both functional and parametric)	
Package Dependency	No	Yes
Relevance to Real World	Moderate, but decreasing due to increased automated handling/assembly	Very high

ANALOG DEVICES TARGETS FOR ESD ROBUSTNESS

Based on reviews of customers' general semiconductor specifications, discussions with various customers, and internal failure analysis results, Analog Devices has established the following ESD target classification pass levels for new products and major die revisions:

- Human body model: ≥2000 V
- Field induced charged device model: ≥750 V for corner/outside pins; ≥500 V for other pins

The targets for FICDM robustness on corner/outside pins are higher than for other pins because the majority of real-world CDM events occur on packages having corner/outside pins. A corner/outside pin on a charged IC is more likely than other pins to contact a hard or virtual ground, therefore resulting in a CDM discharge. For example, on a 16-pin SOIC, the corner pins Pin 1, Pin 7, Pin 8, and Pin 16 are the most likely to be subjected to a CDM discharge. On a 44-pin quad flat package, the corner pins Pin 1, Pin 11, Pin 12, Pin 22, Pin 23, Pin 33, Pin 34, and Pin 44 are particularly susceptible to a CDM discharge. As a final example, on a 225-ball plastic ball grid array (PBGA) package in a 15 × 15 configuration, the 56 balls along the outside rows are the most likely to be subjected to a CDM discharge.

The vast majority of Analog Devices products meet or exceed the target ESD classification levels stated previously. Some products, however, have demanding electrical performance and specification characteristics that preclude the use of standard on-chip ESD protection cells. Examples include

- ICs with extremely low bias/leakage current specifications (pA to fA range)
- ICs with one or more pins that have operating/test voltages beyond the supply rails
- ICs with one or more high frequency pins (typically >800 MHz).

In cases such as these, most pins on the IC will meet Analog Devices' targets for ESD robustness. However, the pins with special electrical performance requirements may not meet these targets. Whenever possible, these pins are not assigned as corner/outside package pins. This minimizes the probability that they will be subjected to real-world ESD events.

Some Analog Devices products, such as RS-232 and RS-485 transceivers, are intended for use in environments that are particularly vulnerable to high voltage ESD and EOS events. For such products, proprietary or patented design/layout techniques are used to achieve robustness levels far above the target ESD levels shown above. In addition, ESD/EOS testing is conducted using additional models/test methods. For example, the input/output pins on the latest versions of the ADM2209E and ADM3311E RS-232 transceivers pass all the following tests:

- ±15,000 V ESD Classification Test Level, as per the IEC 61000-4-2 Air Discharge HBM (RC = 330 Ω,150 pF) [103]
- ±15,000 V ESD Classification Test Level as per the MIL-STD-883 Method 3015 HBM (RC = 1500 Ω,100 pF)
- ±8,000 V ESD Classification Test Level as per the IEC 61000-4-2 Contact Discharge Model (RC = 330 Ω,150 pF)
- ≥ ±2 kV Electrical Fast Transient (EFT) testing per IEC 61000-4-4 [104]

For further details on this testing as well as the ESD/EFT protection schemes, see the ADM2209E and ADM3311E data sheets.

ESD FAILURE MODES AND FAILURE MECHANISMS

Overview

ICs subjected to ESD usually have distinct failure signatures. The most common ESD induced failure mode is leakage or resistive shorts at input/output pins. Other failure modes include excessive supply current, open-circuit pins, or functional failures. The pins causing these failures can sometimes be identified via pin-to-pin current-voltage (I-V) curve tracer testing. However, particularly in the case of the CDM, the damage may be well past the on-chip input/output circuitry, and thus not detectable via I-V testing. In such cases, advanced failure analysis (FA) techniques may be required to locate the ESD damage.

Most ESD induced failures occur due to one of more of the following three failure mechanisms:

- Conductor/resistor melting
- Dielectric damage
- Junction damage/contact spiking

Any of these failure mechanisms can potentially occur on any IC. However, depending on the key features of the corresponding wafer fabrication process (for example, very thin gate oxides, submicron line widths, thin-film resistors, and so on), certain failure mechanisms may predominate.

Conductor/Resistor Melting

Conductor or resistor melting can occur in thin metal interconnects, thin-film or thick-film resistors, and polysilicon resistors/interconnects. This is the easiest ESD failure mechanism to understand. The ESD event causes excessive localized Joule heating that melts the conductor or resistor material. Conductor/resistor melting is most commonly seen on ICs subjected to HBM ESD because real-world HBM events typically have higher energy than real-world CDM events. In most cases, the ESD event completely fuses open the conductor/resistor, terefore resulting in a functional failure of the IC. However, in the case of thin-film and thick-film resistors, partial melting of the resistor material is possible, resulting in only a shift in the resistance and a corresponding parametric failure of the IC.

Figure 108 shows an example of a fused-open aluminum MET1 interconnect on an advanced bipolar IC that was nonfunctional after being subjected to ±2000 V HBM stressing.

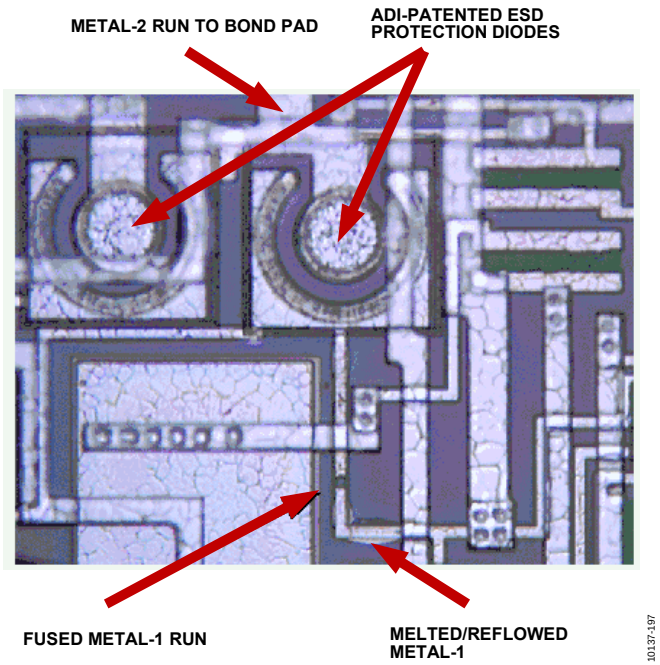

Figure 108. Optical Microscope Image of a 4 µm Wide MET1 Interconnect on a Sample Stressed at ±2000 V HBM

Note that this damage was visible without deprocessing.

In the case of the IC in Figure 108, the 4 µm MET1 run was in the primary path of the ESD current flow during ESD stressing. The fix was simply to widen the metal line to 8 µm. As a result, the IC improved its HBM classification test level to ±4,000 V. Using failure analysis (FA) results from project chips and new products that are subjected to ESD stressing, Analog Devices regularly updates IC design and layout rules so that they reflect best practices for achieving excellent ESD robustness.

Dielectric Damage

Dielectric breakdown occurs when the voltage across a dielectric layer (for example, silicon dioxide, silicon nitride) exceeds its time-dependent dielectric breakdown (TDDB) voltage maximum value, resulting in punchthrough. This TDDB mechanism is the predominant CDM failure mechanism, since the extremely fast rise time is the most likely of all ESD models to result in excessive on-chip voltage. The sequence of events that causes dielectric damage is as follows:

1. The dielectric breakdown voltage is exceeded at a high electric field point, typically a submicron site at an edge, corner, or step in the dielectric layer.
2. Very high current flows through the breakdown point, resulting in adiabatic (highly localized) heating of the immediately adjacent area.
3. A melt filament (for example, amorphous silicon or polysilicon) forms along the conduction site.

Figure 109 and Figure 110 show an example of gate oxide damage sites on a pMOS output driver transistor that exhibited leakage after being subjected to FICDM discharges at the drain/output pin after the sample was charged to ±1500 V. In this case, the gate polysilicon was at nearly ±1500 V when the drain/output pin was instantaneously grounded. This resulted in dielectric breakdown, high current flow, and the formation of a melt filament, as detailed in Step 1 through Step 3.

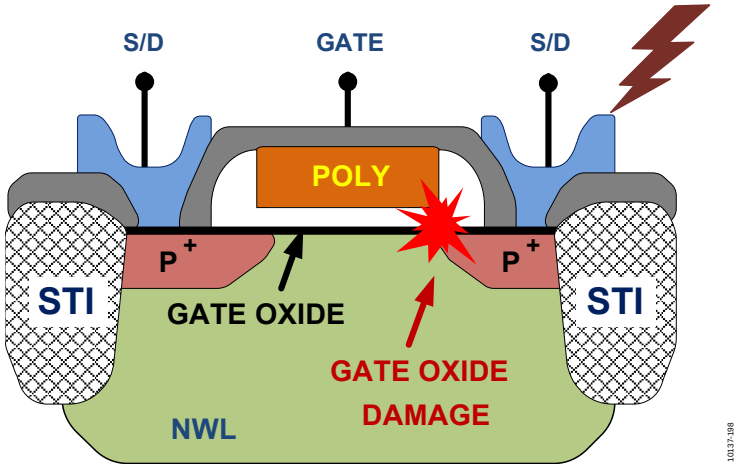

Figure 109. Location of Typical FICDM Gate Oxide Damage

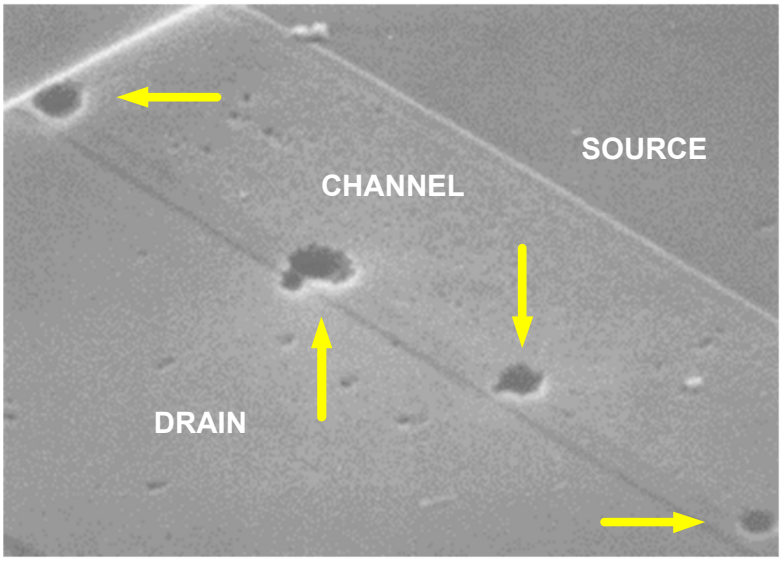

Figure 110. Scanning Electron Microscope (SEM) Image Post Deprocessing to the Silicon Level Showing 4 Pits on a Sample Stressed at ±1,500 V FICDM

These pits are approximately 0.2 µm to 0.5 µm in diameter and correspond to where silicon melted and flowed into the gate oxide.

Analog Devices designs ICs that are relatively immune to dielectric damage by including proprietary ESD protection cells adjacent to bond pads and by including appropriate series resistors between the bond pads and the susceptible dielectric layers. The ESD protection cells are designed to turn on extremely rapidly in response to an ESD event, thus clamping/limiting the voltage at the bond pad.

Junction Damage/Contact Spiking

Junction damage and/or contact spiking typically occur when a shallow P-N junction (for example, the emitter-base junction of a bipolar transistor or the drain-substrate junction of an nMOS transistor) is subjected to avalanche breakdown, followed by secondary breakdown and ultimately thermal run-away. The sequence of events that results in junction damage and lead to contact spiking is as follows:

1. The avalanche breakdown voltage of a reverse-biased P-N junction is exceeded.
2. Secondary breakdown can then occur at a point where the P-N junction is sufficiently hot to cause thermal generation of carriers to exceed avalanche generation of carriers.
3. Very high current is funneled through the secondary breakdown site, resulting in adiabatic (highly localized) heating of the immediately adjacent area.
4. This highly localized heating accelerates the thermal generation of carriers, which further increases the current flow and results in a thermal runaway condition whereby more and more thermally-generated carriers cause higher and higher current flow. This culminates in melted silicon at the initial breakdown site if the temperature exceeds 1415°C.
5. If the heating is sufficient to melt the metal in an adjacent contact opening, the electric field can cause the melted metal to migrate across the junction, resulting in a resistively-shorted junction.

When the melted silicon at the secondary breakdown site on the P-N junction resolidifies after the ESD event, the dopant profile is redisturbed as the P-type and N-type dopants mix together when the silicon melts. In addition, the resolidification process alters the crystal properties of the silicon. The changes in the dopant profile combined with the changes in the silicon crystal properties result in soft reverse-breakdown I-V characteristics. Depending on the severity of the junction damage, the effect on the IC can range from an inconsequential increase in leakage current to a significant increase in leakage current resulting in one or more data sheet parameters being out of specification. Failure analysis at Analog Devices has shown that ESD induced crystal damage at a P-N junction can sometimes be partially annealed out by a 24 hour, 125°C unpowered bake, but the I-V characteristics are still softer than usual. This indicates that an IC junction that is damaged by ESD may actually have decreasing leakage current during field use, especially if the junction temperature is well above 25°C.

If the heating associated with the thermal runaway condition causes the metal in an adjacent contact opening to melt and migrate across the junction, the resulting resistive short typically causes the corresponding pin on the IC to exhibit a hard failure. High temperature baking of the IC has little or no effect on this resistive short.

To reduce the susceptibility to contact spiking, transistor layout rules typically specify increased contact-to-junction spacings for contacts connected to external pins. Special design techniques and layout rules are also used to reduce the susceptibility of a junction to secondary breakdown and thermal run-away. As with conductor/resistor fusing, junction damage and contact spiking occur most commonly on ICs subjected to HBM ESD since HBM events have higher energy than CDM events.

Figure 111 and Figure 112 show an example of drain-channel junction damage and drain contact spiking on an NMOS output transistor that exhibited a resistive short after being subjected to ±2000 V HBM stressing at the drain/output pin.

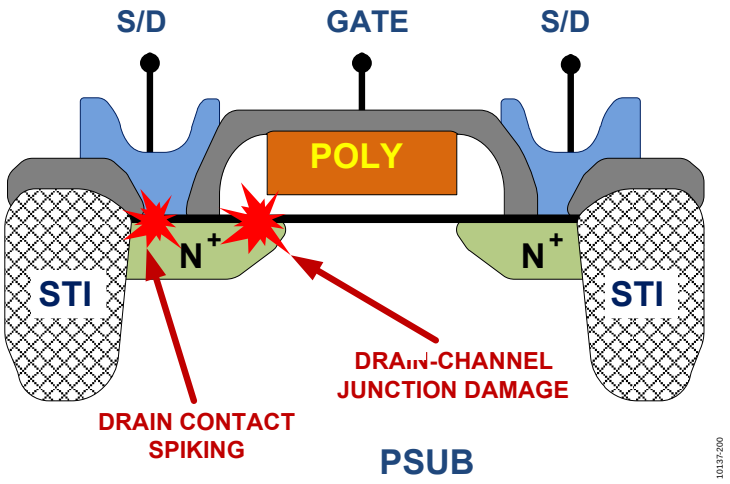

Figure 111. Locations of Typical HBM Contact Spiking and Junction Damage

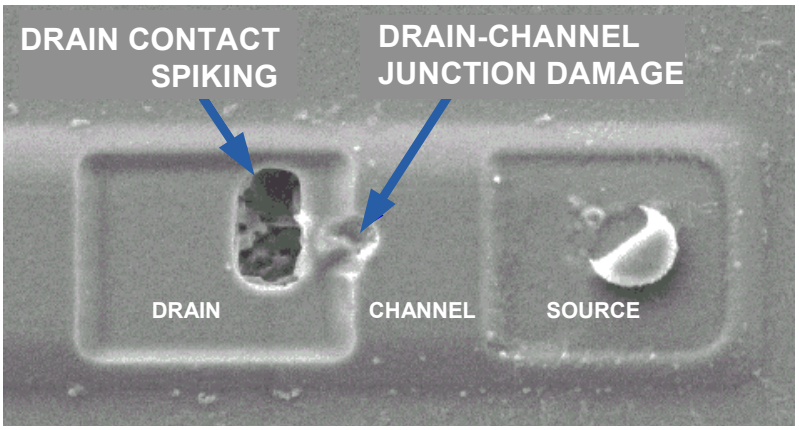

Figure 112. Scanning Electron Microscope (SEM) Image Post Deprocessing to the Silicon Level Showing Drain-to-Channel Junction Damage and Drain Contact Spiking on a Sample Stressed at ±2000 V HBM

In the case of the above IC, the nMOS output transistor was made larger and a series resistor was added between the drain and the output pin. This transistor is now immune to ESD damage during HBM stressing up to at least ±4000 V.

Summary of HBM and FICDM Test Methods

Table 16 provides a summary comparison of the three predominant failure mechanisms caused by ESD.

Table 16. Summary of ESD Failure Mechanisms

Failure	Conductor/Resistor Melting	Dielectric Damage	Junction Damage/Contact Spiking
Failures Occur at:	Thin film, thick film, polysilicon, metal	Any dielectriclayer, but especially thin layers such as gate oxide	Any junction, but especially emitter-base, drain-channel, and other small junctions
Failure Mode:	Resistance shifts and open-circuits	Leakage and resistive shorts	Junction damage: leakage; contact spiking: resistive shorts
Failure Signature:	Partial or complete conductor/resistor fusing	Submicron conductive melt filament through the dielectric	Junction damage: crystal damage across junction; contact spiking: hole in contact area
Most Prevalent on:	Human body model (HBM) failures	Charged device model (CDM) failures	Human body model (HBM) failures
Bake Recoverable:	No	No	Partially, unless resistively shorted
Recoverable at Ambient:	No	No	No

BOARD-LEVEL AND SYSTEM-LEVEL EOS/ESD PROTECTION

The human body model (HBM) and field induced charged device model (FICDM) represent just two of the infinite number of forms of electrical overstress (EOS). As indicated in Figure 113, EOS covers an entire spectrum of events, with the FICDM and dc overvoltage/overcurrent on opposite ends of the spectrum. However, a typical EOS event has a duration on the order of 50 ms. The much longer duration of a typical EOS event results in much more energy being delivered to the IC. For example, whereas +1500 V HBM and CDM discharges have energies of ~1.5 µJ and ~2.0 µJ, respectively, typical EOS events can have energies exceeding 1 J. Therefore, although the failure mechanisms associated with ESD and EOS are similar, the physical damage is generally much more severe with EOS failures. This is shown in Figure 114 and Figure 115, where examples of EOS damage are readily visible with an optical microscope following decapsulation of the plastic package. For a given IC, the higher the energy of the EOS event the more likely permanent damage is to occur.

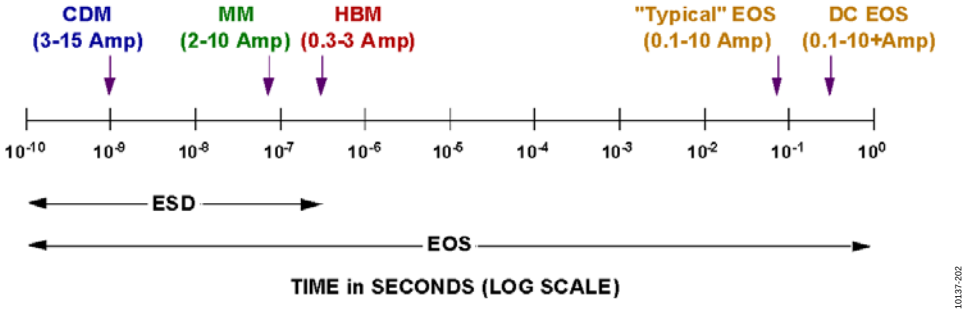

Figure 113. Spectrum Showing the Duration of Common EOS/ESD Events

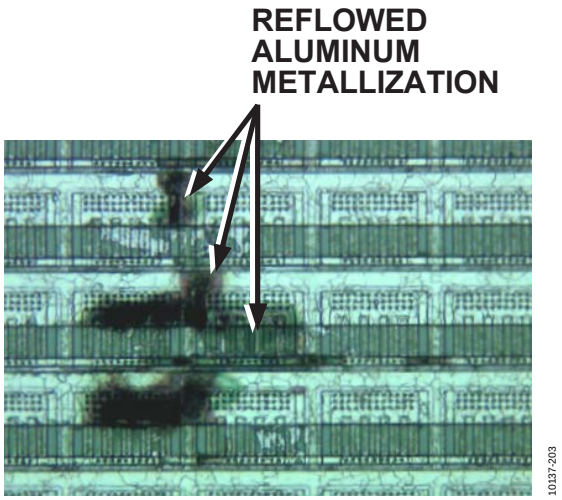

Figure 114. Optical Microscope Image of Severe Electrical Overstress (EOS)

Figure 114 shows damage at a bipolar output transistor. Note the black burn mark where the aluminum metallization melted and reflowed.

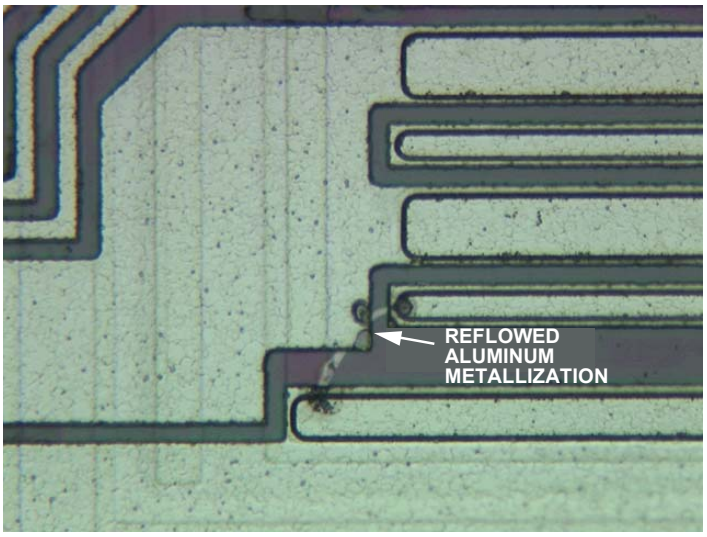

Figure 115. Optical Microscope Image of EOS Damage at a Bipolar Output Transistor

Note the dark burn marks where the aluminum metallization melted and reflowed, forming a white arc track that shorted-out the transistor.

Design for EOS/ESD Protection

Analog Devices uses proprietary and/or patented on-chip protection circuitry to maximize the robustness of its products to EOS/ESD transients at all pins. Analog Devices products use a broad range of EOS/ESD protection circuitry, depending on the wafer fabrication process and the electrical performance requirements of each pin on the product. Analog Devices ICs are typically designed with an individual protection circuit immediately adjacent to each non-substrate bond pad. An ideal protection circuit functions as a perfect switch that is

- Always electrically open (that is, having infinite resistance, zero capacitance, and zero inductance) during normal IC operation
- Instantaneously electrically closed (that is, having zero resistance, zero capacitance, and zero inductance) in response to an EOS/ESD transient.

However, due to fundamental device physics, no matter how well a protection circuit is designed, it is never a perfect switch. More specifically, a protection circuit is a source of parasitic leakage current, capacitance, and inductance during normal IC operation. In addition, all protection circuits have a finite turn-on time in response to an EOS/ESD transient, and have finite on-resistance. These non-ideal characteristics make the design of protection circuits very challenging, especially for high-performance ICs. Analog Devices has responded to this challenge by using teams of ESD engineers, device engineers, design engineers, layout engineers, failure analysis engineers, and reliability engineers to develop many innovative and effective protection circuits for our products.

As an example, Figure 116 shows a generic H-network protection circuit for input/output pins comprised of four protection devices, PD1 through PD4, and a series resistor, R. PD1 and PD2 provide primary protection, while PD3 and PD4 provide secondary protection. The function of PD1 and PD2 is to shunt as much of the EOS/ESD current as possible to one of the supply rails (V+ or GND). Series resistor R slows down very fast transients that may not have been adequately attenuated (clamped) by PD1 or PD2, and it also limits the magnitude of the residual current that is not diverted to a supply rail by PD1 or PD2. This residual current is then diverted to a supply rail by one of the secondary protection devices, PD3 or PD4. PD3 and PD4 are designed to clamp the voltage across internal circuit elements during a CDM discharge event.

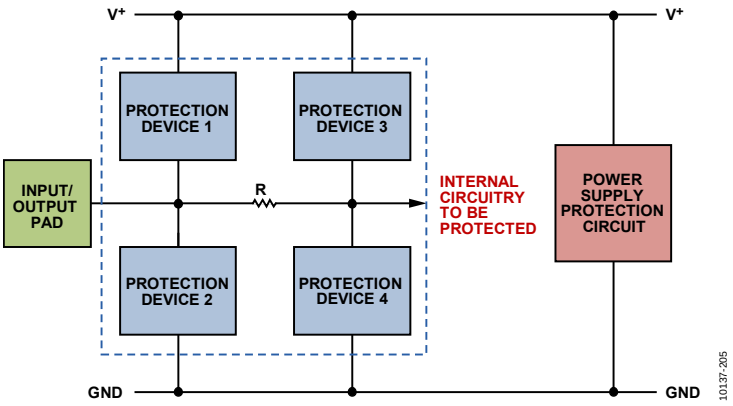

Figure 116. Generic On-Chip H-Network (in Dashed Blue Box)

EOS/ESD Protection Circuit Used on Input/Output Pins

To be fully effective, on-chip EOS/ESD protection circuitry must be included for all pin combinations subject to possible transients. For example, the circuitry shown in Figure 116 provides protection to the input/output pad as follows:

- A positive transient at the input/output pad with respect to V+ turns-on PD1 and PD3, thus conducting the EOS/ESD current to V+ and protecting the internal circuitry. (Note that most of the current is shunted through PD1 since resistor R limits the current through PD3.)
- A positive transient at the input/output pad with respect to GND turns on the power supply protection circuit as well as PD1 and PD3. (Again, most of the current is conducted by primary protection device PD1.) EOS/ESD current then safely flows from the input/output pad to V+ and then to GND, thus protecting the internal circuitry.
- A negative transient at the I/O pad with respect to GND turns-on PD2 and PD4. (Most of the current is shunted through PD2 because R limits the current through PD4.) EOS/ESD current then safely flows from the substrate (GND) out the input/output pad, thus protecting the internal IC circuitry.
- A negative transient at the input/output pad with respect to V+ turns-on the power supply protection circuit as well as PD2 and PD4. (Again, most of the current is conducted by primary protection device PD2.) EOS/ESD current then safely flows from V+ to GND and then out the input/output pad, thus protecting the internal IC circuitry.

Board-Level and System-Level EOS/ESD Protection

First Mate, Last Break Grounding Contacts

Poor or improper grounding of connectors are a primary cause of EOS when the system is under bias. This is generally referred to as hot plugging and the results may be failure of the IC unless it is designed to withstand such conditions.

First-mate, last break grounding refers to contacts that are designed to connect first to the system ground in question and break (or open) last from the system ground. These connectors provide a path for any stray voltage/current to be shunted to a safe ground avoiding any overstress damage from hot plugging to the system. This type of connector has been recommended and adopted by the automotive industry. Extended ground connection ensures the ground is connected first. Research by the Automotive EOS Working Group within ZVEI (the German Electrical and Electronics Industry Group) [110] has shown that extended ground pins (also known as first mate, last break grounding contacts) on automotive connectors greatly reduce incidents of EOS / system-level ESD damage in automotive electronics. Therefore, if end customers have not already implemented this, Analog Devices recommends that they participate in the industry's transition to this proven error-proofing method of eliminating connector-induced EOS/system-level ESD damage. Interested readers are referred to the industry white paper [110] on the subject. Analog Devices advocates such connectors for all systems for EOS immunity.

TVS: Transient Voltage Suppressor

One effective method to protect against EOS/ESD at the board-level and system-level during manufacturing and end-customer application is to use transient voltage suppressor (TVS) devices across the system supply planes as shown in Figure 117. TVS devices are discrete components that typically respond in <1 ns to a transient beyond the breakdown/punch-through voltages of the protected device. TVS devices safely shunt excessive current (up to tens of amps) away from the internal circuitry. They are available in both surface-mount and through-hole packages. TVS devices are also available in a wide range of voltages as well as very low capacitance and/or leakage versions, allowing application in the vast majority of applications.

Key characteristics of a TVS are

- High surge current/voltage handling capability
- Extremely fast response times (<1 ns)
- Very low on-resistance

For further details on the use of TVSs, refer to the AN-311 Application Note, *How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging* [108] and the AN-397 Application Note, *Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reoccurrence* [107].

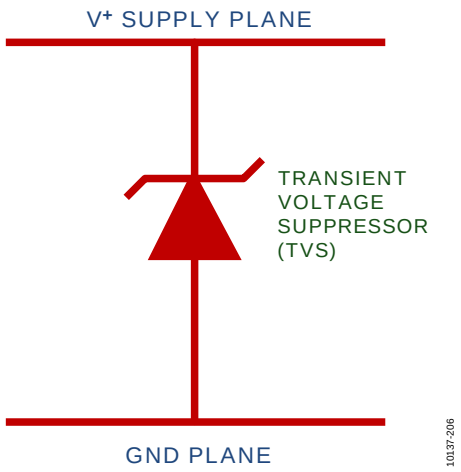

Figure 117. TVS Protection used for Protection Across Supply/Ground Planes in System Applications

Decoupling capacitors are also sometimes used between supply and ground rails for ESD/EOS protection purposes. However, capacitors should not be used exclusively as primary board-level and system-level ESD protection for the following reasons:

- They react slowly to transients.
- Significant voltages still develop across them during transients.
- The capacitor's current shunting capability during a transient is limited. Small capacitor values provide a better current-shunting capability at high frequencies and vice versa for the high value capacitors.

Summary of Board-Level and System-Level EOS/ESD Protection

A highly effective approach to minimizing board-level and system-level EOS/ESD damage is to use extended ground pins on connectors and transient voltage suppressors across supply and ground planes. To ensure EOS immunity, Analog Devices recommends that users review and verify the following in their systems:

1. Review their application and determine if any external capacitors or any inductive loads are connected to the external pins of Analog Devices components. Rapid discharges of charged external capacitors or voltage transients due to rapid changes in the current in an inductor are major causes of board-level and system-level EOS/ESD damage in integrated circuits. If external capacitors or inductive loads may be causing voltage transients on particular pins, the user should consider adding an external series resistor at these pins to limit the current to a safe level. Alternatively, a transient voltage suppressor (where the TVS is selected to prevent the pin voltage from exceeding its absolute maximum rating) may be used on these pins.
2. Ensure that discrete capacitors are not charged when placed on PCBs during the manufacturing operations. This can result in a high current discharge that can damage integrated circuits. One effective method of mitigating this issue is to use static-dissipative tips on pick-and-place equipment. These tips should bridge both terminals of the capacitor to allow a safe discharge of the capacitor prior to board placement.
3. Use a high speed oscilloscope to check for voltage transients exceeding the Absolute Maximum Ratings of IC pins during operation, particularly during power-up and power-down sequences as well as during automotive fault conditions such as a load dump. If such transients are identified and cannot be eliminated, Analog Devices recommends that an external series resistor or a TVS be added to these pins at the board level.

These steps address the most common sources of board-level and system-level EOS/ESD damage.

Latch-Up

Latch-up is an overstress condition that can occur in ICs as a result of uninteded overvoltages, transient displacement current or ionizing radiation that turns on parasitic NPN and PNP bipolar junction transistors, which are cross connected to form a *pnpn*.

Figure 118 shows a cross section of a generic baseline CMOS process technology with these parasitic bipolar structures outlined in a *pnpn* configuration. To understand this physical phenomenon, consider two adjoining MOS transistors of opposite polarity, an nMOS and a pMOS, and the four *n* and *p* diffusions; namely *n+*, *p-substrate*, *n-well* and *p+* as shown in Figure 118. The *p+*, *n-well*, *and P-substrate* form a parasitic PNP bipolar device, wehereas the *n+*, *p-substrate* and *n-well* form a parasitic lateral NPN. These NPN and PNP bipolar transistors are cross-coupled because the base of the PNP device is the collector of the NPN and, similarly, the base of the NPN is the collector of the PNP. Under a bias condition where current is injected into the *n+* or *p+* diffusions, lateral currents can generate suffcient voltage to forward bias the emitter-base junctions of the bipolar transistors, activating both of them. If the current-gain product of the two

bipolars are greater than one, they cause regeneration. As a consequence, latch-up occurs. This is when the *pnpn* structure is in a low impedance, high current state. This state is sustainable even when the original stimulus is removed, as long as the voltage between *p*+ and *n*+ remains high enough to retain the same bipolar behavior.

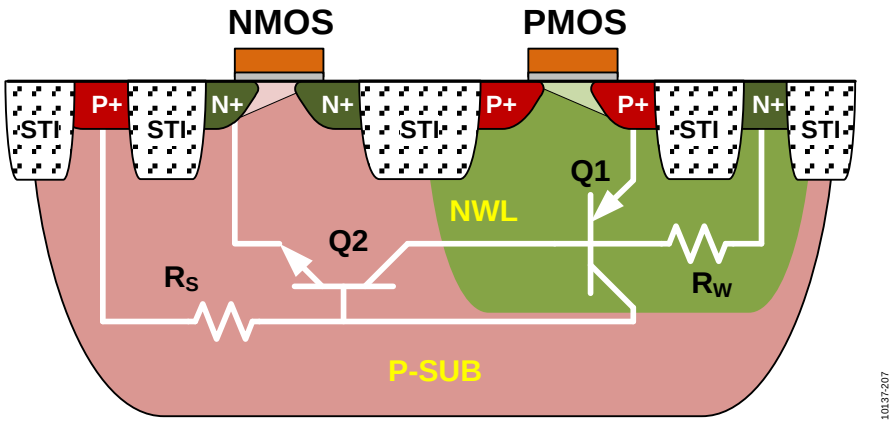

Figure 118. Cross Section and Schematic of Parasitic Bipolar Transistors in a Generic CMOS Process Technology Node

The harmful effects of latch-up are many, including increased leakage current or permanent loss of functionality due to nMOS/pMOS junction damage and metal burnout from overcurrent supplied to the *pnpn* structure. To test the robustness of a particular product to latch-up, a test is conducted (JEDEC standard JESD78) where the product is stressed to the maximum permissible supply voltage and current is injected into the indvidual pins for a pre-detrmined duration (typically ~5 ms with a stress pulse rise time of 5 µs). The product passes the latch-up test if the maximum latchup trigger voltage is reached without sustainable overcurrent, or if the maximum injected current into and/or sourced out of the device pin does not cause sustainable overcurrent.

SUMMARY

Analog Devices is committed to developing and releasing ICs that have high levels of robustness to component electrical overstress (EOS) transients, including electrostatic discharge (ESD) and latch-up. All new products are ESD tested to the human body model (HBM) and the field induced charged device model (FICDM), as well as latch-up. Analog Devices uses stringent methods for this HBM and FICDM testing, consistent with the latest industry standards. Analog Devices' expertise in on-chip EOS/ESD protection circuitry is demonstrated by its broad portfolio of patents in this area. More importantly, Analog Devices' continuous focus on maximizing the robustness of its products has resulted in a downward trend in the number of customer returns due to ESD damage.

PRODUCT ANALYSIS

INTRODUCTION

Product analysis, or failure analysis, is a key contributor to Analog Devices' overall quality improvement. To maintain success, it is imperative that customers have a high level of confidence in Analog Devices' competency as a supplier. Part of the in-built product analysis philosophy is to emphasize the concept of continuous quality improvement with the realization that product analysis is a significant contributor to the quality and reliability of products. Through feedback of problems identified during product analysis and pinpointing precise areas for process improvement, the contributions of the product analysis groups to Analog Devices' excellence in quality and reliability are invaluable.

The Analog Devices product analysis groups are dedicated to providing customers with uncompromising support, whatever the issue. Analog Devices demands that product analysis techniques be flawless and that analyst teams be comprised of highly trained and skilled professionals. As an engineering group under the direction of the Quality Assurance department, members are required to be versatile in their problem management techniques. As product analysis requests filter in from external and internal sources, the analysts may be exposed to a wide range of problems. It is the ability to cope with such a diversity of clients and issues that makes the product analysis group unique in its insight into all stages of the semiconductor manufacturing process.

There are three product analysis centers and regional customer support centers within Analog Devices that provide technical assistance to customers in the form of failure analysis. The centers are located in Limerick, Ireland; the Philippines; and Wilmington, Massachusetts. Offering highly professional engineering support services, advanced product analysis techniques, customer advocacy programs, and measured customer response times with continuous focus on prompt and timely failure analysis, these centers are structured to reflect Analog Devices' policy of total quality management. The following section outlines the responsibilities that face the product analysis engineering groups in meeting Analog Devices' quality objectives.

DEFINITIONS

The following product analysis definitions are used throughout this section:

Product Analysis or Failure Analysis (FA)

This is the general definition given to the activity that follows when an integrated circuit fails to perform to its expected specification. It combines advanced analytical techniques from physics, electrical measurement, materials analysis, and chemistry to identify the cause of failure.

Failure Verification

This is the confirmation that the device being analyzed is an actual failure.

Failure Mode

This is the reported characteristics of the failure, for example, open circuit or I_{DD}.

Failure Mechanism

This is the physical mechanism or conditions that created the observed failure, for example, gate oxide breakdown or lifted bond.

Failure Site

This is the exact physical location in a package or on a die that has resulted in the failure.

Root Cause of Failure

This is the actual cause of failure, the first event or condition that triggered, whether directly or indirectly, the occurrence of the failure; for example, where a lifted bond wire was the failure mechanism, why it lifted would be termed the root cause.

Corrective Action

This is a list of one or more actions taken to eliminate or avoid a reoccurrence of a failure mechanism.

SOURCES OF FAILURE

The product analysis requests originate from a wide variety of customers and there is a need for a clear breakdown. The requests for FA may be generated by an external customer, that is, a customer return, or generated internally from reliability evaluations/new product qualifications/fabrication process yield issues.

CUSTOMER RETURNS PROCEDURE

A customer can report product quality complaints by one of the following methods:

- By contacting an Analog Devices representative who will assist in initiating a customer alerts and returns environment (CARE) form.
- By the return materials authorization (RMA) process.

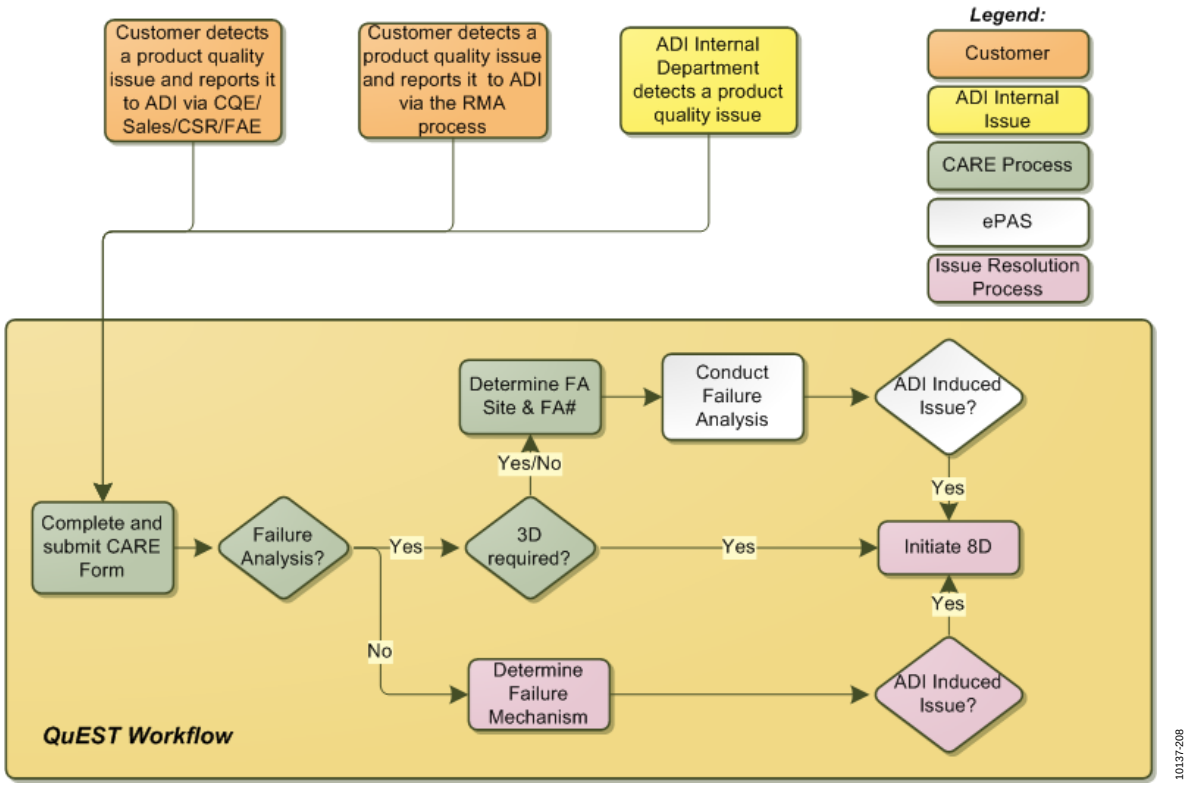

Figure 119. Customer Returns Flowchart

INTERNAL PRODUCT ANALYSIS REQUESTS

As failure analysis, an internal service group, a large proportion of the workload stems from internally generated sources. These are reliability engineering failures: failures produced from ongoing reliability monitors, ELF programs, and reliability qualifications.

These include failures from the following reliability stress tests: burn in, life test, HAST, pressure cooker, temperature cycling, thermal shock, and solderability. Included are any failures generated from a new product qualification and wafer fabrication process yield failures. All these failures are analyzed to their root cause because the results are vital for quality, yield, and reliability improvement.

PRODUCT ANALYSIS TRACKING

The electronic product analysis system (EPAS) is Analog Devices' centralized database for failure analysis. It is used to track open/closed FA requests and store various information, such as customer, product, failure mechanism cycle time for data trend analysis. This system is also used to write up, store, and electronically generate and approve failure analysis reports.

PRODUCT ANALYSIS SEQUENCE

The flow chart in Figure 120 provides a general guideline for the path of a typical FA. The path is not predetermined; the sequence of steps is determined by the particulars of the failure analysis request. However, as a minimum requirement, all analyses typically include an automatic electrical test, an external visual examination, and most importantly, a failure verification and localization step.

Product Analysis Prerequisites

Before a failure analysis begins, there are certain details to consider.

- Device information: a completed CARE form, reliability tracking sheet, or other form of documentation that details device type, serial number, date code, and manufacturing lot number.
- Point of failure: where in the process did the devices fail?
- Failure mode: a description of the failure behavior.
- Operating conditions: device application, environmental conditions, time to fail.
- Automatic electrical test: the suspected failures must be tested on a production tester to the applicable QA test program and the test results recorded.

When all the above information is collected, it is analyzed by an FA preprocessing team that reviews the validity of the FA.

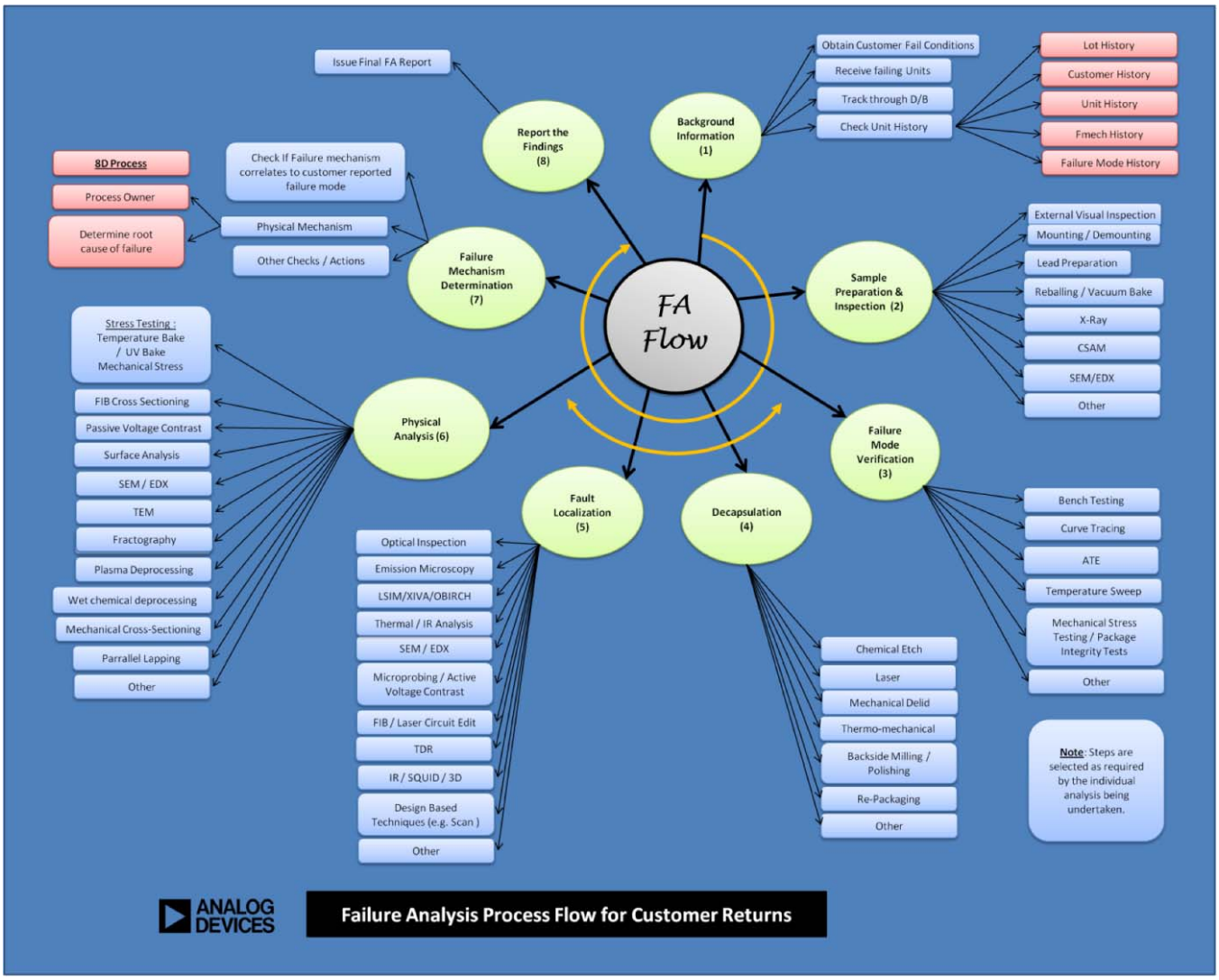

Figure 120. Failure Analysis Flow

PRODUCT ANALYSIS CAPABILITIES

The range of analytical techniques available to a product analysis group reflects its commitment to competency in quality. Analog Devices has a well-balanced range of analytical techniques available, with continuous focus on acquiring new techniques. If necessary, techniques that are not directly available to Analog Devices are sourced and contracted.

Currently available techniques are as follows:

- Package analysis: optical inspection, x-ray, and acoustic microscopy
- Sophisticated bench testing equipment
- Decapsulation techniques for all products
- Internal visual inspection
- Defect location: emission microscopy, microprobing, mechanical cross sectioning
- Chemical and dry depassivating methods
- Scanning electron microscopy
- FIB microsurgery and cross sectioning

BACKGROUND INFORMATION

- Acquire known good devices
- Confirm FA socket capability and evaluation board capability (all open top)
- Consult the reliability engineer about priority
- Consult a reliability, test, or design engineer about qualification and device history for any similar failures
- Determine what the qualification is for, such as new product, design edit, and so on

External Visual Inspection

Inspect the device for defects/abnormalities/nonconformance in the device leads, package, or package markings. This is typically performed with an optical microscope at a variety of magnifications.

X-Ray Analysis

An x-ray system is used as part of the package assessment technique that identifies package cracks, severe die cracks, open bond wires, and lifted ball bonds. The system is extremely useful when used in conjunction with acoustic microscopy because lifted bonds and cracked wires may be associated with delaminated portions of a package. 3D x-ray analysis is also available.

Confocal Scanning Acoustic Microscopy (CSAM)

The acoustic microscope is a nondestructive method of detecting variations in the physical properties of a package or a die. The operation is based on simple acoustic principles. The devices under examination are placed into a large container of deionized water. An ultrasonic transducer is placed near the surface of the device below the water line. The transducer generates a series of high frequency waves that impinge upon the various package components. Based on the nature of the material the acoustic wave penetrates, a reflected and partially reflected wave is generated and detected by the transducer. Based on the amplitude and the phases of the reflected waves, the acoustic microscope can detect internal package cracks, die cracks, voids in the die attach, and interface delamination.

Curve Tracer

A tool used to characterize the I-V curve of a particular pin by applying a voltage to a device pin and plotting the resultant current. A known good unit is usually used as a reference. Curve tracing can detect open circuits, short circuits, and leaky device characteristics.

Figure 121. Curve Trace Oscilloscope

Powered Curve Trace Analysis

Curve trace is performed on the device while the device is powered up in its failing mode, as per bench testing. This technique can provide curve trace capability to the internal circuitry, that is, beyond the ESD protection.

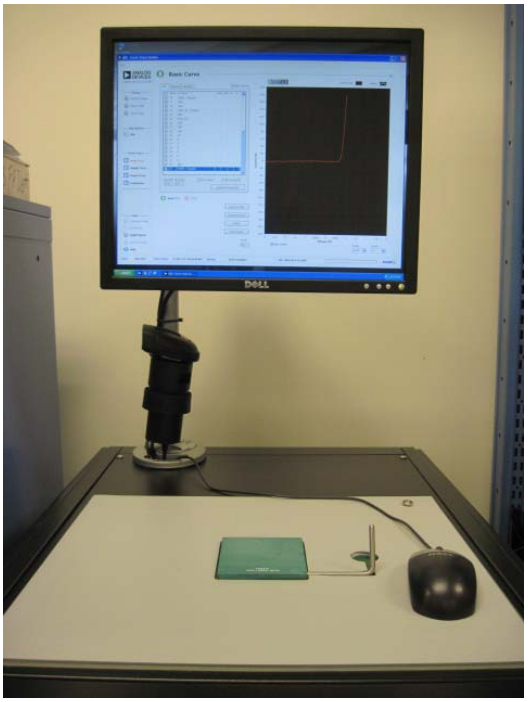

Figure 122. Automated Curve Tracer

Automated Test Equipment (ATE) Testing

ATE testing is used to verify that the returned device passes or fails the production test program. This can be performed at ambient, hot, or cold temperatures.

Bench Testing

The failing device is electrically stimulated using the necessary bench test equipment. With the aid of the product data sheets and ATE datalogs, the device is powered up and the failure mode verified accordingly. Electrical verification must be confirmed before destructive analysis is performed.

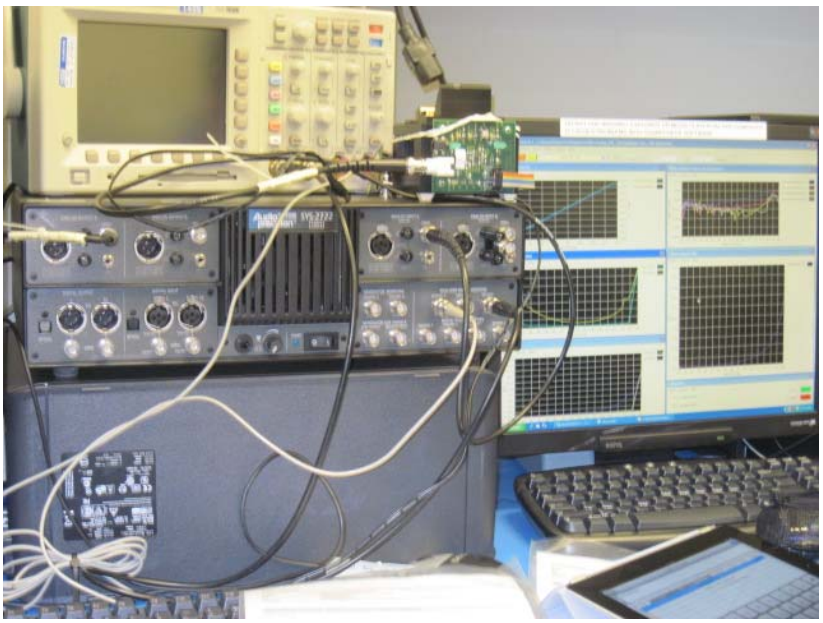

Figure 123. Bench Test Set-up

Bake Out

Bake out provides additional failure mechanism information on an electrically verified failure. A typical bake-out condition is 24 hours at 150°C in an unbiased environment.

Burn In

The burn in technique refers to a biasing operation at 125°C, sometimes used to recreate a failure mechanism. Burn-in accelerates the normal operating life of a device.

Decapsulation

The decapsulation procedure is undertaken when all applicable nondestructive analysis have been performed. Chemical decapsulation is the most common method used throughout Analog Devices. The decapping system uses hot nitric or sulfuric acid to chemically etch plastic packages for internal package inspection. The mechanical decapping method is used less often and is performed using mechanical decapping tools on hermetic and plastic packages.

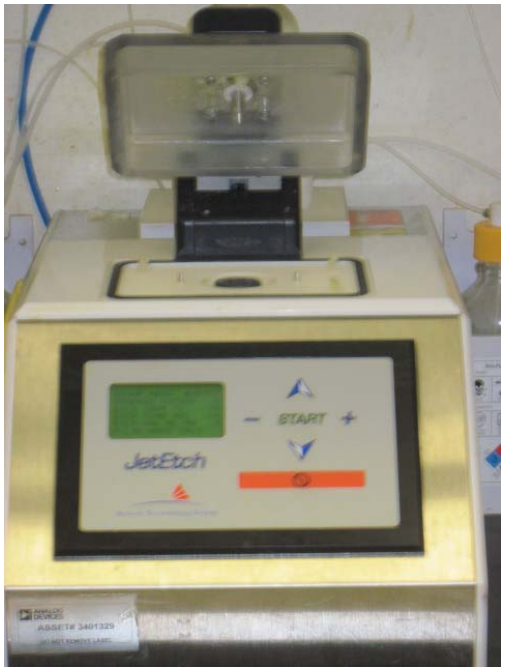

Figure 124. JetEtch Decapsulation Machine

Backside IC Thinning/Preparation

Backside IC thinning/preparation is performed when through-silicon analysis is needed. The process varies depending on package type and IC thickness, but the goal is to expose, thin, and polish the silicon to enable through-silicon IR inspection or backside fault isolation analysis (photon emission, LSIM, thermal analyses). A selective area of the package can be precision milled to expose the region of interest, or a small selected area of a sample can be polished to partially remove a layer of material.

Figure 125. Ultra Tec Backside Thinning Machine

Internal Visual Inspection

Internal visual inspection is a thorough optical examination of the exposed die, which is usually performed using a standard optical microscope at a variety of magnifications. Dark field microscopy is also available.

Figure 126. Internal Visual Station

Infrared (IR) Inspection

IR inspection is a technique used for through-silicon inspection and imaging, and is useful for flip chip packages as well as inspection of MEMS devices, which utilize a silicon cap to protect mechanical components on the IC.

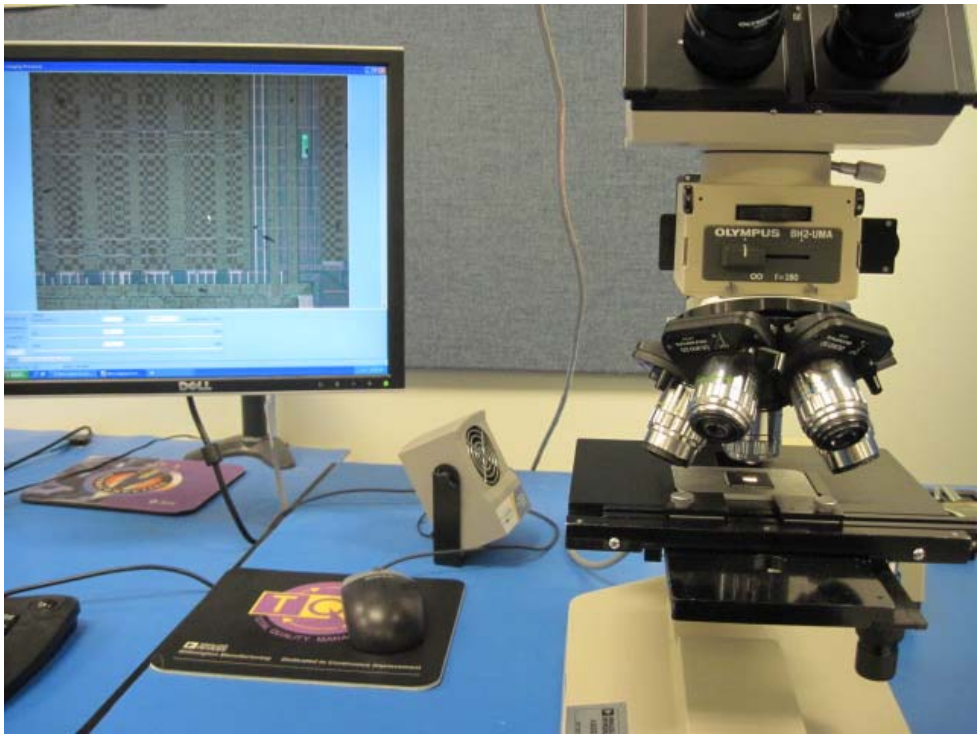

Figure 127. Infrared Inspection Station

Emission Microscopy

Emission microscopy is a fault isolation technique that detects visible light emitted from a biased IC. Anomalous photon emissions usually occur due to recombination in silicon devices. A known good unit confirms any anomalous emission sites on the failing device.

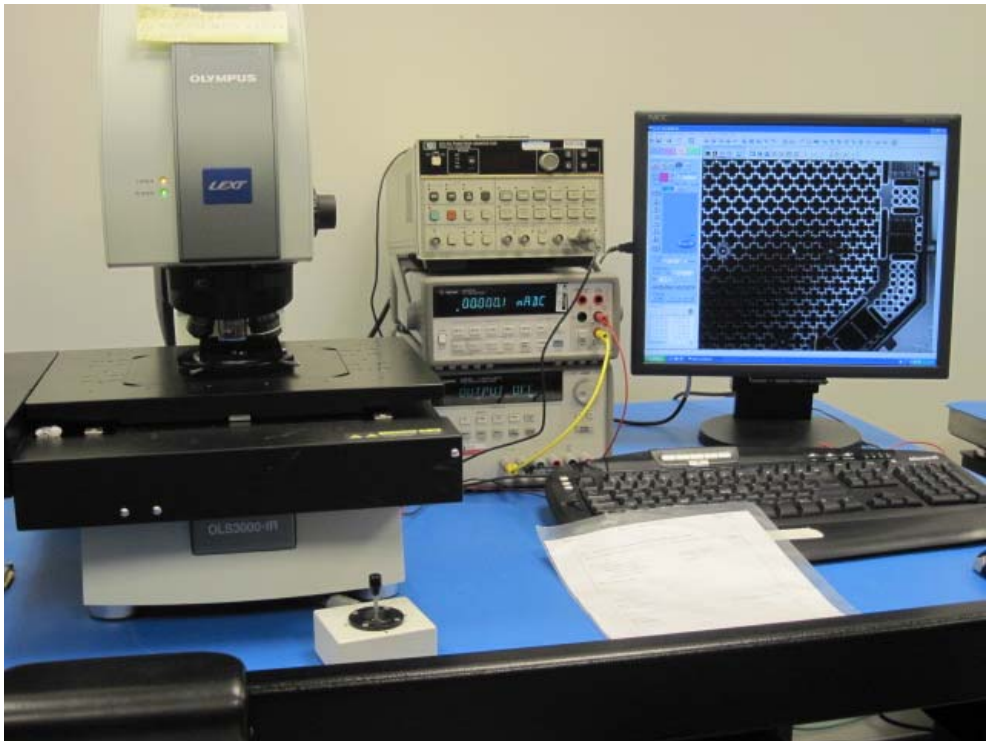

Figure 128. Emission Microscopy Station

Thermal/IR Analysis

Thermal/IR analysis is a fault isolation technique that uses an InGaAs detector to capture a temperature profile of a device under test. A known good unit is used to confirm any anomalies on the failing device.

Laser Signal Injection Microscopy (LSIM)

LSIM is used to conduct externally induced voltage alteration (XIVA) or optical beam induced resistance change (OBIRCH) techniques. Both techniques use a scanning laser to heat (1340 nm laser) or induce photo-carriers in (1064 nm laser) the device under test while monitoring the supply for any change in resistance cause by the laser. A known good unit is used to confirm any anomalies on the device under test.

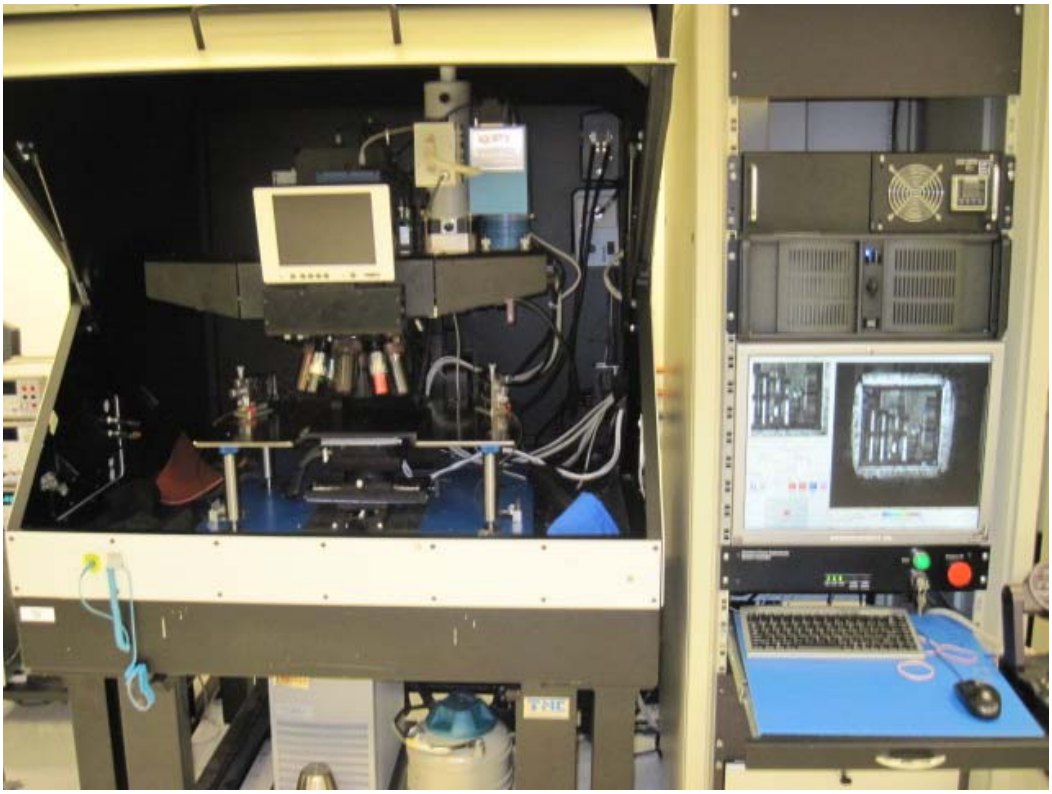

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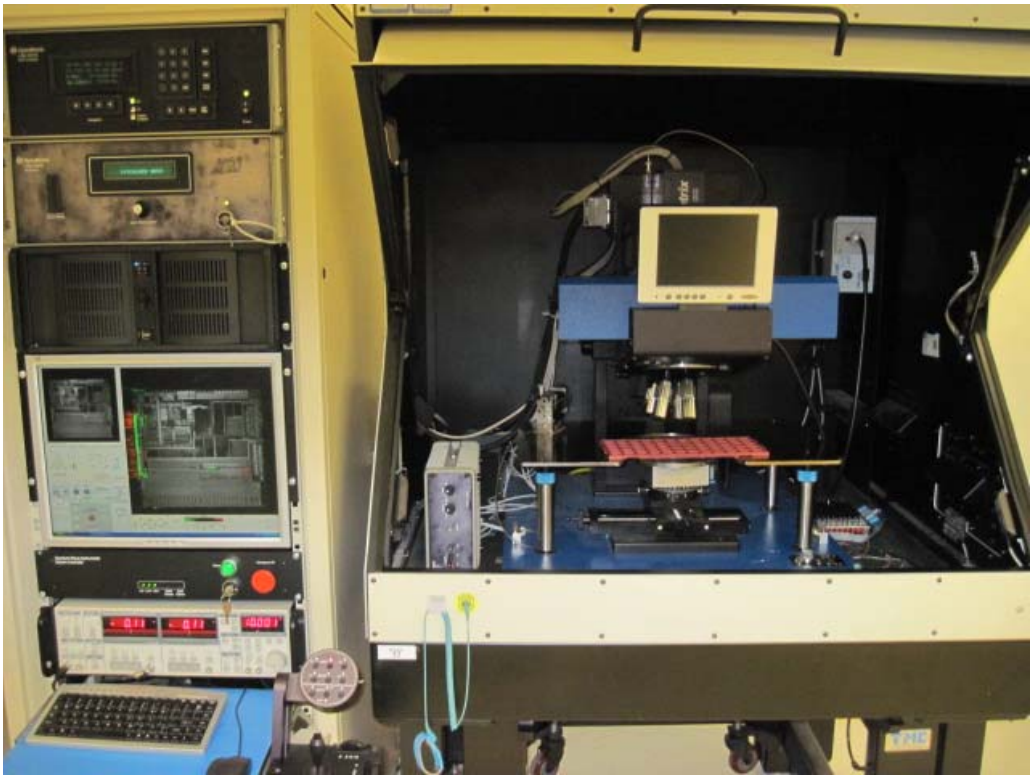
Figure 129. Laser Signal Injection Microscopy Station

Electrical Microprobing

Microprobes can be used to contact the die directly. Microprobing is performed with a probe station along with any of the necessary electrical bench test equipment needed to operate the device.



FFigure 130. Electrical Microprobing Station

Electrical Nanoprobing

A higher resolution version of microprobing, nanoprobing is performed inside an SEM chamber with precision controlled probe manipulators. The technique can contact very small geometries, allowing individual devices to be characterized electrically at various layers of the die. A sophisticated electrometer/curve tracer is dedicated to this tool.

Figure 131. Electrical Nanoprobing Station

Reactive Ion Etcher (RIE)

The RIE technique uses a combination of gases to etch passivation and dielectrics. Plasma is generated using various ratios of sulfur hexafluoride, oxygen, carbon tetrafluoride, and/or trifluoromethane. The plasma etches the appropriate target material is etched away under the optimal conditions of RF power, bias, and gas pressure.

10137-221

Figure 132. Reactive Ion Etcher

Chemical Deprocessing

A variety of chemical etches and techniques are available to selectively remove selected IC layers.

Cross Sectioning Techniques

Encapsulated and nonencapsulated cross sectioning are the two main cross sectioning techniques employed by Analog Devices. The encapsulated method requires the failing unit to be set in an epoxy mixture and mounted on a cross sectioning wheel. The unit is then ground to the required location using abrasive sheets and then polished on a cloth with mildly abrasive colloidal suspensions. In the nonencapsulated method, the die or package is mounted on a cross sectioning stub. Again, the cross sectioning tool is used to grind the die back to the target site.

Parallel Polishing

This technique can be used for both package level and die level deprocessing. This can be performed on a parallel polishing tool or by hand, depending on the sample. Dies can be also precisely thinned or polished for emission microscopy.

10137-222

Figure 133. Parallel Polishing Tool

Scanning Electron Microscopy

Scanning electron microscopy (SEM) provides Analog Devices' highest magnification and resolution for imaging samples, down to deep submicron geometries. A beam of electrons is focused and scanned over the area of interest, and the resulting secondary electrons are collected to give an image. Certain SEM applications use the beam to electrically stimulate the device. These techniques are electron beam induced current (EBIC), voltage contrast, charge induced voltage alteration (CIVA), and resistive contrast imaging (RCI). The environmental SEM (ESEM) application allows analysis of highly insulating samples by minimizing sample charging under the electron beam.

Figure 134. Scanning Electron Microscopy Station

Energy Dispersive X-Ray (EDX)

EDX is a technique used in conjunction with the SEM to qualitatively or semi-quantitatively determine elemental composition on a sample surface (Atomic Number 5 or higher). It is useful in cases where a contaminant is suspected.

Transmission Electron Microscopy (TEM)

TEM is a microscopy technique where a beam of electrons is transmitted through a thinned sample, which interacts with the sample as it passes through. The diffracted beam is then detected and processed after passing through the sample.

Focused Ion Beam (FIB) Cross Sectioning and Device Edit

The focused ion beam (FIB) system is Analog Devices' most advanced method of cross sectioning. It has many applications for the purposes of failure analysis, including precision cross sections through defect locations. It can selectively cut through interconnects, and tungsten probe pads can be deposited to isolate failures and allow electrical characterization. Device edits can also be performed, through exposure and severing of buried traces and/or rerouting conductors to other locations. These device edits can allow rapid process verification, fault isolation, and electrical testing that may otherwise be impossible. The dual-beam FIB combines an ion beam with a SEM column, allowing a small sample area to be cross sectioned and imaged simultaneously, allowing precise fault isolation to be used as an alternative to liquid crystal analysis.

CURRENT AND FUTURE EXPECTATIONS FOR RELIABILITY

INTRODUCTION

The electronics industry has always striven for the highest levels in quality and reliability. Anyone involved in the industry knows the pace with which the industry progresses and the methodologies the industry uses to guarantee high levels of quality and reliability. Over the last two decades, the emphasis has shifted from end-of-line statistically based stress testing to more proactive techniques. These techniques, embraced by Analog Devices, involve a shift in ownership and emphasis for reliability from reliability engineering to the process and product engineers. Consequently, the reliability engineering groups are the monitors and interpreters of the product and process reliability results. They work in a proactive manner as team members with the process and product developers to resolve any issues.

The reliability engineering groups are a valuable resource that actively investigates new process and package reliability issues before the technologies become available for full-scale manufacturing. Papers have been published by Schafft, Gerling, Riordan, Prendergast, and others [1 – 7, 20 – 22, 25, 25, 30 – 32], outlining the effectiveness of a proactive approach to reliability.

Building in reliability, proactive process control, and design for reliability are all phrases developed to quantify the new reliability revolution within the electronics industry. They constitute an organized method of moving toward improved product reliability. These phrases refer to methodologies and concepts brought about by cross-departmental cooperation, teamwork, and training that involve deploying reliability statistics, concepts, strategies, and techniques into all levels of product and process development.

The Analog Devices approach has been to work to ensure that the reliability of products and process is evaluated and characterized at advanced stages of product and process development. There are many examples to illustrate this approach [83 – 93]. An IEEE International Reliability Physics Symposium paper published in 1993 correlates yield, quality, and reliability for a particular failure mechanism.

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ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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