Welcome to the virtual design and evaluation environment of ADIsimPLL. The following presentation will guide you automatically through a series of screens that illustrate the superior functionality, unlimited flexibility, and user friendly interface this design and evaluation software tool has to offer. This software has been developed by engineers for engineers for the sole purpose of optimizing your designs making it faster and easier to accomplish your individual goals. From the entry-level engineer to the seasoned veteran, ADIsimPLL has an arsenal of onboard tools and options that are guaranteed to maximize the efficiency of your circuit design.

Click to Start

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Did you know... The ADF4116, ADF4117 and ADF4118 are pin compatible, lower phase noise replacements for the LMX2306, LMX2316 and LMX2326 single devices respectively. Drop-in replacements for the LMX dual devices are also available.

The ADF4116, ADF4117 and ADF4118 devices use fixed prescalers and can operate up to 3.0GHz. The ADF4110 through ADF4113 single PLL devices (and ADF4210 through ADF4213 dual PLL devices) allow control of prescaler division ratio and can operate up to 4.0GHz.

www.analog.com/pll
If this is the first time you have used SimPLL we would recommend running the tutorial.

The tutorial can be run at any later stage from the Help menu.

- Run Tutorial
- Do not show this again

OK
Welcome to the ADI SimPLL™ Tutorial

ADI SimPLL is the easy way to design, analyse and simulate Phase Locked Loop frequency synthesizers using the ADF4000 range of PLL ICs from Analog Devices. We will guide you through the design of a simple PLL and show how to analyse the performance (including phase noise, transient response, phase jitter, ACI, lock time to frequency and/or phase tolerances).

We will then demonstrate how to add and simulate features such as transient speedup techniques and lock detect circuits (both analogue and the newer digital filter circuits).

All this in an easy to use spreadsheet-like application.

Introducing the New PLL Wizard

In SimPLL all new designs start with the New PLL Wizard. This guides you through specifying the frequency requirements for the PLL, choosing the PLL chip, VCO and reference, and selecting the loop filter type. All choices can be altered later if desired.

For this tutorial we are going to design a PLL to cover 100MHz to 130MHz in 25kHz steps using an ADF4116 PLL IC. We have arranged the needed data to be pre-entered in the New PLL Wizard. Please work through the wizard, you may experiment with the buttons on any page, but to ensure that the PLL you design matches that in the tutorial, SimPLL will restore the original data before allowing you to proceed to the next page. Press Next on each page and Finish on the last page.
Tutorial - Frequency Requirements

Specifying Frequency Requirements

The frequency requirements for your PLL synthesizer are specified simply as the maximum and minimum frequencies of the required frequency range and the spacing of the channels within that range.

For our PLL we require the frequency range to be from 100MHz to 130MHz in 25kHz steps.

This data has already been entered on the next screen. Press Next to view the next screen and then press Next again to move onto selecting the PLL IC.
Output Frequency Requirements

Specify the Output Frequency requirements for your PLL synthesizer:

- Minimum Frequency: 100 MHz
- Maximum Frequency: 130 MHz
- Channel Spacing: 25.0 kHz

If you have a given reference frequency that you must use then check the box below and enter the frequency. Otherwise the reference frequency can be selected later.

Use Reference Frequency of:

All frequencies are entered in Hz. To enter 10 MHz simply type "10M" or "10e6". To enter 22.5kHz type "22.5k" or "22.5e3" and so on.
Selecting the PLL IC

On the next page you choose the PLL IC for your design. To assist in the selection there is a selection guide and access to detailed datasheets for all devices.

Once the chip is selected it is necessary to choose the Lock Detect Circuit and Speedup Circuit. The options in these fields are only enabled if the IC supports that option.

For the tutorial we have decided to start with an ADF4116 IC, analogue lock detect circuit and no speedup circuit. (We will change these later.)

Press Next to view the next screen and then press Next again to move onto selecting the VCO.
Selecting the VCO

The VCO can either be selected from one of our library files (or you can easily create your own library files - they are simple text files) or a custom idealised VCO. A library VCO can have a tabulated tuning law and tabulated phase noise data.

Selecting a custom VCO requires entering the tuning sensitivity \( K_v \). Phase noise can be added later in SimPLL.

For our initial investigations we are going to select a custom VCO with a \( K_v \) of 10MHz/V. Later we will specify phase noise for this VCO.

Press **Next** to view the next screen and then press **Next** again to move onto selecting the Reference frequency.
Select the VCO you wish to use, or choose 'custom' to enter detailed VCO characteristics later.

- From Library
  - VCO Library: user
  - VCO Model: tutorialVCO

- Custom
  - \( K_v = 10.0 \text{MHz/V} \)

For a custom VCO, enter the desired \( K_v \) in Hz/V (this can be changed later). For example, to enter 10 MHz/V, simply enter "10M" or "10e6". Phase noise data can be entered later.
Tutorial - Reference Specification

Selecting the Reference

Like the VCO, the Reference source can either be selected from one of our (or your) library files or a custom Reference. A library Reference oscillator can have tabulated phase noise data. Selecting a custom Reference simply requires entering the frequency. Phase noise can be added later in SimPLL.

For this tutorial the reference frequency is set to 10MHz.

Press Next to view the next screen and then press Next again to move onto selecting the Loop Filter.

For Help, press F1
PLL Reference Selection

Reference frequency must be between 25.00kHz and 100.0MHz and a multiple of 25.00kHz.

To use a crystal oscillator choose "custom" and enter the crystal frequency. For an external reference oscillator select it from the library, or use custom and enter the

- From Library
  - Ref. Library: user
  - Ref. Model: TCX010

- Custom
  - Frequency: 10.000MHz

For a custom Reference, enter the desired frequency in Hz. For example, to enter 10MHz simply enter "10M" or "10e6". Phase noise details can be entered later.

[Back] [Next] [Cancel] [Help]
Selecting the Loop Filter

SimPLL supports a number of loop filter topologies. Only those that are compatible with the speedup technique selected are shown. If an active filter is selected then the Op Amp selection is enabled, where you can select an op-amp from one of our (or your) library files.

We have decided to commence the tutorial with a simple two-capacitor passive filter.

Press Next to view the next screen and then press Finish to complete the Wizard and move into SimPLL proper to begin analyzing and optimizing the PLL we have designed.
Loop Filter Selection

Select the Loop Filter configuration. Filters shown match the Phase Detector and Speedup Mode selected earlier.

- Op Amp Selection
  - Ideal
  - Custom
  - Library

Op Amp Library: Analog Devices
Op Amp Model: AD711
Finding Your Way Around SimPLL

Let's have a quick look at the gadgets that will help you get around in SimPLL, and to get back to this tutorial.

Tutorial Navigation Buttons

These buttons are located in the lower right-hand corner of this document. They only appear when this tutorial is visible and are used to navigate between tutorial pages. Pressing >> advances to the next page, and << returns to the previous page.

To view the rest of this page you will need to use the scrollbar on the right.

Results Navigation Tabs

The navigation tab bar appears below this tutorial text. It is used to move between pages of results, and this Tutorial when it is running. (Normally there is no Tutorial tab.) Click on the other tabs to see the other pages, make sure that you return to this tutorial page when you are ready to continue. If all the other tabs are not visible, use the mouse to drag the splitter bar at the left end of the scrollbar. Alternatively, if you are short of screenspace, the arrows at the left end of the tabs can be used to bring the obscured tabs into view.

Main Screen

OK, so you are already finding your way around the SimPLL screen. We just need to name a few parts of the screen. In normal usage the main screen of SimPLL is divided into two parts as shown below:
Notes:
1. TSSOP pin numbers shown
2. Voc1 Analog Vcc
3. Voc2 Digital Vcc
4. Vp Charge Pump power supply
5. Voc1 = Voc2, Vp = Voc1
6. CE = 0V powers down chip
7. Consult manufacturer's data sheet for full details
Design1 analysed at 02/13/02 09:43:06

PLL Chip is ADF4116
VCO is custom
Reference is custom

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 114MHz

Phase Noise Table
Freq Total VCO Ref Chip Filter
100 -93.73 -- -- -93.81 -111.5
1.00k -88.97 -- -- -91.73 -92.25
10.0k -106.0 -- -- -110.5 -107.9
100k -145.7 -- -- -150.3 -147.6
1.00M -185.7 -- -- -190.3 -187.6

Phase jitter using brick wall filter
from 10.0kHz to 100kHz
Phase Jitter 0.02 degrees rms

Carrier Recovery phase jitter
Carrier recovery bandwidth 6.4kHz damping factor 0.7071
Symbol Filter cutoff 32.0kHz Butterworth with 3 poles
Phase Jitter 0.09 degrees rms

Residual FM
from 300 Hz to 5.00kHz is 8.52 Hz

FM SNR
sinusoidal modulation with 10.0kHz peak deviation
Signal to Noise Ratio = 58.4 dB

ACP - Channel 1
Channel 1 is centred 25.0kHz from carrier with bandwidth 15.0kHz
Power in channel = -78.6dBc

---- End of Frequency Domain Results ----
Thank you for taking time to preview

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