Mini Tutorial
MT-099

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Analog Circuit Simulation

Analog Devices, Inc.

IN THIS MINI TUTORIAL

The SPICE circuit simulation tool is explored in detail, including micromodeling vs. macromodeling for operational amplifiers.

INTRODUCTION

In recent years there has been much pressure placed on system designers to verify their designs with computer simulations before committing to actual printed circuit board layouts and hardware. Simulating complex digital designs is extremely beneficial, and very often the prototype phase can be eliminated entirely. The same is not true for most analog circuits. While simulation can give a greater degree of confidence in the final design, completely bypassing the prototype phase in high speed/high performance analog or mixed-signal circuit designs can be risky. For this reason, simulation must be accompanied with some amount of prototyping when dealing with analog circuits. Prototyping techniques are discussed in more detail in MT-100.

The most popular analog circuit simulation tool is the simulation program with integrated circuit emphasis (SPICE), available in multiple forms for various computer platforms. However, to achieve meaningful simulation results, designers need accurate models of many system components. The most critical of these are realistic models for integrated circuits.

The operational amplifier is a fundamental building block in nearly all analog circuits, and in the early 1990s, Analog Devices, Inc., developed an advanced operational amplifier SPICE model, which is still in use today. Within this innovative open amplifier architecture, gain and phase response can be fully modeled, enabling designers to accurately predict ac, dc, and transient performance behavior.

This modeling methodology also includes other devices such as instrumentation amplifiers, voltage references, and analog multipliers.

The following discussion relates to operational amplifiers and illustrates the fundamental principles. The following lists some major SPICE simulation objectives:

- Understanding realistic simulation goals
- Evaluating available models accordingly
- Knowing the capabilities for each competing operation amplifier model
- Breadboarding following the simulation

The popularity of SPICE simulation has led to many operational amplifier macromodel releases, which software mimics amplifier electrical performance. However, with numerous models available there may be uncertainty as to what is or is not modeled or the accuracy of a model. Consider these points when reviewing simulation results. Therefore, verification of a model is important, checking it by comparison to the actual device performance conditions before trusting it for serious designs.

A successful first design step using only an accurate operational amplifier model does not guarantee valid simulations. A simulation based on incomplete information has limited value. All parts of a target circuit must be modeled, including the surrounding passive components, various parasitic effects, and temperature changes. Then, the circuit must be verified in a lab by breadboarding and prototyping.

A breadboard circuit is a quickly executed mockup of a circuit design using a semipermanent lab platform, such as a breadboard circuit, that is less than final physical form. It is intended to show real performance, but without the total physical environment. A good breadboard can reveal behavior not predicted by SPICE because of an incomplete model, external circuit parasitics, or numerous other reasons. However, by using SPICE along with intelligent breadboarding techniques, a circuit can be efficiently and quickly designed with reasonably good assurance of working properly on a prototype version or a final printed circuit board (PCB).

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REVISION HISTORY

10/2016—Rev. 0 to Rev. A

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2/2009—Revision 0: Initial Version

MACROMODEL vs. MICROMODEL

The distinction between macromodel and micromodel is often unclear. A micromodel uses the transistor level and other SPICE models of an IC device, with all active and passive parts fully characterized according to the manufacturing process. In differentiating this type of model from a macromodel, some authors use the term device level model to describe the resulting overall operational amplifier model (see the References section). Typically, use a micromodel in the design process of an IC.

A macromodel is a less complex way to simulate operational amplifier performance. Taking into consideration final device performance, it uses ideal native SPICE elements to model observed behavior. When developing a macromodel, a real device is measured in terms of lab and data sheet performance and is adjusted to match this behavior. Some aspects of performance can be sacrificed in doing this. Table 1 compares the major advantages and disadvantages between macromodels and micromodels.

Table 1. Comparison of Macromodels and Micromodels

Model	Methodology	Advantages	Disadvantages
Macromodel	Ideal elements model device behavior	Fast simulation time, easily modified	May not model all characteristics
Micromodel	Fully characterized transistor level circuit	Most complete model	Slow simulation possible, convergence, difficulty, nonavailability

There are advantages and disadvantages to both models. A micromodel can give a complete and accurate model of operational amplifier circuit behavior under almost all conditions. But, because of a large number of transistors and diodes with nonlinear junctions, simulation time is very long. Of course, manufacturers are also reluctant to release such models, since they contain proprietary information. Although all transistors can be included, it does not guarantee total accuracy, as the transistor models do not cover all operational regions precisely. Furthermore, with a high node count, SPICE can have convergence difficulties, causing a failed simulation. This point makes a micromodel virtually useless for multiple amplifier active filters.

A carefully developed macromodel can produce both accurate results and simulation time savings. In more advanced macromodels, transient and ac device performance can be similarly replicated. Operational amplifier nonlinear behavior can also be included, such as output voltage and current swing limits.

However, because these macromodels are still simplifications of real devices, all nonlinearities are not modeled. For example, not all SPICE models include common-mode input voltage range or noise. Typically, in model development, parameters are optimized specifically for the intended application; for example, ac and transient response.

Including every possible characteristic can lead to cumbersome macromodels that can have convergence problems. Thus, SPICE macromodels include those operational amplifier behavior characteristics critical to intended performance for normal operating conditions, but not necessarily all nonlinear behavior.

THE SPICE OPERATIONAL AMPLIFIER MACROMODELS

The basic SPICE model was developed as an operational amplifier macromodeling advance and as an improved design tool for more accurate application circuit simulations. Since being introduced in 1990, it has become a standard operational amplifier macromodel topology, as evidenced by industry adoption of the frequency shaping concepts; refer to AN-840 and AN-856.

Prior to about 1990, a dominant operational amplifier model architecture was the Boyle model (see the References section). This macromodel, developed in the early 1970s, cannot accurately model higher speed amplifiers. The primary reason for this is that it has limited frequency shaping ability—only two poles and no zeroes. In contrast, the SPICE model topology has a flexible and open architecture, allowing virtually unlimited pole and zero frequency shaping stages to be cascaded. This difference provides a more accurate ac and transient response compared to the more simplistic Boyle model topology.

A SPICE model is comprised of three main stages. The first is a combined input and gain stage that includes transistor models appropriate to the device being modeled (for example, NPN bipolar transistor, PNP bipolar transistor, junction gate field-effect transistor (JFET), or metal–oxide–semiconductor field-effect transistor (MOSFET)).

The second stage is the synthetic pole and zero stage, comprising of ideal SPICE native elements. Depending on the frequency response of the operational amplifier, there can be few to many pole and zero stages. The third stage is an output stage, which couples the first two sections to the outside world.

Before describing these sections in detail, it is important to realize that many variations upon the following techniques do exist. This is due to not just differences from one operational amplifier model to another, but also to evolutionary topology developments in operational amplifier hardware, which leads to corresponding modeling changes. For example, modern operational amplifiers often include either rail-to-rail output stages, rail-to-rail input stages, or both. Consequently, more recent developments in the SPICE models have addressed these issues, along with corresponding model developments.

Furthermore, although the Boyle model and the original SPICE models are designed to support voltage feedback operational amplifier topologies, subsequent additions have added current feedback amplifier topologies. Reference 9 describes an SPICE current feedback macromodel which appeared just shortly after the voltage feedback model of Reference 3.

These current feedback macromodels are discussed in more detail in the following sections.

Input and Gain/Pole Stages

A basic SPICE voltage feedback operational amplifier macromodel input stage is shown in Figure 1 and uses what are typically the only transistors in the entire model. The example in Figure 1 shows the Q1 to Q2 NPN pair. These are needed to properly model the differential input stage characteristics of an operational amplifier. This stage is designed for unity gain by the proper choice of the Q1 to Q2 operating current and gain setting resistors R3 to R4 and R5 to R6.

Although this example uses NPN transistors, the input stage is easily modified to use PNP bipolars, JFET, or MOSFET devices. The rest of the input stage uses simple SPICE elements such as resistors, capacitors, and controlled sources.

The open-loop gain vs. frequency characteristics of the modeled operational amplifier is provided by the gain stage (see Figure 1).

The controlled source, gm_1, senses the differential collector voltage, V_D, from the input stage, converting V_D to a proportional current. The gm_1 output current flows into load Resistor R7, producing a single-ended voltage referenced to an internal voltage, EREF. Typically, this voltage is derived as a supply voltage midpoint and is used throughout the model.

By making the gm_1 to R7 product equal to the specified gain of the operational amplifier, this stage produces the entire open-loop gain of the macromodel. This design factor means that all other model stages operate at unity gain, a feature leading to significant flexibility in adding and deleting subsequent stages. This approach allows the quick synthesis of the complex ac characteristics typical of high performance, high speed operational amplifiers. In addition, this stage also provides the dominant pole of the amplifier ac response. The open-loop pole frequency is set by selection of capacitor C3, as noted in the diagram.

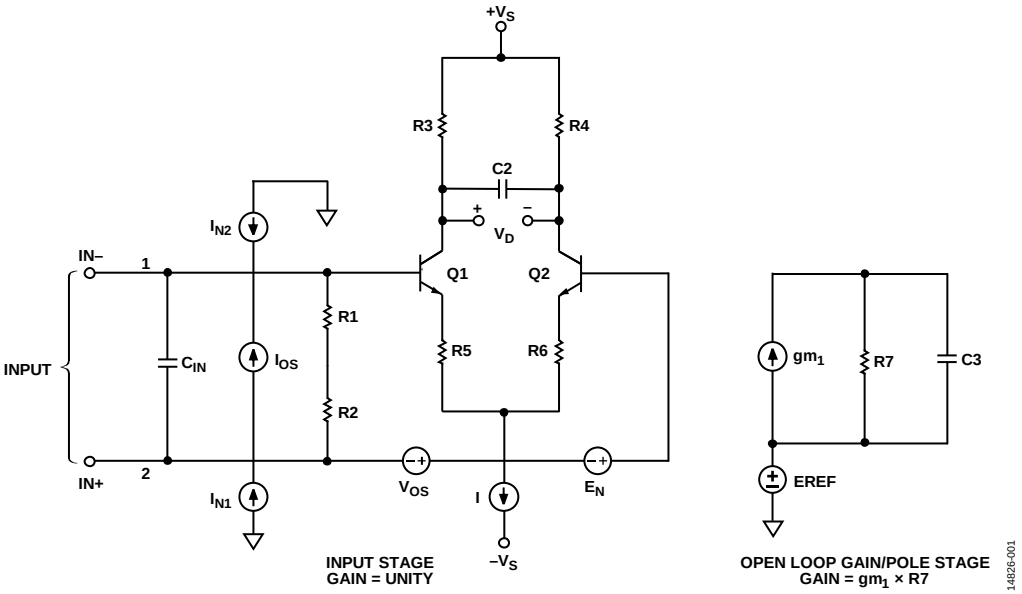

Figure 1. Input and Gain/Pole Stages of SPICE Macromodel

Frequency Shaping Stages

Following the gain stage of the macromodel is a variable, but unlimited, number of pole and/or zero stages, which in combination provide frequency response shaping. Typical topologies for these stages are as shown in Figure 2. The stages can be either a single pole, a single zero, or combined pole/zero or zero/pole stages. All such stages have a dc transfer gain of unity and a given amplifier type can have all or just a few of these stages, as can be require to synthesize the response.

The pole or zero frequency is set by the combination of the resistor(s) and capacitor or resistor(s) and inductor. Because an infinite number of values are possible in SPICE, choice of resistor/capacitor (RC) values is somewhat arbitrary, and a wide range work. Early SPICE models used relatively RC high values, while more recent models employ lower RC values to reduce noise (described in more detail later). In all instances, it is assumed that each stage provides zero loading to the driving stage. The stages shown reflect no particular operational amplifier, but example principles can be found within the OP27 model.

Because all of these frequency shaping stages are dc-coupled and have unity gain, any number of the stages can be added or deleted with no affect on the model low frequency response. Most importantly, the high frequency gain and phase response can be tailored to match a real amplifier response. The benefits of this frequency shaping flexibility are apparent in performance comparisons of the SPICE model closed-loop pulse response and stability analysis, versus a more simplistic model. This point is demonstrated in the Transient Response section.

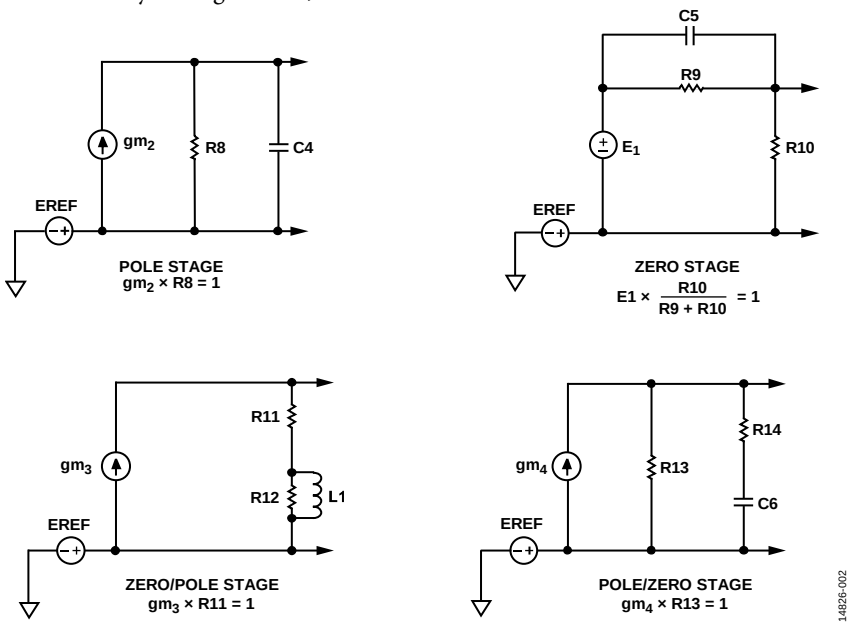

Figure 2. The Frequency Shaping Stages Possible Within the SPICE Model

Output Stages

A general form of the output stage for the SPICE model, shown in Figure 3, models a number of important operational amplifier characteristics. The Thevenin equivalent resistance of R_{O1} and R_{O2} mimics the operational amplifier dc open-loop output impedance, while the inductor local oscillator (LO) models the rise in impedance at high frequencies. A unity-gain characteristic for the stage is set by the g_7 to R_{O1} and g_8 to R_{O2} products. Additionally, output load current is correctly reflected in the supply currents. This feature is a significant improvement over the Boyle model because the power consumption of the loaded circuit can be analyzed accurately. Furthermore, circuits using the operational amplifier supply currents as part of the signal path can also be correctly simulated. The output stage, shown in Figure 3, is not intended to reflect any particular operational amplifier, but resembles the AD817.

With the recent advent of numerous rail-to-rail output stage operational amplifiers, there are currently customized model topologies. This expands the SPICE library to include rail-to-rail model behavior, matching operational amplifier architectures using P and N MOSFET devices, as well as bipolar devices. Characteristically, a rail-to-rail output stage includes several key differentiating performance points.

The first point is the ability to swing the operational amplifier output within a few mV of both supplies. The second point is that such an output stage has a voltage gain greater than one. The third point is the relatively high output impedance, which is high contrasted to traditional emitter follower outputs.

Examples of several modeling approaches to rail-to-rail output stages are found in the ADI SPICE macromodel library. The OP295 employs complementary metal-oxide semiconductor (CMOS) devices to realize a rail-to-rail output, while the OP284 uses bipolar devices to the same end. The macromodels of the AD8031 and AD823 use synthesis techniques to model rail-to-rail outputs. The AD8051/AD8052/AD8054, AD8552, and AD623 utilize combinations of selected discrete device models and synthesis techniques, to realize rail-to-rail output operation for both operational amplifier and instrumentation amplifier devices.

In addition to rail-to-rail output operation, many modern operational amplifiers also feature rail-to-rail input stages. Such stages essentially duplicate, for example, an NPN-based differential stage with a complementary PNP stage, both stages operating in parallel. This allows the operational amplifier to provide a common-mode (CM) range that includes both supply rails. This performance feature can also be accomplished within CMOS operational amplifiers, using both a P and N type CMOS differential pairs. Model examples reflecting rail-to-rail input stages include the OP284, AD8031, and AD8552.

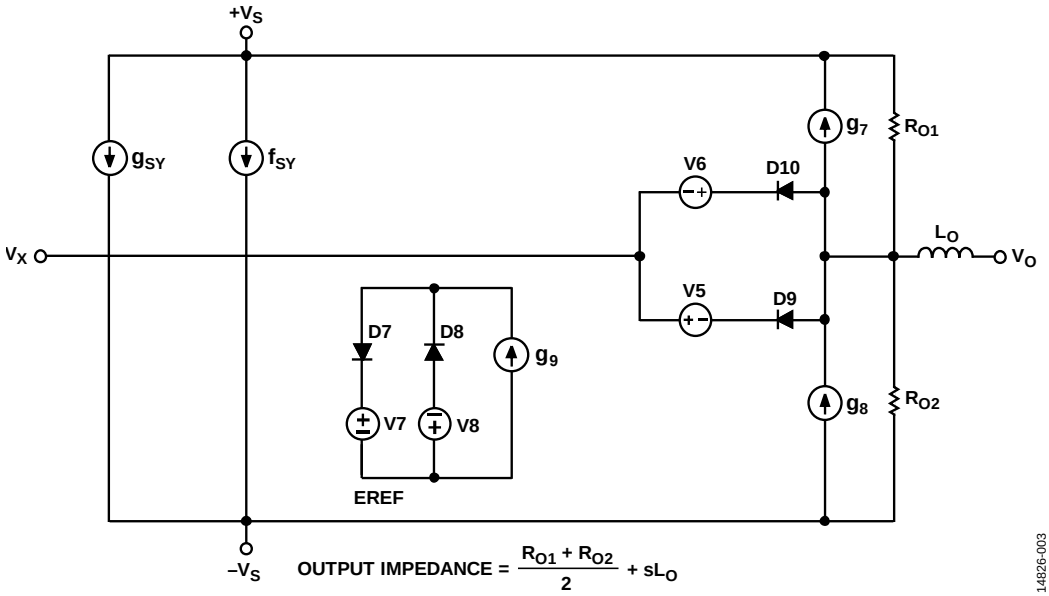

Figure 3. General-Purpose Macromodel Output Stage

Transient Response

The performance advantage of the multiple pole/zero stages is readily demonstrated in a transient pulse response test (see Figure 4 to Figure 6). These figures compare the OP249 operational amplifier, the SPICE model, and the Boyle model. It reveals the improved execution resulting from the unlimited number of poles and zeros in this model.

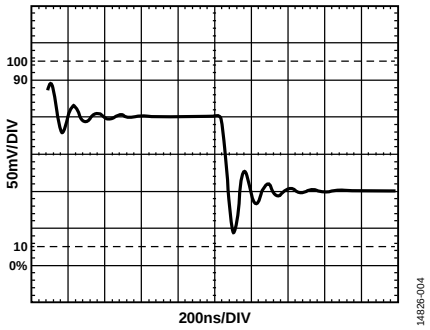

Figure 4. Pulse Response Comparison of an OP249 Follower

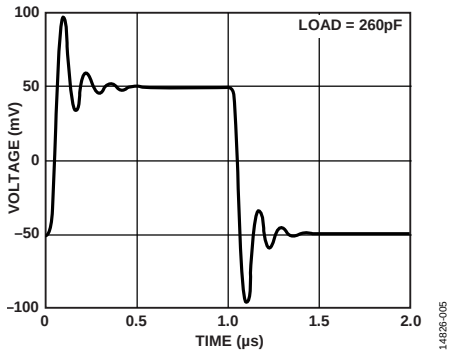

Figure 5. Model Favors the SPICE Model in Terms of Fidelity

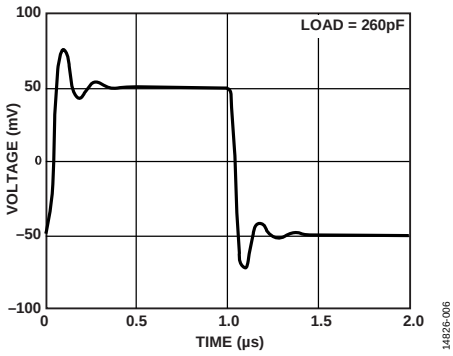

Figure 6. Model Does Not Favor the Boyle Model in Terms of Fidelity

Using the OP249 amplifier, with the output connected to the inverting input and a 260 pF capacitive load, Figure 4 to Figure 6 shows the transient analysis plots for a unity gain follower circuit.

This results in ringing, shown in Figure 4. Note that the SPICE model accurately predicts the amount of overshoot and frequency of the damped ringing (see Figure 5). In contrast, the Boyle model (see Figure 6) predicts about half the overshoot and significantly less ringing.

Noise Model

An important enhancement to the SPICE model is the ability to realistically model noise performance of an operational amplifier and is easier than analyzing noise by hand. A complete analysis is an involved and tedious task that involves adding all individual noise contributions from all active devices and all resistors in use, and referring them to the input.

To aid this task, the SPICE model is enhanced to include noise generators that accurately mimic the broadband and 1/f noise of an operational amplifier.

Conceptually, this involves making an existing model noiseless and then adding discrete noise generators to emulate the target device. As noted earlier, all Analog Devices models are not necessarily designed for this noise accurate performance. Selected device models are designed for noise, however, when typical uses include low noise applications.

The first step is an exercise in scaling down the model internal impedances. For example, by reducing the resistances in the pole/zero stages from a base resistance of 1 MΩ to 1 Ω, total noise is reduced dramatically, shown in Figure 7 and Table 2.

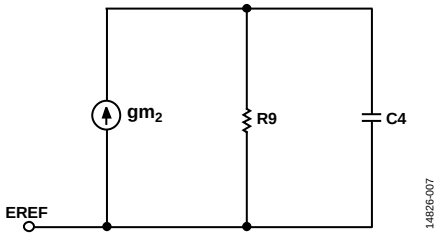

Figure 7. Reducing Pole/Zero Cell Impedances to Low Values to Achieve Low Noise Operation

Table 2. Parameter Noise Comparison

Parameter	Noisy	Noiseless
R9	1×10^6 Ω	1 Ω
gm_2	1×10^{-6}	1.0
C4	159×10^{-15}	159×10^{-8}
Noise	129 nV/√Hz	129 pV/√Hz

In the Noisy column of Table 2, the noise from the pole stage with a large R9 resistor value is 129 nV/√Hz. But when this resistor is scaled down by a factor of 1×10^6 to 1 Ω in the Noiseless column, stage noise is 129 pV/√Hz. The transconductance and capacitance values are also scaled by the same factor, maintaining the same gain and pole frequency. To make the input stage of the model noiseless, it is operated at a high current and with reduced load resistances, making noise contributions negligible. Extending these techniques to the entire model renders it essentially noiseless.

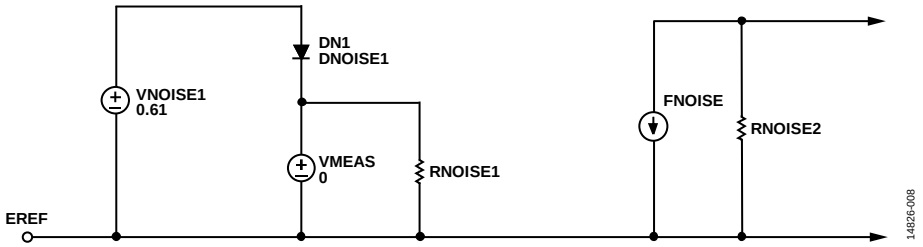

Figure 8. A Basic SPICE Noise Generator Formed with Diodes, Resistors, and Controlled Sources

Once achieving global noise reduction is achieved, add independent noise sources, one for voltage noise and two for current noise. The basic noise source topology used as seen in Figure 8, and can be set up to produce both voltage and current noise outputs.

Within SPICE, semiconductor models can generate flicker noise (1/f). The noise generators use diodes, such as DN1, to produce this portion of the noise, modeling the 1/f noise of the operational amplifier. By properly specifying diode model parameters and bias voltage VNOISE1, the 1/f noise is tailored to match the operational amplifier. The noise current from DN1 passes through a zero voltage source. Here, VMEAS is used as a measurement device, combining the 1/f noise from DN1 and the broadband noise from RNOISE1.

RNOISE1 is selected to provide an appropriate broadband noise (see Figure 8). The combined noise current in VMEAS is monitored by FNOISE (see Figure 8), and appears as a voltage across RNOISE2. This voltage is injected in series with one amplifier input via a controlled voltage source, such as E_N of Figure 1. Use either FNOISE or a controlled voltage source coefficient for overall noise voltage scaling.

Current noise generation is similar, except the RNOISE2 voltage producing resistor is not used and two current controlled sources drive the amplifier inputs. With all noise generators symmetrical about ground, dc errors are not introduced.

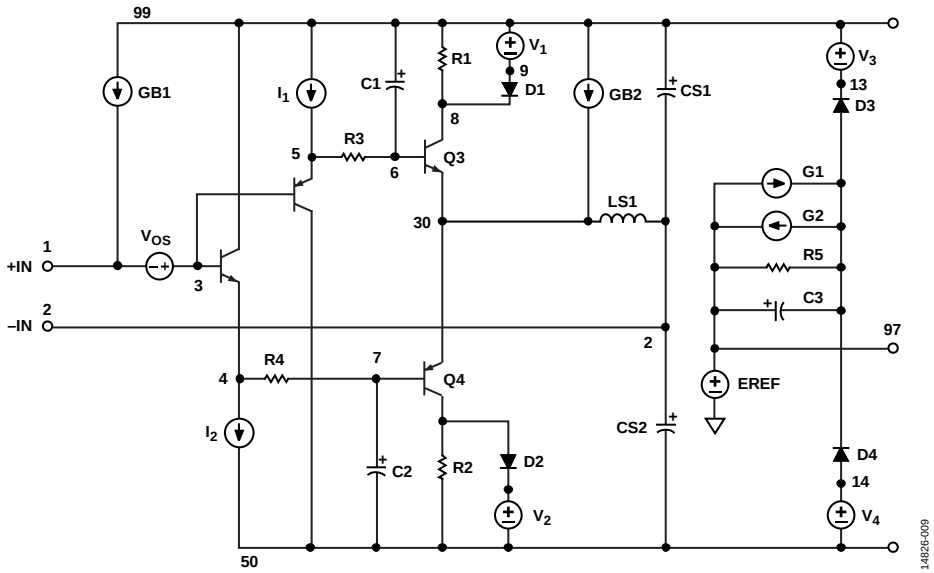

Figure 9. Input and Gain Stages of Current Feedback operational amplifier Macromodel

CURRENT FEEDBACK AMPLIFIER MODELS

As noted previously, a new model topology is developed for current feedback amplifiers to accommodate the unique input stage structure. The model uses a topology, shown in Figure 9, for the input and gain stages. The remaining model portions (not shown) contain multiple pole/zero stages and the output stage, and are essentially the same as voltage feedback amplifiers, described previously in the Input and Gain/Pole Stages section.

The four bipolar transistor input stage resembles actual current feedback amplifiers, with a high impedance noninverting input (+IN) and a low impedance inverting input (–IN). In current feedback amplifiers, the maximum slew rate is very high, because dynamic slew current is not limited to a differential pair tail current (voltage feedback operational amplifiers). In current feedback operational amplifier designs, much larger amounts of error current can flow in the inverting input, as developed by the feedback network. Internally, this current flows in either Q3 or Q4, and charges the C3 compensation capacitor via current mirrors.

The current mirrors of the SPICE model are actually voltage controlled current sources in the G1 and G2 gain stages. They sense voltage drops across the R1 and R2 input stage resistors, and translate into the C3 charging current. By making the value of G1 and G2 equal to the R1 to R2 reciprocal, the slew currents are identical. By clamping the R1 to R2 voltage drops via D1 to V1 and D2 to V2, the maximum current is limited, setting the highest slew rate. Open loop gain or transresistance of the model is set by R5 and the open loop pole frequency by C3 to R5 (see Figure 1). The output from across R5 to C3 (Node 12) drives the succeeding frequency shaping stages of the model, and EREF is again an internal reference voltage.

A unique property of current feedback amplifiers is that bandwidth is a function of the feedback resistor and the internal compensation capacitor, C3. The lower the feedback resistor, the greater the bandwidth, until a practical lower limit is reached, that is, the value at which the device oscillates. As the model includes a low impedance inverting input, it accurately mimics real device behavior as radio frequency (RF) is altered. Figure 10 to Figure 12 compares the SPICE model to the AD811 video amplifier. As shown in Figure 10 and Figure 11, the model accurately predicts the gain roll-off at the much lower frequency for the 1 kΩ feedback resistor as opposed to the 500 Ω resistor.

The current feedback amplifier input and gain stage is an enhancement to the SPICE model that increases flexibility in modeling different operational amplifier devices and provides a net increase in design cycle speed.

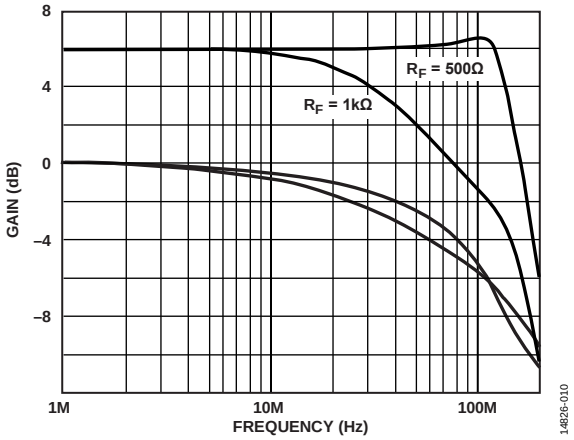

Figure 10. Real AD811 Current Feedback Operational Amplifier

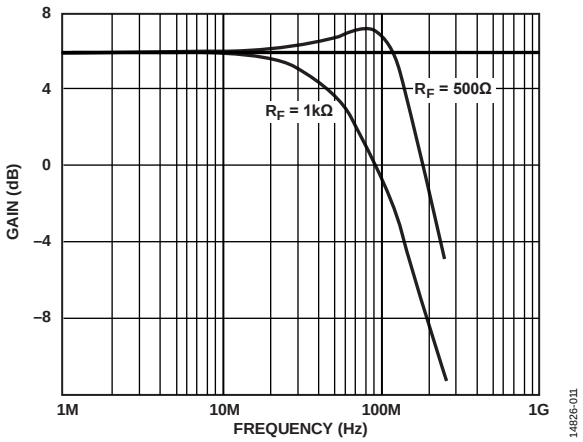

Figure 11. Macromodel AD811 Current Feedback Operational Amplifier

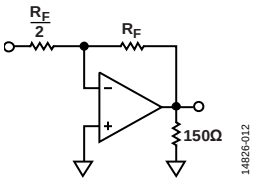

Figure 12. AD811 Simulation Circuit

MODELING PC BOARD PARASITICS

PCB parasitics can have significant impact on the performance of a circuit. This is especially true for high speed circuits. A few picofarads of capacitance on the input node can determine whether a circuit is stable or oscillates and must be carefully considered when simulating the circuit to achieve meaningful results.

To illustrate the impact of PCB parasitics, the simple voltage follower circuit of Figure 14 is built on a carefully laid out PCB and on a component plug in type of prototype board. Use the AD847 operational amplifier because of the50 MHz bandwidth, making the parasitic effects more critical (smaller values of capacitance have a greater effect on results).

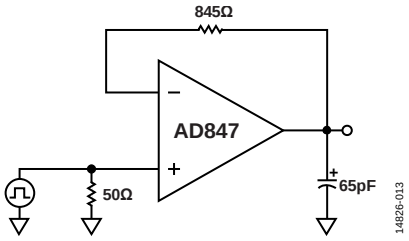

Figure 13. Voltage Follower

As a result, this circuit executed on a carefully laid out PCB has a clean response with minor overshoot and ringing (see Figure 14). The SPICE model results also closely agree with the real device, showing a corresponding simulation (see Figure 15).

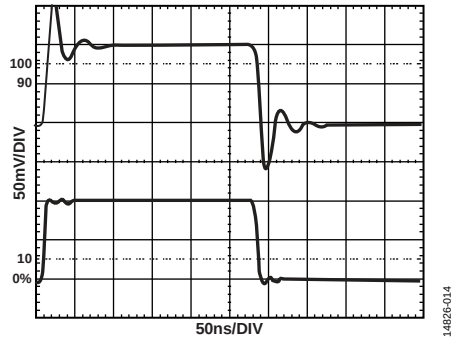

Figure 14. Lab Testing Results

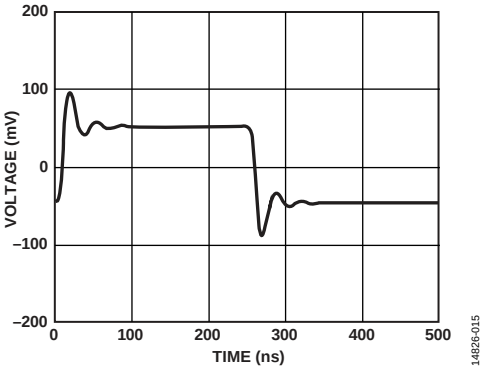

Figure 15. Simulation Results

However, the same circuit built on the plug in prototype board shows distinctly different results. In general, the prototype board shows worse performance due to the relatively high nodal capacitances around the operational amplifier inputs, degrading the square wave response to severe ringing, much less than the full capability of the device (see Figure 16 and Figure 17).

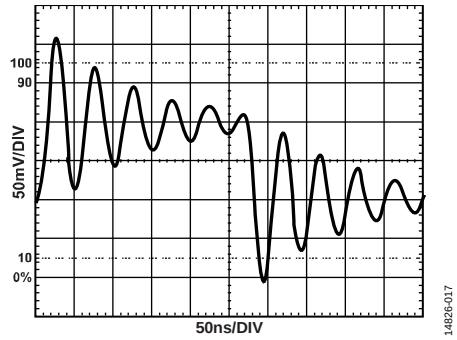

Figure 16. Without Low Parasitics, Lab Testing Results Show Convergence With A Poorly Damped Response

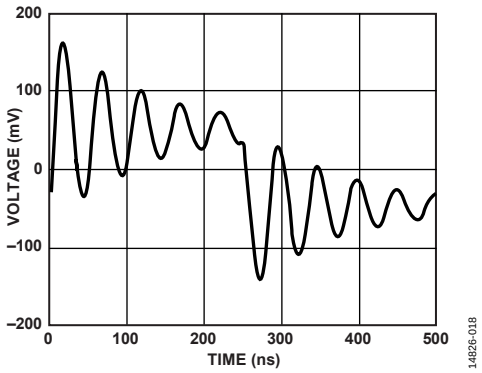

Figure 17. Without Low Parasitics, Parallel Simulation Show Convergence With A Poorly Damped Response

The voltage follower circuit, Figure 18, shows the additional capacitances as inherent to the prototype board. With this test circuit and corresponding analysis, there is, initially, no agreement between the poor lab test and the parallel SPICE test. However, when the relevant PCB parasitic capacitances are included in the SPICE file, then the simulation results do agree with the real circuit, as noted in the right picture.

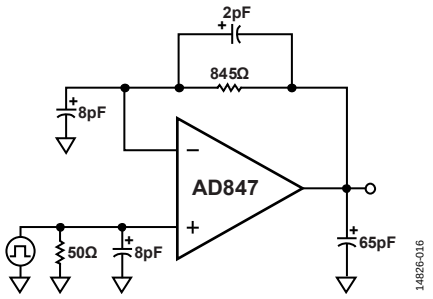

Figure 18. Voltage Follower Circuit

This example illustrates several key points. One, PCB parasitics can easily make a high speed circuit behave differently from a simplistic SPICE analysis. Secondly, when the SPICE netlist is adjusted to more reasonably reflect the parasitic elements of a PCB, then the simulation results do compare with the actual lab test. Finally, a clean PCB layout with minimal parasitics is critically important to high speed designs operating at 1 GHz or higher.

The simulation can also be used as a rough measure of the PCB layout design. If the simulation, without any parasitics, agrees with the PCB, then there is a reasonable assurance the PCB is carefully laid out.

Parasitic PCB elements are not the only area that can cause differences between the simulation and the breadboard. A circuit can exhibit nonlinear behavior during power-up that causes a device to lock up. Or, a device can oscillate due to insufficient power supply decoupling or lead inductance.

SPICE circuits do not need bypassing, but real world ones always need bypassing. It is impossible to anticipate all normal or abnormal operating conditions to which an amplifier might be subjected.

It is always important to prototype circuits and thoroughly check them in the lab. Careful forethought in these stages of design minimizes any unknown problems from showing up when the final PCBs are manufactured.

OTHER DESIGN AND SIMULATION TOOLS

Analog Devices has a large number of useful design tools located at the Design Center on the Analog Devices website.

ADIsimPE, which is powered by SIMetrix/SIMPLIS, is a circuit simulation suite optimized for the design and development of analog and mixed signal circuits. The SIMetrix mode is ideal for the simulation of general nonswitching circuits. It provides full PSpice® compatibility for use with industry-standard SPICE models. The SIMPLIS mode simulates the operation of switching circuits with vastly improved robustness, speed, and accuracy compared to standard SPICE models. It is particularly useful for switching power supply, phase-locked loops (PLLs), and analog-to-digital converter (ADC)/digital-to-analog converter (DAC) applications.

ADIsimPE includes the following:

- Extensive library of Analog Devices IC models and application schematics.
- Full schematics capture and editing capabilities with easy waveform viewing and analysis.
- SPICE mode SIMetrix simulation ideal for operational amplifiers, references, and linear regulators.
- SIMPLIS mode simulation optimized for switching power supplies and PLLs.
- Integration capability with ADIsimPower design tools.
- Supported by EngineerZone.

REFERENCES

L. W. Nagel, "SPICE2: A Computer Program to Simulate Semiconductor Circuits," May 1975, UCB/ERL M75/520, Univ. of California, Berkeley, CA, 94720.

Andrei Vladimirescu, K.Zhang, A.R.Newton, D.O.Pederson, "SPICE Version 2G User's Guide," August 1981, Department of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, CA, 94720.

Mark Alexander, Derek Bowers, "SPICE-Compatible Op Amp Macro-Models," *EDN*, February 15, 1990 and March 1, 1990 (available as Analog Devices, Inc. AN-138).

Joe Buxton, "Analog Circuit Simulation**,"** Chapter 13 of *Amplifier Applications Guide*, 1992, Analog Devices, Inc., Norwood, MA, ISBN 0-916550-10-9.

Andrei Vladimerescu, *The SPICE Book*, John Wiley & Sons, New York, 1994, ISBN 0-471-60926-9.

"Development of an Extensive SPICE Macromodel for 'Current-Feedback' Amplifiers," National Semiconductor AN-840, July 1992.

David Hindi, "A SPICE Compatible Macromodel for CMOS Operational Amplifiers," National Semiconductor AN-856, September 1992.

Boyle, et al, "Macromodelling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid State Circuits,* Vol. SC-9, No. 6, December 1974.

Derek Bowers, Mark Alexander, Joe Buxton, "A Comprehensive Simulation Macromodel for 'Current Feedback' Operational Amplifiers," *IEE Proceedings*, Vol. 137, Pt. G, # 2, April 1990.

PSpice® simulation software, http://www.pspice.com/.

Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 12.

Walter G. Jung, *Operational Amplifier Applications*, Analog Devices, 2002, ISBN 0-916550-26-5, Chapter 7. Also available as *Operational Amplifier Applications Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7844-5. Chapter 7.

Walt Kester, *High Speed System Applications*, Analog Devices, 2006, ISBN-10: 1-56619-909-3, ISBN-13: 978-1-56619-909-4, Part 4.

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