
Analog Switches and Multiplexers Basics

INTRODUCTION

Solid-state analog switches and multiplexers have become an essential component in the design of electronic systems which require the ability to control and select a specified transmission path for an analog signal. These devices are used in a wide variety of applications including multi-channel data acquisition systems, process control, instrumentation, video systems, etc.

Switches and multiplexers of the late 1960s were designed with discrete MOSFET devices and were manufactured in small PC boards or modules. With the development of CMOS processes (yielding good PMOS and NMOS transistors on the same substrate), switches and multiplexers rapidly gravitated to integrated circuit form in the mid-1970s, with product introductions such as the Analog Devices' popular AD7500-series (introduced in 1973). A dielectrically-isolated family of these parts introduced in 1976 allowed input overvoltages of ± 25 V (beyond the supply rails) and was insensitive to latch-up.

These early CMOS switches and multiplexers were typically designed to handle signal levels up to ± 10 V while operating on ± 15 -V supplies. In 1979, Analog Devices introduced the popular ADG200-series of switches and multiplexers, and in 1988 the ADG201-series was introduced which was fabricated on a proprietary linear-compatible CMOS process (LC²MOS). These devices allowed input signals to ± 15 V when operating on ± 15 -V supplies.

A large number of switches and multiplexers were introduced in the 1980s and 1990s, with the trend toward lower on-resistance, faster switching, lower supply voltages, lower cost, lower power, and smaller surface-mount packages.

Today, analog switches and multiplexers are available in a wide variety of configurations, options, etc., to suit nearly all applications. On-resistances less than 0.5Ω , picoampere leakage currents, signal bandwidths greater than 1 GHz, and single 1.8-V supply operation are now possible with modern CMOS technology. Industrial products are also available which operate on ± 15 V supplies using Analog Devices' [iCMOS®](#) (industrial CMOS) process.

Although CMOS is by far the most popular IC process today for switches and multiplexers, bipolar processes (with JFETs) and complementary bipolar processes (also with JFET capability) are often used for special applications such as video switching and multiplexing where the high performance characteristics required are not attainable with CMOS. Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time is generally not fast enough, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch on-resistance with signal level (R_{ON} modulation) can introduce unwanted distortion in differential gain and phase. Multiplexers based on complementary bipolar technology offer better solutions at video frequencies—with obvious power and cost increases above CMOS devices.

CMOS SWITCH BASICS

The ideal analog switch has no on-resistance, infinite off-impedance and zero time delay, and can handle large signal and common-mode voltages. Real CMOS analog switches meet none of these criteria, but if we understand the limitations of analog switches, most of these limitations can be overcome.

CMOS switches have an excellent combination of attributes. In its most basic form, the MOSFET transistor is a voltage-controlled resistor. In the "on" state, its resistance can be less than 1 Ω , while in the "off" state, the resistance increases to several hundreds of megohms, with picoampere leakage currents. CMOS technology is compatible with logic circuitry and can be densely packed in an IC. Its fast switching characteristics are well controlled with minimum circuit parasitics.

MOSFET transistors are bilateral. That is, they can switch positive and negative voltages and conduct positive and negative currents with equal ease. A MOSFET transistor has a voltage controlled resistance which varies nonlinearly with signal voltage as shown in Figure 1.

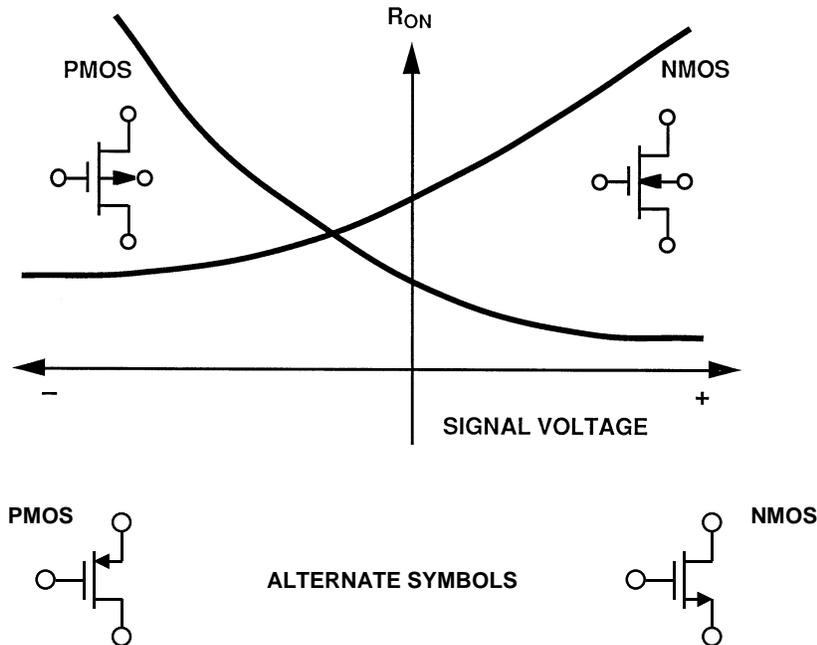


Figure 1: MOSFET Switch ON-Resistance Versus Signal Voltage

The complementary-MOS process (CMOS) yields good P-channel and N-channel MOSFETs. Connecting the PMOS and NMOS devices in parallel forms the basic bilateral CMOS switch of Figure 2. This combination reduces the on-resistance, and also produces a resistance which varies much less with signal voltage.

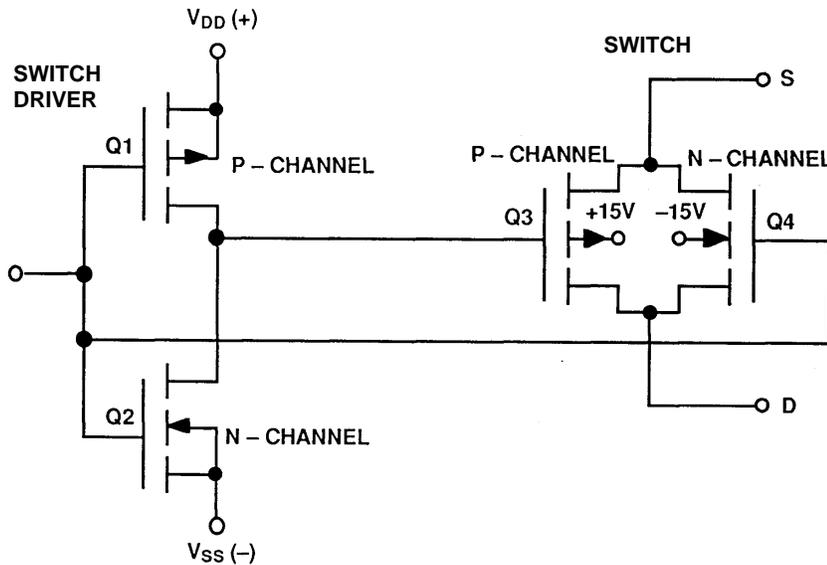


Figure 2: Basic CMOS Switch Uses Complementary Pair to Minimize R_{ON} Variation due to Signal Swings

Figure 3 shows the on-resistance changing with channel voltage for both N-type and P-type devices. This nonlinear resistance can cause errors in dc accuracy as well as ac distortion. The bilateral CMOS switch solves this problem. On-resistance is minimized, and linearity is also improved. The bottom curve of Figure 3 shows the improved flatness of the on-resistance characteristic of the switch.

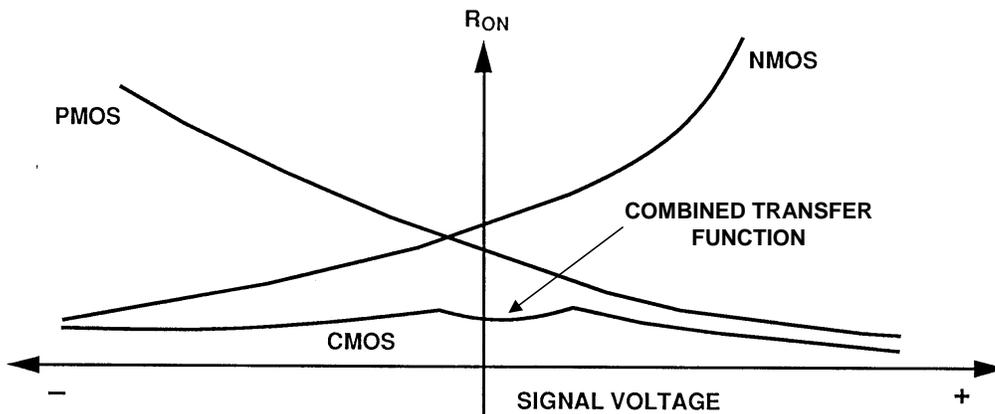


Figure 3: CMOS Switch ON-Resistance Versus Signal Voltage

The [ADG8xx-series](#) of CMOS switches are specifically designed for less than 0.5Ω on-resistance and are fabricated on a sub-micron process. These devices can carry currents up to 400 mA, operate on a single 1.8 V to 5.5 V supply (depending on the particular device), and are rated over an extended temperature range of -40°C to $+125^{\circ}\text{C}$. Typical on-resistance over temperature and input signal level is shown in Figure 4.

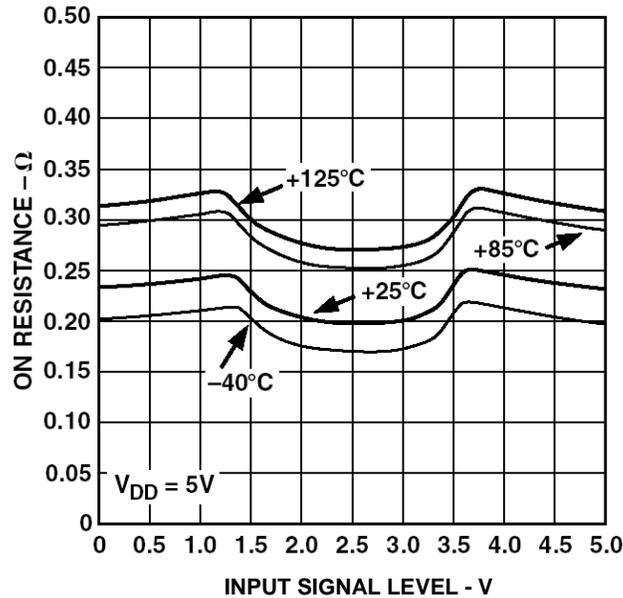


Figure 4: ON-Resistance Versus Input Signal for [ADG801/ADG802](#) CMOS Switch, $V_{DD} = +5\text{ V}$

ERROR SOURCES IN THE BASIC CMOS SWITCH

It is important to understand the error sources in an analog switch. Many affect ac and dc performance, while others only affect ac. Figure 5 shows the equivalent circuit of two adjacent CMOS switches. The model includes leakage currents and junction capacitances.

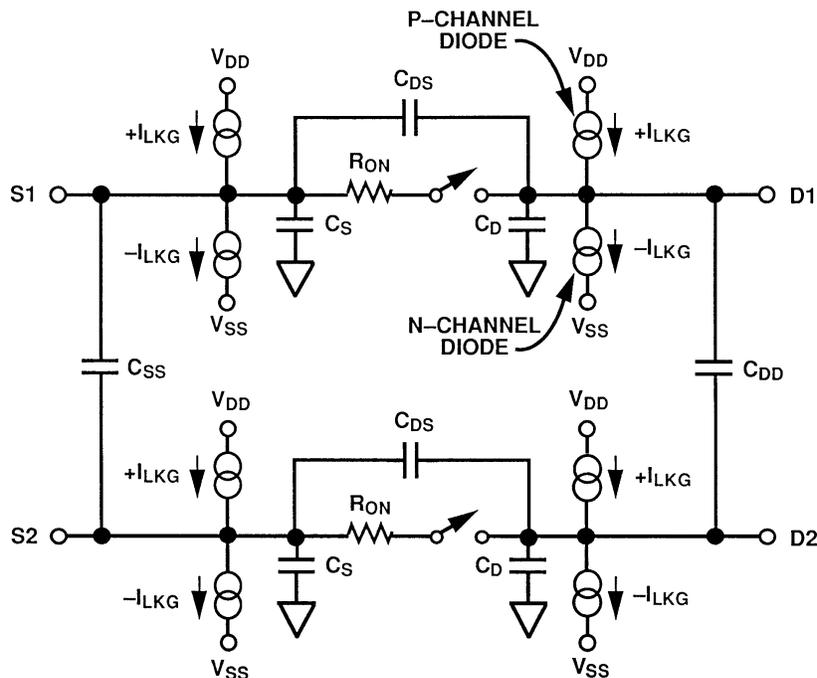
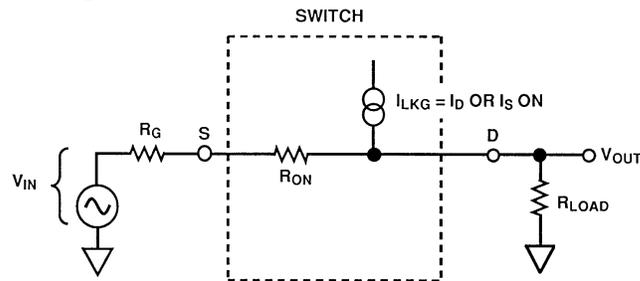


Figure 5: Equivalent Circuit of Two Adjacent CMOS Switches

DC errors associated with a single CMOS switch in the on state are shown in Figure 6. When the switch is on, dc performance is affected mainly by the switch on-resistance (R_{ON}) and leakage current (I_{LKG}). A resistive attenuator is created by the R_G - R_{ON} - R_{LOAD} combination which produces a gain error. The leakage current, I_{LKG} , flows through the equivalent resistance of R_{LOAD} in parallel with the sum of R_G and R_{ON} .

Not only can R_{ON} cause gain errors—which can be calibrated using a system gain trim—but its variation with applied signal voltage (R_{ON} modulation) can introduce distortion—for which there is no calibration. Low resistance circuits are more subject to errors due to R_{ON} , while high resistance circuits are affected by leakage currents. Figure 6 also gives equations that show how these parameters affect dc performance.



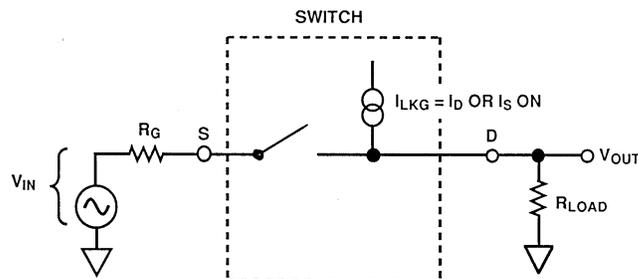
$$V_{OUT} = V_{IN} \left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}} \right] + I_{LKG} \left[\frac{R_{LOAD} (R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}} \right]$$

IF $R_G \rightarrow 0$,

$$V_{OUT} = V_{IN} \left[\frac{R_{LOAD}}{R_{ON} + R_{LOAD}} \right] + I_{LKG} \left[\frac{R_{LOAD} R_{ON}}{R_{ON} + R_{LOAD}} \right]$$

Figure 6: Factors Affecting DC Performance for ON Switch Condition: R_{ON} , R_{LOAD} , and I_{LKG}

When the switch is OFF, leakage current can introduce errors as shown in Figure 7. The leakage current flowing through the load resistance develops a corresponding voltage error at the output.

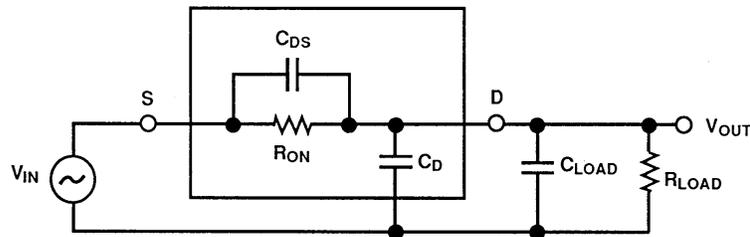


Leakage current creates error voltage at V_{OUT} equal to:

$$V_{OUT} = I_{LKG} \times R_{LOAD}$$

Figure 7: Factors Affecting DC Performance for OFF Switch Condition: I_{LKG} and R_{LOAD}

Figure 8 illustrates the parasitic components that affect the ac performance of CMOS switches. Additional external capacitances will further degrade performance. These capacitances affect feedthrough, crosstalk and system bandwidth. C_{DS} (drain-to-source capacitance), C_D (drain-to-ground capacitance), and C_{LOAD} all work in conjunction with R_{ON} and R_{LOAD} to form the overall transfer function.



$$A(s) = \left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}} \right] \left[\frac{sR_{ON}C_{DS} + 1}{s \left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}} \right) (C_{LOAD} + C_D + C_{DS}) + 1} \right]$$

$$A(\text{dB}) = 20 \log \left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}} \right] + 10 \log \left[\omega^2 (R_{ON}C_{DS})^2 + 1 \right] - 10 \log \omega^2 \left[\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}} \right)^2 (C_{LOAD} + C_D + C_{DS})^2 + 1 \right]$$

**Figure 8: Dynamic Performance Considerations:
Transfer Accuracy Versus Frequency**

In the equivalent circuit, C_{DS} creates a frequency zero in the numerator of the transfer function $A(s)$. This zero usually occurs at high frequencies because the switch on-resistance is small. The bandwidth is also a function of the switch output capacitance in combination with C_{DS} and the load capacitance. This frequency pole appears in the denominator of the equation.

The composite frequency domain transfer function may be re-written as shown in Figure 9 which shows the overall Bode plot for the switch in the on state. In most cases, the pole breakpoint frequency occurs first because of the dominant effect of the output capacitance C_D . Thus, to maximize bandwidth, a switch should have low input and output capacitance and low on-resistance.

The series-pass capacitance, C_{DS} , not only creates a zero in the response in the ON-state, it degrades the feedthrough performance of the switch during its OFF state. When the switch is off, C_{DS} couples the input signal to the output load as shown in Figure 10.

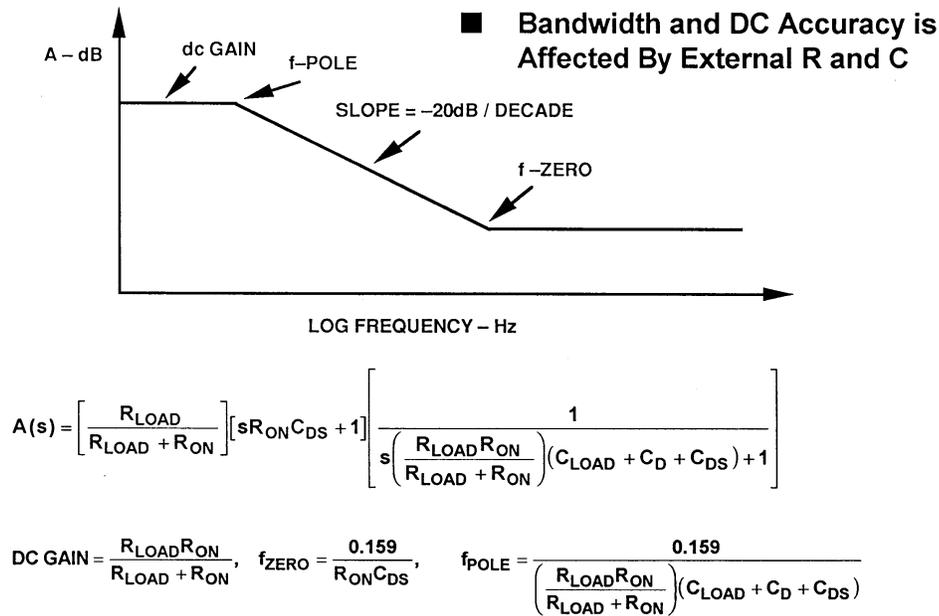


Figure 9: Bode Plot of CMOS Switch Transfer Function in the ON State

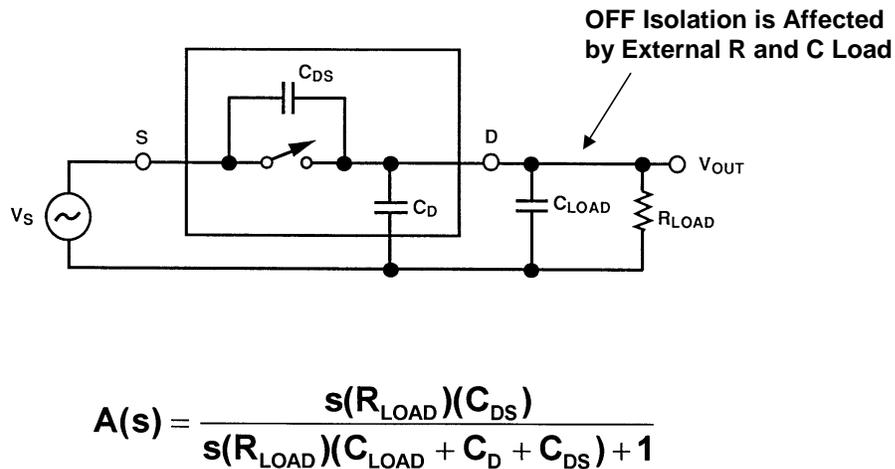


Figure 10: Dynamic Performance Considerations: Off Isolation

Large values of C_{DS} will produce large values of feedthrough, proportional to the input frequency. Figure 11 illustrates the drop in OFF-isolation as a function of frequency. The simplest way to maximize the OFF-isolation is to choose a switch that has as small a C_{DS} as possible.

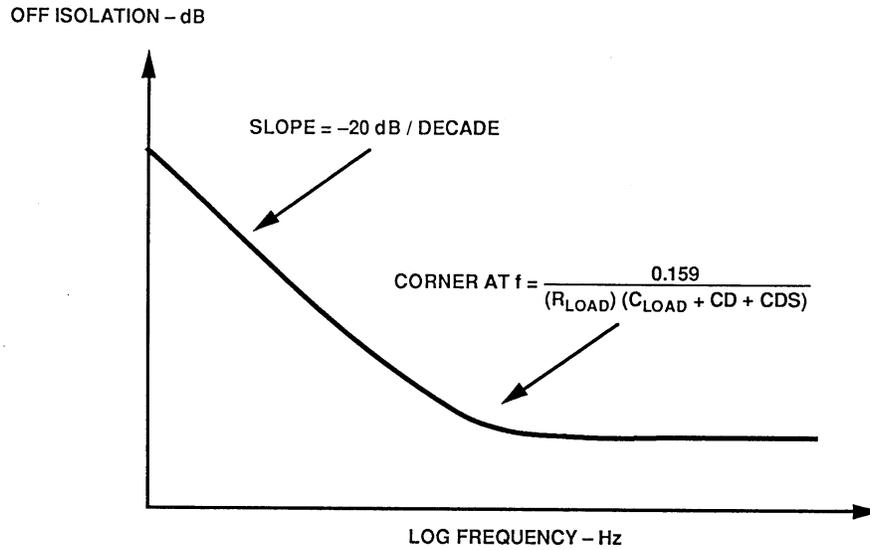


Figure 11: Off Isolation Versus Frequency

Figure 12 shows typical CMOS analog switch OFF-isolation as a function of frequency for the [ADG708](#) 8-channel multiplexer. From dc to several kilohertz, the multiplexer has nearly 90-dB isolation. As the frequency increases, an increasing amount of signal reaches the output. However, even at 10 MHz, the switch shown still has nearly 60 dB of isolation.

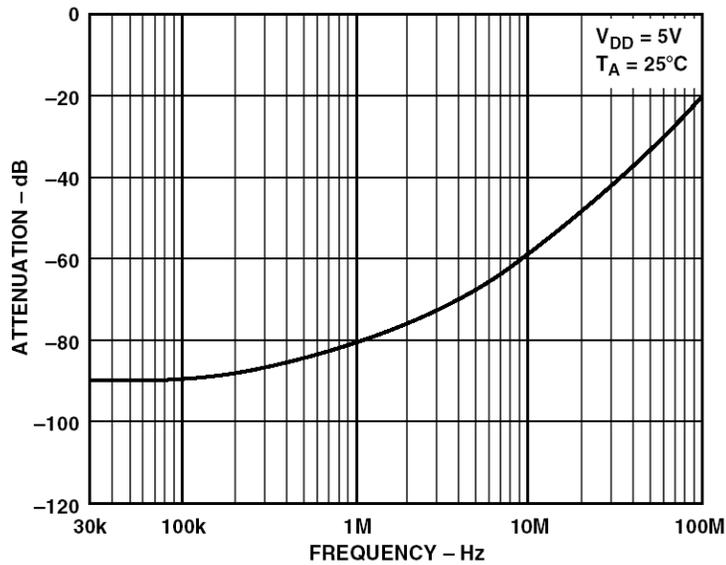


Figure 12: OFF-Isolation Versus Frequency for ADG708 8-Channel Multiplexer

Another ac parameter that affects system performance is the charge injection that takes place during switching. Figure 13 shows the equivalent circuit of the charge injection mechanism.

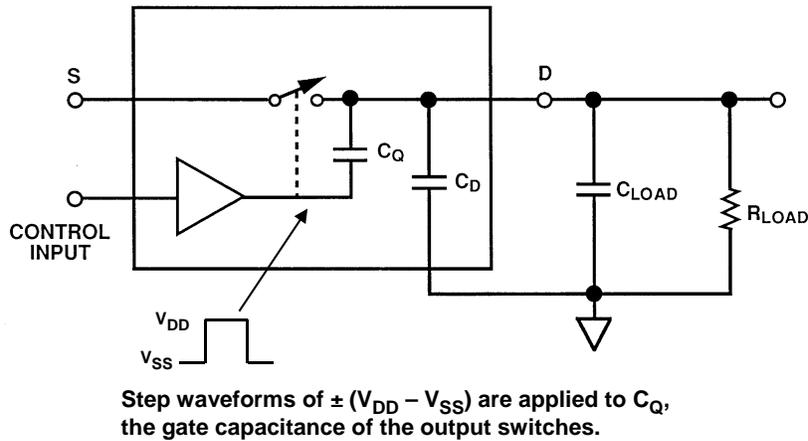


Figure 13: Dynamic Performance Considerations: Charge Injection Model

When the switch control input is asserted, it causes the control circuit to apply a large voltage change (from V_{DD} to V_{SS} , or vice versa) at the gate of the CMOS switch. This fast change in voltage injects a charge into the switch output through the gate-drain capacitance C_Q . The amount of charge coupled depends on the magnitude of the gate-drain capacitance.

The charge injection introduces a step change in output voltage when switching as shown in Figure 14. The change in output voltage, ΔV_{OUT} , is a function of the amount of charge injected, Q_{INJ} (which is in turn a function of the gate-drain capacitance, C_Q) and the load capacitance, C_L .

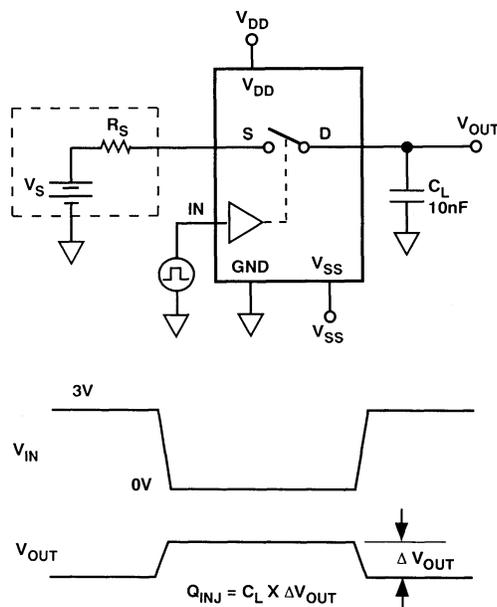


Figure 14: Effects of Charge Injection on Output

Another problem caused by switch capacitance is the retained charge when switching channels. This charge can cause transients in the switch output, and Figure 15 illustrates the phenomenon. Assume that initially S2 is closed and S1 open. C_{S1} and C_{S2} are charged to -5 V . As S2 opens, the -5 V remains on C_{S1} and C_{S2} , as S1 closes. Thus, the output of Amplifier A sees a -5 V transient. The output will not stabilize until Amplifier A's output fully discharges C_{S1} and C_{S2} and settles to 0 V . The scope photo in Figure 16 depicts this transient. The amplifier's transient load settling characteristics will therefore be an important consideration when choosing the right input buffer.

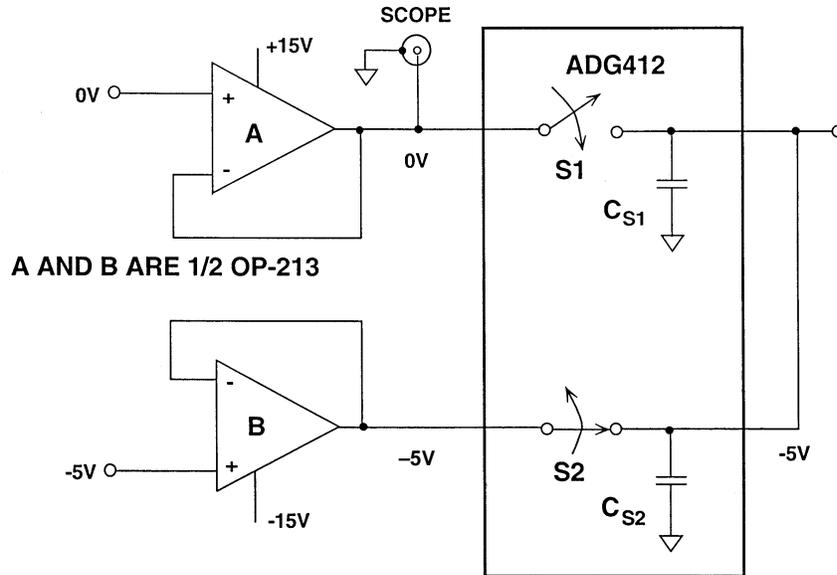
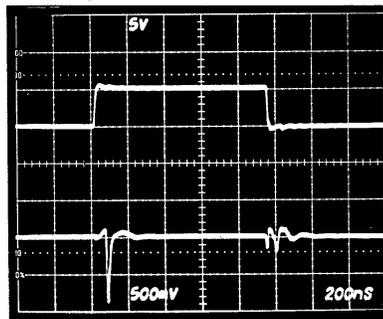


Figure 15: Charge Coupling Causes Dynamic Settling Time Transient When Multiplexing Signals

SWITCH CONTROL
5V/div.

AMPLIFIER A OUTPUT
500mV/div.



HORIZONTAL SCALE: 200ns/div.

Figure 16: Output of Amplifier Shows Dynamic Settling Time Transient Due to Charge Coupling

Crosstalk is related to the capacitances between two switches. This is modeled as the C_{SS} capacitance shown in Figure 17.

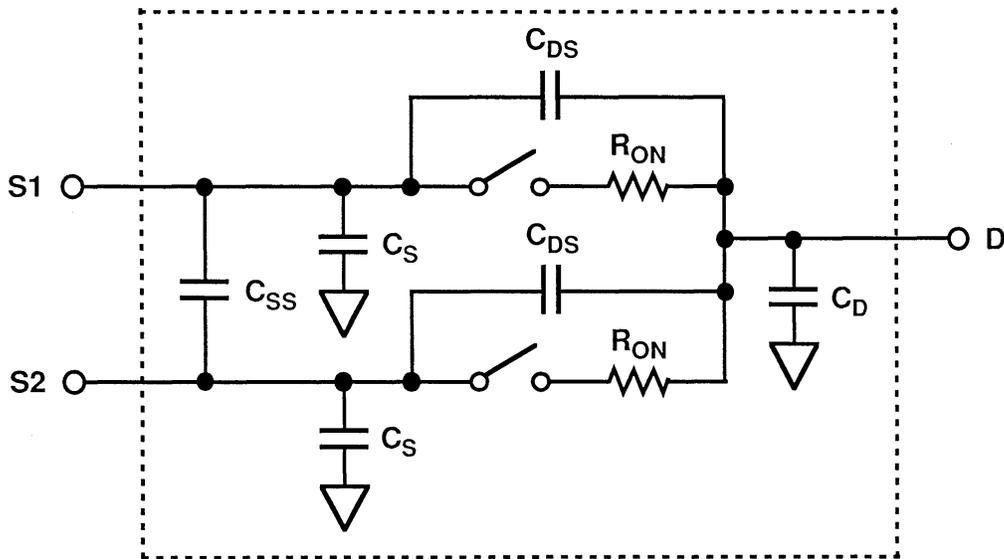


Figure 17: Channel-to-Channel Crosstalk Equivalent Circuit for Adjacent Switches

Figure 18 shows typical crosstalk performance of the [ADG708](#) 8-channel CMOS multiplexer.

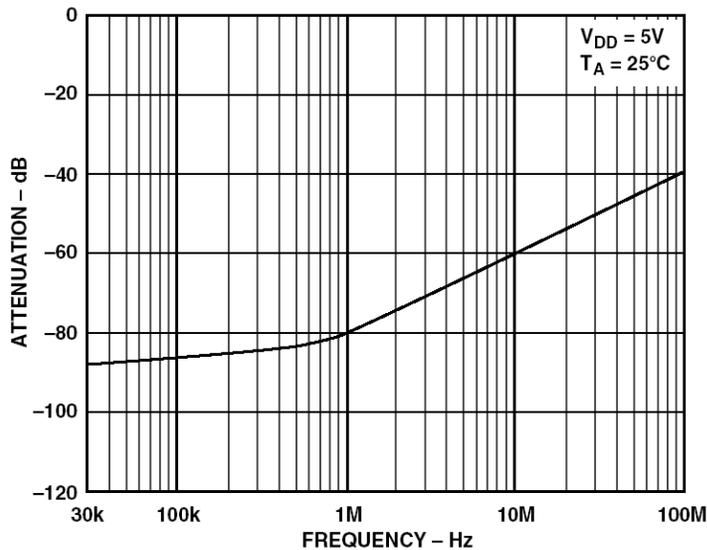
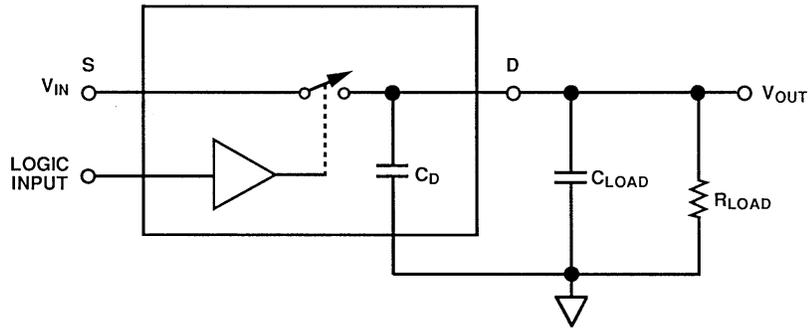


Figure 18: Crosstalk Versus Frequency for ADG708 8-Channel Multiplexer

Finally, the switch itself has a settling time that must be considered. Figure 19 shows the dynamic transfer function. The settling time can be calculated, because the response is a function of the switch and circuit resistances and capacitances. One can assume that this is a single-pole

system and calculate the number of time constants required to settle to the desired system accuracy as shown in Figure 20.



$$\text{OFF - TO - ON: } t_{\text{SETT}} = t_{\text{ON}} + \left(\frac{R_{\text{ON}} R_{\text{LOAD}}}{R_{\text{ON}} + R_{\text{LOAD}}} \right) (C_{\text{LOAD}} + C_{\text{D}}) \left(-\ln \frac{\% \text{ERROR}}{100} \right)$$

$$\text{ON - TO - OFF: } t_{\text{SETT}} = t_{\text{OFF}} + (R_{\text{LOAD}}) (C_{\text{LOAD}} + C_{\text{D}}) \left(-\ln \frac{\% \text{ERROR}}{100} \right)$$

Settling time is the time required for the switch output to settle within a given error band of the final value.

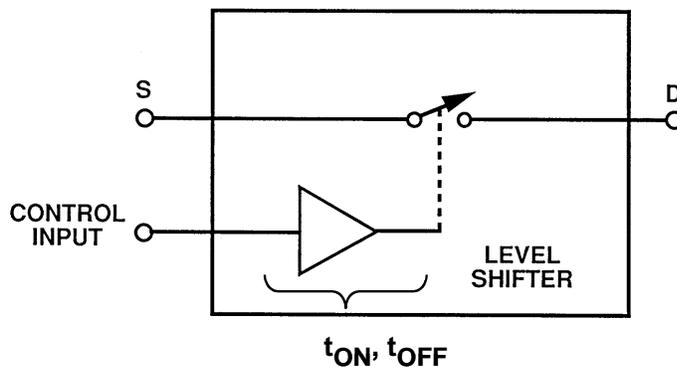
Figure 19: Multiplexer Settling Time

RESOLUTION, # OF BITS	LSB (%FS)	# OF TIME CONSTANTS
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

Figure 20: Number of Time Constants Required to Settle to 1 LSB Accuracy for a Single-Pole System

APPLYING THE ANALOG SWITCH

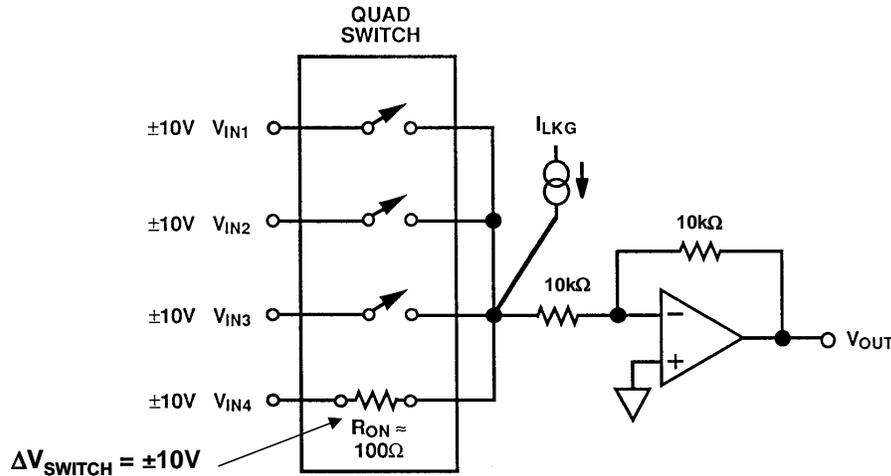
Switching time is an important consideration in applying analog switches, but switching time should not be confused with settling time. ON and OFF times are simply a measure of the propagation delay from the control input to the toggling of the switch, and are largely caused by time delays in the drive and level-shift circuits (see Figure 21). The t_{ON} and t_{OFF} values are generally measured from the 50% point of the control input leading edge to the 90% point of the output signal level.



- ◆ t_{ON} and t_{OFF} should not be confused with settling time.
- ◆ t_{ON} and t_{OFF} are simply a measure of the propagation delay from control input to operation of the analog switch. It is caused by time delays in the drive / level-shifter logic circuitry.
- ◆ t_{ON} and t_{OFF} are measured from the 50% point of the control input to the 90% point of the output signal level.

Figure 21: Applying the Analog Switch: Dynamic Performance Considerations

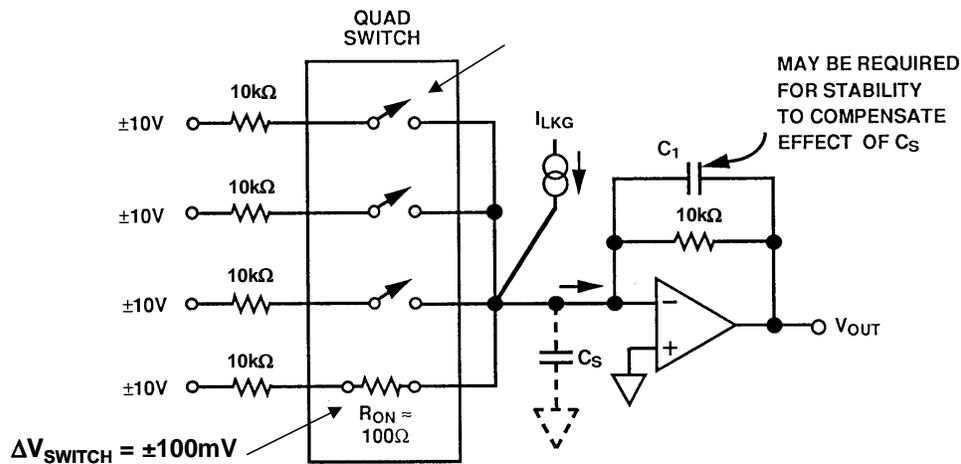
We will next consider the issues involved in buffering a CMOS switch or multiplexer output using an op amp. When a CMOS multiplexer switches inputs to an inverting summing amplifier, it should be noted that the on-resistance, and its nonlinear change as a function of input voltage, will cause gain and distortion errors as shown in Figure 22. If the resistors are large, the switch leakage current may introduce error. Small resistors minimize leakage current error but increase the error due to the finite value of R_{ON} .



- ◆ ΔR_{ON} caused by ΔV_{IN} , degrades linearity of V_{OUT} relative to V_{IN} .
- ◆ ΔR_{ON} causes overall gain error in V_{OUT} relative to V_{IN} .

Figure 22: Applying the Analog Switch: Unity Gain Inverter with Switched Input

To minimize the effect of R_{ON} change due to the change in input voltage, it is advisable to put the multiplexing switches at the op amp summing junction as shown in Figure 23. This ensures the switches are only modulated with about ± 100 mV rather than the full ± 10 V—but a separate resistor is required for each input leg.



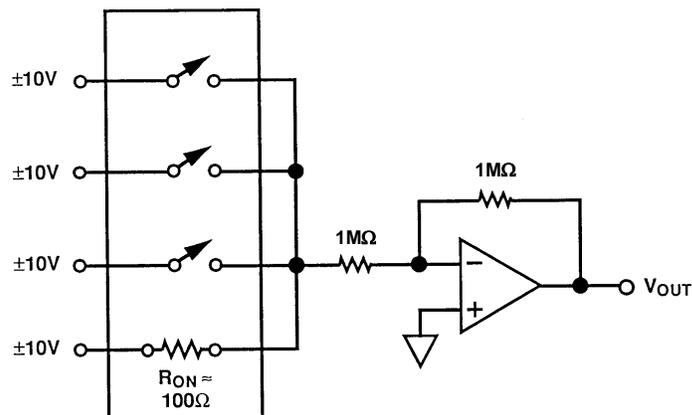
- ◆ Switch drives a virtual ground.
- ◆ Switch sees only ± 100 mV, not ± 10 V, minimizes ΔR_{ON} .

Figure 23: Applying the Analog Switch: Minimizing the Influence of ΔR_{ON}

It is important to know how much parasitic capacitance has been added to the summing junction as a result of adding a multiplexer, because any capacitance added to that node introduces phase shift to the amplifier closed loop response. If the capacitance is too large, the amplifier may become unstable and oscillate. A small capacitance, C_1 , across the feedback resistor may be required to stabilize the circuit.

The finite value of R_{ON} can be a significant error source in the circuit shown in Figure 24. The gain-setting resistors should be at least 1,000 times larger than the switch on-resistance to guarantee 0.1% gain accuracy. Higher values yield greater accuracy but lower bandwidth and greater sensitivity to leakage and bias current.

A better method of compensating for R_{ON} is to place one of the switches in series with the feedback resistor of the inverting amplifier as shown in Figure 25. It is a safe assumption that the multiple switches, fabricated on a single chip, are well-matched in absolute characteristics and tracking over temperature. Therefore, the amplifier is closed-loop gain stable at unity gain, since the total feedforward and feedback resistors are matched.



- ◆ ΔR_{ON} is small compared to $1M\Omega$ switch load.
- ◆ Effect on transfer accuracy is minimized.
- ◆ Bias current and leakage current effects are now very important.
- ◆ Circuit bandwidth degrades.

Figure 24: Applying the Analog Switch: Minimizing Effects of ΔR_{ON} Using Large Resistor Values

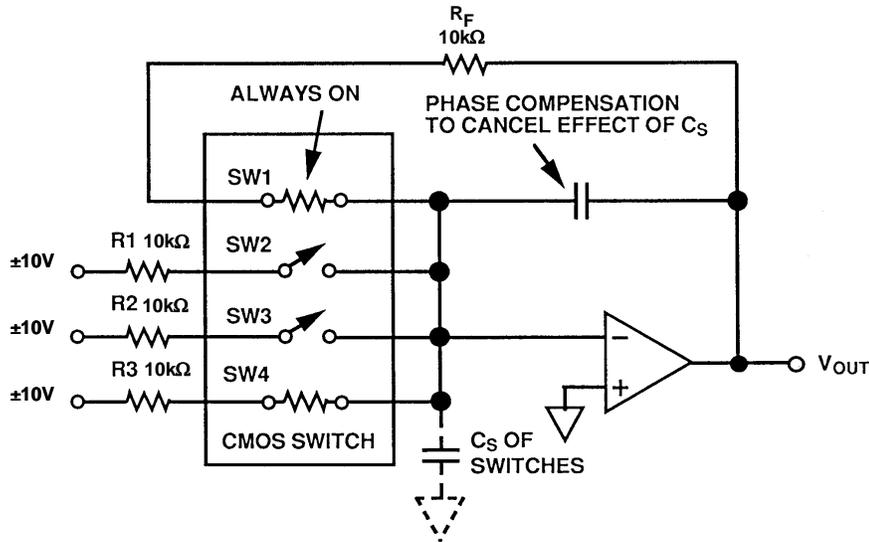


Figure 25: Applying the Analog Switch: Using "Dummy" Switch in Feedback to Minimize Gain Error Due to ΔR_{ON}

The best multiplexer design drives the non-inverting input of the amplifier as shown in Figure 26. The high input impedance of the non-inverting input eliminates the errors due to R_{ON} .

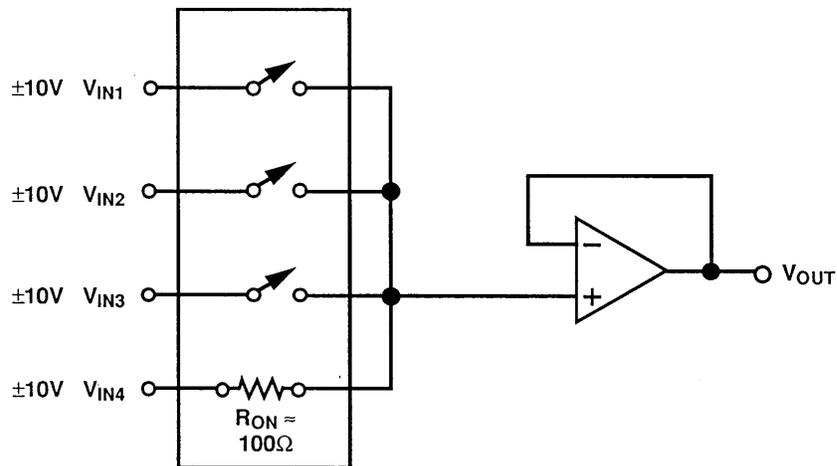
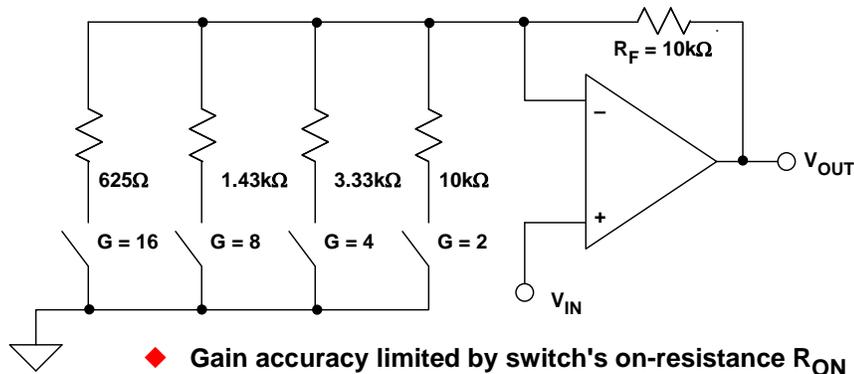


Figure 26: Applying the Analog Switch: Minimizing the Influence of ΔR_{ON} Using Non-Inverting Configuration

CMOS switches and multiplexers are often used with op amps to make programmable gain amplifiers (PGAs). To understand R_{ON} 's effect on their performance, consider Figure 27, a poor PGA design. A non-inverting op amp has 4 different gain-set resistors, each grounded by a switch, with an R_{ON} of 100-500 Ω . Even with R_{ON} as low as 25 Ω , the gain of 16 error would be 2.4%, worse than 8-bit accuracy! R_{ON} also changes over temperature, and from switch-to-switch.

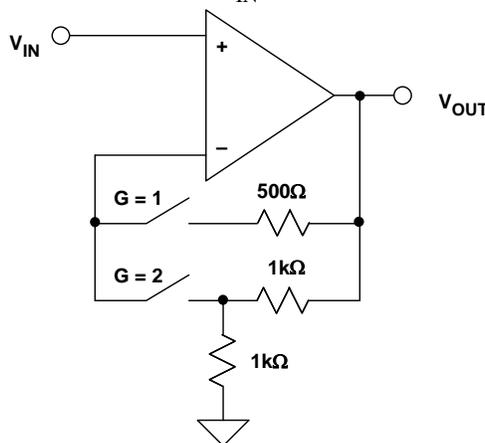


- ◆ Gain accuracy limited by switch's on-resistance R_{ON} and R_{ON} modulation
- ◆ R_{ON} typically 1 - 500Ω for CMOS or JFET switch
- ◆ For $R_{ON} = 25\Omega$, there is a 2.4% gain error for $G = 16$
- ◆ R_{ON} drift over temperature limits accuracy
- ◆ Must use very low R_{ON} switches

Figure 27: A Poorly Designed PGA Using CMOS Switches

To attempt "fixing" this design, the resistors might be increased, but noise and offset could then be a problem. The only way to improve accuracy with this circuit is to use relays, with virtually no R_{ON} . Only then will the few mΩ of relay R_{ON} be a small error vis-à-vis 625 Ω.

It is much better to use a circuit insensitive to R_{ON} ! In Figure 28, the switch is placed in series with the inverting input of an op amp. Since the op amp input impedance is very large, the switch R_{ON} is now irrelevant, and gain is now determined solely by the external resistors. Note— R_{ON} may add a small offset error if op amp bias current is high. If this is the case, it can readily be compensated with an equivalent resistance at V_{IN} .



- ◆ R_{ON} is not in series with gain setting resistors
- ◆ R_{ON} is small compared to input impedance
- ◆ Only slight offset errors occur due to bias current flowing through the switches

Figure 28: Alternate PGA Configuration Minimizes the Effects of R_{ON}

1-GHz CMOS SWITCHES

The [ADG918/ADG919](#) are the first switches using a CMOS process to provide high isolation and low insertion loss up to and exceeding 1 GHz. The switches exhibit low insertion loss (0.8 dB) and relatively high off isolation (37 dB) when transmitting a 1-GHz signal. In high frequency applications with throughput power of +18 dBm or less at 25°C, they are a cost-effective alternative to gallium arsenide (GaAs) switches. A block diagram of the devices are shown in Figure 29 along with isolation and loss versus frequency plots given in Figure 30.

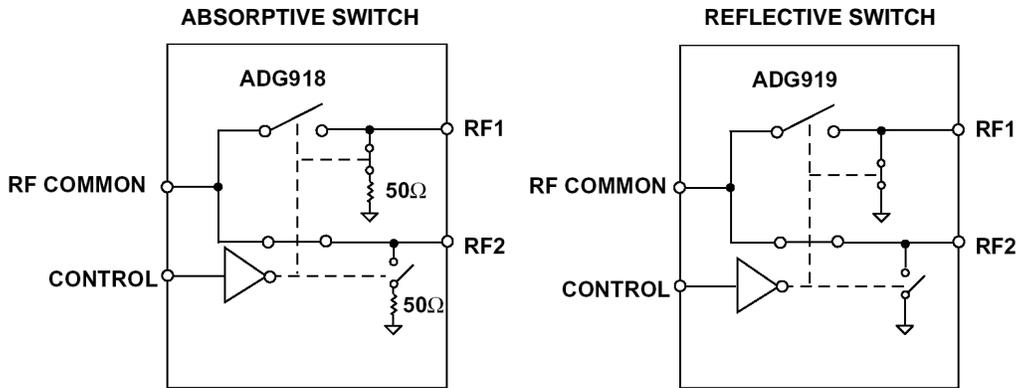


Figure 29: 1-GHz CMOS 1.65-V to 2.75-V 2:1 Mux/SPDT Switches

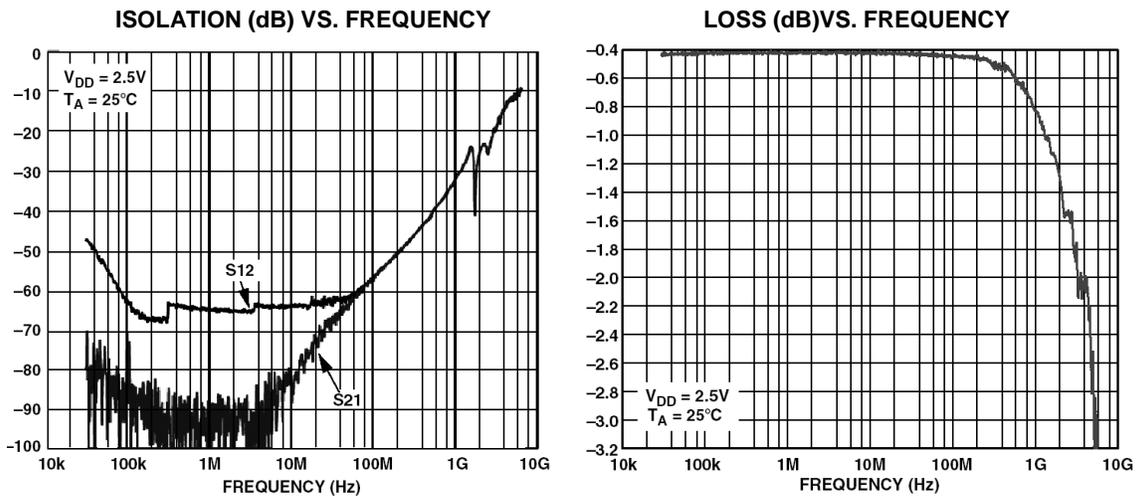


Figure 30: Isolation and Frequency Response of AD918/AD919 1-GHz Switch

The ADG918 is an absorptive switch with 50- Ω terminated shunt legs that allow impedance matching with the application circuit, while the ADG919 is a reflective switch designed for use where the terminations are external to the chip. Both offer low power consumption ($<1 \mu\text{A}$), tiny packages (8-lead MSOP and 3 mm \times 3 mm lead frame chip scale package), single-pin control voltage levels that are CMOS/LVTTL compatible, making the switches ideal for wireless applications and general-purpose RF switching.

PARASITIC LATCHUP IN CMOS SWITCHES AND MUXES

Because multiplexers are often at the front-end of a data acquisition system, their inputs generally come from remote locations—hence, they are often subjected to overvoltage conditions. An understanding of the problem as it relates to CMOS devices is particularly important. Although this discussion centers around multiplexers, it is germane to nearly all types of CMOS parts.

Most CMOS analog switches are built using junction-isolated CMOS processes. A cross-sectional view of a single switch cell is shown in Figure 31. Parasitic SCR (silicon controlled rectifier) latchup can occur if the analog switch terminal has voltages more positive than V_{DD} or more negative than V_{SS} . Even a transient situation, such as power-on with an input voltage present, can trigger a parasitic latchup. If the conduction current is too great (several hundred milliamperes or more), it can damage the switch.

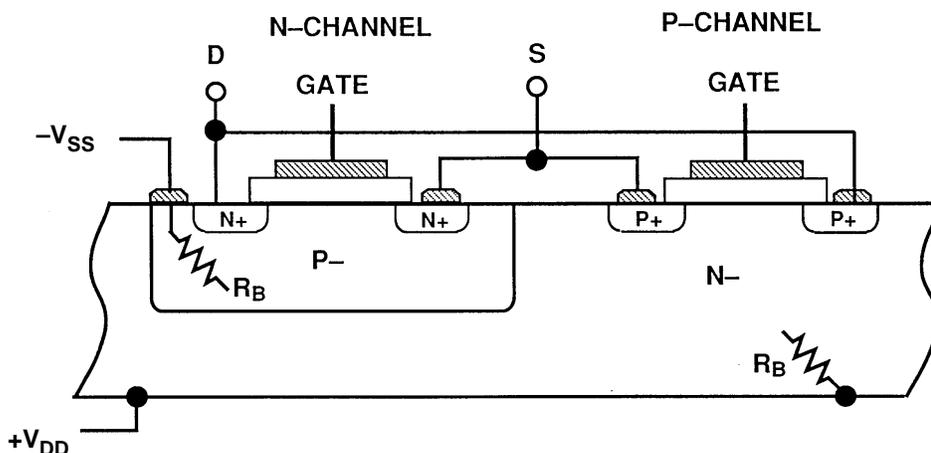


Figure 31: Cross-Section of a Junction-Isolation CMOS Switch

The parasitic SCR mechanism is shown in Figure 32. SCR action takes place when either terminal of the switch (source or the drain) is either one diode drop more positive than V_{DD} or one diode drop more negative than V_{SS} . In the former case, the V_{DD} terminal becomes the SCR gate input and provides the current to trigger SCR action. In the case where the voltage is more negative than V_{SS} , the V_{SS} terminal becomes the SCR gate input and provides the gate current. In either case, high current will flow between the supplies. The amount of current depends on the collector resistances of the two transistors, which can be fairly small.

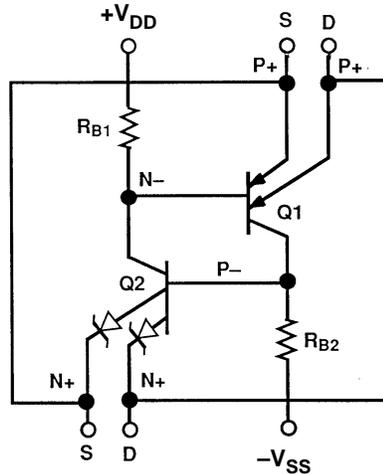
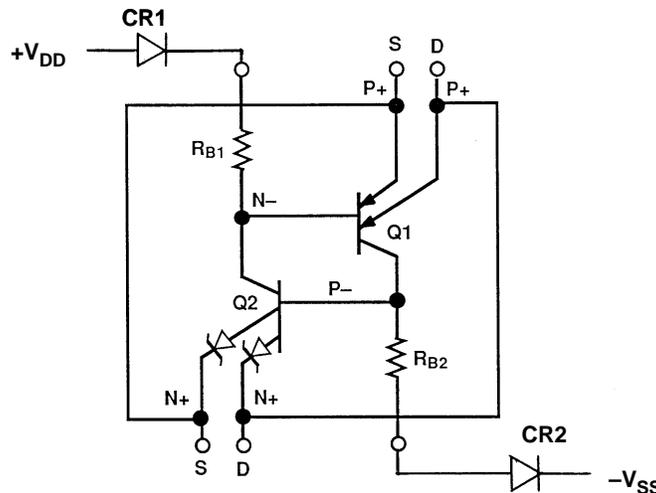


Figure 32: Bipolar Transistor Equivalent Circuit for CMOS Switch Shows Parasitic SCR Latch

In general, to prevent the latchup condition, the inputs to CMOS devices should never be allowed to be more than 0.3 V above the positive supply or 0.3 V below the negative supply. Note that this restriction also applies when the power supplies are off ($V_{DD} = V_{SS} = 0$ V), and therefore devices can latchup if power is applied to a part when signals are present on the inputs. Manufacturers of CMOS devices invariably place this restriction in the data sheet table of absolute maximum ratings. In addition, the input current under overvoltage conditions should be restricted to 5-30 mA, depending upon the particular device.

In order to prevent this type of SCR latchup, a series diode can be inserted into the V_{DD} and V_{SS} terminals as shown in Figure 33. The diodes block the SCR gate current. Normally the parasitic transistors Q1 and Q2 have low beta (usually less than 10) and require a comparatively large gate current to fire the SCR. The diodes limit the reverse gate current so that the SCR is not triggered.



Diodes CR1 and CR2 block base current drive to Q1 and Q2 in the event of overvoltage at S or D.

Figure 33: Diode Protection Scheme for CMOS Switch

If diode protection is used, the analog voltage range of the switch will be reduced by one V_{BE} drop at each rail, and this can be inconvenient when using low supply voltages.

As noted, CMOS switches and multiplexers can also be protected from possible overcurrent by inserting a series resistor to limit the current to a safe level as shown in Figure 34, generally less than 5-30 mA. Because of the resistive attenuator formed by R_{LOAD} and R_{LIMIT} , this method works only if the switch drives a relatively high impedance load.

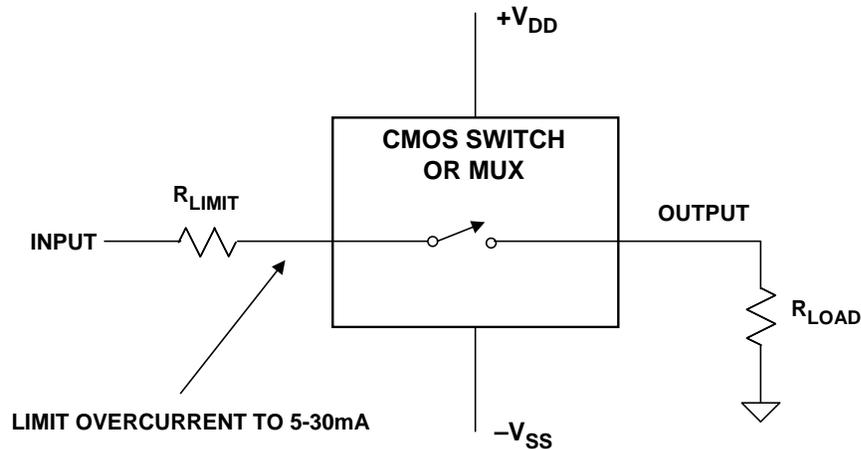


Figure 34: Overcurrent Protection Using External Resistor

A common method for input protection is shown in Figure 35 where Schottky diodes are connected from the input terminal to each supply voltage as shown. The diodes effectively prevent the inputs from exceeding the supply voltage by more than 0.3-0.4 V, thereby preventing latchup conditions. In addition, if the input voltage exceeds the supply voltage, the input current flows through the external diodes to the supplies, not the device. Schottky diodes can easily handle 50-100 mA of transient current, therefore the R_{LIMIT} resistor can be quite low.

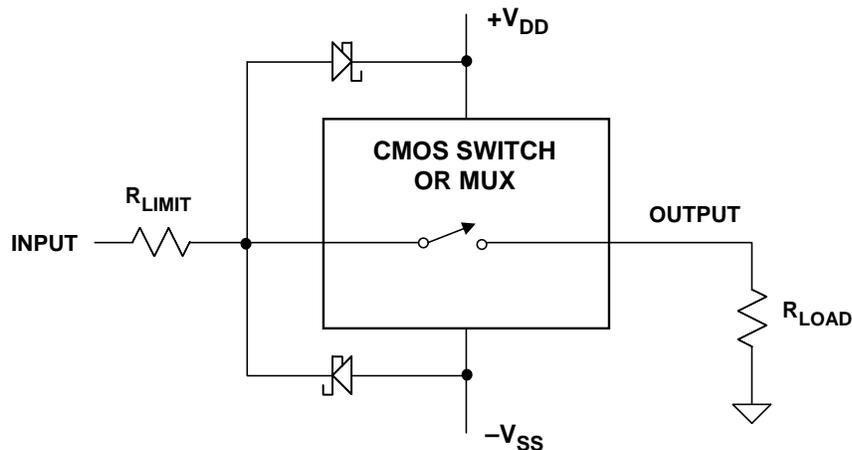


Figure 35: Input Protection Using External Schottky Diodes

Most CMOS devices have internal ESD-protection diodes connected from the inputs to the supply rails, making the devices less susceptible to latchup. However, the internal diodes begin conduction at 0.6 V, and have limited current-handling capability, thus adding the external Schottky diodes offers an added degree of protection. However, the effects of the diode leakage and capacitance must be considered.

Note that latchup protection does not provide overcurrent protection, and vice versa. If both fault conditions can exist in a system, then both protective diodes and resistors should be used.

Analog Devices uses trench-isolation technology to produce its LC²MOS analog switches. The process reduces the latchup susceptibility of the device, the junction capacitances, increases switching time and leakage current, and extends the analog voltage range to the supply rails.

Figure 36 shows the cross-sectional view of the trench-isolated CMOS structure. The buried oxide layer and the side walls completely isolate the substrate from each transistor junction. Therefore, no reverse-biased PN junction is formed. Consequently the bandwidth-reducing capacitances and the possibility of SCR latchup are greatly reduced.

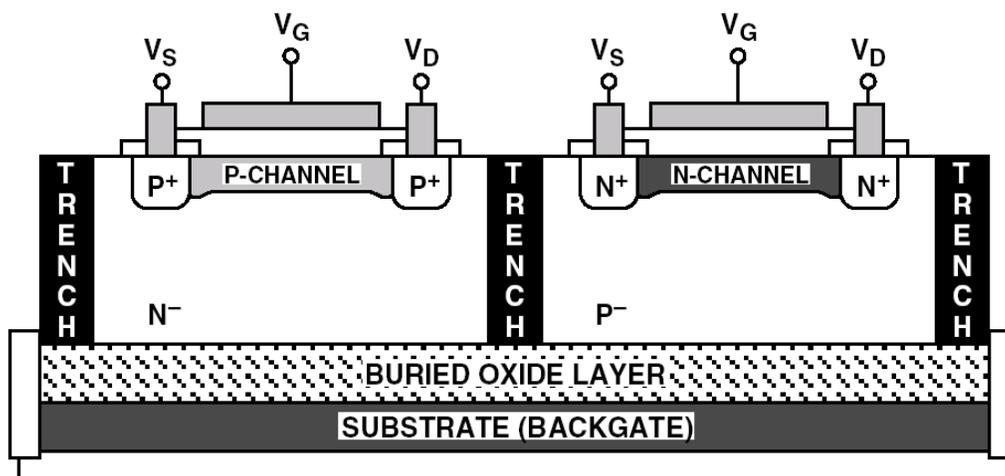


Figure 36: Trench-Isolation LC²MOS Structure

The [ADG508F](#), [ADG509F](#), [ADG528F](#), [ADG438F](#), and [ADG439F](#) are $\pm 15\text{V}$ trench-isolated LC²MOS multiplexers which offer "fault protection" for input and output overvoltages between -40 V and $+55\text{ V}$. These devices use a series structure of three MOSFETS in the signal path: an N-channel, followed by a P-channel, followed by an N-channel. In addition, the signal path becomes a high impedance when the power supplies are turned off. This structure offers a high degree of latchup and overvoltage protection—at the expense of higher R_{ON} ($\sim 300\ \Omega$), and more R_{ON} variation with signal level. For more details of this protection method, refer to the individual product data sheets.

REFERENCES:

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as [*Linear Circuit Design Handbook*](#), Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 7.
2. Walt Kester, [*Analog-Digital Conversion*](#), Analog Devices, 2004, ISBN 0-916550-27-3, Chapter 7. Also available as [*The Data Conversion Handbook*](#), Elsevier/Newnes, 2005, ISBN 0-7506-7841-0, Chapter 7.

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