

Basic DAC Architectures II: Binary DACs

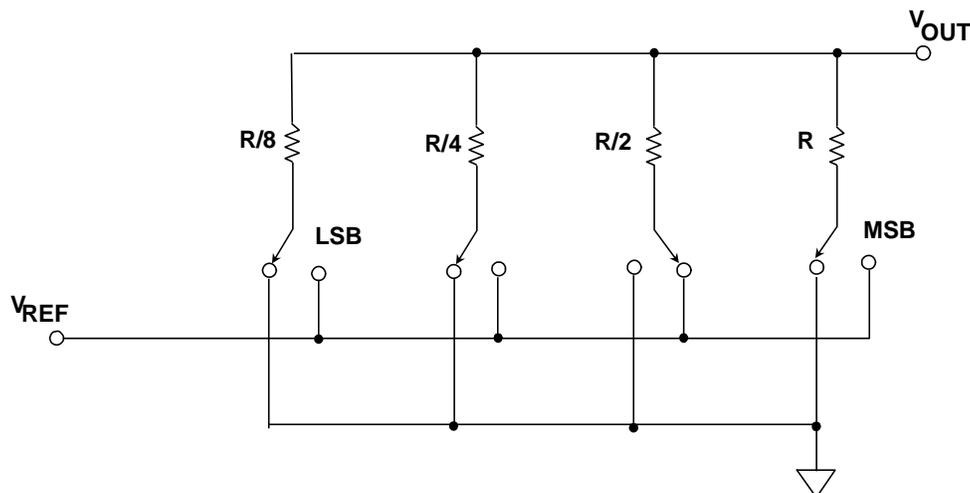
by Walt Kester

INTRODUCTION

While the string DAC and thermometer DAC architectures are by far the simplest, they are certainly not the most efficient when high resolutions are required. Binary-weighted DACs utilize one switch per bit and were first developed in the 1920s (see References 1, 2, and 3). Since then, the architecture has remained popular and forms the backbone for modern precision as well as high-speed DACs.

BINARY-WEIGHTED DACS

The voltage-mode binary-weighted resistor DAC shown in Figure 1 is usually the simplest textbook example of a DAC. However, this DAC is not inherently monotonic and is actually quite hard to manufacture successfully at high resolutions. In addition, the output impedance of the voltage-mode binary DAC changes with the input code.



Adapted from: B. D. Smith, "Coding by Feedback Methods," Proceedings of the I. R. E., Vol. 41, August 1953, pp. 1053-1058

Figure 1: Voltage-mode Binary-Weighted Resistor DAC

Current-mode binary DACs are shown in Figure 2A (resistor-based), and Figure 2B (current-source based). An N-bit DAC of this type consists of N weighted current sources (which may simply be resistors and a voltage reference) in the ratio 1:2:4:8:.....:2^{N-1}. The LSB switches the 2^{N-1} current, the MSB the 1 current, etc. The theory is simple but the practical problems of manufacturing an IC of an economical size with current or resistor ratios of even 128:1 for an 8-bit DAC are significant, especially as they must have matched temperature coefficients.

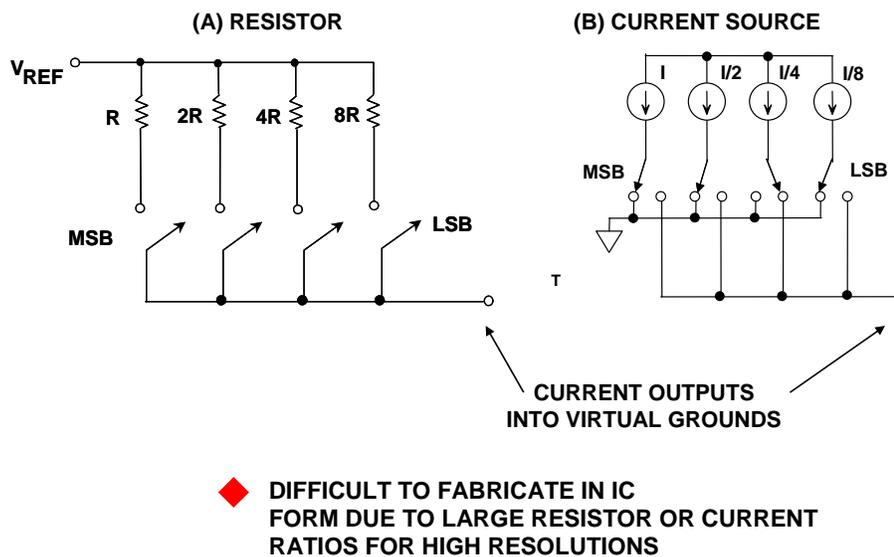


Figure 2: Current-Mode Binary-Weighted DACs

If the MSB current is slightly low in value, it will be less than the sum of all the other bit currents, and the DAC will not be monotonic (the differential non-linearity of most types of DACs is worst at major bit transitions). This architecture is virtually never used on its own in integrated circuit DACs, although, again, 3- or 4-bit versions have been used as components in more complex structures.

However, there is another binary-weighted DAC structure that has recently become widely used. This uses binary-weighted capacitors as shown in Figure 3. The problem with a DAC using capacitors is that leakage causes it to lose its accuracy within a few milliseconds of being set. This may make capacitive DACs unsuitable for general purpose DAC applications, but it is not a problem in successive approximation ADCs, since the conversion is complete in a few μs or less—long before leakage has any appreciable effect.

The successive approximation ADC has a very simple structure, low power, and reasonably fast conversion times. It is probably the most widely used general-purpose ADC architecture, but in the mid-1990s the subranging ADC was starting to overtake the successive approximation type in popularity because the R-2R thin-film resistor DAC in the successive approximation ADC made the chip larger and more expensive than that of a subranging ADC, even though the subranging types tend to use more power. The development of sub-micron CMOS processes made possible very small (and therefore cheap), and very accurate switched capacitor DACs. These enabled a new generation of successive approximation ADCs to be made small, cheap, low-power and precise, and thus to regain their popularity (such as the Analog Devices' PulSAR® family, for example).

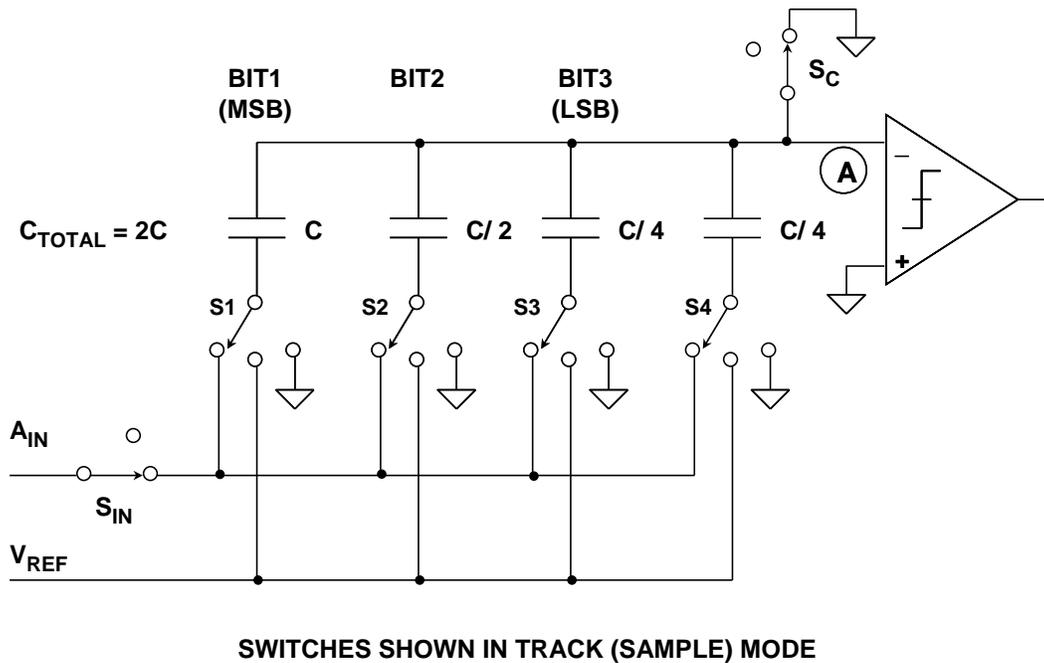


Figure 3: Capacitive Binary-Weighted DAC in Successive Approximation ADC

The use of capacitive charge redistribution DACs offers another advantage as well—the DAC itself behaves as a sample-and-hold circuit (SHA), so neither an external SHA nor allocation of chip area for a separate integral SHA are required.

R-2R DACs

One of the most common DAC building-block structures is the R-2R resistor ladder network shown in Figure 4. It uses resistors of only two different values, and their ratio is 2:1. An N-bit DAC requires 2N resistors, and they are quite easily trimmed. There are also relatively few resistors to trim.

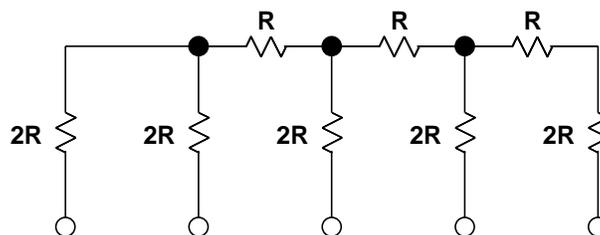
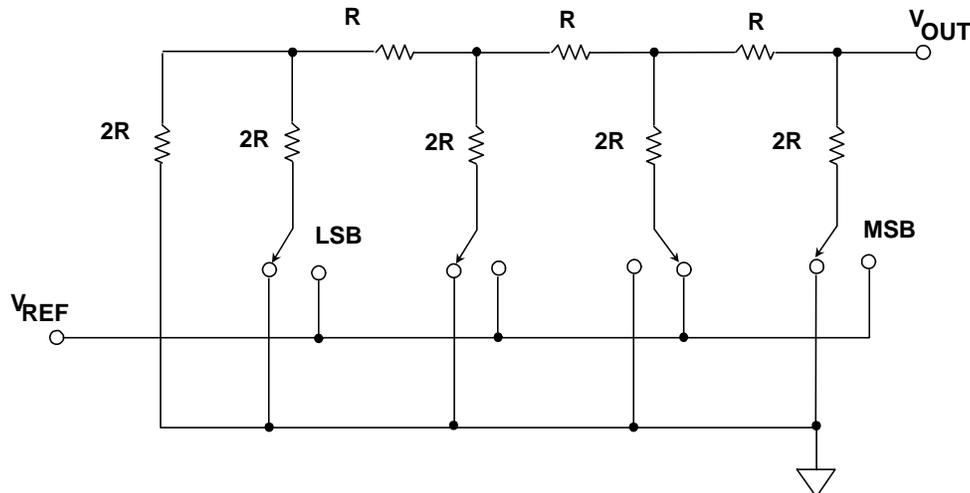


Figure 4: 4-Bit R-2R Ladder Network

There are two ways in which the R-2R ladder network may be used as a DAC—known respectively as the *voltage mode* and the *current mode*. They are sometimes called "normal"

mode and "inverted" mode, respectively, but as there is no consensus on whether the voltage mode or the current mode is the "normal" mode for a ladder network, so this nomenclature can be misleading. Each mode has its advantages and disadvantages.

In the voltage mode R-2R ladder DAC shown in Figure 5, the "rungs" or arms of the ladder are switched between V_{REF} and ground, and the output is taken from the end of the ladder. The output may be taken as a voltage, but the output impedance is independent of code, so it may equally well be taken as a current into a virtual ground. As mentioned earlier, this architecture was proposed by B. D. Smith in 1953 (Reference 3).

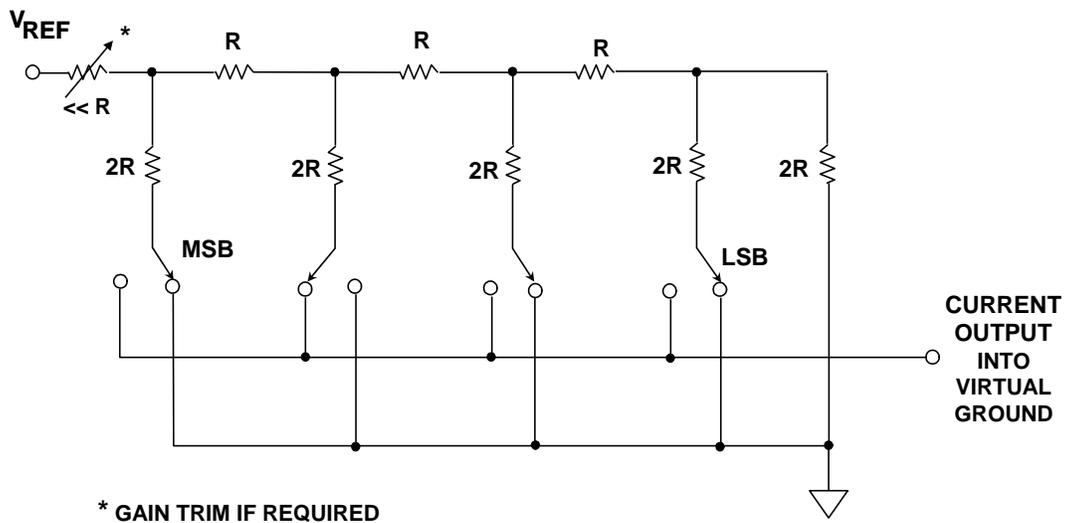


Adapted from: B. D. Smith, "Coding by Feedback Methods," Proceedings of the I. R. E., Vol. 41, August 1953, pp. 1053-1058

Figure 5: Voltage-Mode R-2R Ladder Network DAC

The voltage output is an advantage of this mode, as is the constant output impedance, which eases the stabilization of any amplifier connected to the output node. Additionally, the switches switch the arms of the ladder between a low impedance V_{REF} connection and ground, which is also, of course, low impedance, so capacitive glitch currents tend not to flow in the load. On the other hand, the switches must operate over a wide voltage range (V_{REF} to ground). This is difficult from a design and manufacturing viewpoint, and the reference input impedance varies widely with code, so that the reference input must be driven from a very low impedance. In addition, the gain of the DAC cannot be adjusted by means of a resistor in series with the V_{REF} terminal.

In the current-mode R-2R ladder DAC shown in Figure 6, the gain of the DAC may be adjusted with a series resistor at the V_{REF} terminal, since in the current mode, the end of the ladder, with its code-independent impedance, is used as the V_{REF} terminal; and the ends of the arms are switched between ground (or, sometimes, an "inverted output" at ground potential) and an output line which must be held at ground potential. The normal connection of a current-mode ladder network output is to an op amp configured as current-to-voltage (I/V) converter, but stabilization of this op amp is complicated by the DAC output impedance variation with digital code. As was previously mentioned, this architecture is sometimes referred to as an "inverted R-2R" DAC.



**Figure 6: Current-Mode R-2R Ladder Network DAC
Often Used in Multiplying DACs**

Current-mode operation has a larger switching glitch than voltage mode since the switches connect directly to the output line(s). However, since the switches of a current-mode ladder network are always at ground potential, their design is less demanding and, in particular, their voltage rating does not affect the reference voltage rating. If switches capable of carrying current in either direction (such as CMOS devices) are used, the reference voltage may have either polarity, or may even be ac. Such a structure is one of the most common types used as a multiplying DAC (MDAC).

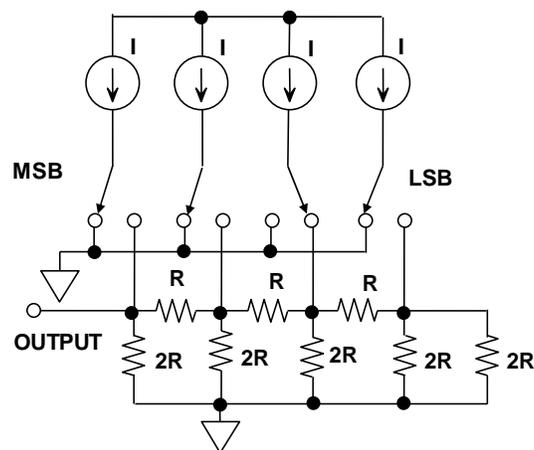
Since the switches are always at, or very close to, ground potential, the maximum reference voltage may greatly exceed the logic voltage, provided the switches are make-before-break—which they are in this type of DAC—and the resistors must be thin film. It is not uncommon for a CMOS MDAC to accept a ± 30 V reference (or even a 60-V peak-to-peak ac reference) while working from a single 5-V supply.

In all DACs, the output is the product of the reference voltage and the digital code, so in that sense, all DACs are multiplying DACs. But some DACs use an external reference voltage which may be varied over a wide range. These are "Multiplying DACs" or MDACs where the analog output is the product of the analog input and the digital code. They are extremely useful in many different applications. A strict definition of an MDAC is that it will continue to work correctly as its reference is reduced to zero, but sometimes the term is used less stringently for DACs which work with a reference range of 10:1 or even 6:1—a better name for devices of this type might be "semi-multiplying" DACs.

While some types of multiplying DACs will work only with references of one polarity (*two quadrant*) others handle bipolar (positive or negative) references, and can work with an ac signal as a reference as well. A bipolar DAC that will work with bipolar reference voltages is known as a *four-quadrant* multiplying DAC. Some types of MDACs are so configured that they can work with reference voltages substantially greater than their supply voltage.

Current-mode ladder networks and CMOS switches permit positive, negative, and ac V_{REF} as previously shown in Figure 6. While this is a simple implementation of an MDAC, several others are possible.

Another popular form of R-2R DAC switches equal currents into the R-2R network as shown in Figure 7. This architecture was first implemented by Bernard M. Gordon at EPSCO (now Analogic, Inc.) in a vacuum tube 11-bit, 50-kSPS successive approximation ADC. Gordon's 1955 patent application (Reference 5) describes the ADC, which was the first commercial offering of a complete converter. In this architecture the output impedance of the DAC is equal to R, and this structure is often used in high-speed video DACs. A distinct advantage is that only a 2:1 resistor ratio is required regardless of the resolution. In some applications, however, the relatively low output impedance of the R-2R network can be a disadvantage.



Adapted from: Bernard M. Gordon and Robert P. Talambiras, "Signal Conversion Apparatus," U.S. Patent 3,108,266, filed July 22, 1955, issued October 22, 1963

Figure 7: Equal Current Sources Switched into an R-2R Ladder Network

Figure 8 shows a DAC using binary-weighted currents switched into a load. The output impedance is high, and this architecture generally has a volt or so of output compliance. The main problem with all of the binary-weighted DACs discussed thus far is that high resolutions require large resistor ratios, making manufacture very difficult.

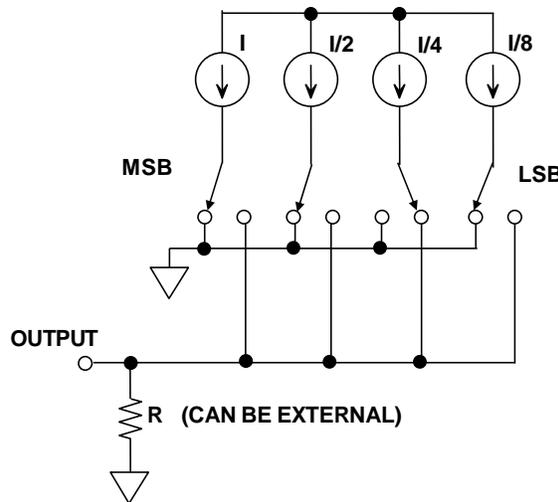


Figure 8: Binary-Weighted Current Sources Switched into a Load

SOME HISTORICAL PERSPECTIVE ON MONOLITHIC DACs

In 1970 Analog Devices introduced the AD550 "μDAC" monolithic quad (4-bit) current switch building block IC shown in Figure 9. Notice that the binary-weighted currents were generated using an external thin film network—on-chip laser trimmed thin film resistor technology was not developed until several years later. The transistor areas are scaled (8:4:2:1), thereby ensuring equal current densities in all the transistors for optimum V_{BE} matching.

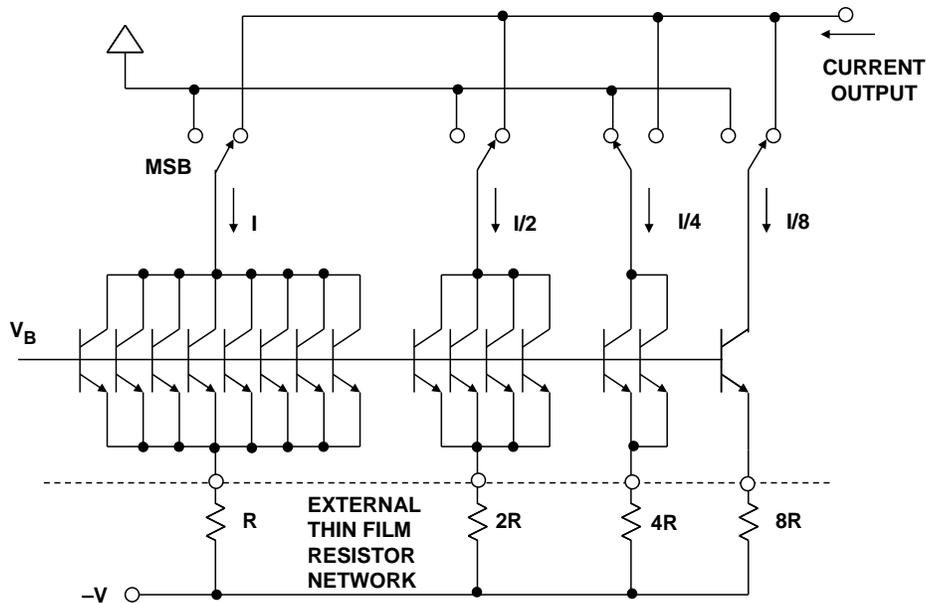
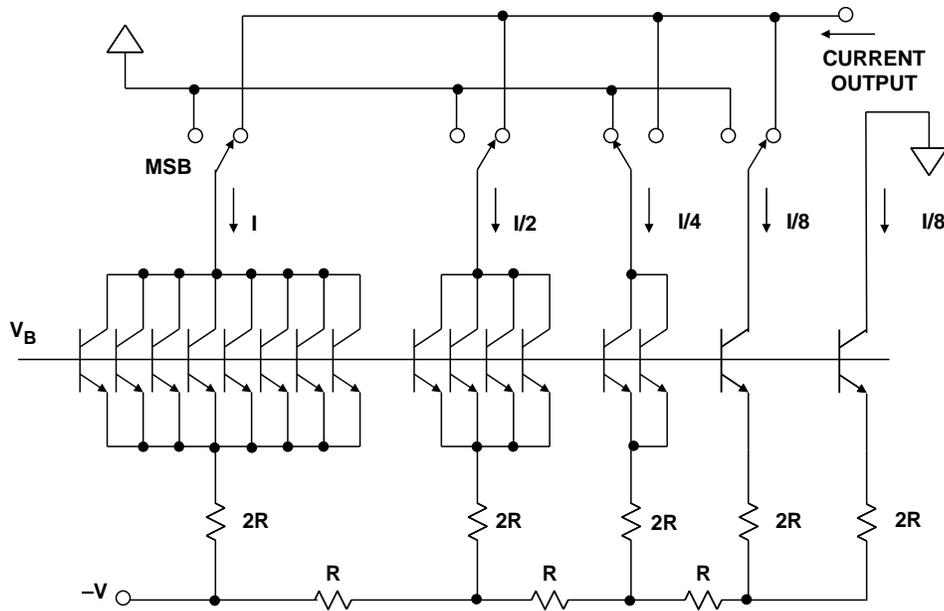


Figure 9: Binary-Weighted 4-Bit DAC, the AD550 "μDAC" Quad Switch

An alternative method of developing the binary-weighted currents in the quad switch is shown in Figure 10, where an R-2R ladder network connected to the transistor emitters accomplishes the binary current division.



**Figure 10: Binary-Weighted 4-Bit DAC:
R/2R Ladder Network Current Setting Resistors**

Figure 11 shows how three AD550 quad switches with 16:1 inter-stage attenuators are connected to form a 12-bit current-output DAC. Note that the maximum required resistor ratio of 16:1 is manageable. This monolithic "quad switch" (AD550 μ DAC) along with a thin film resistor network (AD850), voltage reference, and an op amp formed the popular building blocks for 12-bit DACs in the early 1970s before the complete function was available in IC form several years later. The concept for the quad switch was patented by James J. Pastoriza (1970 filing, Reference 6).

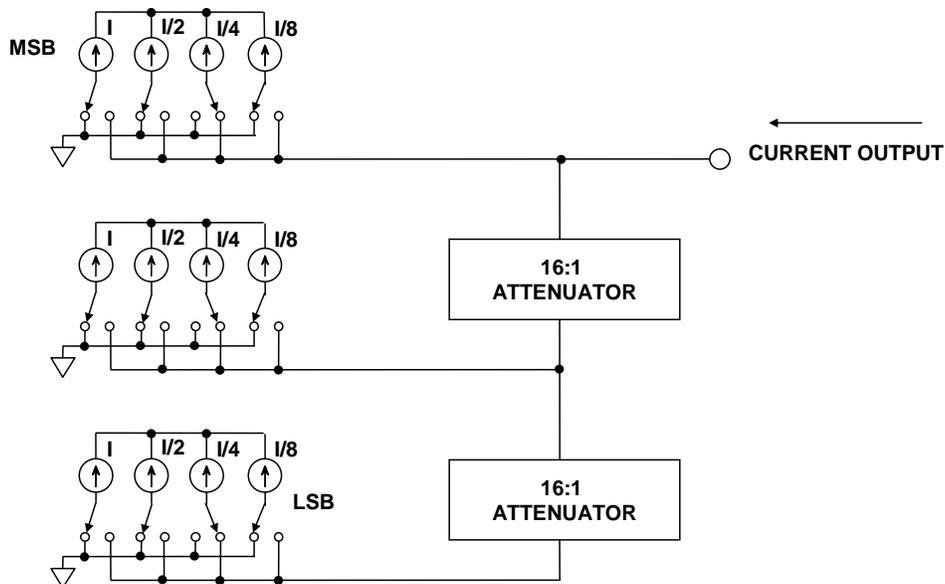
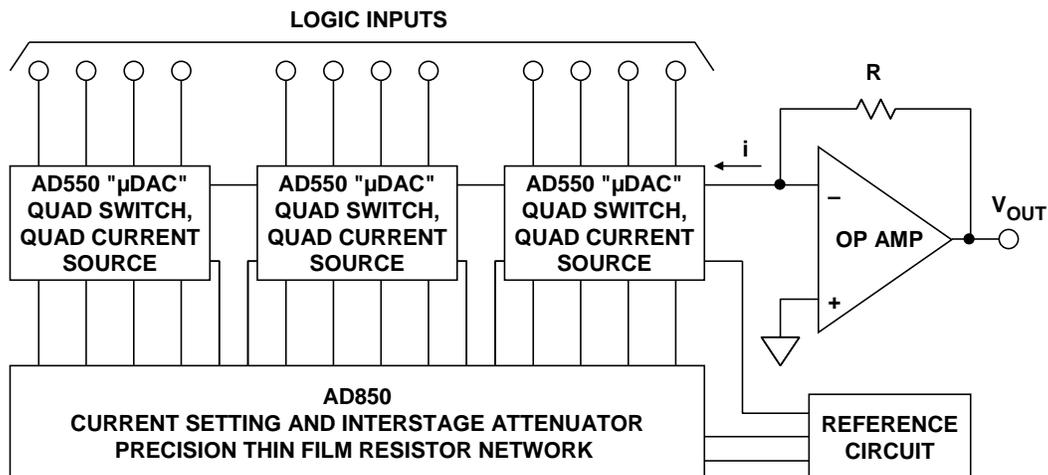


Figure 11: 12-Bit Current-Output DAC Using Cascaded Binary "Quad Switches"

The complete 1970-vintage 12-bit DAC solution, shown in Figure 12, consists of three monolithic quad switches, a thin-film resistor network, an op amp, and a voltage reference. The matching provided by the monolithic quad switches along with the accuracy and tracking of the external thin film network provided 12-bit performance without the need for additional trimming. An interesting and complete analysis of this 12-bit DAC based on the quad switches can be found in Reference 7.



James J. Pastoriza, "Solid State Digital-to-Analog Converter,"
U.S. Patent 3,747,088, filed December 30, 1970, issued July 17, 1973

Figure 12: A 1970 Vintage 12-Bit DAC Using Quad Current Switches, Thin Film Resistor Network, Op Amp, and Zener Diode Voltage Reference

One of the problems in implementing a completely monolithic 12-bit DAC using the quad switch approach is that each 4-bit DAC requires emitter areas scaled 8:4:2:1. This requires a total of 15 unit emitter areas, and consumes a fairly large chip area. A few years after the introduction of the quad switch building block, Paul Brokaw of Analog Devices invented a technique in which only the first two current sources have an emitter scaling of 2:1. Subsequent current sources have the same unit emitter area but operate at different current densities—while still maintaining stable currents over temperature. Paul Brokaw's classic patent (filed in 1975) describes this technique in detail, and this particular patent is probably the most referenced and cited patent relating to data converters (Reference 8).

It should be noted that the basic circuit principles set forth in these early IC DACs are still widely used today.

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2. John C. Schelleng, "Code Modulation Communication System," *U.S. Patent 2,453,461*, Filed June 19, 1946, Issued November 9, 1948. (*vacuum tube binary DAC using binary weighted voltages summed into load resistor with equal resistor weights*).
3. B. D. Smith, "Coding by Feedback Methods," *Proceedings of the I. R. E.*, Vol. 41, August 1953, pp. 1053-1058. (*Smith uses an internal binary weighted DAC and also points out that a non-linear transfer function can be achieved by using a DAC with non-uniform bit weights, a technique which is widely used in today's voiceband ADCs with built-in companding. He was also one of the first to propose using an R/2R ladder network within the DAC core*).
4. Bruce K. Smith, "Digital Attenuator," *U.S. Patent 1,976,527*, filed July 17, 1958, issued March 21, 1961. (*describes a transistorized voltage output DAC similar to B. D. Smith above*).
5. Bernard M. Gordon and Robert P. Talambiras, "Signal Conversion Apparatus," *U.S. Patent 3,108,266*, filed July 22, 1955, issued October 22, 1963. (*classic patent describing Gordon's 11-bit, 50kSPS vacuum tube successive approximation ADC done at Epsco. The internal DAC represents the first known use of equal currents switched into an R/2R ladder network.*)
6. James J. Pastoriza, "Solid State Digital-to-Analog Converter," *U.S. Patent 3,747,088*, filed December 30, 1970, issued July 17, 1973. (*the first patent on the quad switch approach to building high resolution DACs*).
7. Eugene R. Hnatek, *A User's Handbook of D/A and A/D Converters*, John Wiley, New York, 1976, ISBN 0-471-40109-9, pp. 282-295. (*contains an excellent description of the Analog Devices' AD550 monolithic μ DAC quad current switch, and AD850 thin film network—building blocks for 12-bit DACs introduced in 1970*).
8. Adrian Paul Brokaw, "Digital-to-Analog Converter with Current Source Transistors Operated Accurately at Different Current Densities," *U.S. Patent 3,940,760*, filed March 21, 1975, issued February 24, 1976. (*the most referenced data converter patent ever issued*).
9. Walt Kester, [Analog-Digital Conversion](#), Analog Devices, 2004, ISBN 0-916550-27-3, Chapter 3. Also available as [The Data Conversion Handbook](#), Elsevier/Newnes, 2005, ISBN 0-7506-7841-0, Chapter 3.

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