

SECTION 8

HARDWARE DESIGN TECHNIQUES

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ANALOG CIRCUIT SIMULATION

In recent years there has been much pressure placed on system designers to verify their designs with computer simulations before committing to actual printed circuit board layouts and hardware. Simulating complex digital designs is extremely beneficial, and very often, the prototype phase can be eliminated entirely. However, bypassing the prototype phase in high-speed/high-performance analog or mixed-signal circuit designs can be risky for a number of reasons.

For the purposes of this discussion, an *analog* circuit is any circuit which uses ICs such as op amps, instrumentation amps, programmable gain amps (PGAs), voltage controlled amps (VCAs), log amps, mixers, analog multipliers, voltage references, etc. A *mixed-signal* circuit is an A/D converter (ADC), D/A converter (DAC), or combinations of these in conjunction with some amount of digital signal processing which may or may not be on the same IC as the converters. Switching regulators must be classified as high-speed analog circuits because of the frequencies generated by the internal or external switching action.

Consider a typical IC operational amplifier. It may contain some 20-40 transistors, almost as many resistors, and a few capacitors. A complete SPICE (Simulation Program with Integrated Circuit Emphasis, see Reference 1) model will contain all these components, and probably a few of the more important parasitic capacitances and spurious diodes formed by the various junctions in the op-amp chip. For high-speed ICs, the package and wirebond parasitics may also be included. This is the type of model that the IC designer uses to optimize the device during the design phase and is typically run on a CAD workstation. Because it is a detailed model, it will be referred to as a *micromodel*. In simulations, such a model will behave very much like the actual op-amp, but not exactly.

The IC designer uses transistor and other device models based on the actual process upon which the component is fabricated. Semiconductor manufacturers invest considerable time and money developing and refining these device models so that the IC designers can have a high degree of confidence that the first silicon will work and that mask changes (costing additional time and money) required for the final manufactured product are minimized.

However, these *device* models are not published, neither are the IC *micromodels*, as they contain proprietary information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing several ICs (each represented by its own micromodel) to reach a useful result. SPICE micromodels of analog ICs often fail to converge (especially under transient conditions), and multiple IC circuits make this a greater possibility.

For these reasons, the SPICE models of analog circuits published by manufacturers or software companies are *macromodels* (as opposed to *micromodels*), which simulate the major features of the component, but lack fine detail. Most manufacturers of linear ICs (including Analog Devices) provide these macromodels for components such as operational amplifiers, analog multipliers, references, etc. (Reference 2 and 3). These models represent *approximations* to the actual circuit, and parasitic effects such as package capacitance and inductance and PC board layout are rarely included. The models are designed to work with various versions of SPICE simulation programs such as PSpice® (Reference 4) and run on workstations or personal computers. The models are simple enough so that circuits using multiple ICs can be simulated in a reasonable amount of computation time and with good certainty of convergence. Consequently, SPICE modeling does not always reproduce the exact performance of a circuit and should always be verified experimentally using a carefully built prototype.

Finally, there are mixed-signal ICs such as A/D and D/A converters which have *no* SPICE models, or if they exist, the models do not simulate dynamic performance (Signal-to-noise, effective bits, etc.), and prototypes of circuits using them should always be built. In addition to mixed-signal ICs, switching regulators do not lend themselves to SPICE modelling. The dynamics of either magnetic-based or switched capacitor-based regulators are far too complex for simple macromodels.

ANALOG CIRCUIT SIMULATION CONSIDERATIONS

- **ADSpice Macromodels (Over 500) Exist for the Following:**
 - ◆ **Amplifiers**
 - ◆ **Analog Multipliers**
 - ◆ **Multiplexers and Switches**
 - ◆ **Voltage References**
- **No Practical SPICE Macromodels for:**
 - ◆ **ADCs, DACs**
 - ◆ **Switching Regulators**
- **There is No Substitute for a Good Prototype!!**

Figure 8.1

PROTOTYPING TECHNIQUES

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The basic principle of a breadboard or prototype is that it is a *temporary* structure, designed to test the performance of a circuit or system, and must therefore be easy to modify.

There are many commercial prototyping systems, but almost all of them are designed to facilitate the prototyping of *digital* systems, where noise immunities are hundreds of millivolts or more. Non copper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems are, without exception, unsuitable for high performance or high frequency analog prototyping because their resistance, inductance, and capacitance are too high. Even the use of standard IC sockets is inadvisable in many prototyping applications.

An important consideration in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits (including switching power supplies) as well as low speed precision circuits (including references and low dropout linear regulators), especially when prototyping circuits involving ADCs or DACs. The differentiation between *high-speed* and *high-precision* mixed-signal circuits is difficult to make. For example, 16+ bit ADCs (and DACs) may operate on high speed clocks (>10MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100kSPS. Successful prototyping of these circuits requires that equal attention be given to good high-speed and high-precision circuit techniques. Switching regulators also fall into the high-speed category. Even though their desired output is a DC voltage, low output ripple voltage is highly dependent upon the use of proper high-speed grounding, layout, and decoupling techniques.

The simplest technique for analog prototyping uses a solid copper-clad board as a ground plane (Reference 5 and 6). The ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows HF decoupling paths to be very short. All lead lengths should be as short as possible, and signal routing should separate high-level and low-level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, 18-gauge or larger insulated wire should be used. Parallel runs should not be "bundled" because of possible coupling. Ideally the layout (at least the relative placement of the components on the board) should be similar to the layout to be used on the final PCB. This approach is often referred to as *deadbug prototyping* because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

Figure 8.2 shows a hand-wired breadboard using two high speed op amps which gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120Ω , although this may vary as much as $\pm 40\%$ depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect both sides together with short pieces of wire soldered to both sides of the board. If care is not taken, however, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

HANDWIRED "DEADBUG" PROTOTYPE

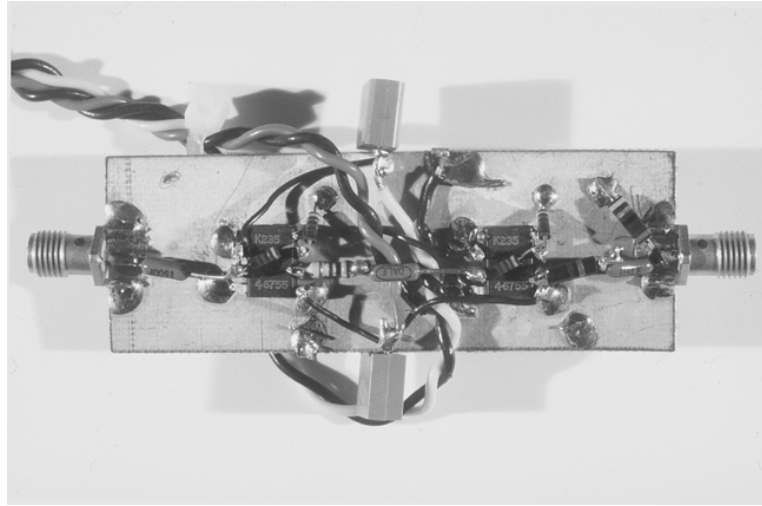


Figure 8.2

Pieces of copper-clad board may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with connections through holes) with the board itself providing screening. In this case, the board will need standoffs at the corners to protect the components on the underside from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Robert A. Pease of National Semiconductor (Reference 6) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also, if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless, the technique is very practical and widely used because the circuit may easily be modified (assuming the person doing the modifications is adept at using a soldering iron, solder-wick, and a solder-sucker).

Copper-clad boards are available with pre-drilled holes on 0.1" centers (Reference 7). Because of the loss of copper area due to the pre-drilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board. However, this type of board is convenient if the ICs in the prototype have the proper pin spacing.

In a variation of this technique, the ICs and other components are mounted on the non-copper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. The copper surrounding each

hole used for a via must be drilled out to prevent shorting. This approach requires that all IC pins be on 0.1" centers. Low profile sockets can be used for low frequency circuits, and the socket pins allow easy point-to-point wiring.

There is a commercial breadboarding system which has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages: it is rigid, components are close to the ground plane, and where necessary, node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" (Reference 8).

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 3-pin SOT-23 packages to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50 Ω , 60 Ω , 75 Ω or 100 Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low-inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors. A few of the many types of Solder-Mount building-block components are shown in Figure 8.3.

SAMPLES OF "SOLDER-MOUNT" COMPONENTS

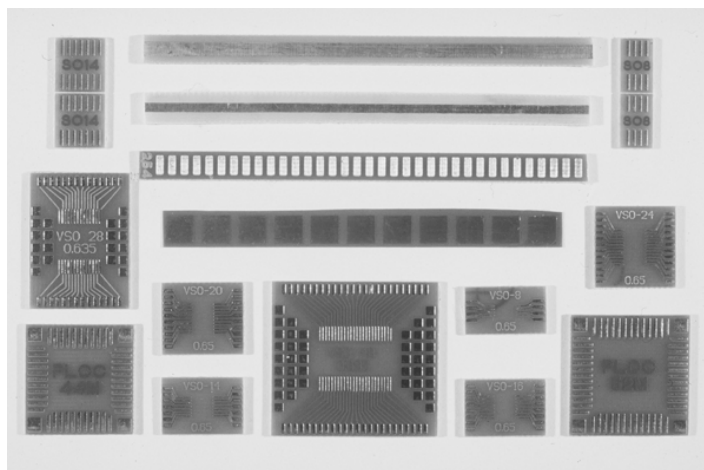


Figure 8.3

HARDWARE DESIGN TECHNIQUES

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PC board, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

Both the "deadbug" and the "Solder-Mount" prototyping techniques become somewhat tedious for complex analog or mixed-signal circuits. Larger circuits are often better prototyped using more formal layout techniques.

Another approach to prototyping analog circuits is to actually lay out a single or double-sided board using CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections (Reference 9). Although most layout software has some amount of auto-routing capability, this feature is best left to digital designs. After the components are placed in their desired positions, the interconnections should be routed manually following good analog layout guidelines. After the layout is complete, the software verifies the connections per the schematic diagram net list.

Many design engineers find that they can use CAD techniques to lay out simple boards themselves, or work closely with a layout person who has experience in analog circuit boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made. Rather than use a PC board manufacturer, however, automatic drilling and milling machines are available which accept the PG tape directly (Reference 10). These systems produce single and double-sided circuit boards directly by drilling all holes and use a milling technique to remove copper, and to create insulation paths for the finished board. The result is a board very similar to the final manufactured double-sided PC board, the chief exception being that there is no "plated-through" hole capability, and any "vias" between the two layers of the board must be wired and soldered on both sides. Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit, typically 10 to 12 mils.

Figures 8.4 and 8.5 show the top and bottom side of a switching regulator prototype based on the ADP3000. A CAD system was used in the layout, and the board was fabricated using a PC board milling machine (board cutter). The size of the board is approximately 2.5" by 3.5".

The input to the regulator is on the left-hand side of the board (top view), and it is decoupled directly to the ground plane with three 33 μ F/16V tantalum surface mount capacitors. Note that the connections are directly from the input pad to the ground plane for minimum parasitic series resistance and inductance. The ADP3000 IC is mounted in a low-profile socket on the bottom side of the board near the center. The external energy transfer inductor is located in the upper part of the board slightly to the right of the center of the board. It is mounted in an encapsulated plastic package suitable for surface mounting. The output of the ADP3000 is decoupled with a

33 μ F/16V surface mount capacitor and is followed by an LC filter before connecting to the output load.

Notice that all connections are short, especially those to the surface mount capacitors. This isolates the high-speed switching currents to a small area and prevents interference with other circuits which the regulator may be supplying.

HANDWIRED PROTOTYPE (ADP3000) TOP VIEW

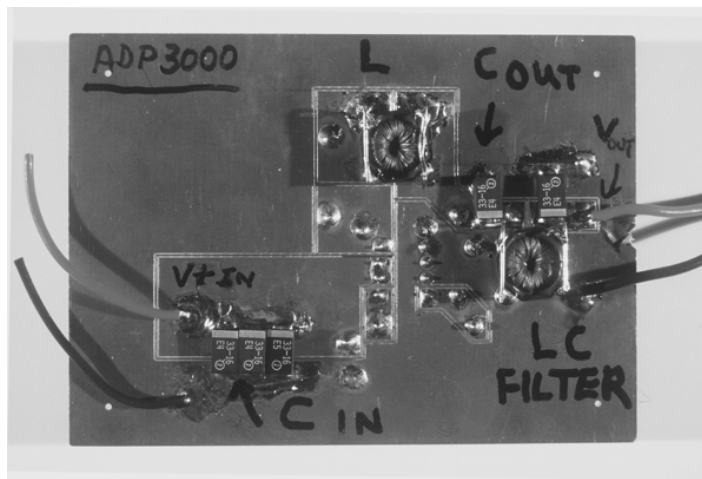


Figure 8.4

In Figure 8.5 (bottom view) note that the ADP3000 is mounted in a low profile IC socket for convenience. The "catch diode" is located directly beneath the ADP3000. The two resistors to the right of the ADP3000 set the output voltage, and the resistor above and to the left of the ADP3000 is the current-limiting resistor. The loop of wire allows the inductor current to be monitored with a current probe. Note that the resistors are in individual pin sockets to allow easy modifications.

HANDWIRED PROTOTYPE (ADP3000) BOTTOM VIEW

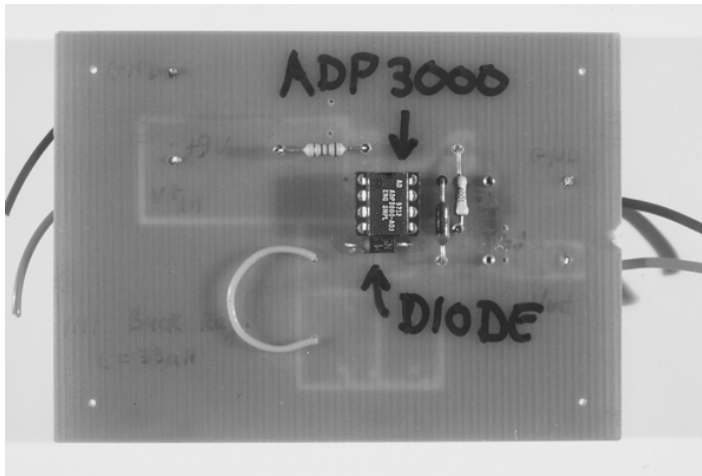


Figure 8.5

IC sockets, however, can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even *low-profile* sockets often introduce enough parasitic capacitance and inductance to degrade the performance of the circuit. If sockets must be used in high speed circuits, an IC socket made of individual *pin sockets* (sometimes called *cage jacks*) mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5mm around each ungrounded pin socket and solder the grounded ones to ground on both sides of the board). Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections between them (see Figure 8.6).

The spring-loaded gold-plated contacts within the pin socket makes good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket, and pin sockets should never be used in the high-current paths associated with linear or switching regulators. The uncapped versions allow the IC pins to extend out the bottom of the socket. After the prototype is functional and no further changes are to be made, the IC pins can be soldered directly to the bottom of the socket, thereby making a permanent and rugged connection.

PIN SOCKETS (CAGE JACKS) HAVE MINIMUM PARASITIC RESISTANCE, INDUCTANCE, AND CAPACITANCE

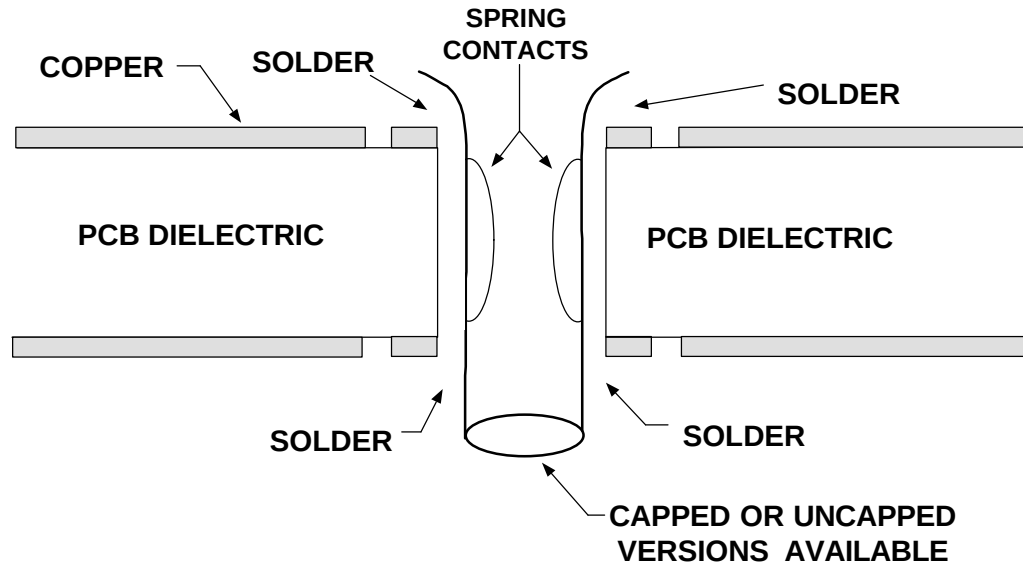


Figure 8.6

The prototyping techniques discussed so far have been limited to single or double-sided PC boards. Multilayer PC boards do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multi-layer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic capacitance ($<1\text{pF}$) between the prototype and the final board may cause subtle differences in bandwidth and settling time. Oftentimes prototyping is done with DIP packages, when the final production package is an SOIC. This can account for differences between prototype and final PC board performance. However this option may not be available, as many new ICs are only being introduced in surface mount packages.

EVALUATION BOARDS

Walt Kester

Most manufacturers of analog ICs provide evaluation boards (usually at a nominal cost) which allow customers to evaluate products without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. The artwork or CAD file is usually made available free of charge,

should the customer wish to copy the layout directly or make modifications to suit the application.

Figure 8.7 shows the very compact evaluation board for the ADP3300 50mA low dropout linear regulator. The ADP3300 is located in the center of the board and is in a SOT-23 6-lead package. The input capacitor (C1) and output capacitor (C2) are both 0.47 μ F low inductance surface mount devices. The Noise Reduction capacitor (C3) is 10nF. Resistor R1 is a pullup resistor for the open-collector error output pin. The entire active circuit (located within the small square) is approximately 0.6" by 0.6" (15.2mm by 15.2mm).

EVALUATION BOARD FOR ADP3300 LOW DROPOUT REGULATOR



Figure 8.7

Switching regulators, such as the ADP1148, place more exacting demands on layout and decoupling. The evaluation board for the ADP1148 is shown in Figures 8.8 (top view) and 8.9 (bottom view - ground plane). The board size is approximately 2" by 2" (5.1cm by 5.1cm). The input decoupling capacitors (C1 and C1A) are each 220 μ F/25V general purpose aluminum electrolytic capacitors. Also there is a 1 μ F tantalum in parallel with C1 and C1A (labeled C2).

The output capacitors (C6 and C6A) are each low ESR OS-CON 220 μ F/10V. The ADP1148 is located to the right of the center of the board and is in a 14-pin SOIC surface mount package. The energy transfer inductor (L1) is a 68 μ H surface mount part from Coiltronics. Other readily visible components making up the regulator are two power MOSFETs (Q1 and Q2) and a 0.05 Ω current sense resistor (R2).

EVALUATION BOARD FOR ADP1148 SWITCHING REGULATOR - TOP VIEW

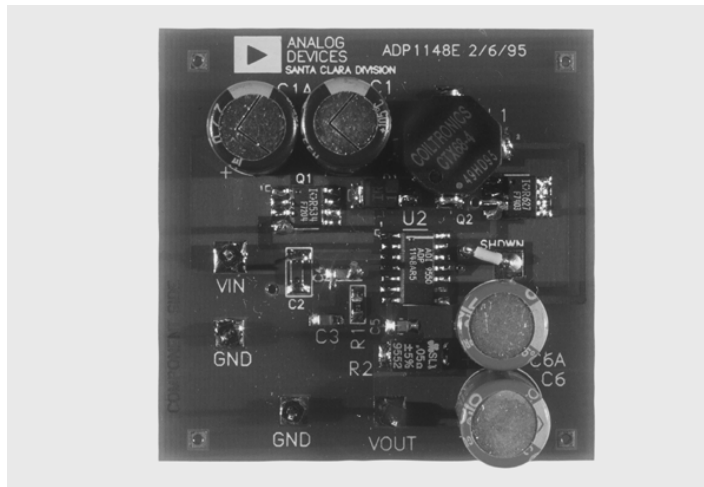


Figure 8.8

EVALUATION BOARD FOR ADP1148 SWITCHING REGULATOR - BOTTOM VIEW (GROUND PLANE)

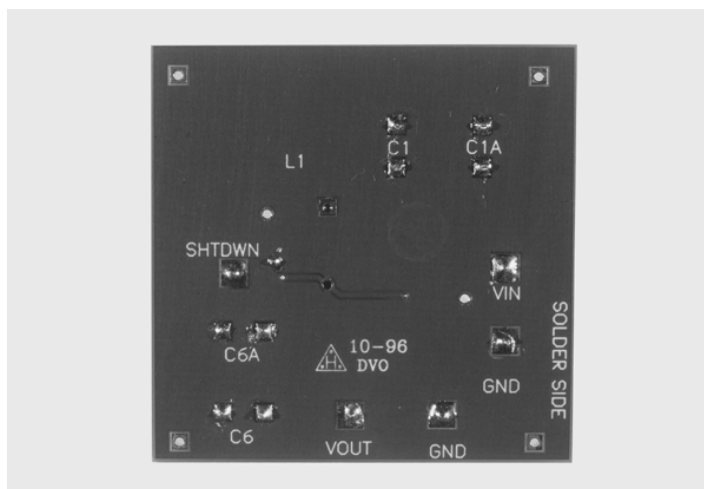


Figure 8.9

The bottom side of the board (ground plane, or "solder side") is shown in Figure 8.9. Note that with the exception of a single crossover and a few vias, the entire layer is ground plane. This in conjunction with the compact layout ensures that high frequency ground currents generated by the switching action of the regulator are localized to prevent EMI/RFI.

Evaluation boards can range from relatively simple ones (linear regulators, for example) to rather complex ones for mixed-signal ICs such as A/D converters. ADC evaluation boards often have on-board memory and DSPs for analyzing the ADC performance. Software is often provided with these more complex evaluation boards so that they can interface with a personal computer to perform complex signal analysis such as histogram and FFT testing.

In summary, good analog designers utilize as many tools as possible to ensure that the final system design performs correctly. The first step is the intelligent use of IC macromodels, where available, to simulate the circuit. The second step is the construction of a prototype board to further verify the design and the simulation. The final PCB layout should be then be based on the prototype layout as much as possible.

Finally, evaluation boards can be extremely useful in evaluating new analog ICs, and allow designers to verify the IC performance with a minimum amount of effort. The layout of the components on the evaluation board can serve as a guide to both the prototype and the final PC board layout. Gerber files are generally available for all evaluation board layouts and may be obtained at no charge.

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8. RDI Wainwright, 69 Madison Ave., Telford, PA, 18969-1829, Tel. 215-723-4333, Fax. 215-723-4620.

Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.
9. Schematic Capture and Layout Software:
PADS Software, INC, 165 Forest St., Marlboro, MA, 01752 and
ACCEL Technologies, Inc., 6825 Flanders Dr., San Diego, CA, 92121
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GROUNDING TECHNIQUES FOR REGULATOR CIRCUITS

Walt Kester, Walt Jung

The importance of maintaining a low impedance large area ground plane is critical to practically all analog circuits today, especially high current low dropout linear regulators or switching regulators. The ground plane not only acts as a low impedance return path for high frequency switching currents but also minimizes EMI/RFI emissions. In addition, it serves to minimize unwanted voltage drops due to high load currents. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced. When using multilayer PC boards, it is wise to add a power plane. In this way, low impedances can be maintained on both critical layers.

Figure 8.10 shows a grounding arrangement for a low dropout linear regulator such as the ADP3310. It is important to minimize the total voltage drop between the input voltage and the load, as this drop will subtract from the voltage dropped across the pass transistor and reduce its headroom. For this reason, these runs should be wide, heavy traces and are indicated by the wide interconnection lines on the diagram. The low-current ground (GND) and V_{OUT} (sense) pins of the ADP3310 are connected directly to the load so that the regulator regulates the voltage at the load rather than at its own output. The I_S and V_{IN} connections to the R_S current sense resistor should be made directly to the resistor terminals to minimize parasitic resistance, since the current limit resistor is typically a very low value (milliohms). In fact, for very low values it may actually consist of a PC board trace of the proper width, length, and thickness to yield the desired resistance.

GROUNDING AND SIGNAL ROUTING TECHNIQUES FOR LOW DROPOUT REGULATORS METHOD 1

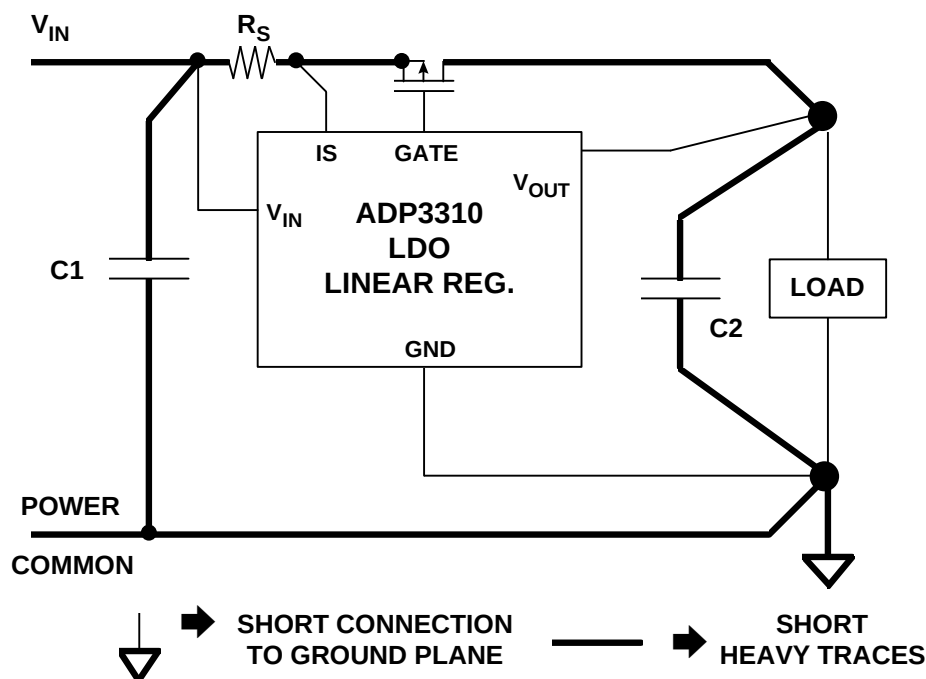


Figure 8.10

The input decoupling capacitor (C1) should be connected with short leads at the regulator input in order to absorb any transients which may couple onto the input voltage line. Similarly, the load capacitor (C2) should have minimum lead length in order to absorb transients at that point and prevent them from coupling back into the regulator. The single-point connection to the low impedance ground plane is made directly at the load.

Figure 8.11 shows a grounding arrangement which is similar to that of Figure 8.10 with the exception that all ground connections are made with direct connections to the ground plane. This method works extremely well when the regulator and the load are on the same PC board, and the load is distributed around the board rather than located at one specific point. If the load is not distributed, the connection from V_{OUT} (sense) should be connected directly to the load as shown by the dotted line in the diagram. This ensures the regulator provides the proper voltage at the load regardless of the drop in the trace connecting the pass transistor output to the load.

GROUNDING AND SIGNAL ROUTING FOR LOW DROPOUT REGULATOR METHOD 2

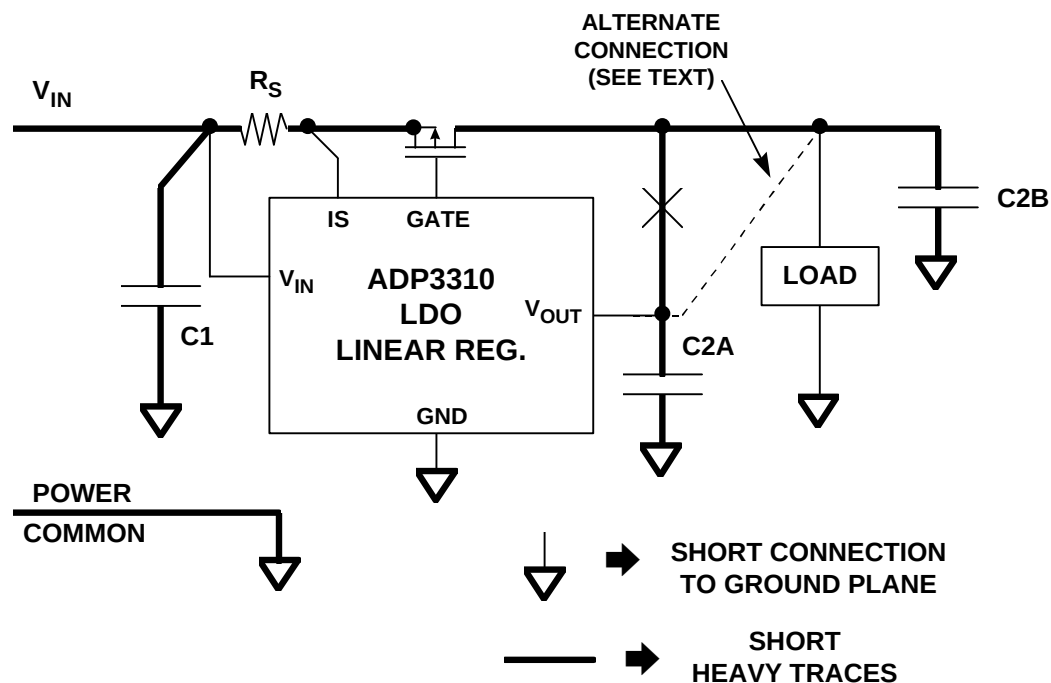
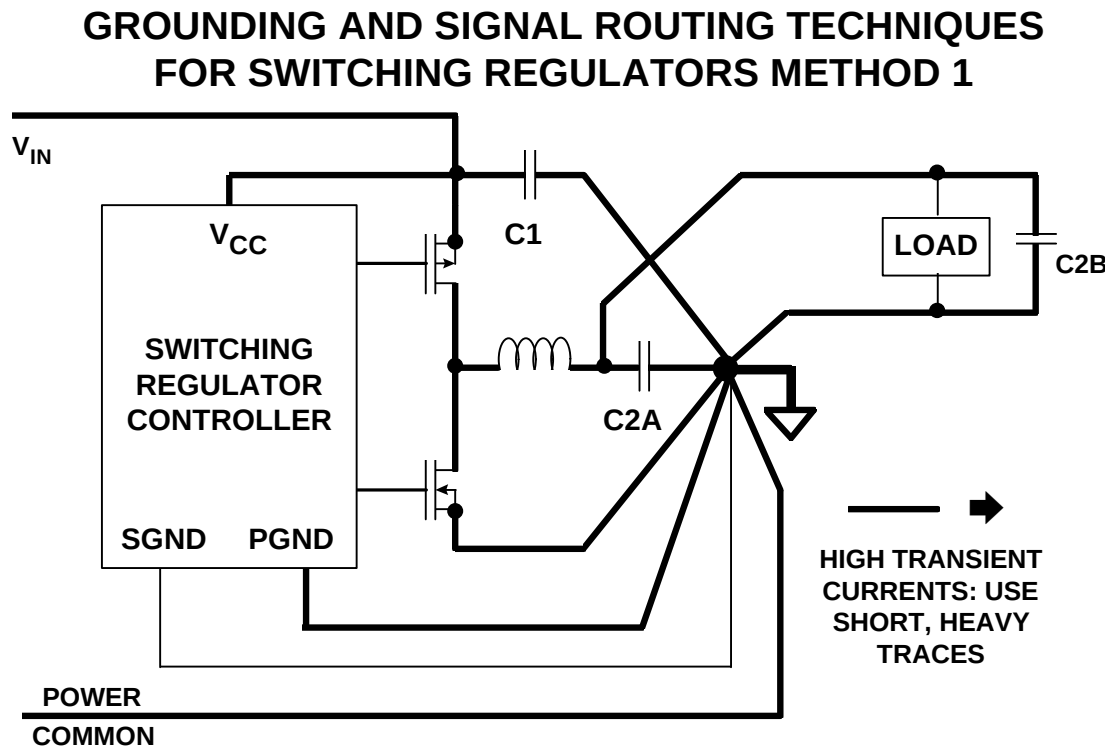


Figure 8.11

Switching regulators present major challenges with respect to layout, grounding, and filtering. The discussion above on linear regulators applies equally to switchers, although the importance of DC voltage drops may not be as great.

There is no way to eliminate high frequency switching currents in a switching regulator, since they are necessary for the proper operation of the regulator. What one must do, however, is to recognize the high switching current paths and take proper measures to ensure that they do not corrupt circuits on other parts of the

board or system. Figure 8.12 shows a generic synchronous switching regulator controller IC and the associated external MOSFET switching transistors. The heavy bold lines indicate the paths where there are large switching currents and/or high DC currents. Notice that all these paths are connected together at a single-point ground which in turn connects to a large area ground plane.



In order to minimize stray inductance and resistance, each of the high current paths should be as short as possible. Capacitors C1 and C2A must absorb the bulk or the input and output switching current and shunt it to the single-point ground. Any additional resistance or inductance in series with these capacitors will degrade their effectiveness. Minimizing the area of all the loops containing the switching currents prevents them from significantly affecting other parts of the circuit. In actual practice, however, the single-point concept in Figure 8.12 is difficult to implement without adding additional lead length in series with the various components. The added lead length required to implement the single-point grounding scheme tends to degrade the effects of using the single-point ground in the first place.

A more practical solution is to make multiple connections to the ground plane and make each of them as short as possible. This leads to the arrangement shown in Figure 8.13, where each critical ground connection is made directly to the ground plane with the shortest connection length possible. By physically locating all critical components associated with the regulator close together and making the ground connections short, stray series inductance and resistance are minimized. It is true that several small ground loops may occur using this approach, but they should not cause significant system problems because they are confined to a very small area of the overall ground plane. Refer back to Figure 8.9 (ADP1148 switching regulator

evaluation board - ground plane side) and note that this approach to grounding was used.

GROUNDING AND SIGNAL ROUTING TECHNIQUES FOR SWITCHING REGULATORS METHOD 2

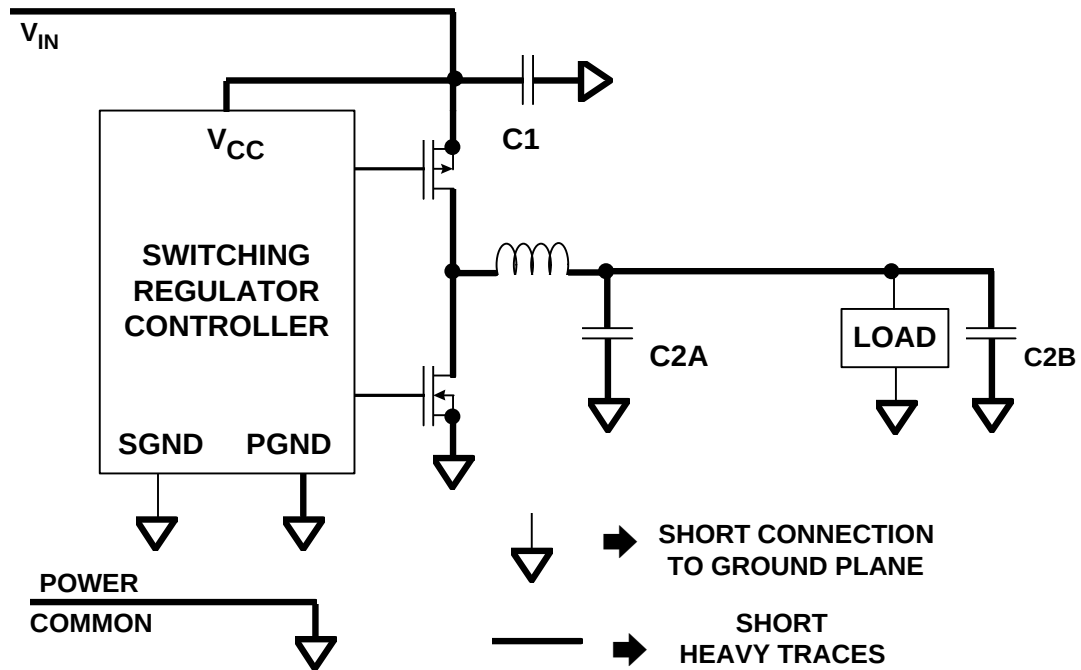


Figure 8.13

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POWER SUPPLY NOISE REDUCTION AND FILTERING

Walt Jung, Walt Kester, Bill Chestnut

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the spikes can contain frequency components extending to 100MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, with the output loading of your system.

The following section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes various DC-DC converters as well as popular 5V (PC type) supplies.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a *source*, a *path*, and a *receptor* [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. This section focuses on reducing switching power supply noise with external post filters.

Tools useful for combating high frequency switcher noise are shown by Figure 8.14. They differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small sized.

SWITCHING REGULATOR NOISE REDUCTION TOOLS

- Capacitors
- Inductors
- Ferrites
- Resistors
- Linear Post Regulation
- Proper Layout and Grounding Techniques
- PHYSICAL SEPARATION FROM SENSITIVE ANALOG CIRCUITS!!

Figure 8.14

Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory to the design of effective practical supply filters. There are generally three classes of capacitors useful in 10kHz-100MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These can in turn be further sub-divided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 8.15.

TYPES OF CAPACITORS

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	OS-CON Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 μF	120 μF	120 μF	100 μF	1 μF	0.1 μF
Rated Voltage	25 V	25 V	20 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.02 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (*)	$\cong$ 100 kHz	$\cong$ 500 kHz	$\cong$ 1 MHz	$\cong$ 1 MHz	$\cong$ 10 MHz	$\cong$ 1 GHz

(*) Upper frequency strongly size and package dependent

Figure 8.15

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They also have relatively high leakage currents (up to tens of μA , and strongly dependent upon design specifics).

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100V or less, with capacitance of 500 μF or less [Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 5]. The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in very broad value ranges and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10 μF /50V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10m Ω or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

HARDWARE DESIGN TECHNIQUES

Typically using a wound layer-type construction, film capacitors can be inductive, which can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 4, 5, 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several μF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of 0.1 μF or less, with 0.01 μF representing a more practical upper limit.

Multilayer ceramic “chip caps” are very popular for bypassing/ filtering at 10MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying “free” damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted in an impedance vs. frequency plot. This occurs where $|Z|$ falls to a minimum level, nominally equal to the capacitor’s ESR at that frequency. This low Q resonance can generally be noted to cover a relatively wide frequency range of several octaves. Contrasted to the very high Q sharp resonances of film and ceramic caps, the low Q behavior of electrolytics can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at -55°C vs. the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the -10°C ESR at 100kHz is no more than 2 $\times$ that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

As noted, all real capacitors have parasitic elements which limit their performance. The equivalent electrical network representing a real capacitor models both ESR

and ESL as well as the basic capacitance, plus some shunt resistance (see Figure 8.16). In such a practical capacitor, at low frequencies the net impedance is almost purely capacitive. At intermediate frequencies, the net impedance is determined by ESR, for example about 0.12Ω to 0.4Ω at 125kHz, for several types. Above about 1MHz these capacitor types become inductive, with impedance dominated by the effect of ESL. All electrolytics will display impedance curves similar in general shape to that of Figure 8.17. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly effected by package style).

CAPACITOR EQUIVALENT CIRCUIT AND PULSE RESPONSE

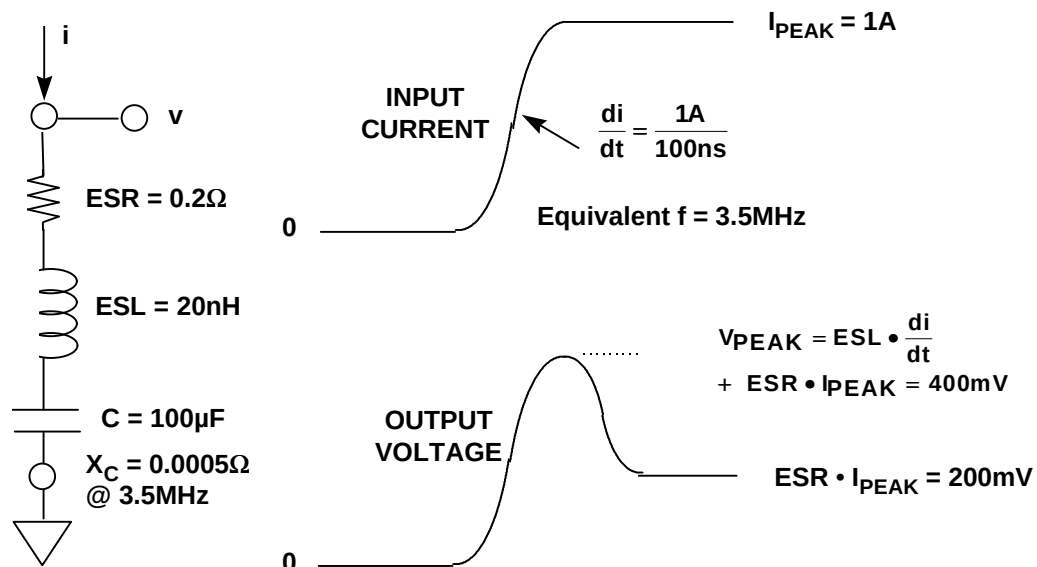


Figure 8.16

Regarding inductors, *Ferrites* (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful in power supply filters [Reference 9]. At low frequencies ($<100kHz$), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites become resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 8.18 summarize a number of ferrite characteristics.

ELECTROLYTIC CAPACITOR IMPEDANCE VERSUS FREQUENCY

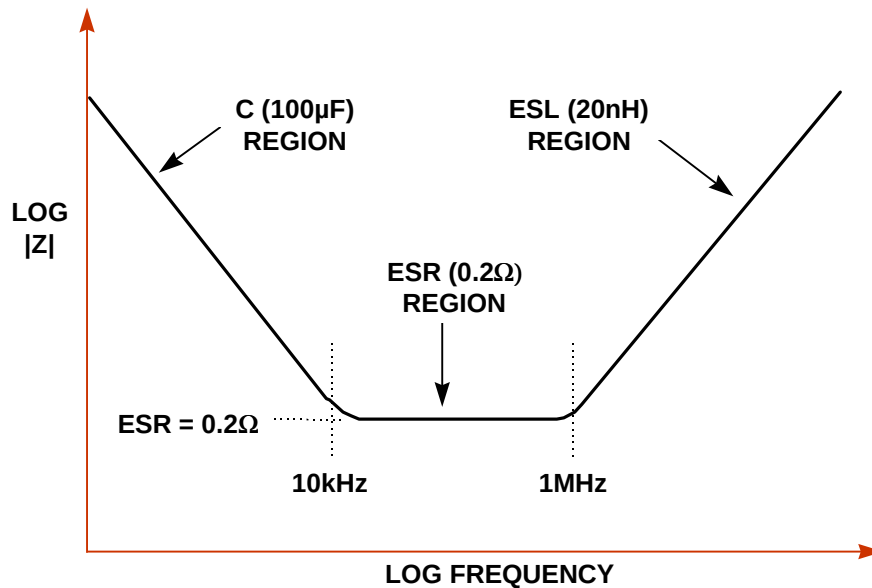


Figure 8.17

FERRITES SUITABLE FOR HIGH FREQUENCY FILTERS

- Ferrites Good for Frequencies Above 25kHz
- Many Sizes and Shapes Available Including Leaded "Resistor Style"
- Ferrite Impedance at High Frequencies Primarily Resistive -- Ideal for HF Filtering
- Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low
- High Saturation Current Versions Available
- Choice Depends Upon:
 - ◆ Source and Frequency of Interference
 - ◆ Impedance Required at Interference Frequency
 - ◆ Environmental: Temperature, AC and DC Field Strength, Size / Space Available
- Always Test the Design!

Figure 8.18

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 10 and 11). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 11). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available.

PSpice ferrite models for Fair-Rite materials are available, and allow ferrite impedance to be estimated [see Reference 12]. These models have been designed to match measured impedances rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the DC current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should lead to a proper ferrite selection.

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switcher's DC output so as to produce an *analog ready* 5V supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies. A basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to a 1-10MHz range. This larger filter is used as a *card entry filter* providing broadband filtering for all power entering a PC card. Smaller, more simple local filter stages are also used to provide higher frequency decoupling right at the power pins of individual stages.

SWITCHING REGULATOR EXPERIMENTS

In order to better understand the challenge of filtering switching regulators, a series of experiments were conducted with representative devices (see Figure 8.19).

The first series of experiments were conducted on a low power switching regulator, the ADP3000. The regulator was tested in the boost configuration with a 2V input and a 5V/100mA output. The prototype board shown previously in Figures 8.4 and 8.5 was used for the tests.

The second series of experiments were conducted on the ADP3000 configured in the buck mode with a 9V input and a 5V/100mA output. Again, the prototype board shown previously in Figures 8.4 and 8.5 was used for the tests.

The third series of experiments involved the ADP1148 synchronous buck regulator with a 9V input and a 3.3V/1A output. An evaluation board similar to that shown in Figures 8.8 and 8.9 was used.

The fourth series of experiments were conducted on the ADP1148 synchronous buck regulator driving an ADP3310 low dropout linear regulator. The ADP1148 was configured for a 9V input and a 3.75V/1A output, and the ADP3310 for a 3.3V/1A output.

The fifth series of experiments were made on the ADP3605 +5V to –3V switched capacitor voltage converter. The ADP3605 output load was set for 100mA.

FILTERING SWITCHING REGULATOR OUTPUTS - SUMMARY OF EXPERIMENTS

- **ADP3000, 2V to 5V/100mA Boost Regulator**
- **ADP3000, 9V to 5V/100mA Buck Regulator**
- **ADP1148, 9V to 3.3V/1A Buck Regulator**
- **ADP1148, 9V to 3.75V/1A Buck Regulator with
ADP3310, 3.3V/1A Linear LDO Post Regulator**
- **ADP3605, 5V to –3V/100mA Switched Capacitor
Voltage Converter**

Figure 8.19

In addition to observing typical input and output waveforms, the objective of these experiments was to reduce the output ripple to less than 10mV peak-to-peak, a value suitable for driving most analog circuits.

Measurements were made using a Tektronix wideband digitizing oscilloscope with the input bandwidth limited to 20MHz so that the ripple generated by the switching

regulators could be more readily observed. In a system, power supply ripple frequencies above 20MHz are best filtered locally at each IC power pin with a low inductance ceramic capacitor and perhaps a series-connected ferrite bead.

Probing techniques are critical for accurate ripple measurements. A standard passive 10X probe was used with a "bayonet" probe tip adapter for making the ground connection as short as possible (see Figure 8.20). Use of the "ground clip lead" is not recommended in making this type of measurement because the lead length in the ground connection forms an unwanted inductive loop which picks up high frequency switching noise, thereby corrupting the signal being measured.

PROPER PROBING TECHNIQUES

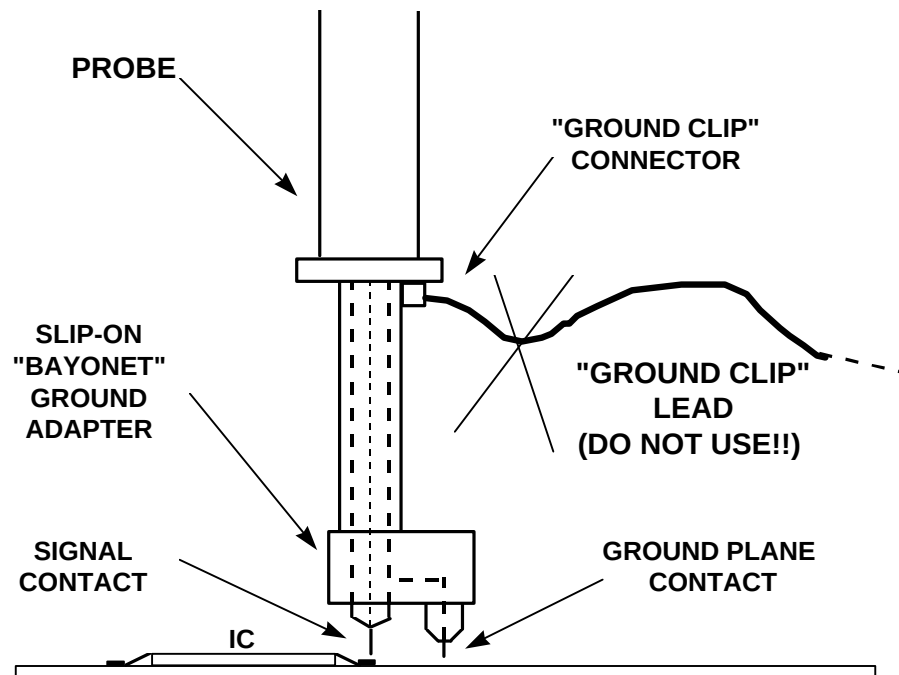


Figure 8.20

Note: Schematic representation of proper physical grounding is almost impossible. In all the following circuit schematics, the connections to ground are made to the ground plane using the shortest possible connecting path, regardless of how they are indicated in the actual circuit schematic diagram.

ADP3000 2V TO 5V/100mA BOOST REGULATOR

Figure 8.21 shows the connection diagram for the ADP3000 used as a 2V to 5V/100mA boost regulator. The actual switch is internal to the device. Multiple capacitors are used on both the input and output in order to lower the ESR and ESL.

ADP3000 2V TO 5V BOOST REGULATOR

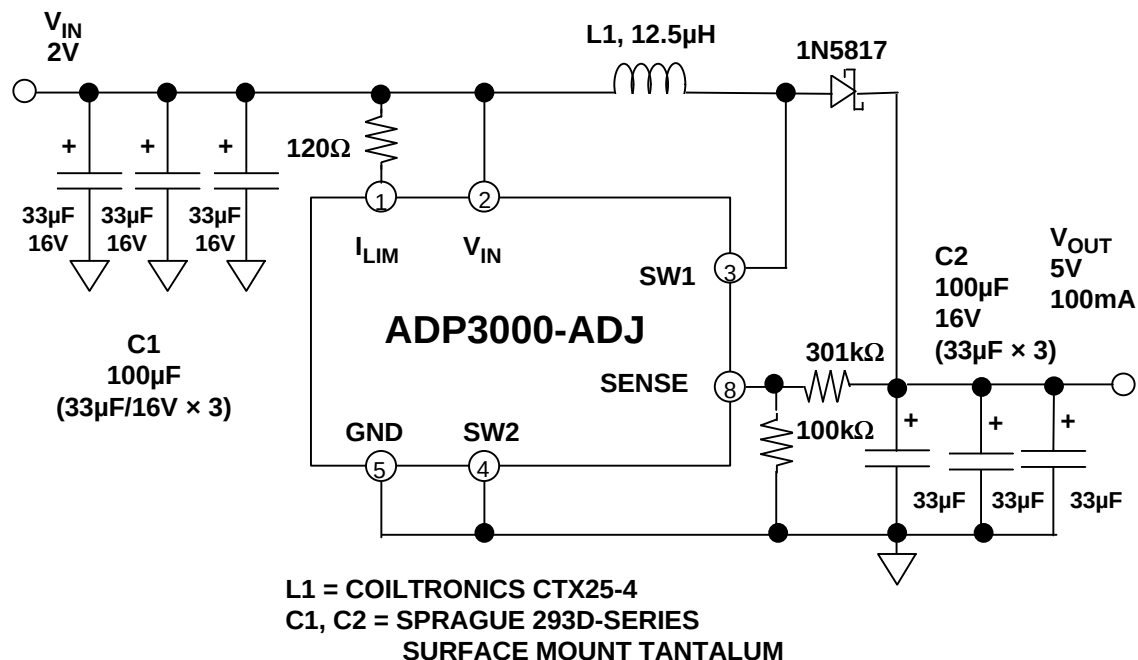
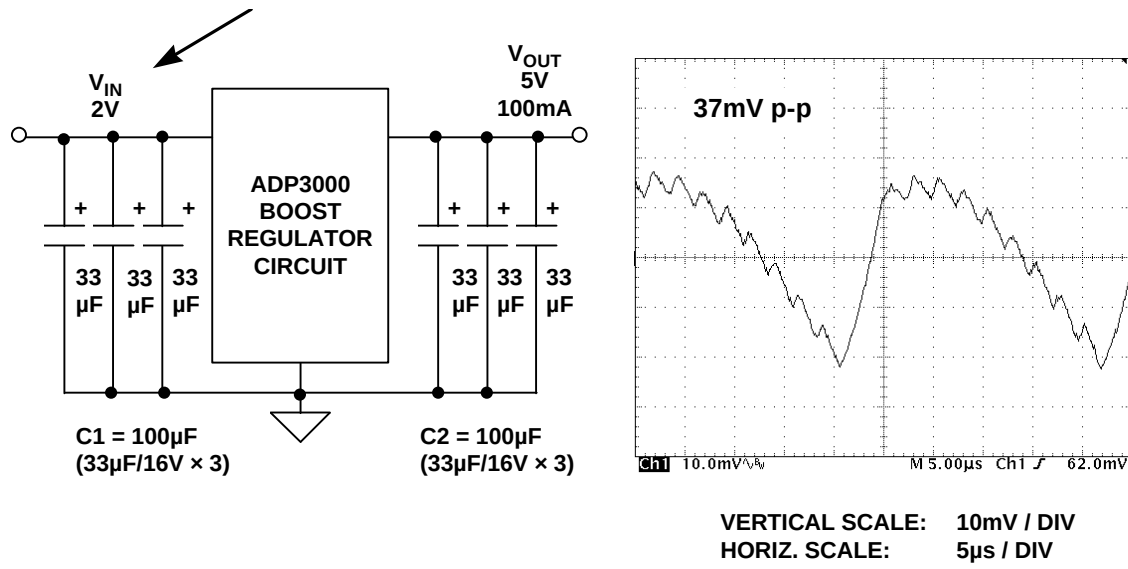


Figure 8.21

The input waveform of the boost regulator is shown in Figure 8.22 and is typical of the gated-oscillator type of regulation used in the ADP3000. It consists of series of gradually decreasing ramp waveforms during the time the inductor is being switched at the 400kHz internal oscillator rate. When the output voltage reaches the proper value, the internal oscillator is turned off, and the input capacitors recharge, as indicated by the positive-going ramp voltage. During this interval, the output voltage gradually decays until the point at which the internal oscillator is gated on again, and the cycle repeats itself.

The output waveform for the circuit is shown in Figure 8.23. This waveform is also characteristic of gated-oscillator boost regulators as indicated by the pulsating waveforms followed by the decaying ramp voltage. It should be noted that the ripple in this waveform is almost entirely determined by the equivalent ESR of the parallel combination of the output capacitors. Adding more capacitors would reduce the ripple, but a more effective method is to add an LC filter on the output as shown in Figure 8.24.

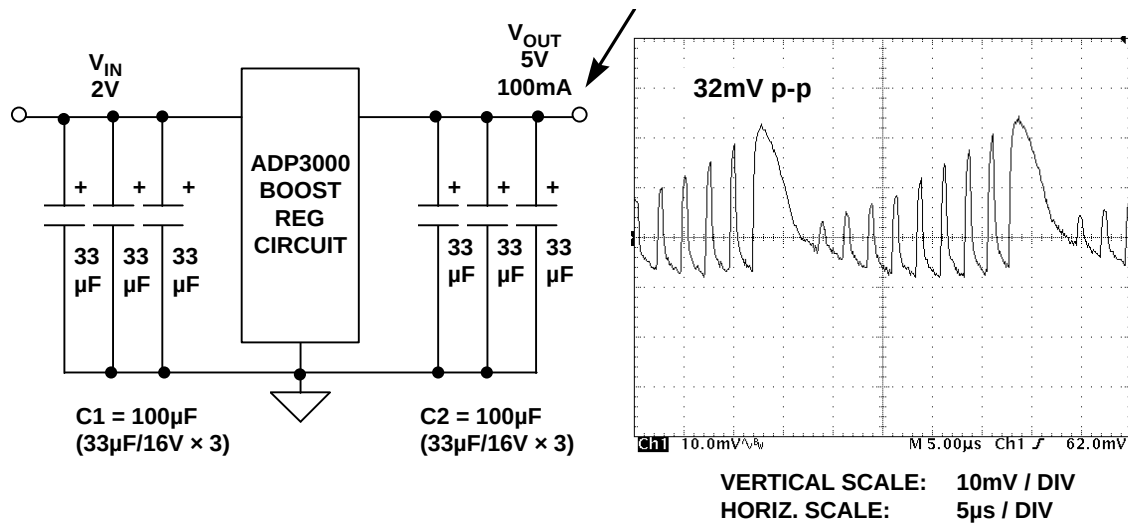
ADP3000 - BOOST INPUT WAVEFORM



$C1 = C2 = 33\mu F/16V \times 3$, SPRAGUE 293D SURFACE MOUNT TANTALUM

Figure 8.22

ADP3000 BOOST - OUTPUT WAVEFORM



$C1 = C2 = 33\mu F/16V \times 3$, SPRAGUE 293D SURFACE MOUNT TANTALUM

Figure 8.23

ADP3000 BOOST FILTERED OUTPUT, CONDITION #1

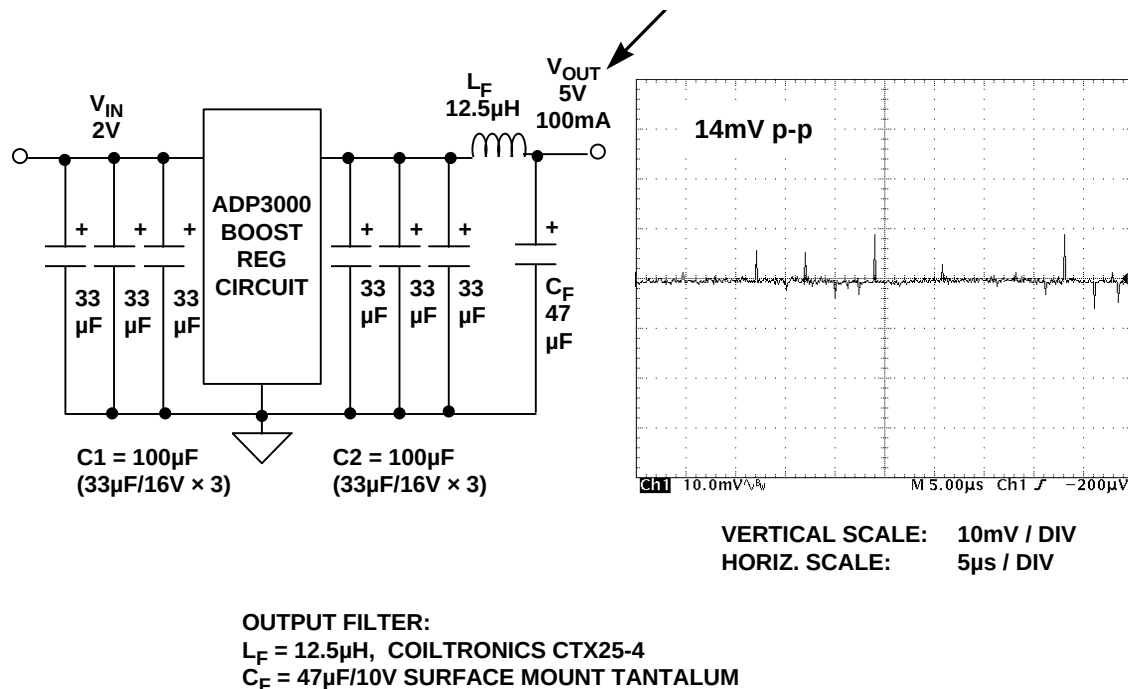


Figure 8.24

The inductor selected ($L_F = 12.5 \mu\text{H}$) was the same value and type used as the energy transfer inductor in the regulator circuit, thereby ensuring the inductor has adequate current-carrying capability. The capacitor ($C_F = 47 \mu\text{F}$) was a surface mount tantalum. Peak-to-peak ripple was reduced from 32mV to 14 mV, consisting mostly of high frequency spikes. In order to reduce the high frequency spikes, a second capacitor ($C_{F2} = 10 \mu\text{F}$) was added in parallel with the 47 μF . This output filter combination reduced the ripple to approximately 3mV as shown in Figure 8.25. The ESL of the 10 μF capacitor was approximately 2.2nH (Kemet T491C-series).

From this experiment, we concluded that the 47 μF surface mount tantalum filter capacitor had an ESL/ESR combination which was not sufficiently low to remove the high frequency ripple components. The capacitor was removed and replaced with a 33 μF tantalum (Sprague 293D-series). In addition, the regulator output capacitor ($C2$) was reduced to a single 33 μF tantalum (also Sprague 293D-series). The resulting output waveform is shown in Figure 8.26. Note that the high frequency components have been removed, but a small amount of ripple remains at the frequency of the gated oscillator bursts (approximately 40kHz).

ADP3000 BOOST FILTERED OUTPUT, CONDITION #2

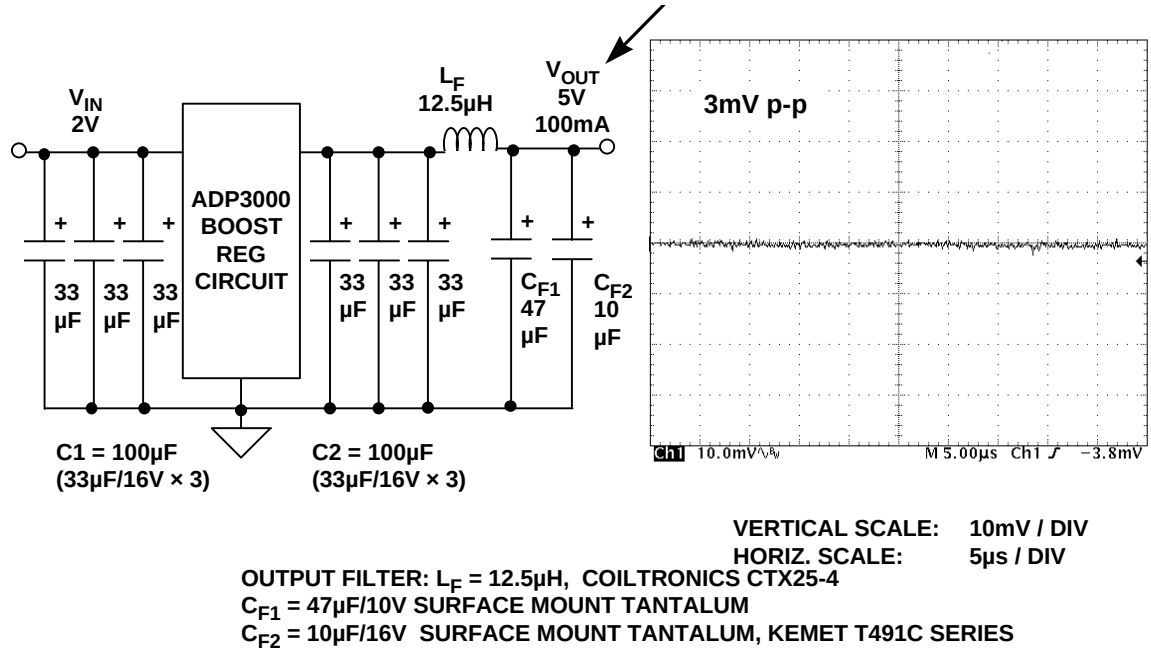


Figure 8.25

ADP3000 BOOST FILTERED OUTPUT, CONDITION #3

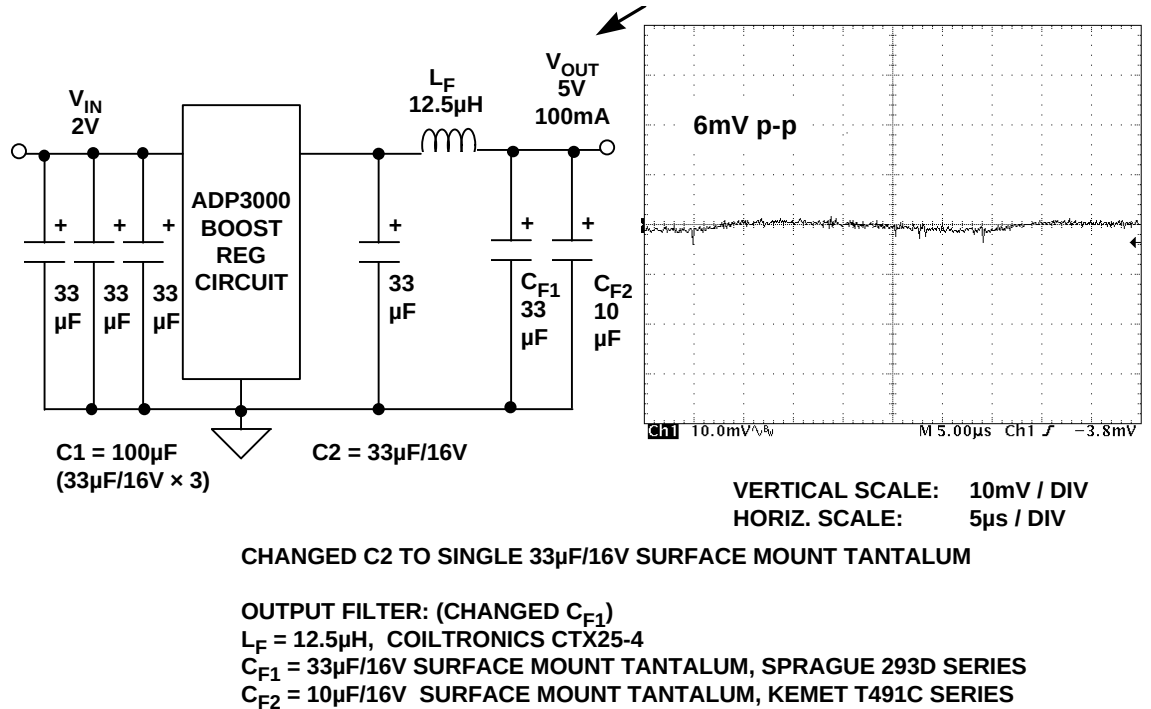


Figure 8.26

ADP3000 9V TO 5V/100mA BUCK REGULATOR

The circuit for the ADP3000 9V to 5V/100mA buck regulator is shown in Figure 8.27. The input waveform is shown in Figure 8.28. Note that the pulsating waveform followed by an increasing ramp voltage is characteristic of the gated-oscillator buck input. The corresponding output waveform is shown in Figure 8.29. The output filter chosen (see Figure 8.30) consisted of a 12.5 μ H inductor followed by a 33 μ F capacitor in parallel with a 10 μ F capacitor (identical to the filter used in the circuit shown in Figure 8.26). The ripple was reduced from 30mV to approximately 6mV peak-to-peak.

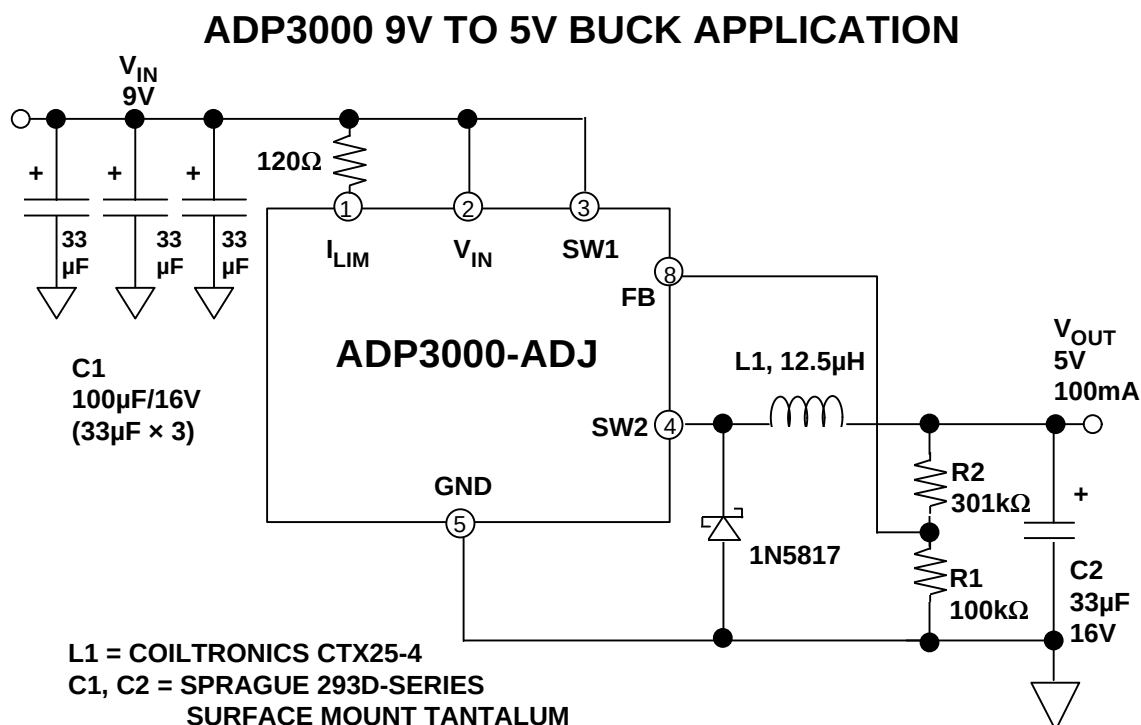
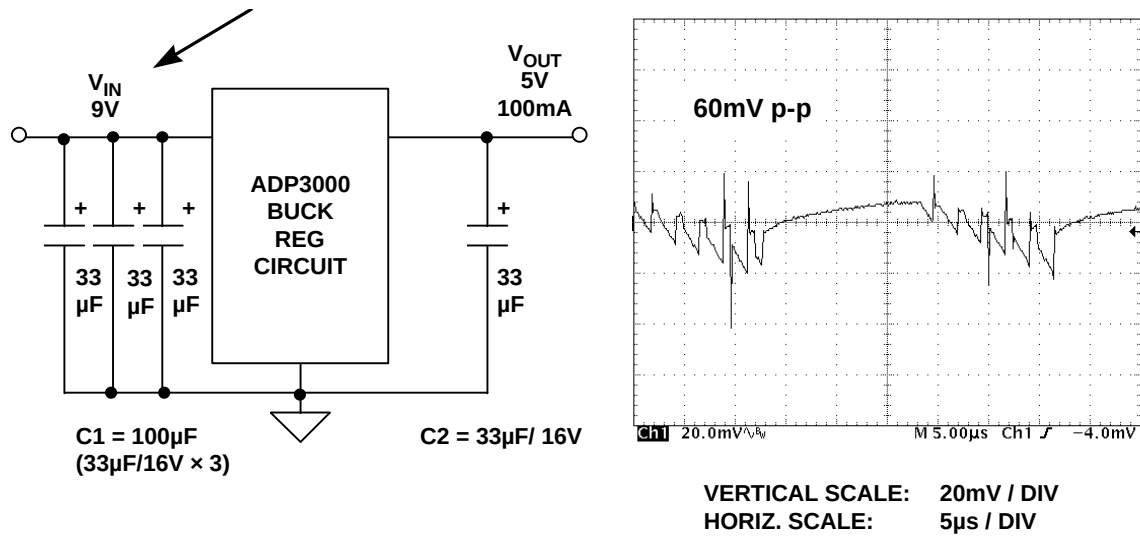


Figure 8.27

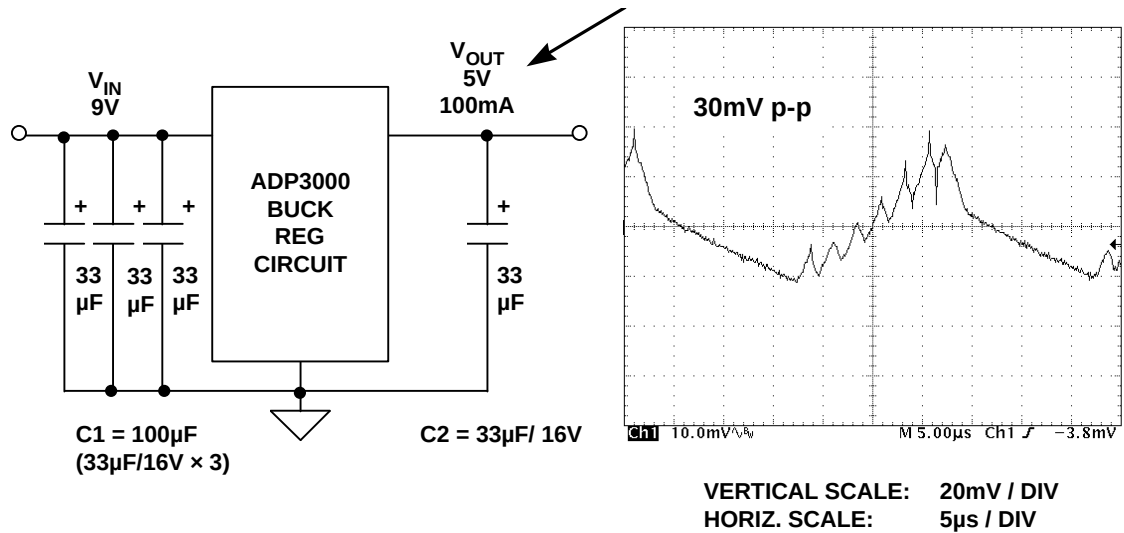
ADP3000 BUCK INPUT WAVEFORM



C1 = 33 μ F/16V $\times$ 3 , SPRAGUE 293D SURFACE MOUNT TANTALUM
C2 = 33 μ F/16V , SPRAGUE 293D SURFACE MOUNT TANTALUM

Figure 8.28

ADP3000 BUCK OUTPUT WAVEFORM



C1 = 33 μ F/16V $\times$ 3 , SPRAGUE 293D SURFACE MOUNT TANTALUM
C2 = 33 μ F/16V , SPRAGUE 293D SURFACE MOUNT TANTALUM

Figure 8.29

ADP3000 BUCK FILTERED OUTPUT

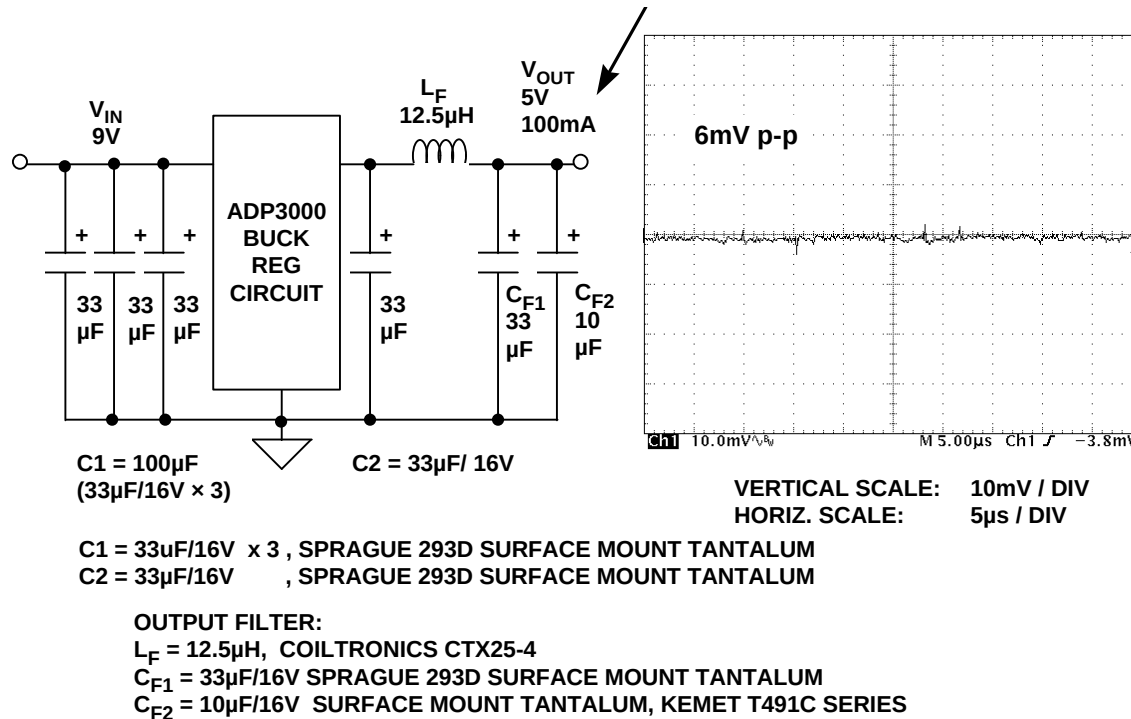


Figure 8.30

ADP1148 9V TO 3.3V/1A BUCK REGULATOR

The circuit for the ADP1148 9V to 3.3V/1A buck regulator is shown in Figure 8.31, and the input waveform in Figure 8.32. The input waveform is characteristic of the PWM buck regulator. The decaying portion of the waveform occurs when the inductor is connected to the input. The flat portion is when the input is disconnected from the inductor. The fundamental switching frequency is approximately 150kHz.

The output waveform of the ADP1148 buck regulator is shown in Figure 8.33. Note that the output filter capacitors consist of two leaded OS-CON types with very low ESR (approximately 0.02Ω each). This results in a low ripple of 6mV peak-to-peak, which is acceptable without further filtering.

ADP1148 BUCK REGULATOR APPLICATION

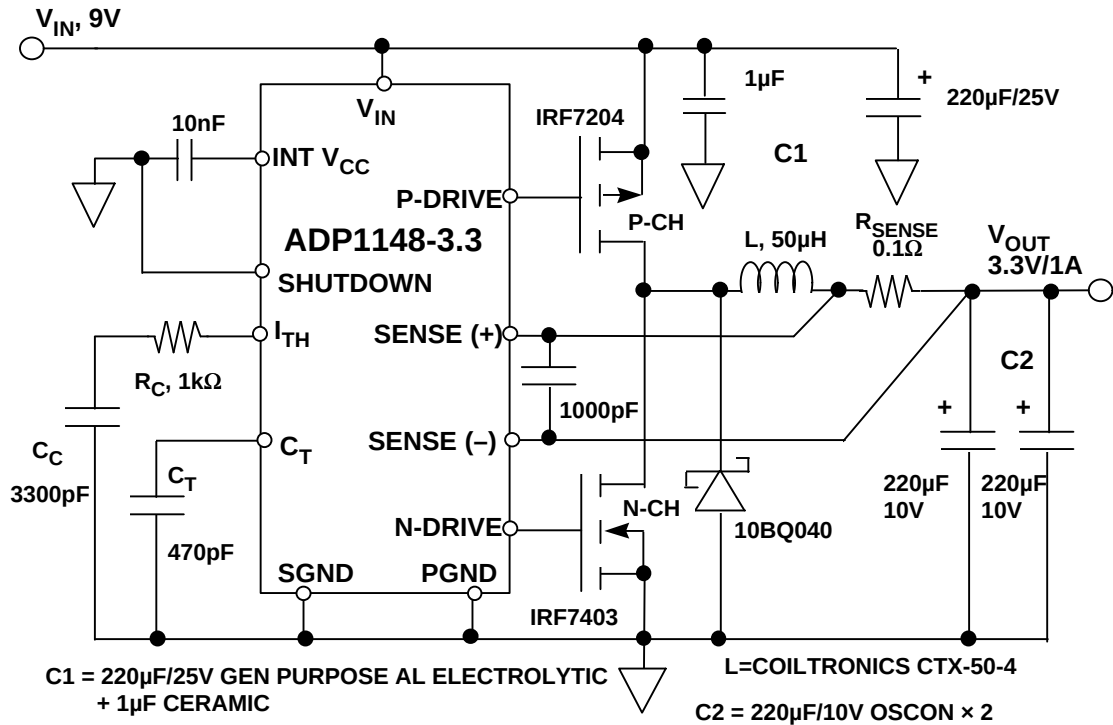


Figure 8.31

ADP1148 BUCK INPUT WAVEFORM - CONDITION 1

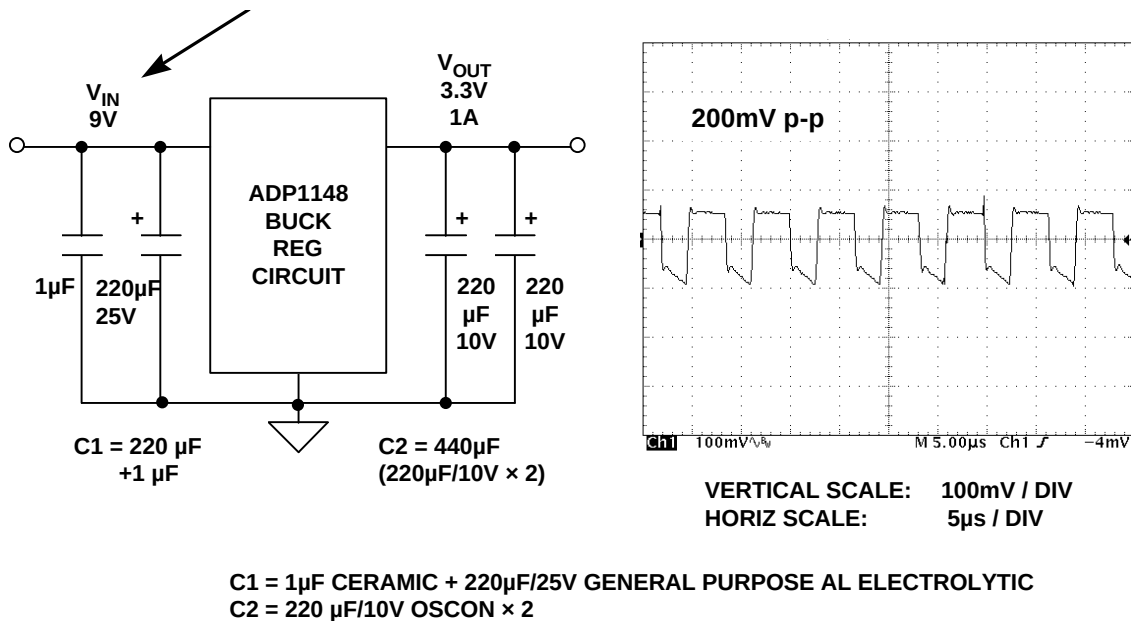


Figure 8.32

In order to evaluate the effects of an output filter, the ripple was increased by replacing the two OS-CON output capacitors with a single 100μF leaded tantalum. The resulting output ripple was increased to 40mV and is shown in Figure 3.34. Now, the effects of a filter could be evaluated. It consisted of a 50μH inductor followed by a 100μF leaded tantalum. Ripple was reduced from 40mV to 3mV as shown in Figure 3.35.

ADP1148 BUCK OUTPUT WAVEFORM - CONDITION 1

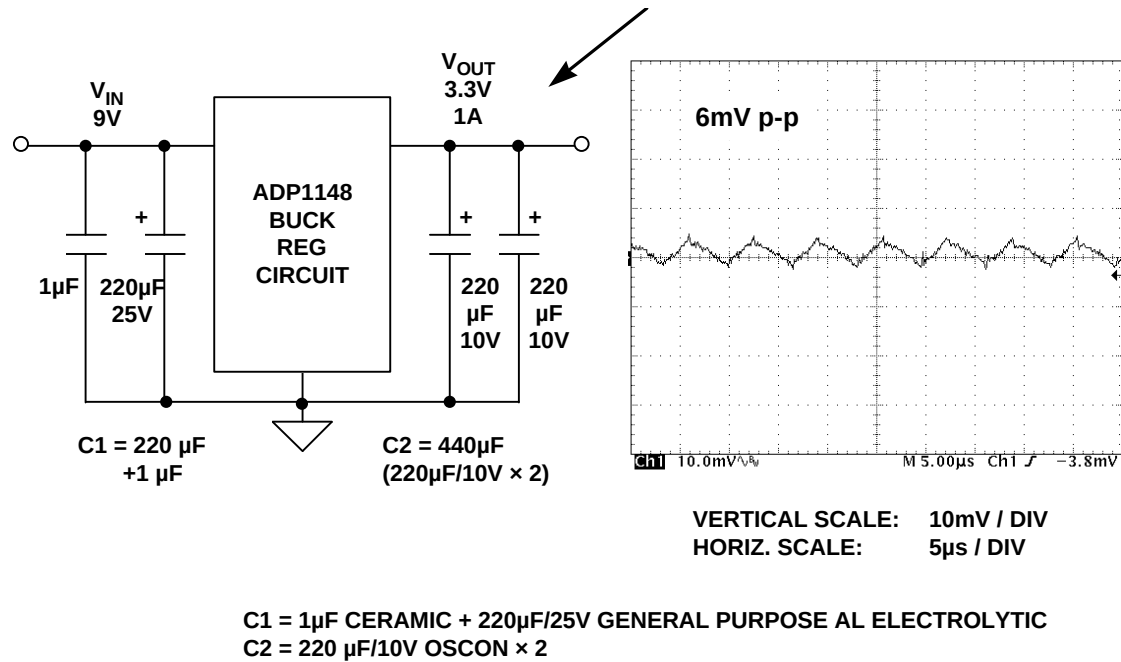


Figure 8.33

ADP1148 BUCK OUTPUT - CONDITION 2

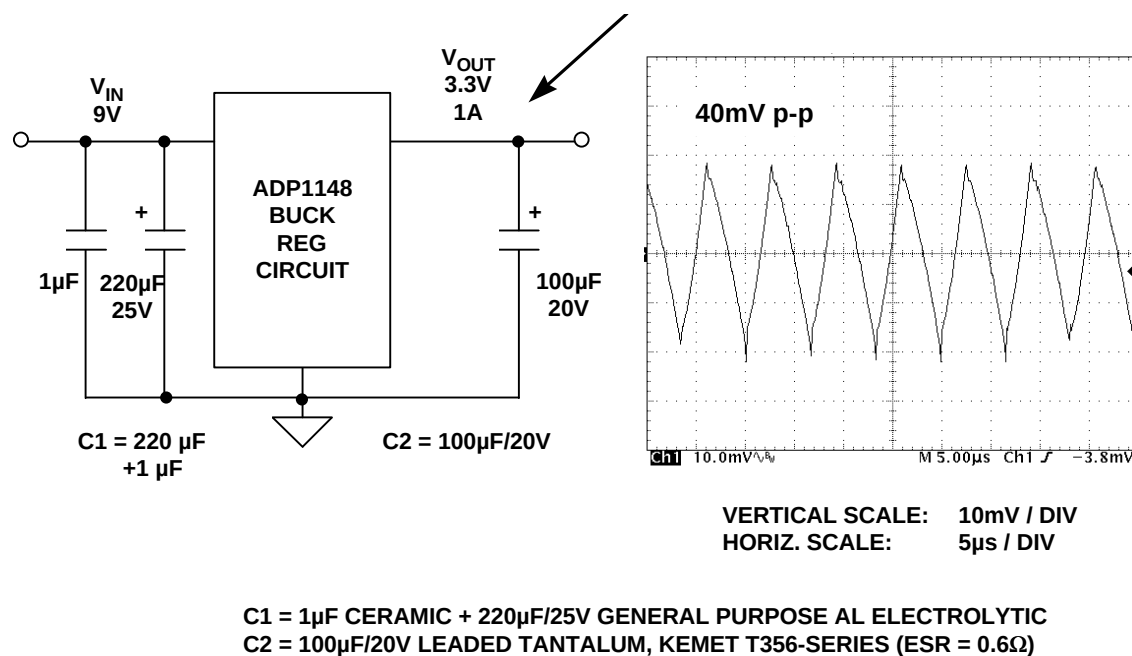


Figure 8.34

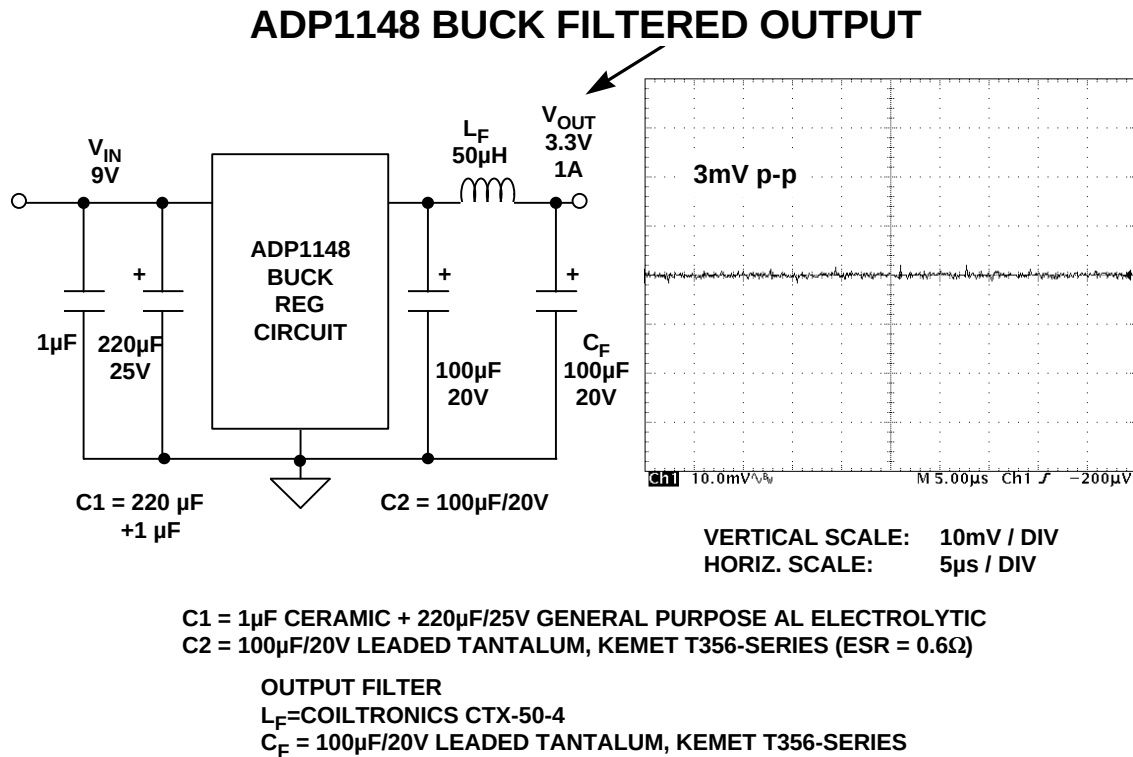


Figure 8.35

ADP1148 9V TO 3.75V BUCK REGULATOR FOLLOWED BY ADP3310 3.3V LINEAR LOW DROPOUT POST REGULATOR

Linear regulators are often used following switching regulators for better regulation and lower noise. Low dropout (LDO) regulators such as the ADP3310 are desirable in these applications because they require only a small input-to-output series voltage to maintain regulation. This minimizes power dissipation in the pass device and may eliminate the need for a heat sink. Figure 8.36 shows the ADP1148 buck regulator configured for a 9V input and a 3.75V/1A output. The output drives an ADP3310 linear LDO regulator configured for 3.75V input and 3.3V/1A output. The input and output of the ADP3310 is shown in Figure 8.37. Notice that the regulator reduces the ripple from 25mV to approximately 5mV.

ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

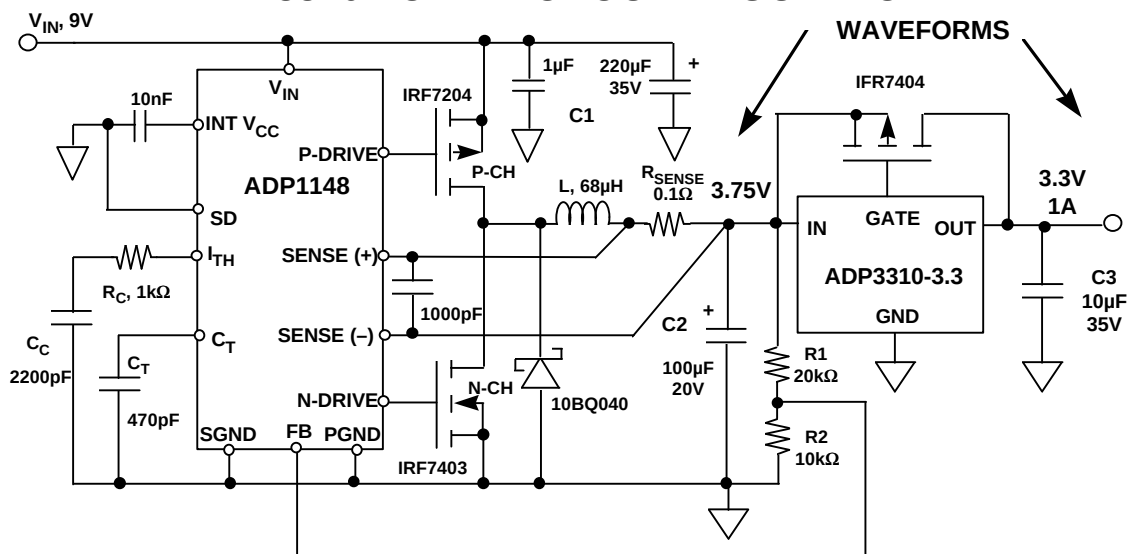


Figure 8.36

WAVEFORMS FOR ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

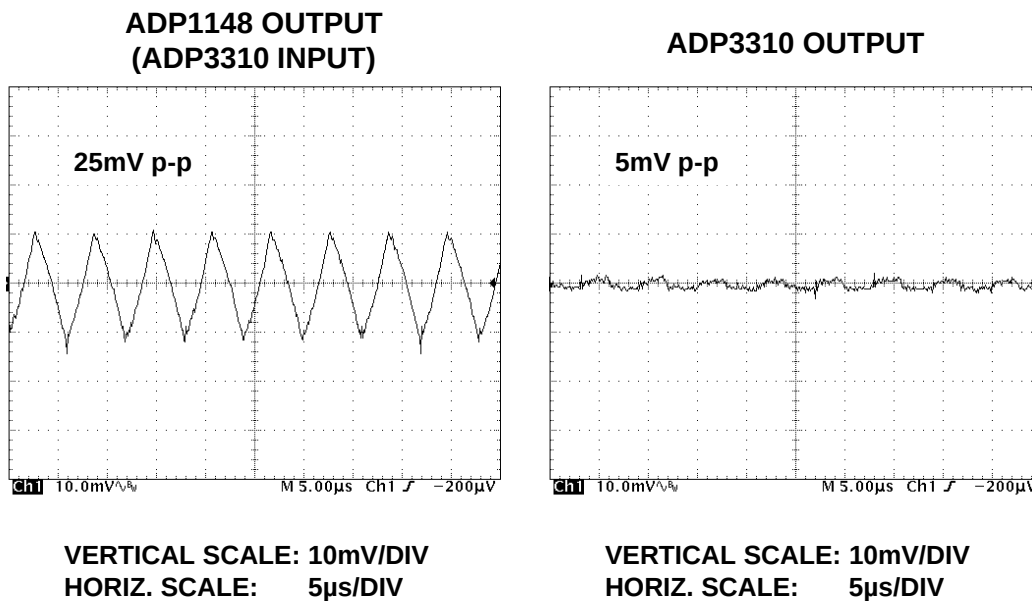


Figure 8.37

ADP3605 +5V to -3V/100mA Switched Capacitor Voltage Converter

Figure 8.38 shows the application circuit for the ADP3605 switched capacitor voltage converter. All three capacitors (input, output, and pump) are 10 μ F surface mount tantalum (Kemet T491C-series). Input and output waveforms are shown in Figure 8.39, where the output ripple is approximately 120mV peak-to-peak.

The addition of a 10 μ H/10 μ F output filter reduced the ripple to approximately 5mV as shown in Figure 8.40.

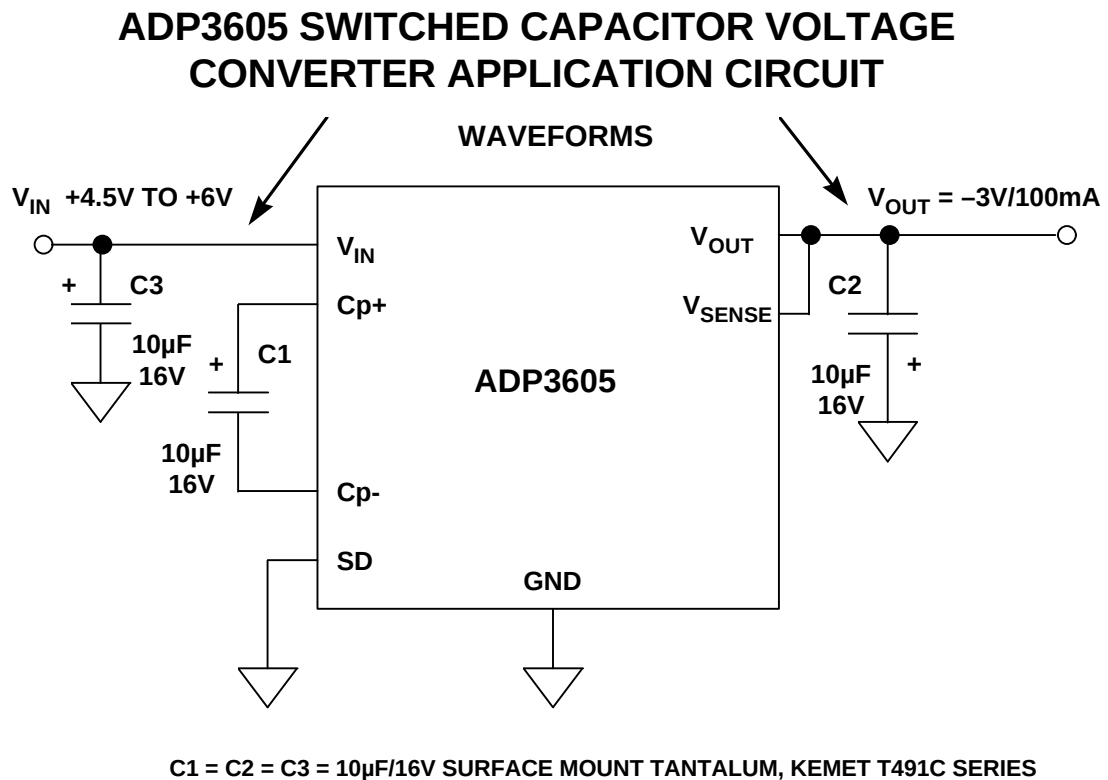


Figure 8.38

ADP3605 INPUT AND OUTPUT WAVEFORMS

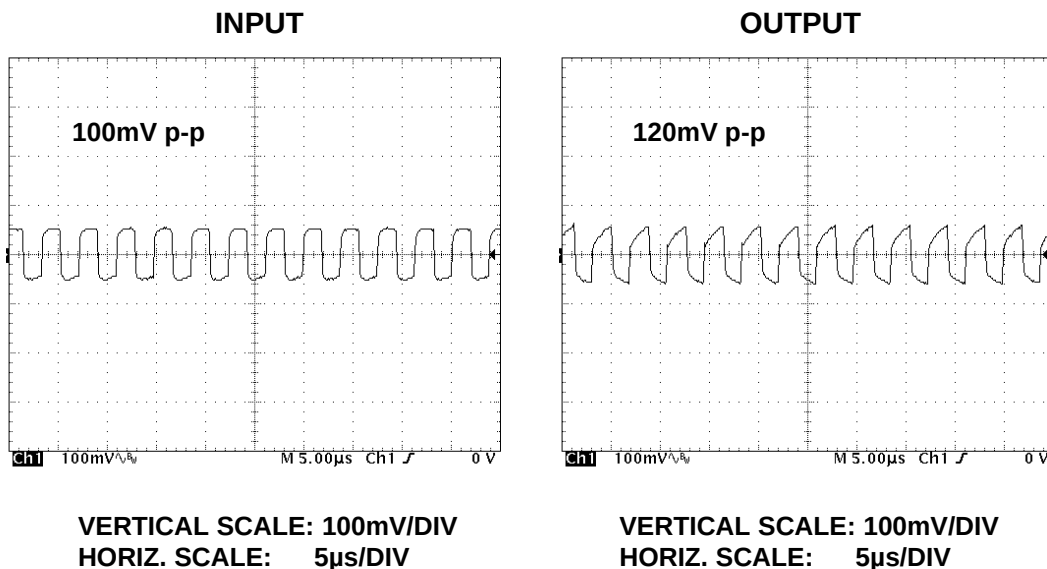


Figure 8.39

ADP3605 FILTERED OUTPUT

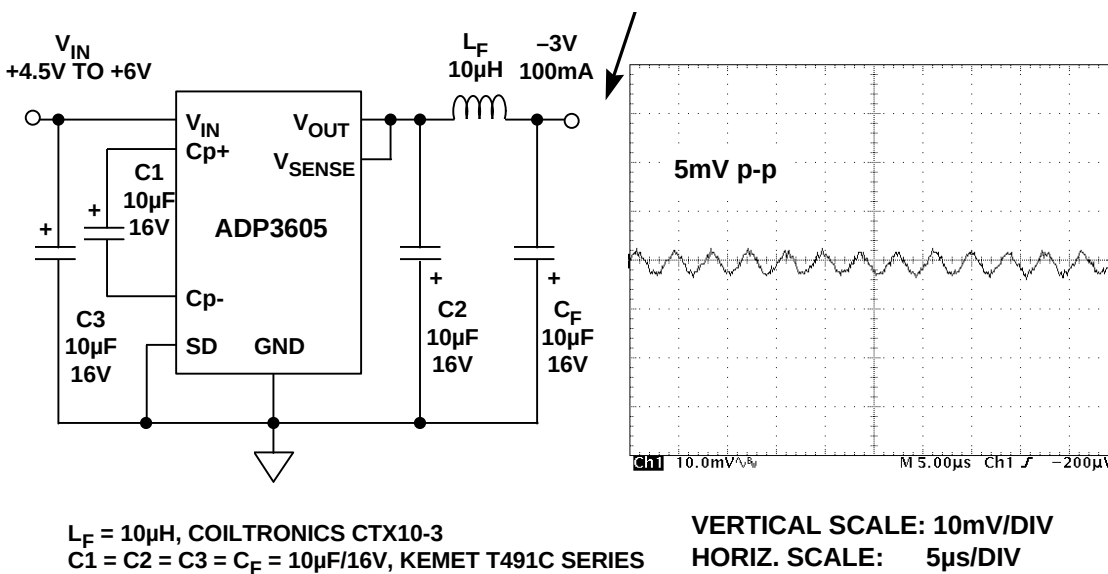


Figure 8.40

SUMMARY OF RESULTS OF EXPERIMENTS

The preceding experiments serve to illustrate the large number of tradeoffs which can be made when filtering switching regulator outputs. The success of any combination is highly dependent upon a compact layout and the use of a large area

ground plane. As has been stated earlier, all connections to the ground plane should be made as short as possible to minimize parasitic resistance and inductance.

Output ripple can be reduced by the addition of low ESL/ESR capacitors to the output. However, it may be more efficient to use an LC filter to accomplish the ripple reduction. In any case, proper component selection is critical. The inductor should not saturate under the maximum load current, and its DC resistance should be low enough as not to induce significant voltage drop. The capacitors should have low ESL and ESR and be rated to handle the required ripple current.

Low dropout linear post regulators provide both ripple reduction as well as better regulation and can be effective, provided the sacrifice in efficiency is not excessive.

Finally, it is difficult to predict the output ripple current analytically, and there is no substitute for a prototype using the real-world components. Once the filter is proven to provide the desired ripple attenuation (with some added safety margin), care must be taken that parts substitutions or vendor changes are not made in the final production units without first testing them in the circuit for equivalent performance.

SUMMARY OF RESULTS

- **Proper Layout and Grounding (using Ground Plane) Mandatory**
- **Low ESL/ESR Capacitors Give Best Results**
- **External LC Filters Very Effective in Reducing Ripple**
- **Linear Post Regulation Effective for Noise Reduction and Best Regulation**
- **Completely Analytical Approach Difficult, Prototyping is Required for Optimum Results**
- **Once Design is Finalized, Do Not Switch Vendors or Use Parts Substitutions Without First Verifying Their Performance in Circuit**
- **High Frequency Localized Decoupling at IC Power Pins is Still Required**

Figure 8.41

LOCALIZED HIGH FREQUENCY POWER SUPPLY FILTERING

The LC filters described in the previous section are useful in filtering switching regulator outputs. However, it may be desirable to place similar filters on the individual PC boards where the power first enters the board. Of course, if the switching regulator is placed on the PC board, then the LC filter should be an integral part of the regulator design.

Localized high frequency filters may also be required at each IC power pin (see Figure 8.42). This simple filter can be considered an option, one which is exercised

dependent upon the high frequency characteristics of the associated IC and the relative attenuation desired. It uses Z1, a leaded ferrite bead such as the Panasonic EXCELSA39, providing a resistance of more than 80Ω at 10MHz, increasing to over 100Ω at 100MHz. The ferrite bead is best used with a local high frequency decoupling cap right at the IC power pins, such as a $0.1\mu\text{F}$ ceramic unit shown.

HIGH FREQUENCY LOCALIZED DECOUPLING

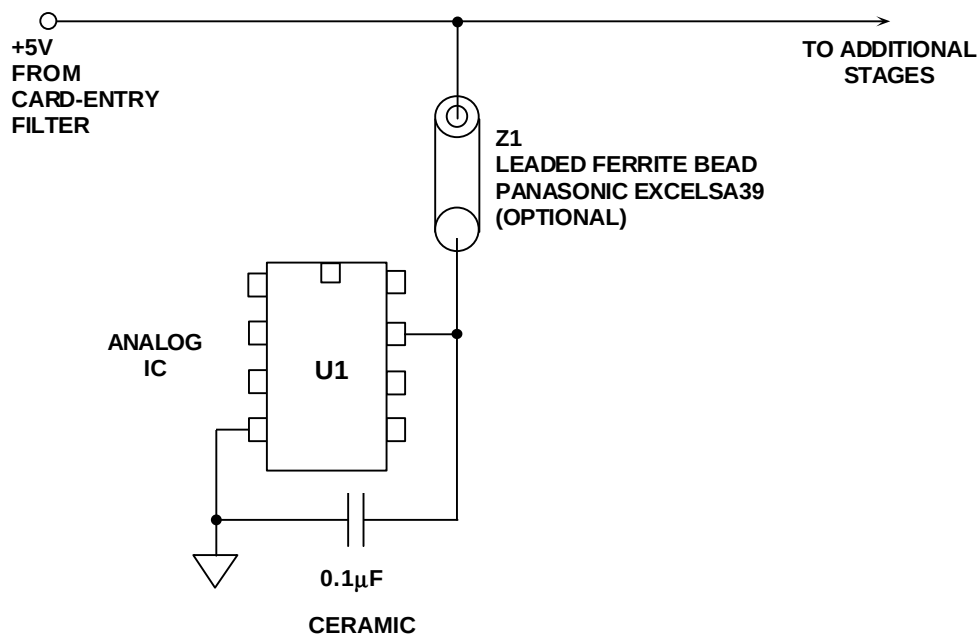


Figure 8.42

The following list summarizes the switching power supply filter layout/construction guidelines which will help ensure that the filter does the best possible job:

- (1) *Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits. This minimizes ESR, and maximizes filter performance. Pick chokes for low DL at the rated DC current, as well as low DCR.*
- (2) *Use short and wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.*
- (3) *Use short leads or better yet, leadless components, to minimize lead inductance. This minimizes the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred. Make all connections to the ground plane as short as possible.*
- (4) *Use a large-area ground plane for minimum impedance.*

(5) *Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the simulation. While simulation is not absolutely necessary, it does instill confidence in a design when correlation is achieved(see Reference 15).*

The discussion above assumes that the incoming AC power is relatively clean, an assumption not always valid. The AC power line can also be an EMI entry/exit path! To remove this noise path and reduce emissions caused by the switching power supply or other circuits, a *power line filter* is required.

It is important to remember that AC line power can potentially be lethal! Do not experiment without proper equipment and training! All components used in power line filters should be UL approved, and the best way to provide this is to specify a packaged UL approved filter. It should be installed in such a manner that it is the first thing the AC line sees upon entering the equipment. Standard three wire IEC style line cords are designed to mate with three terminal male connectors integral to many line filters. This is the best way to achieve this function, as it automatically grounds the third wire to the shell of the filter and equipment chassis via a low inductance path.

Commercial power line filters can be quite effective in reducing AC power-line noise. This noise generally has both common-mode and differential-mode components. Common-mode noise is noise that is found on any two of the three power connections (black, white, or green) with the same amplitude and polarity. In contrast, differential-mode noise is noise found only between two lines. By design, most commercially available filters address both noise modes (see Reference 16).

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THERMAL MANAGEMENT

Walt Jung, Walt Kester

For reliability reasons, modern semiconductor-based systems are increasingly called upon to observe some form of *thermal management*. All semiconductors have some specified safe upper limit for junction temperature (T_J), usually on the order of 150°C (but sometimes 175°). Like maximum power supply potentials, maximum junction temperature is a worst case limitation which shouldn't be exceeded. In conservative designs, it won't be approached by less than an ample safety margin. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. The cooler semiconductors can be kept during operation, the more closely they will approach maximum useful life.

Thermal basics

The general symbol θ is used for *thermal resistance*, that is:

θ = thermal resistance, in units of °C/watt (or, °C/W).

θ_{JA} and θ_{JC} are two more specific terms used in dealing with semiconductor thermal issues, which are explained below.

In general, a device with a thermal resistance θ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1W, as measured between two reference points. Note that this is a linear relation, so a 500mW dissipation in the same part will produce a 50°C differential, and so forth. For any power P (in watts), calculate the effective temperature differential (ΔT) in °C as:

$$\Delta T = P \times \theta,$$

where θ is the total applicable thermal resistance. Figure 8.43 summarizes these thermal relationships.

As the relationships signify, to maintain a low T_J , either θ or the power dissipated (or both) must be kept low. A low ΔT is the key to extending semiconductor lifetimes, as it leads to low maximum junction temperatures.

In semiconductors, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either the case of the device, or the *ambient temperature*, T_A , that of the surrounding air. This then leads in turn to the above mentioned individual thermal resistances, θ_{JA} and θ_{JC} .

THERMAL DESIGN BASICS

- θ = Thermal Resistance ($^{\circ}\text{C}/\text{W}$)
- $\Delta T = P \times \theta$
- θ_{JA} = Junction - to - Ambient Thermal Resistance
- θ_{JC} = Junction - to - Case Thermal Resistance
- θ_{CA} = Case - to - Ambient Thermal Resistance
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $T_J = T_A + (P \times \theta_{JA})$, P = Total Device Power
Dissipation
- $T_{J(\text{Max})} = 150^{\circ}\text{C}$ (Sometimes 175°C)

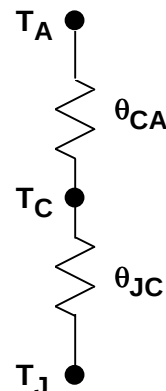


Figure 8.43

Taking the more simple case first, θ_{JA} is the thermal resistance of a given device measured between its *junction* and the *ambient* air. This thermal resistance is most often used with small, relatively low power ICs which do not dissipate serious amounts of power, that is 1W or less. θ_{JA} figures typical of op amps and other small devices are on the order of 90-100 $^{\circ}\text{C}/\text{W}$ for a plastic 8 pin DIP package. It must be understood that thermal resistances are highly package dependent, as different materials have differing degrees of thermal conductivity. As a general rule of thumb, thermal resistance for the conductors within packaging materials is closely analogous to electrical resistances, that is copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance (lowest θ).

A summary of the thermal resistances of various IC packages is shown in Figures 8.44, 8.45, and 8.46. In general, most of these packages do not lend themselves to easy heat sink attachment (with notable exceptions, such as the older round metal can types or the TO-220 package). Devices which *are* amenable to heat sink attachment will often be noted by a θ_{JC} dramatically lower than the θ_{JA} . See for example the 15 pin SIP package (used by the AD815), the TO-220 package, and the TO-263 package.

STANDARD PACKAGE THERMAL RESISTANCES - 1

Package	ADI Designation	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Comment
3 pin SOT-23	SOT-23-3	300	180	ADT45/ADT50
5 pin SOT-23	SOT-23-5	190		ADT05
6 pin SOT-23	SOT-23-6	165	92	ADP3300
8 pin plastic DIP	N-8	90		AD823
8 pin ceramic DIP	D-8	110	22	AD712
8 pin SOIC	R-8	160	60	
8 pin SOIC	R-8	90	60	ADP3367 Thermal Coastline
8 pin metal can	H-08A (TO-99)	150	45	OP07
10 pin metal can	H-10A (TO-100)	150	25	AD582
12 pin metal can	H-12A (TO-8)	100	30	AD841

Figure 8.44

STANDARD PACKAGE THERMAL RESISTANCES - 2

Package	ADI Designation	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Comment
14 pin plastic DIP	N-14	150		AD713
14 pin ceramic DIP	D-14	110	30	AD585
14 pin SOIC	R-14	120		AD813
15 pin SIP	Y-15	41	2	AD815 Through-Hole
16 pin plastic DIP	N-16	120	40	
16 pin ceramic DIP	D-16	95	22	AD524
16 pin SOIC	R-16	85		AD811
18 pin ceramic DIP	D-18	120	35	AD7575

Figure 8.45

STANDARD PACKAGE THERMAL RESISTANCES - 3

Package	ADI Designation	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Comment
20 pin plastic DIP	N-20	102	31	
20 pin ceramic DIP	D-20	70	10	
20 pin SOIC	R-20	74	24	
24 pin plastic DIP	N-24	105	35	
24 pin ceramic DIP	D-24	120	35	AD7547
28 pin plastic DIP	N-28	74	24	
28 pin ceramic DIP	D-28	51	8	
28 pin SOIC	R-28	71	23	
TO-220		53	3	Through-Hole
TO-263 (D2PAK)		73	3	Surface Mount

Figure 8.46

θ_{JC} is the thermal resistance of a given device as measured between its *junction* and the device *case*. This form is most often used with larger power semiconductors which do dissipate significant amounts of power, that is typically more than 1W. The reason for this is that a *heat sink* generally must be used with such devices, to maintain a sufficiently low internal junction temperature. A heat sink is simply an additional low thermal resistance device attached externally to a semiconductor part to aid in heat removal. It will have some additional thermal resistance of its own, also rated in °C/W.

Rather than just a single number, θ in this case will be composed of more than one component, i.e., θ_1 , θ_2 , etc. Like series resistors, thermal impedances add, making a net calculation relatively simple. For example, to compute a net θ_{JA} given a relevant θ_{JC} , the thermal resistance of the heat sink, θ_{CA} , or *case to ambient* is added to the θ_{JC} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA},$$

and the result is the θ_{JA} for that specific circumstance.

A real example illustrating these relationships is shown by Figure 8.47. These curves indicate the maximum power dissipation vs. temperature characteristic for a device using standard 8-pin SOIC and a thermal coastline 8-pin SOIC. Expressed in this fashion, the curves are often referred to as *derating* curves. The proprietary Analog Devices' thermal coastline package allows additional power to be dissipated with no increase in package size. For a $T_{J(max)}$ of 150°C, the upper curve shows the allowable power in a thermal coastline package. This corresponds to a θ which can be calculated by dividing the ΔT by P at any point. For example, 1W of power is

allowed at a T_A of 60°C , so the ΔT is $150^\circ\text{C} - 60^\circ\text{C} = 90^\circ\text{C}$. Dividing by 1W gives the thermal coastline package's θ of 90°C/W . Similarly, the standard 8-pin SOIC package yields 160°C/W . Given such data as these derating curves, the θ_{JA} for a given device can be readily determined, as above.

MAXIMUM POWER DISSIPATION VS. TEMPERATURE FOR STANDARD AND THERMAL COASTLINE 8-PIN SOICs

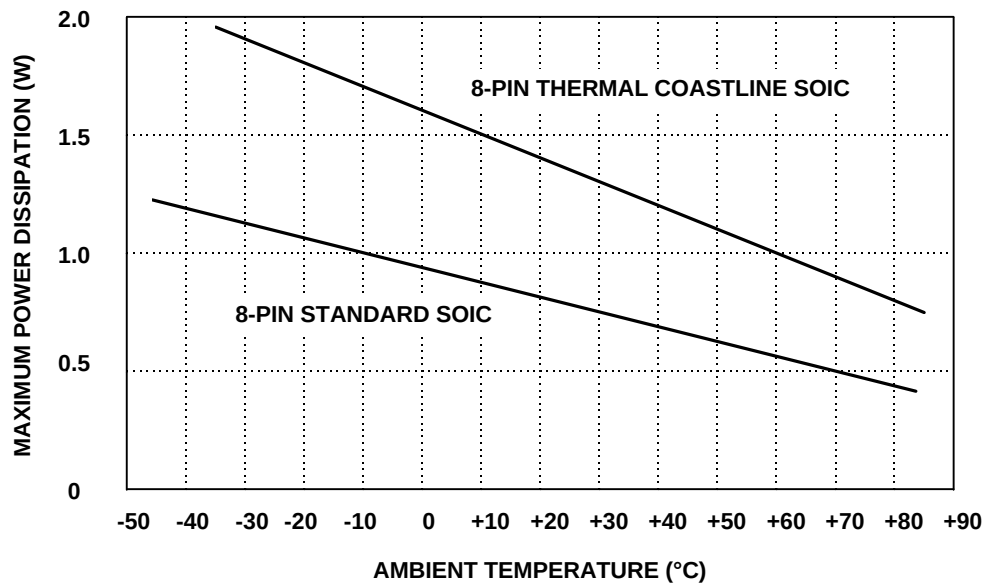


Figure 8.47

A physical comparison of the standard 8-pin SOIC leadframe and the Analog Devices' thermal coastline leadframe is shown in Figure 8.48 and 8.49. Note that the geometry of the thermal coastline leadframe increases the amount of heat transferred to the pins by decreasing the face-to-face distance between the leadframe and the paddle as well as increasing the width of the adjoining faces.

THERMAL COASTLINE PACKAGE

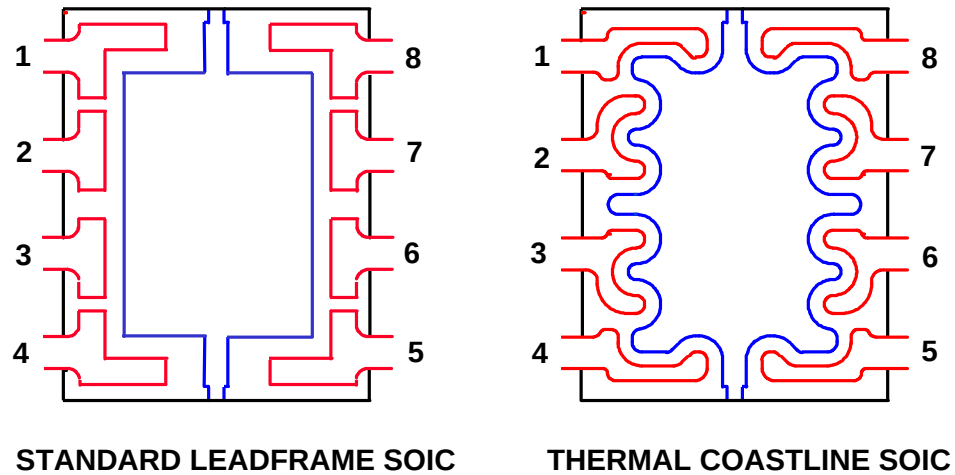


Figure 8.48

DETAILS OF THERMAL COASTLINE PACKAGE

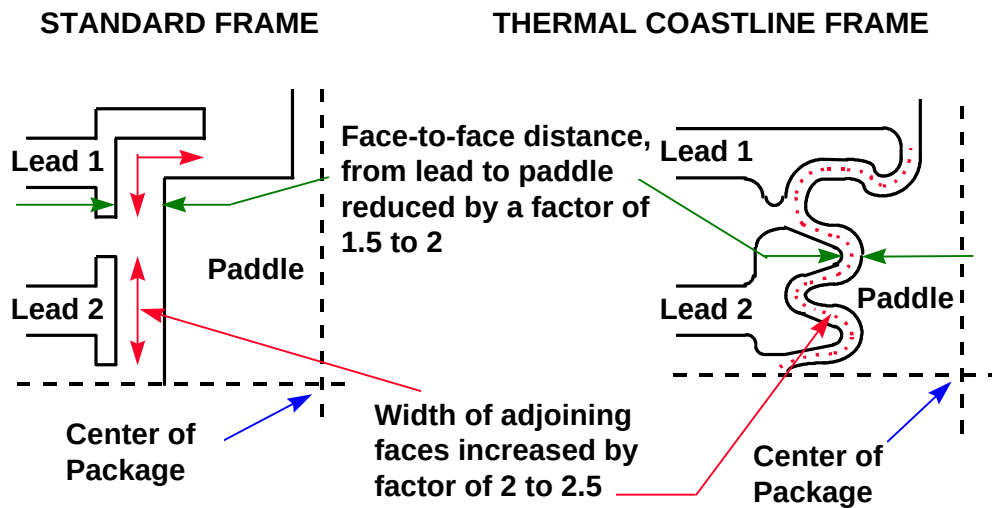


Figure 8.49

Heat Sink and Airflow Considerations

The fundamental purpose of heat sinks and airflow is to allow high power dissipation levels while maintaining safe junction temperatures. There are many tradeoffs which can be made between airflow and heat sink area, and this section examines some of them.

A thermal model of an IC and a heat sink is shown in Figure 8.50. The critical parameter is the junction temperature, T_J , which must be kept below 150°C for most ICs. The model shows the various thermal resistances and temperatures at various parts of the system. T_A is the ambient temperature, T_S is the heat sink temperature, T_C is the IC case temperature, and T_J is the junction temperature. The heat sink is usually attached to the IC in such a manner as to minimize the difference between the IC case temperature and the heat sink temperature. This is accomplished by a variety of means, including thermal grease, machined surface contact area, etc. In any case, the thermal resistance between the heat sink and the IC case can usually be made less than 1°C/W.

HEAT SINK BASICS

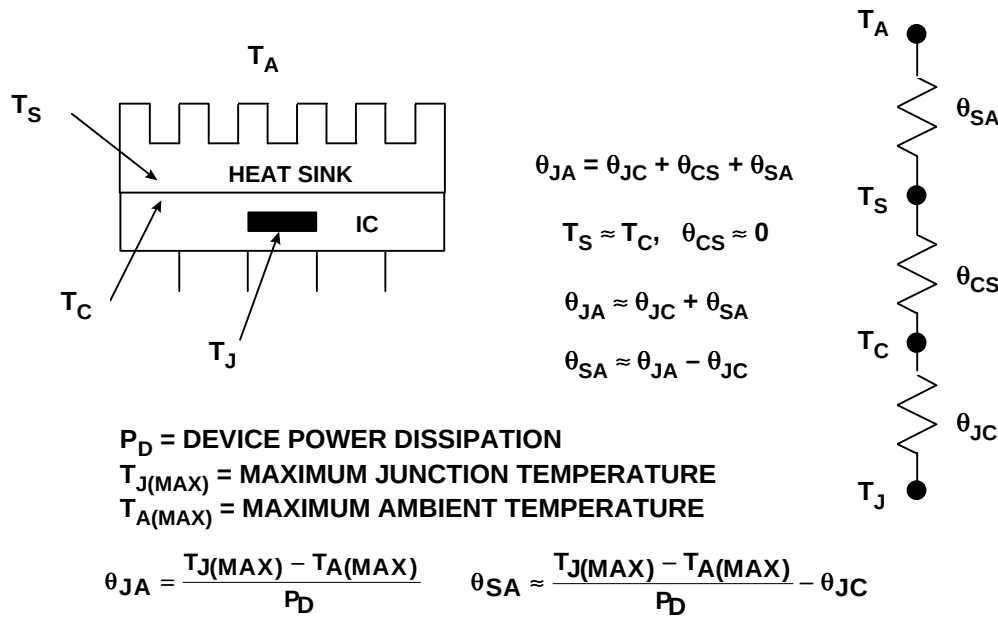


Figure 8.50

The junction-to-ambient thermal resistance, θ_{JA} , is therefore the sum of the three thermal resistance terms:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA},$$

where θ_{JC} is the junction-to-case thermal resistance, θ_{CS} the case-to-heat sink thermal resistance, and θ_{SA} the heat sink-to-ambient thermal resistance. Each term is multiplied by the device power dissipation, P_D , to determine the temperature rise associated with each thermal resistance:

$$T_J = P_D(\theta_{JA}) = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA}).$$

HARDWARE DESIGN TECHNIQUES

In most situations the maximum junction temperature, $T_{J(MAX)}$, maximum ambient temperature, $T_{A(MAX)}$, and P_D are known quantities, and it is desired to calculate the required heat sink thermal resistance, θ_{SA} , which will limit the junction temperature to $T_{J(MAX)}$ under the specified conditions. We know that the junction-to-ambient thermal resistance, θ_{JA} , can be expressed in terms of $T_{J(MAX)}$, $T_{A(MAX)}$, and P_D as follows:

$$\theta_{JA} = \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D}.$$

We also know that θ_{SA} can be expressed in terms of θ_{JA} , θ_{CS} , and θ_{JC} :

$$\theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS} = \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} - \theta_{JC} - \theta_{CS}.$$

In most cases, θ_{CS} can be less than 1°C/W with the use of thermal grease, and the expression for the maximum allowable heat sink-to-ambient resistance reduces to:

$$\theta_{SA} \approx \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} - \theta_{JC}.$$

A design example will help clarify the process and identify the various tradeoffs. Consider the low dropout linear regulator circuit shown in Figure 8.51 based on the ADP3310.

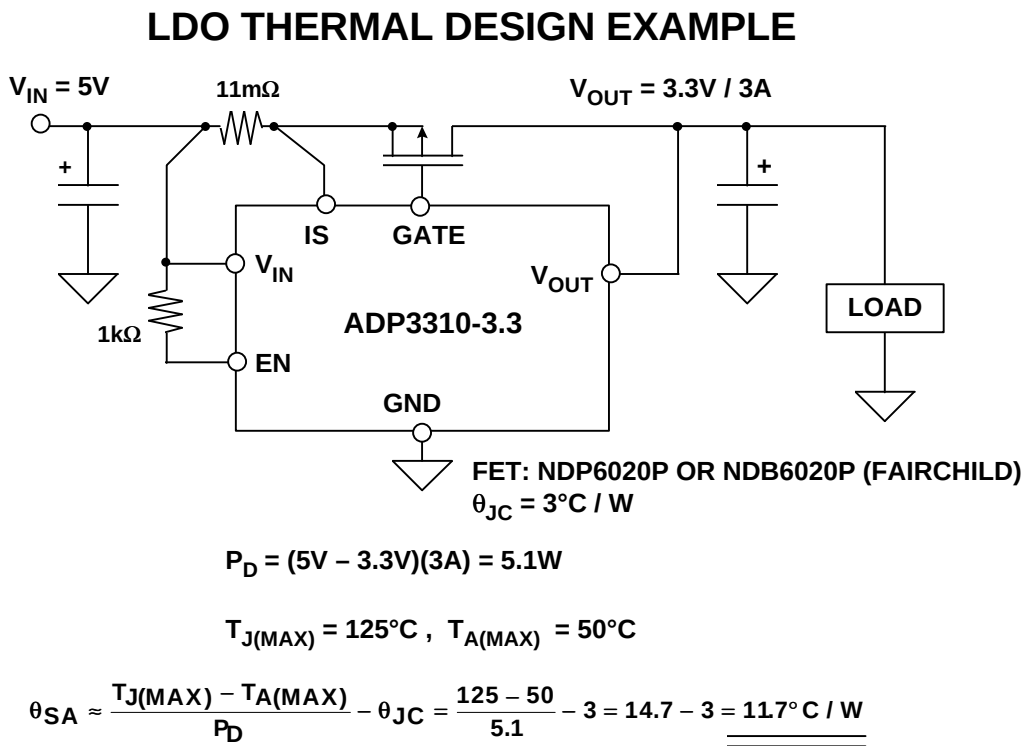


Figure 8.51

The power dissipated in the FET pass transistor (Fairchild NDP6020P or NDB6020P) due to the 1.7V drain-to-source voltage drop and the 3A output current is 5.1W. Now assume that we want to hold the maximum transistor junction temperature to $T_{J(MAX)} = 125^{\circ}\text{C}$ at an ambient temperature of $T_{A(MAX)} = 50^{\circ}\text{C}$. The junction-to-case thermal resistance of the FET is specified by the manufacturer to be 3°C/W . We can now calculate the maximum allowable heat sink case-to-ambient thermal resistance (neglecting θ_{CS} , the case-to-heat sink thermal resistance):

$$\theta_{SA} < \frac{T_{J(MAX)} - T_{A(MAX)}}{P_D} - \theta_{JC} = \frac{125 - 50}{5.1} - 3 = 14.7 - 3 = 11.7^{\circ}\text{C/W}.$$

The 6020P Fairchild FET is available in two packages as shown in Figure 8.52. The TO-220 style has a junction-to-ambient thermal resistance of 53°C/W (no airflow) and has a metal tab which is designed to be bolted to a heat sink. The TO-263 style has a junction-to-ambient thermal resistance of 73°C/W (no airflow) and is designed for surface mounting. The metal drain tab of the surface mount package is designed to be soldered directly to the PC board pad which acts as a heat sink.

TO-220 AND TO-263 (D²PAK) PACKAGES FOR FAIRCHILD NDP6020P/NDB6020P FETs

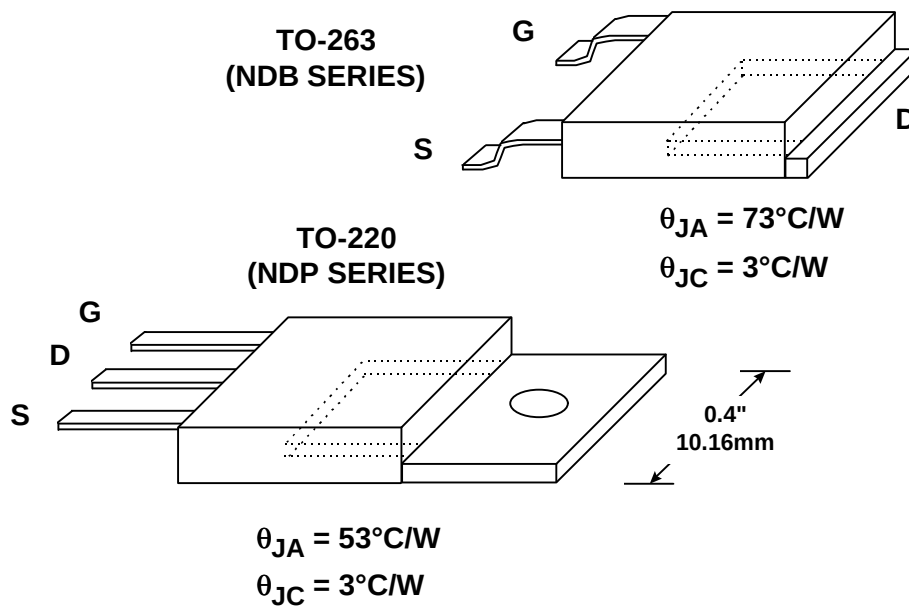


Figure 8.52

We will first select a suitable heat sink for the TO-220 package. Heat sink manufacturers such as AAVID Thermal Technologies have a variety of heat sinks suitable for a wide range of power dissipation levels. Selection tables provide nominal power dissipation, thermal resistance, and physical size for each heat sink available for a given package style.

A heat sink suitable for the TO-220 package is shown in Figure 8.53. It is a finned heat sink manufactured by AAVID Thermal Technologies (AAVID part number 582002B12500). The width of the heat sink is approximately 1.9". The entire assembly is bolted to the PC board, and the through-hole pins of the FET are then soldered to pads on the PC board.

The sink-to-ambient thermal resistance of this heat sink as a function of airflow is shown in Figure 8.54. Notice that even with no airflow, the thermal resistance is approximately 5°C/W, which is much less than the calculated maximum allowable value of 11.7°C/W. This heat sink will therefore provide more than adequate design margin under the specified operating conditions.

AAVID 582002B12500 HEAT SINK FOR TO-220

(Courtesy AAVID Thermal Technologies, Inc.)

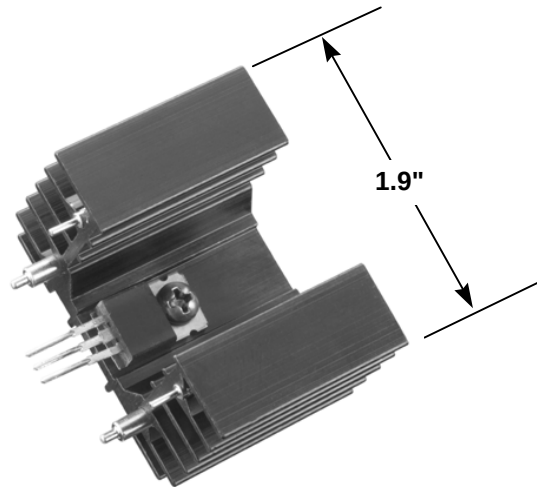
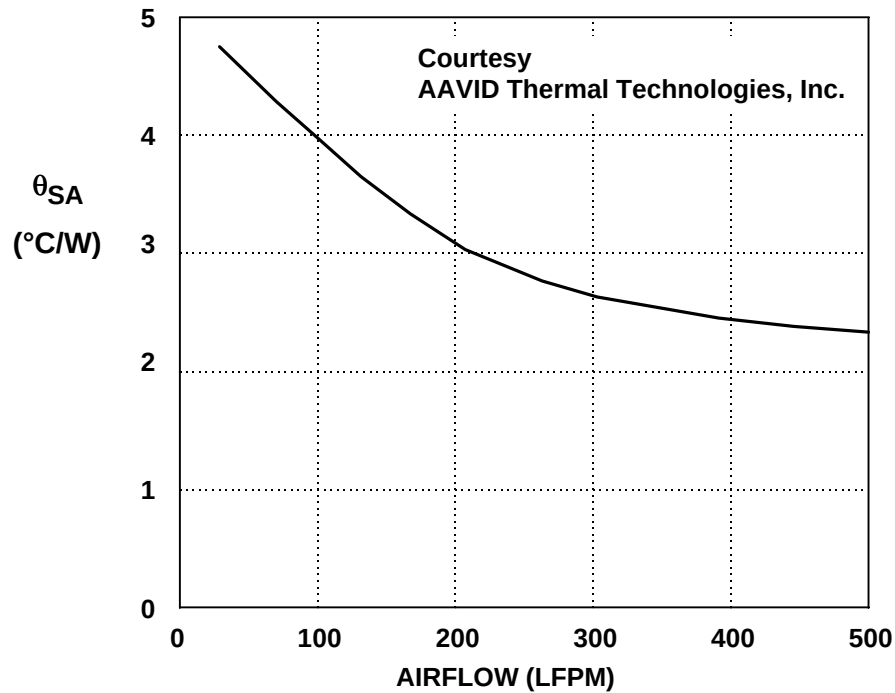


Figure 8.53

**THERMAL RESISTANCE VS. AIRFLOW FOR
AAVID 582002B12500 HEAT SINK****Figure 8.54**

Now consider the alternate package, the surface mount TO-263 package. Because the drain pad connection acts as a heat sink, the thermal resistance is a function of the drain pad area on the PC board. Figure 8.55 shows the thermal resistance of the package as a function of PC board drain pad area which is acting as the heat sink. Note that even with 2 square inches of pad area, the thermal resistance is still $30^{\circ}\text{C}/\text{W}$, which is well above the calculated maximum allowable value of $11.7^{\circ}\text{C}/\text{W}$.

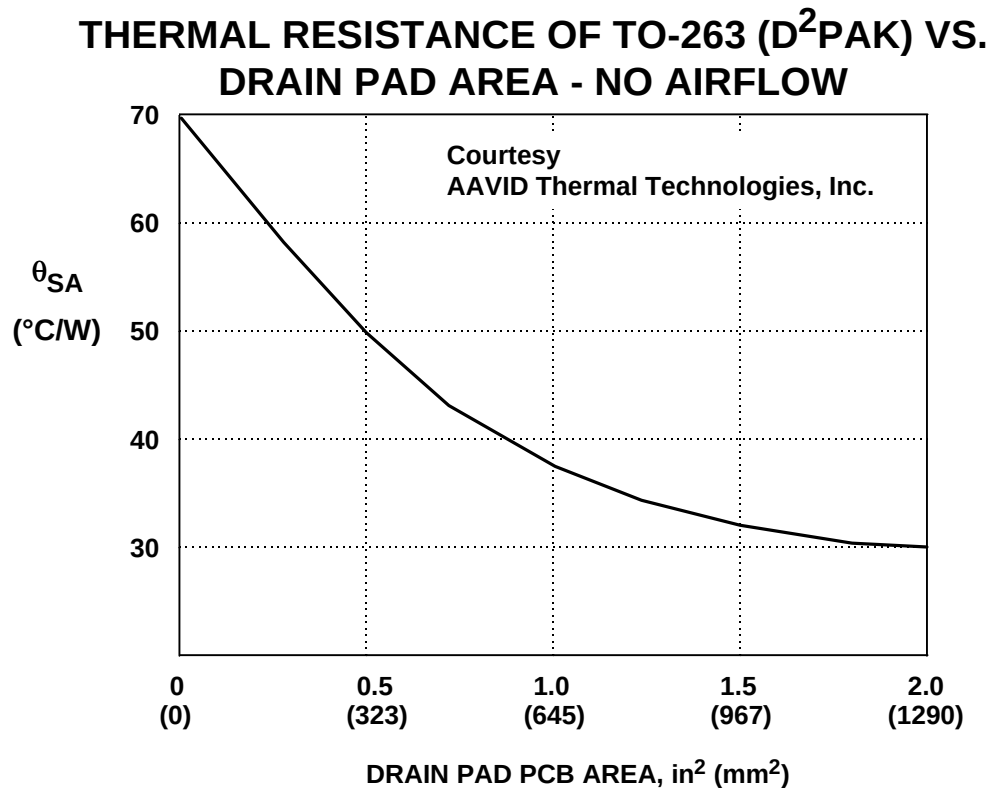


Figure 8.55

The situation can be improved by the addition of a surface-mount heat sink as shown in Figure 8.56 (AAVID part number 573300). This heat sink solders to two pads on the PC board which are extensions of the drain pad connecting area. The thermal resistance of this combination as a function of airflow is shown in Figure 8.57. Note that with the addition of the surface mount heat sink, the thermal resistance of the combination is reduced to approximately 10°C /W with a reasonable amount of airflow (200 linear feet per minute). The curve also shows the thermal resistance with no heat sink as a function of airflow, clearly indicating that a heat sink is required in order to meet the design requirements in a surface mount package.

AAVID 573300 HEAT SINK FOR TO-263 D²PAK

(Courtesy Aavid Thermal Technologies, Inc.)

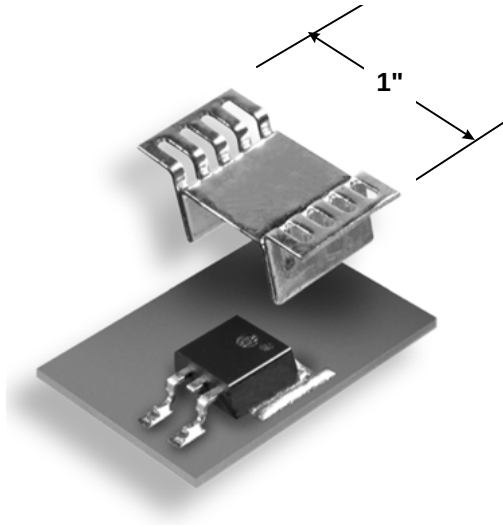


Figure 8.56

THERMAL RESISTANCE OF AAVID 573300 SURFACE MOUNT HEAT SINK VS. AIRFLOW

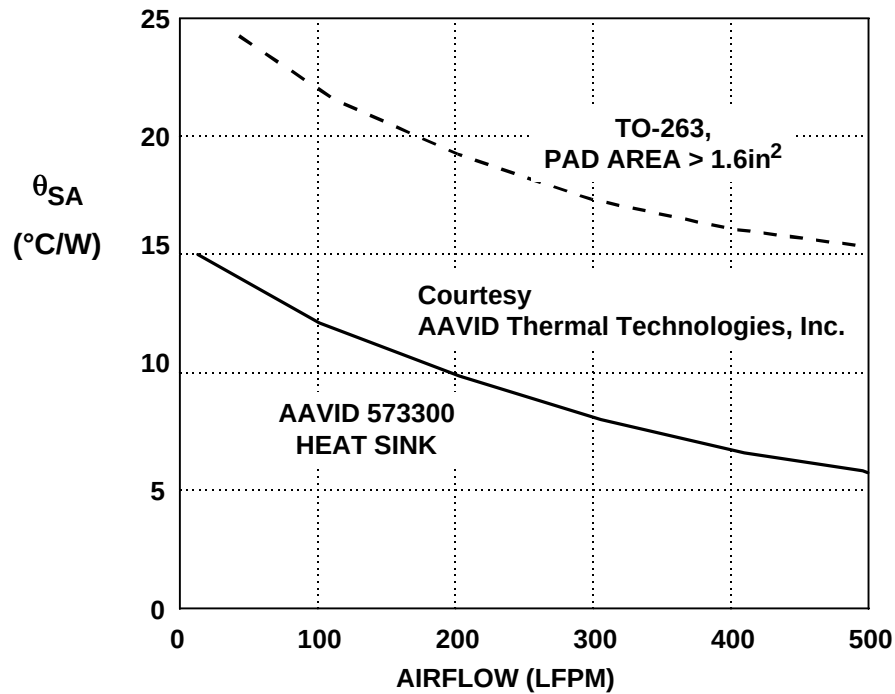


Figure 8.57

These examples illustrate the basic process of thermal design and heat sink selection. Larger heat sinks may lessen or even eliminate the need for airflow. However, when operating heat sinks with no air flow, the heatsink must be oriented such that thermal convection currents can carry the heat away from the heat sink. If additional airflow is required, the air must be allowed to pass freely around the heat sink with no obstruction. Note that small SOIC packages are also useful in conjunction with PCB copper heatsink areas (see References 6 and 7).

Further information on thermal management using heat sinks can be obtained from References 1-7.

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EMI/RFI CONSIDERATIONS

Electromagnetic interference (EMI) has become a hot topic in the last few years among circuit designers and systems engineers. Although the subject matter and prior art have been in existence for over the last 50 years or so, the advent of portable and high-frequency industrial and consumer electronics has provided a comfortable standard of living for many EMI testing engineers, consultants, and publishers. With the help of EDN Magazine and Kimmel Gerke Associates, this section will highlight general issues of EMC (electromagnetic compatibility) to familiarize the system/circuit designer with this subject and to illustrate proven techniques for protection against EMI.

A PRIMER ON EMI REGULATIONS

The intent of this section is to summarize the different types of electromagnetic compatibility (EMC) regulations imposed on equipment manufacturers, both voluntary and mandatory. Published EMC regulations apply at this time only to equipment and systems, and not to components. Thus, EMI *hardened* equipment does not necessarily imply that each of the components used (integrated circuits, especially) in the equipment must also be EMI *hardened*.

Commercial Equipment

The two driving forces behind commercial EMI regulations are the FCC (Federal Communications Commission) in the U. S. and the VDE (Verband Deutscher Elektrotechniker) in Germany. VDE regulations are more restrictive than the FCC's with regard to emissions and radiation, but the European Community will be adding immunity to RF, electrostatic discharge, and power-line disturbances to the VDE regulations, and now requires mandatory compliance. In Japan, commercial EMC regulations are covered under the VCCI (Voluntary Control Council for Interference) standards and, implied by the name, are much looser than their FCC and VDE counterparts.

All commercial EMI regulations primarily focus on *radiated* emissions, specifically to protect nearby radio and television receivers, although both FCC and VDE standards are less stringent with respect to *conducted* interference (by a factor of 10 over radiated levels). The FCC Part 15 and VDE 0871 regulations group commercial equipment into two classes: Class A, for all products intended for business environments; and Class B, for all products used in residential applications. For example, Figure 8.58 illustrates the electric-field emission limits of commercial computer equipment for both FCC Part 15 and VDE 0871 compliance.

RADIATED EMISSION LIMITS FOR COMMERCIAL COMPUTER EQUIPMENT

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Frequency (MHz)	Class A (at 3m)	Class B (at 3m)
30 - 88	300 $\mu\text{V/m}$	100 $\mu\text{V/m}$
88 - 216	500 $\mu\text{V/m}$	150 $\mu\text{V/m}$
216 - 1000	700 $\mu\text{V/m}$	200 $\mu\text{V/m}$

Figure 8.58

In addition to the already stringent VDE emission limits, the European Community EMC standards (IEC and IEEE) now requires mandatory compliance to these additional EMI threats: Immunity to RF fields, electrostatic discharge, and power-line disturbances. All equipment/systems marketed in Europe must exhibit an immunity to RF field strengths of 1-10V/m (IEC standard 801-3), electrostatic discharge (generated by human contact or through material movement) in the range of 10-15kV (IEC standard 801-2), and power-line disturbances of 4kV EFTs (extremely fast transients, IEC standard 801-4) and 6kV lightning surges (IEEE standard C62.41).

Military Equipment

The defining EMC specification for military equipment is MIL-STD-461 which applies to radiated equipment emissions and equipment susceptibility to interference. Radiated emission limits are very typically 10 to 100 times more stringent than the levels shown in Figure 8.58. Required limits on immunity to RF fields are typically 200 times more stringent (RF field strengths of 5-50mV/m) than the limits for commercial equipment.

Medical Equipment

Although not yet mandatory (as of December, 1997), EMC regulations for medical equipment are presently being defined by the FDA (Food and Drug Administration) in the USA and the European Community. The primary focus of these EMC regulations will be on immunity to RF fields, electrostatic discharge, and power-line disturbances, and may very well be more stringent than the limits spelled out in MIL-STD-461. The primary objective of the medical EMC regulations is to guarantee safety to humans.

Industrial- and Process-Control Equipment

Presently, equipment designed and marketed for industrial- and process-control applications are not required to meet pre-existing mandatory EMC regulations. In fact, manufacturers are exempt from complying to any standard in the USA. However, since industrial environments are very much electrically *hostile*, all equipment manufacturers are required to comply with all European Community EMC regulations as of 1996.

Automotive Equipment

Perhaps the most difficult and hostile environment in which electrical circuits and systems must operate is that found in the automobile. All of the key EMI threats to electrical systems exist here. In addition, operating temperature extremes, moisture, dirt, and toxic chemicals further exacerbate the problem. To complicate matters further, standard techniques (ferrite beads, feed-through capacitors, inductors, resistors, shielded cables, wires, and connectors) used in other systems are not generally used in automotive applications because of the cost of the additional components.

Presently, automotive EMC regulations, defined by the very comprehensive SAE Standards J551 and J1113, are not yet mandatory. They are, however, very rigorous. SAE standard J551 applies to vehicle-level EMC specifications, and standard J1113 (functionally similar to MIL-STD-461) applies to all automotive electronic modules. For example, the J1113 specification requires that electronic modules cannot radiate electric fields greater than 300nV/m at a distance of 3 meters. This is roughly 1000 times more stringent than the FCC Part 15 Class A specification. In many applications, automotive manufacturers are imposing J1113 RF field immunity limits on *each of the active components* used in these modules. Thus, in the very near future, automotive manufacturers will require that IC products comply with existing EMC standards and regulations.

EMC Regulations' Impact on Design

In all these applications and many more, complying with mandatory EMC regulations will require careful design of individual circuits, modules, and systems using established techniques for cable shielding, signal and power-line filtering against both small- and large-scale disturbances, and sound multi-layer PCB layouts. The key to success is to incorporate sound EMC principles early in the design phase to avoid time-consuming and expensive redesign efforts.

A DIAGNOSTIC FRAMEWORK FOR EMI/RFI PROBLEM SOLVING

With any problem, a strategy should be developed before any effort is expended trying to solve it. This approach is similar to the scientific method: initial circuit misbehavior is noted, theories are postulated, experiments designed to test the theories are conducted, and results are again noted. This process continues until all theories have been tested and expected results achieved and recorded. With respect to EMI, a problem solving framework has been developed. As shown in Figure 8.59, the model suggested by Kimmel-Gerke in [Reference 1] illustrates that all three elements (a *source*, a *receptor* or *victim*, and a *path* between the two) must exist in order to be considered an EMI problem. The sources of electromagnetic interference can take on many forms, and the ever-increasing number of portable instrumentation and personal communications/computation equipment only adds the number of possible sources and receptors.

A DIAGNOSTIC FRAMEWORK FOR EMI

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ANY INTERFERENCE PROBLEM CAN BE BROKEN DOWN INTO:

- The **SOURCE** of interference
- The **RECEPTOR** of interference
- The **PATH** coupling the source to the receptor

SOURCES	PATHS	RECEPTORS
Microcontroller ♦ Analog ♦ Digital	Radiated ♦ EM Fields ♦ Crosstalk Capacitive Inductive	Microcontroller ♦ Analog ♦ Digital Communications ♦ Receivers
ESD Communications Transmitters Power Disturbances Lightning	Conducted ♦ Signal ♦ Power ♦ Ground	Other Electronic Systems

Figure 8.59

Interfering signals reach the receptor by *conduction* (the circuit or system interconnections) or *radiation* (parasitic mutual inductance and/or parasitic capacitance). In general, if the frequencies of the interference are less than 30MHz, the primary means by which interference is coupled is through the *interconnects*. Between 30MHz and 300MHz, the primary coupling mechanism is *cable radiation and connector leakage*. At frequencies greater than 300MHz, the primary mechanism is *slot and board radiation*. There are many cases where the interference is broadband, and the coupling mechanisms are combinations of the above.

When all three elements exist together, a framework for solving any EMI problem can be drawn from Figure 8.60. There are three types of interference with which the circuit or system designer must contend. The first type of interference is that generated by and emitted from an instrument; this is known as circuit/system *emission* and can be either *conducted* or *radiated*. An example of this would be the personal computer. Portable and desktop computers must pass the stringent FCC Part 15 specifications prior to general use.

THREE TYPES OF INTERFERENCE EMISSIONS - IMMUNITY - INTERNAL

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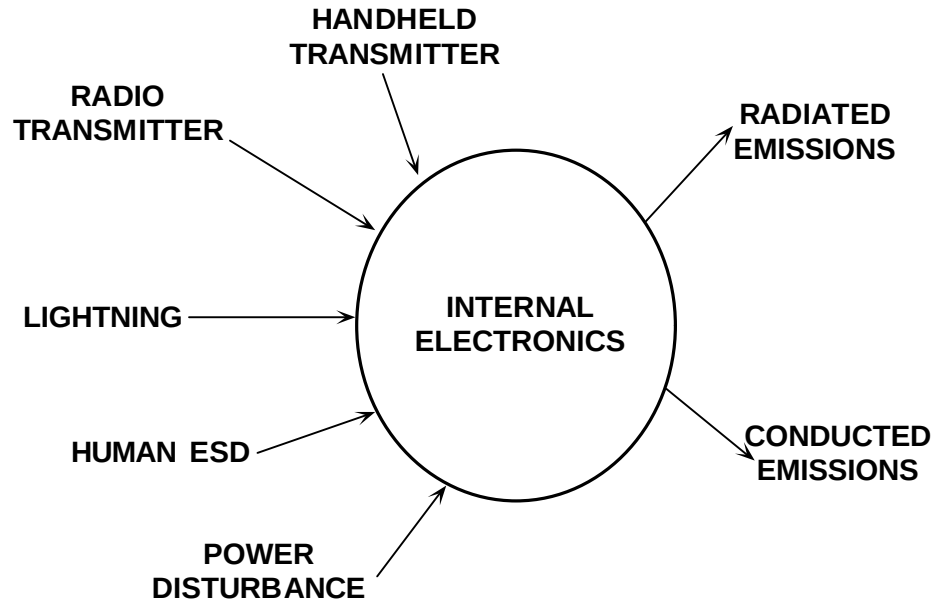


Figure 8.60

The second type of interference is circuit or system *immunity*. This describes the behavior of an instrument when it is exposed to large electromagnetic fields, primarily electric fields with an intensity in the range of 1 to 10V/m at a distance of 3 meters. Another term for immunity is *susceptibility*, and it describes circuit/system behavior against radiated or conducted interference.

The third type of interference is *internal*. Although not directly shown on the figure, internal interference can be high-speed digital circuitry within the equipment which affects sensitive analog (or other digital circuitry), or noisy power supplies which can contaminate both analog and digital circuits. Internal interference often occurs between digital and analog circuits, or between motors or relays and digital circuits. In mixed signal environments, the digital portion of the system often interferes with analog circuitry. In some systems, the internal interference reaches such high levels that even very high-speed digital circuitry can affect other low-speed digital circuitry as well as analog circuits.

In addition to the source-path-receptor model for analyzing EMI-related problems, Kimmel Gerke Associates have also introduced the FAT-ID concept [Reference 1]. FAT-ID is an acronym that describes the five key elements inherent in any EMI problem. These five key parameters are: *frequency, amplitude, time, impedance, and distance*.

The *frequency* of the offending signal suggests its path. For example, the path of low-frequency interference is often the circuit conductors. As the interference frequency increases, it will take the path of least impedance, usually stray capacitance. In this case, the coupling mechanism is radiation.

Time and frequency in EMI problems are interchangeable. In fact, the physics of EMI shows that the time response of signals contains all the necessary information to construct the spectral response of the interference. In digital systems, both the signal rise time and pulse repetition rate produce spectral components according to the following relationship:

$$f_{\text{EMI}} = \frac{1}{\pi \cdot t_{\text{rise}}} \quad \text{Eq. 8.1}$$

For example, a pulse having a 1ns rise time is equivalent to an EMI frequency of over 300MHz. This time-frequency relationship can also be applied to high-speed analog circuits, where slew rates in excess of 1000V/μs and gain-bandwidth products greater than 500MHz are not uncommon.

When this concept is applied to instruments and systems, EMI emissions are again functions of signal rise time and pulse repetition rates. Spectrum analyzers and high speed oscilloscopes used with voltage and current probes are very useful tools in quantifying the effects of EMI on circuits and systems.

Another important parameter in the analysis of EMI problems is the physical dimensions of cables, wires, and enclosures. Cables can behave as either passive antennas (receptors) or very efficient transmitters (sources) of interference. Their physical length and their shield must be carefully examined where EMI is a concern. As previously mentioned, the behavior of simple conductors is a function of length, cross-sectional area, and frequency. Openings in equipment enclosures can behave as slot antennas, thereby allowing EMI energy to affect the internal electronics.

PASSIVE COMPONENTS: YOUR ARSENAL AGAINST EMI

Minimizing the effects of EMI requires that the circuit/system designer be completely aware of the primary arsenal in the battle against interference: *passive components*. To use successfully these components, the designer must understand their non-ideal behavior. For example, Figure 8.61 illustrates the *real* behavior of the passive components used in circuit design. At very high frequencies, wires become transmission lines, capacitors become inductors, inductors become capacitors, and resistors behave as resonant circuits.

ALL PASSIVE COMPONENTS EXHIBIT "NON-IDEAL" BEHAVIOR

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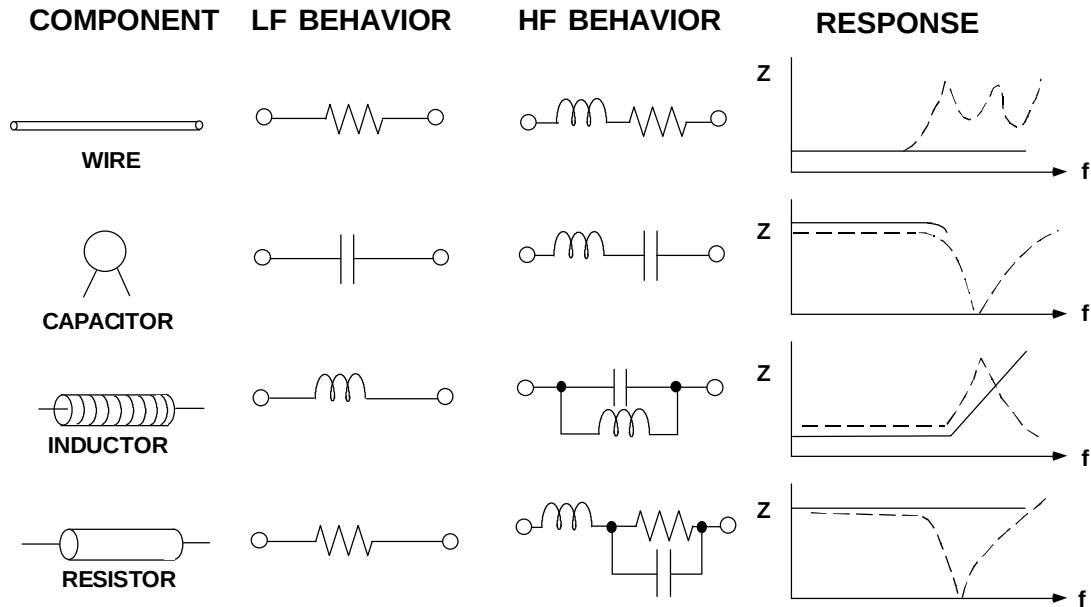


Figure 8.61

A specific case in point is the frequency response of a simple wire compared to that of a ground plane. In many circuits, wires are used as either power or signal returns, and there is no ground plane. A wire will behave as a very low resistance (less than $0.02\Omega/\text{ft}$ for 22-gauge wire) at low frequencies, but because of its parasitic inductance of approximately $20\text{nH}/\text{inch}$, it becomes inductive at frequencies above 13kHz . Furthermore, depending on size and routing of the wire and the frequencies involved, it ultimately becomes a transmission line with an uncontrolled impedance. From our knowledge of RF, unterminated transmission lines become antennas with gain. On the other hand, large area ground planes are much more well-behaved, and maintain a low impedance over a wide range of frequencies. With a good understanding of the behavior of *real* components, a strategy can now be developed to find solutions to most EMI problems.

RADIO FREQUENCY INTERFERENCE

The world is rich in radio transmitters: radio and TV stations, mobile radios, computers, electric motors, garage door openers, electric jackhammers, and countless others. All this electrical activity can affect circuit/system performance and, in extreme cases, may render it inoperable. Regardless of the location and magnitude of the interference, circuits/systems must have a minimum level of immunity to radio frequency interference (RFI). The next section will cover two general means by which RFI can disrupt normal instrument operation: the direct effects of RFI sensitive analog circuits, and the effects of RFI on shielded cables.

Two terms are typically used in describing the sensitivity of an electronic system to RF fields. In communications, radio engineers define *immunity* to be an instrument's *susceptibility to the applied RFI power density at the unit*. In more general EMI analysis, the *electric-field intensity* is used to describe RFI stimulus. For comparative purposes, Equation 8.2 can be used to convert electric-field intensity to power density and vice-versa:

$$\bar{E} \left(\frac{V}{m} \right) = 61.4 \sqrt{P_T \left(\frac{mW}{cm^2} \right)} \quad \text{Eq. 8.2}$$

where E = Electric Field Strength, in volts per meter, and
 P_T = Transmitted power, in milliwatts per cm^2 .

From the standpoint of the source-path-receptor model, the *strength of the electric field*, E, surrounding the receptor is a function of *transmitted power*, *antenna gain*, and *distance* from the source of the disturbance. An approximation for the electric-field intensity (for both near- and far-field sources) in these terms is given by Equation 8.3:

$$\bar{E} \left(\frac{V}{m} \right) = 5.5 \left(\frac{\sqrt{P_T \cdot G_A}}{d} \right) \quad \text{Eq. 8.3}$$

where E = Electric field intensity, in V/m;
 P_T = Transmitted power, in mW/cm²;
 G_A = Antenna gain (numerical); and
d = distance from source, in meters

For example, a 1W hand-held radio at a distance of 1 meter can generate an electric-field of 5.5V/m, whereas a 10kW radio transmission station located 1km away generates a field smaller than 0.6V/m.

Analog circuits are generally more sensitive to RF fields than digital circuits because analog circuits, operating at high gains, must be able to resolve signals in the microvolt/millivolt region. Digital circuits, on the other hand, are more immune to RF fields because of their larger signal swings and noise margins. As shown in Figure 8.62, RF fields can use inductive and/or capacitive coupling paths to generate noise currents and voltages which are amplified by high-impedance analog instrumentation. In many cases, out-of-band noise signals are detected and rectified by these circuits. The result of the RFI rectification is usually unexplained offset voltage shifts in the circuit or in the system.

RFI CAN CAUSE RECTIFICATION IN SENSITIVE ANALOG CIRCUITS

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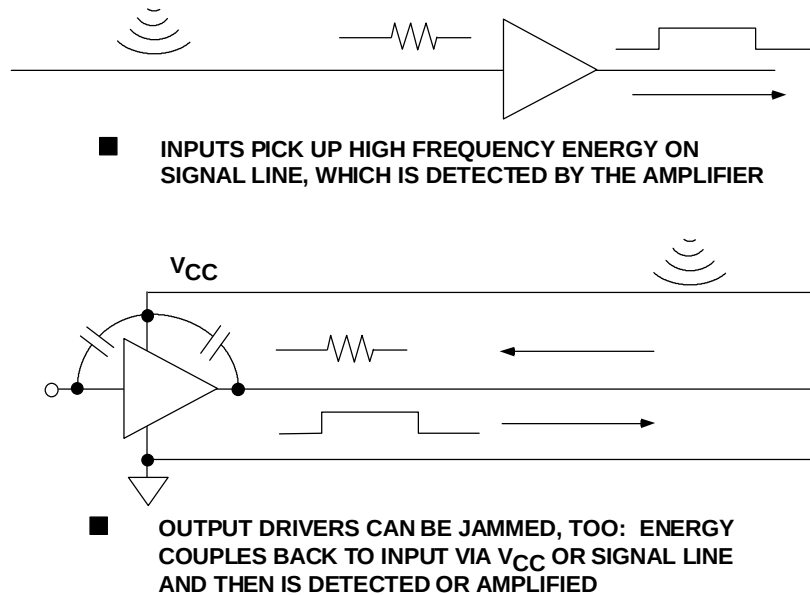


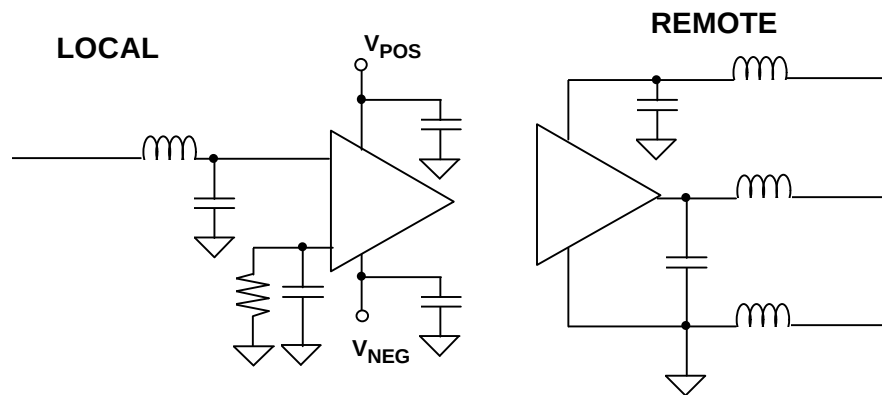
Figure 8.62

There are techniques that can be used to protect analog circuits against interference from RF fields (see Figure 8.63). The three general points of RFI coupling are *signal inputs*, *signal outputs*, and *power supplies*. At a minimum, all power supply pin connections on analog and digital ICs should be decoupled with 0.1 μ F ceramic capacitors. As was shown in Reference 3, low-pass filters, whose cutoff frequencies are set no higher than 10 to 100 times the signal bandwidth, can be used at the inputs and the outputs of signal conditioning circuitry to filter noise.

Care must be taken to ensure that the low pass filters (LPFs) are effective at the highest RF interference frequency expected. As illustrated in Figure 8.64, real low-pass filters may exhibit *leakage* at high frequencies. Their inductors can lose their effectiveness due to parasitic capacitance, and capacitors can lose their effectiveness due to parasitic inductance. A rule of thumb is that a conventional low-pass filter (made up of a single capacitor and inductor) can begin to *leak* when the applied signal frequency is 100 to 1000 higher than the filter's cutoff frequency. For example, a 10kHz LPF would not be considered very efficient at filtering frequencies above 1MHz.

KEEPING RFI AWAY FROM ANALOG CIRCUITS

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- Decouple all voltage supplies to analog chip with high-frequency capacitors
- Use high-frequency filters on all lines that leave the board
- Use high-frequency filters on the voltage reference if it is not grounded

Figure 8.63

A SINGLE LOW PASS FILTER LOSES EFFECTIVENESS AT 100 - 1000 f_{3dB}

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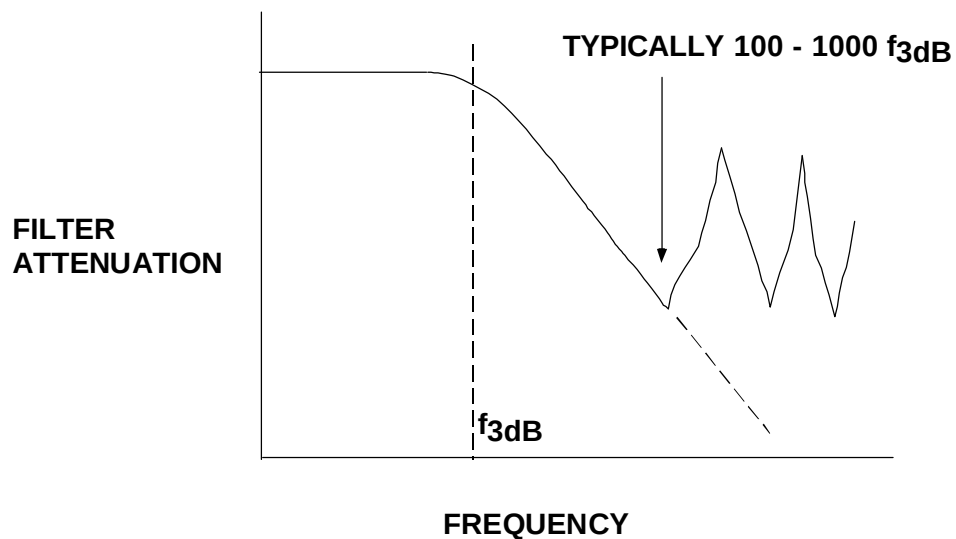
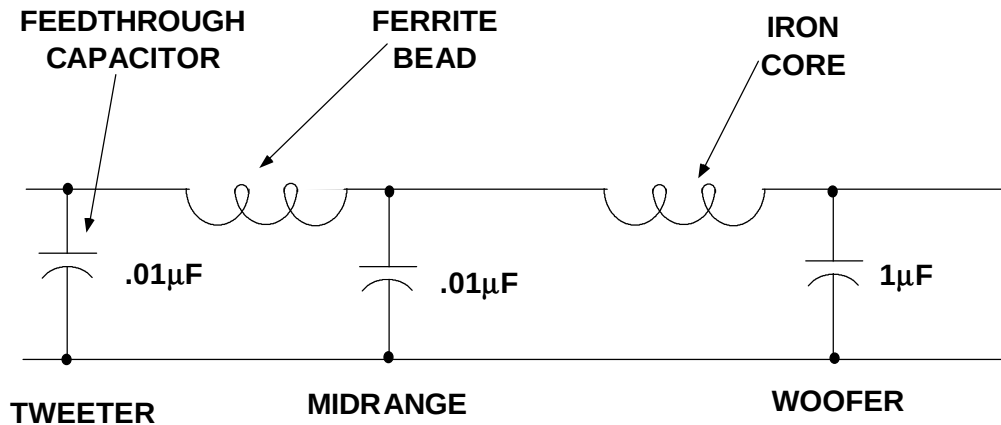


Figure 8.64

Rather than use one LPF stage, it is recommended that the interference frequency bands be separated into *low-band*, *mid-band*, and *high-band*, and then use individual filters for each band. Kimmel Gerke Associates use the stereo speaker analogy of *woofer-midrange-tweeter* for RFI low-pass filter design illustrated in Figure 8.65. In this approach, low frequencies are grouped from 10kHz to 1MHz, mid-band frequencies are grouped from 1MHz to 100MHz, and high frequencies grouped from 100MHz to 1GHz. In the case of a shielded cable input/output, the high frequency section should be located close to the shield to prevent high-frequency leakage at the shield boundary. This is commonly referred to as *feed-through* protection. For applications where shields are not required at the inputs/outputs, then the preferred method is to locate the high frequency filter section as close the analog circuit as possible. This is to prevent the possibility of pickup from other parts of the circuit.

MULTISTAGE FILTERS ARE MORE EFFECTIVE

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STEREO SPEAKER ANALOGY

Figure 8.65

Another cause of filter failure is illustrated in Figure 8.66. If there is any impedance in the ground connection (for example, a long wire or narrow trace connected to the ground plane), then the high-frequency noise uses this impedance path to bypass the filter completely. Filter grounds must be broadband and tied to low-impedance points or planes for optimum performance. High frequency capacitor leads should be kept as short as possible, and low-inductance surface-mounted ceramic chip capacitors are preferable.

NON-ZERO (INDUCTIVE AND/OR RESISTIVE) FILTER GROUND REDUCES EFFECTIVENESS

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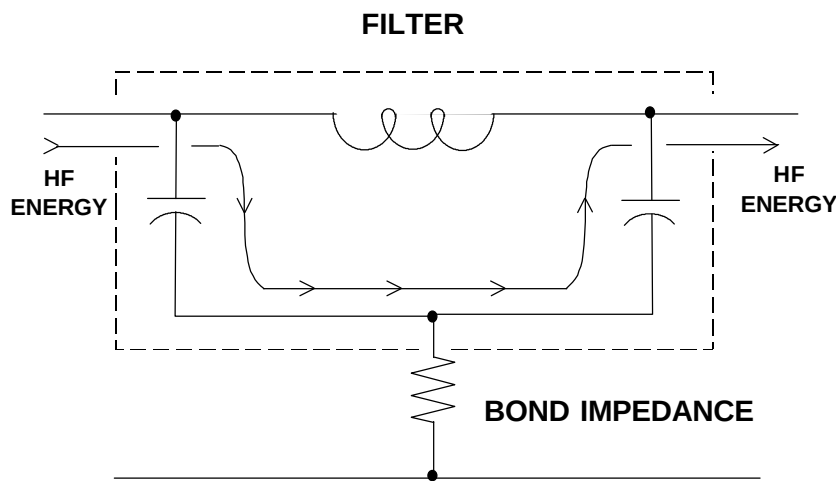


Figure 8.66

SOLUTIONS FOR POWER-LINE DISTURBANCES

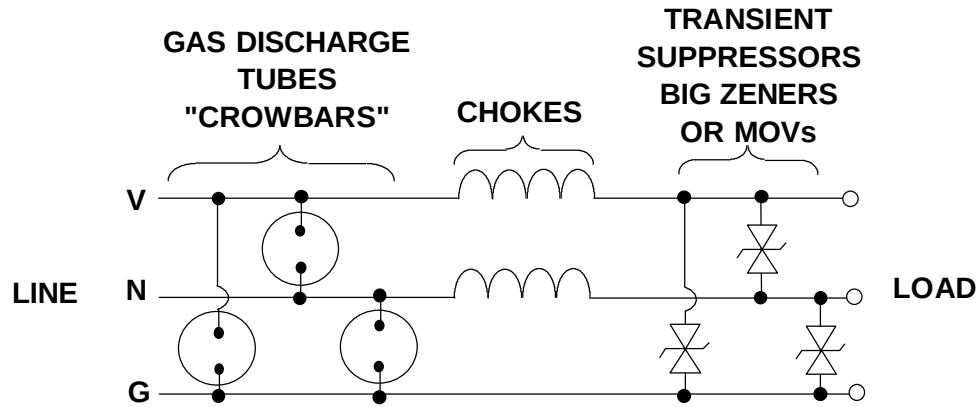
The goal of this next section is not to describe in detail all the circuit/system failure mechanisms which can result from power-line disturbances or faults. Nor is it the intent of this section to describe methods by which power-line disturbances can be prevented. Instead, this section will describe techniques that allow circuits and systems to accommodate *transient* power-line disturbances.

Figure 8.67 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10kV and as fast as 10ns. Gas discharge tubes (crowbars) and large geometry zener diodes (clamps) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOVs) can be substituted for the zener diodes in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.

Commercial EMI filters, as illustrated in Figure 8.68, can be used to filter less catastrophic transients or high-frequency interference. These EMI filters provide both common-mode and differential mode filtering. An optional choke in the safety ground can provide additional protection against common-mode noise. The value of this choke cannot be too large, however, because its resistance may affect power-line fault clearing. These filters work in both directions: they are not only protect the equipment from surges on the power line but also prevent transients from the internal switching power supplies from corrupting the power line.

POWER LINE DISTURBANCES CAN GENERATE EMI

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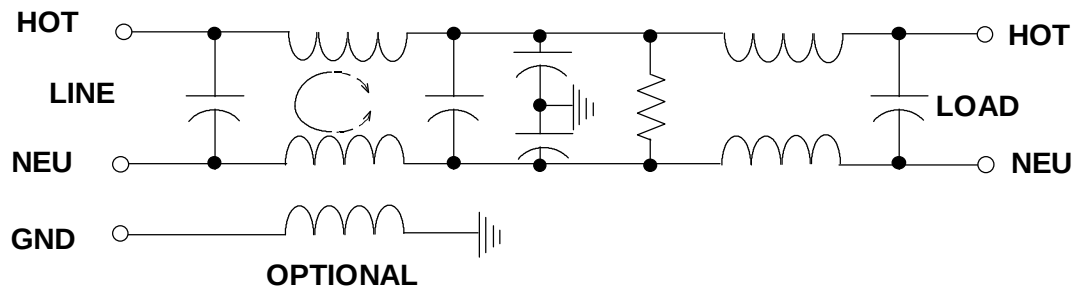


■ COMMON-MODE AND DIFFERENTIAL MODE PROTECTION

Figure 8.67

SCHEMATIC FOR A COMMERCIAL POWER LINE FILTER

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NOTE: OPTIONAL CHOKE ADDED FOR COMMON-MODE PROTECTION

Figure 8.68

Transformers provide the best common-mode power line isolation. They provide good protection at low frequencies (<1MHz), or for transients with rise and fall times greater than 300ns. Most motor noise and lightning transients are in this range, so isolation transformers work well for these types of disturbances. Although the isolation between input and output is galvanic, isolation transformers do not provide sufficient protection against extremely fast transients (<10ns) or those caused by high-amplitude electrostatic discharge (1 to 3ns). As illustrated in Figure 8.69, isolation transformers can be designed for various levels of differential- or common-

mode protection. For differential-mode noise rejection, the Faraday shield is connected to the neutral, and for common-mode noise rejection, the shield is connected to the safety ground.

FARADAY SHIELDS IN ISOLATION TRANSFORMERS PROVIDE INCREASING LEVELS OF PROTECTION

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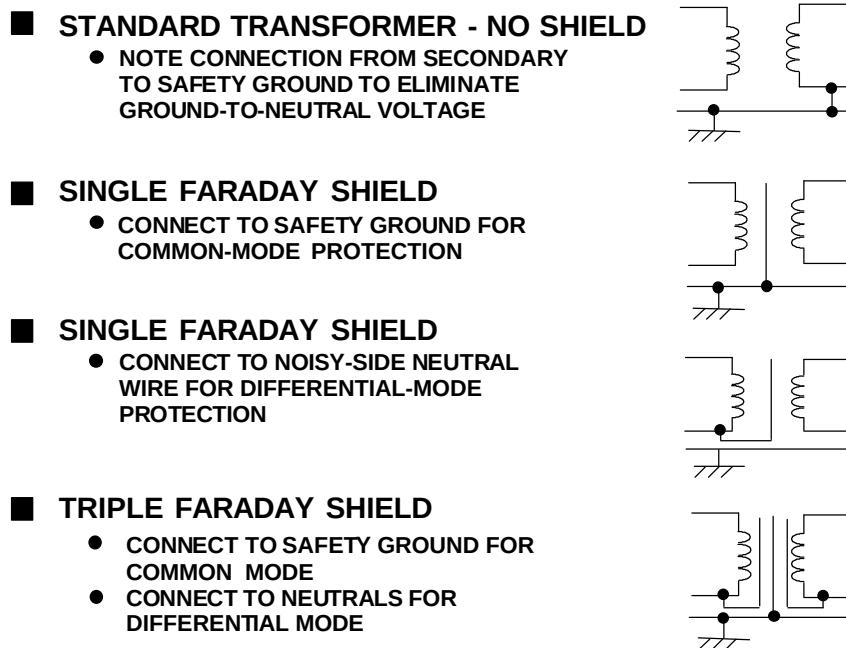


Figure 8.69

PRINTED CIRCUIT BOARD DESIGN FOR EMI PROTECTION

This section will summarize general points regarding the most critical portion of the design phase: the printed circuit board layout. It is at this stage where the performance of the system is most often compromised. This is not only true for signal-path performance, but also for the system's susceptibility to electromagnetic interference and the amount of electromagnetic energy radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

Figure 8.70 is a real-world printed circuit board layout which shows all the paths through which high-frequency noise can couple/radiate into/out of the circuit. Although the diagram shows digital circuitry, the same points are applicable to precision analog, high-speed analog, or mixed analog/digital circuits. Identifying critical circuits and paths helps in designing the PCB layout for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

METHODS BY WHICH HIGH FREQUENCY ENERGY COUPLE AND RADIATE INTO CIRCUITRY VIA PLACEMENT

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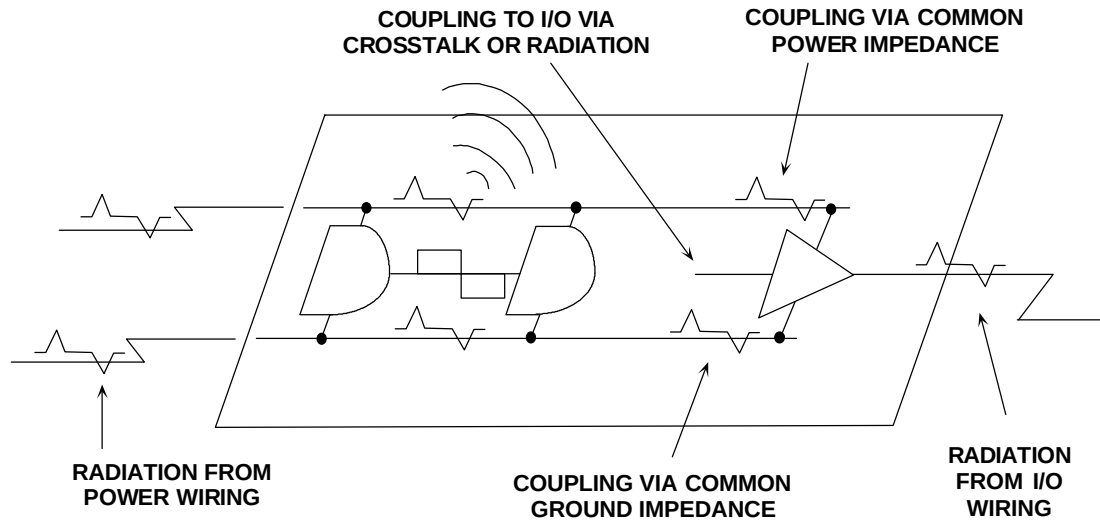


Figure 8.70

A key point in minimizing noise problems in a design is to *choose devices no faster than actually required by the application*. Many designers assume that faster is better: fast logic is better than slow, high bandwidth amplifiers are clearly better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed is not required by the system. Unfortunately, faster is not better, but worse where EMI is concerned.

Many fast DACs and ADCs have digital inputs and outputs with rise and fall times in the nanosecond region. Because of their wide bandwidth, the sampling clock and the digital inputs can respond to any form of high frequency noise, even glitches as narrow as 1 to 3ns. These high speed data converters and amplifiers are easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. Adding a small ferrite bead just before the decoupling capacitor as shown in Figure 8.71 is very effective in filtering high frequency noise on the supply lines. For those circuits that require bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce the emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

POWER SUPPLY FILTERING AND SIGNAL LINE SNUBBING GREATLY REDUCES EMI EMISSIONS

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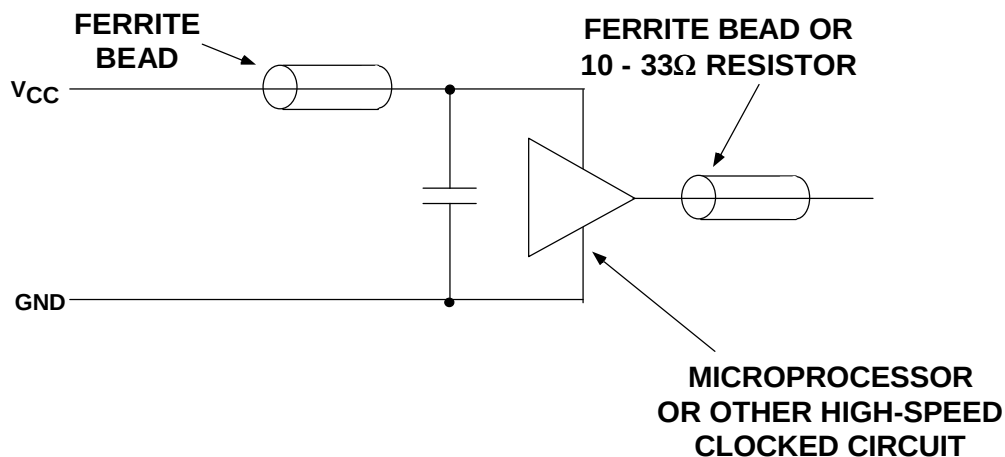


Figure 8.71

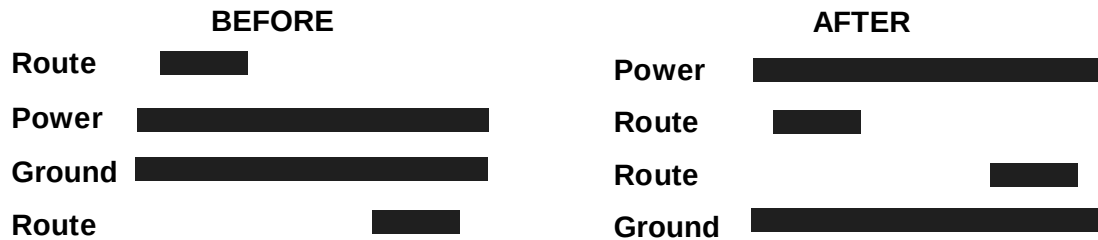
Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution, and critical paths routed by hand.

Properly designed multilayer printed circuit boards can reduce EMI emissions and increase immunity to RF fields by a factor of 10 or more compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes nor analog and digital power planes.

The preferred multi-layer board arrangement is to embed the signal traces between the power and ground planes, as shown in Figure 8.72. These low-impedance planes form very high-frequency *stripline* transmission lines with the signal traces. The return current path for a high frequency signal on a trace is located directly above and below the trace on the ground/power planes. The high frequency signal is thus contained inside the PCB, thereby minimizing emissions. The embedded signal trace approach has an obvious disadvantage: debugging circuit traces that are hidden from plain view is difficult.

"TO EMBED OR NOT TO EMBED" THAT IS THE QUESTION

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■ Advantages of Embedding

- ◆ Lower impedances, therefore lower emissions and crosstalk
 - | Reduction in emissions and crosstalk is significant above 50MHz
- ◆ Traces are protected

■ Disadvantages of Embedding

- ◆ Lower interboard capacitance, harder to decouple
 - | Impedances may be too low for matching
- ◆ Hard to prototype and troubleshoot buried traces

Figure 8.72

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).* A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 8.73 for a number of logic families.

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of $f_{\max}$, then the equivalent risetime, t_r , can be calculated using the equation $t_r = 0.35/f_{\max}$. The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

LINE TERMINATION SHOULD BE USED WHEN LENGTH OF PCB TRACK EXCEEDS 2 inches/ns

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DIGITAL IC FAMILY	t_r, t_s (ns)	PCB TRACK LENGTH (inches)	PCB TRACK LENGTH (cm)
GaAs	0.1	0.2	0.5
ECL	0.75	1.5	3.8
Schottky	3	6	15
FAST	3	6	15
AS	3	6	15
AC	4	8	20
ALS	6	12	30
LS	8	16	40
TTL	10	20	50
HC	18	36	90

t_r = rise time of signal in ns

t_f = fall time of signal in ns

For analog signals @ $f_{\max}$, calculate $t_r = t_f = 0.35 / f_{\max}$

Figure 8.73

Equation 8.4 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_0(\Omega) = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left[\frac{5.98d}{0.89w + t} \right] \quad \text{Eq. 8.4}$$

where ϵ_r = dielectric constant of printed circuit board material;
 d = thickness of the board between metal layers, in mils;
 w = width of metal trace, in mils; and
 t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq. 8.5:

$$t_{pd}(\text{ns} / \text{ft}) = 1.017 \sqrt{0.475\epsilon_r + 0.67} \quad \text{Eq. 8.5}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 ($\epsilon_r=4.7$) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be 88Ω and 1.7ns/ft (7"/ns), respectively.

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SHIELDING CONCEPTS

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1,2, and 6 cited at the end of the section for more detailed information.

Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π , or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_0 = 377\Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377Ω . If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377Ω .

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. Both concepts are illustrated in Figure 8.74. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

REFLECTION AND ABSORPTION ARE THE TWO PRINCIPAL SHIELDING MECHANISMS

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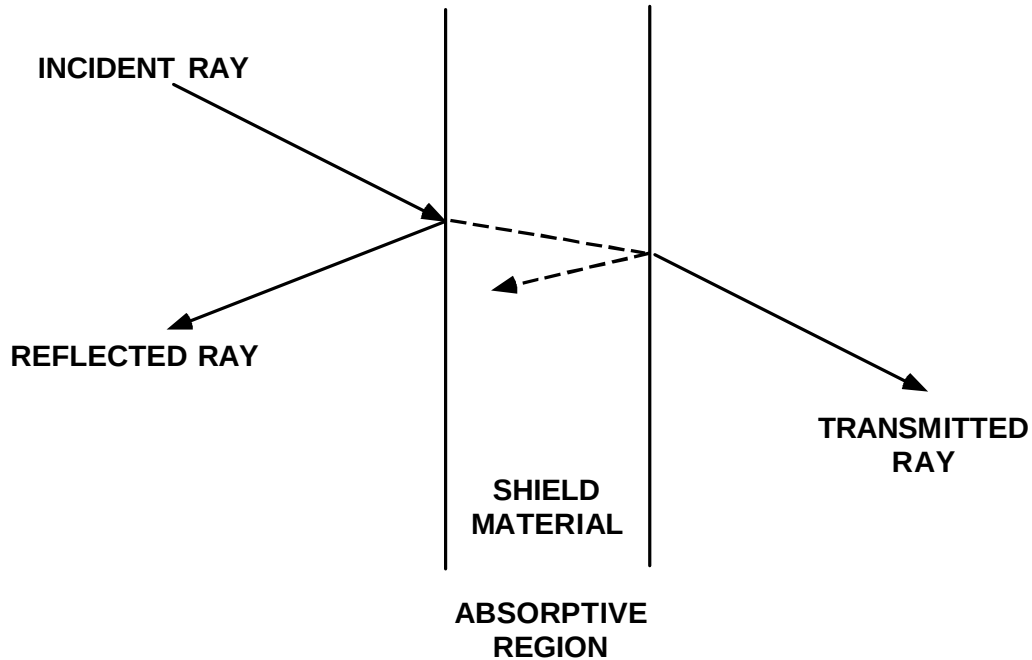


Figure 8.74

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(\text{dB}) = 322 + 10\log_{10} \left[\frac{\sigma_r}{\mu_r f^3 r^2} \right] \quad \text{Eq. 8.6}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;
 μ_r = relative permeability of the shielding material, in Henries per meter;
 f = frequency of the interference, and
 r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(\text{dB}) = 14.6 + 10\log_{10} \left[\frac{f r^2 \sigma_r}{\mu_r} \right] \quad \text{Eq. 8.7}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}(\text{dB}) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \quad \text{Eq. 8.8}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(\text{dB}) = 3.34 \, t \sqrt{\sigma_r \mu_r f} \quad \text{Eq. 8.9}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_s , increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Figure 8.75.

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation (see Figure 8.76). Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

CONDUCTIVITY AND PERMEABILITY FOR VARIOUS SHIELDING MATERIALS

MATERIAL	RELATIVE CONDUCTIVITY	RELATIVE PERMEABILITY
Copper	1	1
Aluminum	1	0.61
Steel	0.1	1,000
Mu-Metal	0.03	20,000

Conductivity: Ability to Conduct Electricity

Permeability: Ability to Absorb Magnetic Energy

Figure 8.75

ANY OPENING IN AN ENCLOSURE CAN ACT AS AN EMI WAVEGUIDE BY COMPROMISING SHIELDING EFFECTIVENESS

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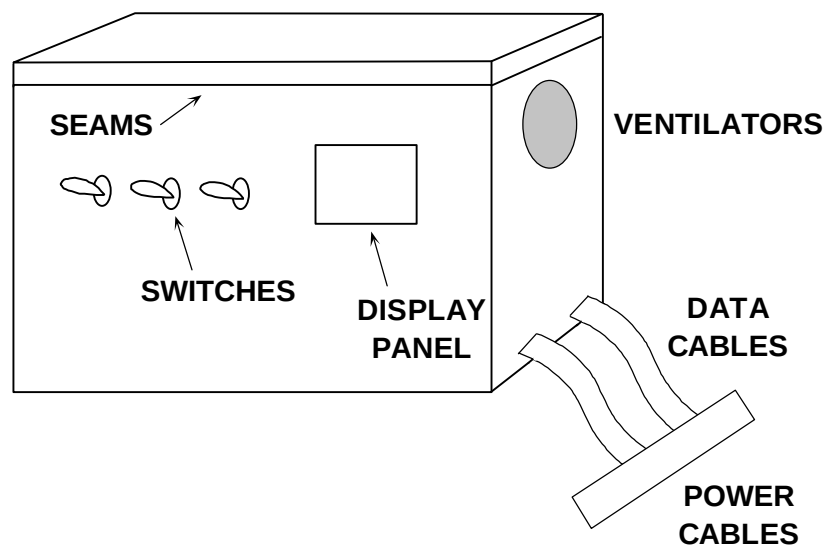


Figure 8.76

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 8.10 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness (dB)} = 20 \log_{10} \left(\frac{\lambda}{2 \cdot L} \right) \quad \text{Eq. 8.10}$$

where λ = wavelength of the interference and
L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.

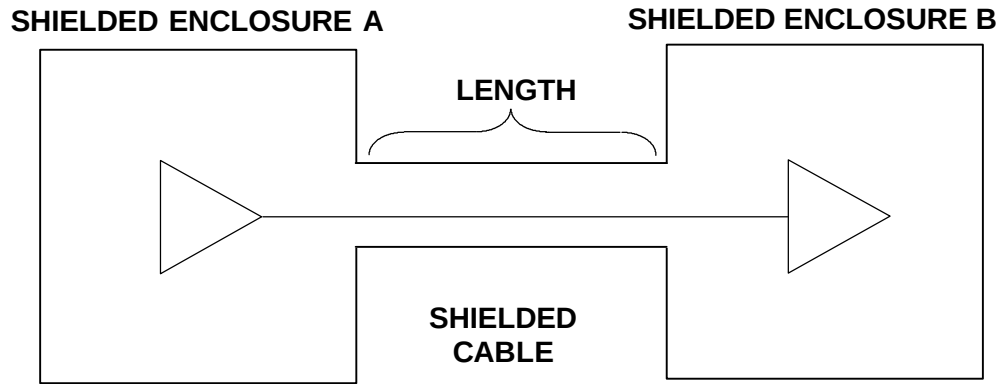
Sensors and Cable Shielding

The improper use of cables and their shields is a significant contributor to both radiated and conducted interference. As illustrated in Figure 8.77, effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness.

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50/60Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable. To protect circuits against low-frequency electric-field pickup, only one end of the shield should be returned to a low-impedance point. A generalized example of this mechanism is illustrated in Figure 8.78.

LENGTH OF SHIELDED CABLES DETERMINES AN "ELECTRICALLY LONG" OR "ELECTRICALLY SHORT" APPLICATION

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FULLY SHIELDED ENCLOSURES CONNECTED BY FULLY SHIELDED CABLE KEEP ALL INTERNAL CIRCUITS AND SIGNAL LINES INSIDE THE SHIELD.

- TRANSITION REGION: $1/20$ WAVELENGTH

Figure 8.77

CONNECT THE SHIELD AT ONE POINT AT THE LOAD TO PROTECT AGAINST LOW FREQUENCY (50/60Hz)

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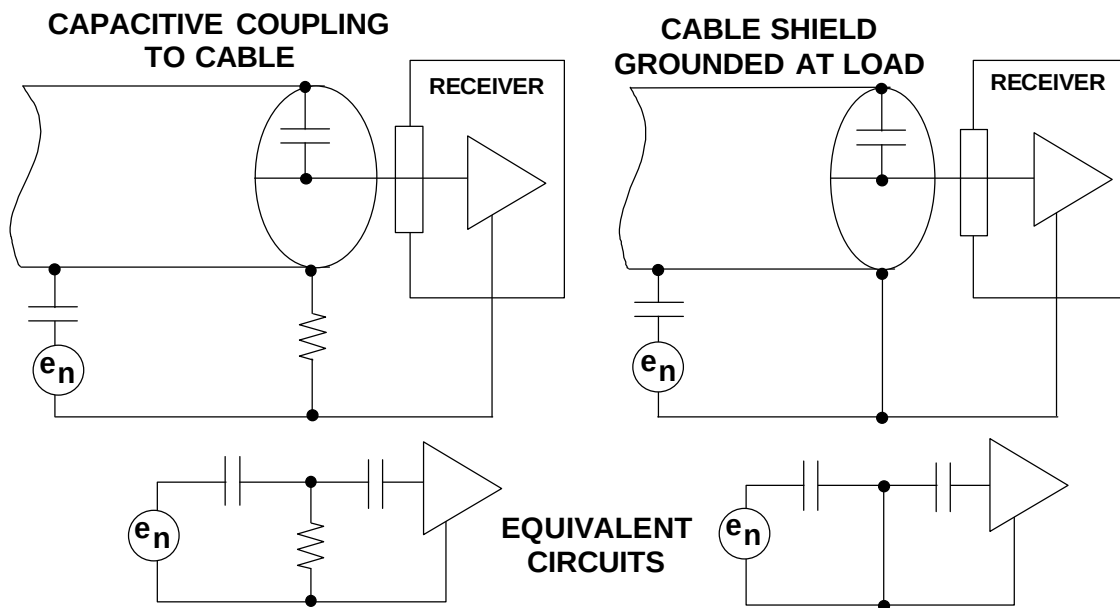


Figure 8.78

In this example, the shield is grounded at the receiver. An exception to this approach (which will be highlighted again later) is the case where line-level ($>1V_{rms}$) audio signals are transmitted over long distances using twisted pair, shielded cables. In these applications, the shield again offers protection against low-frequency interference, and an accepted approach is to ground the shield at the driver end (LF and HF ground) and ground it at the receiver with a capacitor (HF ground only).

In those applications where the length of the cable is *electrically long*, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency ($<1MHz$), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference ($>1MHz$), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure. Low-frequency ground loops can be eliminated by replacing one of the DC shield connections to ground with a low inductance $0.01\mu F$ capacitor. This capacitor prevents low frequency ground loops and shunts high frequency interference to ground.

The best shield can be compromised by poor connection techniques. Shields often use “pig-tail” connections to make the connection to ground. A “pig-tail” connection is a single wire connection from shield to either chassis or circuit ground. This type of connection is inexpensive, but at high frequency, it does not provide low impedance. Quality shields do not leave large gaps in the cable/instrument shielding system. Shield gaps provide paths for high frequency EMI to enter the system. The cable shielding system should include the cable end connectors. Ideally, cable shield connectors should make 360° contact with the chassis ground.

As shown in Figure 8.79, pigtail terminations on cables very often cause systems to fail radiated emissions tests because high-frequency noise has coupled into the cable shield, generally through stray capacitance. If the length of the cable is considered *electrically long* at the interference frequency, then it can behave as a very efficient quarter-wave antenna. The cable pigtail forms a matching network, as shown in the s, to radiate the noise which coupled into the shield. In general, pigtails are only recommended for applications below 10kHz, such as 50/60Hz interference protection. For applications where the interference is greater than 10kHz, shielded connectors, electrically and physically connected to the chassis, should be used.

"SHIELDED" CABLE CAN CARRY HIGH FREQUENCY CURRENT AND BEHAVES AS AN ANTENNA

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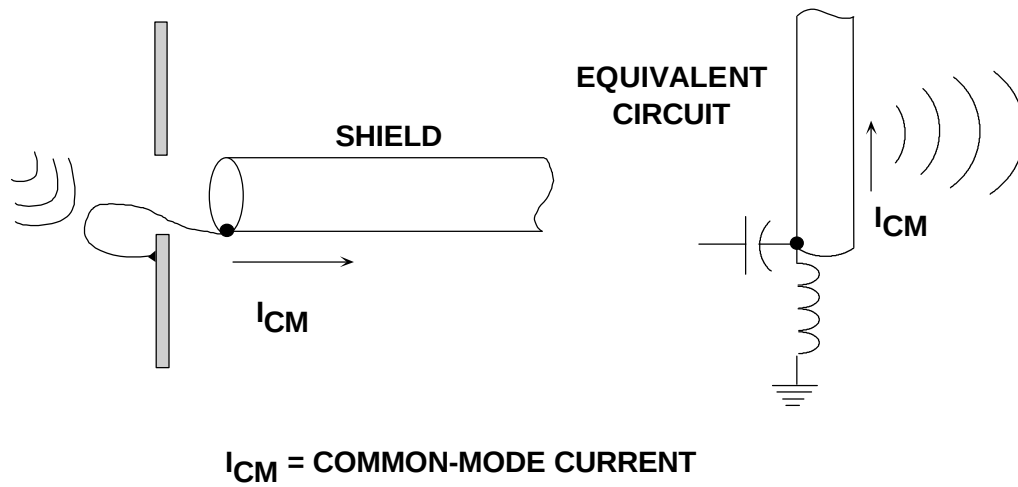


Figure 8.79

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