Section 8. Replacing or Integrating PLL's with DDS solutions

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DDS vs Standard PLL

PLL (phase-locked loop) frequency synthesizers are long-time favorites with designers who need stable, *programmable* high & low frequencies, and high quality signal sources or clocks. They are well understood, widely available, and inexpensive. What can a DDS do that a PLL can't?

- Extremely fast frequency changes make a DDS *thousands* of times more agile than a PLL. This makes DDS a natural choice for frequency-hopping and spread-spectrum.
- Frequency resolution is extraordinary! Up to one-millionth of a Hertz
- Fundamental output frequency span > 40 octaves (.000001 Hz to 150 MHz)
- Effortless ultra high-speed digital phase modulation (PSK) and FSK
- Perfect, exactly repeatable synchronization of multiple DDS's (allowing quadrature and other phase offset relationships to be easily accomplished)

Applications requiring any of the above traits should evaluate DDS as a possible solution. As an example, consider *dielectrophoresis* This phenomenon is utilized in micro-biology studies to separate, move and rotate individual cells or bacteria in a polarized medium using non-uniform traveling fields, typically under a microscope. The traveling waves are emitted from micro-electrodes that are excited by synchronized signals from two DDS's. Rotation and movement of particles is accomplished by connecting the synchronized signals of relative differing phases to successive electrodes (0°, 90°, 180° , 270°, etc.) which in turn generate the traveling field in which the particles move. Differing particles are affected differently by various wavelength signals, and as such, it is desirable to generate signals over a wide frequency range. DDS, by virtue of its extremely wide output frequency span, phase offset capability and precise synchronization, is an ideal vehicle to generate the synchronized signals from 1 kHz to 50 MHz typically used in this technique.

One major difference between a PLL and a DDS is the PLL's ability to lock its output to the input phase of a reference clock. A standard PLL can easily lock its VCO to a 10 MHz input signal and provided a phase locked 20 MHz output signal. The DDS can get extremely close to the 20 MHz output frequency but requires an internal clock speed that is at least twice that of the output frequency. A DDS with a 6× multiplier will synchronize with the 10 MHz master clock and internally clock at a 60 MHz rate that will (with 32-bit resolution) output a 19.9999999954 MHz or 20.000000009 MHz signal, but exactly 20 MHz can not be achieved. In fact, the *only* time the DDS output is an *exact integer division* of its system clocking frequency is when the division factor is a power of two, 2^N. Only then will the input clock and the output frequency be "phase-locked" or synchronized.

The above PLL example dramatically reverses itself when attempting to construct a PLL to output exactly 19.9999999954 MHz for a 10 MHz input signal! Imagine trying to digitally

increment or decrement a PLL in sub-Hz steps. So it can be seen that there are optimum applications for DDS's just as there are for PLL's.

A DDS can be equipped with a tunable reference clock oscillator that will allow it to perform like the VCO in a PLL. Exact frequency tuning is accomplished by first setting the tuning word *close* to the desired output frequency. The DDS reference clock frequency is tuned (without altering the frequency tuning word) until the output frequency exactly matches the desired frequency. This requires the DDS reference oscillator to be somewhat tunable while retaining high-Q characteristics such as low phase noise and frequency stability (such as in a VCXO). The 6× clock multiplier (of an AD9851 DDS) comes in handy because changes in the reference oscillator frequency will be multiplied by 6, giving considerably more tuning range to a VCXO (voltage controlled crystal oscillator). Figure 8-1 shows a partial block diagram of a practical system.

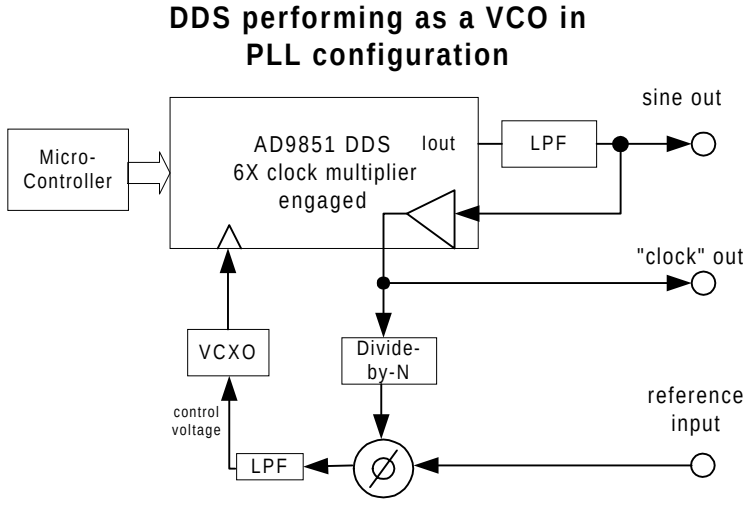

Figure 8-1. DDS Combined with PLL

The system in Figure 8-1 has very limited applications and is limited to output frequencies of approximately 40% of the system clock. The primary DDS advantage over a standard VCO in this configuration is its thirty-octave range of operation (.04 Hz to 70 MHz). Most of the other desirable DDS traits are lost in this configuration due to the presence of the "divide-by-N" stage and filters that take time to settle.

Integrating DDS with PLL's for Higher Output Frequencies

Another interesting application that combines the extreme frequency resolution trait of a DDS with the high frequency attribute of a PLL is seen in Figure 8-2. Here, the DDS acts as a fractional "Divide-by-N" stage within the feedback loop of a PLL. This gives the PLL sub-Hertz resolution at output frequencies up to the system clock limit of the DDS – typically 50 to 300 MHz. Any DDS spurs within the PLL bandwidth will be multiplied (gained-up) by 20 Log (Fout/Fref) .

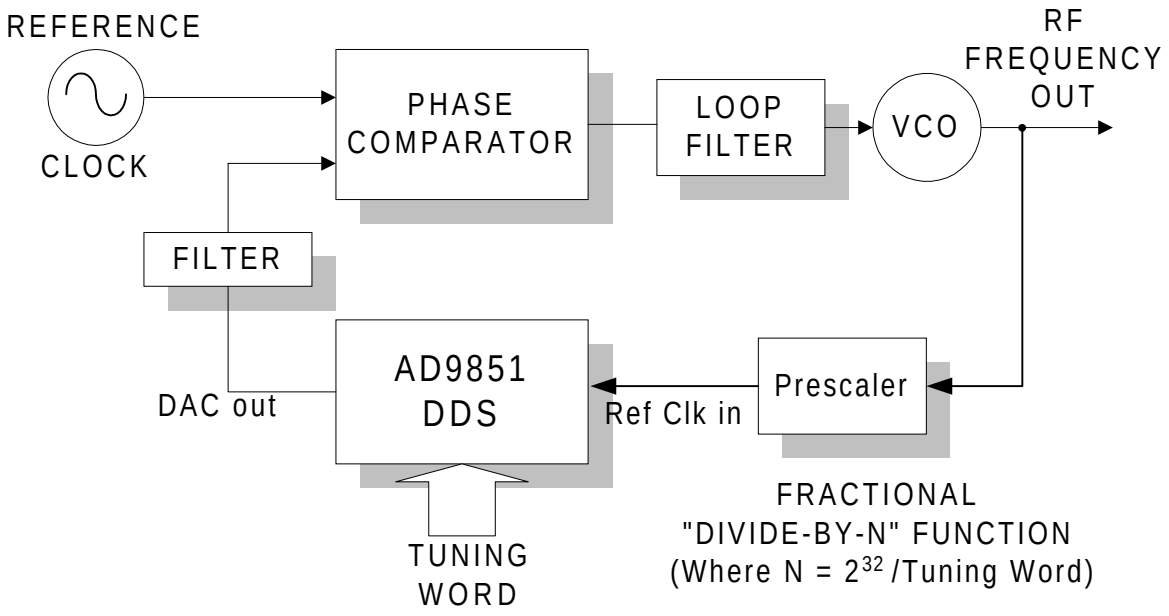

Figure 8-2. Fractional "Divide-by-N" Allows Sub-Hertz Frequency Resolution at VHF

Figure 8-3 below shows the DDS performing the local oscillator function in an analog mixer within the PLL loop. This gives the PLL greatly increased frequency resolution at the VCO output frequency while retaining the high signal quality traits of the fixed PLL reference oscillator. The VCO could be operating at HF, VHF, UHF or microwave frequencies. The "divide-by-N" stage could be a fixed divider or a course, programmable divider that selects a particular frequency range while the DDS provides the fine frequency resolution within that range. DDS spurs will be reduced in the "divide-by-N" stage but augmented by the same amount in the frequency multiplication process. Therefore, any DDS spurs within the PLL loop bandwidth will be passed along *unchanged* to the output. Spur reduction and augmentation follow the standard processing gain or loss of 20Log Fout/Fref. Simply stated, flaws (spurs, jitter, phase noise) in the reference signal that are within the loop passband of a PLL will be multiplied along with the frequency. Greater PLL multiplication factors result in greater reference signal degradation at the output. Practical output limitations are imposed by the need to adequately filter the mixer output.

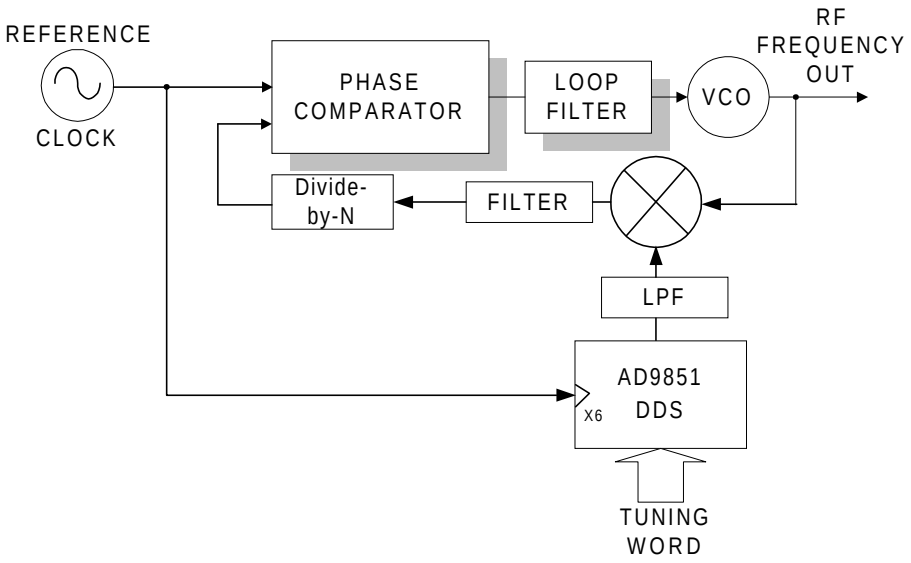

Figure 8-3. DDS as Local Oscillator in Mixer/PLL at UHF or Microwave Output Frequencies

Practical Application of a DDS Driving a PLL at 900 MHz

Figure 8-4 shows a 14.0 MHz output signal of an AD9851 DDS that is being input as a reference to a National Semiconductor LMX1501A, 900 MHz PLL evaluation board. Figure 8-5 shows the impact of PLL frequency multiplication on the phase noise and spurs of the reference signal after multiplication to 896 MHz by the LMX1501A. In this instance, the 14.0 MHz signal from the DDS was first divided by a factor of 64 in the LMX1501A, yielding a phase noise improvement of 36 dB. The resulting signal was then multiplied by a factor of 4096, yielding a phase noise degradation of 72 dB. Overall phase noise is theoretically degraded by approximately 36 dB within the PLL loop bandwidth. Spurs are located beyond the PLL loop bandwidth and are only slightly augmented.

Note: The LMX1501A evaluation board was being operated at 3.1 volts and the DDS reference input signal is approximately 10 dB below the recommended input level. These two factors were both seen to have an adverse impact on the overall phase noise of the PLL output. The examples shown below are meant to demonstrate the impact of PLL multiplication on reference input phase noise and spur levels and do not represent an optimized system.

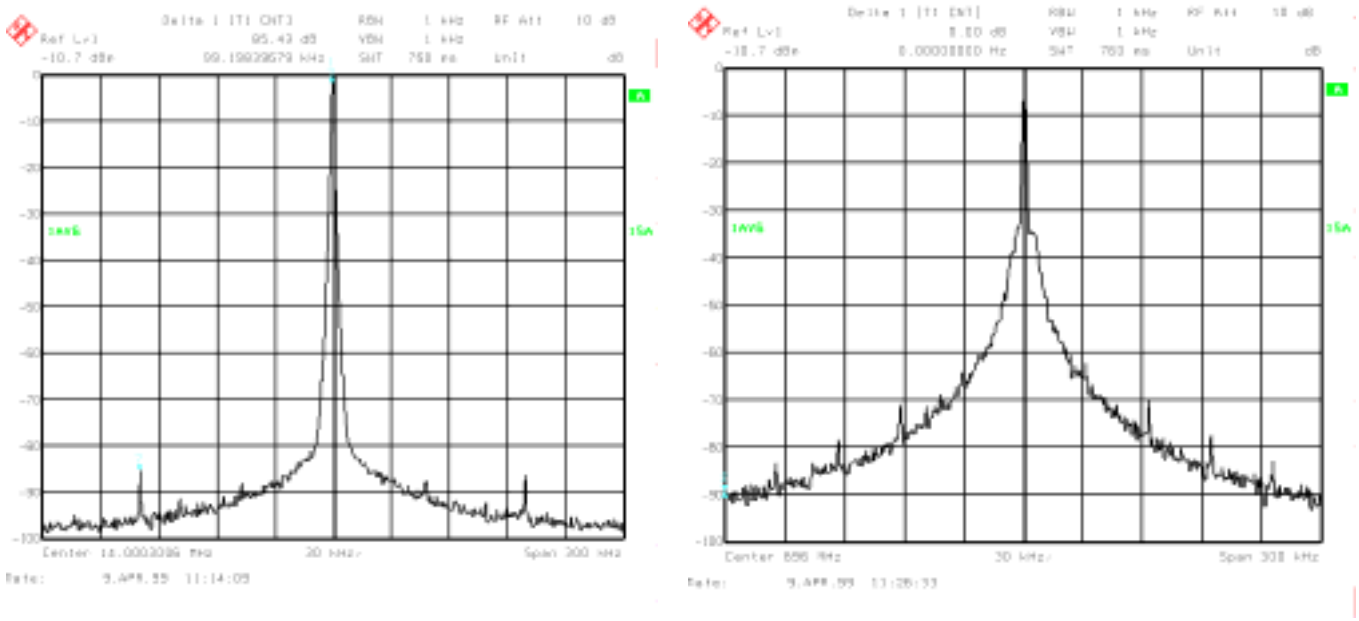

Figure 8-4. 14 MHz DDS Reference Signal to PLL

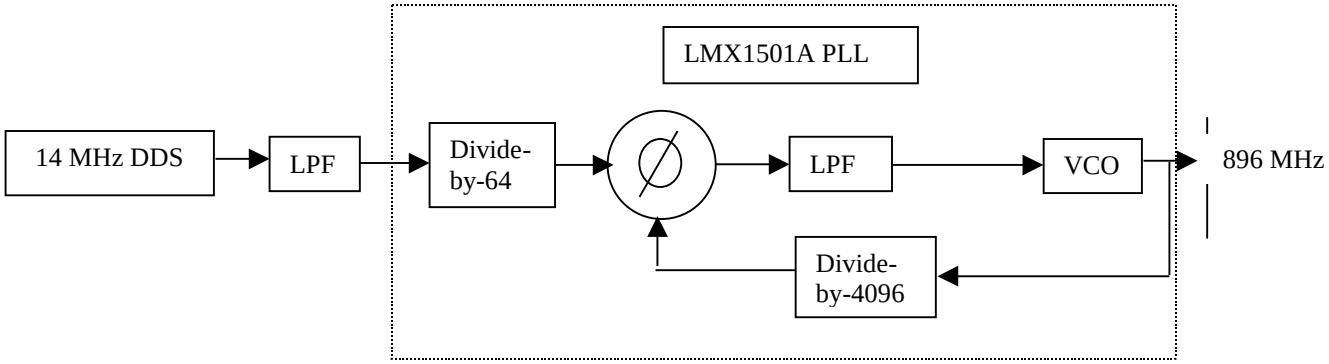

Figure 8-5: 896 MHz PLL output

Figures 8-6 and 8-7, show a DDS output with spurs and the PLL's response, both within and outside of the loop bandwidth. The same PLL conditions exist as explained above. The PLL loop bandwidth at this particular divide-by-N appears to extend to approximately 80 kHz as seen by the PLL's diminishing response to spurs beyond that cutoff frequency.

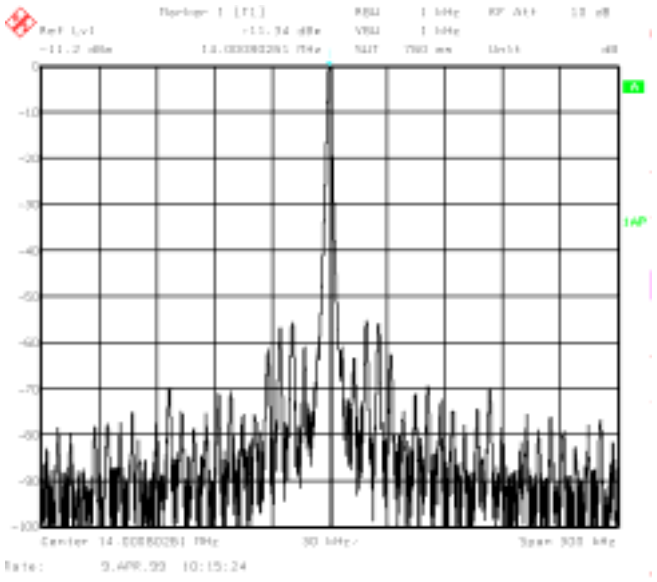

Figure 8-6. 14 MHz DDS Reference Signal with Spurs

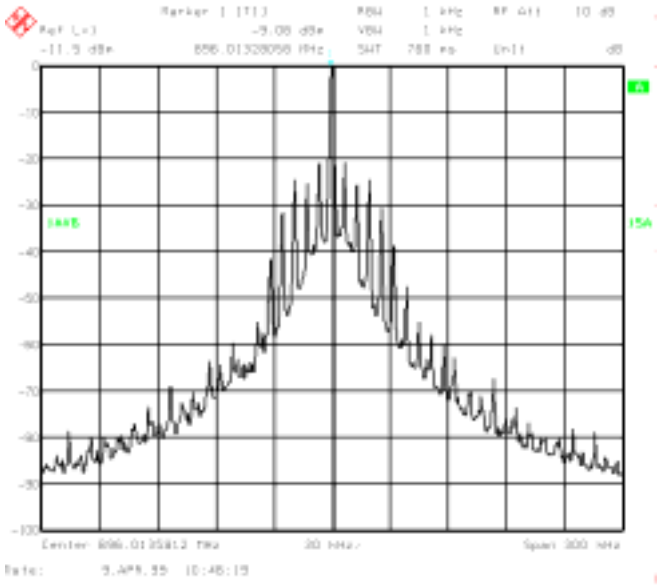

Figure 8-7.896 MHz LMX1501A PLL Output

Comparing Figure 8-5 with Figure 8-7, designers can see how important it is to keep spur levels at the PLL reference inputs as low as possible or to keep spurs out of the PLL loop bandwidth. A seemingly insignificant reference spur within the loop bandwidth can become a huge component in the VCO output spectrum. Another strategy to control spurs, such as in Figure 8-3, is to place the known spur source ahead of a divide-by-N stage to reduce spurs levels by 20 Log (Fout/Fin). If the divide-by-N stage had been placed at the mixer input instead of the output, then any DDS spurs within the loop bandwidth would have been passed undiminished and subjected to loop gain augmentation.

The need for low output phase noise is an equally important consideration in any noise sensitive system and unfortunately, this is a PLL weakness that requires elaborate avoidance measures to achieve good performance. The inherent phase noise improvement (of the reference signal relative to the output) in DDS is a quality that makes its use nearly ideal as a PLL replacement at lower output frequencies. And, at VHF and higher output frequencies, the DDS can function as a LO in a VHF/UHF mixer (see Figure 8-8) that avoids the multiplication pitfalls of the PLL and maintains the high quality attributes of the DDS signal. A practical output limitation is imposed by the need to adequately filter the mixer output.

Figure 8-8. VHF/UHF Output Maintains Phase Noise and Spur Performance of Low Frequency DDS Output and Avoids PLL Entirely.