

# SECTION 2

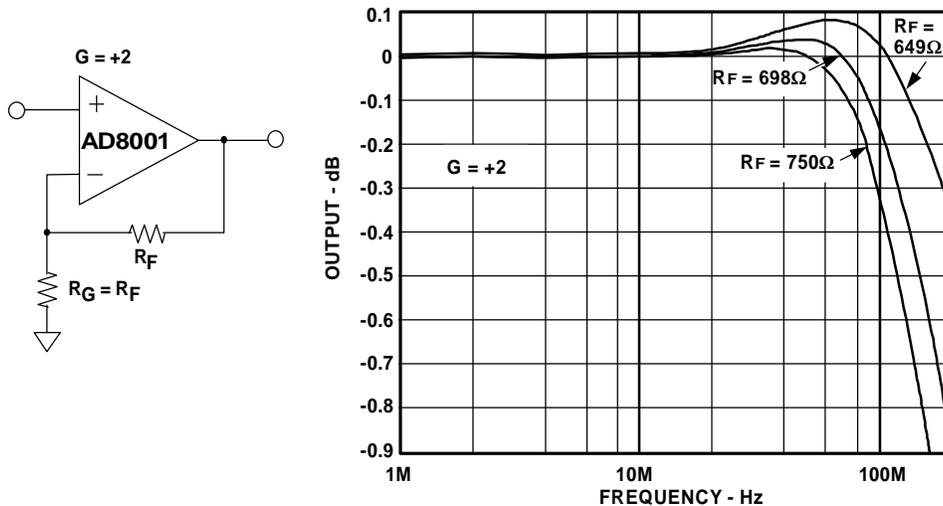
## HIGH SPEED OP AMP APPLICATIONS

*Walt Kester, Walt Jung*

### OPTIMIZING THE FEEDBACK NETWORK FOR MAXIMUM BANDWIDTH FLATNESS IN WIDEBAND CFB OP AMPS

Achieving the highest 0.1dB bandwidth flatness is important in many video applications. Because of the critical relationship between the feedback resistor and the bandwidth of a CFB op amp, optimum bandwidth flatness is highly dependent on the feedback resistor value, the resistor parasitics, as well as the op amp package and PCB parasitics. Figure 2.1 shows the fine scale (0.1dB/division) flatness plotted versus the feedback resistance for the AD8001 in a non-inverting gain of 2. These plots were made using the AD8001 evaluation board with surface mount resistors.

#### AD8001 CFB OP AMP BANDWIDTH FLATNESS OPTIMIZED BY PROPER SELECTION OF FEEDBACK RESISTOR



## 2.1

It is recommended that once the optimum resistor values have been determined, 1% tolerance values should be used. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Surface mount resistors are the optimum choice, and it is not recommended that leaded components be used with high speed op amps at these frequencies because of their parasitics.

Slightly different resistor values may be required to achieve optimum performance in the DIP versus the SOIC packages (see Figure 2.2). The SOIC package exhibits slightly lower parasitic capacitance and inductance than the DIP. The data shows the optimum feedback ( $R_G$ ) and feedforward ( $R_F$ ) resistors for highest 0.1dB bandwidth for the AD8001 in the DIP and the SOIC packages. As you might

suspect, the SOIC package can be optimized for slightly higher 0.1dB bandwidth because of its lower parasitics.

## OPTIMUM VALUES OF $R_F$ AND $R_G$ FOR AD8001 DIP AND SOIC PACKAGES (MAXIMUM 0.1dB BANDWIDTH)

**AD8001AN (DIP) GAIN**

Component	-1	+1	+2
$R_F$	649 $\Omega$	1050 $\Omega$	750 $\Omega$
$R_G$	649 $\Omega$	-	750 $\Omega$
0.1dB Flatness	105MHz	70MHz	105MHz

**AD8001AR (SOIC) GAIN**

Component	-1	+1	+2
$R_F$	604 $\Omega$	953 $\Omega$	681 $\Omega$
$R_G$	604 $\Omega$	-	681 $\Omega$
0.1dB Flatness	130MHz	100MHz	120MHz

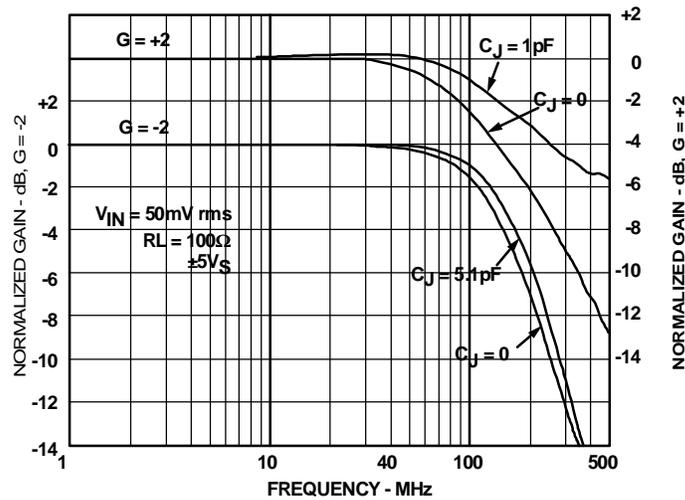


## 2.2

As has been discussed, the CFB op amp is relatively insensitive to capacitance on the inverting input when it is used in the inverting mode (as in an I/V application). This is because the low inverting input impedance is in parallel with the external capacitance and tends to minimize its effect. In the non-inverting mode, however, even a few picofarads of stray inverting input capacitance may cause peaking and instability. Figure 2.3 shows the effects of adding summing junction capacitance to the inverting input of the AD8004 (SOIC package) for  $G = +2$ . Note that only 1pF of added inverting input capacitance ( $C_J$ ) causes a significant increase in bandwidth and an increase in peaking. For  $G = -2$ , however, 5pF of additional inverting input capacitance causes only a small increase in bandwidth and no significant increase in peaking.

High speed VFB op amps are sensitive to stray inverting input capacitance when used in either the inverting or non-inverting mode.

## AD8004 CFB OP AMP SENSITIVITY TO INVERTING INPUT CAPACITANCE FOR $G = +2$ , $G = -2$



2.3

### DRIVING CAPACITIVE LOADS

From system and signal fidelity points of view, transmission line coupling between stages is best, and is described in some detail in the next section. However, complete transmission line system design may not always be possible or practical. In addition, various other parasitic issues need careful consideration in high performance designs. One such problem parasitic is amplifier load capacitance, which potentially comes into play for all wide bandwidth situations which do not use transmission line signal coupling.

A general design rule for wideband linear drivers is that capacitive loading (cap loading) effects should *always* be considered. This is because PC board capacitance can build up quickly, especially for wide and long signal runs over ground planes insulated by a thin, higher K dielectric. For example, a 0.025" PC trace using a G-10 dielectric of 0.03" over a ground plane will run about 22pF/foot (Reference 1). Even relatively small load capacitance (i.e., <100 pF) can be troublesome, since while not causing outright oscillation, it can still stretch amplifier settling time to greater than desirable levels for a given accuracy.

The effects of cap loading on high speed amplifier outputs are not simply detrimental, they are actually an anathema to high quality signals. However, before-the-fact designer knowledge still allows high circuit performance by employing various tricks of the trade to combat the capacitive loading. If it is not driven via a transmission line, remote signal circuitry should be checked for capacitive loading very carefully, and characterized as best possible. Drivers which face poorly defined load capacitance should be bullet-proofed accordingly with an appropriate design technique from the options list below.

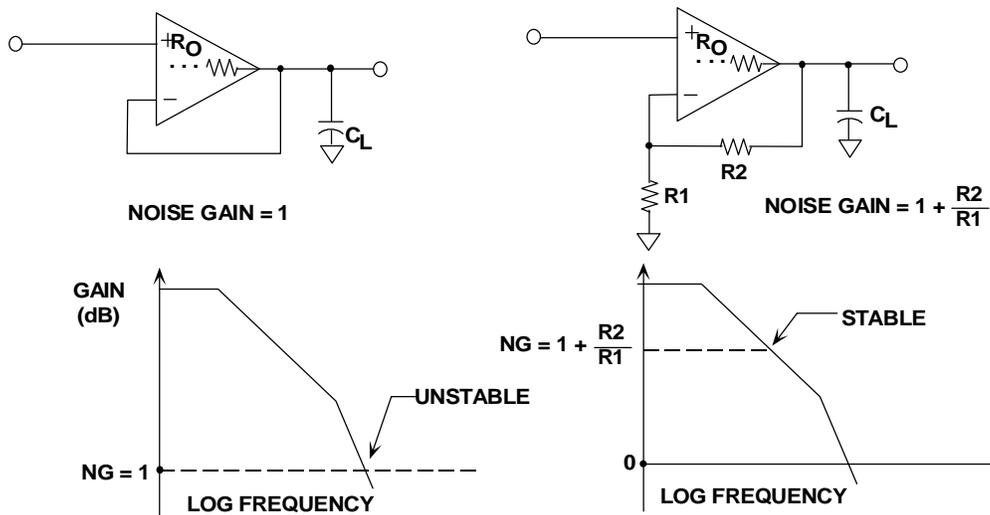
Short of a true matched transmission line system, a number of ways exist to drive a load which is capacitive in nature while maintaining amplifier stability.

*Custom capacitive load (cap load) compensation includes two possible options, namely a); overcompensation, and b); an intentionally forced-high loop noise gain allowing crossover in a stable region. Both of these steps can be effective in special situations, as they reduce the amplifier's effective closed loop bandwidth, so as to restore stability in the presence of cap loading.*

Overcompensation of the amplifier, when possible, reduces amplifier bandwidth so that the additional load capacitance no longer represents a danger to phase margin. As a practical matter however, amplifier compensation nodes to allow this are available on few high speed amplifiers. One such useful example is the AD829, compensated by a single capacitor at pin 5. In general, almost any amplifier using external compensation can always be over compensated to reduce bandwidth. This will restore stability against cap loads, by lowering the amplifier's unity gain frequency.

*Forcing a high noise gain*, is shown in Figure 2.4, where the capacitively loaded amplifier with a noise gain of unity at the left is seen to be unstable, due to a  $1/\beta$  - open loop rolloff intersection on the Bode diagram in an unstable  $-12\text{dB/octave}$  region. For such a case, quite often stability can be restored by introducing a higher noise gain to the stage, so that the intersection then occurs in a stable  $-6\text{dB/octave}$  region, as depicted at the diagram right Bode plot.

## CAPACITIVE LOADING ON OP AMP GENERALLY REDUCES PHASE MARGIN AND MAY CAUSE INSTABILITY, BUT INCREASING THE NOISE GAIN OF THE CIRCUIT IMPROVES STABILITY

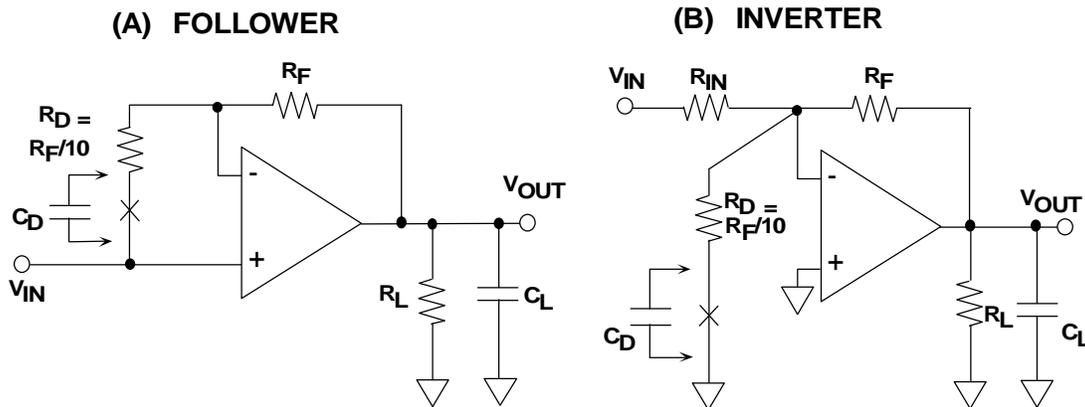


## 2.4

To enable a higher noise gain (which does not necessarily need to be the same as the stage's *signal gain*), use is made of resistive or RC pads at the amplifier input, as in Figure 2.5. This trick is more broad in scope than overcompensation, and has the advantage of not requiring access to any internal amplifier nodes. This generally

allows use with any amplifier setup, even voltage followers. The technique adds an extra resistor  $R_D$ , which works against  $R_F$  to force the noise gain of the stage to a level appreciably higher than the signal gain (which is unity in both cases here). Assuming that  $C_L$  is a value which produces a parasitic pole near the amplifier's natural crossover, this loading combination would likely lead to oscillation due to the excessive phase lag. However with  $R_D$  connected, the higher amplifier noise gain produces a new  $1/\beta$  - open loop rolloff intersection, about a decade lower in frequency. This is set low enough that the extra phase lag from  $C_L$  is no longer a problem, and amplifier stability is restored.

## RAISING NOISE GAIN (DC OR AC) FOR FOLLOWER OR INVERTER STABILITY

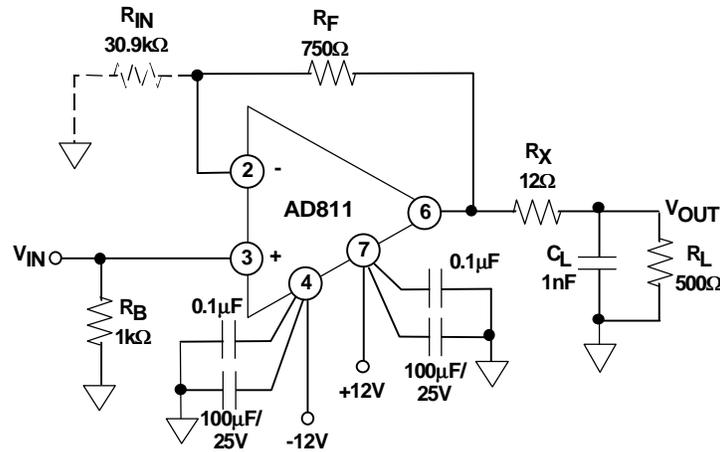


## 2.5

A drawback to this trick is that the DC offset and input noise of the amplifier are raised by the value of the noise gain, when the optional  $C_D$  is *not* present. But, when  $C_D$  is used in series with  $R_D$ , the offset voltage of the amplifier is not raised, and the gained-up AC noise components are confined to a frequency region above  $1/(2\pi \cdot R_D \cdot C_D)$ . A further caution is that the technique can be somewhat tricky when separating these operating DC and AC regions, and should be applied carefully with regard to settling time (Reference 2). Note that these simplified examples are generic, and in practice the absolute component values should be matched to a specific amplifier.

*“Passive” cap load compensation, shown in Figure 2.6, is the most simple (and most popular) isolation technique available. It uses a simple “out-of-the-loop” series resistor  $R_X$  to isolate the cap load, and can be used with any amplifier, current or voltage feedback, FET or bipolar input.*

## OPEN-LOOP SERIES RESISTANCE ISOLATES CAPACITIVE LOAD FOR AD811 CURRENT FEEDBACK OP AMP (CIRCUIT BANDWIDTH = 13.5MHz)



### 2.6

As noted, this technique can be applied to virtually any amplifier, which is a major reason why it is so useful. It is shown here with a current feedback amplifier suitable for high current line driving, the AD811, and it consists of just the simple (passive) series isolation resistor,  $R_X$ . This resistor's minimum value for stability will vary from device to device, so the amplifier data sheet should be consulted for other ICs. Generally, information will be provided as to the amount of load capacitance tolerated, and a suggested minimum resistor value for stability purposes.

Drawbacks of this approach are the loss of bandwidth as  $R_X$  works against  $C_L$ , the loss of voltage swing, a possible lower slew rate limit due to  $I_{MAX}$  and  $C_L$ , and a gain error due to the  $R_X$ - $R_L$  division. The gain error can be optionally compensated with  $R_{IN}$ , which is ratioed to  $R_F$  as  $R_L$  is to  $R_X$ . In this example, a  $\pm 100$ mA output from the op amp into  $C_L$  can slew  $V_{OUT}$  at a rate of  $100V/\mu s$ , far below the intrinsic AD811 slew rate of  $2500V/\mu s$ . Although the drawbacks are serious, this form of cap load compensation is nevertheless useful because of its simplicity. If the amplifier is not otherwise protected, then an  $R_X$  resistor of  $50$ - $100\Omega$  should be used with virtually any amplifier facing capacitive loading. Although a non-inverting amplifier is shown, the technique is equally applicable to inverter stages.

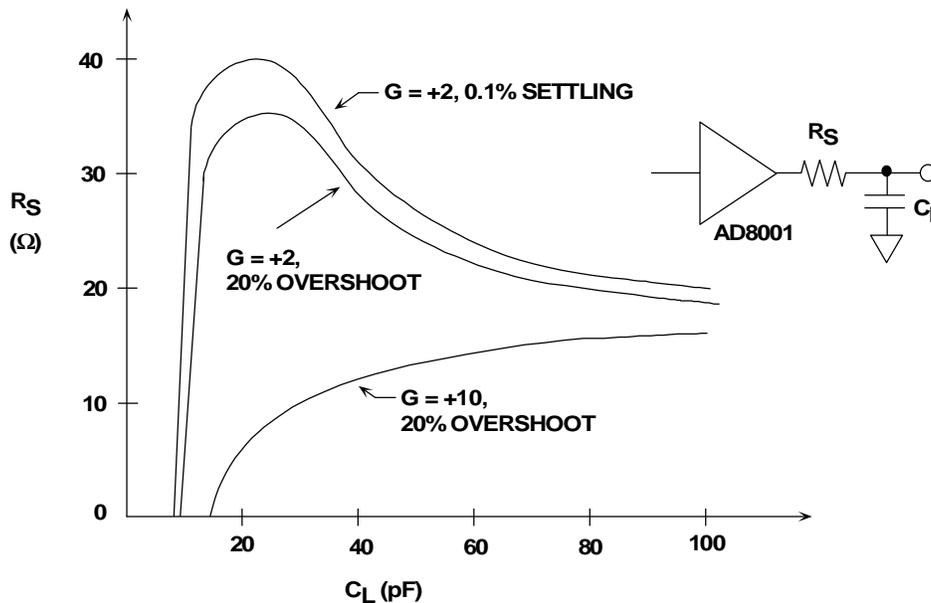
With very high speed amplifiers, or in applications where lowest settling time is critical, even small values of load capacitance can be disruptive to frequency response, but are nevertheless sometimes inescapable. One case in point is an amplifier used for driving ADC inputs. Since high speed ADC inputs quite often look capacitive in nature, this presents an oil/water type problem. In such cases the amplifier *must* be stable driving the capacitance, but it must also preserve its best

bandwidth and settling time characteristics. To address this type of cap load case,  $R_S$  and  $C_L$  performance data for a specified settling time is most appropriate.

Some applications, in particular those that require driving the relatively high impedance of an ADC, do not have a convenient back termination resistor to dampen the effects of capacitive loading. At high frequencies, an amplifier's output impedance is rising with frequency and acts like an inductance, which in combination with  $C_L$  causes peaking or even worse, oscillation. When the bandwidth of an amplifier is an appreciable percentage of device  $F_t$ , the situation is complicated by the fact that the loading effects are reflected back into its internal stages. In spite of this, the basic behavior of most very wide bandwidth amplifiers such as the AD8001 is very similar.

In general, a small damping resistor ( $R_S$ ) placed in series with  $C_L$  will help restore the desired response (see Figure 2.7). The best choice for this resistor's value will depend upon the criterion used in determining the desired response. Traditionally, simply stability or an acceptable amount of peaking has been used, but a more strict measure such as 0.1% (or even 0.01%) settling will yield different values. For a given amplifier, a family of  $R_S - C_L$  curves exists, such as those of Figure 2.7. These data will aid in selecting  $R_S$  for a given application.

## AD8001 $R_S$ REQUIRED FOR VARIOUS $C_L$ VALUES



## 2.7

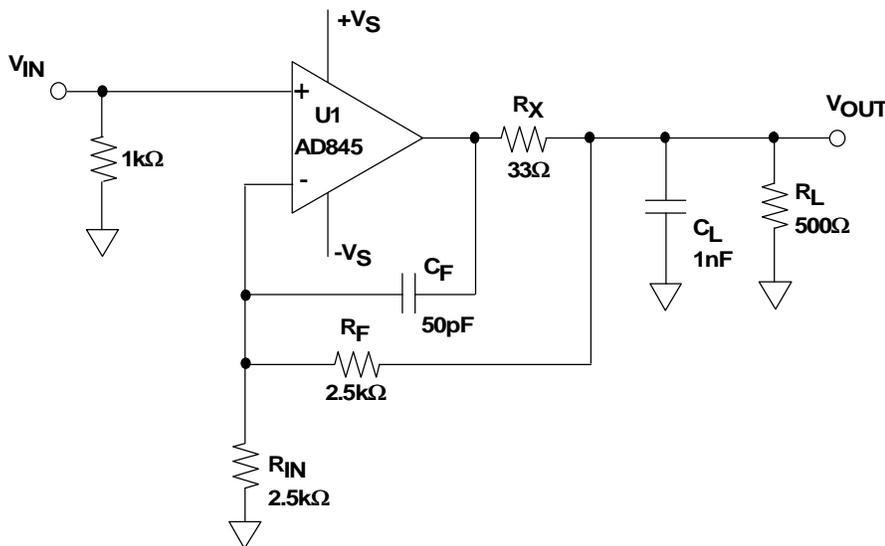
The basic shape of this curve can be easily explained. When  $C_L$  is very small, no resistor is necessary. When  $C_L$  increases to some threshold value an  $R_S$  becomes necessary. Since the frequency at which the damping is required is related to the  $R_S \cdot C_L$  time constant, the  $R_S$  needed will initially increase rapidly from zero, and then will decrease as  $C_L$  is increased further. A relatively strict requirement, such as for 0.1%, settling will generally require a larger  $R_S$  for a given  $C_L$ , giving a curve falling higher (in terms of  $R_S$ ) than that for a less stringent requirement, such as

20% overshoot. For the common gain configuration of +2, these two curves are plotted in the figure for 0.1% settling (upper-most curve) and 20% overshoot (middle curve). It is also worth mentioning that higher closed loop gains lessen the problem dramatically, and will require less  $R_S$  for the same performance. The third (lower-most) curve illustrates this, demonstrating a closed loop gain of 10  $R_S$  requirement for 20% overshoot for the AD8001 amplifier. This can be related to the earlier discussion associated with Figure 2.5.

The recommended values for  $R_S$  will optimize response, but it is important to note that generally  $C_L$  will degrade the maximum bandwidth and settling time performance which is achievable. In the limit, a large  $R_S \cdot C_L$  time constant will dominate the response. In any given application, the value for  $R_S$  should be taken as a starting point in an optimization process which accounts for board parasitics and other secondary effects.

*Active or "in-the-loop" cap load compensation can also be used as shown in Figure 2.8, and this scheme modifies the passive configuration to provide feedback correction for the DC & low frequency gain error associated with  $R_X$ . In contrast to the passive form, active compensation can only be used with voltage feedback amplifiers, because current feedback amplifiers don't allow the integrating connection of  $C_F$ .*

## ACTIVE "IN-LOOP" CAPACITIVE LOAD COMPENSATION CORRECTS FOR DC AND LF GAIN ERRORS



2.8

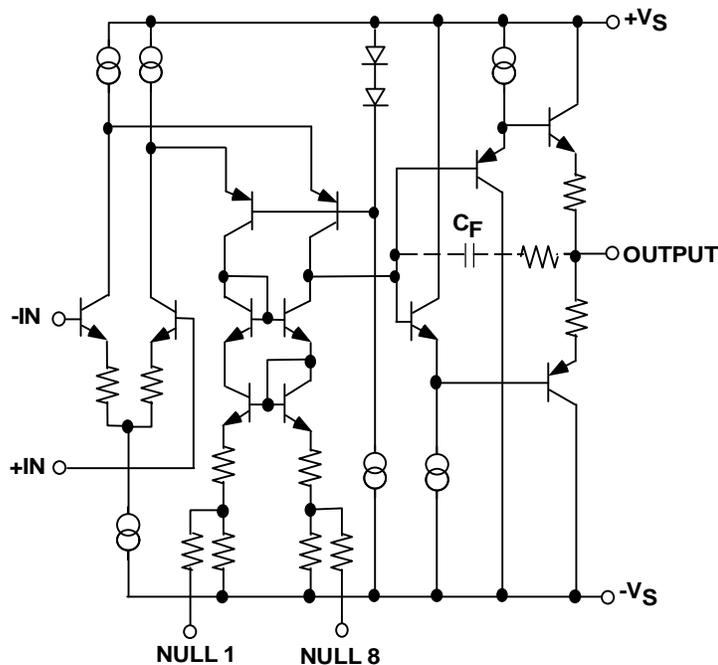
This circuit returns the DC feedback from the output side of isolation resistor  $R_X$ , thus correcting for errors. AC feedback is returned via  $C_F$ , which bypasses  $R_X/R_F$  at high frequencies. With an appropriate value of  $C_F$  (which varies with  $C_L$ , for fixed resistances) this stage can be adjusted for a well damped transient response (Reference 2,3). There is still a bandwidth reduction, a headroom loss, and also (usually) a slew rate reduction, but the DC errors can be very low. A drawback is the need to tune  $C_F$  to  $C_L$ , as even if this is done well initially, any change to  $C_L$  will

alter the response away from flat. The circuit as shown is useful for voltage feedback amplifiers only, because capacitor  $C_F$  provides integration around U1. It also can be implemented in inverting fashion, by driving the bottom end of  $R_{IN}$ .

*Internal cap load compensation involves the use of an amplifier which has topological provisions for the effects of external cap loading. To the user, this is the most transparent of the various techniques, as it works for any feedback situation, for any value of load capacitance. Drawbacks are that it produces higher distortion than does an otherwise similar amplifier without the network, and the compensation against cap loading is somewhat signal level dependent.*

The internal cap load compensated amplifier sounds at first like the best of all possible worlds, since the user need do nothing at all to set it up. Figure 2.9, a simplified diagram of an AD817 amplifier with internal cap load compensation, shows how it works. The cap load compensation is the  $C_F$ -resistor network shown around the unity gain output stage of the amplifier - note that the dotted connection of this network underscores the fact that it only makes its presence felt for certain load conditions.

## AD817 SIMPLIFIED SCHEMATIC ILLUSTRATES INTERNAL COMPENSATION FOR DRIVING CAPACITIVE LOADS



2.9

Under normal (non-capacitive or light resistive) loading, there is limited input/output voltage error across the output stage, so the  $C_F$  network then sees a relatively small voltage drop, and has little or no effect on the AD817's high impedance compensation node. However when a capacitor (or other heavy) load is present, the high currents in the output stage produce a voltage difference across the  $C_F$  network, which effectively adds capacitance to the compensation node. With this relatively heavy loading, a net larger compensation capacitance results, and reduces the amplifier speed in a manner which is adaptive to the external

capacitance,  $C_L$ . As a point of reference, note that it requires 6.3mA peak current to support a 2Vp-p swing across a 100pF load at 10MHz.

Since this mechanism is resident in the amplifier output stage and it affects the overall compensation characteristics dynamically, it acts independent of the specific feedback hookup, as well as size of the external cap loading. In other words, it can be transparent to the user in the sense that no specific design conditions need be set to make it work (other than selecting an IC which employs it). Some amplifiers using internal cap load compensation are the AD847 and the AD817, and their dual equivalents, AD827 and AD826.

There are, however, some caveats also associated with this internal compensation scheme. As with the passive compensation techniques, bandwidth decreases as the device slows down to prevent oscillation with higher load currents. Also, this adaptive compensation network has its greatest effect when enough output current flows to produce significant voltage drop across the  $C_F$  network. Conversely, at small signal levels, the effect of the network on speed is less, so greater ringing may actually be possible for some circuits for lower-level outputs.

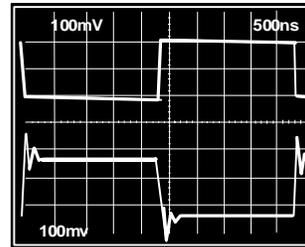
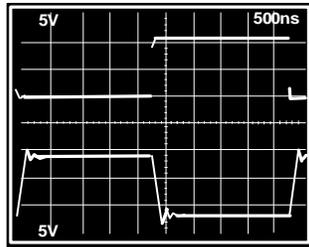
## RESPONSE OF INTERNAL CAP LOAD COMPENSATED AMPLIFIER VARIES WITH SIGNAL LEVEL

(A)  $V_{OUT} = 10V$  p-p

(B)  $V_{OUT} = 200mV$  p-p

Vertical Scale: 5V/div

Vertical Scale: 100mV/div



Horizontal Scale: 500ns/div

AD817 INVERTER

$R_F = R_{IN} = 1k\Omega$

$R_L = 1k\Omega, C_L = 1nF, V_S = \pm 15V$



2.10

The dynamic nature of this internal cap load compensation is illustrated in Figure 2.10, which shows an AD817 unity gain inverter being exercised at both high and low output levels, with common conditions of  $V_S = \pm 15V$ ,  $R_L = 1k\Omega$ ,  $C_L = 1nF$ , and using  $1k\Omega$  input/feedback resistors. In both photos the input signal is on the top trace and the output signal is on the bottom trace, and the time scale is fixed. In the 10Vp-p output (A) photo at the left, the output has slowed down appreciably to accommodate the capacitive load, but settling is still relatively clean, with a small percentage of overshoot. This indicates that for this high level case, the bandwidth reduction due to  $C_L$  is most effective. However, in the (B) photo at the right, the

200mVp-p output shows greater overshoot and ringing, for the lower level signal. The point is that the performance of the cap load compensated amplifier is signal dependent, but is always stable with any cap load.

Finally, because the circuit is based on a nonlinear principle, the internal network affects distortion performance and load drive ability, and these factors influence amplifier performance in video applications. Though the network's presence does not by any means make devices like the AD847 or AD817 unusable for video, it does not permit the very lowest levels of distortion and differential gain and phase which are achievable with otherwise comparable amplifiers (for example, the AD818 which is an AD817 without the internal compensating network).

While the individual techniques for countering cap loading outlined above have various specific tradeoffs as noted, all of the techniques have a common drawback of reducing speed (both bandwidth and slew rate). If these parameters cannot be sacrificed, then a matched transmission line system is the solution, and is discussed in more detail later in the chapter. As for choosing among the cap load compensation schemes, it would seem on the surface that amplifiers using the internal form offer the best possible solution to the problem- just pick the right amplifier and forget about it. And indeed, that would seem the "panacea" solution for all cap load situations - if you use the "right" amplifier you never need to think about cap loading again. Could there be more to it?

Yes! The "gotcha" of internal cap load compensation is subtle, and lies in the fact that the dynamic adaptive nature of the compensation mechanism actually can produce higher levels of distortion, vis-à-vis an otherwise similar amplifier, *without* the  $C_F$ -resistor network. Like the old saying about no free lunches, if you care about attaining top-notch levels of high frequency AC performance, you should give the issue of whether to use an internally compensated cap load amplifier more serious thought than simply picking a trendy device.

On the other hand, if you have no requirements for the lowest levels of distortion, then such an amplifier could be a good choice. Such amplifiers are certainly easier to use, and relatively forgiving about loading issues. Some applications of this chapter illustrate the distortion point specifically, quoting performance in a driver circuit with/without the use of an internal cap load compensated amplifiers.

## **CABLE DRIVERS AND RECEIVERS**

High quality video signals are best transmitted over terminated coaxial cable having a controlled characteristic impedance. The characteristic impedance is given by the equation  $Z_0 = \sqrt{L/C}$  where L is the distributed inductance per foot, and C is the distributed capacitance per foot. Popular values are 50, 75, and 93 or 100Ω.

If a length of coaxial cable is terminated, it presents a *resistive* load to the driver. If left unterminated, however, it may present a predominately capacitive load to the driver depending on the output frequency. If the length of an unterminated cable is much less than the wavelength of the output frequency of the driver, then the load appears approximately as a lumped capacitance. For instance, at the audio frequency of 20kHz (wavelength  $\approx$  50,000 feet, or 9.5miles), a 5 foot length of unterminated 50Ω coaxial cable would appear as a lumped capacitance of

approximately 150pF (the distributed capacitance of coaxial cable is about 30pF/ft). At 100MHz (wavelength  $\approx$  10 feet), however, the unterminated coax must be treated as a transmission line in order to calculate the standing wave pattern and the voltage at the unterminated cable output.

Because of skin effect and wire resistance, coaxial cable exhibits a loss which is a function of frequency. This varies considerably between cable types. For instance the attenuation in at 100MHz of RG188A/U is 8dB/100ft, RG58/U is 5.5dB/100ft, and RG59/U 3.6dB/100ft (Reference 4).

Skin effect also affects the pulse response of long coaxial cables. The response to a fast pulse will rise sharply for the first 50% of the output swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform risetime is 30 times greater than the 0 to 50% risetime when the cable is skin effect limited (see Reference 5).

## DRIVING CABLES

- **All Interconnections are Really Transmission Lines Which Have a Characteristic Impedance (Even if Not Controlled)**
- **The Characteristic Impedance is Equal to  $\sqrt{L/C}$ , where L and C are the Distributed Inductance and Capacitance**
- **Correctly Terminated Transmission Lines Have Impedances Equal to Their Characteristic Impedance**
- **Unterminated Transmission Lines Behave Approximately as Lumped Capacitance if the Wavelength of the Output Frequency is Much Greater than the Length of the Cable**
  - ◆ **Example: At 20kHz (Wavelength = 9.5 miles), 5 feet of Unterminated 50 $\Omega$  Cable (30pF/ft) Appears Like 150pF Load**
  - ◆ **Example: At 100MHz (Wavelength = 10 feet), 5 feet of 50 $\Omega$  Cable Must be Properly Terminated to Prevent Reflections and Standing Waves!!!!**

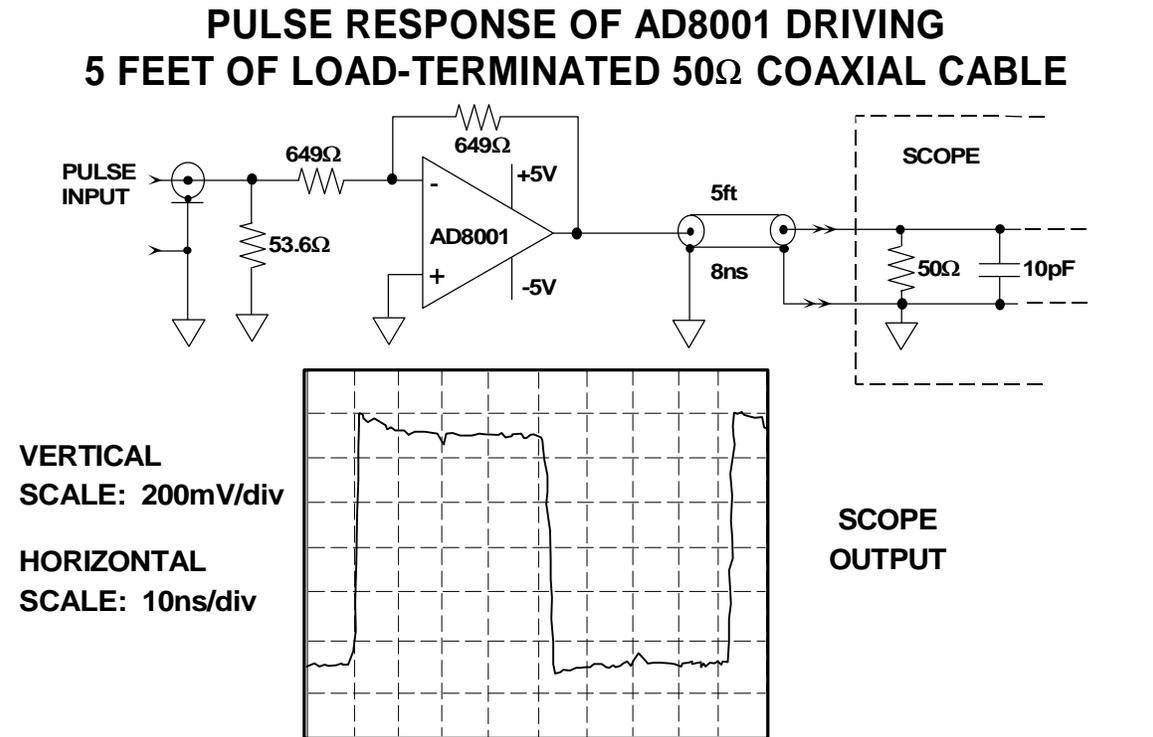


## 2.11

It is useful to examine what happens for conditions of proper and improper cable source/load terminations. To illustrate the behavior of a high speed op amp driving a coaxial cable, consider the circuit of Figure 2.12. The AD8001 drives 5 feet of 50 $\Omega$  coaxial cable which is load-end terminated in the characteristic impedance of 50 $\Omega$ . No termination is used at the amplifier (driving) end. The pulse response is also shown in the figure.

The output of the cable was measured by connecting it directly to the 50 $\Omega$  input of a 500MHz Tektronix 644A digitizing oscilloscope. The 50 $\Omega$  resistor termination is

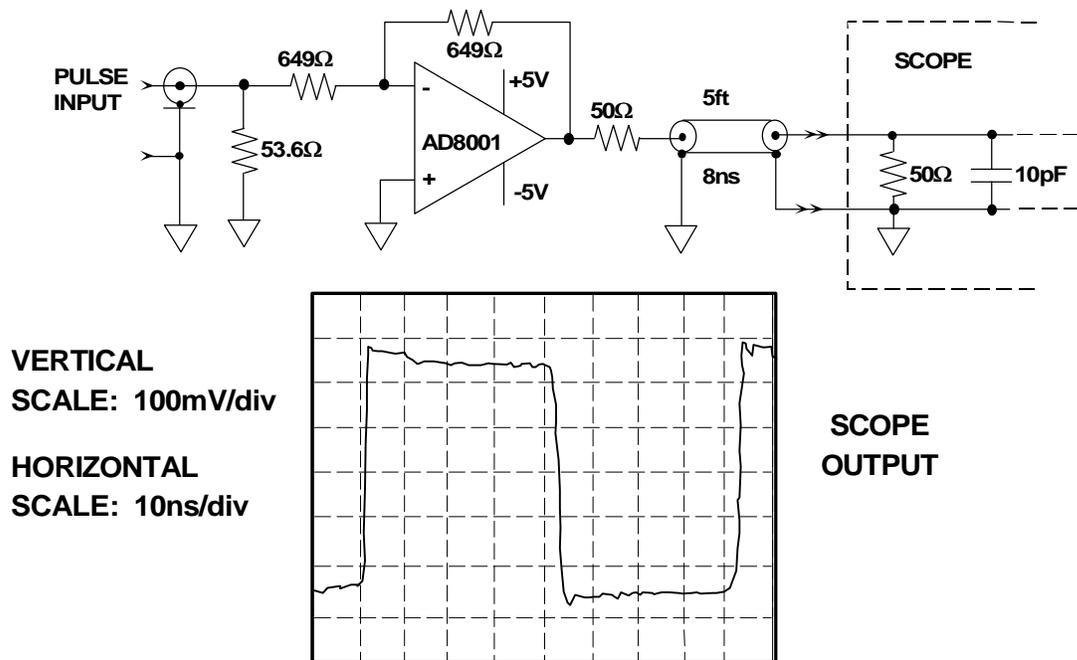
actually the input of the scope. The  $50\Omega$  load is not a perfect termination (the scope input capacitance is about  $10\text{pF}$ ), so some of the pulse is reflected out of phase back to the source. When the reflection reaches the op amp output, it sees the closed-loop output impedance of the op amp which, at  $100\text{MHz}$ , is approximately  $100\Omega$ . Thus, it is reflected back to the load with no phase reversal, accounting for the negative-going "blip" which occurs approximately  $16\text{ns}$  after the leading edge. This is equal to the round-trip delay of the cable ( $2 \cdot 5\text{ft} \cdot 1.6\text{ ns/ft} = 16\text{ns}$ ). In the frequency domain (not shown), the cable mismatch will cause a loss of bandwidth flatness at the load.



2.12

Figure 2.13 shows a second case, the results of driving the same coaxial cable, but now used with both a  $50\Omega$  source-end as well as a  $50\Omega$  load-end termination. This case is the preferred way to drive a transmission line, because a portion of the reflection from the load impedance mismatch is absorbed by the amplifier's source termination resistor. The disadvantage is that there is a  $2\times$  gain reduction, because of the voltage division between the equal value source/load terminations. However, a major positive attribute of this configuration, with matched source and load terminations in conjunction with a low-loss cable, is that the best bandwidth flatness is ensured, especially at lower operating frequencies. In addition, the amplifier is operated under near optimum loading conditions, i.e., a resistive load.

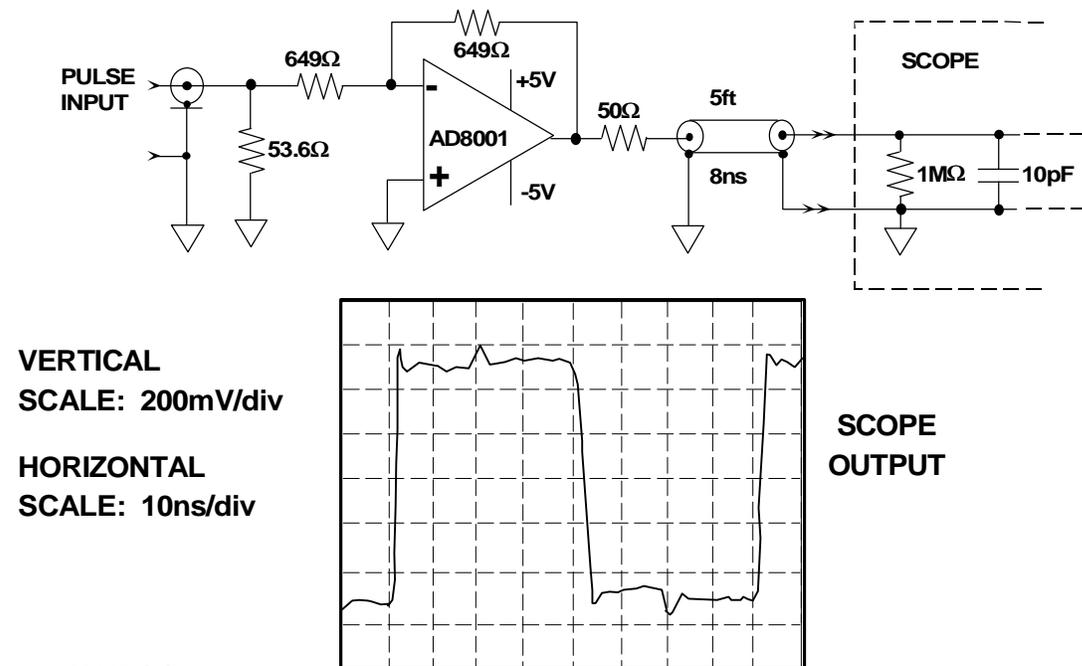
## PULSE RESPONSE OF AD8001 DRIVING 5 FEET OF SOURCE AND LOAD-TERMINATED 50Ω COAXIAL CABLE



**2.13**

Source-end (only) terminations can also be used as shown in Figure 2.14, where the op amp is source terminated by the 50Ω resistor which drives the cable. The scope is set for 1MΩ input impedance, representing an approximate open circuit. The initial leading edge of the pulse at the op amp output sees a 100Ω load (the 50Ω source resistor in series with the 50Ω coax impedance). When the pulse reaches the load, a large portion is reflected in phase because of the high load impedance, resulting in a full-amplitude pulse at the load. When the reflection reaches the source-end of the cable, it sees the 50Ω source resistance in series with the op amp closed loop output impedance (approximately 100Ω at the frequency represented by the 2ns risetime pulse edge). The reflected portion remains in phase, and appears at the scope input as the positive-going "blip" approximately 16ns after the leading edge.

## PULSE RESPONSE OF AD8001 DRIVING 5 FEET OF SOURCE-TERMINATED 50Ω COAXIAL CABLE

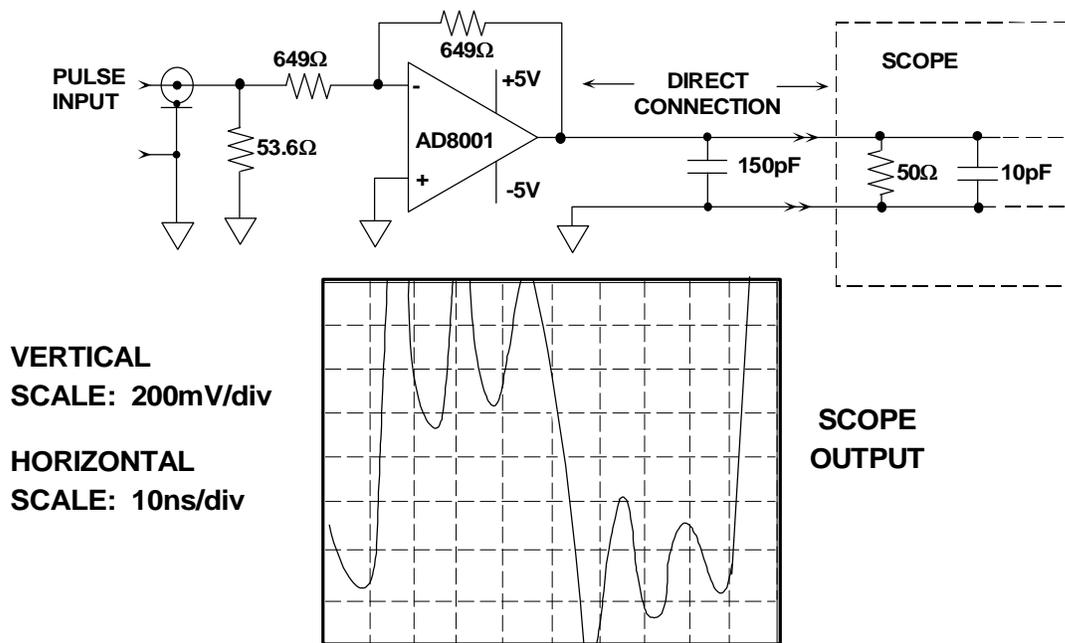


2.14

From these experiments, one can easily see that the preferred method for minimum reflections (and therefore maximum bandwidth flatness) is to use both source and load terminations and try to minimize any reactance associated with the load. The experiments represent a worst-case condition, where the frequencies contained in the fast edges are greater than 100MHz. (Using the rule-of-thumb that bandwidth =  $0.35/\text{risetime}$ ). At video frequencies, either load-only, or source-only terminations may give acceptable results, but the data sheet should always be consulted to determine the op amp's closed-loop output impedance at the maximum frequency of interest. A major disadvantage of the source-only termination is that it requires a truly high impedance load (high resistance and minimal parasitic capacitance) for minimum absorption of energy. It also places a burden on this amplifier to maintain a low output impedance at high frequencies.

Now, for a truly worst case, let us replace the 5 feet of coaxial cable with an uncontrolled-impedance cable (one that is largely capacitive with little inductance). Let us use a capacitance of 150pF to simulate the cable (corresponding to the total capacitance of 5 feet of coaxial cable whose distributed capacitance is about 30pF/foot). Figure 2.15 shows the output of the AD8001 driving a lumped 160pF capacitance (including the scope input capacitance of 10pF). Notice the overshoot and ringing on the pulse waveform due to the capacitive loading. This example illustrates the need to use good quality controlled-impedance coaxial cable in the transmission of high frequency signals.

## PULSE RESPONSE OF AD8001 DRIVING 160pF || 50Ω LOAD

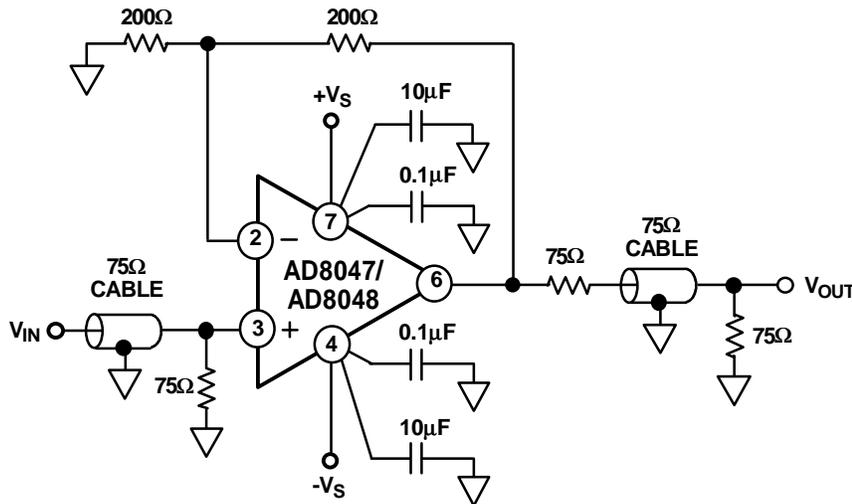


2.15

## A HIGH PERFORMANCE VIDEO LINE DRIVER

The AD8047 and AD8048 VFB op amps have been optimized to offer outstanding performance as video line drivers. They utilized the "quad core"  $g_m$  stage as previously described for high slew rate and low distortion. The AD8048 (optimized for  $G = +2$ ) has a differential gain of 0.01% and a differential phase of  $0.02^\circ$ , making it suitable for HDTV applications. In the configuration shown in Figure 2.16, the 0.1dB bandwidth is 50MHz for  $\pm 5V$  supplies, slew rate is  $1000V/\mu s$ , and 0.1% settling time is 13ns. Total quiescent current is 6mA ( $\pm 5V$ ), and quiescent power dissipation 60mW.

**VIDEO LINE DRIVER USING AD8047/AD8048:**  
 $\Delta G = 0.01\%$ ,  $\Delta\phi = 0.02^\circ$ , 50MHz 0.1dB BANDWIDTH, 6mA ( $\pm 5V$ )



2.16

## DIFFERENTIAL LINE DRIVERS/RECEIVERS

Many applications require gain/phase matched complementary or differential signals. Among these are analog-digital-converter (ADC) input buffers, where differential operation can provide lower levels of 2nd harmonic distortion for certain converters. Other uses include high frequency bridge excitation, and drivers for balanced transmission twisted pair lines such as in ADSL and HDSL.

The transmission of high quality signals across noisy interfaces (either between individual PC boards or between racks) has always been a challenge to design engineers. Differential techniques using high common-mode-rejection-ratio (CMRR) instrumentation amplifiers largely solves the problem at low frequencies.

At audio frequencies, transformers, or products such as the SSM-2142 balanced line driver and SSM-2141/SSM-2143 line receiver offer outstanding CMRRs and the ability to transmit low-level signals in the presence of large amounts of noise. At high frequencies, small toroid transformers using bifilar windings are effective.

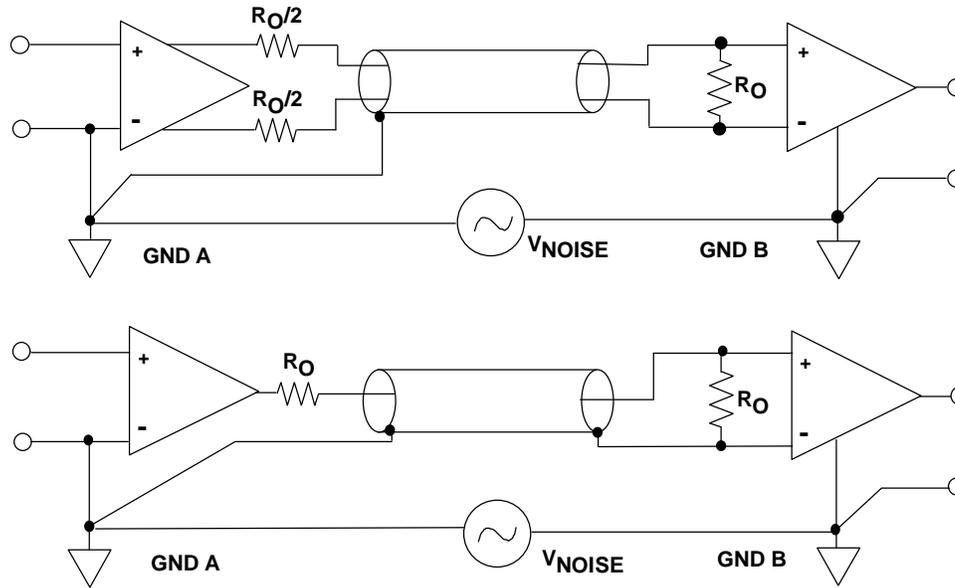
The problem of signal transmission at video frequencies is complex. Transformers are not effective, because the baseband video signal has low-frequency components down to a few tens of Hz. Video signals are generally single-ended, and therefore don't adapt easily to balanced transmission line techniques. In addition, shielded twin-conductor coaxial cable with good bandwidth is usually somewhat bulky and expensive. Finally, designing high bandwidth, low distortion differential video drivers and receivers with high CMRRs at high frequencies is an extremely difficult task.

Even with the above problems, there are differential techniques available now which offer distinct advantages over single-ended methods. Some of these techniques make

use of discrete components, while others utilize the latest in state-of-the-art video differential amplifiers.

Two solutions to the problem of differential transmission and reception are shown in Figure 2.17. The first represents the ideal case, where a balanced differential line driver drives a balanced twin-conductor coaxial cable which in turn drives a differential line receiver. This circuit, however, is difficult to implement fully at video frequencies for the reasons previously discussed.

## TWO APPROACHES FOR DIFFERENTIAL LINE DRIVING/RECEIVING



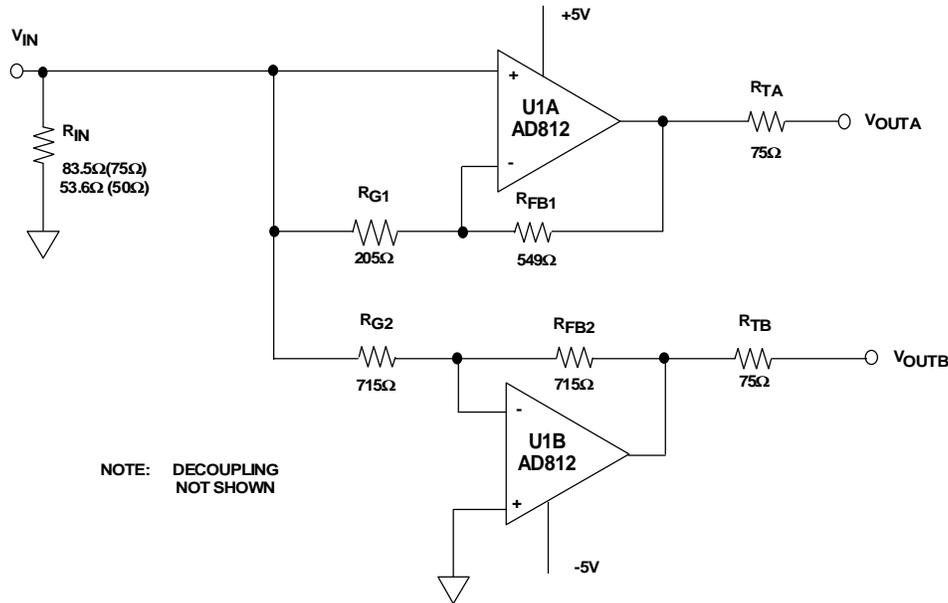
2.17

The second and most often used approach makes use of a single-ended driver which drives a source-terminated coaxial cable. The shield of the coaxial cable is grounded at the transmitting end. At the receiving end, the coaxial cable is terminated in its characteristic impedance, but the shield is left floating in order to prevent a ground loop between the two systems. The common mode ground noise is rejected by the CMRR of the differential line receiver. The success of this approach depends upon the characteristics of the line receiver.

### **Inverter-Follower Differential Driver**

The circuit of Figure 2.18 is useful as a high speed differential driver for driving high speed 10-12 bit ADCs, differential video lines, and other balanced loads at levels of 1-4V<sub>rms</sub>. As shown it operates from  $\pm 5V$  supplies, but it can also be adapted to supplies in the range of  $\pm 5$  to  $\pm 15V$ . When operated directly from  $\pm 5V$  as here, it minimizes potential for destructive ADC overdrive when higher supply voltage buffers drive a  $\pm 5V$  powered ADC, in addition to minimizing driver power.

## DIFFERENTIAL DRIVER USING INVERTER/FOLLOWER



### 2.18

In many of these differential drivers the performance criteria is high. In addition to low output distortion, the two signals should maintain gain/phase flatness. In this topology, two sections of an AD812 dual current feedback amplifier are used for the channel A & B buffers, U1A & U1B. This can provide inherently better open-loop bandwidth matching than the use of two singles (where bandwidth varies between devices from different manufacturing lots).

The two buffers here operate with precise gains of  $\pm 1$ , as defined by their respective feedback and input resistances. Channel B buffer U1B is conventional, and uses a matched pair of 715 $\Omega$  resistors- the value for using the AD812 on  $\pm 5V$  supplies.

In channel A, non-inverting buffer U1A has an inherent signal gain of 1, by virtue of the bootstrapped feedback network  $R_{FB1}$  and  $R_{G1}$  (Reference 5). It also has a higher noise gain, for phase matching. Normally a current feedback amplifier operating as a simple unity gain follower would use one (optimum) resistor  $R_{FB1}$ , and no gain resistor at all. Here, with input resistor  $R_{G1}$  added, a U1A noise gain like that of U1B results. Due to the bootstrap connection of  $R_{FB1}$ - $R_{G1}$ , the signal gain is maintained at unity. Given the matched open loop bandwidths of U1A and U1B, similar noise gains in the A-B channels provide closely matched output bandwidths between the driver sides, a distinction which greatly impacts overall matching performance.

In setting up a design for the driver, the effects of resistor gain errors should be considered for  $R_{G2}$ - $R_{FB2}$ . Here a worst case 2% mis-match will result in less than 0.2dB gain error between channels A and B. This error can be improved simply by specifying tighter resistor ratio matching, avoiding trimming.

If desired, phase matching is trimmed via  $R_{G1}$ , so that the phase of channel A closely matches that of B. This can be done for new circuit conditions, by using a pair of closely matched (0.1% or better) resistors to sum the A and B channels, as  $R_{G1}$  is adjusted for the best null conditions at the sum node. The A-B gain/phase matching is quite effective in this driver, with test results of the circuit as shown 0.04dB and  $0.1^\circ$  between the A and B output signals at 10MHz, when operated into dual 150Ω loads. The 3dB bandwidth of the driver is about 60MHz.

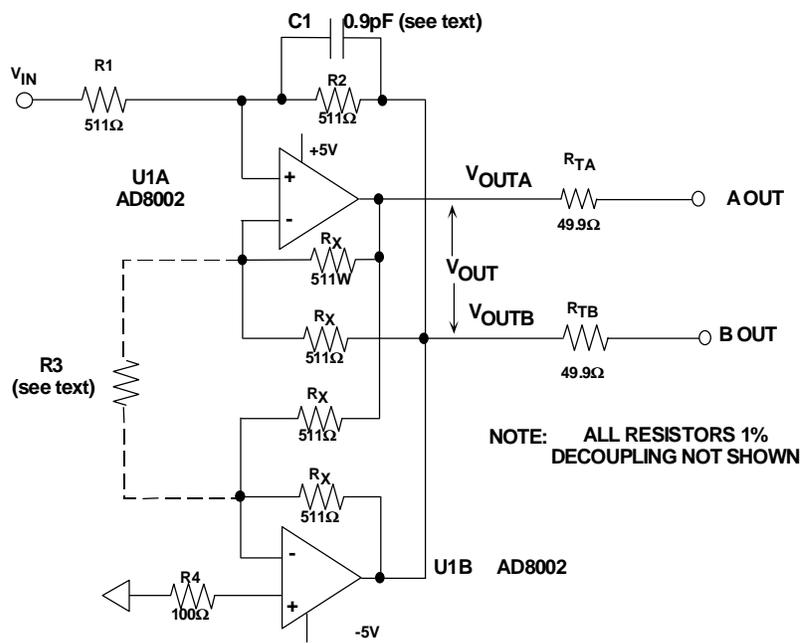
Net input impedance of the circuit is set to a standard line termination value such as 75Ω (or 50Ω), by choosing  $R_{IN}$  so that the desired value results with  $R_{IN}$  in parallel with  $R_{G2}$ . In this example, an  $R_{IN}$  value of 83.5Ω provides a standard input impedance of 75Ω when paralleled with 715Ω. For the circuit just as shown, dual voltage feedback amplifier types with sufficiently high speed and low distortion can also be used. This allows greater freedom with regard to resistor values using such devices as the AD826 and AD828.

Gain of the circuit can be changed if desired, but this is not totally straightforward. An easy step to satisfy diverse gain requirements is to simply use a triple amplifier such as the AD813, with the third channel as a variable gain input buffer.

### Cross-Coupled Differential Driver

Another differential driver approach uses cross-coupled feedback to get very high CMR and complementary outputs at the same time. In Figure 2.19, by connecting AD8002 dual current feedback amplifier sections as cross-coupled inverters, their outputs are forced equal and opposite, assuring zero output common mode voltage.

## CROSS-COUPLED DIFFERENTIAL DRIVER PROVIDES BALANCED OUTPUTS AND 250MHz BANDWIDTH



2.19

The gain cell which results, U1A and U1B plus cross-coupling resistances  $R_X$ , is fundamentally a differential input and output topology, but it behaves as a voltage feedback amplifier with regard to the feedback port at the U1A (+) node. The gain of the stage from  $V_{IN}$  to  $V_{OUT}$  is:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2R_2}{R_1}$$

where  $V_{OUT}$  is the differential output, equal to  $V_{OUTA} - V_{OUTB}$ .

This relationship may not be obvious, so it can be derived as follows:

Using the conventional inverting op amp gain equation, the input voltage  $V_{IN}$  develops an output voltage  $V_{OUTB}$  given by:

$$V_{OUTB} = -V_{IN} \frac{R_2}{R_1}.$$

Also,  $V_{OUTA} = -V_{OUTB}$ ,

because  $V_{OUTA}$  is inverted by U1B.

However,  $V_{OUT} = V_{OUTA} - V_{OUTB} = -2V_{OUTB}$ .

Therefore,

$$V_{OUT} = -2\left(-V_{IN} \frac{R_2}{R_1}\right) = 2V_{IN} \frac{R_2}{R_1}, \text{ and}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{2R_2}{R_1}.$$

This circuit has some unique benefits. First, differential gain is set by a single resistor ratio, so there is no necessity for side-side resistor matching with gain changes, as is the case for conventional differential amplifiers (see line receivers, below). Second, because the (overall) circuit emulates a voltage feedback amplifier, these gain resistances are not as restrictive as in the case of a conventional current feedback amplifier. Thus, they are not highly critical as to value as long as the equivalent resistance seen by U1A is reasonably low ( $\leq 1\text{k}\Omega$  in this case). Third, the cell bandwidth can be optimized to the desired gain by a single optional resistor,  $R_3$ , as follows. If for instance, a net gain of 20 is desired ( $R_2/R_1=10$ ), the bandwidth would otherwise be reduced by roughly this amount, since without  $R_3$ , the cell operates with a constant gain-bandwidth product (working in the voltage feedback mode). With  $R_3$  present however, advantage can be taken of the AD8002 current feedback amplifier characteristics. Additional internal gain is added by the connection of  $R_3$ , which, given an appropriate value, effectively raises gain-bandwidth to a level so as to restore the bandwidth which would otherwise be lost by the higher closed loop gain.

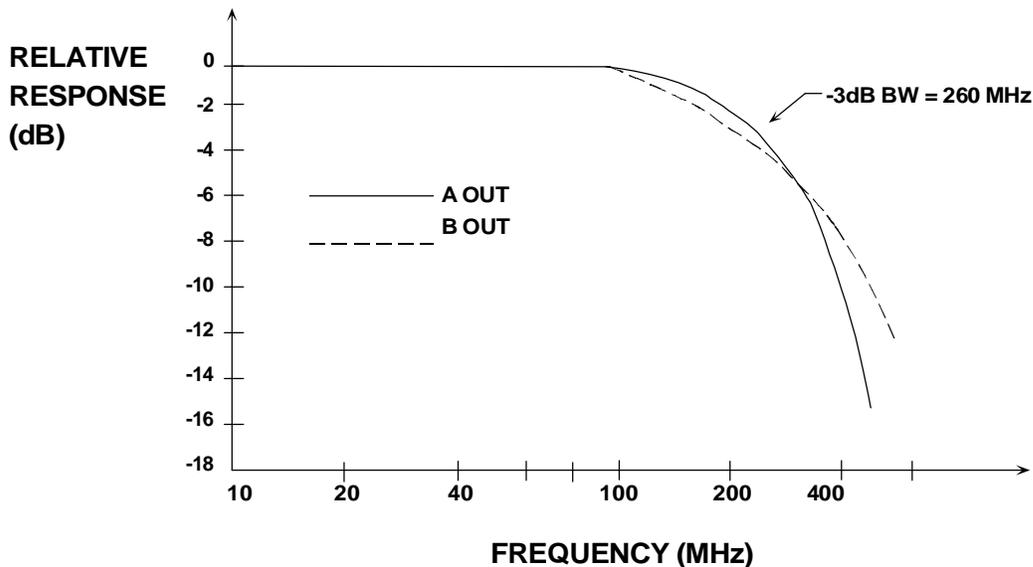
In the circuit as shown, no R3 is necessary at the low working gain of 2 times differential, since the 511Ω R<sub>X</sub> resistors are already optimized for maximum bandwidth. Note that these four matched R<sub>X</sub> resistances are somewhat critical, and will change in absolute value with the use of another current feedback amplifier. At higher gain closed loop gains as set by R2/R1, R3 can be chosen to optimize the working transconductance in the input stages of U1A and U1B, as follows:

$$R3 \cong \frac{R_x}{(R2/R1) - 1}$$

As in any high speed inverting feedback amplifier, a small high-Q chip type feedback capacitance, C1, may be needed to optimize flatness of frequency response. In this example, a 0.9pF value was found optimum for minimizing peaking. In general, provision should be made on the PC layout for an NPO chip capacitor in the range of 0.5-2pF. This capacitor is then value selected at board characterization for optimum frequency response.

For the dual trace, 1-500MHz swept frequency response plot of Figure 2.20, output levels were 0dBm into matched 50Ω loads, through back termination resistances R<sub>TA</sub> and R<sub>TB</sub>, at V<sub>OUTA</sub> and V<sub>OUTB</sub>. In this plot the vertical scale is 2dB/div, and it shows the 3dB bandwidth of the driver measuring about 250MHz, with peaking about 0.1dB. The four R<sub>X</sub> resistors along with R<sub>TA</sub> and R<sub>TB</sub> control low frequency amplitude matching, which was within 0.1dB in the lab tests, using 511Ω 1% resistor types. For tightest amplitude matching, these resistor ratios can be more closely controlled.

### FREQUENCY RESPONSE OF AD8002 CROSS-COUPLED DRIVER IS >250MHz (C1 = 0.9pF ± 0.1pF)



## 2.20

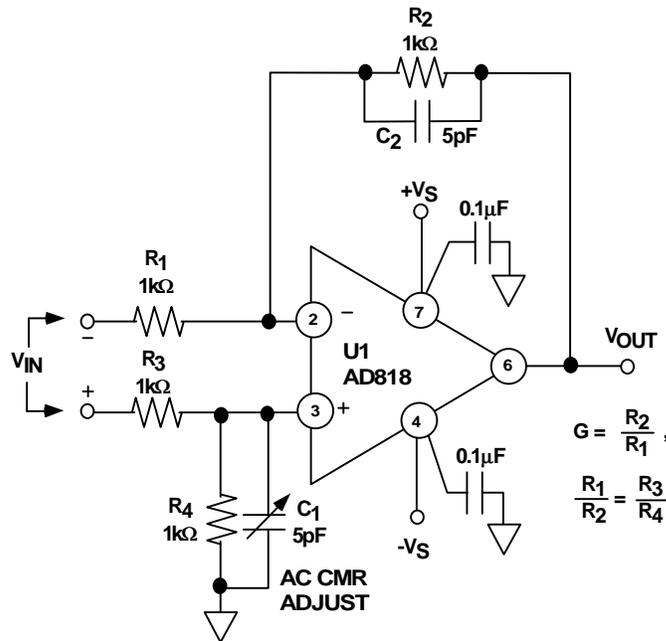
Due to the high gain-bandwidths involved with the AD8002, the construction of this circuit should follow RF rules, with the use of a ground plane, chip bypass capacitors

of zero lead length at the  $\pm 5V$  supply pins, and surface mount resistors for lowest inductance.

#### 4 Resistor Differential Line Receiver

Figure 2.21 shows a low cost, medium performance line receiver using a high speed op amp rated for video use. It is actually a standard 4 resistor difference amplifier optimized for high speed, with a differential to single-ended gain of  $R_2/R_1$ . Using low value, DC accurate/AC trimmed resistances for  $R_1$ - $R_4$  and a high speed, high CMR op amp provides the good performance.

### SIMPLE VIDEO LINE RECEIVER USING THE AD818 OP AMP



## 2.21

Practically speaking however, at low frequencies resistor matching can be more critical to overall CMR than the rated CMR of the op amp. For example, the worst case CMR (in dB) of this circuit due to resistor mismatch is:

$$\text{CMR} = 20 \log_{10} \left( \frac{1 + \frac{R_2}{R_1}}{4K_r} \right).$$

In this expression the term “ $K_r$ ” is a single resistor tolerance in fractional form (1%=0.01, etc.), and it is assumed the amplifier has significantly higher CMR ( $\geq 100\text{dB}$ ). Using discrete 1% metal films for  $R_1/R_2$  and  $R_3/R_4$  yields a worst case CMR of 34dB, 0.1% types 54dB, etc. Of course 4 random 1% resistors will on the average yield a CMR better than 34dB, but not dramatically so. A single substrate dual matched pair thin film network is preferred, for reasons of best noise rejection and simplicity. One type suitable is the Ohmtek 1005, (Reference 6) which has a ratio match of 0.1%, which will provide a worst case low frequency CMR of 66 dB.

This circuit has an interesting and desirable side property. Because of the resistors it divides down the input voltage, and the amplifier is protected against overvoltage. This allows CM voltages to exceed  $\pm 5V$  supply rails in some cases without hazard. For operation with  $\pm 15V$  supplies, inputs should not exceed the supply rails.

At frequencies above 1MHz, the bridge balance is dominated by AC effects, and a C1-C2 capacitive balance trim should be used for best performance. The C1 adjustment is intended to allow this, providing for the cancellation of stray layout capacitance(s) by electrically matching the net C1-C2 values. In a given PC layout with low and stable parasitic capacitance, C1 is best adjusted once in 0.5pF increments, for best high frequency CMR. Using designated PC pads, production values then would use the trimmed value. Good AC matching is essential to achieving good CMR at high frequencies. C1-C2 should be types similar physically, such as NPO (or other stable) ceramic chip style capacitors.

While the circuit as shown has unity gain, it can be gain-scaled in discrete steps, as long as the noted resistor ratios are maintained. In practice, this means using taps on a multi-ratio network for gain change, so as to raise both R2 and R4, in identical proportions. There is no other simple way to change gain in this receiver circuit. Alternately, a scheme for continuous gain control without interaction with CMR is to follow this receiver with a scaling amplifier/driver with adjustable gain. The similar AD828 dual amplifier allows this with the addition of only two resistors.

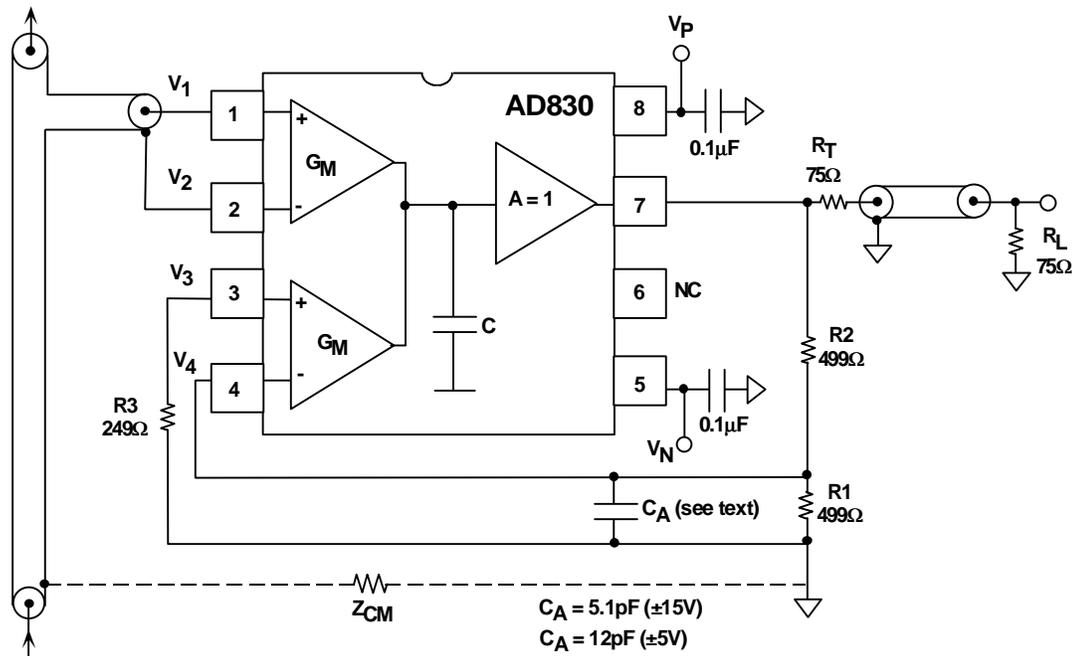
Video gain/phase performance of this stage is dependent upon the device used for U1 and the operating supply voltages. Suitable voltage feedback amplifiers work best at supplies of  $\pm 10 - \pm 15V$ , which maximizes op amp bandwidth. And, while many high speed amplifiers function in this circuit, those expressly designed with low distortion video operation perform best. The circuit as shown can be used with supplies of  $\pm 5$  to  $\pm 15V$ , but lowest NTSC video distortion occurs for supplies of  $\pm 10V$  or more, where differential gain/differential phase errors are less than 0.01%/0.05°. Operating at  $\pm 5V$  supplies, the distortion rises somewhat, but the lowest power drain of 70mW occurs.

One drawback to this circuit is that it does load a 75 $\Omega$  video line to some extent, and so should be used with this loading taken into account. On the plus side, it has wide dynamic range for both signal and CM voltages, plus the inherent overvoltage protection.

### **Active Feedback Differential Line Receiver**

Fully integrating the line receiver function eliminates the resistor-related drawbacks of the 4 resistor line receiver, improving CMR performance, ease of use, and overall circuit flexibility. An IC designed for this function is the AD830 active feedback amplifier (Reference 7,8). Its use as a differential line receiver with gain is illustrated in Figure 2.22.

## VIDEO LOOP-THROUGH CONNECTION USING THE AD830



### 2.22

The AD830 operates as a feedback amplifier with two sets of fully differential inputs, available at pins 1-2 and 3-4, respectively. Internally, the outputs of the two stages are summed and drive a buffer output stage. Both input stages have high CMR, and can handle differential signals up to  $\pm 2V$ , and CM voltages can range up to  $-V_S+3V$  or  $+V_S-2.1V$ , with a  $\pm 1V$  differential input applied. While the AD830 does not normally need protection against CM voltages, if sustained transient voltage beyond the rails is encountered, an optional pair of equal value ( $\cong 200\Omega$ ) resistances can be used in series with pins 1-2.

In this device the overall feedback loop operates so that the differential voltages  $V_{1-2}$  and  $V_{3-4}$  are forced to be equal. Feedback is taken from the output back to one input differential pair, while the other pair is driven by a differential input signal. An important point of this architecture is that high CM rejection is provided by the two differential input pairs, so CMR isn't dependent on resistor bridges and their associated matching problems. The inherently wideband balanced circuit and the quasi-floating operation of the driven input provide the high CMR, which is typically 100dB at DC.

The general expression for the U1 stage's gain "G" is like a non-inverting op amp, or:

$$G = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R2}{R1}$$

For lowest DC offset, balancing resistor R3 is used (equal to  $R1 \parallel R2$ ).

In this example of a video "loop-through" connection, the input signal tapped from a coax line and applied to one input stage at pins 1-2, with the scaled output signal

tied to the second input stage between pins 3-4. With the R1-R2 feedback attenuation of 2/1, the net result is that the output of U1, is then equal to  $2 \cdot V_{IN}$ , i.e., a gain of 2.

Functionally, the input and local grounds are isolated by the CMR of the AD830, which is typically 75dB at frequencies below 1MHz, 60dB at 4.43MHz, and relatively supply independent.

With the addition of an output source termination resistor  $R_T$ , this circuit has an overall loaded gain of unity at the load termination,  $R_L$ . It is a ground isolating video repeater, driving the terminated 75 $\Omega$  output line, delivering a final output equal to the original input,  $V_{IN}$ .

NTSC video performance will be dependent upon supplies. Driving a terminated line as shown, the circuit has optimum video distortion levels for  $V_S = \pm 15V$ , where differential gain is typically 0.06%, and differential phase 0.08°. Bandwidth can be optimized by the optional 5.1pF (or 12pF) capacitor,  $C_A$ , which allows a 0.1dB bandwidth of 10MHz with  $\pm 15V$  operation. The differential gain and phase errors are about 2 $\times$  at  $\pm 5V$ .

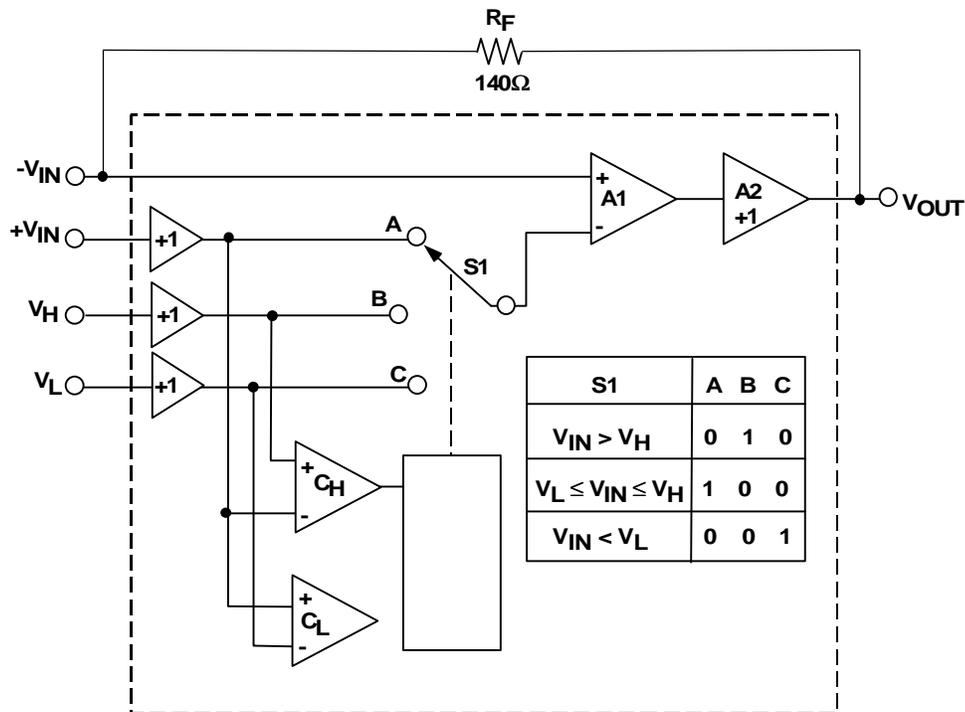
## HIGH SPEED CLAMPING AMPLIFIERS

There are many situations where it is desirable to clamp the output of an op amp to prevent overdriving the circuitry which follows. Specially designed high speed, fast recovery clamping amplifiers offer an attractive alternative to designing external clamping/protection circuits. The AD8036/AD8037 low distortion, wide bandwidth clamp amplifiers represent a significant breakthrough in this technology. These devices allow the designer to specify a high ( $V_H$ ) and low ( $V_L$ ) clamp voltage. The output of the device clamps when the input exceeds either of these two levels. The AD8036/AD8037 offer superior clamping performance compared to competing devices that use output-clamping. Recovery time from overdrive is less than 5ns.

The key to the AD8036 and AD8037's fast, accurate clamp and amplifier performance is their proprietary input clamp architecture. This new design reduces clamp errors by more than 10x over previous output clamp based circuits, as well as substantially increasing the bandwidth, precision, and versatility of the clamp inputs.

Figure 2.23 is an idealized block diagram of the AD8036 connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200V/ $\mu$ s, 240MHz high voltage gain, differential to single-ended amplifier) and A2 (a  $G=+1$  high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater.

## AD8036/AD8037 CLAMP AMPLIFIER EQUIVALENT CIRCUIT



### 2.23

The input clamp section is comprised of comparators  $C_H$  and  $C_L$ , which drive switch  $S1$  through a decoder. The unity-gain buffers in series with the  $+V_{IN}$ ,  $V_H$ , and  $V_L$  inputs isolate the input pins from the comparators and  $S1$  without reducing bandwidth or precision.

The two comparators have about the same bandwidth as  $A1$  (240MHz), so they can keep up with signals within the useful bandwidth of the AD8036. To illustrate the operation of the input clamp circuit, consider the case where  $V_H$  is referenced to +1V,  $V_L$  is open, and the AD8036 is set for a gain of +1 by connecting its output back to its inverting input through the recommended 140Ω feedback resistor. Note that the main signal path always operates closed loop, since the clamping circuit only affects  $A1$ 's noninverting input.

If a 0V to +2V voltage ramp is applied to the AD8036's  $+V_{IN}$  for the connection just described,  $V_{OUT}$  should track  $+V_{IN}$  perfectly up to +1V, then should limit at exactly +1V as  $+V_{IN}$  continues to +2V.

In practice, the AD8036 comes close to this ideal behavior. As the  $+V_{IN}$  input voltage ramps from zero to 1V, the output of the high limit comparator  $C_H$  starts in the off state, as does the output of  $C_L$ . When  $+V_{IN}$  just exceeds  $V_H$  (practically, by about 18mV),  $C_H$  changes state, switching  $S1$  from "A" to "B" reference level. Since the + input of  $A1$  is now connected to  $V_H$ , further increases in  $+V_{IN}$  have no effect on the AD8036's output voltage. The AD8036 is now operating as a unity-gain buffer for the  $V_H$  input, as any variation in  $V_H$ , for  $V_H > 1V$ , will be faithfully produced at  $V_{OUT}$ .

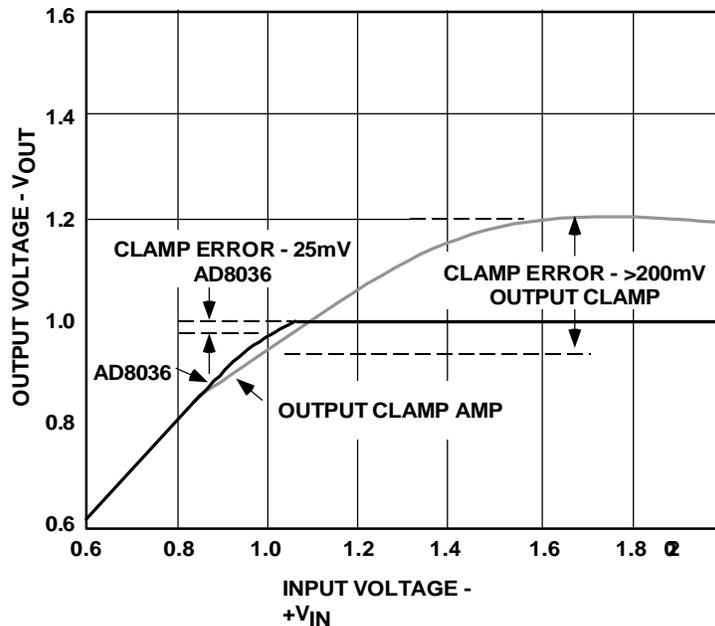
Operation of the AD8036 for negative input voltages and negative clamp levels on  $V_L$  is similar, with comparator  $C_L$  controlling  $S1$ . Since the comparators see the

voltage on the  $+V_{IN}$  pin as their common reference level, the voltage  $V_H$  and  $V_L$  are defined as "High" or "Low" with respect to  $+V_{IN}$ . For example, if  $V_{IN}$  is set to zero volts,  $V_H$  is open, and  $V_L$  is +1V, comparator  $C_L$  will switch S1 to "C", so the AD8036 will buffer the voltage on  $V_L$  and ignore  $+V_{IN}$ .

The performance of the AD8036/AD8037 closely matches the ideal just described. The comparator's threshold extends from 60mV inside the clamp window defined by the voltages on  $V_L$  and  $V_H$  to 60mV beyond the window's edge. Switch S1 is implemented with current steering, so that A1's + input makes a continuous transition from say,  $V_{IN}$  to  $V_H$  as the input voltage traverses the comparator's input threshold from 0.9V to 1.0V for  $V_H = 1.0V$ .

The practical effect of the non-ideal operation is to soften the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the input clamping circuit. Figure 2.24 is a graph of  $V_{OUT}$  versus  $V_{IN}$  for the AD8036 and a typical output clamp amplifier. Both amplifiers are set for  $G=+1$  and  $V_H = +1V$ .

## COMPARISON BETWEEN INPUT AND OUTPUT CLAMPING



2.24

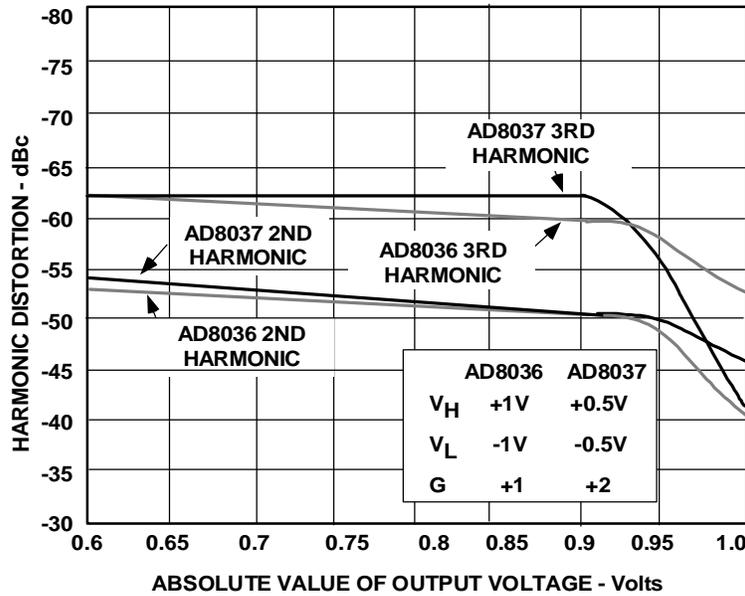
The worst case error between  $V_{OUT}$  (ideally clamped) and  $V_{OUT}$  (actual) is typically 18mV times the amplifier closed-loop gain. This occurs when  $V_{IN}$  equals  $V_H$  (or  $V_L$ ). As  $V_{IN}$  goes above and/or below this limit,  $V_{OUT}$  will stay within 5mV of the ideal value.

In contrast, the output clamp amplifier's transfer curve typically will show some compression starting at an input of 0.8V, and can have an output voltage as far as 200mV over the clamp limit. In addition, since the output clamp causes the amplifier to operate open-loop in the clamp mode, the amplifier's output impedance will increase, potentially causing additional errors, and the recovery time is significantly longer.

It is important that a clamped amplifier such as the AD8036/AD8037 maintain low levels of distortion when the input signals approach the clamping voltages. Figure 2.25 shows the second and third harmonic distortion for the amplifiers as the output approaches the clamp voltages. The input signal is 20MHz, the output signal is 2V peak-to-peak, and the output load is 100Ω.

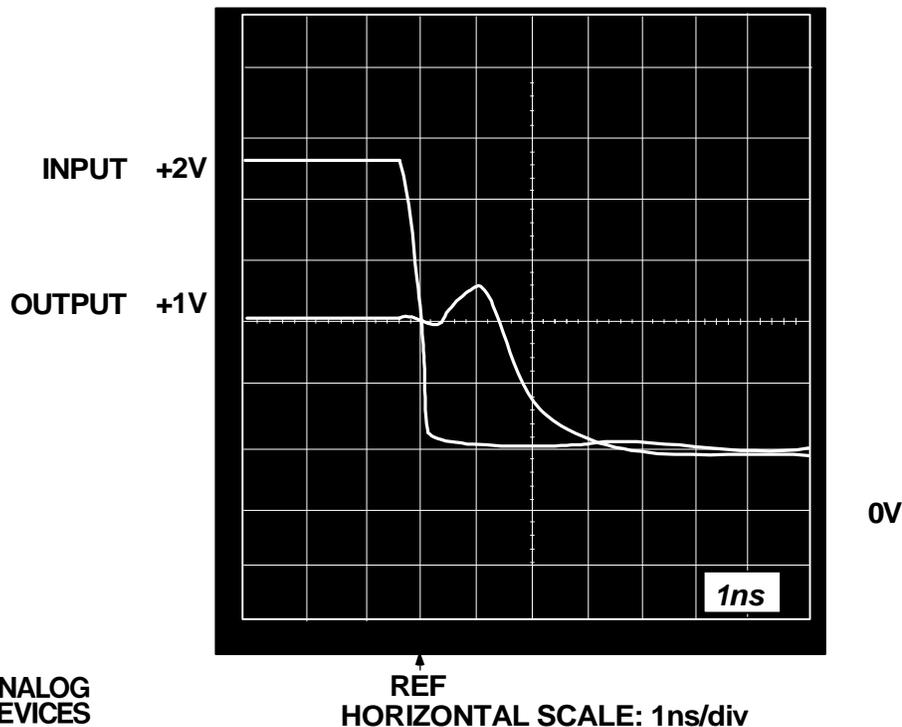
Recovery from step voltage which is two times over the clamping voltage is shown in Figure 2.26. The input step voltage starts at +2V and goes to 0V (left-hand traces on scope photo). The input clamp voltage ( $V_H$ ) is set at +1V. The right-hand trace shows the output waveform. The key specifications for the AD8036/AD8037 clamped amplifiers are summarized in Figure 2.27.

**AD8036/AD8037 DISTORTION NEAR CLAMPING REGION,  
OUTPUT = 2V p-p, LOAD = 100Ω, f = 20MHz**



2.25

## AD8036/AD8037 OVERDRIVE (2x) RECOVERY



2.26

## AD8036/AD8037 SUMMARY SPECIFICATIONS

- Proprietary Input Clamping Circuit with Minimized Nonlinear Clamping Region
- Small Signal Bandwidth: 240MHz (AD8036), 270MHz (AD8037)
- Slew Rate: 1500V/ $\mu$ s
- 1.5ns Overdrive Recovery
- Low Distortion: -72dBc @ 20MHz (500 $\Omega$  load)
- Low Noise: 4.5nv/ $\sqrt{\text{Hz}}$ , 2pA/ $\sqrt{\text{Hz}}$
- 20mA Supply Current on  $\pm$ 5V

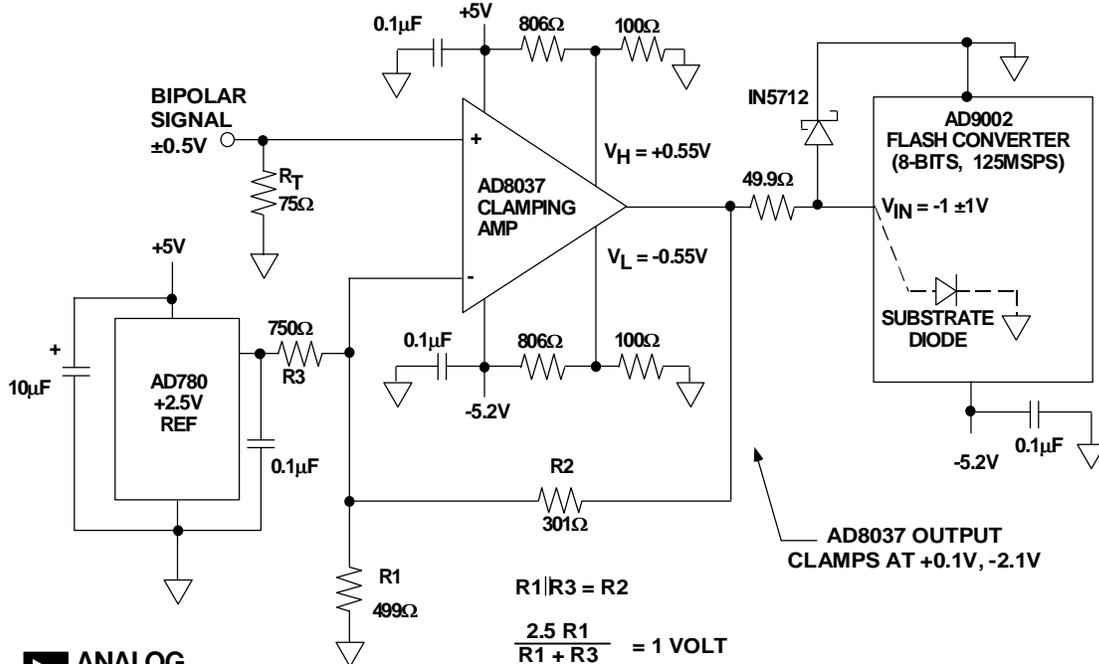


2.27

Figure 2.28 shows the AD9002 8-bit, 125MSPS flash converter driven by the AD8037 (240MHz bandwidth) clamping amplifier. The clamp voltages on the AD8037 are set to +0.55 and -0.55V, referenced to the  $\pm$ 0.5V input signal, with the external resistive dividers. The AD8037 also supplies a gain of two, and an offset of -1V (using the AD780 voltage reference), to match the 0 to -2V input range of the AD9002 flash converter. The output signal is clamped at +0.1V and -2.1V. This multi-function clamping circuit therefore performs several important functions as

well as preventing damage to the flash converter which occurs if its input exceeds +0.5V, thereby forward biasing the substrate diode. The 1N5712 Schottky diode adds further protection during power-up.

## AD9002 8-BIT, 125MSPS FLASH CONVERTER DRIVEN BY AD8037 CLAMP AMPLIFIER



2.28

The feedback resistor,  $R2 = 301\Omega$ , is selected for optimum bandwidth per the data sheet recommendation. For a gain of two, the parallel combination of  $R1$  and  $R3$  must also equal  $R2$ :

$$\frac{R1 \cdot R3}{R1 + R3} = R2 = 301\Omega$$

(nearest 1% standard resistor value).

In addition, the Thevenin equivalent output voltage of the AD780 +2.5V reference and the  $R3/R1$  divider must be +1V to provide the -1V offset at the output of the AD8037.

$$\frac{2.5 \cdot R1}{R1 + R3} = 1 \text{ volt}$$

Solving the equations yields  $R1 = 499\Omega$ ,  $R3 = 750\Omega$  (using the nearest 1% standard resistor values).

Other input and output voltages ranges can be accommodated by appropriate changes in the external resistors.

Further examples of applications of these fast clamping op amps are given in Reference 9.

## **SINGLE-SUPPLY/RAIL-TO-RAIL CONSIDERATIONS**

The market is driving high speed amplifiers to operate at lower power on lower supply voltages. High speed bipolar processes, such as Analog Devices' CB and XFCB, are basically 12V processes, and circuits designed on these processes are generally limited to  $\pm 5V$  power supplies (or less). This is ideal for high speed video, IF, and RF signals, which rarely exceed 5V peak-to-peak.

The emphasis on low power, battery-operated portable communications and instrumentation equipment has brought about the need for ICs which operate on single +5V, and +3V, and lower supplies. The term *single-supply* has various implications, some of which are often further confused by marketing hype.

There are many obvious reasons for lower power dissipation, such as the ability to function without fans, reliability issues, etc. There are, therefore, many applications for single-supply devices other than in systems which have only one supply voltage. For example, the lower power dissipation of a single-supply ADC may be the reason for its selection, rather than the fact that it requires just one supply.

There are also systems which truly operate on a single power supply. In such cases, it can often be difficult to maintain DC coupling from a transducer all the way through to the ADC. In fact, AC coupling is often used in single-supply systems, with DC restoration preceding the ADC. This may be required to prevent the loss of dynamic range which would otherwise occur because of the need to provide adequate headroom to an AC coupled signal of arbitrary duty cycle. In the AC-coupled portions of such systems, a "false-ground" is often created, usually centered between the rails.

There are other disadvantages associated with lower power supply voltages. Signal swings are limited, therefore high-speed single-supply circuits tend to be more sensitive to corruption by wideband noise, etc. The single-supply op amp and ADC usually utilize the same power bus that supplies the digital circuits, making proper filtering and decoupling extremely critical.

In order to maximize the signal swing in single-supply circuits, it is desirable that a high speed op amp utilize as much of the supply range as possible on both the input and output. Ideally, a true *rail-to-rail* input op amp has an input common-mode range that includes both supply rails, and an output range which does likewise. This makes for some interesting tradeoffs and compromises in the circuit design of the op amp.

In many cases, an op amp may be fully specified for both dual  $\pm 5V$  and single-supply operation but neither its input nor its output can actually swing closer than about 1V to either supply rail. Such devices must be used in applications where the input and output common-mode restrictions are not violated. This generally involves offsetting the inputs using a false ground reference scheme.

To summarize, there are many tradeoffs involved in single-supply high-speed designs. In many cases, using devices specified for operation on +5V, but without true rail inclusive input/output operation can give good performance. Amplifiers are

also becoming available that are true single supply rail-to-rail devices. Understanding single-supply rail-to-rail input and output limitations is easy if you understand a few basics about the circuitry inside the op amp. We shall consider input and output stages separately.

## HIGH SPEED SINGLE SUPPLY AMPLIFIERS

- **Single Supply Offers:**
  - ◆ **Lower Power**
  - ◆ **Battery Operated Portable Equipment**
  - ◆ **Simplifies Power Supply Requirements (one voltage)**
  
- **Design Tradeoffs:**
  - ◆ **Limited Signal Swings Increase Sensitivity to Noise**
  - ◆ **Usually Share Noisy Digital Power Supply**
  - ◆ **DC Coupling Throughout is Difficult**
  - ◆ **Rail-to-Rail Input and Output Increases Signal Swing, but not Required in All Applications**
  - ◆ **Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs**

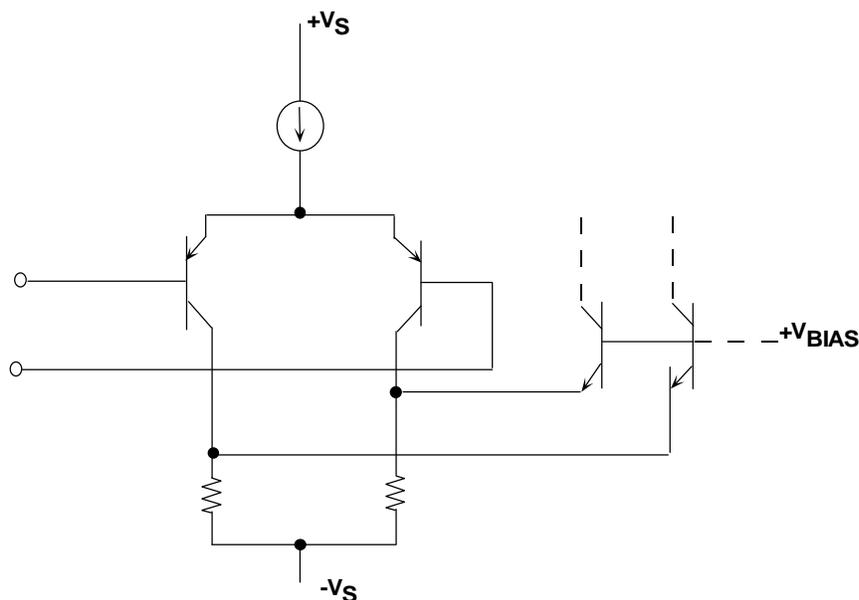


2.29

There is some demand for high-speed op amps whose input common-mode voltage includes both supply rails. Such a feature is undoubtedly useful in some applications, but engineers should recognize that there are relatively few applications where it is absolutely essential. These should be carefully distinguished from the many applications where common-mode range *close* to the supplies or one that includes one of the supplies is necessary, but input rail-to-rail operation is not.

In many single-supply applications, it is required that the input go to only one of the supply rails (usually ground). Amplifiers which will handle zero-volt inputs are relatively easily designed using PNP differential pairs (or N-channel JFET pairs) as shown in Figure 2.30 (circuit used in the AD8041, AD8042, AD8044). The input common-mode range of such an op amp extends from about 200mV below the negative supply to within about 1V of the positive supply. If the stage is designed with N-channel JFETs (AD820/AD822/AD823/AD824), the input common-mode range would also include the negative rail.

## OP90 AND OPX93 INPUT STAGE ALLOWS INPUT TO GO TO THE NEGATIVE RAIL

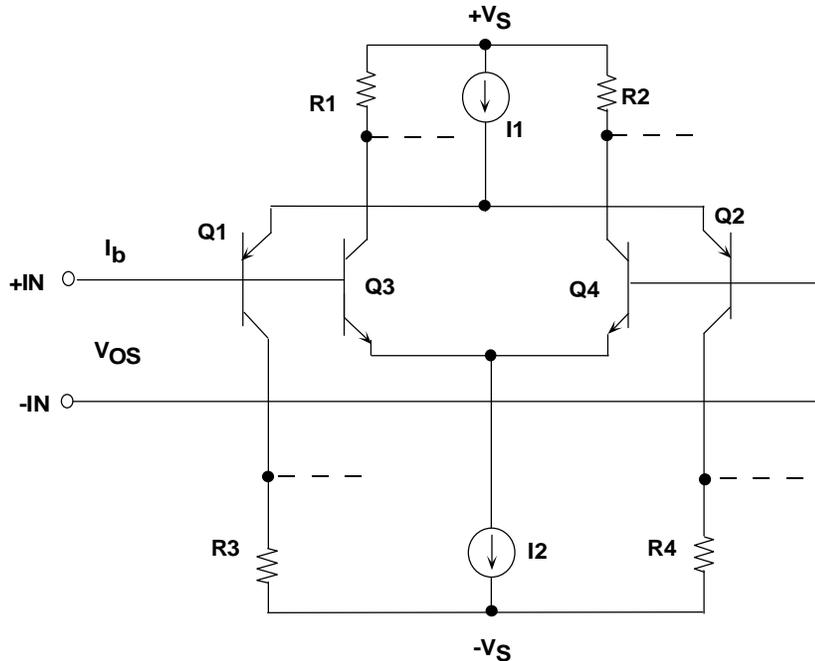


### 2.30

The input stage could also be designed with NPN transistors (or P-channel JFETs), in which case the input common-mode range would include the positive rail and to within about 1V of the negative rail; however, this requirement typically occurs in applications such as high-side current sensing, a low-frequency measurement application. The OP282/OP482 input stage uses the P-channel JFET input pair whose input common-mode range includes the positive rail.

True rail-to-rail input stages require two long-tailed pairs (see Figure 2.31), one of NPN bipolar transistors (or N-channel JFETs), the other of PNP transistors (or N-channel JFETs). These two pairs exhibit *different* offsets and bias currents, so when the applied input common-mode voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources (I1 and I2) remain active throughout the entire input common-mode range, amplifier input offset voltage is the *average* offset voltage of the NPN pair and the PNP pair. In those designs where the current sources are alternatively switched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply.

## RAIL-TO-RAIL INPUT STAGE TOPOLOGY



### 2.31

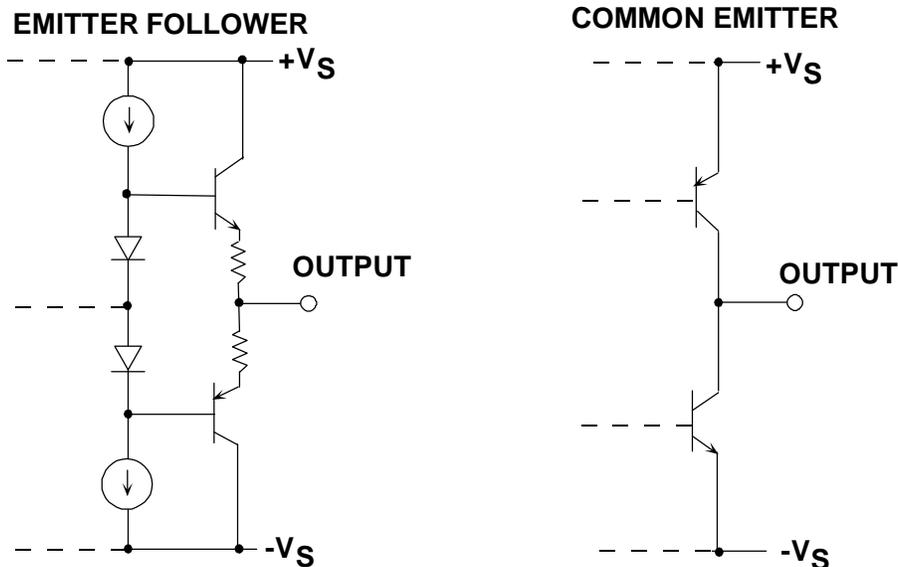
Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the common-mode input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair somewhere along the input common-mode voltage range. Devices like the AD8031/AD8032 (specified for  $\pm 5V$ ,  $+5V$ ,  $+3V$ , and  $+2.5V$ ) have a common-mode crossover threshold at approximately  $1V$  below the positive supply. The PNP differential input stage is active from about  $200mV$  below the negative supply to within about  $1V$  of the positive supply. Over this common-mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly. Also, amplifier bias currents, dominated by the PNP differential pair over most of the input common-mode range, change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

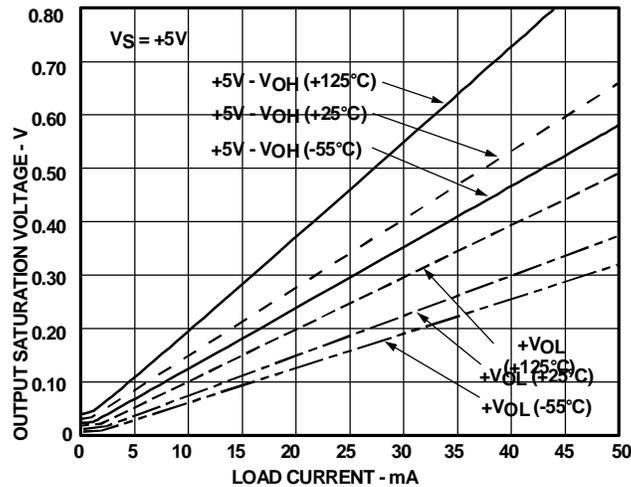
Applications which require true rail-rail inputs should therefore be carefully evaluated, and the amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable.

Figure 2.32 shows two typical high-speed op amp output stages. The emitter-follower stage is widely used, but its output voltage range is limited to within about 1V of either supply voltage. This is sufficient for many applications, but the common-emitter stage (used in the AD8041/8042/8044/8031/8032 and others) allows the output to swing to within the transistor saturation voltage,  $V_{CE(SAT)}$ , of the rails. For small amounts of load current (less than  $100\mu\text{A}$ ), the saturation voltage may be as low as 5 to 20mV, but for higher load currents, the saturation voltage can increase to several hundred millivolts (for example, 500mV at 50mA). This is illustrated in Figure 2.33 for the AD8042 (zero-volts in, rail-to-rail output). The solid curves show the output saturation voltage of the PNP transistor (output sourcing current), and the dotted curves the NPN transistor (sinking current). The saturation voltage increases with increasing temperature as would be expected.

## HIGH SPEED SINGLE SUPPLY OP AMP OUTPUT STAGES



## AD8042 OUTPUT SATURATION VOLTAGE VERSUS LOAD CURRENT



2.33

An output stage constructed of CMOS FETs can provide true rail-to-rail performance, but only under no-load conditions, and in much lower frequency amplifiers. If the output must source or sink current, the output swing is reduced by the voltage dropped across the FETs internal "on" resistance (typically  $100\Omega$ ).

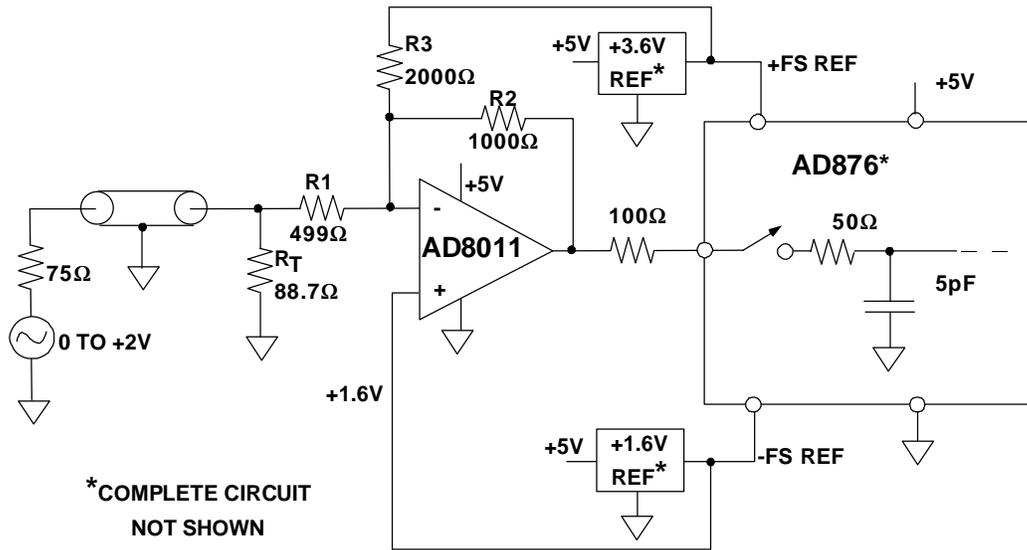
### SINGLE SUPPLY OP AMP APPLICATIONS

The following section illustrates a few applications of op amps in single-supply circuits. All of the op amps are fully specified for both  $\pm 5V$  and  $+5V$  (and  $+3V$  where the design supports it). Both rail-to-rail and non-rail-to-rail applications are shown.

#### A Single-Supply 10-bit 20MSPS ADC Direct-Coupled Driver Using the AD8011

The circuit in Figure 2.34 shows the AD8011 op amp driving the AD876 10-bit, 20MSPS ADC in a direct-coupled application. The input and output common-mode voltage of the AD8011 must lie between approximately  $+1$  and  $+4V$  when operating on a single  $+5V$  supply. The input range of the AD876 is 2V peak-to-peak centered around a common-mode value of  $+2.6V$ , well within the output voltage range of the AD8011. The upper and lower range setting voltages are  $+1.6V$  and  $+3.6V$  and are supplied externally to the AD876. They are easily derived from a resistor divider driven by a reference such as the REF198 ( $+4.096V$ ). The two taps on the resistor divider should be buffered using precision single-supply op amps such as the AD822 (dual).

## DC COUPLED SINGLE SUPPLY DRIVER FOR AD876 10-BIT, 20MSPS ADC



### 2.34

The source is represented as a 2V video signal referenced to ground. (The equivalent of a current generator of 0 to 27mA in parallel with the 75Ω source resistor. The termination resistor,  $R_T$ , is selected such that the parallel combination of  $R_T$  and  $R_1$  is 75Ω. The peak-to-peak swing at the termination resistor is 1V, so the AD8011 must supply a gain of two.

The non-inverting input of the AD8011 is biased to a common-mode voltage of +1.6V (well within its allowable common-mode range).  $R_3$  is calculated as follows:

When the source voltage is zero-volts, there is a current of 3.0mA flowing through  $R_1$  (499Ω) and into 40.6Ω to ground (the equivalent parallel combination of the 75Ω source and the 88.7Ω termination resistor is 40.6Ω). The output of the AD8011 should be +3.6V under these conditions. This means that 2mA must flow through  $R_2$ . Therefore  $R_3$  (connected to the +3.6V source) must supply 1.0mA into the summing junction (+1.6V), and therefore its value must be 2000Ω.

The input of the AD876 has a series MOSFET switch that turns on and off at the sampling frequency. This MOSFET is connected to a hold capacitor internal to the device. The on impedance of the MOSFET is about 50Ω, while the hold capacitor is about 5pF.

In a worst case condition, the input voltage to the AD876 will change by a full-scale value (2V) in one sampling cycle. When the input MOSFET turns on, the output of the op amp will be connected to the charged hold capacitor through the series resistance of the MOSFET. Without any other series resistance, the instantaneous current that flows would be 40mA. This causes settling problems for the op amp.

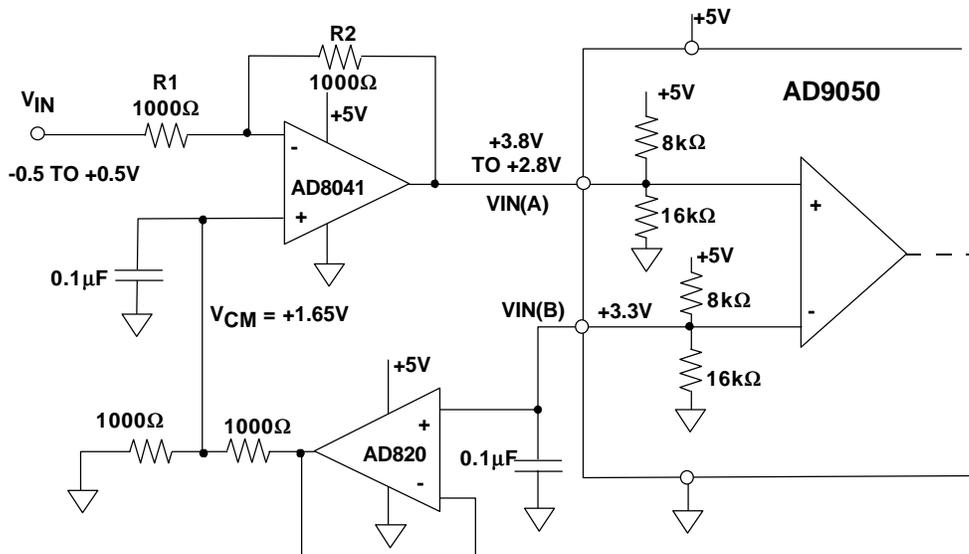
The series 100Ω resistor limits the instantaneous current to about 13mA. This resistor cannot be made too large, or the high frequency performance will be affected. In practice, the optimum value is often determined experimentally.

The sampling MOSFET of the AD876 is closed for half of each cycle (25ns when sampling at 20MSPS). Approximately 7 time constants are required for settling to 10 bits. The series 100Ω resistor along with the 50Ω on resistance and the 5pF hold capacitor form a time constant of about 750ps. These values leave a comfortable margin for settling. Overall, the AD8011 provides adequate buffering for the AD876 ADC without introducing distortion greater than that of the ADC itself.

### A 10-Bit, 40MSPS ADC Low-Distortion Single-Supply ADC Driver Using the AD8041 Op Amp

A DC coupled application which requires the rail-to-rail output capability of the AD8041 is shown in Figure 2.35 as a driver for the AD9050 10-bit, 40MSPS single-supply ADC. The input range of the AD9050 is 1V p-p centered around +3.3V. The maximum input signal is therefore +3.8V. The non-inverting input of the AD8041 is driven with a common-mode voltage of +1.65V which is derived from the unused differential input of the AD9050. This allows the op amp to act as a level shifter for the ground-referenced bipolar input 1V p-p signal, with unity gain as determined by the 1kΩ resistors, R1 and R2.

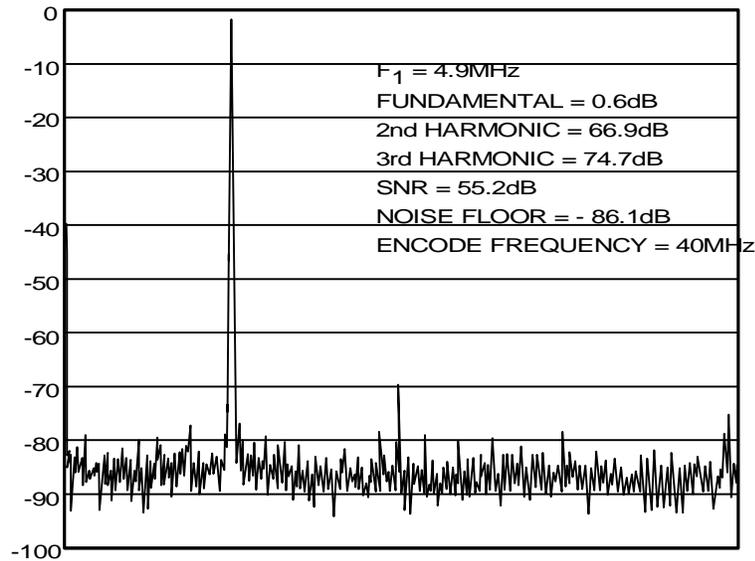
### DC COUPLED SINGLE-SUPPLY DRIVER FOR AD9050 10-BIT, 40MSPS ADC



2.35

Op amps with complementary emitter follower outputs such as the AD8011 (operating on +5V) generally will exhibit high frequency distortion for sinewaves with full-scale amplitudes of 1V p-p centered at +3.3V. Because of its common emitter output stage, however, the AD8041 is capable of driving the AD9050, while maintaining a distortion floor of greater than 66dB with a 4.9MHz fullscale input (see Figure 2.36).

## FFT OUTPUT OF AD9050 CIRCUIT WITH 4.9MHz INPUT AND 40MSPS SAMPLING FREQUENCY



2.36

### Single-Supply RGB Buffer

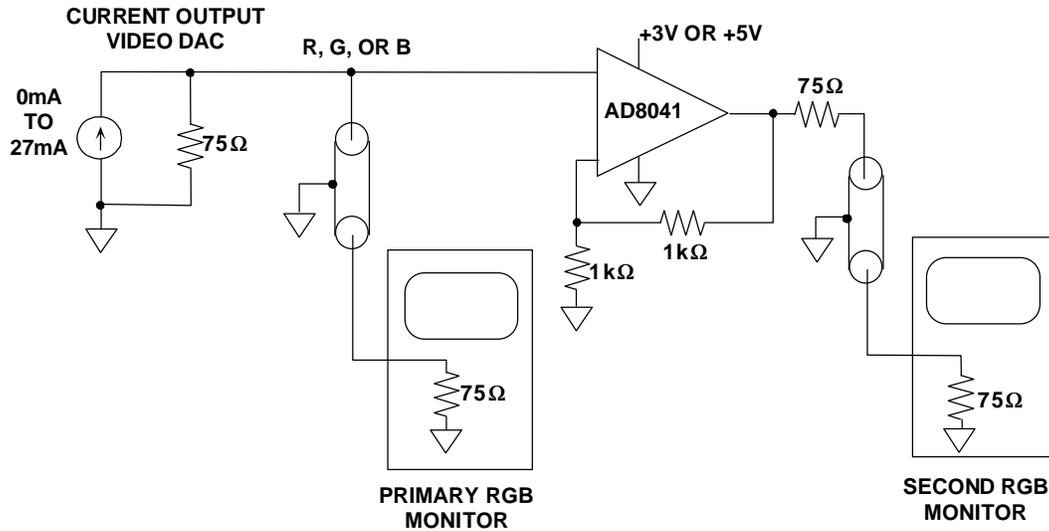
Op amps such as the AD8041/AD8042/ and AD8044 can provide buffering of RGB signals that include ground while operating from a single +3V or +5V supply. The signals that drive an RGB monitor are usually supplied by current output DACs that operate from a single +5V supply. Examples of such are triple video DACs like the ADV7120/21/22 from Analog Devices.

During the horizontal blanking interval, the current output of the DACs goes to zero, and the RGB signals are pulled to ground by the termination resistors. If more than one RGB monitor is desired, it cannot simply be connected in parallel because it will provide an additional termination. Therefore, buffering must be provided before connecting a second monitor.

Since the RGB signals include ground as part of their dynamic output range, it has previously been required to use a dual supply op amp to provide this buffering. In some systems, this is the only component that requires a negative supply, so it can be quite inconvenient to incorporate this multiple monitor feature.

Figure 2.37 shows a diagram of one channel of a single supply gain-of-two buffer for driving a second RGB monitor. No current is required when the amplifier output is at ground. The termination resistor at the monitor helps pull the output down at low voltage levels.

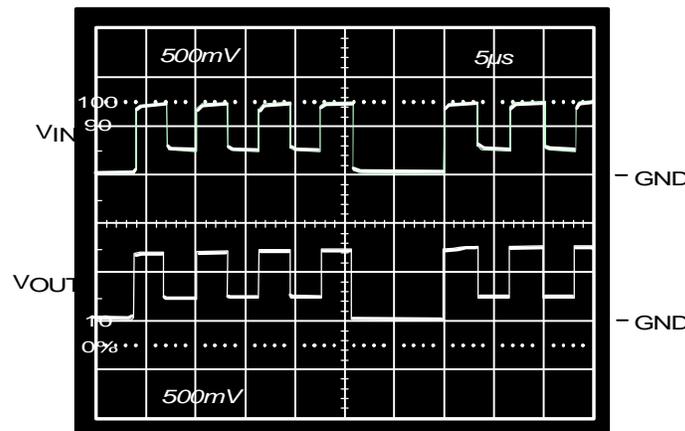
## SINGLE SUPPLY RGB BUFFER OPERATES ON +3V OR +5V



2.37

Figure 2.38 shows the output of such a buffer operating from a single +3V supply and driven by the Blue signal of a color bar pattern. Note that the input and output are at ground during the horizontal blanking interval. The RGB signals are specified to output a maximum of 700mV peak. The output of the AD8041 is +1.4V with the termination resistors providing a divide-by-two. The Red and Green signals can be buffered in the same manner with a duplication of this circuit. Another possibility is to use the quad AD8044 single-supply op amp.

### INPUT/OUTPUT OF SINGLE SUPPLY RGB BUFFER OPERATING ON +3V



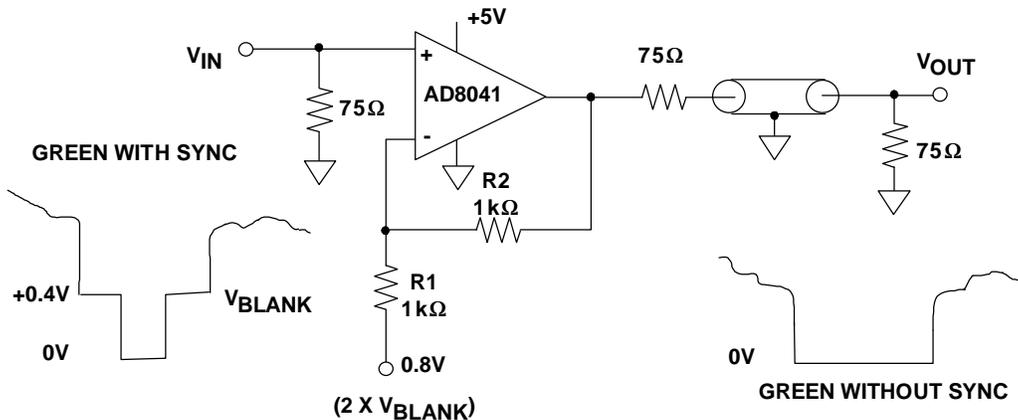
2.38

## Single-Supply Sync Stripper

Some RGB monitors use only three cables total and carry the synchronizing signals and the Green (G) signal on the same cable. The sync signals are pulses that go in the negative direction from the blanking level of the G signal.

In some applications, such as prior to digitizing component video signals with ADCs, it is desirable to remove or strip the sync portion from the G signal. Figure 2.39 is a circuit using the AD8041 running on a single +5V supply that performs this function.

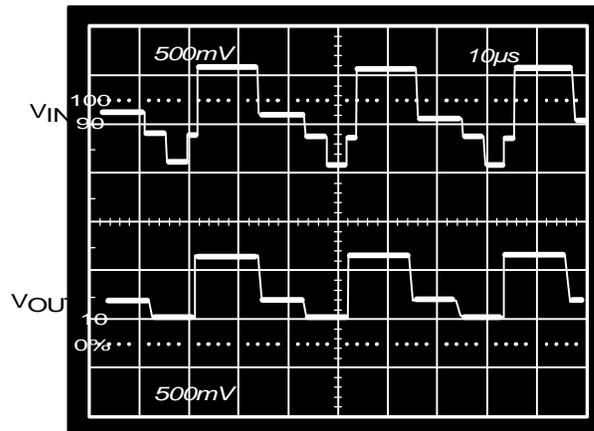
### SINGLE SUPPLY VIDEO SYNC STRIPPER



2.39

The upper waveform in Figure 2.40 shows the Green plus sync signal that is output from an ADV7120, a single supply triple video DAC. Because the DAC is single supply, the lowest level of the sync tip is at ground or slightly above. The AD8041 is set from a gain of two to compensate for the divide-by-two of the output terminations. The reference voltage for  $R1$  should be twice the DC blanking level of the G signal. If the blanking level is at ground and the sync tip is negative, as in some dual supply systems, then  $R1$  can be tied to ground. In either case, the output will have the sync removed and have the blanking level at ground.

## INPUT/OUTPUT OF SINGLE SUPPLY SYNC STRIPPER



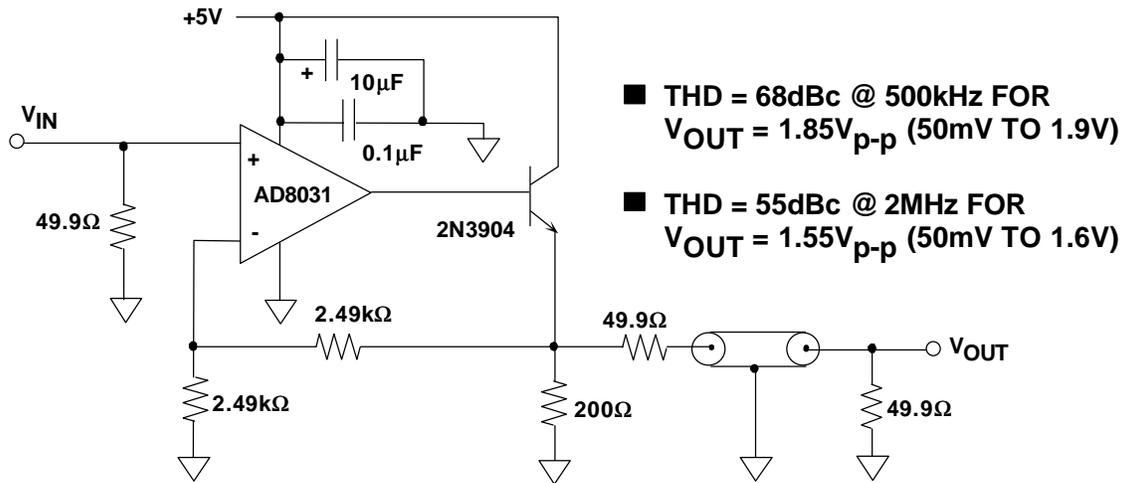
2.40

### **A Single-Supply Video Line Driver with Zero-Volt Output, Eamon Nash**

When operated with a single supply, the AD8031 80MHz rail-to-rail voltage feedback op amp has optimum distortion performance when the signal has a common mode level of  $V_s/2$ , and when there is about 500mV of headroom to each rail. If low distortion is required for signals which swing close to ground, an emitter follower can be used at the op amp output.

Figure 2.41 shows the AD8031 configured as a single supply gain-of-two line driver. With the output driving a back terminated  $50\Omega$  line, the overall gain is unity from  $V_{in}$  to  $V_{out}$ . In addition to minimizing reflections, the  $50\Omega$  back termination resistor protects the transistor from damage if the cable is short circuited. The emitter follower, which is inside the feedback loop, ensures that the output voltage from the AD8031 stays about 700mV above ground. Using this circuit excellent distortion is obtained even when the output signal swings to within 50mV of ground. The circuit was tested at 500kHz and 2MHz using a single +5V supply. For the 500kHz signal, THD was 68dBc with a peak-to-peak swing at  $V_{out}$  of 1.85V (50mV to +1.9V). This corresponds to a signal at the emitter follower output of 3.7V p-p (100mV to 3.8V). Data was taken with an output signal of 2MHz, and a THD of 55dBc was measured with a  $V_{out}$  of 1.55V p-p (50mV to 1.6V).

## LOW DISTORTION ZERO-VOLT OUTPUT SINGLE SUPPLY LINE DRIVER USING AD8031



### 2.41

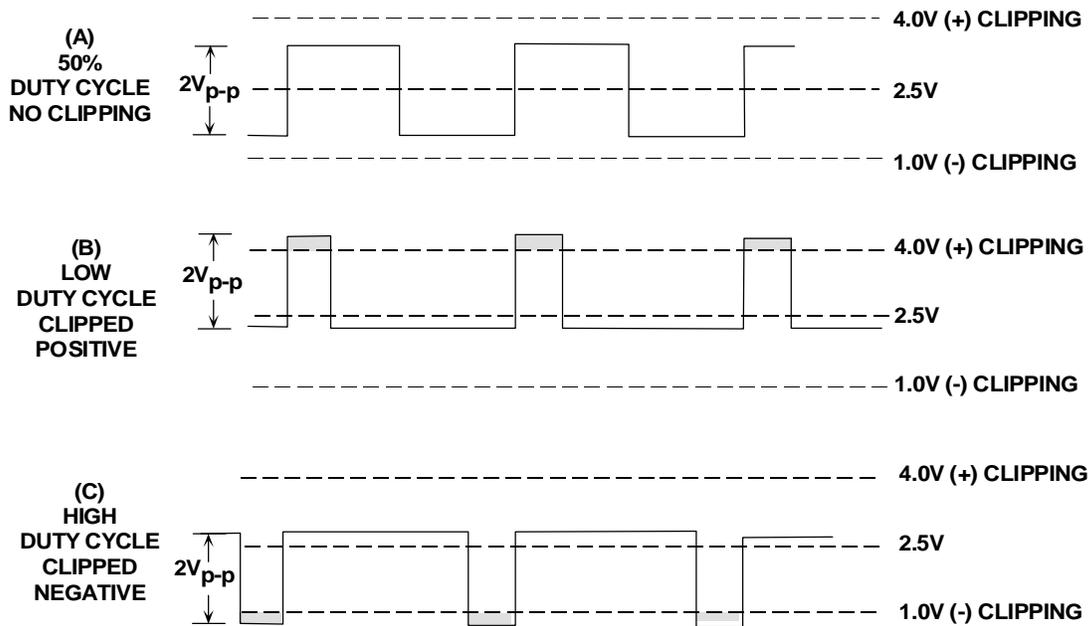
This circuit can also be used to drive the analog input of a single supply high speed ADC whose input voltage range is ground-referenced. In this case, the emitter of the external transistor is connected directly to the ADC input. A peak positive voltage swing of approximately 3.8V is possible before significant distortion begins to occur.

### Headroom Considerations in AC-Coupled Single-Supply Circuits

The AC coupling of arbitrary waveforms can actually introduce problems which don't exist at all in DC coupled or DC restored systems. These problems have to do with the waveform duty cycle, and are particularly acute with signals which approach the rails, as they can in low supply voltage systems which are AC coupled.

In Figure 2.42 (A), an example of a 50% duty cycle square wave of about 2V<sub>p-p</sub> level is shown, with the signal swing biased symmetrically between the upper and lower clip points of a 5V supply amplifier. Assume that the amplifier has a complementary emitter follower output and can only swing to the limited DC levels as marked, about 1V from either rail. In cases (B) and (C), the duty cycle of the input waveform is adjusted to both low and high duty cycle extremes *while maintaining the same peak-to-peak input level*. At the amplifier output, the waveform is seen to clip either negative or positive, in (B) and (C), respectively.

## WAVEFORM DUTY CYCLE TAXES HEADROOM IN AC COUPLED AMPLIFIERS

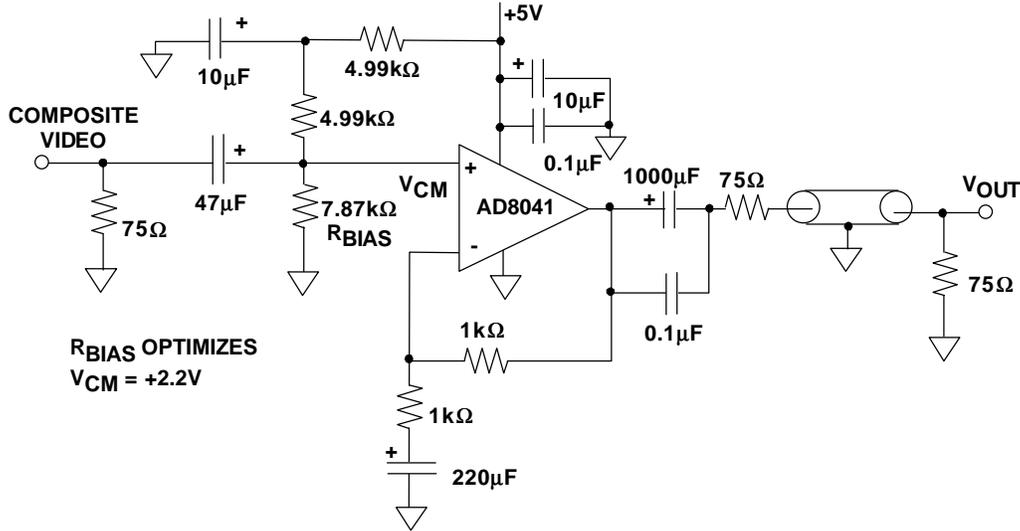


**2.42**

Since standard video waveforms *do* vary in duty cycle as the scene changes, the point is made that low distortion operation on AC coupled single supply stages must take the duty cycle headroom degradation effect into account. If a stage has a 3Vp-p output swing available before clipping, and it must cleanly reproduce an *arbitrary* waveform, then the maximum allowable amplitude is less than 1/2 of this 3Vp-p swing, that is <math><1.5\text{Vp-p}</math>. An example of violating this criteria is the 2Vp-p waveform of Figure 2.42, which is clipping for both the high and low duty cycles. Note that the criteria set down above is based on avoiding hard clipping, while subtle distortion increases may in fact take place at lower levels. This suggests an even more conservative criteria for lowest distortion operation such as composite NTSC video amplifiers.

Figure 2.43 shows a single supply gain-of-two composite video line driver using the AD8041. Since the sync tips of a composite video signal extend below ground, the input must be AC coupled and shifted positively to prevent clipping during negative excursions. The input is terminated in  $75\Omega$  and AC coupled via the  $47\mu\text{F}$  to a voltage divider that provides the DC bias point to the input. Setting the optimal common-mode bias voltage requires some understanding of the nature of composite video signals and the video performance of the AD8041.

## SINGLE SUPPLY AC COUPLED COMPOSITE VIDEO LINE DRIVER HAS $\Delta G = 0.06\%$ AND $\Delta\phi = 0.06^\circ$



**2.43**

As discussed above, signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capability than their peak-to-peak amplitude after AC coupling. As a worst case, the dynamic signal swing required will approach twice the peak-to-peak value. The two bounding cases are for a duty cycle that is mostly low, but occasionally goes high at a fraction of a percent duty cycle, and vice versa.

Composite video is not quite this demanding. One bounding extreme is for a signal that is mostly black for an entire frame, but occasionally has a white (full intensity), minimum width spike at least once per frame.

The other extreme is for a video signal that is full white everywhere. The blanking intervals and sync tips of such a signal will have negative going excursions in compliance with composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at its highest level (white) for only about 75% of the time.

As a result of the duty cycle variations between the two extremes presented above, a 1V p-p composite video signal that is multiplied by a gain-of-two requires about 3.2V p-p of dynamic voltage swing at the output for the op amp to pass a composite video signal of arbitrary duty cycle without distortion.

The AD8041 not only has ample signal swing capability to handle the dynamic range required, but also has excellent differential gain and phase when buffering these signals in an AC coupled configuration.

To test this, the differential gain and phase were measured for the AD8041 while the supplies were varied. As the lower supply is raised to approach the video signal, the first effect is that the sync tips become compressed before the differential gain

and phase are adversely affected. Thus, there must be adequate swing in the negative direction to pass the sync tips without compression.

As the upper supply is lowered to approach the video, the differential gain and phase were not significantly adversely affected until the difference between the peak video output and the supply reached 0.6V. Thus, the highest video level should be kept at least 0.6V below the positive supply rail.

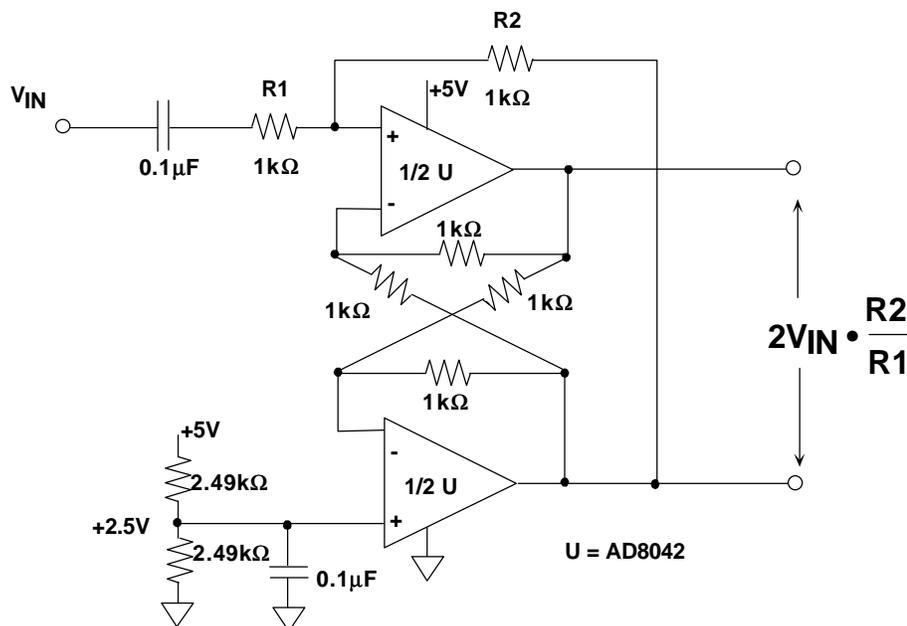
Taking the above into account, it was found that the optimal point to bias the non-inverting input was at +2.2V DC. Operating at this point, the worst case differential gain was 0.06% and the differential phase 0.06°.

The AC coupling capacitors used in the circuit at first glance appear quite large. A composite video signal has a lower frequency band edge of 30Hz. The resistances at the various AC coupling points - especially at the output - are quite small. In order to minimize phase shifts and baseline tilt, the large value capacitors are required. For video system performance that is not to be of the highest quality, the value of these capacitors can be reduced by a factor of up to five with only a slight observable change in the picture quality.

### Single-Supply AC Coupled Single-Ended-to-Differential Driver

The circuit shown in Figure 2.44 provides a flexible solution to differential line driving in a single-supply application and utilizes the dual AD8042. The basic operation of the cross-coupled configuration has been described earlier in this section. The input,  $V_{IN}$ , is a single-ended signal that is capacitively coupled into the feedforward resistor, R1. The non-inverting inputs of each half of the AD8042 are biased at +2.5V. The gain from single-ended input to differential output is equal to  $2R2/R1$ . The gain can be varied by changing one resistor (either R1 or R2).

### SINGLE SUPPLY AC COUPLED DIFFERENTIAL DRIVER



## HIGH SPEED VIDEO MULTIPLEXING WITH OP AMPS UTILIZING DISABLE FUNCTION

A common video circuit function is the multiplexer, a stage which selects one of "N" video inputs and transmits a buffered version of the selected signal to the output. A number of video op amps (AD810, AD813, AD8013) have a *disable* mode which, when activated by applying the appropriate level to a pin on the package, disables the op amp output stage and drops the power to a lower value.

In the case of the AD8013 (triple current-feedback op amp), asserting any one of the disable pins about 1.6V from the negative supply will put the corresponding amplifier into a disabled, powered-down state. In this condition, the amplifier's quiescent current drops to about 0.3mA, its output becomes a high impedance, and there is a high level of isolation from the input to the output. In the case of the gain-of-two line driver, for example, the impedance at the output node will be about equal to the sum of the feedback and feedforward resistors (1.6k $\Omega$ ) in parallel with about 12pF capacitance. Input-to-output isolation is about 66dB at 5MHz.

Leaving the disable pin disconnected (floating) will leave the corresponding amplifier operational, in the enabled state. The input impedance of the disable pin is about 40k $\Omega$  in parallel with 5pF. When driven to 0V, with the negative supply at -5V, about 100 $\mu$ A flows into the disable pin.

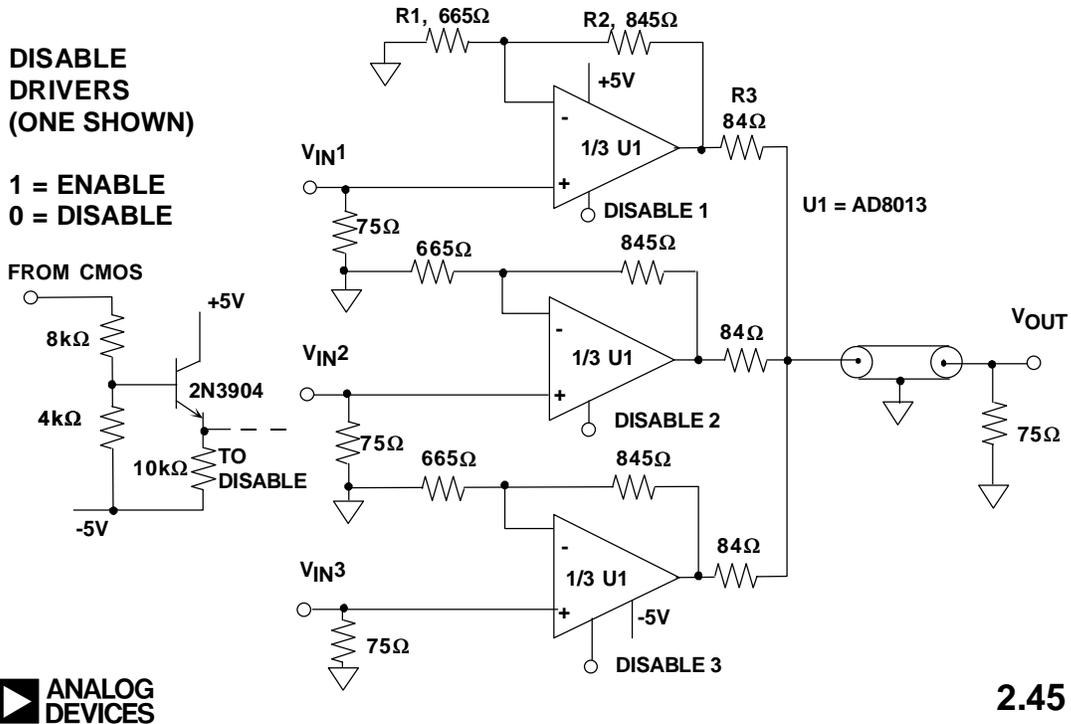
When the disable pins are driven by CMOS logic, on a single +5V supply, the disable and enable times are about 50ns. When operated on dual supplies, level shifting will be required from standard logic outputs to the disable pins.

The AD8013's input stages include protection from the large differential voltages that may be applied when disabled. Internal clamps limit this voltage to about  $\pm 3$ V. The high input-to-output isolation will be maintained for voltages below this limit.

Wiring the amplifier outputs together as shown in Figure 2.45 will form a 3:1 multiplexer with about 50ns switching time between channels. The 0.1dB bandwidth of the circuit is 35MHz, and the OFF channel isolation is 60dB at 10MHz. The simple logic level-shifting circuit shown on the diagram does not significantly affect switching time.

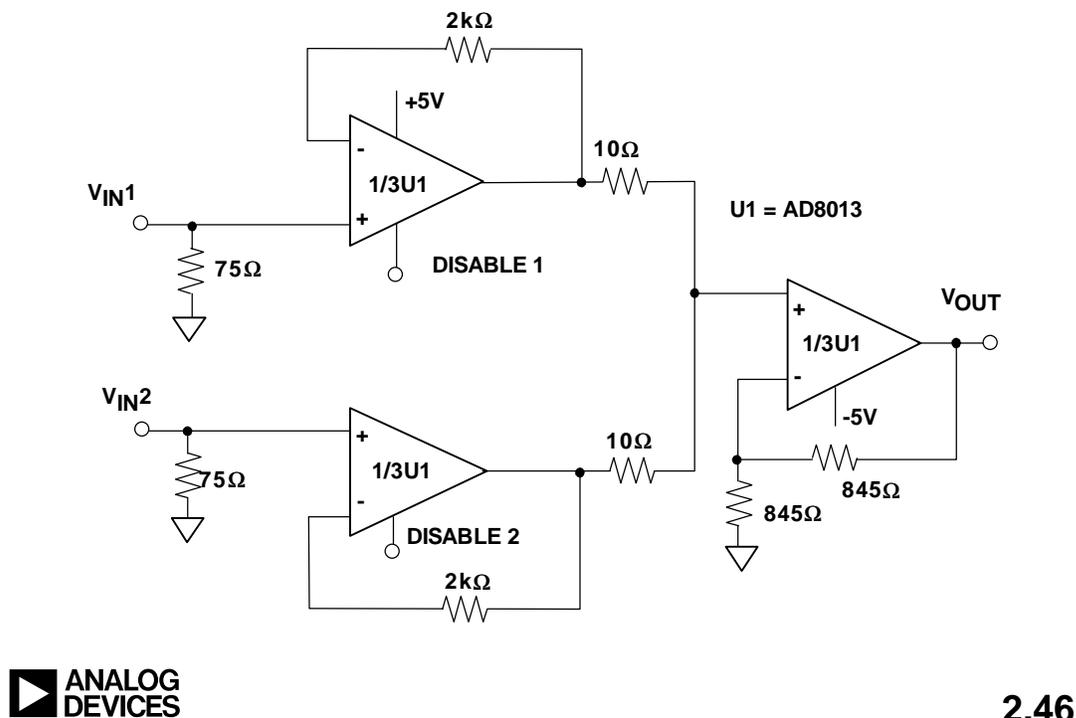
The resistors were chosen as follows. The feedback resistor R2 of 845 $\Omega$  was chosen first for optimum bandwidth of the AD8013 current feedback op amp. When any given channel is ON, it must drive both the termination resistor R<sub>L</sub>, and the net dummy resistance, R<sub>X</sub>/2, where R<sub>X</sub> is an equivalent series resistance equal to R1 + R2 + R3. To provide a net overall gain of unity plus an effective source resistance of 75 $\Omega$ , the other resistor values must be as shown.

## 3:1 VIDEO MULTIPLEXER SWITCHES IN 50ns

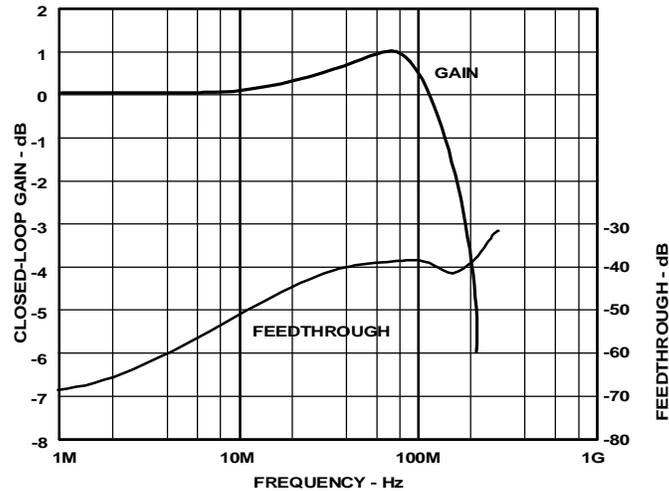


Configuring two amplifiers as unity gain followers and using the third to set the gain results in a high performance 2:1 multiplexer as shown in Figure 2.46. The circuit takes advantage of the very low crosstalk between the amplifiers and achieves the OFF channel isolation shown in Figure 2.47. The differential gain and phase performance of the circuit is 0.03% and 0.07°, respectively.

## 2:1 VIDEO MULTIPLEXER



## 2:1 MULTIPLEXER ON-CANNEL GAIN AND MUX OFF-CANNEL FEEDTHROUGH VS. FREQUENCY

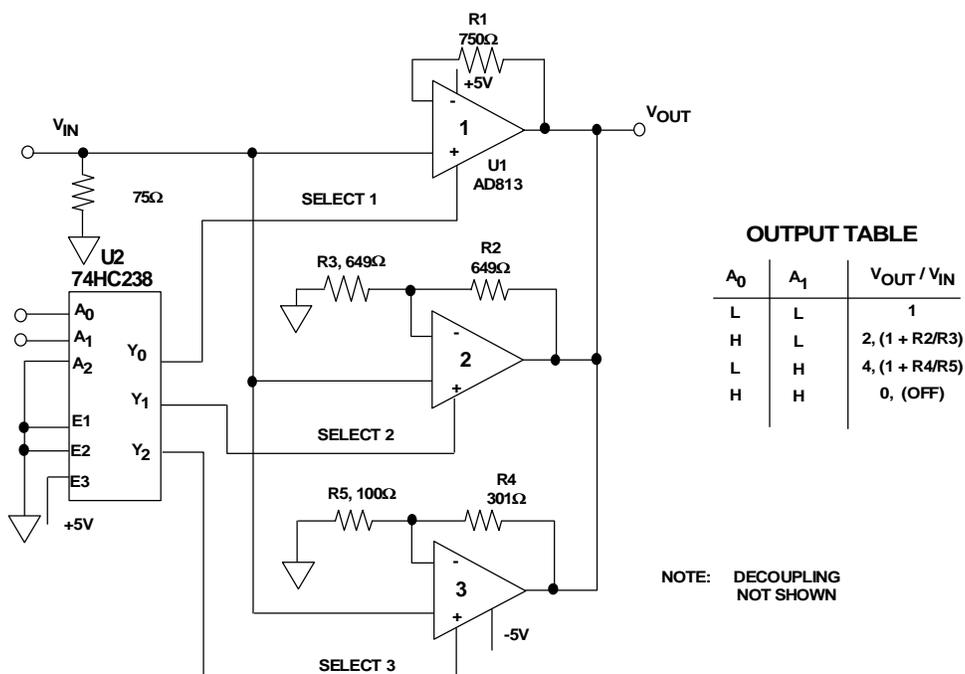


2.47

### VIDEO PROGRAMMABLE GAIN AMPLIFIER USING THE AD813 TRIPLE CURRENT FEEDBACK OP AMP

Closely related to the multiplexers described above is a programmable gain video amplifier, or PGA, as shown in Figure 2.48. In the case of the AD813, the individual op amps are disabled by pulling the disable pin about 2.5V below the positive supply. This puts the corresponding amplifier in its powered down state. In this condition, the amplifier's quiescent supply current drops to about 0.5mA, its output becomes a high impedance, and there is a high level of isolation between the input and the output. Leaving the disable pin disconnected (floating) will leave the amplifier operational, in the enabled state. The input impedance of the disable pins is about 35k $\Omega$  in parallel with 5pF. When grounded, about 50 $\mu$ A flows out of a disable pin when operating on  $\pm$ 5V supplies. The switching threshold is such that the disable pins can be driven directly from +5V CMOS logic with no level shifting (as was required in the previous example).

## PROGRAMMABLE GAIN AMPLIFIER USING AD813 TRIPLE CFB OP AMP



2.48

With a two-line digital control input, this circuit can be set up to provide 3 different gain settings. This makes it a useful circuit in various systems which can employ signal normalization or gain ranging prior to A/D conversion, such as CCD systems, ultrasound, etc. The gains can be binary related as here, or they can be arbitrary. An extremely useful feature of the AD813 CFB current feedback amplifier is the fact that the bandwidth does not reduce as gain is increased. Instead, it stays relatively constant as gain is raised. Thus more useful bandwidth is available at the higher programmed gains than would be true for a fixed gain-bandwidth product VFB amplifier type.

In the circuit, channel 1 of the AD813 is a unity gain channel, channel 2 has a gain of 2, and channel 3 a gain of 4, while the fourth control state is OFF. As is indicated by the table, these gains can be varied by adjustment of the R<sub>2</sub>/R<sub>3</sub> or R<sub>4</sub>/R<sub>5</sub> ratios. For the gain range and values shown, the PGA will be able to maintain a 3dB bandwidth of about 50MHz or more for loading as shown (a high impedance load of 1kΩ or more is assumed). Fine tuning the bandwidth for a given gain setting can be accomplished by lowering the resistor values at the higher gains, as shown in the circuit, where for G=1, R<sub>1</sub>=750Ω, for G=2, R<sub>2</sub>=649Ω, and for G=4, R<sub>4</sub>=301Ω.

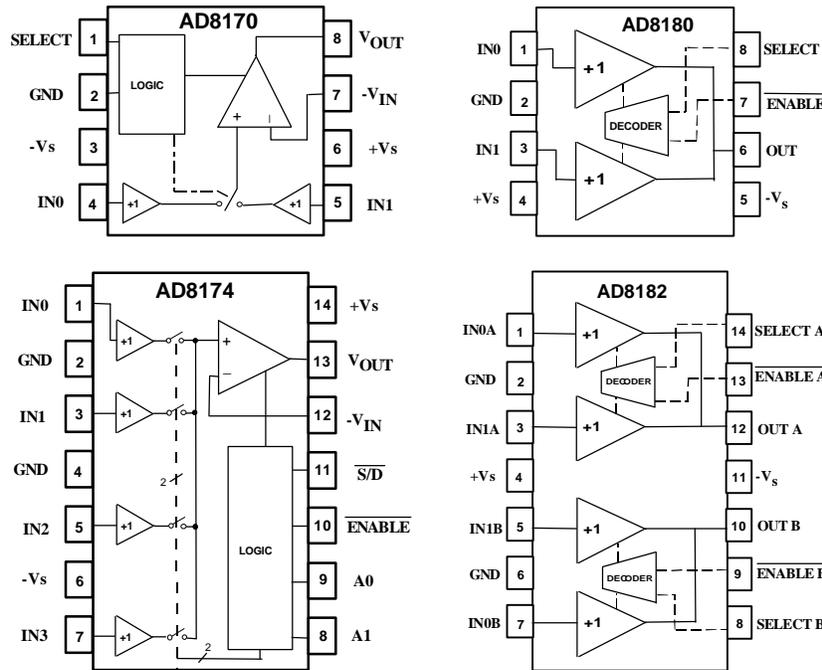
## VIDEO MULTIPLEXERS AND CROSSPOINT SWITCHES

Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time (typically 100ns or so) is not fast enough for today's applications, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch "on" resistance with signal level (called *R<sub>on</sub> modulation*) introduces unwanted distortion and degradation

in differential gain and phase. Multiplexers based on complementary bipolar technology offer a better solution at video frequencies.

Functional block diagrams of the AD8170/8174/8180/8182 bipolar video multiplexer are shown in Figure 2.49. These devices offer a high degree of flexibility and are ideally suited to video applications, with excellent differential gain and phase specifications. Switching time for all devices in the family is 10ns to 0.1%. The AD8170/8174 muxes include an on-chip current feedback op amp output buffer whose gain can be set externally. Off channel isolation and crosstalk are typically greater than 80dB for the entire family. Key specifications are shown in Figure 2.50.

## AD8170/8174/8180/8182 BIPOLAR VIDEO MULTIPLEXERS



2.49

## AD817X AND AD818X MULTIPLEXER KEY SPECIFICATIONS

- 10ns Switching Time
- Wide Bandwidth (-3dB BW):
  - ◆ 200MHz (AD817X)
  - ◆ 600MHz (AD818X)
- Gain Flatness (0.1dB):
  - ◆ 80MHz (AD817X)
  - ◆ 150MHz (AD818X)
- 0.02% / 0.02° Differential Gain and Phase (AD817X,  $R_L = 150\Omega$ )

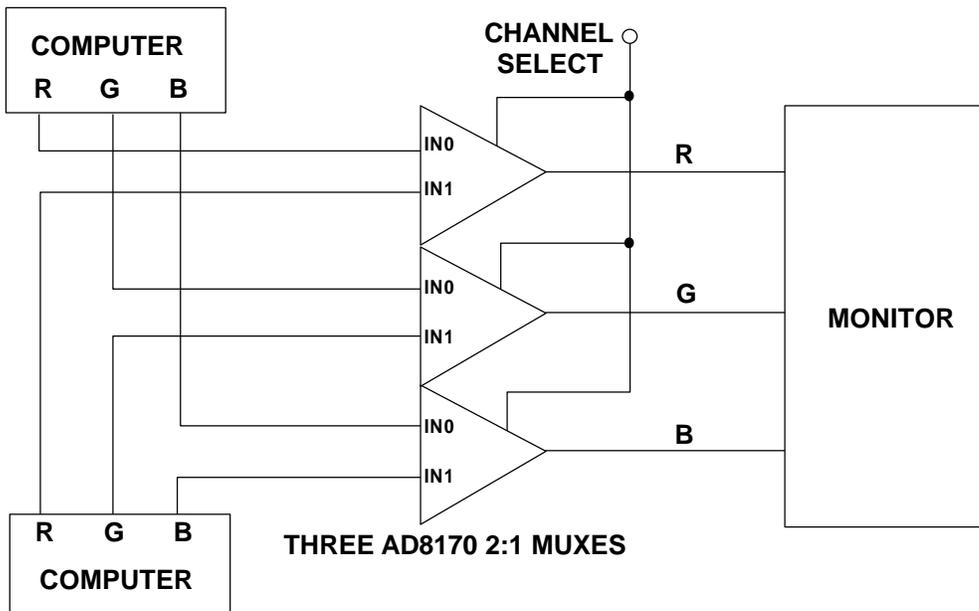
- 0.02% / 0.03° Differential Gain and Phase (AD818X,  $R_L = 1k\Omega$ )
- Off-Channel Isolation and Crosstalk  $> -80dB @ 10MHz$
- Low Power ( $\pm 5V$  Supplies):
  - ◆ AD8170 - 65mW
  - ◆ AD8174 - 85mW
  - ◆ AD8180 - 35mW
  - ◆ AD8182 - 70mW



2.50

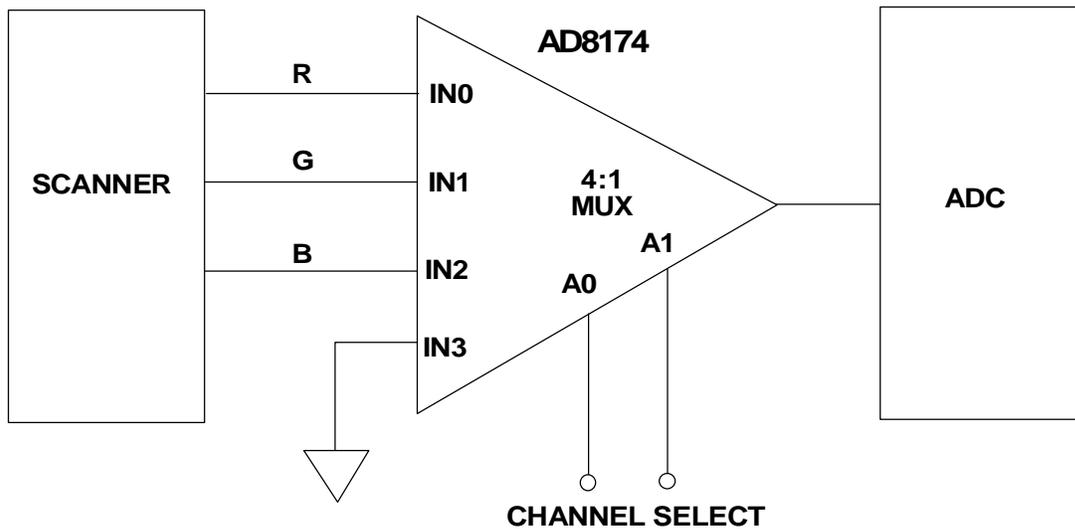
Figure 2.51 shows an application circuit for three AD8170 2:1 muxes where the RGB monitor can be switched between two computers. The AD8174 4:1 mux is used in Figure 2.52 to allow a single high speed ADC to digitize the RGB outputs of a scanner. Figure 2.53 shows two AD8174 4:1 muxes expanded into an 8:1 mux.

### DUAL SOURCE RGB MULTIPLEXER USING THREE 2:1 MUXES



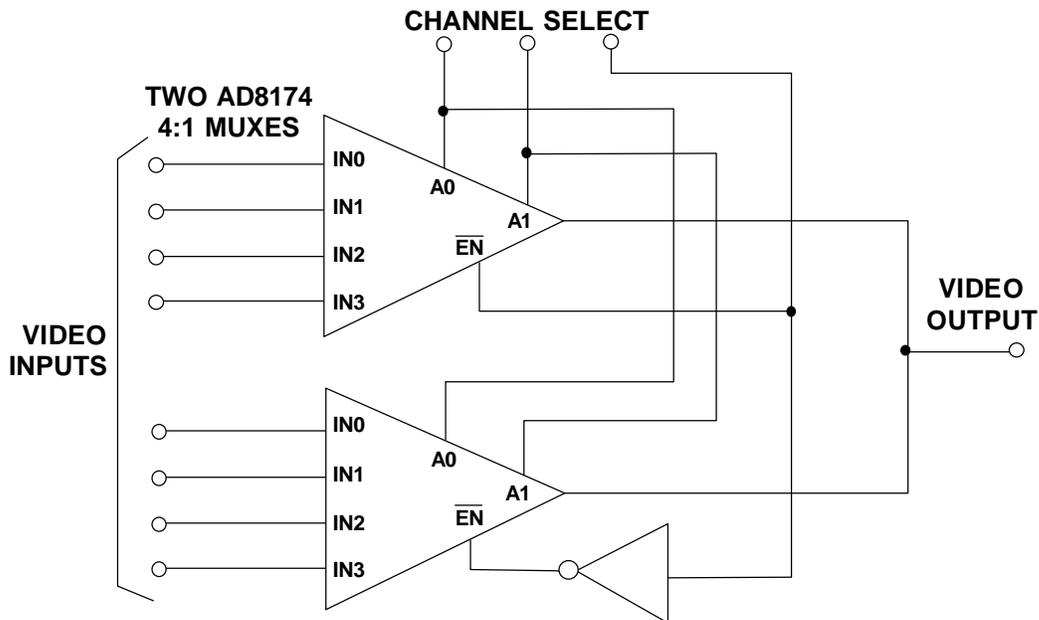
2.51

## DIGITIZING RGB SIGNALS WITH ONE ADC AND A 4:1 MUX



2.52

## EXPANDING TWO 4:1 MUXES INTO AN 8:1 MUX

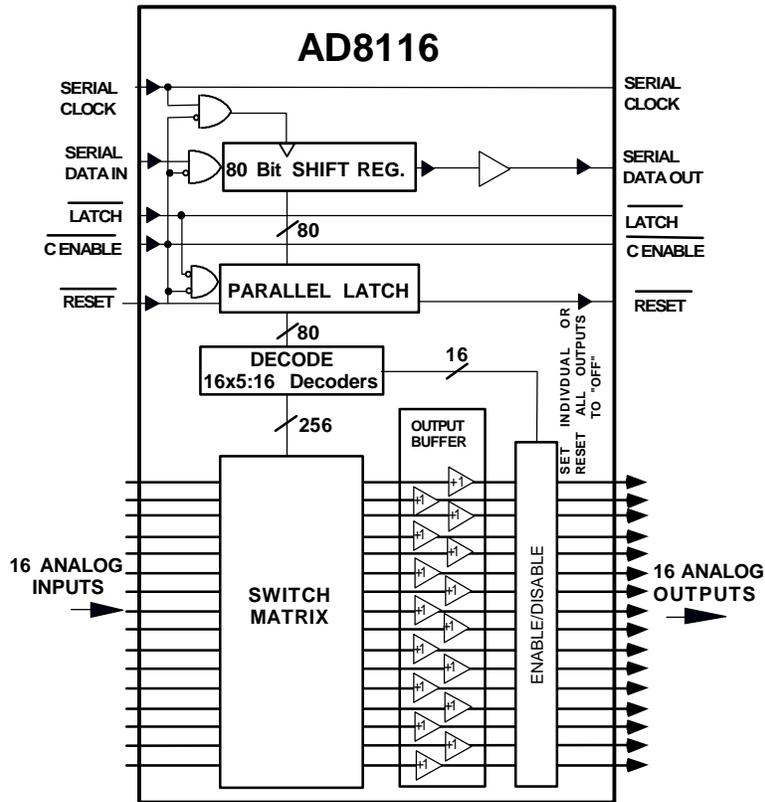


2.53

The AD8116 extends the concepts above to yield a 16×16 buffered video crosspoint switch matrix (Figure 2.54). The 3dB bandwidth is greater than 200MHz, and the 0.1dB gain flatness extends to greater than 40MHz. Channel switching time is less than 30ns to 0.1%. Crosstalk is 70dB and isolation is 90dB (both measured at 10MHz). Differential gain and phase is 0.01% and 0.01° for a 150Ω load. Total power dissipation is 900mW on ±5V supplies.

The AD8116 includes output buffers which can be put into a high impedance state for paralleling crosspoint stages so that the off channels do not load the output bus. The channel switching is performed via a serial digital control which can accommodate "daisy chaining" of several devices. The AD8116 is packaged in a 128-pin TQFP package. Key specifications for the device are summarized in Figure 2.55.

### AD8116 16x16 BUFFERED VIDEO CROSSPOINT SWITCH



## AD8116 CROSSPOINT SWITCH KEY SPECIFICATIONS

- 16x16 Buffered Inputs and Outputs
- Output Buffer Disable Feature Allows Expansion
- 3dB Bandwidth 200MHz, 0.1dB Bandwidth 40MHz
- 30ns Switching to 0.1%
- Differential Gain 0.01%, Differential Phase 0.01°
- Power Dissipation: 900mW ( $\pm 5V$  Supplies)
- 128-pin TQFP, 0.36 Square Inches Area



2.55

## HIGH POWER LINE DRIVERS AND ADSL

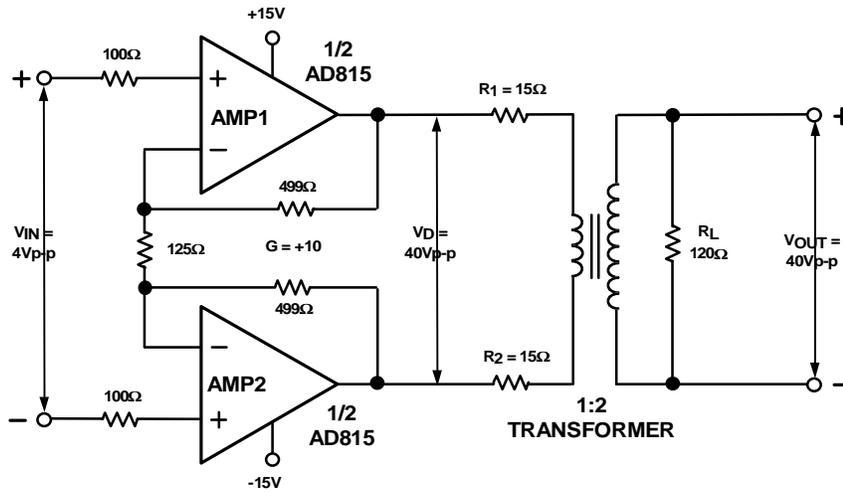
ADSL (Asymmetric Digital Subscriber Line) uses the current subscriber line connection to the central office to transmit data as high as 8Mbps, almost 300 times the speed of the fastest traditional modem. ADSL uses the entire bandwidth (approximately 1MHz) of the connection in addition for the modulation scheme called Discrete Multi Tone (DMT).

Although high-speed fiber links already exist, it is still too difficult and expensive to bring them directly to every residence. ADSL uses the existing infrastructure for "the last mile" connecting the home and the local central office (which already has a high-speed fiber link to the national network).

Many applications are uneven (asymmetric) in their bandwidth needs - sending more information in one direction than the other. Typically, a user will request a video channel, ask for information from a central database, or view complex graphical images on a web page. All of these applications require considerable bandwidth. In contrast, the user may only send commands or files back up to the server. Realizing this, ADSL was designed to deliver a bigger downstream capacity to the home, while having a smaller two-way capacity.

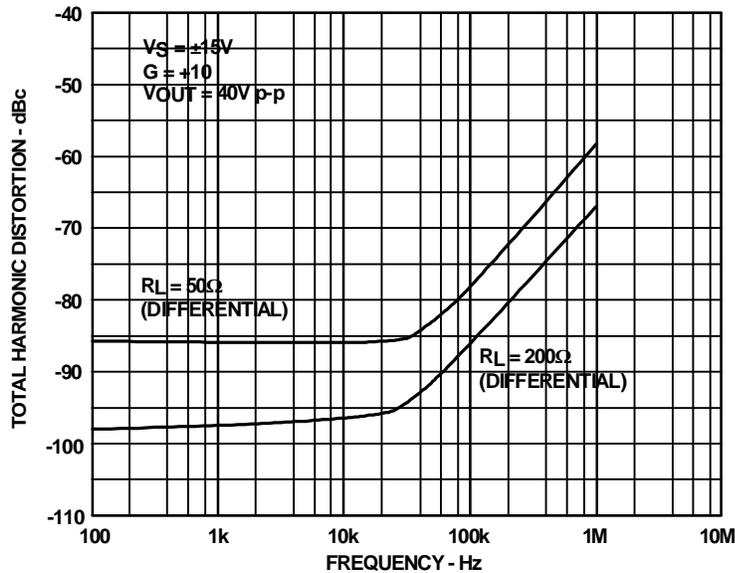
Key to the ADSL system is the requirement for a low-distortion differential drive amplifier which delivers approximately 40V p-p into a 60 $\Omega$  differential load impedance. The AD815 dual high current driver can deliver 40V p-p differential into a 50 $\Omega$  load (corresponding to 400mA peak current!) using the application circuit shown in Figure 2.56. Low harmonic distortion is also required for ADSL applications, since it affects system bit error rates. The typical distortion of the device is shown in Figure 2.57 for 50 $\Omega$  and 200 $\Omega$  differential loads.

## ADSL DIFFERENTIAL LINE DRIVER USING THE AD815



2.56

## THD VS. FREQUENCY FOR AD815 DIFFERENTIAL DRIVER



2.57

There are three AD815 models, two are available in a 15-pin power package, and the third as a 24-pin thermally enhanced SOIC. The 15-pin power package (AD815AY-through hole and AD815AVR-surface mount) has a low thermal resistance ( $\theta_{JA} = 41^\circ\text{C/W}$ ) which can be reduced considerably (to  $\theta_{JA} = 16^\circ\text{C/W}$ ) by connecting the package to an area of copper which acts as a heat sink. The AD815 incorporates a thermal shutdown circuit to protect the die from thermal overload.

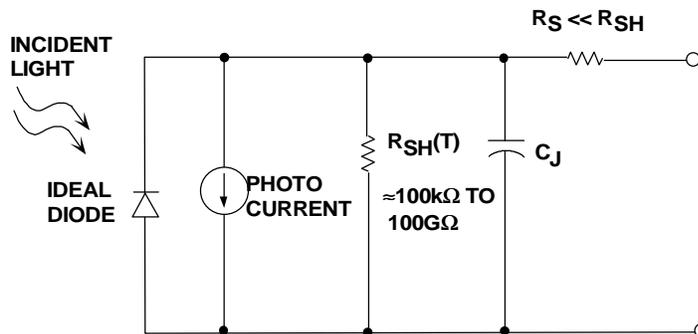
The AD815 also has applications as a general purpose high current coil, transformer, or twisted pair cable driver, a CRT convergence adjustment control, or a video signal distribution amplifier. Each amplifier in the AD815 is capable of driving 6 back-terminated 75Ω video loads with a differential gain and phase of 0.05% and 0.45° respectively.

## HIGH SPEED PHOTODIODE PREAMPS

Photodiodes generate a small current which is proportional to the level of illumination. They have many applications ranging from precision light meters to high-speed fiber optic receivers.

The equivalent circuit for a photodiode is shown in Figure 2.58. One of the standard methods for specifying the sensitivity of a photodiode is to state its short circuit photocurrent ( $I_{SC}$ ) at a given light level from a well defined light source. The most commonly used source is an incandescent tungsten lamp running at a color temperature of 2850K. At 100fc (foot-candles) illumination (approximately the light level on an overcast day), the short circuit current is usually in the picoamps to hundreds of microamps range for small area (less than 1mm<sup>2</sup>) diodes.

### PHOTODIODE EQUIVALENT CIRCUIT



## 2.58

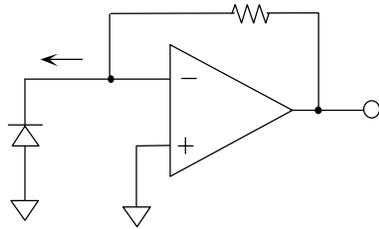
The short circuit current is very linear over 6 to 9 decades of light intensity, and is therefore often used as a measure of absolute light levels. The open circuit forward voltage drop across the photodiode varies logarithmically with light level, but, because of its large temperature coefficient, the diode voltage is seldom used as an accurate measure of light intensity.

The shunt resistance is usually in the order of several hundred kΩ to more than 1GΩ at room temperature, and decreases by a factor of two for every 10°C rise in

temperature. Diode capacitance is a function of junction area and the diode bias voltage. A value of 10 to 50pF at zero bias is typical for small area diodes.

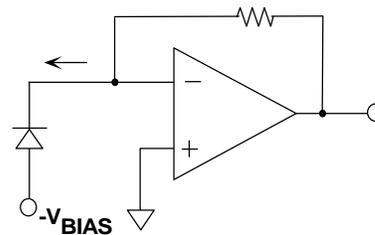
Photodiodes may either be operated with zero bias (*photovoltaic* mode) or reverse bias (*photoconductive* mode) as shown in Figure 2.59. The most precise linear operation is obtained in the photovoltaic mode, while higher switching speeds are realizable when the diode is operated in the photoconductive mode. Under reverse bias conditions, a small amount of current called *dark current* will flow even when there is no illumination. There is no dark current in the photovoltaic mode. In the photovoltaic mode, the diode noise is basically the thermal noise generated by the shunt resistance. In the photoconductive mode, shot noise due to conduction is an additional source of noise. Photodiodes are usually optimized during the design process for use in either the photovoltaic mode or the photoconductive mode, but not both.

## PHOTODIODE MODES OF OPERATION



### PHOTOVOLTAIC

- Zero Bias
- No Dark Current
- Precision Applications
- Low Noise (Johnson)



### PHOTOCONDUCTIVE

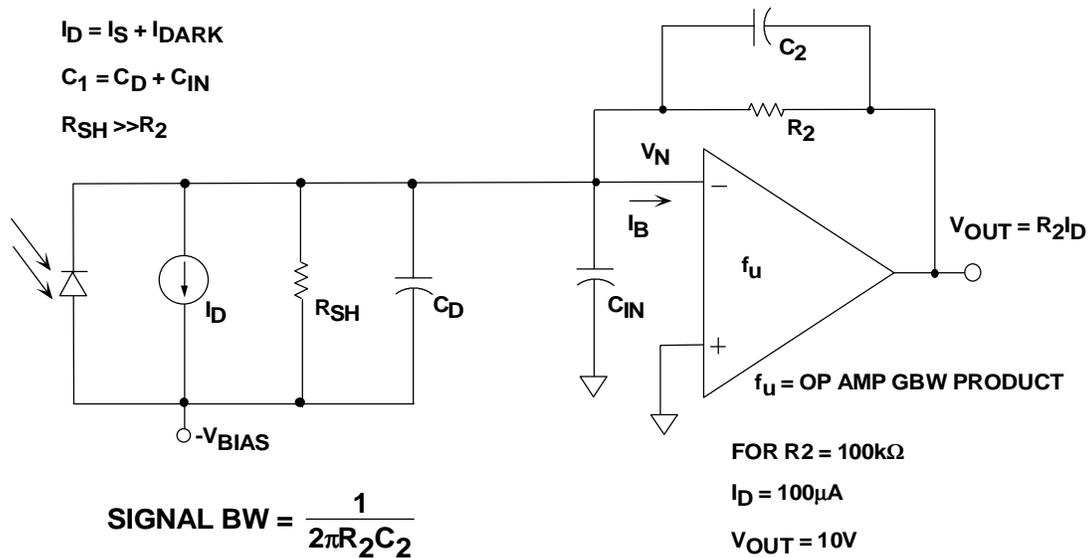
- Reverse Bias
- Dark Current Exists
- High Speed Applications
- Higher Noise (Johnson + Shot)



2.59

Optimizing photodiode preamplifiers is probably one of the most challenging of design problems, especially if high bandwidth and direct coupling is required. Figure 2.60 shows a basic photodiode preamp designed with an op amp connected as a current-to-voltage converter.

## HIGH BANDWIDTH PHOTODIODE PREAMP EQUIVALENT CIRCUIT



2.60

The sensitivity of the circuit is determined by the amount of photodiode current multiplied by the feedback resistor  $R_2$ . The key parameters of the diode (see Figure 2.61) are its sensitivity (output current as a function of illumination level), dark current (the amount of current which flows due to the reverse bias voltage when the diode is not illuminated), risetime, shunt capacitance, and shunt resistance.

The key parameters of the op amp are its input voltage and current noise, bias current, unity gain-bandwidth product,  $f_u$ , and input capacitance,  $C_{in}$ .

The HP 5082-4204 PIN Photodiode will be used as an example for our discussion. Its characteristics are given in Figure 2.61. It is typical of many commercially available PIN photodiodes. As in most high-speed photodiode applications, the diode is operated in the reverse-biased or *photoconductive* mode. This greatly lowers the diode junction capacitance, but causes a small amount of *dark current* to flow even when the diode is not illuminated (we will show a circuit which compensates for the dark current error later in the section).

### HP 5082-4204 PHOTODIODE

- Sensitivity: 350 $\mu A$  @ 1mW, 900nm
- Maximum Linear Output Current: 100 $\mu A$
- Area: 0.002cm<sup>2</sup> (0.2mm<sup>2</sup>)
- Capacitance: 4pF @ 10V reverse bias

- Shunt Resistance:  $10^{11}\Omega$
- Risetime: 10ns
- Dark Current: 600pA @ 10V reverse bias



## 2.61

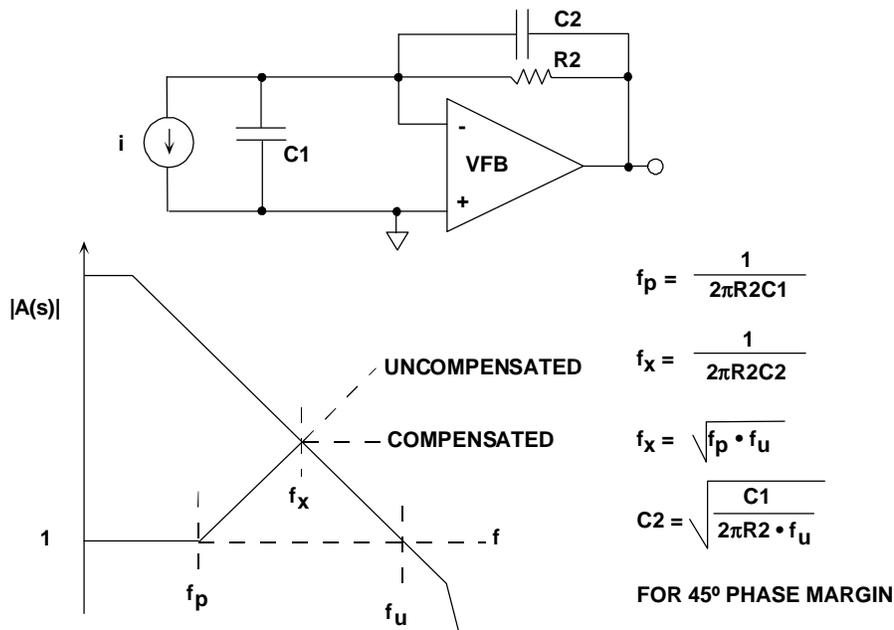
This photodiode is linear with illumination up to approximately 50 to 100 $\mu$ A of output current. The dynamic range is limited by the total circuit noise and the diode dark current (assuming no dark current compensation).

Using the simple circuit shown in Figure 2.60, assume that we wish to have a full scale output of 10V for a diode current of 100 $\mu$ A. This determines the value of the feedback resistor R2 to be 10V/100 $\mu$ A = 100k $\Omega$ .

### Analysis of Frequency Response and Stability

The photodiode preamp model is the classical second-order system shown in Figure 2.62, where the I/V converter has a total input capacitance C1 (the sum of the diode capacitance and the op amp input capacitance). The shunt resistance of the photodiode is neglected since it is much greater than R2, the feedback resistor.

### COMPENSATING FOR INPUT CAPACITANCE IN A CURRENT-TO-VOLTAGE CONVERTER USING VFB OP AMP



## 2.62

The net input capacitance, C1, forms a pole at a frequency  $f_p$  in the noise gain transfer function as shown in the Bode plot.

$$f_p = \frac{1}{2\pi R_2 C_1}.$$

Note that we are neglecting the effects of the compensation capacitor C2 and are assuming that it is small relative to C1 and will not significantly affect the pole frequency  $f_p$  when it is added to the circuit. In most cases, this approximation yields results which are close enough, considering the other variables in the circuit.

If left uncompensated, the phase shift at the frequency of intersection,  $f_x$ , will cause instability and oscillation. Introducing a zero at  $f_x$  by adding the feedback capacitor C2 stabilizes the circuit and yields a phase margin of about 45 degrees.

$$f_x = \frac{1}{2\pi R_2 C_2}$$

Since  $f_x$  is the geometric mean of  $f_p$  and the unity-gain bandwidth frequency of the op amp,  $f_u$ ,

$$f_x = \sqrt{f_p \cdot f_u}.$$

These equations can be solved for C2:

$$C_2 = \sqrt{\frac{C_1}{2\pi R_2 \cdot f_u}}.$$

This value of C2 will yield a phase margin of about 45 degrees. Increasing the capacitor by a factor of 2 increases the phase margin to about 65 degrees (see References 4 and 5).

In practice, the optimum value of C2 should be optimized experimentally by varying it slightly to optimize the output pulse response.

### **Selection of the Op Amp**

The photodiode preamp should be a wideband FET-input one in order to minimize the effects of input bias current and allow low values of photocurrents to be detected. In addition, if the equation for the 3dB bandwidth,  $f_x$ , is rearranged in terms of  $f_u$ ,  $R_2$ , and  $C_1$ , then

$$f_x = \sqrt{\frac{f_u}{2\pi R_2 C_1}},$$

where  $C_1 = C_D + C_{in}$

By inspection of this equation, it is clear that in order to maximize  $f_x$ , the FET-input op amp should have both a high unity gain-bandwidth product,  $f_u$ , and a low input capacitance,  $C_{in}$ . In fact, the ratio of  $f_u$  to  $C_{in}$  is a good figure-of-merit when evaluating different op amps for this application. Figure 2.63 compares a number of FET-input op amps suitable for photodiode preamps.

## FET-INPUT OP AMP COMPARISON TABLE FOR WIDE BANDWIDTH PHOTODIODE PREAMPS

	Unity GBW Product, $f_u$ (MHz)	Input Capacitance $C_{in}$ (pF)	$f_u/C_{in}$ (MHz/pF)	Input Bias Current $I_b$ (pA)	Voltage Noise @10kHz (nV/ $\sqrt{\text{Hz}}$ )
AD823	16	1.8	8.9	3	16
AD843	34	6	5.7	600	19
AD744	13	5.5	2.4	100	16
AD845	16	8	2	500	18
AD745*	20	20	1	250	2.9
AD645	1	1	1	1.5	8
AD820	1.9	2.8	0.7	2	13
AD743	4.5	20	0.2	250	2.9

\* Stable for Noise Gains  $\geq 5$ , Usually the Case, Since  
High Frequency Noise Gain =  $1 + C_1/C_2$ , and  $C_1$  Usually  $\geq 4C_2$ .



### 2.63

By inspection, the AD823 op amp has the highest ratio of unity gain-bandwidth product to input capacitance, in addition to relatively low input bias current. For these reasons, it was chosen for the wideband photodiode preamp design.

Using the diode capacitance,  $C_D=4\text{pF}$ , and the AD823 input capacitance,  $C_{in}=1.8\text{pF}$ , the value of  $C_1 = C_D+C_{in} = 5.8\text{pF}$ . Solving the above equations using  $C_1=5.8\text{pF}$ ,  $R_2=100\text{k}\Omega$ , and  $f_u=16\text{MHz}$ , we find that:

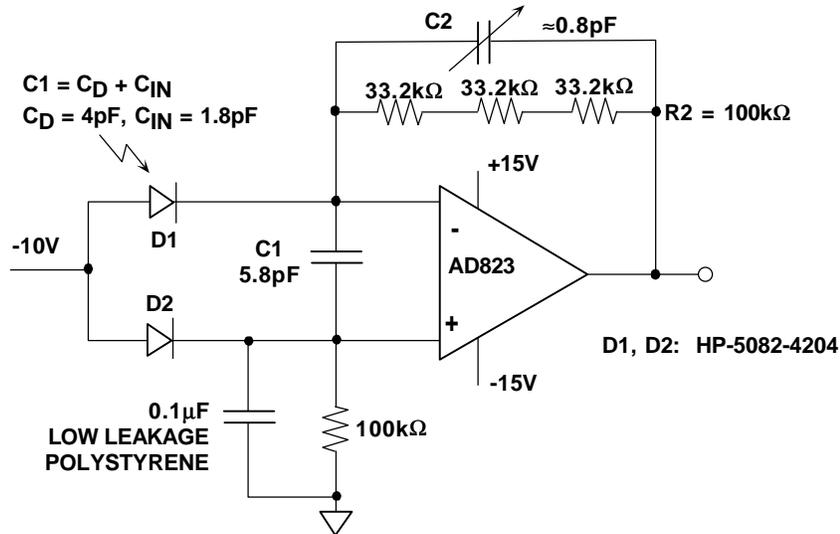
$$\begin{aligned} f_p &= 274\text{kHz} \\ C_2 &= 0.76\text{pF} \\ f_x &= 2.1\text{MHz} \end{aligned}$$

In the final design (Figure 2.64), note that the  $100\text{k}\Omega$  resistor is replaced with three  $33.2\text{k}\Omega$  film resistors to minimize stray capacitance. The feedback capacitor,  $C_2$ , is a variable  $1.5\text{pF}$  ceramic and is adjusted in the final circuit for best bandwidth/pulse response. The overall circuit bandwidth is approximately  $2\text{MHz}$ .

The full scale output voltage of the preamp for  $100\mu\text{A}$  diode current is  $10\text{V}$ , and the error (RTO) due to the photodiode dark current of  $600\text{pA}$  is  $60\text{mV}$ . The dark current

error can be canceled using a second photodiode of the same type in the non-inverting input of the op amp as shown in Figure 2.64.

## 2MHz BANDWIDTH PHOTODIODE PREAMP WITH DARK CURRENT COMPENSATION



2.64

### Photodiode Preamp Noise Analysis

As in most noise analyses, only the key contributors need be identified. Because the noise sources combine in an RSS manner, any single noise source that is at least three or four times as large as any of the others will dominate.

In the case of the wideband photodiode preamp, the dominant sources of output noise are the input voltage noise of the op amp,  $V_{ni}$ , and the resistor noise due to  $R2$ ,  $V_{nR2}$ . The input current noise of the FET-input op amp is negligible. The shot noise of the photodiode (caused by the reverse bias) is negligible because of the filtering effect of the shunt capacitance  $C1$ . The resistor noise is easily calculated by knowing that a  $1k\Omega$  resistor generates about  $4nV/\sqrt{Hz}$ , therefore, a  $100k\Omega$  resistor generates  $40nV/\sqrt{Hz}$ . The bandwidth for integration is the signal bandwidth,  $2.1MHz$ , yielding a total output rms noise of:

$$V_{nR2}(OUT) = 40\sqrt{1.57 \cdot 2.1 \cdot 10^6} = 73\mu V_{rms}.$$

The factor of 1.57 converts the approximate single-pole bandwidth of  $2.1MHz$  into the *equivalent noise bandwidth*.

The output noise due to the input voltage noise is obtained by multiplying the noise gain by the voltage noise and integrating the entire function over frequency. This would be tedious if done rigorously, but a few reasonable approximations can be made which greatly simplify the math. Obviously, the low frequency  $1/f$  noise can be

neglected in the case of the wideband circuit. The primary source of output noise is due to the high-frequency noise-gain peaking which occurs between  $f_p$  and  $f_u$ . If we simply assume that the output noise is constant over the entire range of frequencies and use the maximum value for AC noise gain  $[1+(C1/C2)]$ , then

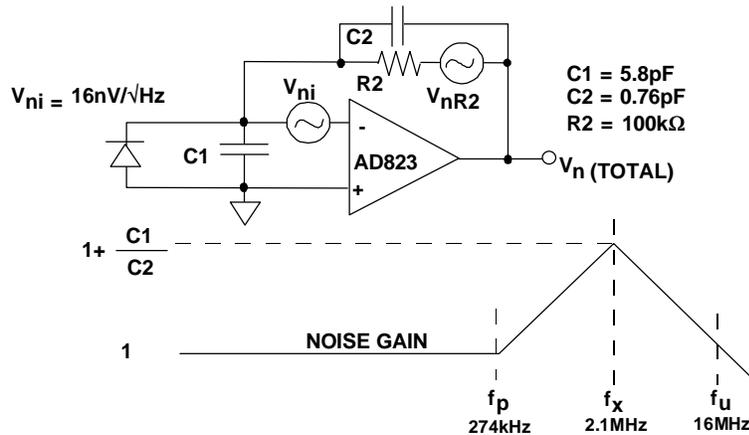
$$V_{ni(OUT)} \approx V_{ni} \left( 1 + \frac{C1}{C2} \right) \sqrt{1.57f_x} = 250\mu V_{rms}.$$

The total rms noise referred to the output is then the RSS value of the two components:

$$V_{n(TOTAL)} = \sqrt{(73)^2 + (250)^2} = 260\mu V_{rms}.$$

The total output dynamic range can be calculated by dividing the full scale output signal (10V) by the total output rms noise, 260 $\mu$ Vrms, and converting to dB, yielding approximately 92dB.

### EQUIVALENT CIRCUIT FOR OUTPUT NOISE ANALYSIS



■  $V_{ni(out)} \approx V_{ni} \left( 1 + \frac{C1}{C2} \right) \sqrt{1.57f_x} = 250\mu V_{rms}$

■  $V_{nR2(out)} \approx \sqrt{4kTR2 \cdot 1.57f_x} = 73\mu V_{rms}$

■  $V_{n(TOTAL)} = \sqrt{250^2 + 73^2} = 260\mu V_{rms}$

■  $DYNAMIC RANGE = 20 \log \left[ \frac{10V}{260\mu V} \right] = 92dB$



2.65

## REFERENCES

1. Walt Kester, *Maintaining Transmission Line Impedances on the PC Board*, within Chapter 11 of **System Applications Guide**, Analog Devices, 1993.
2. Joe Buxton, *Careful Design Tames High-Speed Op Amps*, **Electronic Design**, April 11, 1991.
3. Walt Jung, *Op Amps in Line-Driver and Receiver Circuits, Part 1*, **Analog Dialogue**, Vol. 26-2, 1992.
4. William R. Blood, Jr., **MECL System Design Handbook** (HB205, Rev.1), Motorola Semiconductor Products, Inc., 1988.
5. Dave Whitney, Walt Jung, *Applying a High-Performance Video Operational Amplifier*, **Analog Dialogue**, 26-1, 1992.
6. Ohmtek, Niagara Falls, NY, (716) 283-4025.
7. Walt Kester, *Video Line Receiver Applications Using the AD830 Active Feedback Amplifier Topology*, within Chapter 11 of **System Applications Guide**, Analog Devices, 1993.
8. Walt Jung, *Analog-Signal-Processing Concepts Get More Efficient*, **Electronic Design Analog Applications Issue**, June 24, 1993.
9. Peter Checkovich, *Understanding and Using High-Speed Clamping Amplifiers*, **Analog Dialogue**, Vol. 29-1, 1995.
10. Walt Jung, Scott Wurcer, *Design Video Circuits Using High-Speed Op-Amp Systems*, **Electronic Design Analog Applications Issue**, November 7, 1994.
11. W. A. Kester, *PCM Signal Codecs for Video Applications*, **SMPTE Journal**, No. 88, November 1979, pp. 770-778.
12. *IEEE Standard for Performance Measurements of A/D and D/A Converters for PCM Television Circuits*, **IEEE Standard 746-1984**.
13. **Practical Analog Design Techniques**, Chapters 1, 2, and 4, 1995, Analog Devices.
14. **Amplifier Applications Guide**, 1992, Analog Devices.
15. Jerald G. Graeme, **Photodiode Amplifiers: Op Amp Solutions**, McGraw Hill, 1995.