

Evaluating the **AD8338** Low Power VGA

FEATURES

Full featured evaluation board for the **AD8338**
On-board voltage regulator
On-board potentiometers for direct adjustment, with test points for electronic adjustment
All analog design, no software needed

EVALUATION KIT CONTENTS

AD8338-EVALZ evaluation board
AD8338-EVALZ user guide (**UG-559**)

ADDITIONAL EQUIPMENT NEEDED

A signal generator
A power supply capable of 6 V to 20 V output
An oscilloscope with a 100 MHz minimum bandwidth
3 SMA (M) to BNC (M) cables

ONLINE RESOURCES

AD8338 data sheet
UG-559 user guide

GENERAL DESCRIPTION

This user guide describes the **AD8338** evaluation board and discusses common configurations. The design of this board (**AD8338-EVALZ**) emphasizes simplicity and ease of use, which is evident in the minimalist approach to connector implementation.

The **AD8338** data sheet, available at www.analog.com, covers the details for the operation of the **AD8338**. The **AD8338** data sheet should be consulted in conjunction with this user guide. The data sheet not only assists designers in their end applications but also provides important information to understand the operation of the **AD8338** evaluation board, especially its initial configuration and power up.

AD8338-EVALZ EVALUATION BOARD



Figure 1.

11510-001

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REVISION HISTORY

3/16—Rev. A to Rev. B

Changes to Figure 1	1
Changes to Features and Evaluation Kit Contents Sections	1
Changes to Evaluation Board Quick Start Procedures.....	3
Combined Input Signals and Output Signals Headings to Modes and Input and Output Signals	3
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8/13—Rev. 0 to Rev. A

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Changes to Figure 6.....	6

5/13—Revision 0: Initial Version

EVALUATION BOARD QUICK START PROCEDURES

INITIAL SETUP

The [AD8338](#) evaluation board needs only a few external connections. Setting up this board for the first time requires the following:

- A dc supply to power the evaluation board from 6 V to 20 V (6 V is preferred)
- Cables to connect the board to the signal source
- Cables to connect the board to the oscilloscope

INITIAL CONNECTIONS

First, connect two SMA to BNC cables from the output SMA connectors (OUTP, OUTM) to the oscilloscope. Set the oscilloscope to 1 M Ω input impedance. The [AD8338](#) is not specified to drive 50 Ω impedances; therefore, it must drive a high impedance load.

When using the [AD8338](#) in standalone mode, which is fully differential in and out, set up the signal source as a differential output using two channels. Set the phase of the first channel to be in phase and set the second channel to be out of phase (180°).

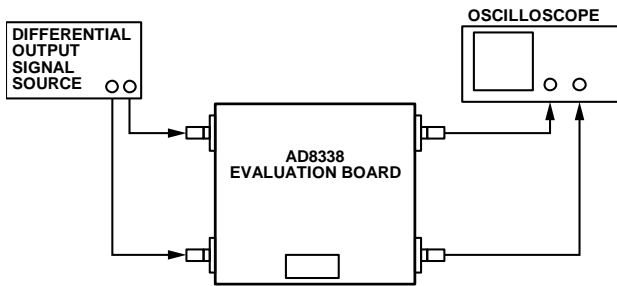


Figure 2. Basic Connections for the [AD8338](#) Evaluation Module, Differential Mode

POWERING UP THE [AD8338](#)

Take the following steps to power up the [AD8338](#) evaluation board:

1. Before applying any signals or supplies, set the jumpers to their default settings, as indicated on the printed circuit board (PCB).
2. Set the power supply to 6 V.
3. Enable the output.
4. Set the output amplitude on the signal generator to 0.1 V on each channel (200 mV difference amplitude). Note that the [AD8338-EVALZ](#) board includes on-board 50 Ω terminators.
5. Adjust the potentiometer (labeled GAIN ADJ) counter-clockwise until stopped.
6. Enable the outputs.

Upon correct configuration, the output signal appears on the oscilloscope. Manually adjust gain by adjusting the GAIN ADJ potentiometer. If these work, then basic operation of the [AD8338-EVALZ](#) is verified.

CONFIGURING FOR SINGLE-ENDED INPUT, DIFFERENTIAL OUTPUT

The [AD8338-EVALZ](#) is equipped with the [ADA4940-1](#) differential driver amplifier. Bring this amplifier into the signal chain through the setting of the J5, J6, J7, and J8 jumpers as highlighted in Figure 3.

When these jumpers (J5 to J7 and J8) are set, the input connectors (J3 and J4) are disconnected from the [AD8338](#), and fed into the [ADA4940-1](#). Input Connector J4 becomes inert and is no longer necessary and Input Connector J3 becomes the single-ended input source. The [ADA4940-1](#) operates in unity-gain difference.

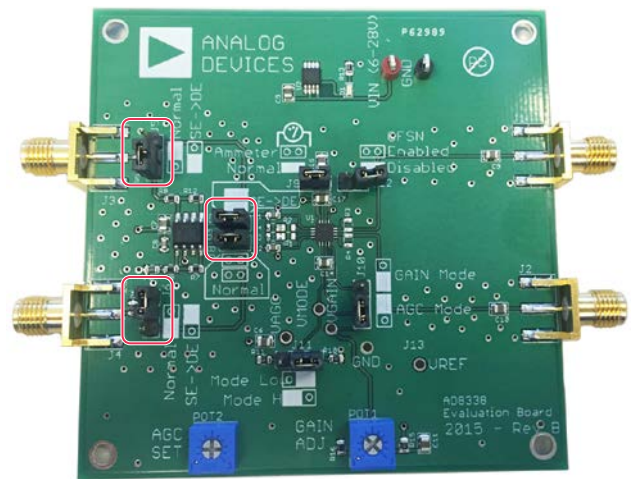


Figure 3. [AD8338-EVALZ](#) Board with Jumpers Set for Single-Ended Input Mode

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The [AD8338](#) evaluation board includes the [ADP1720](#) low dropout regulator (LDO). The LDO supplies a very clean 5.0 V supply to the [AD8338](#) and [ADA4940-1](#).

Note that, because the supply input to the evaluation board is not reverse bias protected, it is important to exercise care when connecting your power supplies to prevent damage.

INPUT CONTROLS

The [AD8338-EVALZ](#) has two primary input controls, GAIN ADJUST and AGC SET (see Figure 1). An external voltage applied to the respective test points overrides the potentiometer, allowing for direct electronic control.

The MODE signal can also be overridden with an external signal by driving the associated test point.

MODES AND INPUT AND OUTPUT SIGNALS

AGC Mode

AGC mode attempts to regulate the output magnitude to a target rms voltage. This mode requires altering some jumper settings. As shown in Figure 6, Jumper J10 is shifted by one pin. For easy identification, refer to the silkscreen reference on the evaluation board. (See Figure 7 for electrical information; changing connection from Pin 2 and Pin 3 to Pin 1 and Pin 2.) This connects the GAIN pin to the DETO pin, and puts the evaluation board into AGC mode. After altering the jumper settings, set the rms voltage by applying a voltage of the 0 V to 3.0 V range on the VAGC pin.

When the AGC mode is disabled, the MODE pin selects the direction of the gain slope, either positive or negative. While the AGC mode is disabled, the GAIN pin directly controls the gain with an input ranging between 0.1 V and 1.1 V. When the AGC circuit is not in use, tie the VAGC pin to VREF.

In this mode, the user controls the rms output level through applying an input signal to VAGC. For the lowest gain, VAGC is tied to VREF, where the loop attempts to attenuate the output to 0 V rms.

As the input to VAGC moves away from the 1.5 V of VREF (in either the positive or negative direction), the gain increases.

Enable or disable offset nulling through the removal or placement of Jumper J12. By default, the jumper is not installed, enabling offset nulling. The application of the offset nulling feature applies a capacitor between OFNS and VREF, where the internal correction circuit passes signals of a higher frequency.

Input Signals

The signal inputs to the evaluation board start with SMA connectors designated by J3 and J4. On the board, these signals are terminated to ground with 49.9 Ω resistors. The inputs are then fed into the inputs of the [AD8338](#) directly (in the default configuration), or to the inputs of an [ADA4940-1](#) differential amplifier. In the worst-case scenario, the effective input impedance seen by the signal generator is 45 Ω (a VSWR match of 1.1:1).

Output Signals

The [AD8338](#) outputs swing nearly up to 1.5 V relative to VREF, regardless of device power supply. On the evaluation board, these outputs are ac-coupled through 0.1 μ F capacitors and should not be loaded with terminating values less than 500 Ω (per each output). Below 500 Ω , the linearity of the outputs begins to degrade.

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

Factory Default Configuration

The [AD8338](#) evaluation board ships with a default configuration shown in Figure 4 whereby offset nulling is enabled, MODE is set to high, and the system gain increases by rotating GAIN ADJ clockwise.

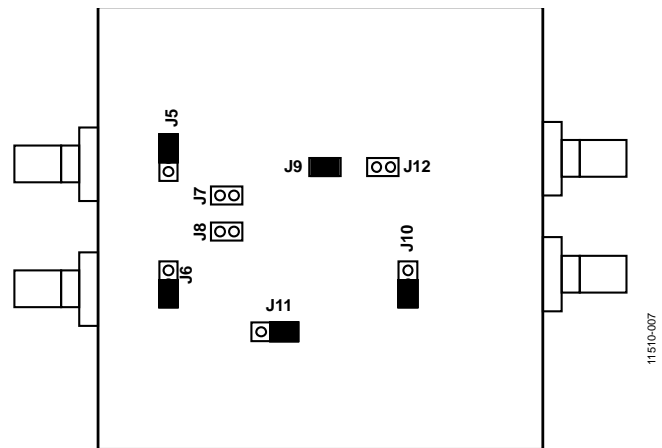


Figure 4. Standard Jumper Configuration

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Configuration for Decreasing Gain with Increasing Voltage on GAIN Pin

Figure 5 shows the basic connections of the evaluation board. MODE is set to low to achieve these results. In this configuration, turning GAIN ADJ clockwise causes a decrease in applied gain. At full rotation clockwise, the gain equals 0 dB.

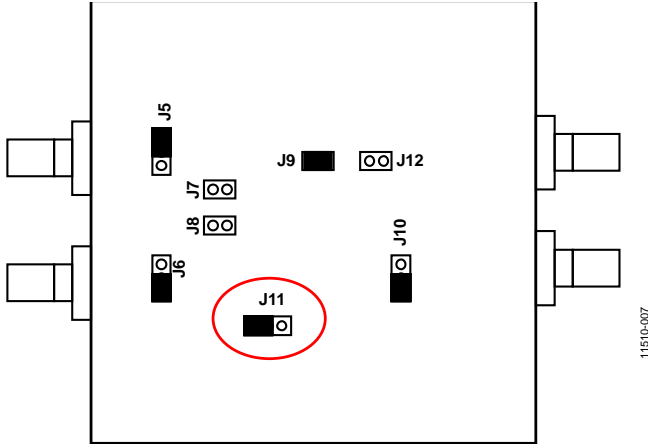


Figure 5. Jumper Configuration for MODE = Low

Configuration for Using AGC Loop

For the application of the AGC loop, set MODE on the AD8338 to high. Set the DETO jumper (P5) as shown in Figure 6. With the board configured as illustrated in Figure 6, the signal into VAGC sets the output rms level.

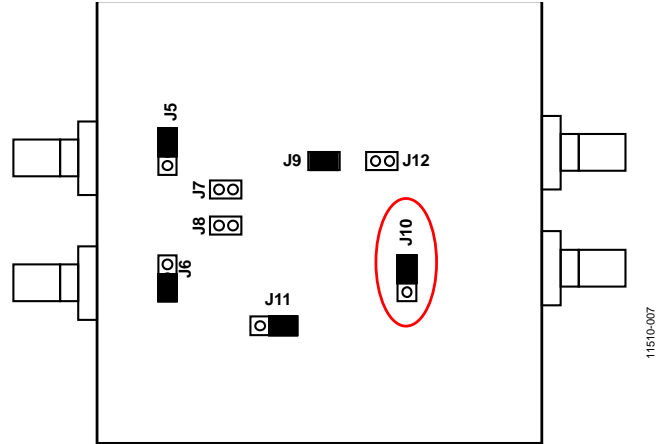


Figure 6. Jumper Settings for AGC Mode

EVALUATION BOARD SCHEMATIC

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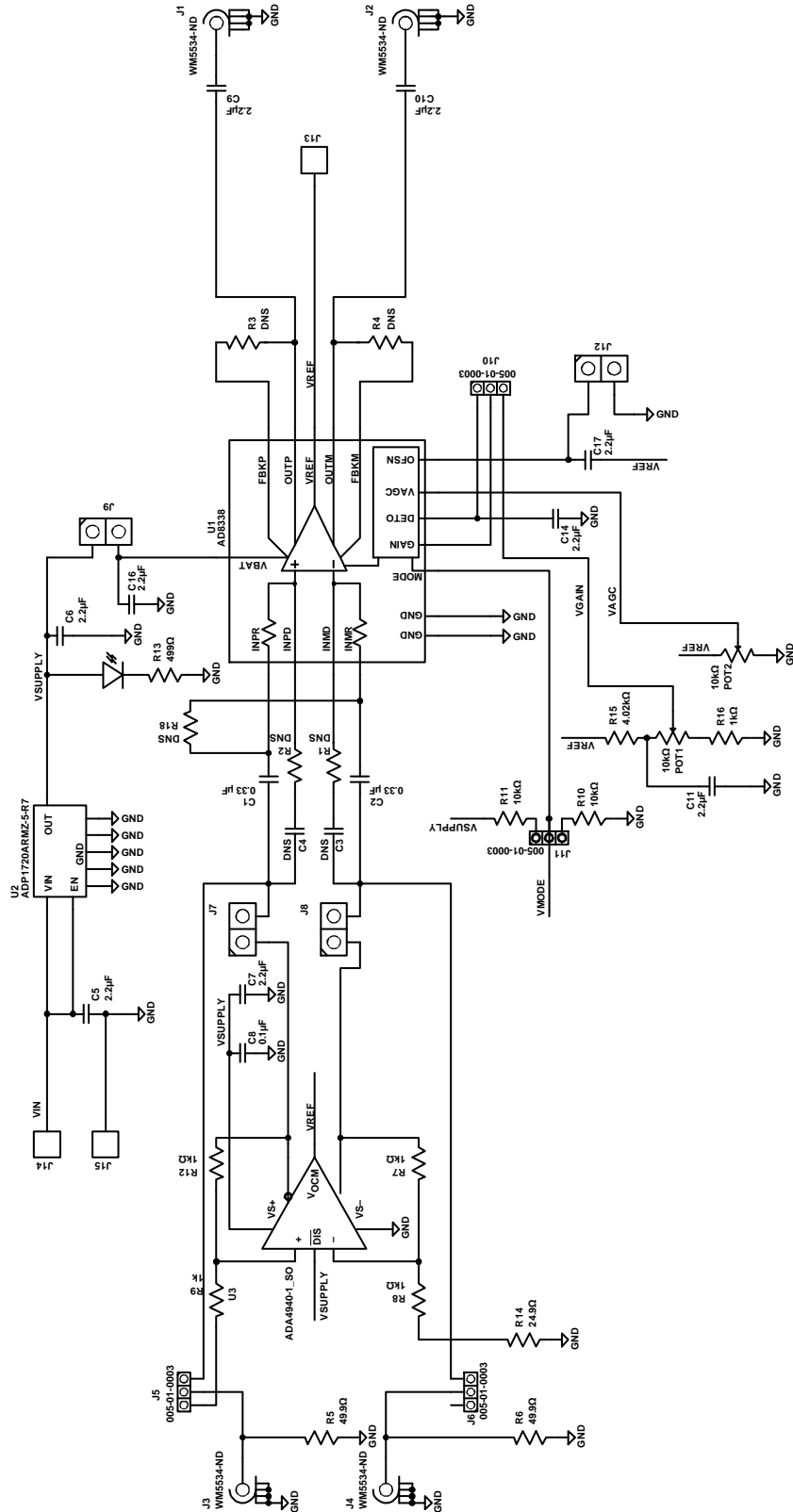


Figure 7. Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Qty.	Reference Designator	Description	Manufacturer	Part Number
4	J7, J8, J9, J12	Standard 0.100 spacing	TE Connectivity	5-146269-1
1	D1	0603 LED: green	Dialight	598-8060-102F
1	C8	0.10 μ F capacitor, 25 V, 0603 package	Kemet	C0603C104K3RAC7411
2	C1, C2	1 μ F ceramic capacitor, 6.3 V, 0603 package	Murata	GRM033R60J105MEA2D
4	J5, J6, J10, J11	Inline 3-pin header	TE Connectivity	4-103321-5
2	R10, R11	10 k Ω resistor, 0603 size	Vishay	CRCW060310K0FKEA
2	POT1, POT2	10k	Vishay	T73YB103KT20
1	J14	Red large testpoint	Kobiconn	151-107-RC
2	J13, J15	Black, large test point	Kobiconn	151-103-RC
5	R7, R8, R9, R12, R16	1.0 k Ω , 0.1 W, 0603	KOA Speer	RK73H1JTDD1001F
9	C5, C6, C7, C9, C10, C11, C14, C16, C17	2.2 μ F capacitor, 0805 package	TDK	C2012X7R1C225K125AB
1	R14	24.9 Ω resistor, 1%, 0603	Vishay	CRCW060324R9FKEA
1	R15	4.02 k Ω resistor, 1%	Vishay	CRCW06034K02FKEB
2	R5, R6	49.9 Ω resistor, 0603	KOA Speer	RK73H1JTDD49R9F
1	R13	499 Ω resistor, 0603	Vishay	CRCW0603499RFKEA
1	U1	AD8338 , low power, 80 dB VGA, low frequency to 18 MHz	Analog Devices, Inc.	AD8338ACPZ-R7
1	U3	Low power, low distortion ADC driver	Analog Devices	ADA4940-1ARZ
1	U2	4 V to 28 V input LDO, 50 mA output, 5 V	Analog Devices	ADP1720ARMZ-5-R7
4	J1, J2, J3, J4	Standard size end launch SMA connector	Cinch Connectivity Solutions	142-0701-801
8	J5, J6, J7, J8, J9, J10, J11, J12	Shunt jumpers(placed over assembled headers); a golden board is provided for reference	3M	969102-0000-DA

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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