Universal Evaluation Board for Dual High Speed Op Amps in MSOP Packages

FEATURES

- Enables quick breadboarding/prototyping
- User-defined circuit configuration
- Edge-mounted SMA connector provisions
- Easy connection to test equipment and other circuits
- RoHS compliant

GENERAL DESCRIPTION

The Analog Devices, Inc., high speed universal evaluation board (EB-O8RM-2Z) is designed to help customers quickly prototype new dual op amp circuits and reduce design time. The evaluation board can be used with almost any Analog Devices dual op amp in various configurations and applications. Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the circuit side of the bare evaluation board.

The evaluation board is a 2-layer PCB that accepts SMA connectors on the input and output for efficient connection to test equipment. The ground plane, component placement, and supply bypassing are laid out to minimize parasitic inductances and capacitances. The evaluation board components are primarily SMT 0805 case size, with the exception of the electrolytic bypass capacitors (C1, C2), which are 3528 case size.

There are two options for supply bypassing. The first option is connecting additional shunt capacitors (C3, C4) in parallel with the electrolytic capacitors (C1, C2) from each supply to ground. This technique of power supply bypassing provides wideband rejection of unwanted noise on the supply lines. It is implemented by placing a 0 Ω resistor in the C5 position and shunt capacitors in the C1, C2, C3, and C4 positions.

The second approach to supply bypassing is to connect one capacitor between the supply rails. This method uses fewer components and can improve the power supply rejection ratio (PSRR) at higher frequencies. It is implemented by inserting a 0 Ω resistor in the C3 position, inserting the bypass capacitor in the C4 position, and omitting C5. Optimal bypassing is circuit dependent and therefore must be evaluated by the designer.

Figure 3 shows the evaluation board schematic. Figure 4 and Figure 6 show the evaluation board assembly drawings. The PCB layout pattern for the component side is shown in Figure 5, and the PCB layout pattern for the circuit side is shown in Figure 7.
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REVISION HISTORY
5/10—Revision 0: Initial Version
Figure 3. EB-08RM-2Z Universal Evaluation Board Schematic
Figure 4. Board Assembly Drawing, Component Side

Figure 5. Board Layout Pattern, Component Side

Figure 6. Board Assembly Drawing, Circuit Side

Figure 7. Board Layout Pattern, Circuit Side
### ORDERING INFORMATION

#### BILL OF MATERIALS

Table 1.

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<tr>
<th>Quantity</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Package</th>
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<tbody>
<tr>
<td>6</td>
<td>+VS, −VS, GND1, GND2, GND3, GND4</td>
<td>Testpoint</td>
<td>TP</td>
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<td>2</td>
<td>C1, C2</td>
<td>10 μF capacitor</td>
<td>C3528</td>
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<td>3</td>
<td>C3, C4, C5</td>
<td>User-defined capacitor</td>
<td>C0805</td>
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<td>DUT</td>
<td>Device</td>
<td>MSOP</td>
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<td>SMA/SMT</td>
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<td>16</td>
<td>RF1, RF2, RGN1, RGN2, RGP1, RGP2, RL1, RL2, RP1, RP2, RPI1, RPI2, RT1, RT2, RS1, RS2</td>
<td>User-defined resistor</td>
<td>R0805</td>
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NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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