Evaluation Board for the ADGS5412 Serially Controlled, High Voltage, Latch-Up Proof, Quad SPST Switch

FEAT URES
- SPI interface with error detection
- Includes CRC, invalid read/write address, and SCLK count error detection
- Analog supply voltages
  - Dual-supply: ±9 V to ±22 V
  - Single-supply: 9 V to 40 V
- PC control in conjunction with the evaluation software
  - EVAL-SDP-CB1Z SDP

EVALUATION KIT CONTENTS
- EVAL-ADGS5412SDZ

DOCUMENTS NEEDED
- ADGS5412 data sheet

EQUIPMENT NEEDED
- EVAL-SDP-CB1Z controller board
- ACE software with EVAL-ADGS5412SDZ plug-in
- DC voltage source
  - ±22 V for dual-supply
  - 40 V for single-supply
- Optional digital logic supply: 3.3 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION
The EVAL-ADGS5412SDZ is the evaluation board for the ADGS5412. The ADGS5412 is a latch-up proof, quad single-pole, single-throw (SPST) switch controlled by a serial peripheral interface (SPI). The SPI has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read/write address detection, and serial clock (SCLK) count error detection. It is possible to daisy-chain multiple ADGS5412 devices together. This enables the configuration of multiple devices with a minimal amount of digital lines. The ADGS5412 also supports burst mode that decreases the time between SPI commands.

Figure 1 shows the EVAL-ADGS5412SDZ in a typical evaluation setup. The EVAL-ADGS5412SDZ is controlled by the EVAL-SDP-CB1Z system demonstration platform (SDP), which connects to a PC via a USB port. The ADGS5412 is on the center of the evaluation board and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device, and a fourth terminal provides users with a defined digital logic supply voltage, if required. Alternatively, the digital logic supply voltage can be supplied from the SDP.

Full specifications on the ADGS5412 are available in the ADGS5412 data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

The evaluation board interfaces to the USB port of a PC via the SDP board. The EVAL-SDP-CB1Z board (SDP-B controller board) is available to order on the Analog Devices website at www.analog.com.
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REVISION HISTORY

5/2017—Revision 0: Initial Version
ADGS5412 EVALUATION BOARD LAYOUT

Figure 1.
EVALUATION BOARD HARDWARE

POWER SUPPLIES
Connector J1 provides access to the supply pins of the ADGS5412. VDD, GND, and VSS on J1 terminal block link to the appropriate pins on the ADGS5412. For dual-supply voltages, the evaluation board can be powered from ±9 V to ±22 V. For single-supply voltages, the GND and VSS terminals must connect together and power the evaluation board with 9 V to 40 V. Additionally, 3.3 V is supplied to the VL pin of the ADGS5412 by the SDP when Link LK1 is in Position B. When controlling the ADGS5412 by another method other than the SDP, supply between 2.7 V and 5.5 V to the VL pin of the ADGS5412 via the EXT_VL screw terminal input on J1. LK1 must be in Position A.

INPUT SIGNALS
Two screw connectors, J2 and J3, are provided to connect to both the source and drain pins of the ADGS5412. Additional subminiature version B (SMB) connector pads are available if extra connections are required.

Each trace on the source and drain side includes two sets of 0603 pads, which can place a load on the signal path to ground.

A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads can create a simple resistor-capacitor (RC) filter.

LINK OPTIONS
A number of link options are provided on the EVAL-ADGS5412SDZ evaluation board that must be set for the required operating conditions before using. Table 1 describes the positions of the links to control the evaluation board via the SDP board using a PC and external power supplies. The functions of these link options are described in detail in Table 2.

When using the SDP in conjunction with the EVAL-ADGS5412SDZ, LK1 must be in Position B to avoid damage to the SDP.

Table 1. Link Options for SDP Control (Default)

<table>
<thead>
<tr>
<th>Link Number</th>
<th>Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>B</td>
</tr>
<tr>
<td>LK2</td>
<td>B</td>
</tr>
</tbody>
</table>

Table 2. Link Functions

<table>
<thead>
<tr>
<th>Link Number</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK1</td>
<td>This link selects the source of the VL voltage supplied to the ADGS5412. Position A selects EXT_VL from J1. Position B selects the 3.3 V from the SDP.</td>
</tr>
<tr>
<td>LK2</td>
<td>This link selects how a hardware reset is performed. Position A indicates the SW1 push button performs a hardware reset. Position B indicates the SDP can perform a hardware reset.</td>
</tr>
</tbody>
</table>
EVALUATION BOARD SOFTWARE
INSTALLING THE SOFTWARE

The EVAL-ADGS5412SDZ evaluation board uses the Analog Devices Analysis Control Evaluation (ACE) software. ACE is a desktop software application that allows the evaluation and control of multiple evaluation systems.

ACE installs the necessary SDP drivers and .NET Framework 4 by default. Install ACE before connecting the SDP. The ACE software and access to full instructions on how to install and use ACE can be found on the Analog Devices website.

After the installation is finished, the EVAL-ADGS5412SDZ evaluation board plug-ins appear when opening ACE.

INITIAL SET UP

To set up the evaluation board, complete the following steps:

1. Connect the evaluation board to the SDP board and connect the SDP board to the computer via a USB cable.
2. Power the evaluation board as described in the Power Supplies section.
3. Run the ACE application. The EVAL-ADGS5412SDZ board plug-ins appear in the attached hardware section of the Start tab.
4. Double-click on the evaluation board plug-in to open the evaluation board view seen in Figure 2.
5. The chip block diagram can be accessed by double-clicking on the ADGS5412 icon (see Figure 2). This view provides a basic representation of functionality of the evaluation board. The main functions are labeled in Figure 3.
BLANK DIAGRAM AND DESCRIPTION

The EVAL-ADGS5412SDZ software is organized so that it appears similar to the functional block diagram shown in the ADGS5412 data sheet. In this way, it is easy to correlate the functions on the EVAL-ADGS5412SDZ board with the description in the data sheets. A full description of each block, register, and setting is given in the ADGS5412 data sheet.

Some of the blocks and their functions are described here as they pertain to the evaluation board. The full screen block diagram, shown in Figure 4, describes the functionality of each

Table 3. Block Diagram Functions

<table>
<thead>
<tr>
<th>Label</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>The dropdown menus configure SW1 to SW4 as open or closed.</td>
</tr>
<tr>
<td>B</td>
<td>The INVALID RW ENABLE, SCLK COUNT ENABLE, and CRC ENABLE checkboxes enable or disable the error detection features on the SPI interface.</td>
</tr>
<tr>
<td>C</td>
<td>The BURST MODE ENABLE checkbox enables or disables burst mode.</td>
</tr>
<tr>
<td>D</td>
<td>The RW ERROR FLAG, SCLK ERROR, and CRC ERROR FLAG indicators illuminate red if the relevant error flags assert in the error flags register.</td>
</tr>
<tr>
<td>E</td>
<td>The Clear Flags button clears the error flags register.</td>
</tr>
<tr>
<td>F</td>
<td>The Apply Changes button applies all modified values to the devices.</td>
</tr>
</tbody>
</table>

Figure 4. EVAL-ADGS5412SDZ Block Diagram with Labels
MEMORY MAP

All registers are fully accessible from the Memory Map tab; this allows registers to be edited at a bit level (see Figure 5 and Figure 6). The bits shaded in dark gray are read-only bits and cannot be accessed from ACE. All other bits are toggled. The Apply Changes button transfers data to the device.

All changes here correspond to the block diagram; for example, if the internal register bit is enabled, it displays as enabled on the block diagram. Any bits or registers that are bold are modified values that have not been transferred to the evaluation board. After clicking Apply Changes, the data is transferred to the evaluation board.

![Figure 5. ADGS5412 Memory Map](image1.png)

![Figure 6. ADGS5412 Memory Map with Unapplied Changes in the SW_DATA Register](image2.png)
EVALUATION BOARD SCHEMATICS AND ARTWORK

Figure 7. EVAL-ADG5412SDZ Schematic 1

Figure 8. EVAL-ADG5412SDZ Schematic 2
Figure 9. EVAL-ADGS5412SDZ Schematic 3

Figure 10. EVAL-ADGS5412SDZ Silk Screen
Figure 11. EVAL-ADGS5412SDZ Top Layer

Figure 12. EVAL-ADGS5412SDZ Layer 2
I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**Table 4.**

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 to C2</td>
<td>50 V tantalum capacitor, 10 μF, D size</td>
</tr>
<tr>
<td>C3 to C6, C8</td>
<td>50 V, X7R multilayer ceramic capacitor, 0.1 μF, 0603</td>
</tr>
<tr>
<td>C7</td>
<td>Capacitor, 10 μF, 0805, 16 V</td>
</tr>
<tr>
<td>D1 to D4</td>
<td>Not placed</td>
</tr>
<tr>
<td>S1 to S4</td>
<td>Not placed</td>
</tr>
<tr>
<td>T1 to T8</td>
<td>Red test point</td>
</tr>
<tr>
<td>GND1, GND2</td>
<td>Black test point</td>
</tr>
<tr>
<td>J1 to J3</td>
<td>4-pin terminal block, 5 mm pitch</td>
</tr>
<tr>
<td>J4</td>
<td>120-way connector, 0.6 mm pitch</td>
</tr>
<tr>
<td>J5</td>
<td>Through hole, header, 4 × 2, 2.54 mm</td>
</tr>
<tr>
<td>LK1, LK2</td>
<td>3-pin single inline (SIL) header and shorting link</td>
</tr>
<tr>
<td>R2 to R7, R12 to R15, R17, R18, R21, R22, R27, R28, R32, R34, R35</td>
<td>Not placed</td>
</tr>
<tr>
<td>R8 to R11, R16, R19, R20, R23 to R26, R33</td>
<td>Resistor, 0 Ω, 0603, 1%</td>
</tr>
<tr>
<td>R1</td>
<td>Resistor, 10 kΩ, 0.063 W, 1%, 0603</td>
</tr>
<tr>
<td>R29</td>
<td>Resistor, 1 kΩ, 0.063 W, 1%, 0603</td>
</tr>
<tr>
<td>R30, R31</td>
<td>Resistor, 100 kΩ, 0.063 W, 1%, 0603</td>
</tr>
<tr>
<td>SW1</td>
<td>Surface mount device (SMD) push button switch</td>
</tr>
<tr>
<td>U1</td>
<td>ADGS5412, SPI controlled, quad SPST switch</td>
</tr>
<tr>
<td>U2</td>
<td>ADGB189, 1.8 V to 5.5 V, 2:1 multiplexer/SPDT switch</td>
</tr>
<tr>
<td>U3</td>
<td>24LC32A-I/MS, 32 kΩ, I2 C serial EEPROM</td>
</tr>
</tbody>
</table>

PC refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).