Evaluation Board for the **ADP5054** 4-Channel Power Management Unit

**FEATURES**

- Wide input voltage range: 4.5 V to 15.5 V
- Full featured evaluation board for the **ADP5054**
  - Channel 1: programmable 2 A/4 A/6 A buck regulator
  - Channel 2: programmable 2 A/4 A/6 A buck regulator
  - Channel 3: 2.5 A sync buck regulator
  - Channel 4: 2.5 A sync buck regulator
- Standalone operation capability
- Cascading options for four buck regulators
- Dedicated enable option for each channel
- Mode option to select power savings mode (PSM) or forced pulse width modulation (FPWM) operation
- Programmable switching frequency from 250 kHz to 2 MHz
- Frequency synchronization input or output

**EQUIPMENT NEEDED**

- Input power source
- Voltmeter
- Ammeter
- Load resistors or electrical load

**GENERAL DESCRIPTION**

This user guide describes the evaluation of the **ADP5054** and includes detailed schematics and printed circuit board (PCB) layouts.

The **ADP5054** evaluation board combines four high performance buck regulators in a 48-lead LFCSP package to meet the demanding performance and board space requirements. The **ADP5054** evaluation board connects to high input voltages, up to 15 V directly without any preregulators.

Full details on the device are provided in the **ADP5054** data sheet, and it is recommended that the data sheet be consulted in conjunction with this evaluation board user guide.

![ADP5054 Evaluation Board](image-url)
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REVISION HISTORY

3/15—Revision 0: Initial Version
USING THE EVALUATION BOARD

POWERING UP THE EVALUATION BOARD

The ADP5054 evaluation board is supplied fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

Enable Jumpers

Each channel has its own enable pin that must be pulled high to enable that channel (see Table 1). Pull the enable pin low or leave it floating to disable the channel.

The enable control for each regulator has a 0.811 V precision enable threshold that allows the ADP5054 to be easily sequenced between channels or other input/output supplies. The enable control can also be used as a programmable undervoltage lockout (UVLO) input by the resistor divider.

Table 1. Channels of the Enable Pins

<table>
<thead>
<tr>
<th>Channel</th>
<th>Pin</th>
<th>Enable Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel 1: Buck</td>
<td>EN1</td>
<td>J-EN1</td>
<td>0.8 V precision enable</td>
</tr>
<tr>
<td>Channel 2: Buck</td>
<td>EN2</td>
<td>J-EN2</td>
<td>0.8 V precision enable</td>
</tr>
<tr>
<td>Channel 3: Buck</td>
<td>EN3</td>
<td>J-EN3</td>
<td>0.8 V precision enable</td>
</tr>
<tr>
<td>Channel 4: Buck</td>
<td>EN4</td>
<td>J-EN4</td>
<td>0.8 V precision enable</td>
</tr>
</tbody>
</table>

Power Input Jumpers

Each channel except Channel 1 has its own power input jumper, which allows the device to support separate input voltage or cascaded options for all channels. Channel 1 input voltage is tied to PVIN1_4 and does not need a jumper.

The power input for the buck regulators is 4.5 V to 15.5 V. Shunt S1, S2, and S3 to allow the easy setup of Channel 2, Channel 3, and Channel 4 using the same input voltage with Channel 1 for the buck regulators.

Table 2. Channels of Power Input Jumpers

<table>
<thead>
<tr>
<th>Channel</th>
<th>Pin</th>
<th>Input Jumper</th>
<th>Input Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel 2: Buck</td>
<td>PVIN2</td>
<td>S1</td>
<td>4.5 V to 15.5 V</td>
</tr>
<tr>
<td>Channel 3: Buck</td>
<td>PVIN3</td>
<td>S2</td>
<td>4.5 V to 15.5 V</td>
</tr>
<tr>
<td>Channel 4: Buck</td>
<td>PVIN4</td>
<td>S3</td>
<td>4.5 V to 15.5 V</td>
</tr>
</tbody>
</table>

Jumper J-SYNC (SYNC/MODE)

The J-SYNC jumper (shown in Figure 1) connects the SYNC/MODE pin of the device to either low or high.

Shunt the center contact of the J-SYNC jumper (SYNC/MODE) to the left pin header so that the SYNC/MODE pin is pulled high to VREG (5 V). This connection switches the buck regulators into FPWM operation.

Shunt the center contact of the J-SYNC jumper to the right pin header to pull the SYNC/MODE pin low, which forces the buck regulators to operate in automatic PWM/PSM operation.

Input Power Source

Before connecting the power source to the ADP5054 evaluation board, turn the evaluation board off. If the input power source includes a current meter, use that meter to monitor the input current. Connect the positive terminal of the power source to the PVIN1_4 terminal (J11) on the evaluation board, and the negative terminal of the power source to the GND terminal (J12) of the board. If the power source does not include a current meter, connect a current meter in series with the input source voltage. Connect the positive terminal of the power source to the positive (+) lead of the current meter, the negative terminal of the power source to the GND terminal (J12), and the negative (−) lead of the current meter to the PVIN1_4 terminal (J11).

Output Load

Turn the board off before connecting the load. Connect an electronic load or resistor to set the load current. If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board, with the positive (+) load connected to one of the channels. For example, connect Buck 1, VOUT1 (J16), and the negative (−) load connection to GND (J15).

If an ammeter is used, connect it in series with the load. Connect the positive (+) ammeter terminal to the evaluation board for Buck 1, VOUT1 (J16), the negative (−) ammeter terminal to the positive (+) load terminal, and the negative (−) load terminal to the evaluation board at GND (J15).

Input and Output Voltmeters

Measure the input and output voltages with voltmeters. Ensure that the voltmeters are connected to the appropriate evaluation board terminals and not to the load or power sources.

If the voltmeters are not connected directly to the evaluation board, the measured voltages are incorrect due to the voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.

Connect the input voltage measuring voltmeter positive (+) terminal to the evaluation board at PVIN1_4 (J11). Connect the input voltage measuring voltmeter negative (−) terminal to the evaluation board at GND (J12).

To measure the output voltage of Buck 1, connect the output voltage measuring voltmeter positive (+) terminal to the evaluation board at VOUT1 (J16). Connect the output voltage measuring voltmeter negative (−) terminal to the evaluation board at GND (J15).
Quick Start

Ensure that the power source voltage for the buck regulators (PVIN1, PVIN2, PVIN3, PVIN4) is 4.5 V to 15.5 V. Shunt the S1, S2, and S3 jumpers to use the same input voltage for the buck regulators. Use the J-EN1, J-EN2, J-EN3, J-EN4 jumpers to enable or disable the desired channel.

Figure 2 shows the ADP5054 board connection diagram. When the power source and load are connected to the evaluation board, the board can be powered for operation. If the load is not enabled, enable the load. Verify that the evaluation board is drawing the proper current and that the output voltage maintains voltage regulation.

After power-up, measure the following output voltages:
- $V_{OUT1} = 1.2$ V, supply up to a 6 A output load
- $V_{OUT2} = 1.8$ V, supply up to a 6 A output load
- $V_{OUT3} = 1.5$ V, supply up to a 2.5 A output load
- $V_{OUT4} = 3.3$ V, supply up to a 2.5 A output load

Figure 2. ADP5054 Board Connection Diagram
MEASURING EVALUATION BOARD PERFORMANCE

MEASURING BUCK REGULATOR OUTPUT VOLTAGE RIPPLE

To observe the output voltage ripple of Buck 1, place an oscilloscope probe across the output capacitor (COUT_x) with the probe ground lead at the negative (−) capacitor terminal and the probe tip at the positive (+) capacitor terminal. Figure 3 shows the typical output ripple waveform.

Set the oscilloscope to ac, 10 mV/division, and 2 μs/division time base, with the bandwidth (BW) set to 20 MHz to avoid noise interfering with the measurements. To minimize coupling, shorten the ground loop of the oscilloscope probe. A good way of measuring the output voltage ripple is to solder a wire to the negative (−) capacitor terminal and wrap it around the barrel of the probe, while the tip directly connects to the positive (+) capacitor terminal as shown in Figure 4.

Typical PSM and FPWM switching waveforms are shown in Figure 5 and Figure 6.

MEASURING BUCK SWITCHING WAVEFORM

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the end of the inductor with the probe ground at GND. Set the oscilloscope to dc, 5 V/division, and 1 μs/division time base.

When the SYNC/MODE pin is set to high, the buck regulators operate in FPWM mode. When the SYNC/MODE pin is set to low, the buck regulators operate in PSM, which improves the light load efficiency.

MEASURING SYNCHRONIZATION INPUT OR OUTPUT

The SYNC/MODE pin can be configured as the clock output by setting the CFG34 pin. A clock is generated at the SYNC/MODE pin with the frequency equal to the internal frequency set by the RT pin.

When the SYNC/MODE pin is configured as the input, the ADP5054 can be synchronized to an external clock applied to the SYNC/MODE pin. The internal clock set by the RT pin must be programmed close to the external clock.
MEASURING BUCK LOAD REGULATION

Test the buck load regulation by increasing the load at the output and examining the change in output voltage. The input voltage must be held constant during this measurement. To minimize voltage drop, use short, low resistance wires, especially for loads approaching maximum current. Typical buck load regulation is shown in Figure 7.

![Figure 7. Buck Load Regulation](image)

MEASURING BUCK LINE REGULATION

To measure the buck line regulation, vary the input voltage and examine the change in the output voltage. Typical buck line regulation is shown in Figure 8.

![Figure 8. Buck Line Regulation](image)

MEASURING BUCK EFFICIENCY

Measure the efficiency, $\eta$, by comparing the input power with the output power.

$$\eta = \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{V_{\text{IN}} \times I_{\text{IN}}}$$

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of IR drops.

![Figure 9. Buck 1/Buck 2 Efficiency, VIN = 12 V, fSW = 600 kHz, MOSFET = SI7232DN, PSM and FPWM Mode](image)

MEASURING INDUCTOR CURRENT

Measure the inductor current by removing one end of the inductor from its pad and connecting a current loop in series. A current probe can be connected to this wire.
MODIFYING THE BOARD

SETTING THE BUCK OUTPUT VOLTAGE (CHANNEL 1 TO CHANNEL 4)

The buck output voltage is set through external resistor dividers, shown in Figure 10 for Buck 1. The output voltage can be factory programmed to default values, as indicated in the ADP5054 data sheet. Connect FB1 to the top of the capacitor on VOUT1 by placing a 0 Ω resistor on RTOP.

In the output adjustable version, the equation for the output voltage setting is

\[ V_{OUT} = V_{REF} \times \left( 1 + \frac{R_{TOP}}{R_{BOT}} \right) \]

where:
- \( V_{OUT} \) is the output voltage.
- \( V_{REF} \) is the 0.8 V feedback reference voltage.
- \( R_{TOP} \) is the feedback resistor from \( V_{OUT} \) to FB.
- \( R_{BOT} \) is the feedback resistor from FB to ground.

The \( V_{REF} \) voltage (FB1, FB2, FB3, FB4) for the buck regulators is 0.800 V in the adjustable version.

![Figure 10. Buck 1 External Output Voltage Setting](image)

When the output voltage of the bucks is changed, the values of inductors, the output capacitors, and the compensation networks must be recalculated and changed for stable operation. See the ADP5054 data sheet for more details on external components selection.

BUCK EXTERNAL RESISTOR DIVIDER SETTING

The ADP5054 evaluation board is supplied with the resistor divider for a target output voltage. Varying the resistor values of the resistor divider networks varies the output voltage accordingly. Table 3 shows the external resistor dividers for each channel.

Table 3. External Resistor Dividers in Each Channel

<table>
<thead>
<tr>
<th>Resistor Divider</th>
<th>Buck 1</th>
<th>Buck 2</th>
<th>Buck 3</th>
<th>Buck 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{TOP} )</td>
<td>R2</td>
<td>R4</td>
<td>R6</td>
<td>R5</td>
</tr>
<tr>
<td>( R_{BOT} )</td>
<td>R28</td>
<td>R29</td>
<td>R31</td>
<td>R30</td>
</tr>
</tbody>
</table>

CHANGING THE SWITCHING FREQUENCY

The switching frequency of the ADP5054 evaluation board is programmed to be 600 kHz. To change the switching frequency, replace the R3 resistor at the RT pin with a different value, as shown in Figure 11.

Program the external resistors on the CFG12 and CFG34 pins to set the channel switching frequency to half.

When the switching frequency is changed, the values of the inductors, the output capacitors, and the compensation networks must be recalculated and changed for stable operation. See the ADP5054 data sheet for more details.

CHANGING THE PEAK CURRENT-LIMIT THRESHOLD IN CHANNEL 1/CHANNEL 2

The peak current limit of the ADP5054 evaluation board in Channel 1 and Channel 2 is set to 10.4 A.

To change the peak current-limit threshold, replace the R8 resistor for Channel 1 (R7 for Channel 2) with a different value, as shown in Table 4. The programmable current-limit threshold feature allows the use of a small sized inductor for low current applications.

Table 4. Load Capability Settings on Channel 1 and Channel 2

<table>
<thead>
<tr>
<th>( \text{RILIM1/RILIM2} )</th>
<th>( I_{OUT} ) in Channel 1/Channel 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floating</td>
<td>4 A, with 6.9 A typical peak current limit</td>
</tr>
<tr>
<td>47 kΩ</td>
<td>2 A, with 3.8 A typical peak current limit</td>
</tr>
<tr>
<td>22 kΩ</td>
<td>6 A, with 10.4 A typical peak current limit</td>
</tr>
</tbody>
</table>

CHANGING THE SOFT START TIME

The soft start time of the ADP5054 on the evaluation board is programmed to be 2 ms for the buck regulators. To program a different soft start time, replace Resistors R16 and R39 for Channel 1 and Channel 2, respectively, and/or Resistors R40 and R18 for Channel 3 and Channel 4, respectively. See the ADP5054 data sheet for more details.
CONFIGURING CHANNEL 1/CHANNEL 2 AND CHANNEL 3/CHANNEL 4 AS 2-PHASE PARALLEL OUTPUTS

Channel 1 and Channel 2 are programmed as individual outputs in the ADP5054 evaluation board. Channel 3 and Channel 4 can be configured as individual outputs as well.

To configure Channel 1/Channel 2 as a 2-phase parallel output, the following steps are required:

1. Short the S4 jumper.
2. Change R39 = 400 kΩ and R16 = 300 kΩ (or R39 = 500 kΩ and R16 = 200 kΩ, or R39 = 600 kΩ and R16 = 100 kΩ) in the CFG12 pin setting.
3. Remove R17 and C8 from the COMP2 pin.
4. Remove R4, and replace R29 with 0 Ω on the FB2 pin.
5. Shunt the J-EN2 jumper to low.
6. Use the FB1 pin (R2 and R28) to set the output voltage.
7. Use the J-EN1 jumper (EN1 pin) to enable or disable the regulator.

To configure Channel 3/Channel 4 as a 2-phase parallel output, the following steps are required:

1. Short the S5 jumper.
2. Change R40 = 300 kΩ and R18 = 400 kΩ (or R40 = 400 kΩ and R18 = 300 kΩ, or R40 = 500 kΩ and R18 = 200 kΩ) in the CFG34 pin setting.
3. Remove R20 and C10 from the COMP4 pin.
4. Remove R5, and replace R30 with 0 Ω on the FB4 pin.
5. Shunt the J-EN4 jumper to low.
6. Use the FB3 pin (R6 and R31) to set the output voltage.
7. Use the J-EN3 jumper (EN3 pin) to enable or disable the regulator.

During the parallel configuration, the input voltage and the current-limit threshold for both channels are the same, and FPWM operation on Channel 1, Channel 2, Channel 3, and Channel 4 is recommended. See the ADP5054 data sheet for more details on configuring as a 2-phase parallel output.
EVALUATION BOARD SCHEMATIC AND ARTWORK

Figure 12. ADP5054 Evaluation Board Schematic
Figure 13. ADP5054 Evaluation Board Recommended Layout, Top Layer

Figure 14. ADP5054 Evaluation Board Recommended Layout, Layer 2
Figure 15. ADP5054 Evaluation Board Recommended Layout, Layer 3

Figure 16. ADP5054 Evaluation Board Recommended Layout, Bottom Layer
## ORDERING INFORMATION

### BILL OF MATERIALS

Table 5.

<table>
<thead>
<tr>
<th>Qty</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U1</td>
<td>Micropower management unit</td>
<td>Analog Devices, Inc.</td>
<td>ADP5054</td>
</tr>
<tr>
<td>1</td>
<td>U2</td>
<td>Dual metal oxide semiconductor field effect transistors, 7.2 mΩ</td>
<td>Infineon</td>
<td>BSC072N03</td>
</tr>
<tr>
<td>4</td>
<td>CIN_1, CIN_2, CIN_3, CIN_4</td>
<td>Multilayer ceramic chip capacitor, 10 μF, 25 V, 0805</td>
<td>Murata</td>
<td>GRM219R61E106KA12L</td>
</tr>
<tr>
<td>6</td>
<td>COUT_1, COUT_2, COUT_3, COUT_5, COUT_6, COUT_8</td>
<td>Multilayer ceramic chip capacitor, 47 μF, 6.3 V, 0805</td>
<td>Murata</td>
<td>GRM21BR60J476ME15</td>
</tr>
<tr>
<td>2</td>
<td>COUT_9, COUT_10, COUT_13, COUT_14</td>
<td>Multilayer ceramic chip capacitor, 47 μF, 6.3 V, 0805</td>
<td>Murata</td>
<td>GRM21BR60J476ME15</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>Inductor, 1.2 μH, 12.5 A</td>
<td>Coilcraft</td>
<td>XAL5030-122ME</td>
</tr>
<tr>
<td>1</td>
<td>L2</td>
<td>Inductor, 1.2 μH, 12.5 A</td>
<td>Coilcraft</td>
<td>XAL5030-122ME</td>
</tr>
<tr>
<td>1</td>
<td>L3</td>
<td>Inductor, 3.3 μH, 5.5 A</td>
<td>Coilcraft</td>
<td>XAL4030-332ME</td>
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<td>1</td>
<td>L4</td>
<td>Inductor, 3.3 μH, 5.5 A</td>
<td>Coilcraft</td>
<td>XAL4030-332ME</td>
</tr>
<tr>
<td>5</td>
<td>C1, C3, C4, C5</td>
<td>Multilayer ceramic chip capacitor, 0.1 μF, 16 V, 0402</td>
<td>Murata</td>
<td>GRM15SR71C104KA88D</td>
</tr>
<tr>
<td>4</td>
<td>C2, C14</td>
<td>Multilayer ceramic chip capacitor, 1 μF, 6.3 V, 0402</td>
<td>Murata</td>
<td>GRM15SR60J105KE19D</td>
</tr>
<tr>
<td>2</td>
<td>C7, C8</td>
<td>Multilayer ceramic chip capacitor, 1 nF, 50 V, 0402</td>
<td>Murata</td>
<td>GRM15SR61H102KA01D</td>
</tr>
<tr>
<td>2</td>
<td>C9, C10</td>
<td>Multilayer ceramic chip capacitor, 2.7 nF, 50 V, 0402</td>
<td>Murata</td>
<td>GRM2165SC1H272JA01D</td>
</tr>
<tr>
<td>1</td>
<td>R2</td>
<td>Resistor, 4.99 kΩ, 1%, 0402</td>
<td>Panasonic</td>
<td>ERJ-2RKF4991X</td>
</tr>
<tr>
<td>1</td>
<td>R3</td>
<td>Resistor, 32.4 kΩ, 1%, 0402</td>
<td>Panasonic</td>
<td>ERJ-2RKF2322X</td>
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<tr>
<td>1</td>
<td>R4</td>
<td>Resistor, 12.4 kΩ, 1%, 0402</td>
<td>Vishay</td>
<td>CRCW040231K6F</td>
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<tr>
<td>1</td>
<td>R5</td>
<td>Resistor, 31.2 kΩ, 1%, 0402</td>
<td>Vishay</td>
<td>CRCW040252K3F</td>
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<tr>
<td>1</td>
<td>R6</td>
<td>Resistor, 8.75 kΩ, 1%, 0402</td>
<td>Panasonic</td>
<td>ERJ-2RKF1242X</td>
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<tr>
<td>2</td>
<td>R7, R8</td>
<td>Resistor, 22 kΩ, 1%, 0402</td>
<td>Panasonic</td>
<td>ERJ-2GEJ223X</td>
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<tr>
<td>1</td>
<td>R17</td>
<td>Resistor, 20 kΩ, 1%, 0402</td>
<td>Panasonic</td>
<td>ERJ-2RKF2002X</td>
</tr>
<tr>
<td>2</td>
<td>R12, R15</td>
<td>Resistor, 10 kΩ, 1%, 0603</td>
<td>Vishay</td>
<td>CRCW060310K0F</td>
</tr>
<tr>
<td>1</td>
<td>R20</td>
<td>Resistor, 51 kΩ, 1%, 0402</td>
<td>Panasonic</td>
<td>ERJ-2RKF2402</td>
</tr>
<tr>
<td>2</td>
<td>R39, R40</td>
<td>Resistor, 0 Ω, 1%, 0402</td>
<td>Panasonic</td>
<td>ERJ-2GE0R00X</td>
</tr>
<tr>
<td>2</td>
<td>D2</td>
<td>LED, 0603</td>
<td>Panasonic</td>
<td>LNJ208B403A</td>
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<tr>
<td>5</td>
<td>J-EN1, J-EN2, J-EN3, J-EN4, J-SYNC</td>
<td>3-pin header</td>
<td>Samtec</td>
<td>TSW-103-08-G-S</td>
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<tr>
<td>15</td>
<td>J11, J12, J15, J16, J17, J18, J19, J20, J21, J22, S1, S2, S3, S4, S5</td>
<td>2-pin header</td>
<td>Samtec</td>
<td>TSW-150-07-T-S</td>
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<td>8</td>
<td>TP9, TP10, TP11, VREG, PWRGD_A0</td>
<td>Test point, 1206</td>
<td>MAC8</td>
<td>HK-1-G</td>
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<tr>
<td>6</td>
<td>COUT_4, COUT_11, COUT_12, COUT_15, COUT_7, COUT_16</td>
<td>No assembly</td>
<td>No assembly</td>
<td>No assembly</td>
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## RELATED LINKS

<table>
<thead>
<tr>
<th>Resource</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADP5054</td>
<td>4-channel integrated power solution with quad buck regulator</td>
</tr>
</tbody>
</table>
NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the “Evaluation Board”), you are agreeing to be bound by the terms and conditions set forth below (“Agreement”) unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you (“Customer”) and Analog Devices, Inc. (“ADI”), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term “Third Party” includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED “AS IS” AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER’S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOSS PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI’S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

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