

Introduction

The ADuC7039 belongs to the second generation of battery sensor from ADI. It is a simplified version, or low cost version, of the ADuC7033. Some features present on the ADuC7033, such as UART and STI, have been removed and others have been simplified.

To migrate from the ADuC7033 to the ADuC7039, a number of hardware and software changes need to be addressed. This document describes an overview of those changes. ADI recommends that the datasheets of both devices should be reviewed in detail before starting your design.

ADuC7033/39 main differences

The following features are in the ADuC7033 but **NOT** in the ADuC7039

- STI
- BSD
- UART
- Timer 3
- Timer 4
- High voltage WU
- PSM
- External interrupt
- External crystal
- External Reference
- 3 GPIO pins less

Any user code, which currently accesses any of these peripherals should be removed from the application software.

There are other modified or simplified features that will affect user hardware and software:

- Package and pin out
- Interrupt controller
- System control
- Timers
- System Clock
- Flash interface
- ADCs
- LIN
- GPIO port
- High voltage interface and registers
- Core and JTAG interface
- Kernel

Package and pinout

The ADuC7039 has a smaller package and different pinout as can be seen from both pin-outs below, in Figure 1 and Figure 2.

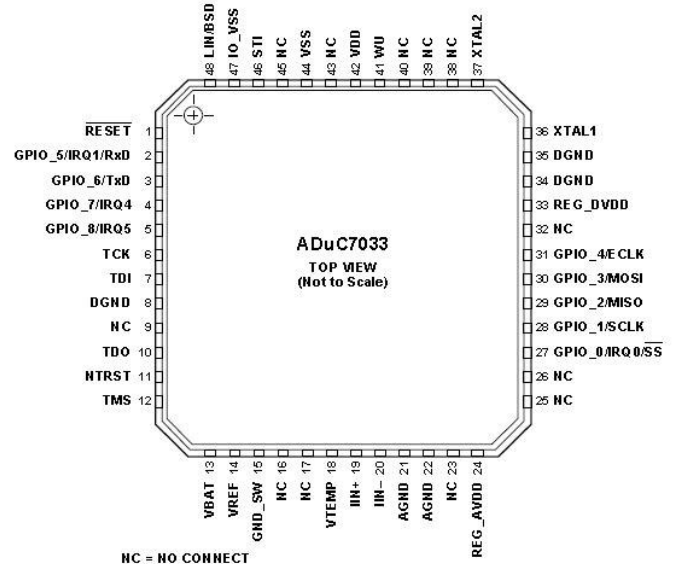


Figure 1. ADuC7033

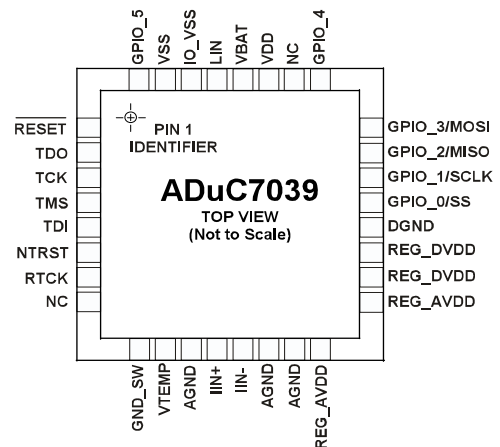
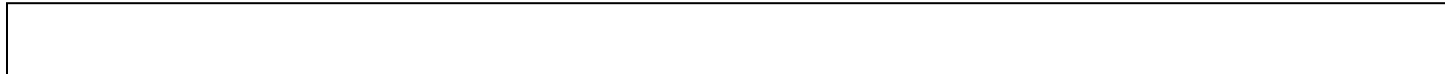


Figure 2. 32-Lead Lead Frame Chip Scale package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad



Interrupt Controller

On both devices, the interrupt controller MMRs are at the same addresses but the bit designations of these MMRs are different.

Table 1. IRQ/FIQ MMRs Bit Designations

Bit	ADuC7033	ADuC7039
0	All interrupts OR'ed	All interrupts OR'ed
1	SWI	SWI
2	Timer0	Timer0
3	Timer1	Timer1 / Wake-up timer
4	Timer2 / Wake-up	Timer2 / Watchdog
5	Timer3 / Watchdog	LIN
6	Timer4 or STI timer	Flash/EE interrupt
7	LIN Hardware	PLL lock
8	Flash/EE interrupt	ADC
9	PLL lock	SPI
10	ADC	High Voltage
11	UART	Low Power Osc
12	SPI master	Reserved
13	XIRQ0 (GPIO IRQ0)	Reserved
14	XIRQ1 (GPIO IRQ1)	Reserved
15	Reserved	Reserved
16	IRQ3 /High voltage	Reserved
17	SPI slave	Reserved
18	XIRQ4 (GPIO IRQ4)	Reserved
19	XIRQ5 (GPIO IRQ5)	Reserved
20 to 31	Reserved	Reserved

System control

The SYSCHK MMR holds the kernel checksum at power up. It was located at address 0xFFFF0240 on the ADuC7033. It is now located at address 0xFFFF0244 on the ADuC7039.

For traceability, three dedicated MMRs were provided on the ADuC7033: SYSSER0, SYSSER1 and SYSALI. T1LD was also used for storing the Assembly lot ID.

On the ADuC7039, 4 internal ARM registers are used at power up: R4, R5, R6 and R7. This means that user startup code needs to store these four 32-bit values before executing initialisation code. FEE0ADR in the ADuC7033, which holds the Model information of the part, is also changed to FEEADR for the ADuC7039.

Timers

The ADuC7033 has 5 timers: T0, T1, T2 or wake up timer, T3 or watchdog timer and T4.

The ADuC7039 has three timers T0, T1 or wake up timer and T2 or watchdog timer.

T2 (watchdog timer) is similar to T3 of the ADuC7033. MMR locations, bit designations, and functionality remain the same. The clock for the Watchdog is 32,000Hz for the ADuC7039, while the ADuC7033 is 32,768Hz

The functionalities, MMR locations and bit definitions of T0 and T1 (wake up timer) have been modified. See datasheet for details.

System Clock

The PLL has three clock sources on the ADuC7033: external crystal, low power oscillator or precision oscillator. These options are reduced to two on the ADuC7039: low power oscillator or precision oscillator.

The bit designations of PLLSTA, PLLCON and POWCON MMRs have been changed. See datasheet for details.

Clock frequency:

The clock frequency of the oscillators has been changed from 131.072 kHz on the ADuC7033 to 128kHz on the ADuC7039.

The precision oscillator is now located on the low voltage die and doesn't need to be configured via the high voltage interface. It is enabled in the PLLCON MMR.

The low power oscillator is not factory calibrated and needs to be calibrated at the customer end of line using the low power clock calibration scheme. This feature is similar to the ADuC7033 with the following differences: OSCOTRM MMR has been renamed LOCUSR0, and is now located at address 0xFFFF0484. This MMR is now write-protected by a key, LOCKEY at address 0xFFFF04A0.

ADCs

The following features are removed:

- Low power mode has been removed and low power plus mode has been renamed low power mode.
- The independent data register for the temperature channel conversion results has been removed. The voltage conversion and temperature conversion results are sharing the same ADC1DAT MMR. This directly affects user code.
- The self calibration of the two ADCs is removed.
- The low power reference and low power reference scaling factor MMR, ADCREF, are removed.
- The IADC threshold count (ADC0THV) and threshold count limit (ADC0TCL) features are removed.

This means that the bit designations in the following MMRs have been modified:

ADCSTA, ADCMDE, ADC0CON, ADC1CON, ADCCFG.

The system calibration sequence has been improved; there is no need to place the ADC in idle mode to write in the calibration MMRs

LIN

The LIN physical driver is enabled on the high voltage interface on the ADuC7039 in the same manner than on the ADuC7033. Note that the HVCFG register bit designation has changed.

The LIN interface on the low voltage die has been completely redesigned and simplified. See datasheet for details.

GPIO

Only 6 GPIO pins are available on the ADuC7039 and they are grouped in one port. They are controlled by 4 MMRs.

Flash interface

On the ADuC7033, a signature command was available to the user to the Flash contents. This signature always includes the kernel contents.

On the ADuC7039, this feature has been modified to be more flexible: it is possible to specify the start page and end page of the Flash to be signed.

The kernel uses this feature to calculate the CRC of page 0. Note that page 0 CRC should now be stored at address **0x1FC** instead of address **0x14**. See kernel section in the datasheet.

High voltage interface and registers

The high voltage interface remains the same and the read/write routine used on the ADuC7033 can be used on the ADuC7039.

The number of features on the high voltage die has been reduced and less registers are necessary to configure and monitor the high voltage features on the ADuC7039.

- There are 4 indirect registers on the ADuC7033: HVCFG0, HVCFG1, HVSTA and HVMON.
- There are 2 indirect registers on ADuC7039: HVCFG and HVSTA.

The read/write of HVMON and HVCFG1 registers commands in the HVCON MMR are removed.

The HVCFG and HVSTA registers have a new bit designation. See datasheet.

Core and JTAG Interface

The ADuC7033 integrates an ARM7TDMI Rev 3 core. The ADuC7039 integrates an ARM7TDMI-S Rev 4 core: The JTAG interface includes the RTCK signal and a multi-tap architecture. The JTAG tools need to be updated.

Kernel

The decision to either enter download mode or execute user code is based on the level on NTRST and the contents of address 0x14 on the ADuC7033. On the ADuC7039, it is based on NTRST pin and contents of address 0x1FC.